# ELECTRONIC CIRCUITS-I

# About the Authors

**S Salivahanan** is the Principal of SSN College of Engineering, Chennai. He obtained his B.E. in Electronics and Communication Engineering from PSG College of Technology, Coimbatore; M.E. degree in Communication Systems from NIT, Trichy; and Ph.D. in the area of Microwave Integrated Circuits from Madurai Kamaraj University. He has four decades of teaching, research, administration and industrial experience, both in India and abroad. He has taught at NIT, Trichy; A.C. College of Engineering and Technology, Karaikudi; R.V. College of Engineering, Bangalore; Mepco Schlenk Engineering College, Sivakasi. He has industrial experience as Scientist/Engineer at Space Applications Centre, ISRO, Ahmedabad; Telecommunication Engineer at State Organisation of Electricity, Iraq; and Electronics Engineer at Electric Dar Establishment, Kingdom of Saudi Arabia.

He is the author of 45 popular textbooks which include Basic Electrical and Electronics Engineering, Electronic Devices and Circuits, Linear Integrated Circuits, and Digital Signal Processing by McGraw-Hill Education (India), which has also been translated into Mandarin, the Chinese language, outside India by McGraw Hill. He has also authored the books on Digital Circuits and Design, Electromagnetic Field Theory, Circuit Theory, Network Analysis and Synthesis and Control Systems Engineering. He has published several papers at national and international levels.

Professor Salivahanan is the recipient of Bharatiya Vidya Bhavan National Award for Best Engineering College Principal for 2011 from ISTE, and IEEE Outstanding Branch Counsellor and Advisor Award in the Asia-Pacific region for 1996–97. He was the Chairman of IEEE Madras Section for two years, 2008 and 2009, and Syndicate Member of Anna University.

He is a senior member of IEEE, fellow of IETE, fellow of Institution of Engineers (India), life member of ISTE and life member of Society for EMC Engineers. He is also a member of IEEE Societies in Microwave Theory and Techniques, Communications, Signal Processing, and Aerospace and Electronics

**N Suresh Kumar** is the Principal of SNS College of Engineering, Coimbatore. He received his Bachelor's degree in Electronics and Communication Engineering from Thiagarajar College of Engineering, Madurai (Tamil Nadu); M.E. degree in Microwave and Optical Engineering from A.C. College of Engineering Technology, Karaikudi (Tamil Nadu); and Ph.D. in the field of EMI/EMC from Madurai Kamaraj University, Madurai (Tamil Nadu). He has over two and a half decades of teaching, administration and research experience and has authored several blockbuster titles published by McGraw-Hill Education (India).

He has published and presented many research papers in international journals and conferences. His areas of interest include Electromagnetic Interference and Compatibility, Microwave Communication and Optical Communication. He has completed research projects funded by DRDO and DST.

Professor Suresh Kumar is the recipient of Eminent Engineer Award from the Institution of Engineers (India). He is a member of IEEE, fellow of IETE, fellow of Institution of Engineers (India) and, life member in ISTE, Society of EMC Engineers, Institute for Smart Structures and Systems and Broadcast Engineering Society. He was a member of Academic Council of Anna University Tirunelveli. He is a member of Board of Studies of Anna University, Chennai.

# ELECTRONIC CIRCUITS-I

**S Salivahanan**
*Principal*
*SSN College of Engineering*
*Chennai, Tamil Nadu*

**N Suresh Kumar**
*Principal*
*Velammal College of Engineering and Technology*
*Madurai, Tamil Nadu*


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# PREFACE

Electronic Circuits is designed specifically to cater to the needs of second year students of B.E. in Electronics and Communication Engineering. The book has a perfect blend of focused content and complete coverage. Simple, easy-to-understand and difficult-jargon-free text elucidates the fundamentals of electronics. Several solved examples, circuit diagrams and adequate questions further help students understand and apply the concepts.

The book will serve the purpose of a text to the engineering students of degree, diploma, AIME and graduate IETE courses and as a useful reference for those preparing for competitive examinations. Also, it will meet the pressing needs of interested readers who wish to gain a sound knowledge and understanding of the principles of electronic devices. Practicing engineers will find the content of significant relevance in their day-to-day functioning.

The book contains five chapters. Chapter 1 discusses Biasing of Discrete BJT, JFET and MOSFET, Chapter 2 explains BJT Amplifiers, Chapter 3 is devoted to Single Stage FET and MOSFET Amplifiers, Chapter 4 deals with Frequency Response of Amplifiers, Chapter 5 describes Power Supplies and Electronic Device Testing.

All the topics have been profusely illustrated with diagrams for better understanding. Equal emphasis has been laid on mathematical derivations as well as their physical interpretations. Illustrative examples are discussed to emphasize the concepts and typical applications. Review questions and exercises have been given at the end of each chapter with a view to help the readers increase their understanding of the subject and to encourage further reading.

We are highly indebted to the management of our institutions for encouraging us from time to time and providing all the necessary facilities. Thanks are due to our colleagues, especially Mr. S. Karthie, Assistant Professor and Dr. K.K. Nagarajan, Associate Professor, Department of ECE, SSNCE for their valuable suggestions and useful comments in the preparation of the manuscript. My thanks are also due to Mr. R. Gopalakrishnan, Mr. K. Rajan and Mr. S. Sankar Kumar for efficiently word processing the manuscript.

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Constructive suggestions and corrections for the improvement of the book would be most welcome and highly appreciated.

**S SALIVAHANAN**

**N SURESH KUMAR**

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CHAPTER

# 1 Biasing of Discrete BJT, JFET and MOSFET

## 1.1 INTRODUCTION

A Bipolar Junction Transistor (BJT) is a three-terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and, hence, the name *bipolar*. The BJT is analogous to a vacuum triode and is comparatively smaller in size. It is used in amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites, and other modern communication systems.

The FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence, the name Field Effect Transistor (FET). As current conduction is only by majority carriers, FET is said to be a unipolar device.

Based on the construction, the FET can be classified into two types as *Junction FET (JFET)* and *Metal Oxide Semiconductor FET (MOSFET)* or *Insulated Gate FET (IGFET)* or *Metal Oxide Silicon Transistor (MOST)*.

Depending upon the majority carriers, JFET has been classified into two types, namely, (i) *N-channel JFET* with electrons as the majority carriers, and (ii) *P-channel JFET* with holes as the majority carriers.

The quiescent operating point of a transistor amplifier should be established in the active region of its characteristics. Since the transistor parameters such as $\beta$, $I_{CO}$, and $V_{BE}$ are functions of temperature, the operating point shifts with changes in temperature. The stability of different methods of biasing transistor (BJT, FET, and MOSFET) circuits and compensation techniques for stabilizing the operating point are discussed in this chapter.

## 1.2 NEED FOR BIASING

In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chosen. These voltages and resistances establish a set of dc voltage $V_{CEQ}$ and current $I_{CQ}$ to operate the transistor in the active region. These voltages and currents are called *quiescent values* which determine the *operating point* or *Q*-point for the transistor. The process of giving proper supply voltages and resistances for obtaining the desired *Q*-point is called *biasing*. The circuits used for getting the desired and proper operating point are known as *biasing circuits*.

The collector current for a common-emitter amplifier is expressed by

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1 + \beta) I_{CO}$$

Here, the three variables $h_{FE}$, i.e., $\beta$, $I_B$, and $I_{CO}$ are found to increase with temperature. For every 10°C rise in temperature, $I_{CO}$ doubles itself. When $I_{CO}$ increases, $I_C$ increases significantly. This causes power dissipation to increase and hence, to make $I_{CO}$ increase. This will cause $I_C$ to increase further and the process becomes cumulative which will lead to thermal runaway that will destroy the transistor. In addition, the quiescent operating point can shift due to temperature changes and the transistor can be driven into the region of saturation. The effect of $\beta$ on the $Q$-point is shown in Fig. 1.1. One more source of bias instability to be considered is due to the variation of $V_{BE}$ with temperature. $V_{BE}$ is about 0.6 V for a silicon transistor and 0.2 V for a germanium transistor at room temperature. As the temperature increases, $|V_{BE}|$ decreases at the rate of 2.5 mV/°C for both silicon and germanium transistors. The transfer-characteristic curve shifts to the left at the rate of 2.5 mV/°C (at constant $I_C$) for increasing temperature and, hence, the operating point shifts accordingly. To establish the operating point in the active region, compensation techniques are needed.

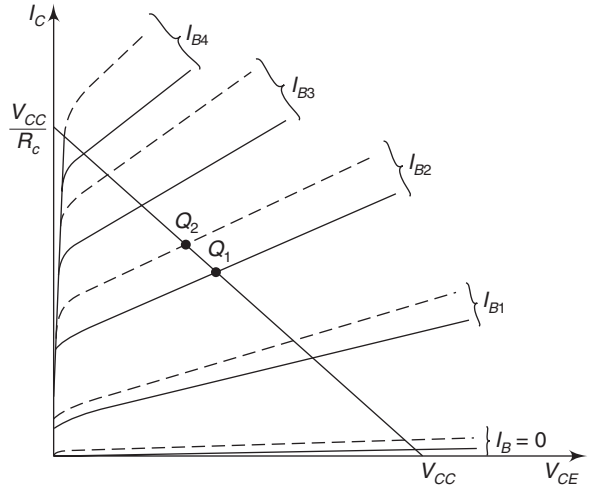



**Fig. 1.1** *Effect of $\beta$ on Q-point*

## 1.3 DC LOAD LINE AND BIAS POINT

Referring to the biasing circuit of Fig. 1.2(a), the values of $V_{CC}$ and $R_C$ are fixed and $I_C$ and $V_{CE}$ are dependent on $R_B$.

Applying Kirchhoff's voltage law to the collector circuit in Fig. 1.2(a), we get $V_{CC} = I_C R_C + V_{CE}$.

The straight line represented by *AB* in Fig. 1.2(b) is called the dc *load line*. The coordinates of the end point *A* are obtained by substituting $V_{CE} = 0$ in the above equation. Then $I_C = \frac{V_{CC}}{R_C}$. Therefore, the coordinates of *A* are $V_{CE} = 0$ and $I_C = \frac{V_{CC}}{R_C}$.

The coordinates of $B$ are obtained by substituting $I_C = 0$ in the above equation. Then $V_{CE} = V_{CC}$. Therefore, the coordinates of $B$ are $V_{CE} = V_{CC}$ and $I_C = 0$. Thus, the dc load line $AB$ can be drawn if the values of $R_C$ and $V_{CC}$ are known.

As shown in Fig. 1.2(b), the optimum $Q$-point is located at the midpoint of the dc load line $AB$ between the saturation and cut-off regions, i.e., $Q$ is exactly midway between $A$ and $B$. In order to get faithful amplification, the $Q$-point must be well within the active region of the transistor.

Even though the $Q$-point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the $Q$-point shifts nearer to either $A$ or $B$, the output voltage and current get clipped, thereby output signal is distorted.

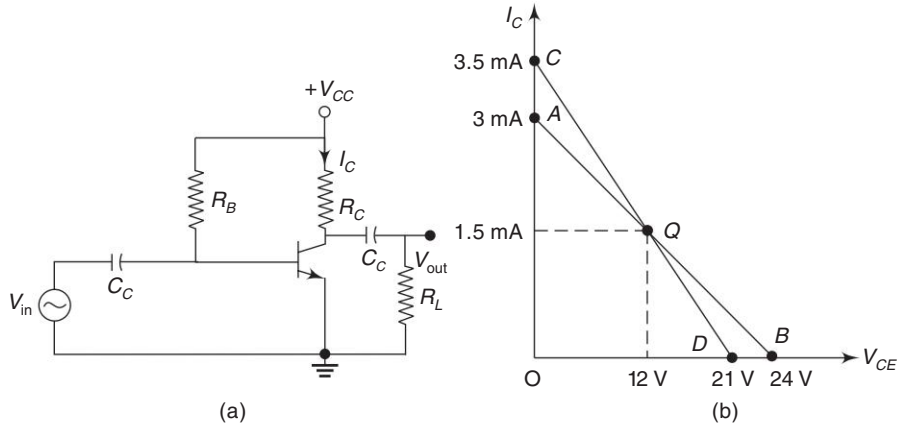



**Fig. 1.2** *(a) Biasing circuit (b) CE output characteristics and load line*

In practice, the $Q$-point tends to shift its position due to any or all of the following three main factors:

(i) Reverse saturation current, $I_{CO}$, which doubles for every 10 °C increase in temperature.
(ii) Base-emitter voltage, $V_{BE}$, which decreases by 2.5 mV per °C.
(iii) Transistor current gain, $\beta$, i.e., $h_{FE}$ which increases with temperature.

Referring to Fig. 1.2(a), the base current $I_B$ is kept constant since $I_B$ is approximately equal to $V_{CC}/R_B$. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as $\beta$ vary over a range. This results in the variation of collector current $I_C$ for a given $I_B$. Hence, in the output characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the $Q$-point to a location which might be completely unsatisfactory.

## 1.4 AC LOAD LINE

After drawing the dc load line, the operating point $Q$ is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence, the ac load line should also pass through the operating point $Q$. The effective ac load resistance, $R_{ac}$, is the combination of $R_C$ parallel to $R_L$, i.e., $R_{ac} = R_C \| R_L$. So the slope of the ac load line $CQD$ will be $\left(-\frac{1}{R_{a.c.}}\right)$.

To draw an ac load line, two end points, viz., maximum $V_{CE}$ and maximum $I_C$ when the signal is applied are required.

Maximum $V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$, which locates the point $D(OD)$ on the $V_{CE}$ axis.

Maximum $I_C = I_{CQ} + \dfrac{V_{CEQ}}{R_{a.c.}}$, which locates the point $C\ (OC)$ on the $I_C$ axis.

By joining points $C$ and $D$, ac load line $CD$ is constructed. As $R_C > R_{ac}$, the dc load line is less steep than the ac load line.

When the signal is zero, we have the exact dc conditions. From Fig. 1.2(b), it is clear that the intersection of dc and ac load lines is the operating point $Q$.

***Voltage Swing Limitations*** In a linear amplifier, symmetrical sinusoidal signals at the input gets amplified as sinusoidal signal at the output, without any clipping. The maximum output symmetrical swing provided by the amplifier can be obtained from the ac load line. The output signal will be clipped if it exceeds this limit, resulting in signal distortion.

## EXAMPLE 1.1

Determine the maximum voltage swing at the output of common emitter amplifier in which the quiescent point is $I_{CQ} = 0.9$ mA and $V_{CEQ} = 9$ V. The ac resistance seen at the output terminal is $R_{ac} = (R_C \parallel R_L) = 2\text{k}\Omega$.

**Solution** The maximum symmetrical peak to peak ac collector current is

$$\Delta i_C = 2\, I_{CQ} = 2 \times 0.9 \text{ mA} = 1.8 \text{ mA}$$

The maximum symmetrical peak to peak output voltage is

$$\left|\Delta v_{EC}\right| = \left|\Delta i_C\right| R_{ac} = 1.8 \times 10^{-3} \times 2 \times 10^{-3} = 3.6 \text{ V}$$

## EXAMPLE 1.2

In the transistor amplifier shown in Fig. 1.2(a), $R_C = 8\ \text{k}\Omega$, $R_L = 24\ \text{k}\Omega$ and $V_{CC} = 24$ V. Draw the dc load line and determine the optimum operating point. Also draw the ac load line.

**Solution**

(a) *dc load line:* Referring to Fig. 1.2(a), we have $V_{CC} = V_{CE} + I_C R_C$.
For drawing the dc load line, the two end points, viz., maximum $V_{CE}$ point (at $I_C = 0$) and maximum $I_C$ point (at $V_{CE} = 0$) are required.

Maximum $\quad V_{CE} = V_{CC} = 24$ V

Maximum $\quad I_C = \dfrac{V_{CC}}{R_C} = \dfrac{24}{8 \times 10^3} = 3$ mA

Therefore, the dc load line $AB$ is drawn with the point $B$ ($OB = 24$ V) on the $V_{CE}$ axis and the point $A$ ($OA = 3$ mA) on the $I_C$ axis, as shown in Fig. 1.2(b).

(b) For fixing the optimum operating point $Q$, mark the middle of the dc load line $AB$ and the corresponding $V_{CE}$ and $I_C$ values can be found.

Here, $\quad V_{CEQ} = \dfrac{V_{CC}}{2} = 12$ V $\quad$ and $\quad I_{CQ} = 1.5$ mA

(c) *ac load line:* To draw an ac load line, two end points, viz., maximum $V_{CE}$ and maximum $I_C$ when the signal is applied, are required.

The ac load, $R_{ac} = R_C \| R_L = \dfrac{8 \times 24}{8 + 24} = 6\ \text{k}\Omega$

Maximum $V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$

$= 12 + 1.5 \times 10^{-3} \times 6 \times 10^{3} = 21\ \text{V}$

This locates the point $D$ ($OD = 21$ V) on the $V_{CE}$ axis.

Maximum collector current $= I_{CQ} + \dfrac{V_{CEQ}}{R_{ac}} = 1.5 \times 10^{-3} + \dfrac{12}{6 \times 10^{3}} = 3.5\ \text{mA}$

This locates the point $C$ ($OC = 3.5$ mA) on the $I_C$ axis. By joining points $C$ and $D$, the ac load line $CD$ is constructed.

## EXAMPLE 1.3

For the transistor amplifier shown in Fig. 1.3(a), $V_{CC} = 12$ V, $R_1 = 8$ kΩ, $R_2 = 4$ kΩ, $R_C = 1$ kΩ, $R_E = 1$ kΩ and $R_L = 1.5$ kΩ. Assume $V_{BE} = 0.7$ V. (a) Draw the dc load line, (b) determine the operating point, and (c) draw the ac load line.

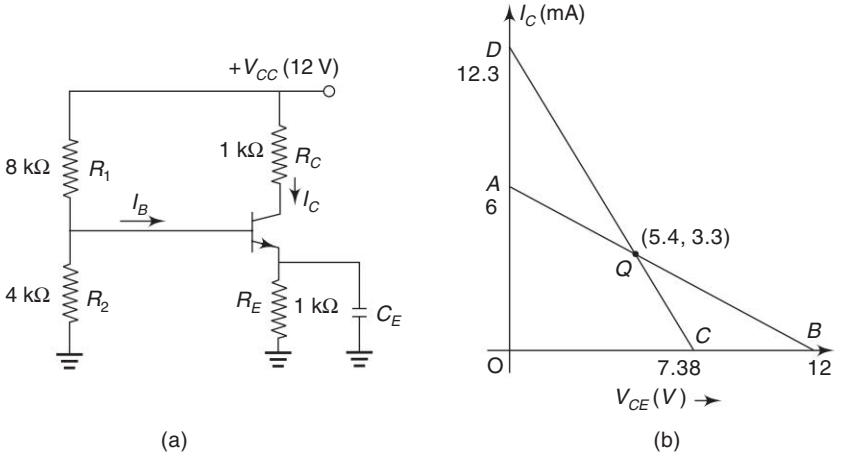
### Solution

(a) *dc load line:* Referring to Fig. 1.3(a), we have $V_{CC} = V_{CE} + I_C (R_C + R_E)$.
To draw the dc load line, we need two end points, viz., maximum $V_{CE}$ point (at $I_C = 0$) and maximum $I_C$ point (at $V_{CE} = 0$).

Maximum $V_{CE} = V_{CC} = 12$ V, which locates the point $B$ ($OB = 12$ V) of the dc load line.

Maximum $I_C = \dfrac{V_{CC}}{R_C + R_E} = \dfrac{12}{(1+1) \times 10^{3}} = 6\ \text{mA}$

This locates the point $A$ ($OA = 6$ mA) of the dc load line. Figure 1.3(b) shows the dc load line $AB$, with (12 V, 6 mA).




(a) (b)

**Fig. 1.3**

(b) *Operating point Q*

The voltage across $R_2$ is $V_2 = \dfrac{R}{R_1 + R_2} V_{CC}$

Therefore, $V_2 = \dfrac{4 \times 10^3}{12 \times 10^3} \times 12 = 4 \text{ V}$

$V_2 = V_{BE} + I_E R_E$

Therefore, $I_E = \dfrac{V_2 - V_{BE}}{R_E} = \dfrac{4 - 0.7}{1 \times 10^3} = 3.3 \text{ mA}$

$I_C \approx I_E = 3.3 \text{ mA}$

$V_{CE} = V_{CC} - I_C (R_C + R_E) = 12 - 3.3 \times 10^{-3} \times 2 \times 10^3 = 5.4 \text{ V}$

Therefore, the operating point $Q$ is at 5.4 V and 3.3 mA, which is shown on the dc load line.

(c) *ac load line:* To draw the ac load line, we need two end points, viz., maximum $V_{CE}$ and maximum $I_C$ when signal is applied.

ac load, $R_{ac} = R_C \parallel R_L = \dfrac{1 \times 1.5\text{k}\Omega}{2.5} = 0.6 \text{ k}\Omega$

Therefore, maximum $V_{CE} = V_{CEQ} + I_{CQ} R_{ac} = 5.4 + 3.3 \times 10^{-3} \times 0.6 \times 10^3 = 7.38 \text{ V}$

This locates the point $C$ ($OC = 7.38$ V) on the $V_{CE}$ axis.

Maximum $I_C = I_{CQ} + \dfrac{V_{CEQ}}{R_{ac}} = 3.3 \times 10^{-3} + \dfrac{5.4}{0.6 \times 10^3} = 12.3 \text{ mA}$

This locates the point $D$ ($OD = 12.3$ mA) on the $I_C$ axis. By joining points $C$ and $D$, the ac load line $CD$ is constructed.

## EXAMPLE 1.4

Design the circuit shown in Fig. 1.4, given Q-point values are to be $I_{CQ} = 1$ mA and $V_{CEQ} = 6$ V. Assume that $V_{CC} = 10$ V, $\beta = 100$ and $V_{BE\,(on)} = 0.7$ V.

**Solution** The collector resistance is

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{10 - 6}{1 \times 10^{-3}} = 4 \text{ k}\Omega$$

The base current is

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1 \times 10^{-3}}{100} = 10 \text{ μA}$$

The base resistance is

$$R_B = \frac{V_{CC} - V_{BE(on)}}{I_{BQ}} = \frac{10 - 0.7}{10 \times 10^{-6}} = 0.93 \text{ M}\Omega$$

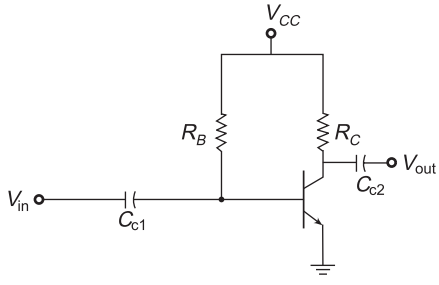



**Fig. 1.4**

## EXAMPLE 1.5

Determine the characteristics of a circuit shown in Fig. 1.5. Assume that $\beta = 100$ and $V_{BE\,(on)} = 0.7$ V.

**Solution** Referring to Fig. 1.5, Kirchhoff's voltage law equation is

$$V_{BB} = I_B R_B + V_{BE\,(on)} + I_E R_E$$

We know that

$$I_E = I_B + I_C = I_B + \beta I_B = (1 + \beta) I_B$$

The base current $I_B = \dfrac{V_{BB} - V_{BE(on)}}{R_B + (1 + \beta) R_E}$

$$= \frac{5 - 0.7}{20 \times 10^3 + 101 \times 600} = 53.34\ \mu\text{A}$$

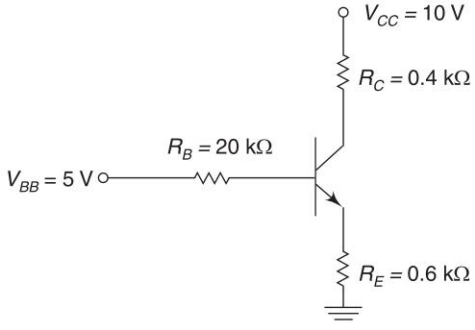



**Fig. 1.5**

Therefore, $I_C = \beta I_B = 100 \times 53.34 \times 10^{-6}$

$$= 5.334\ \text{mA}$$

$$I_E = I_C + I_B = 5.334 \times 10^{-3} + 53.34 \times 10^{-6}$$

$$= 5.38734\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 10 - 5.334 \times 10^{-3} \times 400 - 5.38734 \times 10^{-3} \times 600 = 4.634\ \text{V}$$

The $Q$ point is at $V_{CEQ} = 4.634$ V and $I_{CQ} = 5.334$ mA

## 1.5 THERMAL RUNAWAY

The collector current for the CE circuit of Fig. 1.2 is given by $I_C = \beta I_B + (1 + \beta)\, I_{CO}$. The three variables in the equation, $\beta$, $I_B$, and $I_{CO}$ increase with rise in temperature. In particular, the reverse saturation current or leakage current $I_{CO}$ changes greatly with temperature. Specifically, it doubles for every 10 °C rise in temperature. The collector current $I_C$ causes the collector-base junction temperature to rise which, in turn, increase $I_{CO}$, as a result $I_C$ will increase still further, which will further raise the temperature at the collector-base junction. This process will become cumulative leading to *thermal runaway*. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is normally made larger in size than the emitter in order to help dissipate the heat developed at the collector junction.

However, if the circuit is designed such that the base current $I_B$ is made to decrease automatically with rise in temperature then the decrease in $\beta I_B$ will compensate for the increase in $(1 + \beta) I_{CO}$, keeping $I_C$ almost constant.

In power transistors, the heat developed at the collector junction may be removed by the use of a heat sink, which is a metal sheet fitted to the collector and whose surface radiates heat quickly.

## 1.6 STABILITY FACTOR (*S*)

The extent to which the collector current $I_C$ is stabilized with varying $I_{CO}$ is measured by a stability factor $S$. It is defined as the rate of change of collector current $I_C$ with respect to the collector-base leakage current $I_{CO}$, keeping both the current $I_B$ and the current gain $\beta$ constant.

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \beta \text{ and } I_B \text{ constant} \tag{1.1}$$

The collector current for a CE amplifier is given by

$$I_C = \beta I_B + (\beta + 1) I_{CO} \tag{1.2}$$

Differentiating the above equation with respect to $I_C$, we get

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

Therefore, $$\left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta + 1)}{S}$$

$$S = \frac{1 + \beta}{1 - \beta\left(\frac{dI_B}{dI_C}\right)} \tag{1.3}$$

From this equation, it is clear that this factor $S$ should be as small as possible to have better thermal stability.

***Stability Factors S′ and S″*** The stability factor $S'$ is defined as the rate of change of $I_C$ with $V_{BE}$, keeping $I_{CO}$ and $\beta$ constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

The stability factor $S''$ is defined as the rate of change of $I_C$ with respect to $\beta$, keeping $I_{CO}$ and $V_{BE}$ constant.

$$S'' = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta}$$

## 1.7 DC ANALYSIS AND BIASING METHODS OF BJT

The stability factors for some commonly used biasing circuits are discussed here.

### 1.7.1 Fixed Bias or Base Resistor Method

A common-emitter amplifier using a fixed-bias circuit is shown in Fig. 1.6. The dc analysis of the circuit yields the following equation.

$$V_{CC} = I_B R_B + V_{BE} \tag{1.4}$$

Therefore, $$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since this equation is independent of the current $I_C$, $dI_B/dI_C = 0$ and the stability factor given in Eq. (1.3) reduces to

$$S = 1 + \beta$$

Since $\beta$ is a large quantity, this is a very poor bias stable circuit. Therefore, in practice, this circuit is not used for biasing the base.

The advantages of this method are (i) simplicity, (ii) small number of components required, and (iii) if the supply voltage is very large as compared to $V_{BE}$ of the transistor, then the base current becomes largely independent of the voltage $V_{BE}$.

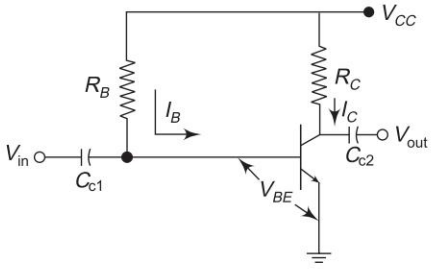



**Fig. 1.6** *Fixed bias circuit*

## EXAMPLE 1.6

In the fixed-bias compensation method shown in Fig. 1.7, a silicon transistor with $\beta = 100$ is used. $V_{CC} = 6$ V, $R_C = 3$ kΩ, $R_B = 530$ kΩ. Draw the dc load line and determine the operating point. What is the stability factor?

**Solution** (a) *dc load line*

$$V_{CE} = V_{CC} - I_C R_C$$

When $I_C = 0$, $V_{CE} = V_{CC} = 6$ V

When $V_{CE} = 0$, $I_C = \dfrac{V_{CC}}{R_C} = \dfrac{6}{3 \times 10^3} = 2$ mA

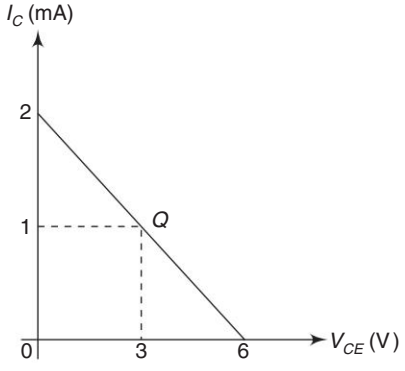



**Fig. 1.7**

(b) *Operating point Q*

For a silicon transistor, $V_{BE} = 0.7$ V

$$V_{CC} = I_B R_B + V_{BE}$$

Therefore, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{6 - 0.7}{530 \times 10^3} = 10$ mA

Therefore, $I_C = \beta I_B = 100 \times 10 \times 10^{-6} = 1$ mA

$$V_{CE} = V_{CC} - I_C R_C = 6 - 1 \times 10^{-3} \times 3 \times 10^3 = 3 \text{ V}$$

Therefore operating point is $V_{CEQ} = 3$ V and $I_{CQ} = 1$ mA.

(c) *Stability factor* $S = 1 + \beta = 1 + 100 = 101$

## EXAMPLE 1.7

Find the collector current and collector-to-emitter voltage for the given circuit as shown in Fig. 1.8.

**Solution** For a silicon transistor, $V_{BE} = 0.7$ V

Base current $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{9 - 0.7}{300 \times 10^3} = 27.67$ μA

Collector current $I_C = \beta I_B$

$= 50 \times 27.67 \times 10^{-6}$

$= 1.38$ mA

Collector-to-emitter voltage

$V_{CE} = V_{CC} - I_C R_C$

$= 9 - 1.38 \times 10^{-3} \times 2 \times 10^3$

$= 6.24$ V

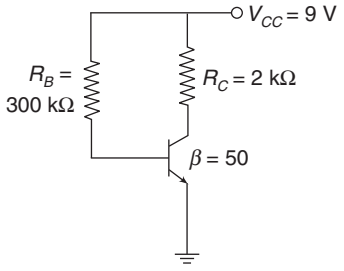



**Fig. 1.8**

## EXAMPLE 1.8

A germanium transistor having $\beta = 100$ and $V_{BE} = 0.2$ V is used in a fixed-bias amplifier circuit where $V_{CC} = 16$ V, $R_C = 5$ kΩ and $R_B = 790$ kΩ. Determine its operating point.

**Solution** For a germanium transistor, $V_{BE} = 0.2$ V

Applying KVL to the base circuit, we have

$V_{CC} - I_B R_B - V_{BE} = 0$

Therefore, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{16 - 0.2}{790 \times 10^3} = 20\ \mu\text{A}$

$I_C = \beta I_B = 100 \times 20\ \mu\text{A} = 2$ mA

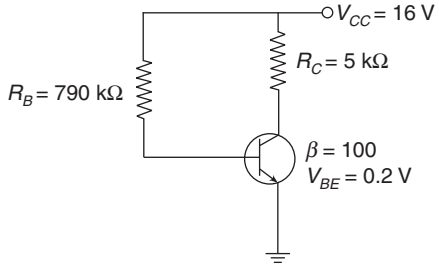



**Fig. 1.9**

Applying KVL to the collector circuit, we have

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C = 16 - 2 \times 10^{-3} \times 5 \times 10^3 = 6$ V

Hence, the operating point is $I_C = 2$ mA and $V_{CE} = 6$ V.

## EXAMPLE 1.9

The circuit as shown in Fig. 1.10 has fixed bias using an *NPN* transistor. Determine the value of base current, collector current, and collector-to-emitter voltage.

**Solution** Applying KVL to the base circuit, we have

$V_{CC} - I_B R_B - V_{BE} = 0$

Therefore, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{25 - 0.7}{180 \times 10^3} = 135\ \mu\text{A}$

$I_C = \beta I_B = 80 \times 135 \times 10^{-6} = 10.8$ mA

Applying KVL to the collector circuit, we have

$V_{CC} - I_C R_C - V_{CE} = 0$

Therefore, $V_{CE} = V_{CC} - I_C R_C$

$= 25 - 10.8 \times 10^{-3} \times 820 = 16.144$ V

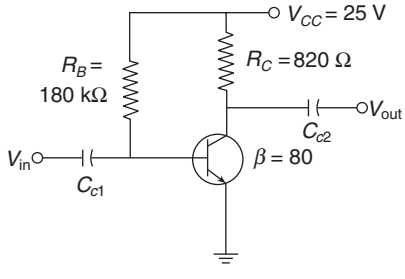



**Fig. 1.10**

**EXAMPLE 1.10**

For a fixed-bias configuration shown in Fig. 1.6, determine $I_C$, $R_C$, $R_B$, and $V_{CE}$ using the following specifications: $V_{CC} = 12$ V, $V_C = 6$ V, $\beta = 80$, and $I_B = 40$ μA.

**Solution** Assume $V_{BE} = 0.7$ V for a silicon transistor.

$$I_C = \beta I_B = 80 \times 40 \times 10^{-6} = 3.2 \text{ mA}$$

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{12 - 6}{3.2 \times 10^{-3}} = 1.875 \text{ k}\Omega$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.7}{40 \times 10^{-6}} = 282.5 \text{ k}\Omega$$

Since the emitter is grounded, $V_E = 0$.

$$V_{CE} = V_C = 6 \text{ V}$$

## 1.7.2 Emitter-Feedback Bias

The emitter-feedback bias network shown in Fig. 1.11 contains an emitter resistor for improving the stability level over that of the fixed-bias configuration. The analysis will be performed by first examining the base-emitter loop and then using the results to investigate the collector-emitter loop.

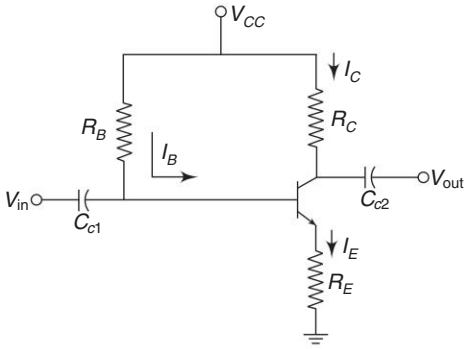



**Fig. 1.11** *Emitter-feedback bias circuit*

***Base-emitter Loop*** Applying Kirchhoff's voltage law for the base-feedback emitter loop, we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \qquad (1.5)$$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{CC} - I_B (R_B + R_E) - V_{BE} - I_C R_E = 0$$

$$V_{CC} - V_{BE} = I_B (R_B + R_E) + I_C R_E$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_E + R_B} - \left( \frac{R_E}{R_E + R_B} \right) I_C \qquad (1.6)$$

Here, $V_{BE}$ is independent of $I_C$.

Hence,
$$\frac{dI_B}{dI_C} = -\left( \frac{R_E}{R_E + R_B} \right) \qquad (1.7)$$

Substituting Eq. (1.7) in Eq. (1.3), we get the stability factor as

$$S = \frac{1 + \beta}{1 + \beta \dfrac{R_E}{R_E + R_B}} \qquad (1.8)$$

Since $1+\dfrac{\beta R_E}{(R_E+R_B)}>1$, $S<(1+\beta)$. Note that the value of the stability factor $S$ is always lower in emitter-feedback bias circuit than that of the fixed-bias circuit. Hence, it is clear that a better thermal stability can be achieved in an emitter-feedback bias circuit than the fixed-bias circuit.

***Collector-Emitter Loop*** Applying Kirchhoff's voltage law for the collector-emitter loop, we get

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E = I_C$, we have

$$V_{CE} - V_{CC} + I_C (R_C + R_E) = 0$$

and

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \tag{1.9}$$

$V_E$ is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E \tag{1.10}$$

The voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$V_C = V_{CE} + V_E \tag{1.11}$$

or

$$V_C = V_{CC} - I_C R_C \tag{1.12}$$

The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_E \tag{1.13}$$

or

$$V_B = V_{BE} + V_E \tag{1.14}$$

## EXAMPLE 1.11

For the emitter-feedback bias circuit, $V_{CC} = 10$ V, $R_C = 1.5$ kΩ, $R_B = 270$ kΩ, and $R_E = 1$ kΩ. Assuming $\beta = 50$, determine (a) stability factor, $S$ (b) $I_B$, (c) $I_C$, (d) $V_{CE}$, (e) $V_C$, (f) $V_E$, (g) $V_B$, and (h) $V_{BC}$.

**Solution**

(a) The stability factor is

$$S = \frac{1+\beta}{1+\dfrac{\beta R_E}{(R_E+R_B)}} = \frac{1+50}{1+\dfrac{(50\times 1\times 10^3)}{1\times 10^3 + 270\times 10^3}}$$

$$= \frac{51}{1+0.185} = \frac{51}{1.185} = 43.04$$

(b)
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E} = \frac{10 - 0.7}{27\times 10^3 + (51)(1\times 10^3)} = \frac{9.3}{321} = 28.97\ \mu\text{A}$$

(c)
$$I_C = \beta I_B = (50)\ (28.97 \times 10^{-6}) = 1.45\ \text{mA}$$

(d)
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$
$$= 10 - 1.45 \times 10^{-3}\ (1.5 \times 10^3 + 1 \times 10^3) = 10 - 3.62 = 6.38\ \text{V}$$

(e)
$$V_C = V_{CC} - I_C R_C = 10 - 1.45 \times 10^{-3}\ (1.5 \times 10^3) = 7.825\ \text{V}$$

(f) $V_E = V_C - V_{CE} = 7.825 - 6.38 = 1.445$ V

or $V_E = I_E R_E = I_C R_E = 1.45 \times 10^{-3} \times 1 \times 10^3 = 1.45$ V

(g) $V_B = V_{BE} + V_E = 0.7 + 1.45 = 2.15$ V

(h) $V_{BC} = V_B - V_C = 2.15 - 7.825 = |5.675|$ V (reverse bias as required)

## EXAMPLE 1.12

Calculate dc bias voltage and currents in the circuit in Fig. 1.12. Neglect $V_{BE}$ of the transistor.

**Solution** Given, $V_{CC} = 20$ V; $R_B = 400$ kΩ, $\beta = 100$, $R_E = 1$ kΩ; $R_C = 2$ kΩ

$$I_B R_B + V_{BE} + I_E R_E = V_{CC}$$

$$\frac{I_C}{\beta} R_B + 0 + (I_C + I_B) R_E = 20$$

$$I_C \left[ \frac{R_B}{\beta} + R_E + \frac{R_E}{\beta} \right] = 20$$

Therefore, $$I_C = \frac{20}{\left[ \frac{400 \times 10^3}{100} + 1 \times 10^3 + 10 \right]} = 4 \text{ mA}$$

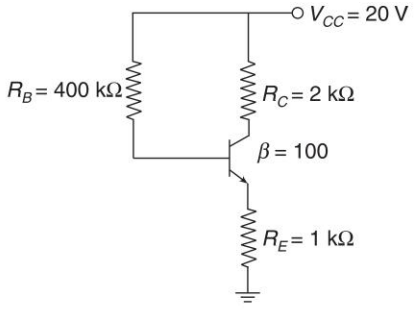



**Fig. 1.12**

$$I_B = \frac{I_C}{\beta} = \frac{4 \times 10^{-3}}{100} = 0.4 \text{ μA}$$

$$V_B = V_{BE} + I_E R_E$$

$$= 0 + 4 \times 10^{-3} \times 1 \times 10^3 = 4 \text{ V, since } I_C \approx I_E$$

### 1.7.3 Collector-to-Base Bias or Collector-Feedback Bias

A common-emitter amplifier using collector-to-base bias circuit is shown in Fig. 1.13. This circuit is the simplest way to provide some degree of stabilization to the amplifier operating point.

If the collector current $I_C$ tends to increase due to either increase in temperature or the transistor has been replaced by the one with a higher $\beta$, the voltage drop across $R_C$ increases, thereby reducing the value or $V_{CE}$. Therefore, $I_B$ decreases which, in turn, compensates the increase in $I_C$. Thus, greater stability is obtained.

The loop equation for this circuit is

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE} \quad (1.15)$$

i.e., $$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \quad (1.16)$$

Therefore, $$\frac{dI_B}{dI_C} = \frac{-R_C}{R_C + R_B} \quad (1.16)$$

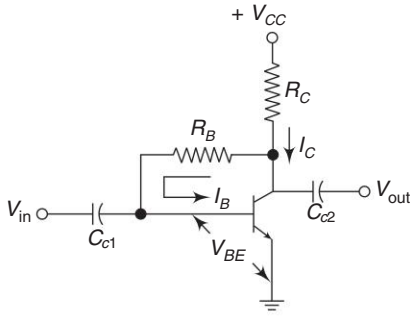



**Fig. 1.13** *Collector-to-base bias circuit*

Substituting Eq. (1.17) into Eq. (1.3), we get

$$S = \frac{1+\beta}{1+\beta\left(\dfrac{R_C}{R_C + R_B}\right)} \tag{1.18}$$

As can be seen, this value of the stability factor is smaller than the value obtained by fixed-bias circuit. Also, $S$ can be made small and the stability can be improved by making $R_B$ small or $R_C$ large.

If $R_C$ is very small, then $S = (\beta + 1)$, i.e., stability is very poor. Hence, the value of $R_C$ must be quite large for good stabilization. Thus, collector-to-base bias arrangement is not satisfactory for the amplifier circuits like transformer-coupled amplifier where the dc load resistance in the collector circuit is very small. For such amplifiers, emitter bias or self-bias will be the most satisfactory transistor biasing for stabilization.

## EXAMPLE 1.13

In the biasing with feedback resistor method, a silicon transistor with feedback resistor is used. The operating point is at 7 V, 1 mA and $V_{CC} = 12$ V. Assume $\beta = 100$. Determine (a) the value of $R_B$, (b) stability factor, and (c) what will be the new operating point if $\beta = 50$ with all other circuit values are same?

**Solution** Refer to Fig. 1.6. We know that for a silicon transistor, $V_{BE} = 0.7$ V.

(a) *To determine* $R_B$

The operating point is at $V_{CE} = 7$ V and $I_C = 1$ mA

Here,
$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12-7}{1\times10^{-3}} = 5\ \text{k}\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{1\times10^{-3}}{100} = 10\ \mu\text{A}$$

Using the relation,

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B} = \frac{12 - 0.7 - 1\times10^{-3}\times5\times10^{3}}{10\times10^{-6}} = 630\ \text{k}\Omega$$

(b) *Stability factor*
$$S = \frac{1+\beta}{1+\beta\left[\dfrac{R_C}{R_C + R_B}\right]} = \frac{1+100}{1+100\left[\dfrac{5\times10^{3}}{(5+630)\times10^{3}}\right]} = 56.5$$

(c) *To determine new operating point when* $\beta = 50$

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE}$$

$$= I_B(\beta R_C + R_B) + V_{BE}$$

i.e.,
$$12 = I_B(50\times5\times10^{3} + 630\times10^{3}) + 0.7$$

$$I_B = \frac{11.3}{880\times10^{3}} = 12.84\ \mu\text{A}$$

Therefore, $I_C = \beta I_B = 50 \times 12.84 \times 10^{-6} = 0.642$ mA

$$V_{CE} = V_{CC} - I_C R_C = 12 - 0.642 \times 10^{-3} \times 5 \times 10^3 = 8.79 \text{ V}$$

Therefore, the coordinates of the new operating point are $V_{CEQ} = 8.79$ V and $I_{CQ} = 0.642$ mA.

## EXAMPLE 1.14

In an *NPN* transistor, if $\beta = 50$ is used in common-emitter circuit with $V_{CC} = 10$ V and $R_C = 2$ kΩ. The bias is obtained by connecting 100 kΩ resistor from collector to base. Find the quiescent point and stability factor.

**Solution** Given, $V_{CC} = 10$ V, $R_C = 2$ kΩ,

$\beta = 50$ and collector to base resistor $R_B = 100$ kΩ

*To determine the quiescent point:* We know that for the collector-to-base bias-transistor circuit,

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE}$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta \cdot R_C}$$

$$= \frac{10 - 0.7}{100 \times 10^3 + 50 \times 2 \times 10^{-3}} = 46.5 \text{ μA}$$

Hence, $I_C = \beta \cdot I_B = 50 \times 46.5 \times 10^{-6} = 2.325$ mA

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.325 \times 10^{-3} \times 2 \times 10^3 = 5.35 \text{ V}$$

Therefore, the coordinates of the new operating point are

$$V_{CEQ} = 5.35 \text{ V and } I_{CQ} = 2.325 \text{ mA}$$

*To find the stability factor S*

$$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C + R_B}\right]} = \frac{1+50}{1+50\left[\frac{2\times10^3}{2\times10^3 + 100\times10^3}\right]} = 25.75$$

## EXAMPLE 1.15

In the collector-to-base *CE* amplifier circuit of Fig. 1.6 having $V_{CC} = 12$ V, $R_C = 250$ kΩ, $I_B = 0.25$ mA, $\beta = 100$, and $V_{CEQ} = 8$ V, calculate $R_B$ and stability factor.

**Solution**
$$R_B = \frac{V_{CEQ}}{I_B} = \frac{8}{0.25 \times 10^{-3}} = 32 \text{ kΩ}$$

Stability factor,
$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)} = \frac{101}{1+100\left(\frac{250}{32+250}\right)} = 56.9$$

## EXAMPLE 1.16

Calculate the quiescent current and voltage of a collector-to-base bias arrangement using the following data: $V_{CC} = 10$ V, $R_B = 100$ kΩ, $R_C = 2$ kΩ, $\beta = 50$, and also specify a value of $R_B$ so that $V_{CE} = 7$ V.

**Solution**

(a) Applying KVL to the base circuit, we have

$$V_{CC} - I_B(1 + \beta) R_C - I_B R_B - V_{BE} = 0$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_C} = \frac{10 - 0.7}{100 \times 10^3 + (1 + 50) \times 2 \times 10^3} = 46\ \mu\text{A}$$

$$I_C = \beta I_B = 50 \times 46\ \mu\text{A} = 2.3\ \text{mA}$$

Applying KVL to the collector circuit, we have

$$V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$$

Therefore,
$$V_{CE} = V_{CC} - (I_B + I_C) R_C$$
$$= 10 - (46 \times 10^{-6} + 2.3 \times 10^{-3}) \times 2 \times 10^3$$
$$= 5.308\ \text{V}$$

Quiescent current, $I_{CQ} = 2.3$ mA and

Quiescent voltage, $V_{CEQ} = 5.308$ V

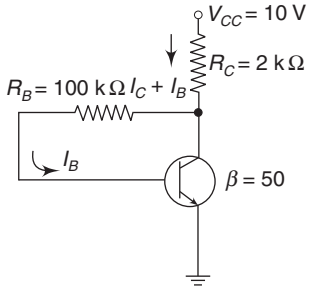



**Fig. 1.14**

(b) Given, $V_{CE} = 7$ V

$$(I_B + I_C) R_C = V_{CC} - V_{CE}$$
$$(1 + \beta) I_B R_C = V_{CC} - V_{CE}$$
$$I_B = \frac{V_{CC} - V_{CE}}{(1 + \beta) R_C} = \frac{10 - 7}{(1 + 50) \times 2 \times 10^3} = 29.41\ \mu\text{A}$$

We have,

$$V_{CC} = I_B R_B + V_{BE}$$
$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{7 - 0.7}{29.41 \times 10^{-6}} = 214.2\ \text{k}\Omega$$

### 1.7.4 Collector-Emitter Feedback Bias

Figure 1.15 shows the collector-emitter feedback-bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here, collector feedback is provided by connecting a resistance $R_B$ from the collector to the base and emitter feedback is provided by connecting an emitter resistance $R_E$ from the emitter to ground. Both the feedbacks are used to control the collector current $I_C$ and the base current $I_B$ in the opposite direction to increase the stability as compared to the previous biasing circuits.

Applying Kirchhoff's voltage law to the current, we get

$$(I_B + I_C) R_E + V_{BE} + I_B R_B + (I_B + I_C) R_C - V_{CC} = 0$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_E + R_C + R_B} - \left(\frac{R_E + R_C}{R_E + R_C + R_B}\right) I_C$$

Since $V_{BE}$ is independent of $I_C$,

$$\frac{dI_B}{dI_C} = -\left(\frac{R_E + R_C}{R_E + R_C + R_B}\right)$$

Substituting the above equation in Eq. (1.35), we get

$$S = \frac{1 + \beta}{1 + \dfrac{\beta (R_E + R_C)}{R_E + R_C + R_B}} \qquad (1.51)$$

From this, it is clear that the stability of the collector-emitter feedback bias circuit is always better than that of the collector-feedback and emitter-feedback circuits.

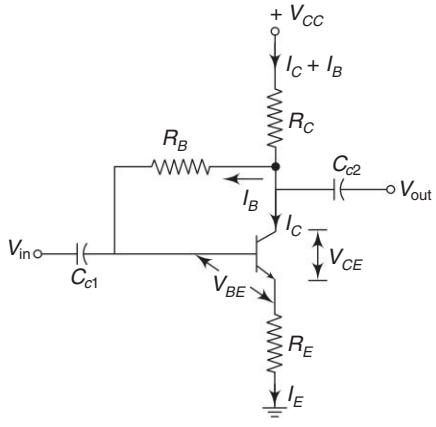



**Fig. 1.15** *Collector-emitter feedback circuit*

## 1.7.5 Voltage-Divider Bias, Self-Bias, or Emitter Bias

A simple circuit used to establish a stable operating point is the self-biasing configuration. The self-bias, also called emitter bias, or emitter resistor, and potential divider circuit, that can be used for low collector resistance, is shown in Fig. 1.16. The current in the emitter resistor $R_E$ causes a voltage drop which is in the direction to reverse bias the emitter junction. For the transistor to remain in the active region, the base-emitter junction has to be forward biased. The required base bias is obtained from the power supply through the potential divider network of the resistances $R_1$ and $R_2$.

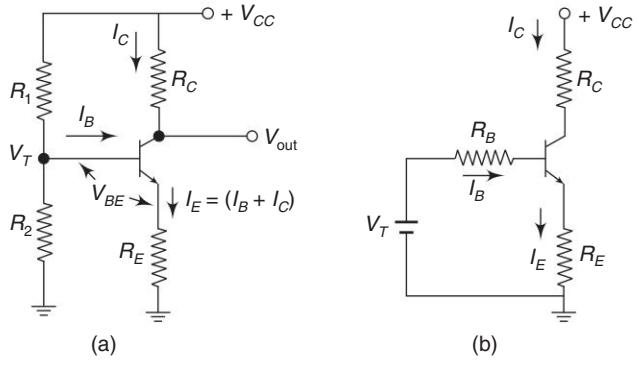



**Fig. 1.16** *(a) Self-bias circuit (b) Thevenin's equivalent circuit*

***Use of Self-bias Circuit as a Constant Current Circuit*** If $I_C$ tends to increase, say, due to increase in $I_{CO}$ with temperature, the current in $R_E$ increases. Hence, the voltage drop across $R_E$ increases thereby decreasing the base current. As a result, $I_C$ is maintained almost constant.

## 1.7.6 Stabilization Factors

***To Determine Stability Factor, S*** Applying Thevenin's theorem to the circuit of Fig. 1.16, for finding the base current, we have,

$$V_T = \frac{R_2 V_{CC}}{R_1 + R_2} \text{ and } R_B = \frac{R_1 R_2}{R_1 + R_2}$$

The loop equation around the base circuit can be written as

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating this equation with respect to $I_C$, we get

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B}$$

Substituting this equation in Eq. (1.35), we get

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)}$$

Therefore,

$$S = (1+\beta)\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}} \tag{1.18}$$

As can be seen, the value of $S$ is equal to one if the ratio $R_B/R_E$ is very small as compared to 1. As this ratio becomes comparable to unity, and beyond towards infinity, the value of the stability factor goes on increasing till $S = 1 + \beta$.

This improvement in the stability up to a factor equal to 1 is achieved at the cost of power dissipation. To improve the stability, the equivalent resistance $R_B$ must be decreased, forcing more current in the voltage divider network of $R_1$ and $R_2$.

Often, to prevent the loss of gain due to the negative feedback, $R_E$ is shunted by a capacitor $C_E$. The capacitive reactance $X_{CE}$ must be equal to about one-tenth of the value of the resistance $R_E$ at the lowest operating frequency.

***To Determine the Stability Factor S′*** The stability factor $S'$ is defined as the rate of change of $I_C$ with $V_{BE}$, keeping $I_{CO}$ and $\beta$ constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}}$$

From Fig. 1.38 (b),

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$= I_B [R_B + R_E] + I_C R_E + V_{BE} \text{ since } [I_E = I_B + I_C] \tag{1.19}$$

We have

$$I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta} \tag{1.20}$$

Substituting Eq. (1.19) in Eq. (1.20), we get

$$V_T = \frac{I_C}{\beta}(R_B + R_E) + V_{BE} + I_C R_E + \frac{I_{CO}}{\beta}(1+\beta)\{R_B + R_E\} \tag{1.21}$$

Differentiating the above equation w.r.t. $V_{BE}$, we get

$$0 = \frac{dI_C}{dV_{BE}}\left(\frac{R_B + R_E}{\beta}\right) + 1 + R_E \frac{dI_C}{dV_{BE}} + 0$$

$$-1 = \frac{dI_C}{dV_{BE}}\left[R_E + \frac{R_B + R_E}{\beta}\right]$$

$$-1 = \frac{dI_C}{dV_{BE}}\left[\frac{R_B + (1+\beta)R_E}{\beta}\right]$$

Therefore,
$$S' = \frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B + (1+\beta)R_E} \tag{1.22}$$

***To Determine the Stability of S″*** The stability factor $S''$ is defined as the rate of change of $I_C$ w.r.t. $\beta$, keeping $I_{CO}$ and $V_{BE}$ constant.

Rearranging Eq. (1.21), we have

$$I_C = \frac{\beta(V_T - V_{BE})}{R_B + (1+\beta)R_E} + \frac{\beta\left(\frac{1+\beta}{\beta}\right) I_{CO}(R_B + R_E)}{R_B + (1+\beta)R_E} \tag{1.23}$$

Since $\beta >> 1$, the numerator of the second term can be written as

$$(R_B + R_E)\left(\frac{1+\beta}{\beta}\right) I_{CO} = (R_B + R_E)\, I_{CO} \tag{1.24}$$

Substituting Eq. (1.24) in Eq. (1.27), we have

$$I_C = \frac{\beta(V_T - V_{BE})}{R_E + (1+\beta)R_E} + \frac{\beta(R_B + R_E) I_{CO}}{R_B + (1+\beta)R_E}$$

Therefore,
$$I_C = \frac{\beta[V_T - V_{BE} + (R_B + R_E) I_{CO}]}{R_B + (1+\beta)R_E}$$

Let,
$$V' = (R_B + R_E) I_{CO}.$$

Therefore,
$$I_C = \frac{\beta[V_T - V_{BE} + V']}{R_B + (1+\beta)R_E} \tag{1.25}$$

Differentiating the above equation w.r.t. $\beta$ and simplifying, we obtain

$$S'' = \frac{dI_C}{d\beta} = \frac{I_C}{\beta\left[1 + \beta\left(\frac{R_E}{R_E + R_B}\right)\right]} = \frac{SI_C}{\beta(1+\beta)} \tag{1.26}$$

## EXAMPLE 1.17

In a CE germanium transistor-amplifier circuit, the bias is provided by self-bias, i.e., emitter resistor and potential-divider arrangement (refer to Fig. 1.7). The various parameters are $V_{CC}$ = 16 V, $R_C$ = 3 kΩ, $R_E$ = 2 kΩ, $R_1$ = 56 kΩ, $R_2$ = 20 kΩ, and $\alpha$ = 0.985. Determine (a) the coordinates of the operating point, and (b) the stability factor *S*.

**Solution** For a germanium transistor, $V_{BE}$ = 0.3 V. As $\alpha$ = 0.985,

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1-0.985} = 66$$

(a) *To find the coordinates of the operating point*

Referring to Fig. 1.16, we have

Thevenin's voltage, $$V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{20 \times 10^3}{76 \times 10^3} \times 16 = 4.21 \text{ V}$$

Thevenin's resistance, $$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{20 \times 10^3 \times 56 \times 10^3}{76 \times 10^3} = 14.737 \text{ k}\Omega$$

The loop equation around the base circuit is

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{\beta} R_B + V_{BE} + \left( \frac{I_C}{\beta} + I_C \right) R_E$$

$$4.21 = \frac{I_C}{66} \times 14.737 \times 10^3 + 0.3 + I_C \left( \frac{1}{66} + 1 \right) \times 2 \times 10^3$$

$$3.91 = I_C \, [0.223 + 2.03] \times 10^3$$

Therefore, $$I_C = \frac{3.91}{2.253 \times 10^3} = 1.73 \text{ mA}$$

Since $I_B$ is very small, $I_C \approx I_E = 1.73$ mA

Therefore, $$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= V_{CC} - I_C \, [R_C + R_E]$$

$$= 16 - 1.73 \times 10^{-3} \times 5 \times 10^3 = 7.35 \text{ V}$$

Therefore, the coordinates of the operating point are $I_C$ = 1.73 mA and $V_{CE}$ = 7.35 V.

(b) *To find the stability factor S,*

$$S = (1+\beta) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} = (1+66) \frac{1 + \frac{14.737}{2}}{1 + 66 + \frac{14.737}{2}} = 67 \times \frac{8.3685}{74.3685} = 7.537$$

## EXAMPLE 1.18

Consider the self-bias circuit where $V_{CC}$ = 22.5 Volt, $R_C$ = 5.6 kΩ, $R_2$ = 10 kΩ, and $R_1$ = 90 kΩ, $h_{fe}$ = 55, $V_{BE}$ = 0.6 V. The transistor operates in active region. Determine (a) operating point, and (b) stability factor.

**Solution** For the given circuit, $V_{BE}$ = 0.6 V, $h_{fe}$ = 55

(a) *To determine the operating point*

Thevenin's voltage, $$V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10 \times 10^3}{100 \times 10^3} \times 22.5 = 2.25 \text{ V}$$

Thevenin's resistance, $$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 10^3 \times 90 \times 10^3}{100 \times 10^3} = 9 \text{ k}\Omega$$

The loop equation around the base circuit is

$$V_B = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{h_{fe}} R_B + V_{BE} + \left( \frac{I_C}{h_{fe}} + I_C \right) R_E$$

$$2.25 = \frac{I_C}{55} \times 9 \times 10^3 + 0.6 + \left( \frac{1}{55} + 1 \right) I_C \times 1 \times 10^3$$

$$2.25 = I_C \times 0.16 \times 10^3 + 0.6 + 1.01 \times I_C \times 10^3$$

$$2.25 = I_C \times 1.17 \times 10^3 + 0.6$$

Therefore, $$I_C = \frac{2.25 - 0.6}{1.17 \times 10^3} = 1.41 \text{ mA}$$

Since $I_B$ is very small, $I_C \approx I_E = 1.41$ mA

Therefore, $$V_{CE} = V_{CC} - I_C R_C - I_E R_E = V_{CC} - I_C (R_C + R_E)$$

$$= 22.5 - 1.41 \times 10^{-3} \times 6.6 \times 10^3 = 13.19 \text{ V}$$

Operating point coordinates are $V_{CE}$ = 13.19 V and $I_C$ = 1.41 mA

(b) *To find the stability factor, S*

$$S = (1 + \beta) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} = (1 + 55) \frac{1 + \frac{9 \times 10^3}{1 \times 10^3}}{1 + 55 + \frac{9 \times 10^3}{1 \times 10^3}} = \frac{56 \times 10}{65} = \frac{560}{65} = 8.6$$

## EXAMPLE 1.19

Figure 1.17 shows the dc bias circuit of a common-emitter transistor amplifier. Find the percentage change in the collector current, if the transistor with $h_{fe}$ = 50 is replaced by another transistor with $h_{fe}$ = 150. It is given that the base-emitter drop $V_{BE}$ = 0.6 V.

**Solution**

(a) For the given circuit, $V_{BE} = 0.6$ V, $h_{fe} = 50$

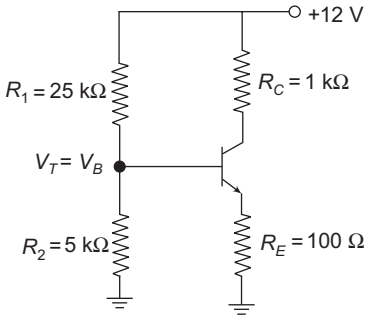



**Fig. 1.17**

Thevenin's voltage, $$V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{30 \times 10^3} \times 12 = 2 \text{ V}$$

Thevenin's resistance, $$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{25 \times 10^3 \times 5 \times 10^3}{30 \times 10^3} = 4.16 \text{ k}\Omega$$

The loop equation around the base circuit is

$$V_T = V_B = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{h_{fe}} R_B + V_{BE} + \left( \frac{I_C}{h_{fe}} + I_C \right) R_E$$

$$2 = \frac{I_C}{50} \times 4.6 \times 10^3 + 0.6 + \left( \frac{1}{50} + 1 \right) \times I_C \times 0.1 \times 10^3$$

$$2 - 0.6 = I_C \times (0.08 + 0.102) \times 10^3$$

Therefore, $$I_C = \frac{14}{0.182 \times 10^3} = 7.69 \text{ mA}$$

(b) For the given circuit, $V_{BE} = 0.6$ V, $h_{fe} = 150$

The loop equation around the base circuit is

$$V_B = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{h_{fe}} R_B + V_{BE} + \left( \frac{I_C}{h_{fe}} + I_C \right) R_E$$

$$2 = \frac{I_C}{50} \times 4.6 \times 10^3 + 0.6 + \left( \frac{1}{50} + 1 \right) \times I_C \times 0.1 \times 10^3$$

$$2 - 0.6 = I_C \times (0.028 + 0.1) \times 10^3$$

Therefore, $$I_C = \frac{1.4}{0.128 \times 10^3} = 10.93 \text{ mA}$$

Change in collector current $$= \frac{10.93 - 7.69}{7.69} = 0.42, \text{ i.e., } 42\%$$

There is 42% change in $I_C$ when $h_{fe}$ changes from 50 to 150.

## EXAMPLE 1.20

If the various parameters of a *CE* amplifier which uses the self-bias method are $V_{CC} = 12$ V, $R_1 = 10$ kΩ, $R_2 = 5$ kΩ, $R_C = 1$ kΩ, $R_E = 2$ kΩ, and $\beta = 100$, find (a) the coordinates of the operating point, and (b) the stability factor, assuming the transistor to be silicon.

**Solution**

(a) *To find the coordinates of the operating point*

Refer Fig. 1.16.

Thevenin's voltage, $V_T = \dfrac{R_2}{R_1 + R_2} V_{CC} = \dfrac{5 \times 10^3}{15 \times 10^3} \times 12 = 4 \text{ V}$

Thevenin's resistance, $R_B = \dfrac{R_1 R_2}{(R_1 + R_2)} = \dfrac{5 \times 10^3 \times 10 \times 10^3}{15 \times 10^3} = 3.33 \text{ k}\Omega$

The loop equation around the basic circuit is

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{\beta} R_B + V_{BE} + \left( \frac{I_C}{\beta} + I_C \right) R_E$$

$$4 = \frac{I_C}{100} \times 3.33 \times 10^3 + 0.7 + I_C \left( \frac{1}{100} + 1 \right) \times 2 \times 10^3$$

$$3.3 = (33.3 + 2020)\, I_C$$

$$I_C = \frac{3.3}{2053.3} = 1.61 \text{ mA}$$

Since $I_B$ is very small, $I_C \approx I_E = 1.61$ mA

Therefore, $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$$= V_{CC} - I_C [R_C + R_E]$$

$$= 12 - 1.61 \times 10^{-3} \times 3 \times 10^3 = 7.17 \text{ V}$$

Therefore, the coordinates of the operating point are $I_C = 1.61$ mA and $V_{CE} = 7.17$ V.

(b) *To find the stability factor S*

$$S = (1 + \beta) \frac{1 + \dfrac{R_B}{R_E}}{1 + \beta + \dfrac{R_B}{R_E}} = (1 + 100) \frac{1 + \dfrac{3.33 \times 10^3}{2 \times 10^3}}{1 + 100 + \dfrac{3.33 \times 10^3}{2 \times 10^3}} = 2.6$$

## EXAMPLE 1.21

Determine the quiescent current and collector-to-emitter voltage for a germanium transistor with $\beta = 50$ in self-biasing arrangement. Draw the circuit with a given component value with $V_{CC} = 20$ V, $R_C = 2$ kΩ, $R_E = 100$ Ω, $R_1 = 100$ kΩ, and $R_2 = 5$ kΩ. Also find the stability factor.

**Solution** For a germanium transistor, $V_{BE} = 0.3$ V and $\beta = 50$

*To find the coordinates of the operating point*

Thevenin's voltage, $V_T = \dfrac{R_2}{R_1 + R_2} V_{CC} = \dfrac{5 \times 10^3}{105 \times 10^3} \times 20 = 0.95 \text{ V}$

Thevenin's resistance, $R_B = \dfrac{R_1 R_2}{R_1 + R_2} = \dfrac{100 \times 10^3 \times 5 \times 10^3}{105 \times 10^3} = 4.76\ \text{k}\Omega$

The loop equation around the base circuit is

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{\beta} R_B + V_{BE} + \left( \frac{I_C}{\beta} + I_C \right) R_E$$

$$0.95 = \frac{I_C}{50} \times 4.76 \times 10^3 + 0.3 + I_C \times \frac{51}{50} \times 100$$

$$0.65 = 197.2\ I_C$$

Therefore, $I_C = \dfrac{0.65}{197.2} = 3.296\ \text{mA}$

Since $I_B$ is very small, $I_C \approx I_E = 3.296\ \text{mA}$

Therefore, $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$$= V_{CC} - I_C (R_C + R_E)$$

$$= 20 - 3.296 \times 10^{-3} \times 2.01 \times 10^3 = 13.375\ \text{V}$$

Therefore, the coordinates of the operating point are $I_C = 3.296$ mA and $V_{CE} = 13.375$ V.

*To find the stability factor S*

$$S = (1 + \beta) \frac{1 + \dfrac{R_B}{R_E}}{1 + \beta + \dfrac{R_B}{R_E}} = (1 + 50) \frac{1 + \dfrac{4.76 \times 10^3}{100}}{1 + 50 + \dfrac{4.76 \times 10^3}{100}} = 25.18$$

## EXAMPLE 1.22

A germanium transistor is used in a self-biasing circuit configuration as shown below with $V_{CC} = 16$ V, $R_C = 1.5$ kΩ and $\beta = 50$. The operating point desired is $V_{CE} = 8$ V and $I_C = 4$ mA. If a stability factor $S = 10$ is desired, calculate the values of $R_1$ and $R_2$ and $R_E$ of the circuit (Fig. 1.18).

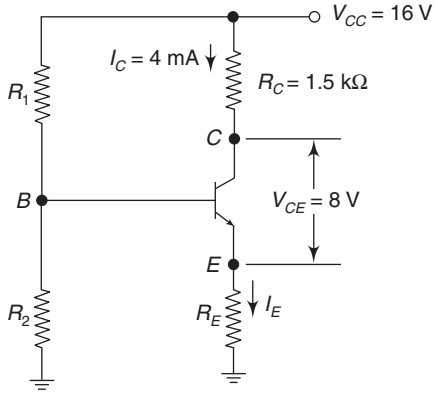



**Fig. 1.18**

**Solution**

*(a) To determine $R_E$*

We know that, $V_{CC} = V_{CE} + I_C (R_C + R_E)$

$$16 = 8 + 4 \times 10^{-3} (1.5 \times 10^3 + R_E)$$

Therefore, $R_E = 500\ \Omega$

*(b) To determine $R_{TH}$*

Given, $S = 10$

Stability factor $$S = \frac{1+\beta}{1+\beta\dfrac{R_E}{R_{TH}+R_E}} = \frac{1+50}{1+50\left(\dfrac{500}{R_{TH}+500}\right)}$$

Upon solving, we get $R_{TH} = 5.58\ \text{k}\Omega$

*(c) To determine $R_2$*

$$R_2 = 0.1\ \beta R_E = 27.98\ \text{k}\Omega$$

*(d) To determine $R_1$*

We know that, $$R_{TH} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$5.58 \times 10^3 = \frac{R_1 \times 27.98 \times 10^3}{R_1 + 27.98 \times 10^3}$$

Therefore, $R_1 = 6.97\ \text{k}\Omega$

## EXAMPLE 1.23

A *CE* transistor amplifier with the voltage-divider bias circuit of Fig. 1.16 is designed to establish the quiescent point at $V_{CE} = 12$ V, $I_C = 2$ mA and stability factor ≤ 5.1. If $V_{CC} = 24$ V, $V_{BE} = 0.7$ V, $\beta = 50$, and $R_C = 4.7\ \text{k}\Omega$, determine the values of resistors $R_E$, $R_1$, and $R_2$.

**Solution**

(a) *To determine $R_E$*

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$
$$= V_{CC} - I_C\,[R_C + R_E], \text{ since } I_C \approx I_E$$
$$12 = 24 - 2 \times 10^{-3}\,[4.7 \times 10^3 + R_E]$$

Therefore, $R_E = 1.3\ \text{k}\Omega$

(b) *To determine $R_1$ and $R_2$*

Stability factor, $$S = \frac{1+\beta}{1+\beta\left(\dfrac{R_E}{R_E + R_B}\right)}, \text{ where } R_B = \frac{R_1 R_2}{(R_1 + R_2)}$$

$$5.1 = \frac{51}{1+50\left(\dfrac{1.3\times10^3}{1.3\times10^3 + R_B}\right)}$$

i.e., $$1+50\left(\frac{1.3\times10^3}{1.3\times10^3 + R_B}\right) = \frac{51}{5.1} = 10$$

Therefore, $$\left(\frac{50 \times 1.3 \times 10^3}{1.3 \times 10^3 + R_B}\right) = 9$$

$$1.3 \times 10^3 + R_B = \frac{50 \times 1.3 \times 10^3}{9} = 7.2 \text{ k}\Omega$$

$$R_B = 5.9 \text{ k}\Omega$$

Also, we know that for a good voltage divider, the value of the resistance $R_2 = 0.1\ \beta R_E$

Therefore, $$R_2 = 0.1 \times 50 \times 1.3 \times 10^3 = 6.5 \text{ k}\Omega$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$5.9 \times 10^3 = \frac{R_1 \times 6.5 \times 10^3}{R_1 + 6.5 \times 10^3}$$

Simplifying, we get $R_1 = 64 \text{ k}\Omega$

## EXAMPLE 1.24

In the circuit shown in Fig. 1.19, if $I_C = 2$ mA and $V_{CE} = 3$ V, calculate $R_1$ and $R_3$.

**Solution** Given, $\beta = 100$, $I_C = 2$ mA, $V_{CE} = 3$ V, $V_{BE} = 0.6$ V, $R_2 = 10$ kΩ and $R_4 = 500\ \Omega$

We know that $$\beta = \frac{I_C}{I_B}$$

Hence, $$I_B = \frac{I_C}{\beta} = \frac{2 \times 10^{-3}}{100} = 20\ \mu\text{A}$$

$$V_{CC} = I_C R_3 + V_{CE} + I_E R_4$$

$$I_E = I_C + I_B = 20 \times 10^{-6} + 2 \times 10^{-3} = 2.02 \text{ mA}$$

Substituting the values, we get

$$15 = 2 \times 10^{-3} \times R_3 + 3 + 2.02 \times 10^{-3} \times 500$$

Therefore, $R_3 = 5.495 \text{ k}\Omega$

$$V_B = V_{BE} + I_E R_4 = 0.6 + 2.02 \times 10^{-3} \times 500 = 1.61$$

From the circuit, $$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$1.61 = \frac{10 \times 10^3 \times 15}{R_1 + 10 \times 10^3}$$

Therefore, $R_1 = 83.17 \text{ k}\Omega$

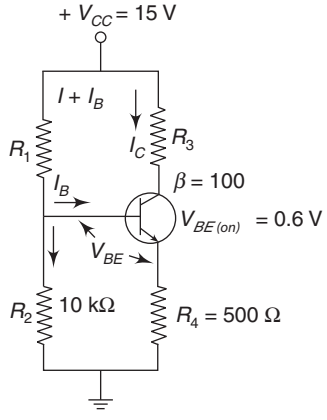



**Fig. 1.19**

## EXAMPLE 1.25

In an *NPN* transistor, $\beta = 50$ is used in common-emitter circuit with $V_{CC} = 10$ V and $R_C = 2$ kΩ. The bias is obtained by connecting the 100 kΩ resistor from collector to base. Find the quiescent point and stability factor.

**Solution** Given, $V_{CC} = 10$ V, $R_C = 2$ kΩ, $\beta = 50$ and collector to base resistor, $R_B = 100$ kΩ

*To determine the quiescent point*

We know that the collector-to-base bias-transistor circuit

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE}$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta \cdot R_C} = \frac{10 - 0.7}{100 \times 10^3 + 50 \times 2 \times 10^{+3}} = 46.5\ \mu\text{A}$$

Hence,
$$I_C = \beta I_B = 50 \times 46.5 \times 10^{-6} = 2.325\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.325 \times 10^{-3} \times 2 \times 10^3 = 5.35\ \text{V}$$

Therefore, the coordinates of the new operating point are

$$V_{CEQ} = 5.35\ \text{V and } I_{CQ} = 2.325\ \text{mA}$$

*To find the stability factor S*

$$S = \frac{1 + \beta}{1 + \beta\left[\frac{R_C}{R_C + R_B}\right]} = \frac{1 + 50}{1 + 50\left[\frac{2 \times 10^3}{2 \times 10^3 + 100 \times 10^3}\right]} = 25.75$$

## EXAMPLE 1.26

Design a voltage-divider bias network using a supply of 24 V, $\beta = 110$ and $I_{CQ} = 4$ mA, $V_{CEQ} = 8$ V. Choose $V_E = V_{CC}/8$.

**Solution** Given: $I_{CQ} = 4$ mA, $V_{CEQ} = 8$ V, $V_E = V_{CC}/8$, $V_{CC} = 24$ V, $\beta = 110$

(a) *To determine $I_B$, $I_E$ and $V_E$*

$$I_B = \frac{I_{CQ}}{\beta} = \frac{4 \times 10^3}{110} = 36.36\ \mu\text{A}$$

$$I_E = I_B + I_C = 36.36 \times 10^{-6} + 4 \times 10^{-3} = 4.03636\ \text{mA}$$

$$V_E = \frac{V_{CC}}{8} = \frac{24}{8} = 3\ \text{V}$$

(b) *To determine $R_E$ and $R_2$*

$$R_E = \frac{V_E}{I_E} = \frac{3}{4.03636 \times 10^{-3}} = 743.244\ \Omega$$

Applying KVL to the collector circuit,

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

Therefore,
$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{24 - 8 - 3}{4 \times 10^{-3}} = 3.25 \text{ k}\Omega$$

(c) *To determine $R_1$ and $R_2$*

$$V_B = V_E + V_{BE} = 3 + 0.7 = 3.7 \text{ V}$$

Referring to Fig. 1.16, consider the current through $R_1$ to be $I + I_B$ and that through $R_2$ to be $I$. Resistors $R_1$ and $R_2$ form the potential divider. For proper operation of the potential divider, the current $I$ should be atleast ten times the $I_B$, i.e., $I \geq 10\, I_B$. Therefore,

$$I = 10\, I_B = 10 \times 36.36 \times 10^{-6} = 363.6 \text{ μA}$$

$$R_2 = \frac{V_B}{I} = \frac{3.7}{363.6 \times 10^{-6}} = 10.176 \text{ k}\Omega$$

$$R_1 = \frac{V_{CC} - V_B}{I + I_B} = \frac{24 - 3.7}{(363.6 + 36.36) \times 10^{-6}} = 50.755 \text{ k}\Omega$$

## EXAMPLE 1.27

Determine the stability factor for the circuit shown in Fig. 1.20.

**Solution**

$$I_2 = \frac{V_{BE} + (I_C + I_B) R_E}{R_2}$$

$$I_1 = I_B + I_2$$

Therefore,
$$I_1 = I_B + \frac{V_{BE} + (I_C + I_B) R_E}{R_2}$$

$$= \frac{I_B R_2 + V_{BE} + (I_C + I_B) R_E}{R_2}$$

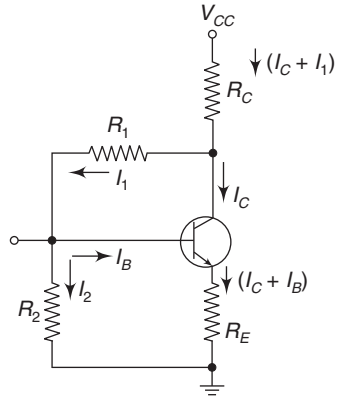



**Fig. 1.20**

Applying KVL to the collector base-emitter loop, we have

$$V_{CC} = (I_C + I_1) R_C - I_1 R_1 - V_{BE} - (I_C + I_B) R_E$$
$$= (I_C + I_1) R_C + I_1 R_1 + V_{BE} + (I_C + I_B) R_E$$
$$= I_C R_C + I_1 R_C + I_1 R_1 + V_{BE} + I_C R_E + I_B R_E$$
$$= I_C (R_C + R_E) + I_1 (R_C + R_1) + V_{BE} + I_B R_E$$

Substituting the value of $I_1$ from the equation determined above, we get

$$V_{CC} = I_C (R_C + R_E) + \frac{I_B R_2 + V_{BE} + (I_C + I_B) R_E}{R_2} (R_C + R_1) + V_{BE} + I_B R_E$$

$$= I_C \left[ R_C + R_E + \frac{(R_C + R_1)}{R_2} \right] + I_B \left[ R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] + \left[ 1 + \frac{(R_C + R_1)}{R_2} \right] V_{BE}$$

We know that $I_C = \beta I_B + (1+\beta)\, I_{CO}$

Therefore, $I_B = \dfrac{I_C - (1+\beta)\, I_{CO}}{\beta}$

Substituting the value of $I_B$, we get

$$V_{CC} = I_C \left[ R_C + R_E + \frac{R_E (R_C + R_1)}{R_2} \right] + \frac{I_C - (1+\beta) I_{CO}}{\beta} \times \left[ R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] + \left[ 1 + \frac{(R_C + R_1)}{R_2} \right] V_{BE}$$

We know that $S = \dfrac{dI_C}{dI_{CO}}$. Hence, differentiating the above equation and assuming $V_{BE}$ constant, we get

$$0 = \frac{\partial I_C}{\partial I_{CO}} \left[ R_C + R_E + \frac{R_E (R_C + R_1)}{R_2} \right] + \frac{\partial I_C}{\partial I_{CO}} \times \frac{1}{\beta} \left[ R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] - \frac{(1+\beta)}{\beta} \left[ R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right]$$

$$= \frac{\partial I_C}{\partial I_{CO}} \left[ \frac{R_2 R_C + R_2 R_E + R_E R_C + R_E R_1}{R_2} \right] + \frac{\partial I_C}{\partial I_{CO}} \times \frac{1}{\beta} \times \left[ \frac{R_2 R_E + R_E R_C + R_E R_1 + R_2 R_C + R_1 R_2}{R_2} \right] - \frac{1+\beta}{\beta} \left[ \frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{R_2} \right]$$

$$= \frac{\partial I_C}{\partial I_{CO}} \left[ \frac{R_2 R_C + R_E (R_1 + R_2 + R_C)}{R_2} \right] + \frac{\partial I_C}{\partial I_{CO}} \times \frac{1}{\beta} \times \left[ \frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{R_2} \right] - \frac{1+\beta}{\beta} \left[ \frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{R_2} \right]$$

$$= \frac{\partial I_C}{\partial I_{CO}} \left[ \frac{R_2 R_C + R_E (R_1 + R_2 + R_C)}{R_2} \right] + \left[ \frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{\beta R_2} \right]$$

$$\frac{\partial I_C}{\partial I_{CO}} = \frac{\dfrac{1+\beta}{\beta} [R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)]}{R_2 R_C + R_E (R_1 + R_2 + R_C) + \dfrac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{\beta}}$$

$$= \frac{\dfrac{1+\beta}{\beta} [R_2 (R_C + R_1) + (R_E (R_1 + R_2 + R_C)]}{\dfrac{\beta (R_2 R_C + R_E (R_1 + R_2 + R_C)) + R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{\beta}}$$

Stability factor, $S = \dfrac{\partial I_C}{\partial I_{CO}} = \dfrac{(1+\beta)[R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)]}{R_1 R_2 + (\beta + 1)[R_2 R_C + R_E (R_1 + R_2 + R_C)]}$

### 1.7.7 Common Base Stability

In a common-base amplifier circuit, the equation for the collector current $I_C$ is given by

$$I_C = \alpha I_E + I_{CO}$$

$$S \approx \frac{dI_C}{dI_{CO}} = 1$$

Since this is highly stable, the common-base amplifier circuit is not in need of bias stabilization.

### 1.7.8 Advantage of Self-bias (Voltage-Divider Bias) Over Other Types of Biasing

In the fixed-bias method discussed in Section 1.7.1, the stability factor is given by

$$S = 1 + \beta$$

Since $\beta$ is normally a large quantity, this circuit provides very poor stability. Therefore, the fixed biasing technique is not preferred for biasing the base.

In the collector-to-base bias method, when $R_C$ is very small, $S \approx 1 + \beta$, which is equal to that of fixed bias. Hence, the collector-to-base bias method is also not preferable. In the self-bias method discussed in Section 1.7.5, when $\frac{R_B}{R_E}$ is very small, $S \approx 1$, which provides good stability. Hence, the self-bias method is the best method over other types of 'biasing'.

## 1.8 BIAS COMPENSATION TECHNIQUES

The various biasing circuits considered in the previous sections used some types of negative feedback to stabilize the operation point. Also, diodes, thermistors, and sensistors can be used to compensate for variations in current.

### 1.8.1 Thermistor and Sensistor Compensations

***Thermistor Compensation*** In Fig. 1.21, a thermistor, $R_T$, having a negative temperature coefficient is connected in parallel with $R_2$. The resistance of the thermistor decreases exponentially with increase of temperature. An increase in temperature will decrease the base voltage $V_{BE}$, reducing $I_B$ and $I_C$. Bias stabilization is also provided by $R_E$ and $C_E$.

***Sensistor Compensation*** In Fig. 1.22, a sensistor, $R_S$, having a positive temperature coefficient is connected across $R_1$ (or $R_E$). $R_S$ increases with temperature. As temperature increases, the equivalent resistance of the parallel combination of $R_1$ and $R_S$ also increases and, hence, the base voltage $V_{BE}$ decreases, reducing $I_B$ and $I_C$. This reduced $I_C$ compensates for the increased $I_C$ caused by the increase in $I_{CO}$, $V_{BE}$, and $\beta$ due to temperature rise.

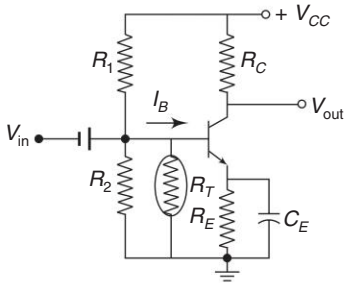



**Fig. 1.21** *Thermistor-bias compensation*

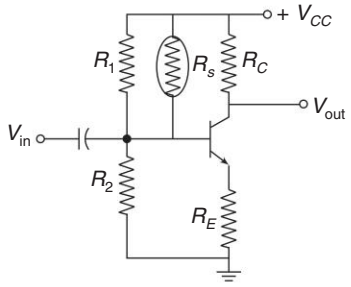



**Fig. 1.22** *Sensistor-bias compensation*

## 1.8.2 Compensation Against Variation in $V_{BE}$ and $I_{CO}$

### *Compensation for $V_{BE}$*

**Diode Compensation in Emitter Circuit** Figure 1.23 shows the Thevenin's equivalent circuit of the voltage-divider bias with bias-compensation technique.

Here, $V_{DD}$ is separately used to keep the diode in the forward-biased condition. If the diode is of same material and type as the transistor, then the voltage across the diode $V_D$ will have the same temperature coefficient (2.5 m V/°C) as the base-to-emitter voltage $V_{BE}$. If $V_{BE}$ changes by a small amount with change in temperature, then $V_D$ also changes by the same amount and, therefore, the changes cancel each other.

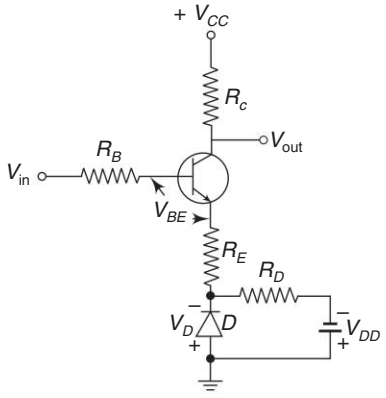



**Fig. 1.23** *Stabilization by voltage-divider bias compensation*

We know that,

$$V_{BE} = V_T - \frac{[R_B + (1+\beta)R_E]}{\beta} I_C + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

Rearranging, we have

$$\frac{[R_B + (1+\beta)R_E}{\beta I_C} I_C = V_T - V_{BE} + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

Hence,

$$I_C = \frac{\beta[V_T - V_{BE}] + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E}$$

From KVL equation of the base circuit of Fig. 1.23, the above equation can be written as

$$I_C = \frac{\beta[V_{in} - V_{BE} - V_D] + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E}$$

Since variation of $V_D$ is same as $V_{BE}$, the collector current $I_C$ will be insensitive to variation in $V_{BE}$.

**Diode Compensation in Voltage-Divider Circuit** Figure. 1.24 shows the diode compensation technique used in voltage-divider bias. Here, the diode is connected in series with the resistance $R_2$ and it is in forward-biased condition. Therefore,

$$I_E = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E}$$

and $$I_C \approx I_E$$

When $V_{BE}$ changes with temperature, $I_C$ also changes. To cancel the change in $I_C$, a diode is used at the base terminal to compensate the change in $V_{BE}$ as shown in Fig. 1.24. The voltage at the base, $V_B$, becomes

$$V_B = V_{R2} + V_D$$

Substituting in the above equation for $I_C$, we get

$$I_C \approx \frac{V_{R2} + V_D - V_{BE}}{R_E}$$

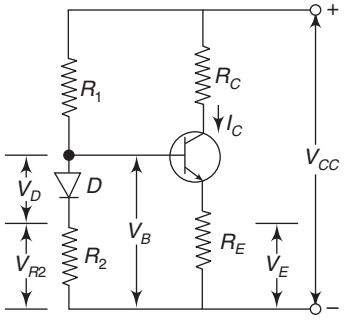



**Fig. 1.24** *Diode compensation in voltage-divider bias circuit*

If the diode is of the same material and type as the transistor, then the voltage across the diode will have the same temperature coefficient (2.5 mV/°C) as the base-to-emitter voltage $V_{BE}$. When $V_{BE}$ changes by a small amount with change in temperature, $V_D$ also changes by the same amount and thus, they cancel each other and the collector current remains constant. Therefore,

$$I_C = \frac{V_{R2}}{R_E}$$

The change in $V_{BE}$ due to temperature is compensated by a change in the diode voltage that keeps $I_C$ stable at the $Q$ point.

***Diode Compensation Against Variation in $I_{CO}$*** Figure 1.25 shows a transistor amplifier with a diode $D$ connected across the base–emitter junction for compensation of change in the collector saturation current $I_{CO}$. The diode is of the same material as the transistor and it is reverse biased by the base–emitter junction voltage $V_{BE}$, allowing the diode reverse saturation current $I_o$ to flow through the diode $D$. The base current $I_B = I - I_o$.

As long as temperature is constant, the diode $D$ operates as a resistor. As the temperature increases, $I_{CO}$ of the transistor increases. Hence, to compensate for this, the base current $I_B$ should be decreased.

The increase in temperature will also cause the leakage current $I_o$ through $D$ to increase and thereby decreasing the base current $I_B$. This is the required action to keep $I_C$ constant.

This method of bias compensation does not need a change in $I_C$ to effect the change in $I_B$, as both $I_o$ and $I_{CO}$ can track almost equally according to the change in temperature.

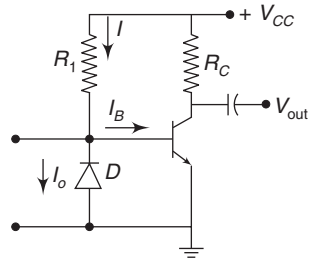



**Fig. 1.25** *Diode-bias compensation*

## 1.9 BIASING BJT SWITCHING CIRCUITS

When the transistor is biased either in the cut-off or saturation region, it can be used as a switching circuit. There are two types of switching circuit using BJT. They are:

(i) Direct-coupled BJT switching circuit and
(ii) Capacitive-coupled BJT switching circuit

### 1.9.1 Direct-Coupled BJT Switching Circuit

Fig.1.26 shows a direct-coupled switching circuit. Here, the signal source is connected to the base of the transistor through base resistor $R_B$. In the circuit shown in Fig. 1.26(a), when the input voltage $V_i$ is zero or negative, the base current will be zero i.e., $I_B \approx 0$ which results in zero collector current i.e., $I_C \approx 0$. Hence, the Q-point of the transistor is biased in the cut-off region leading to transistor in OFF state. Here, only the collector-base leakage current $I_{CBO}$ flows and it is very small, which can always be neglected. Therefore, the collector-emitter voltage $V_{CE}$ of the transistor is given by

$$V_{CE} = V_{CC} - I_C R_C$$

Since $I_C \approx 0$ for the transistor in OFF state, the voltage drop across $R_C$ will be zero.

Hence, $V_{CE} \approx V_{CC}$.

In Fig.1.26(b), when the input voltage $V_i$ is positive, there will be base current $V_B$ resulting in the maximum possible collector current $I_C$ level. Hence, the Q-point of the transistor is biased in the saturation region leading to transistor in ON state. Here, the collector current is limited only by the collector supply voltage $V_{CC}$ and the collector resistor $R_C$. Due to high $I_C$ for the transistor in ON state, there will be high voltage drop across $R_C$ and it is equivalent to $V_{CC}$ i.e., $I_C R_C \approx V_{CC}$. Therefore, the collector-emitter voltage $V_{CE}$ of the transistor is

$$V_{CE} = V_{CC} - I_C R_C \approx 0$$

Also, the base resistor $R_B$ and collector resistor $R_C$ for the transistor in ON state is

$$R_B = \frac{V_i - V_{BE}}{I_B} \quad \text{and} \quad R_C = \frac{V_{CC}}{I_C}$$

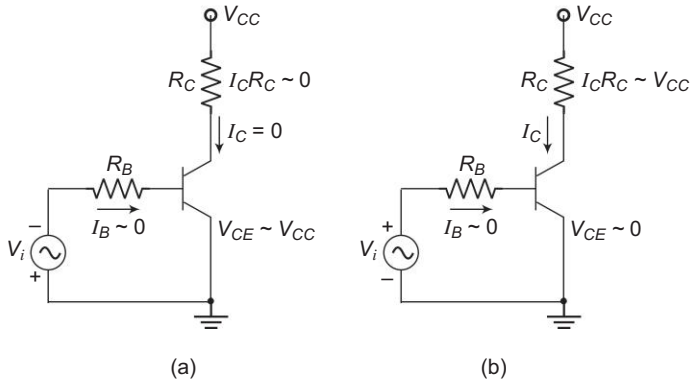



**Fig.1.26** *Direct-coupled BJT switching circuit in (a) OFF state and (b) ON state*

## 1.9.2 Capacitor-Coupled BJT Switching Circuit

Figure 1.27 shows the capacitor-coupled switching circuit using BJT. Here, the fixed bias of BJT biasing circuit is used with the exception that the BJT is biased into saturation. The fixed biasing at the base leads to poor amplification in amplifier circuit whereas it is quite satisfactory in switching circuit.

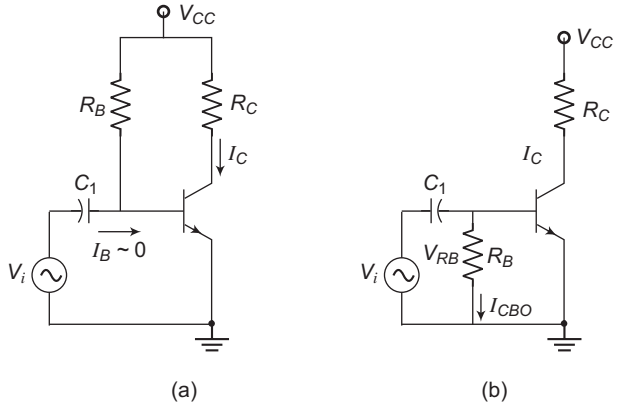



**Fig. 1.27(a)** *Capacitor-coupled BJT switching circuit with the transistor biased normally in* (a) ON state and (b) OFF state

Figure 1.27(a) shows the switching circuit with the transistor biased into saturation i.e., ON state in which $V_{CE} = V_{CE(sat)}$. As one end of the base resistor $R_B$ is connected directly to supply voltage $V_{CC}$, the transistor is initially in ON state and its base current is given by

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The collector current for the transistor is given by

$$I_C = \frac{V_{CC}}{R_C}$$

Now, the capacitor-coupled (pulse waveform) input at the base can switch the device into cut-off i.e., OFF state, which results in $V_{CE} = V_{CC}$.

Figure 1.27(b) shows the switching circuit with the transistor biased into cut-off i.e., OFF state. As one end of the base resistor $R_B$ is connected to ground, it keeps the base-emitter voltage $V_{BE}$ at zero level, to ensure that the device is in OFF state. When the transistor is OFF, the current that flows through $R_B$ is the collector-base leakage current $I_{CBO}$. Hence, the base resistor $R_B$ of the transistor is given by

$$R_B = \frac{V_{RB}}{I_{CBO}}$$

where $V_{RB}$ is the voltage drop across the base resistor $R_B$. The value of base resistor $R_B$ should be 22 kΩ or lower, which is enough to keep the transistor biased in OFF state. Now, the capacitor-coupled input voltage at the base can turn the transistor into saturation i.e., ON state, which results in $V_{CE} = V_{CE\,(sat)}$.

**EXAMPLE 1.28**

Design the capacitor-coupled switching circuit shown in Fig. 1.28.

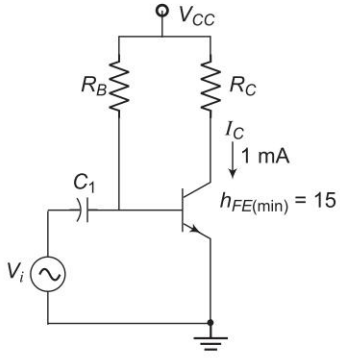



**Fig. 1.28**

**Solution** Collector resistance, $R_C \approx \dfrac{V_{CC}}{I_C} = \dfrac{12}{1\times10^{-3}} = 12\,\text{k}\Omega$

Base current, $I_B = \dfrac{I_C}{h_{FE(\min)}} = \dfrac{1\times10^{-3}}{15} = 66\,\mu\text{A}$

Base resistance, $R_B = \dfrac{V_{CC} - V_{BE}}{I_B} = \dfrac{12-0.7}{66\times10^{-6}} = 171.2\,\text{k}\Omega$

## 1.10 BIASING METHODS OF JFET

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point $Q$ stable in the central portion of the pinch-off region. The $Q$-point should be independent of device-parameter variations and ambient temperature changes. This can be achieved by suitably selecting the gate to source voltage ($V_{GS}$) and drain current ($I_D$) which is referred to as biasing.

### 1.10.1 Fixing the Q-point

The $Q$-point, the quiescent point or operating point for a self-biased JFET, is established by determining the value of drain current $I_D$ for a desired value of gate-to-source voltage, $V_{GS}$, or vice versa. However, if the data sheet of JFET includes a transfer characteristics curve, then the $Q$-point may be determined by using the procedure given below.

(i) Select a convenient value of drain current whose value is generally taken half of the maximum possible value of drain current, $I_{DSS}$. Then find the voltage drop across source resistor, $R_s$, by

$$V_s = I_D R_s$$

and the gate-to-source voltage from the equation

$$V_{GS} = -V_s$$

(ii) Plot the assumed value of drain current, $I_D$, and the corresponding gate-to-source voltage, $V_{GS}$, on the transfer characteristics curve.

(iii) Draw a line through the plotted point and the origin. The point of intersection of the line and the curve gives the desired $Q$-point. Then, read the coordinates of the $Q$-point.

It is necessary to fix the $Q$-point near the midpoint of the transfer characteristic curve of a JFET. The midpoint bias allows a maximum amount of drain current swing between the values of $I_{DSS}$ and the origin.

The following analytical method or graphical method can be used for the design of self-bias circuit.

***Analytical Method*** The values of the maximum drain current, $I_{DSS}$, and the gate-to-source cut-off voltage, $V_{GS(\text{off})}$ are noted down from the data sheets of JFET.

The value of the drain current is determined by

$$I_D = \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right]^2$$

For example, if we select the gate-to-source voltage, $V_{GS} = \dfrac{V_{GS(\text{off})}}{4}$ then the value of the drain current will be

$$I_D = I_{DSS}\{1 - 0.25\}^2 = I_{DSS}(0.75)^2 = 0.56\, I_{DSS}$$

Here, the drain current is slightly more than one-half of $I_{DSS}$. But it will bias the JFET close to the mid-point of the curve. The value of the drain resistor, $R_D$, is selected in such a way that the drain voltage, $V_D$, is equal to half the drain supply voltage, $R_D$. The value of gate resistor, $R_G$, is chosen arbitrarily large, so that it prevents loading on the driving stages.

***Graphical Method*** A self-bias line is drawn such that it intersects the transfer characteristic curve near its midpoint giving the required $Q$-point. Then the coordinates of the $Q$-point are obtained. The value of source resistance, $R_s$, is expressed by the ratio of gate-to-source voltage, $V_{GS}$, to the drain current, $I_D$.

Therefore, the source resistance is given by

$$R_s = \frac{V_{GS}}{I_D}$$

However, a more accurate method is to draw a self-bias line through the coordinates of $I_{DSS}$ and $V_{GS(\text{off})}$ as shown in Fig. 1.29. Then the point of intersection of self-bias line and the transfer characteristic curve locates the $Q$-point. The value of the source resistor is expressed by the relation

$$R_S = \frac{V_{GS(\text{off})}}{I_{DSS}}$$

The value of drain resistor, $R_D$, and the gate resistor, $R_G$, are selected in the same way as discussed above for the analytical method.

An FET may have a combination of self-bias and fixed bias to provide stability of the quiescent drain current against device and temperature variations.

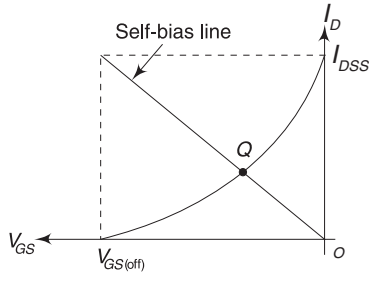



**Fig. 1.29** *Self-bias line through $I_{DSS}$ and $V_{GS(off)}$*

## 1.10.2 Self-bias

Figure 1.30 shows the self-bias circuit for an *N*-channel FET. When the drain voltage $V_{DD}$ is applied, a drain current $I_D$ flows even in the absence of gate voltage ($V_G$). The voltage drop across the resistor $R_s$ produced by the drain current is given by $V_s = I_D R_s$. This voltage drop reduces the gate -to-source reverse voltage required for FET operation. The feedback resistor $R_s$ prevents any variation in FET drain current.

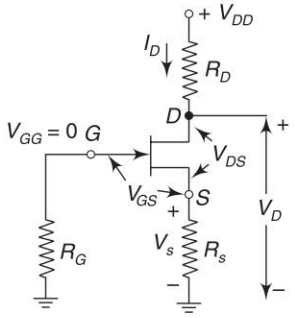



**Fig. 1.30** *Self-bias circuit for an N-channel JFET*

The drain voltage, $V_D = V_{DD} - I_D R_D$

The drain-to-source voltage,

$$V_{DS} = V_D - V_s = (V_{DD} - I_D R_D) - I_D R_s$$
$$= V_{DD} - I_D(R_D + R_s)$$

The gate-to-source voltage

$$V_{GS} = V_{GG} - V_s = 0 - I_D R_s = - I_D R_s$$

When drain current increases, the voltage drop across $R_s$ increases. The increased voltage drop increases the reverse gate-to-source voltage, which decreases the effective width of the channel and, hence, reduces the drain current. Now, the reduced drain current decreases the gate-to-source voltage which, in turn, increases the effective width of the channel thereby increasing the value of drain current.

## 1.10.3 Voltage-Divider Bias

Figure 7.45(a) shows the voltage-divider bias circuit and its Thevenin's equivalent is shown in Fig. 1.31(b). Resistors $R_1$ and $R_2$ connected on the gate side form a voltage divider. The gate voltage,

$$V_{GG} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} \quad \text{and} \quad R_G = \frac{R_1 R_2}{R_1 + R_2}$$

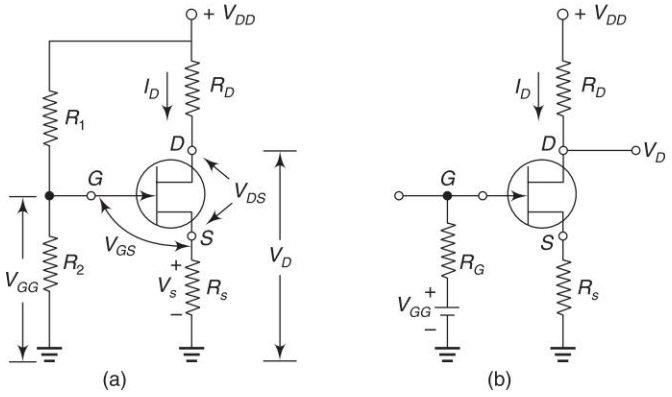



**Fig. 1.31** *(a) Voltage-divider bias circuit (b) Thevenin's equivalent circuit*

The bias satisfies the equation $V_{GS} = V_{GG} - I_D R_s$.

The drain-to-ground voltage, $V_D = V_{DD} - I_D R_D$. If the gate voltage $V_{GG}$ is very large compared to gate-to-source $V_{GS}$, the drain current is approximately constant. In practice, the voltage-divider bias is less effective with JFET than BJT.

This is because, in a BJT, $V_{BE} \approx 0.7$ (silicon) with only minor variations from one transistor to another. But in a JFET, the $V_{GS}$ can vary several volt from one JFET to another.

### 1.10.4 Fixed Bias

The FET device needs dc bias for setting the gate-to-source voltage $V_{GS}$ to give desired drain-current $I_D$. For a JFET, the drain current is limited by $I_{DSS}$. Since the FET has a high input impedance, it does not allow the gate current to flow and the dc voltage of the gate set by a voltage divider or a fixed battery is not affected or loaded by the FET.

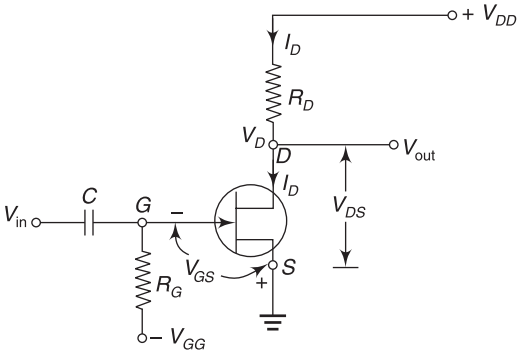



**Fig. 1.32** *Fixed bias circuit for an N-Channel JFET*

The fixed bias circuit for an *N*-channel JFET shown in Fig. 7.46 is obtained by using a supply $V_{GG}$. This supply ensures that the gate is always negative with respect to source and no current flows through resistor $R_G$ and gate terminal, i.e., $I_G = 0$. The $V_{GG}$ supply provides a voltage $V_{GS}$ to bias the *N*-channel JFET, but no resulting current is drawn from the battery $V_{GG}$. Resistor $R_G$ is included to allow any ac signal applied through capacitor *C* to develop across $R_G$. While any ac signal will develop across $R_G$, the dc voltage drop across $R_G$ is equal to $I_G R_G$ which is equal to zero volt.

Then, the gate to source voltage $V_{GS}$ is

$$V_{GS} = V_G - V_s = -V_{GG} - 0 = -V_{GG}$$

The drain-source current $I_D$ is then fixed by the gate-source voltage. This current will cause a voltage drop the drain resistor $R_D$ and is given as

$$V_{DD} = I_D R_D + V_{DS}$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

## 1.11 MOSFET BIASING

### 1.11.1 Biasing of Enhancement MOSFET

Figure 1.33 shows the drain-to-gate bias circuit for enhancement mode MOSFET. Here, the gate bias voltage is

$$V_{GS} = \left[\frac{R_1}{R_1 + R_f}\right] V_{DS}$$

This circuit offers the dc stabilization through the feedback resistor $R_f$. However, the input resistance is reduced because of Miller effect.

Also, the voltage-divider biasing technique given for JFET can be used for the enhancement MOSFET. Here, the dc stability is accomplished by the dc feedback through $R_s$.

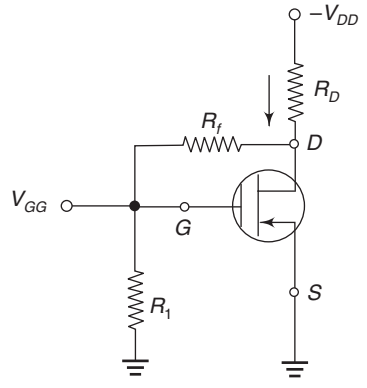



**Fig. 1.33** *Drain-to-gate bias circuit for enhancement MOSFET*

But the self-bias technique given for JFET cannot be used for establishing an operating point for the enhancement MOSFET because the voltage drop across $R_s$ is in a direction to reverse-bias the gate and it actually needs forward-gate bias.

Figure 1.34 shows an *N*-channel enhancement mode MOSFET common-source circuit with source resistor. The gate voltage is

$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

and the gate-to-source voltage is

$$V_{GS} = V_{DD} - V_G$$

Assuming that $V_{GS} > V_{TN}$ and the MOSFET is biased in the saturation region, the drain current is

$$I_D = K_N(V_{GS} - V_{TN})^2$$

Here, the threshold voltage $V_{TN}$ and conduction parameter $K_N$ are functions of temperature.

The drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D$$

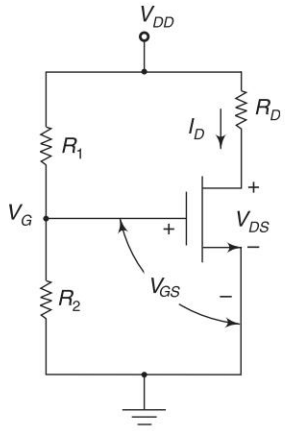



**Fig. 1.34** *N-channel enhancement mode MOSFET common-source circuit with source resistor*

If $V_{DS} > V_{DS\,(sat)} = V_{GS} - V_{TN}$, then the MOSFET is biased in the saturation region. If $V_{DS} < V_{DS\,(sat)} = V_{GS} - V_{TN}$, then the MOSFET is biased in the non-saturation region, and the drain current is given by

$$I_D = K_N\,[2(V_{GS} - V_{TN})\,V_{DS} - V_{DS}^2]$$

## 1.11.2 Biasing of Depletion MOSFET

Both the self-bias technique and voltage-divider bias circuit given for JFET can be used to establish an operating point for the depletion-mode MOSFET.

### EXAMPLE 1.29

Calculate the operating point of the self-biased JFET having the supply voltage $V_{DD} = 20$ V, maximum value of drain current $I_{DSS} = 10$ mA and $V_{GS} = -3$ V at $I_D = 4$ mA. Also, determine the values of resistors $R_D$ and $R_s$ to obtain this bias condition.

**Solution** We know that the value of drain current at *Q*-point,

$$I_{DQ} = \frac{I_{DSS}}{2} = \frac{10 \times 10^{-3}}{2} = 5 \text{ mA}$$

and the value of drain-to-source voltage at *Q*-point,

$$V_{DSQ} = \frac{V_{DD}}{2} = \frac{20}{2} = 10 \text{ V}$$

Therefore, the operating point is at $V_{DS} = 10$ V and $I_D = 5$ mA.

Also, we know that the drain-to-source voltage,

$$V_{DS} = V_{DD} - I_D R_D$$

$$10 = 20 - (4 \times 10^{-3})\,R_D$$

Therefore, $$R_D = \frac{20 - 10}{4 \times 10^{-3}} = 2.5 \text{ k}\Omega$$

The source voltage or voltage across the source resistor $R_s$ is

$$V_s = -V_{GS} = -3 \text{ V}$$

Also, $$V_s = I_D R_s, \quad \text{i.e.,} \quad 3 = (4 \times 10^{-3})\, R_s$$

Therefore, $$R_s = \frac{3}{4 \times 10^{-3}} = 750\ \Omega$$

## EXAMPLE 1.30

Calculate the values of $R_s$ required to self-bias an *N*-channel JFET with $I_{DSS}$ = 40 mA, $V_P = -10$ V and $V_{GSQ} = -5$ V.

**Solution** We know that $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

Substituting the given values, we get

$$I_D = 40 \times 10^{-3}\left[1 - \frac{(-5)}{(-10)}\right]^2 = 10 \text{ mA}$$

Therefore, $$R_s = \left|\frac{V_{DSQ}}{I_D}\right| = \frac{5}{10 \times 10^{-3}} = 500\ \Omega$$

## EXAMPLE 1.31

A JFET amplifier with a voltage-divider biasing circuit, shown in Fig. 1.31, has the following parameters: $V_P = -2$ V, $I_{DSS}$ = 4 mA, $R_D$ = 910 Ω, $R_s$ = 3 kΩ, $R_1$ = 12 MΩ, $R_2$ = 8.57 MΩ and $V_{DD}$ = 24 V. Find the value of the drain current $I_D$ at the operating point. Verify whether the FET will operate in the pinch-off region.

**Solution** We obtain

$$V_{GG} = V_{DD}\frac{R_2}{R_1 + R_2} = 24 \times \frac{8.57 \times 10^6}{(12 + 8.57) \times 10^6} = 10 \text{ V}$$

We know that

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{V_{GG} - I_D R_s}{V_P}\right)^2, \text{ where } V_{GS} = V_{GG} - I_D R_s$$

Expressing $I_D$ and $I_{DSS}$ in mA and $R_S$ in kΩ, we have

$$I_D = 4 \times \left(1 - \frac{10 - I_D \times 3}{-2}\right)^2$$

i.e., $9I_D^2 - 73I_D + 144 = 0$

Therefore, $I_D = 3.39$ mA or 4.72 mA

As $I_D = 4.72$ mA > 4 mA = $I_{DSS}$, this value is inappropriate. So, $I_{DQ} = 3.39$ mA is selected.

Therefore,

$$V_{GSQ} = V_{GG} - I_{DQ}R_s$$
$$= 10 - (3.39 \times 10^{-3} \times 3 \times 10^3) = -0.17 \text{ V}$$

and $$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_s)$$
$$= 24 - 3.39 \times 10^{-3} (0.91 + 3) \times 10^3 = 10.745 \text{ V}$$

Then $$V_{DGQ} = V_{DSQ} - V_{GQS}$$
$$= 10.745 + 0.17 = 10.915 \text{ V}$$

which is greater than $|V_P| = 2$ V. Hence, the FET is in the pinch-off region.

## EXAMPLE 1.32

A voltage-divider bias is provided to an *N*-channel JFET circuit as shown in Fig. 1.35. To establish $I_{DSS} = 10$ mA, $V_P = -3.5$ V, $R_1 + R_2 = 20$ kΩ, $I_D = 5$ mA and $V_{DS} = 5$ V, determine the values of $R_1$, $R_2$ and $R_D$.

**Solution** Let us assume that the JFET is biased in the saturation region. Then the dc drain current is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Therefore, $$5 = 10\left(1 - \frac{V_{GS}}{(-3.5)}\right)^2$$

By solving, we get $V_{GS} = -1.008$ V

The voltage at the source terminal is

$$V_s = I_D R_s - 5 = (5 \times 10^{-3})(0.5 \times 10^3) - 5 = -2.5 \text{V}$$

The gate voltage is

$$V_G = V_{GS} + V_s = -1.008 - 2.5 = -3.508 \text{ V}$$

The gate voltage can be written as

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5$$

Therefore, $$-3.508 = \frac{R_2}{20 \times 10^3}(10) - 5$$

i.e., $R_2 = 2.984$ kΩ

and $R_1 = 117.016$ kΩ

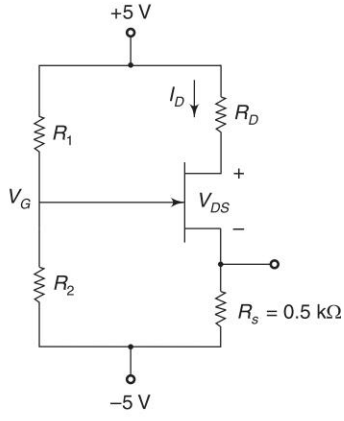



**Fig. 1.35**

The drain-to-source voltage is

$$V_{DS} = 5 - I_D R_D - I_D R_s - (-5)$$

Substituting the specified values, we get

$$R_D = \frac{10 - V_{DS} - I_D R_s}{I_D}$$

$$= \frac{10 - 5 - (5)(0.5)}{5} = 0.5\ \text{k}\Omega$$

$$V_{GS} - V_P = -1.24 - (-3.5) = 2.26\ \text{V}$$

Here, since $V_{DS} > (V_{GS} - V_P)$, the JFET is biased in the saturation region, which satisfies the initial assumption.

## EXAMPLE 1.33

For the circuit shown in Fig. 1.36, find the values of $V_{DS}$ and $V_{GS}$. Given, $I_D = 5$ mA, $V_{DD} = 10$ V, $R_D = 1$ kΩ and $R_s = 500$ Ω.

**Solution**

$$V_{GG} = V_{GS} + I_D R_s$$

Since $V_{GG} = 0$,

$$V_{GS} = -I_D R_s$$

$$= -5 \times 10^{-3} \times 500 = -2.5\ \text{V}$$

We know that $V_{DD} = I_D(R_D + R_s) + V_{DS}$

Therefore, $V_{DS} = V_{DD} - I_D(R_D + R_s)$

$$= 10 - 5 \times 10^{-3}\ (1500)$$

$$= 2.5\ \text{V}$$

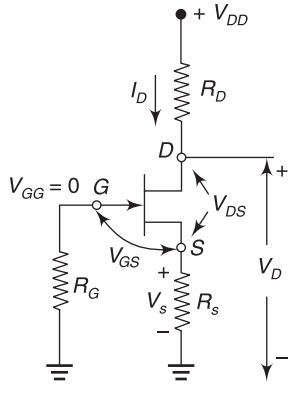



**Fig. 1.36**

## EXAMPLE 1.34

Determine the following for the network shown in Fig. 1.37.

(a) $V_{GSQ}$ (b) $V_{DS}$ (c) $V_D$ (d) $V_G$ (e) $V_s$

**Solution**

(a) $V_{GSQ} = -V_{GG} = -3\text{V}$

(b) $$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 12 \times 10^{-3}\left[1 - \left(\frac{-3}{-6}\right)\right]^2 = 3\ \text{mA}$$

$$V_{DS} = V_{DSQ} = V_{DD} - I_{DQ} R_D$$

$$= 35 - 3 \times 10^{-3} \times 3.5 \times 10^3 = 24.5\ \text{V}$$

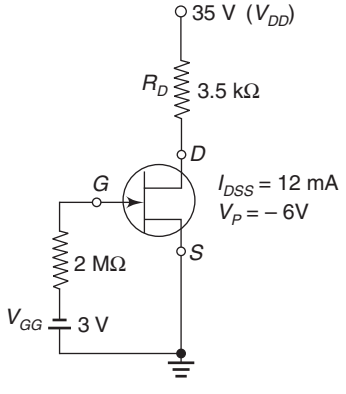



**Fig. 1.37**

(c) $V_D = V_{DS} + V_s = 24.5 + 0 = 24.5$ V

(d) $V_G = -3$V

(e) $V_s = 0$ V

## EXAMPLE 1.35

Determine $I_{DQ}$, $V_{GSQ}$, $V_D$, $V_{DS}$, and $V_{DG}$ for the given network shown in Fig. 1.38.

**Solution** *To find expression for* $V_{GS}$

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{270 \times 10^3}{(2100 + 270) \times 10^3} \times 20 = 2.28 \text{ V}$$

$$V_s = 1.5\, I_D$$

Therefore, $V_{GS} = V_G - V_s = (2.28 - 1.5\, I_D)$

*To find* $I_D$*:*

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{ mA}$$

$$I_D = 8\left[1 - \frac{(2.28 - 1.5\, I_D)}{-4}\right]^2 \text{ mA}$$

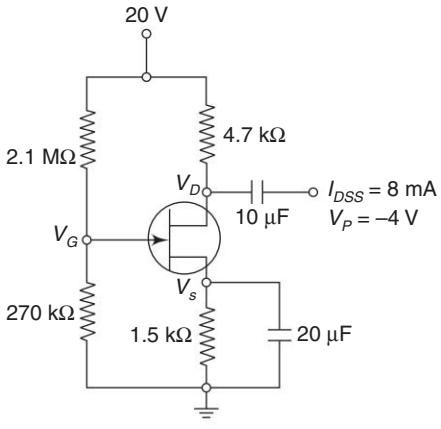



**Fig. 1.38**

Therefore, $I_D = \frac{8}{16}[4 + 2.28 - 1.5\, I_D]^2 = 0.5\,(6.28 - 1.5\, I_D)^2$

$$2I_D = 39.44 - 18.84\, I_D + 2.25\, I_D^2$$

$$2.25\, I_D^2 - 20.84\, I_D + 39.44 = 0$$

Therefore, $$I_D = \frac{20.84 \pm \sqrt{(20.84^2 - (4 \times 2.25 \times 39.44)}}{2 \times 2.25} = 6.6 \text{ mA or } 2.6 \text{ mA}$$

For $I_D = 6.6$ mA, $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$$= 20 - 6.6 \times 10^{-3}(4.7 + 15) \times 10^3 = -20.92$$

Since $V_{DS}$ is negative, this value may be neglected. Let us choose $I_D = 2.65$ mA.

Therefore, $I_{DQ} = 2.65$ mA.

*To find* $V_{GSQ}$*:*

$$V_{GSQ} = 2.28 - 1.5\, I_{DQ} = 2.28 - (1.5 \times 2.65) = -1.695 \text{ V}$$

*To find* $V_{DSQ}$*:*

$$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_s)$$

Therefore, $$V_{DSQ} = 20 - 2.65 \times 10^{-3}\,(4.7 + 1.5) \times 10^{-3} = 3.57 \text{ V}$$

*To find* $V_D$*,* $V_s$ *and* $V_{DG}$*:*

$$V_s = I_D R_s = 2.65 \times 10^{-3} \times 1.5 \times 10^{-3} = 3.975 \text{ V}$$

$$V_D = V_s + V_{DS} = 3.975 + 3.57 = 7.545 \text{ V}$$

Hence, $$V_{DG} = V_D - V_G = 7.545 - 2.28 = 5.265 \text{ V}$$

## EXAMPLE 1.36

For the given measurement $V_s = 1.7$ V for the network as shown in Fig. 1.39, determine

(a) $I_{DQ}$ (b) $V_{GSQ}$
(c) $I_{DSS}$ (d) $V_D$
(e) $V_{DS}$

**Solution** Given, $V_s = 1.7$ V

(a) $$V_s = I_D R_s$$

$$I_{DQ} = \frac{V_s}{R_s} = \frac{1.7}{510} = 3.33 \text{ mA}$$

(b) $$V_{GSQ} = V_G - V_s = -V_s = -1.7 \text{ V}$$

(c) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_{DSS} = \frac{I_D}{\left(1 - \frac{V_{GS}}{V_P}\right)^2} = \frac{3.33 \times 10^{-3}}{\left(1 - \frac{(-1.7)}{(-4)}\right)^2} = 10 \text{ mA}$$

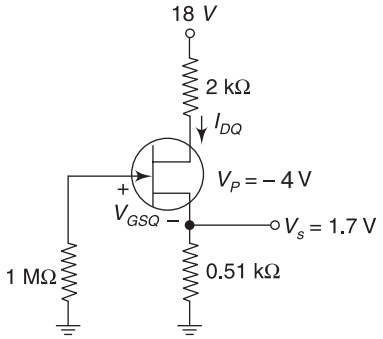



**Fig. 1.39**

(d) $$V_D = V_{DD} - I_D R_D = 18 - 3.33 \times 10^{-3} \times 2 \times 10^3 = 11.34 \text{ V}$$

(e) $$V_{DS} = V_D - V_s = 11.34 - 1.7 = 9.64 \text{ V}$$

## EXAMPLE 1.37

For the circuit shown in Fig. 1.40, calculate $V_0$, $Z_i$, and $Z_0$. Given input is $V_i = 0.2$ V(rms), $I_{DSS} = 9$ mA and $V_P = -4.5$ V.

**Solution**

$$Z_i = R_G = 10 \text{ M}\Omega$$

$$I_D = I_{DD}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 9 \times 10^{-3}\left(1 - \frac{-I_D R_s}{V_P}\right)^2$$

$$= 9 \times 10^{-3}\left(1 - \frac{(-1000\, I_D)}{-4.5}\right)^2$$

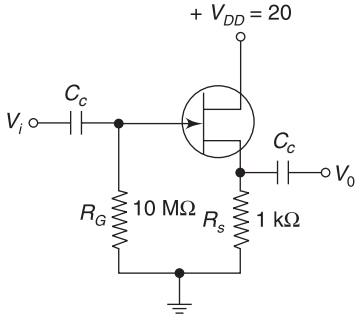



**Fig. 1.40**

$$= 9 \times 10^{-3} (1 - 222.22\, I_D)^2$$

$$= 9 \times 10^{-3}(1 - 444.44\, I_D + 49383 I_D^2)$$

$$I_D = 9 \times 10^{-3} - 4 I_D + 444.45\, I_D^2$$

Therefore, $444.45\, I_D^2 - 5 I_D + 9 \times 10^{-3} = 0$

Solving the quadratic equation, we get

$$I_D = 2.25 \text{ mA or } 9 \text{ mA}$$

Since $I_D < I_{DSS}$, we take $I_D = 2.25$ mA. Therefore,

$$g_{mo} = \frac{2 I_{DSS}}{|V_P|} = \frac{2 \times (9 \times 10^{-3})}{4.5} = 4 \text{ mS}$$

$$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_P}\right)$$

where $V_{GSQ} = - I_D R_s = - 2.25 \times 10^{-3} \times 1000 = - 2.25$ V

$$g_m = 4 \times 10^{-3}\left(1 - \frac{(2.25)}{(-4.5)}\right) = 2 \text{ mS}$$

$$Z_o = \frac{1}{g_m} \| R_s = \frac{1}{2 \times 10^{-3}} \| 1 \times 10^3 = 333.33\ \Omega$$

$$A_V = \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)} = \frac{g_m R_s}{1 + g_m R_s} = \frac{2 \times 10^{-3} \times 1 \times 10^3}{1 + (2 \times 10^{-3} \times 1 \times 10^3)} = 0.667$$

$$V_o = V_i \times A_V = 0.2 \times 0.667 = 0.133 \text{ V}$$

## EXAMPLE 1.38

An *N*-channel JFET having $V_P = - 4$ V and $I_{DSS} = 10$ mA is used in the circuit of Fig. 1.41. The parameter values are $V_{DD} = 18$ V, $R_s = 2\text{k}\Omega$, $R_1 = 450$ k$\Omega$, and $R_2 = 90$ k$\Omega$. Determine $I_D$ and $V_{DS}$.

**Solution**

*To find* $V_{GS}$

$$V_{GS} = V_G - I_D R_s$$

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{90 \times 10^3}{(450 + 90) \times 10^3} \times 18 = 3 \text{ V}$$

Therefore, $V_{GS} = (3 - 2 \times 10^3\, I_D)$

*To find* $I_D$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = 10 \times 10^{-3}\left[1 - \frac{(3 - 2 \times 10^3\, I_D)}{-4}\right]^2$$

$$= \frac{10 \times 10^{-3}}{16}[-4 - 3 + 2 \times 10^3\, I_D]^2$$

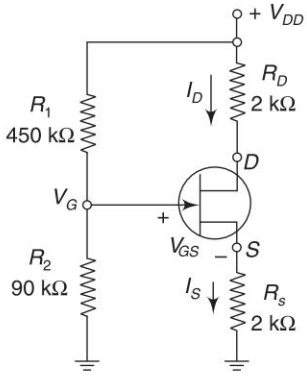



**Fig. 1.41**

Therefore, $1.6\, I_D = 10^{-3}\,[-7 - 2 \times 10^3\, I_D]^2$

$= 0.049 - 28\, I_D + 4 \times 10^3\, I_D^2$

$4 \times 10^3\, I_D^2 - 29.6\, I_D + 0.049 = 0$

$$I_D = \frac{29.6 \pm \sqrt{(29.6)^2 - 4 \times 4 \times 10^3 \times 0.049}}{2 \times 4 \times 10^3}$$

Therefore, $I_D = 4.9$ mA or 2.5 mA

If $I_D = 4.9$ mA, then

$V_{DS} = V_{DD} - I_D\,(R_D + R_S)$

$= 18 - 4.9 \times 10^{-3}\,(2 + 2) \times 10^3 = -3.6$ V

Since $V_{DS}$ would be negative, this value of $I_D$ is not acceptable

Therefore, $I_{DQ} = 2.5$ mA

*To find* $V_{DS}$*:*

$$V_{DS} = V_{DD} - I_{DQ}(R_D + R_s) = 18 - 2.5 \times 10^{-3}\,(2 + 2) \times 10^3 = 8 \text{ V}$$

## EXAMPLE 1.39

Determine $V_{GS}$, $I_D$, $V_{DS}$, $V_D$ and $V_G$ for the circuit shown in Fig. 1.42.

**Solution** *To find* $V_{GSQ}$

For a self-bias circuit, $V_{GSQ} = -I_D R_s = -I_D \times 10^3$

*To find* $I_D$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = 8 \times 10^{-3}\left[1 + \frac{(1 \times 10^3\, I_D)}{-6}\right]^2$$

$$= 8 \times 10^{-3}\left[1 - \frac{1000\, I_D}{6}\right]^2$$

Therefore, $36\, I_D = 8 \times 10^{-3}\,[6 - 1000\, I_D]^2$

$= 8 \times 10^{-3}\,[36 - 12 \times 10^3\, I_D + 10^6\, I_D^2]$

Hence, $8 \times 10^3\, I_D^2 - 132 I_D + 0.288 = 0$

$$I_D = \frac{132 \pm \sqrt{(132)^2 - 4 \times 8 \times 10^3 \times 0.288}}{2 \times 8 \times 10^3}$$

Therefore, $I_D = 13.9$ mA or 2.5 mA

But $I_D$ cannot be higher than $I_{DSS}$, Therefore, $I_D = 2.5$ mA

*To find* $V_{DS}$

$$V_{DS} = V_{DD} - I_D\,(R_D + R_s) = 20 - 2.5 \times 10^{-3}(3.3 + 1) \times 10^3 = 9.25 \text{ V}$$

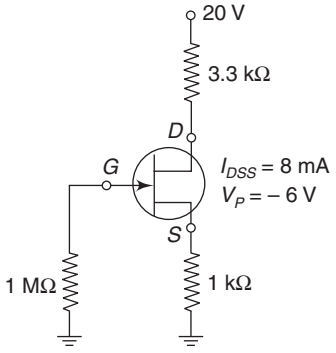



**Fig. 1.42**

*To find $V_{GS}$, $V_D$ and $V_s$*

$$V_{GS} = 1 \times 10^3 \times I_D = 1 \times 10^3 \times 2.5 \times 10^{-3} = 2.5 \text{ V}$$

$$V_s = I_D R_s = 2.5 \times 10^{-3} \times 1 \times 10^3 = 2.5 \text{ V}$$

$$V_D = V_s + V_{DS} = 2.5 + 9.25 = 11.75 \text{ V}$$

## EXAMPLE 1.40

For the network shown in Fig. 1.43, determine the values of $V_{DSQ}$, $I_{DQ}$, $V_D$, $V_G$, $V_S$ and $V_{DS}$.

**Solution**

$$V_G = 0, V_s = I_D R_s$$

$$V_{GS} = V_G - V_s = 0 - I_D R_s = -680\, I_D$$

*To find $I_D$*

We know that $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 12 \times 10^{-3}\left(1 - \left(\frac{-680\, I_D}{-6}\right)\right)^2$$

$$= 154.12\, I_D^2 - 3.7 I_D + 0.012 = 0$$

Therefore, $$I_D = \frac{3.7 \pm \sqrt{13.69 - 7.39}}{308.24}$$

$$= 20 \text{ mA or } 3.8 \text{ mA}$$

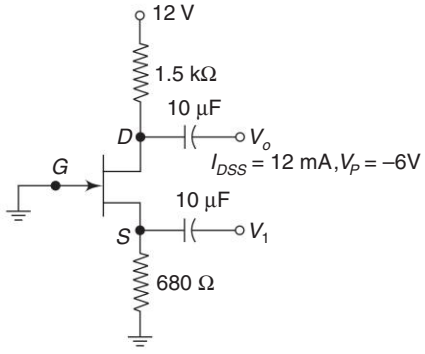



**Fig. 1.43**

Since $I_D$ is less than $I_{DSS}$, $I_{DQ} = 3.8$ mA

*To find $V_{GSQ}$*

$$V_{GSQ} = -680\, I_D = -680 \times 3.8 \times 10^{-3} = -3.6 \text{ V}$$

*To find $V_s$*

$$V_s = I_D R_s = 3.8 \times 10^{-3} \times 680 = 2.58 \text{ V}$$

*To find $V_{DS}$*

$$V_{DS} = V_{DD} - I_D(R_D + R_s)$$

$$= 12 - 3.8 \times 10^{-3}(1.5 \times 10^3 + 680) = 12 - 8.28 = 3.72 \text{ V}$$

*To find $V_D$:*

$$V_D = V_s + V_{DS} = 2.58 + 3.72 = 6.3 \text{ V}$$

## EXAMPLE 1.41

For the common-source *N*-channel MOSFET circuit shown in Fig. 1.44(a) with the threshold voltage $V_{TN} = 1.5$ V, conduction parameter $K_N = 1$ mA/V$^2$, the channel-length modulation parameter $\lambda = 0.01$ V$^{-1}$, $R_i = R_1 \parallel R_2 = 100$ kΩ and the current at the transition point $I_{Dt} = 4$ mA. Design the MOSFET circuit with voltage-divider bias such that $I_{DQ} = 1.5$ mA and *Q*-point is in the middle of the saturation region.

**Solution** *To determine* $V_{DSt}$:

We know that $I_{Dt} = K_N(V_{GSt} - V_{TN})^2$

i.e., $4 \times 10^{-3} = 1 \times 10^{-3} (V_{GSt} - 1.5)^2$

where the subscript *t* indicates transition point values.

Solving, we get $V_{GSt} = 3.5$ V

Therefore, $V_{DSt} = V_{GSt} - V_{TN} = 3.5 - 1.5 = 2$ V

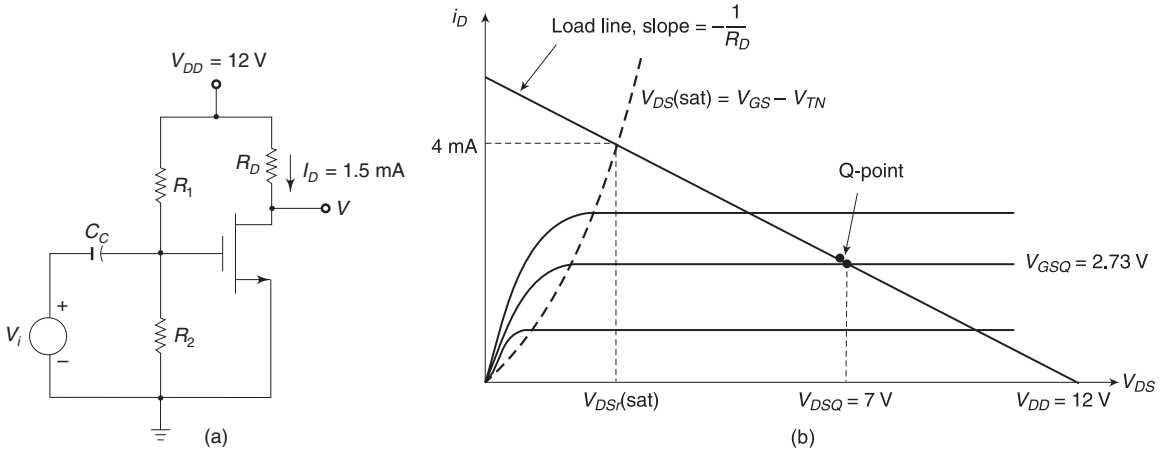



**Fig. 1.44**

Referring to Fig. 1.44(b), if the *Q*-point is in the middle of the saturation region then $V_{DSQ} = 7$ V, which gives 10 V peak-to-peak symmetrical output voltage.

Therefore, $V_{DSQ} = V_{DD} - I_{DQ}R_D$

i.e., $$R_D = \frac{V_{DD} - V_{DSQ}}{I_{DQ}} = \frac{12 - 7}{1.5 \times 10^{-3}} = 3.33 \text{ k}\Omega$$

Then, $$I_{DQ} = K_N (V_{GSQ} - V_{TN})^2$$

$$1.5 \times 10^{-3} = 1 \times 10^{-3} (V_{GSQ} - 1.5)^2$$

Therefore, $V_{GSQ} = 2.73$ V

Then, $$V_{GSQ} = 2.73 = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{1}{R_1}\right)\left(\frac{R_1 R_2}{R_1 + R_2}\right)(V_{DD})$$

$$2.73 = \frac{R_i}{R_1}(V_{DD}) = \frac{(100 \times 10^3)(12)}{R_1}$$

By solving, we get $R_1 = 439.6$ kΩ and $R_2 = 129.45$ kΩ

**EXAMPLE 1.42**

For the *N*-channel depletion-mode MOSFET circuit shown in Fig. 1.45. $V_{TN} = -2$ V and $K_N = 0.1$ mA/V$^2$. Assume that $V_{DD} = 5$ V and $R_s = 5$ kΩ. Determine $I_D$ and $V_{DS}$.

**Solution** Let us assume that the MOSFET is biased in the saturation region. Then the dc drain current is

$$I_D = K_N (V_{GS} - V_{TN})^2$$
$$= K_N (-V_{TN})^2$$
$$= (0.1)(-(-2))^2 = 0.4 \text{ mA}$$

The dc drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_s$$
$$= 5 - (0.4)(5) = 3 \text{ V}$$

Then,
$$V_{DS(\text{sat})} = V_{GS} - V_{TN}$$
$$= 0 - (-2) = 2 \text{ V}$$

Since $V_{DS} > V_{DS(\text{sat})}$, the MOSFET is biased in the saturation region.

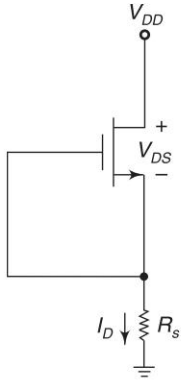



**Fig. 1.45**

## 1.12 BIASING FET SWITCHING CIRCUITS

When a JFET or MOSFET is used as a switching circuit, it will operate either in OFF state or ON state. The biasing of JFET and MOSFET switching circuits are discussed in this section.

### 1.12.1 JFET Switching

When the drain current of JFET is zero, the JFET device is in OFF state with a small drain-source leakage current, which can always be ignored. When the drain-source voltage is small, the device will be in ON state. Here, the voltage drop across the drain and source $V_{DS(\text{ON})}$ depends on the drain current $I_D$ and the channel resistance $r_{DS(\text{ON})}$. It is given by

$$V_{DS(\text{ON})} = I_D r_{DS(\text{ON})}$$

Generally, the channel resistance is very low for junction field effect transistors when used in switching applications. There are two types of switching circuit using JFET. They are

(i) Direct-coupled JFET switching circuit

(ii) Capacitive coupled JFET switching circuit

***Direct-coupled JFET switching circuit*** Figure 1.46(a) shows a direct-coupled switching circuit using N-channel JFET and the input/output waveforms are shown in Fig. 1.46(b).

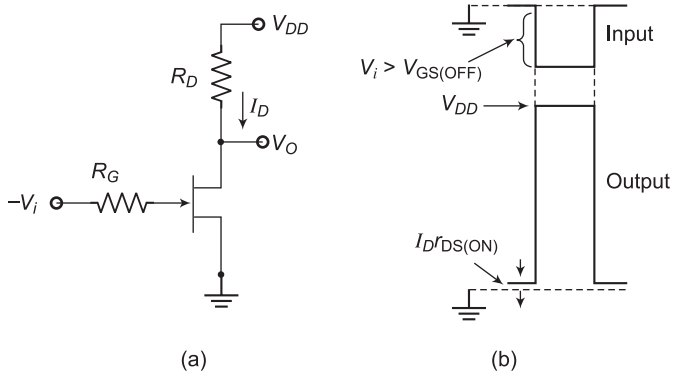



**Fig. 1.46** *JFET switching circuit (a) Direct-coupled circuit and (b) input/output waveforms*

When the JFET gate and source voltages are equal, i.e., $V_i = 0$, the depletion region will not penetrate into the channel. As a result, the output voltage will be $V_O = V_{DS(ON)} = I_D r_{DS(ON)}$. The device goes to OFF state when the input voltage $V_i$ becomes greater than the gate-source cut-off voltage. As a result, the output voltage will be maximum i.e., equal to $V_{DD}$ as shown in Fig. 1.46(b).

With very small drain-source voltage, the device will be in ON state. Also, from Fig. 1.46(a), we know that $V_{DD} \approx I_D R_D$. From this equation, the drain current $I_D$ can be determined by knowing the values of $V_{DD}$ and $R_D$. The drain-source voltage $V_{DS(ON)}$ can be determined by knowing the values of $r_{DS(ON)}$ and $I_D$ The drain-source leakage current specified for the device should be smaller than the drain current.

To switch back to OFF state, the input voltage $V_i$ of JFET should be made greater than the maximum gate-source cut-off voltage. At the same time, $V_i$ should not be large that the drain-gate voltage ($V_{DG} = V_{DD} + V_i$) reaches the breakdown voltage. Based on thumb rule, in OFF state, the input voltage is selected 1 V greater than $V_{GS(OFF)max}$.

ie., $$V_i = -V_{GS(OFF)max} + 1V$$

The gate resistor $R_G$ used in the switching circuit is mainly used to limit the gate current when gate-source junction of JFET becomes forward biased. Using higher resistance values for $R_G$ may reduce the switching speed of the circuit. Therefore, smaller values are always preferred for gate resistance.

***Capacitor-coupled JFET switching circuit*** Figure 1.47 shows two capacitor-coupled JFET switching circuits. When the gate-source voltage of JFET is zero, i.e., $V_{GS} = 0$, the device will be in ON state as seen in Fig. 1.47(a). When the negative biased gate-source voltage ($-V_{GS}$) of JFET is greater than the pinch-off voltage, the device will be in OFF state as seen in Fig. 1.47(b).

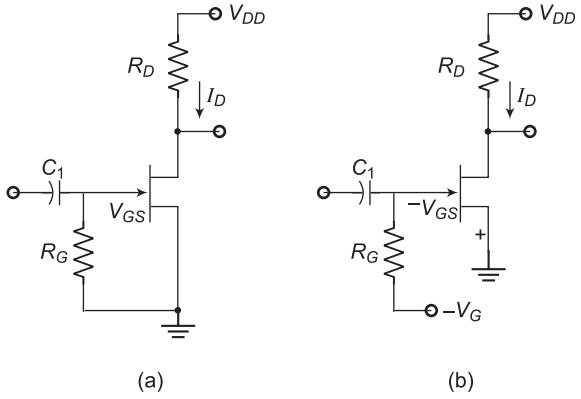



**Fig. 1.47** *Capacitor-coupled JFET switching circuit in (a) ON state and (b) OFF state*

The JFET device can be switched ON or OFF by a capacitor coupled input pulse in both the circuits. The design equations for capacitor coupled circuit are similar to that used in direct coupled circuit.

### 1.12.2 MOSFET Switching

Figure 1.48 shows two capacitor-coupled switching circuits using N-channel enhancement MOSFET. When the gate-source voltage of MOSFET is zero, i.e., $V_{GS} = 0$, the device will be in OFF state as seen in Fig. 1.48(a). When the gate-source voltage of MOSFET becomes positive biased, the device will be in ON state as seen in Fig. 1.48(b). Here, the positive bias for $V_{GS}$ is obtained from the voltage divider bias resistors $R_1$ and $R_2$. To turn the device to OFF state, a negative-going input voltage can be applied. The drain current $I_D$ and drain-source voltage $V_{DS(ON)}$ can be obtained from the equations used for direct-coupled JFET switching circuit. The gate-source voltage $V_{GS}$ should be smaller than the minimum threshold voltage of the MOSFET in order to switch the device to OFF state.

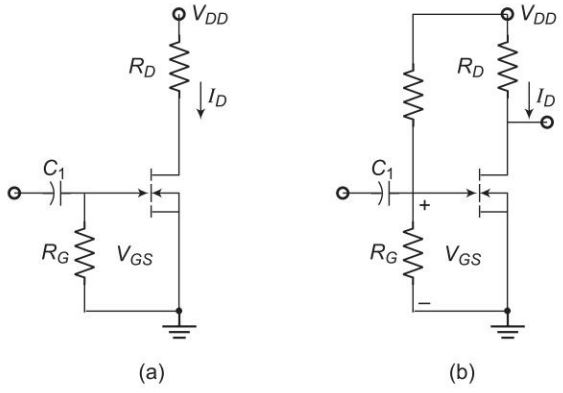



**Fig. 1.48** *Capacitor-coupled E-MOSFET switching circuit in (a) ON state and (b) OFF state*

## REVIEW QUESTIONS

1. What is meant by $Q$-point?
2. What is the need for biasing a transistor?
3. What factors are to be considered for selecting the operating point $Q$ for an amplifier?
4. Distinguish between dc and ac load lines with suitable diagrams.
5. Briefly explain the reasons for keeping the operating point of a transistor fixed.
6. What is thermal runaway? How can it be avoided?
7. What three factors contribute to thermal instability?
8. Define 'stability factor.' Why would it seem more reasonable to call this an instability factor?
9. Draw a fixed-bias circuit and derive an expression for the stability factor.
10. If the coordinates of the operating point of a CE amplifier using fixed bias or base-resistor method of biasing are $V_{CE} = 6$ V and $I_C = 1$ mA, determine the value of $R_C$ and $R_B$. [*Ans.* $R_C = 3$ kΩ, $R_B = 300$ kΩ]
11. Consider a common emitter *NPN* transistor with fixed bias as shown in Fig. 1.6. If $\beta = 80$, $R_B = 390$ kΩ, $R_C = 1.5$ kΩ, and $V_{CC} = 30$ V, find the coordinates of the $Q$-point. [*Ans.* 21 V, 6 mA]
12. A germanium transistor having $\beta = 100$ and $V_{BE} = 0.2$ V is used in a fixed-bias amplifier circuit where $V_{CC} = 16$ V, $R_C = 5$ kΩ and $R_B = 790$ kΩ. Determine its operating point.
13. Derive an expression for the stability factor of a collector-to-base bias circuit.
14. Mention the disadvantages of collector-to-base bias. Can they be overcome?
15. In a germanium transistor CE amplifier biased by feedback resistor method, $V_{CC} = 20$ V, $V_{BE} = 0.2$ V, $\beta = 100$ and the operating point is chosen such that $V_{CE} = 10.4$ V and $I_C = 9.9$ mA. Determine the values of $R_B$ and $R_C$. [*Ans.* 100 kΩ, 1 kΩ]
16. Draw a circuit diagram of CE transistor amplifier using emitter biasing. Describe qualitatively the stability action of the circuit.

**17.** Draw a voltage-divider bias circuit and derive an expression for its stability factor.

**18.** Why does the potential divider method of biasing become universal?

**19.** If the various parameters of a CE amplifier which uses the self-bias method are $V_{CC} = 12$ V, $R_1 = 10$ kΩ, $R_2 = 5$ kΩ, $R_C = 1$ kΩ, $R_E = 2$ kΩ and $\beta = 100$, find (i) the coordinates of the operating point, and (ii) the stability factor, assuming the transistor to be of silicon. [*Ans.* $V_{CE} = 7.05$ V, $I_C = 1.65$ mA, $S = 2.62$]

**20.** In a CE germanium transistor amplifier using self-bias circuit, $R_C = 2.2$ kΩ, $\beta = 50$, $V_{CC} = 9$ V and the operating point is required to be set at $I_C = 2$ mA and $V_{CE} = 3$V. Determine the values of $R_1$, $R_2$ and $R_E$.
[*Ans.* $R_1 = 17.75$ kΩ, $R_2 = 4.75$ kΩ, $R_E = 800$ Ω]

**21.** Determine the operating point for the circuit of a potential-divider bias arrangement with $R_2 = R_C = 5$ kΩ, $R_E = 1$ kΩ and $R_1 = 40$ kΩ. [*Ans.* $V_{CE} = 6$ V, $I_C = 1$ mA]

**22.** Calculate the values of $R_1$ and $R_C$ in the voltage-divider bias circuit so that $Q$-point is at $V_{CE} = 6$ V and $I_C = 2$ mA. Assume the transistor parameters are: $\alpha = 0.985$, $I_{CBO} = 4$ μA and $V_{BE} = 0.2$ V.
[*Ans.* $R_C = 3$ kΩ, $R_1 = 5.54$ kΩ]

**23.** Determine the stability factor for a CB amplifier circuit.

**24.** Draw a circuit which uses a diode to compensate for changes in $I_{CO}$. Explain how stabilization is achieved in the circuit.

**25.** How will you provide temperature compensation for the variations of $V_{BE}$ and stabilization of the operating point?

**26.** What is the principle of providing thermal stabilization by means of different methods of transistor biasing? How does this differ from the compensation techniques using a diode or thermistor or sensistor?

**27.** Explain the circuit operation of direct-coupled switching circuit using BJT when the transistor is switched ON or OFF.

**28.** Draw and explain the circuit of capacitor-coupled transistor switching circuit biased in normally (a) ON state and (b) OFF state.

**29.** A direct-coupled BJT switching circuit has $V_{CC} = 8$Vand $V_i = 5$V. Determine suitable resistances for $R_B$ and $R_C$ to give $I_C = 3$ mA.

**30.** Draw two biasing circuits for a JFET or a depletion type MOSFET.

**31.** Determine the values of resistors $R_D$ and $R_s$ for a self-biased $P$-channel JFET having the following parameters: $V_P = 5$ V, $I_{DSS} = 12$ mA, $V_{DD} = 12$ V, $I_D = 5$ mA and $V_{DS} = 6$ V.
[*Ans.* $R_D = 1.5$ kΩ; $R_s = 525$Ω]

**32.** Determine the value of $R_s$ required to self-bias an $N$-channel JFET with $I_{DSS} = 50$ mA, $V_P = -10$ V and $V_{GSQ} = -5$ V. [*Ans.* $R_S = 400$ Ω]

**33.** In a self-bias $N$-channel JFET circuit, the operating point is to be set at $I_D = 1.5$ mA and $V_{DS} = 10$ V. The JFET parameters are $I_{DSS} = 5$ mA and $V_P = -2$ V. Find the values of $R_s$ and $R_D$. Given that $V_{DD} = 20$ V. [*Ans.* $R_s = 0.6$ kΩ, $R_D = 6$ kΩ.]

**34.** In an $N$-channel JFET biased by potential divider method, it is desired to set the operating point at $I_D = 2.5$ mA and $V_{DS} = 8$ V. If $V_{DD} = 30$ V, $R_1 = 1$ MΩ and $R_2 = 500$ kΩ. Find the value of $R_s$. The parameters of JFET are $I_{DSS} = 10$ mA and $V_P = -5$ V. [*Ans.* $R_s = 5$ kΩ].

**35.** Draw two biasing circuits for an enhancement type MOSFET.

**36.** Explain the circuit operation of direct-coupled switching circuit using N-channel JFET with a neat circuit diagram. Sketch the input and output waveforms.

**37.** Draw and explain the circuit of capacitor-coupled JFET switching circuit biased in normally (a) ON state and (b) OFF state.

**38.** Describe the operation of capacitor-coupled switching circuit using E-MOSFET device biased in normally ON state and OFF state with a neat circuit diagram.

CHAPTER

# 2 BJT Amplifiers

## 2.1 INTRODUCTION

The equivalent circuit for a transistor can be drawn using simple approximations by retaining its essential features, at the same time discarding its less important qualities. These equivalent circuits will aid in analyzing transistor circuits easily and rapidly. In this chapter, small-signal equivalent circuits of the transistor are derived. Small-signal operation is that in which the ac input signal voltages and currents are in the order of ±10% of *Q*-point voltages and currents.

As the *h*-parameter values vary considerably with the individual transistors of the same type and the accuracy of the analysis depends on the operating conditions, an alternate model known as the hybrid-$\pi$ model which employs the emitter-base input resistance ($r_\pi$) and transconductance ($g_m$) is gaining importance now-a-days.

Since the BJT is a three terminal device, the small signal analysis can be performed for three basic transistor configurations, depending on which one of the three transistor terminals is used as signal ground. These three basic configurations are common emitter, common collector and common base.

## 2.2 SMALL SIGNAL ANALYSIS OF CE AMPLIFIER USING HYBRID-$\pi$ EQUIVALENT CIRCUIT

### 2.2.1 CE Amplifier with Voltage Divider Bias

Consider a common emitter amplifier employing voltage divider bias or self bias as shown in Fig. 2.1. The analysis of CE amplifier with bypassed emitter resistor $R_E$ can be obtained using the hybrid-$\pi$ equivalent circuit.

Here, the analysis is done in the midband region and therefore, all the physical capacitors ($C_1$, $C_2$ and $C_E$) shown in Fig. 2.1 will be short circuited in the equivalent circuit. For ac analysis, the dc source $V_{CC}$ is also short circuited. Now, the equivalent circuit for the CE amplifier is drawn by using hybrid-$\pi$ model. The hybrid-$\pi$ model can be drawn either by using transconductance parameter or current gain parameter.

The hybrid-$\pi$ model, in general, consists of

(i) Base spreading resistance $r_{bb'}$

(ii) Equivalent resistance between base and emitter denoted as $r_\pi$

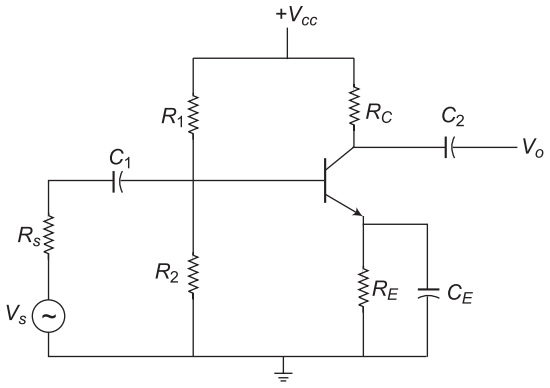



**Fig. 2.1** *CE amplifier with bypassed $R_E$*

(iii) A current source $g_m V_\pi$ where $V_\pi$ denotes the drop across diffusion resistance $r_\pi$ or a current source $\beta I_b$ to represent collector current

(iv) ac collector resistance $r_o$, connected between collector and emitter

Figure 2.2 shows the equivalent circuit of hybrid-$\pi$ model with transconductance parameter $g_m$ for CE amplifier configuration. The small signal analysis of CE amplifier is done based on the assumption that the base spreading resistance $r_{bb'}$ is short circuited.

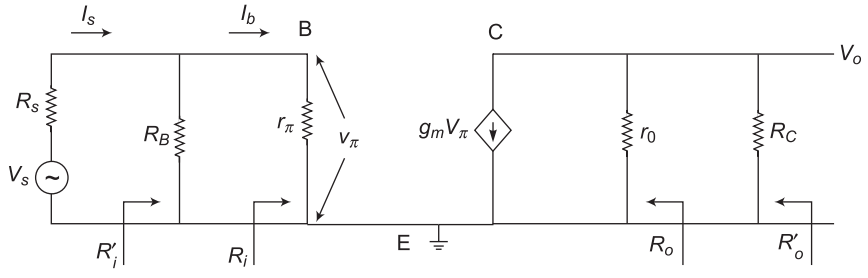



**Fig. 2.2** *Small signal hybrid-$\pi$ equivalent circuit for CE amplifier*

***Input Resistance*** The input resistance $R_i$ to the amplifier is

$$R_i = r_\pi$$

where $r_\pi = \dfrac{V_T}{I_{BQ}} = \dfrac{\beta V_T}{I_{CQ}}$ is called the base emitter resistance or diffusion resistance. By considering the bias resistors, the input resistance $R_i'$ for CE amplifier becomes

$$R_i' = R_B \| r_\pi$$

where $R_B = R_1 \| R_2$.

***Voltage Gain*** The voltage gain ($A_V$) is the ratio of output voltage ($V_o$) to input voltage ($V_i$) as given by

$$A_V = \frac{V_o}{V_i}$$

From Fig. 2.2, it is seen that the small signal output voltage is

$$V_o = -g_m V_\pi (r_o \| R_C)$$

where $g_m = \dfrac{I_{CQ}}{V_T}$ is the transconductance, $r_o = \dfrac{V_A}{I_{CQ}}$ is the small signal transistor internal output resistance and $V_A$ is the Early voltage.

Though the collector current flows through the parallel combination of $r_o$ and $R_C$, it is in a direction to produce a negative output voltage. Since $V_i = V_\pi$, the voltage gain can be expressed as

$$A_V = \frac{V_o}{V_\pi} = -g_m (r_o \| R_C)$$

By voltage divider rule, we know that

$$V_\pi = \left( \frac{R_i'}{R_S + R_i'} \right) \cdot V_s$$

where $R_i' = R_1 \| R_2 \| r_\pi$.

Considering the source voltage $V_s$, the overall voltage gain $A_{VS}$ can be determined as

$$A_{Vs} = \frac{V_o}{V_s} = -g_m (r_o \| R_C) \left( \frac{R_i'}{R_S + R_i'} \right)$$

$$= A_V \frac{R_i'}{R_S + R_i'}$$

***Current Gain*** The current gain ($A_I$) is the ratio of output current ($I_o$) to input base current ($I_b$) as given by

$$A_I = \frac{I_o}{I_b}$$

Since the collector-emitter resistance $r_o$ is high, the output current $I_o \approx -g_m V_\pi$.

Therefore, the current gain is

$$A_I = \frac{-g_m V_\pi}{V_\pi / r_\pi} = -g_m r_\pi = -\beta \qquad \text{(since } I_b = V_\pi / r_\pi\text{)}$$

By current divider rule, we have

$$I_b = \frac{R_B}{R_B + R_i} I_s$$

The overall current gain $A_{IS}$ is given by

$$A_{Is} = \frac{I_o}{I_s} = \frac{I_o}{I_b} \left( \frac{R_B}{R_B + R_i} \right) = -g_m r_\pi \left( \frac{R_B}{R_B + R_i} \right) = A_I \left( \frac{R_B}{R_B + R_i} \right)$$

***Output Resistance*** The output resistance, by looking into the output terminals without the load resistance ($R_C$) is

$$R_o = r_o$$

With load resistance, the output resistance is $R_o' = r_o \parallel R_C$.

## EXAMPLE 2.1

Determine the small signal voltage gain, current gain, input resistance and output resistance for the CE amplifier shown in Fig. 2.1 with $R_S = 500\ \Omega$, $R_1 = 250\ \text{k}\Omega$, $R_2 = 75\ \text{k}\Omega$, $R_E = 600\ \Omega$ and $R_C = 5.6\ \text{k}\Omega$. Assume that the transistor parameters, $I_{CQ} = 1\ \text{mA}$, $\beta = 120$ and Early voltage $V_A = 100$.

**Solution** Given that, for CE amplifier, $R_S$ = 500 Ω, $R_1$ = 250 kΩ, $R_2$ = 75 kΩ, $R_E$ = 600 Ω and $R_C = 5.6\ \text{k}\Omega$. The small signal hybrid-$\pi$ parameters in the equivalent circuit of CE amplifier are given by

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{120 \times 26 \times 10^{-3}}{1 \times 10^{-3}} = 3.12\ \text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1 \times 10^{-3}}{26 \times 10^{-3}} = 38.4\ \text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{100}{1 \times 10^{-3}} = 100\ \text{k}\Omega$$

*Input Resistance*

$$R_i' = R_1 \parallel R_2 \parallel r_\pi = (250 \times 10^3) \parallel (75 \times 10^3) \parallel (3.12 \times 10^3) = 2.96\ \text{k}\Omega$$

*Small signal voltage gain*

$$A_{Vs} = \frac{V_o}{V_s} = -g_m (r_o \parallel R_C) \left( \frac{R_i'}{R_S + R_i'} \right)$$

$$= -38.4 \times 10^{-3} \times \left[ (100 \times 10^3) \parallel (5.6 \times 10^3) \right] \left( \frac{2.96}{0.5 + 2.96} \right) = -174$$

*Small signal current gain*

$$A_{Vs} = -g_m r_\pi \left( \frac{R_B}{R_B + R_i} \right) \qquad \text{where } R_B = R_1 \parallel R_2 \text{ and } R_i = r_\pi$$

$$= -38.4 \times 10^{-3} \times 3.12 \times 10^3 \left( \frac{57.69 \times 10^3}{(57.69 \times 10^3) + (3.12 \times 10^3)} \right) = -113.7$$

*Output resistance*

$$R_o' = r_o \parallel R_C = (100 \times 10^3) \parallel (5.6 \times 10^3) = 5.3\ \text{k}\Omega$$

### 2.2.2 CE Amplifier with Unbypassed $R_E$

Figure 2.3 shows the CE amplifier with unbypassed $R_E$, i.e., without emitter capacitor $C_E$.

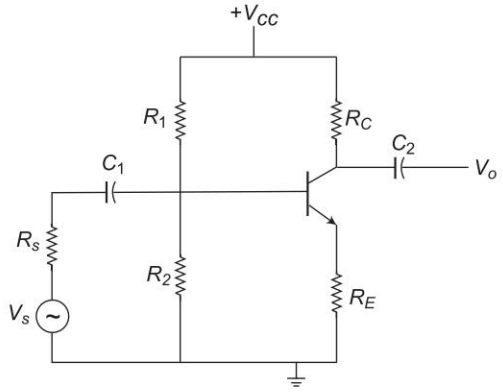



**Fig. 2.3** *CE amplifier with unbypassed $R_E$*

The analysis of this amplifier is obtained by drawing the hybrid-$\pi$ model equivalent circuit with the current gain parameter $\beta$ as shown in Fig. 2.4.

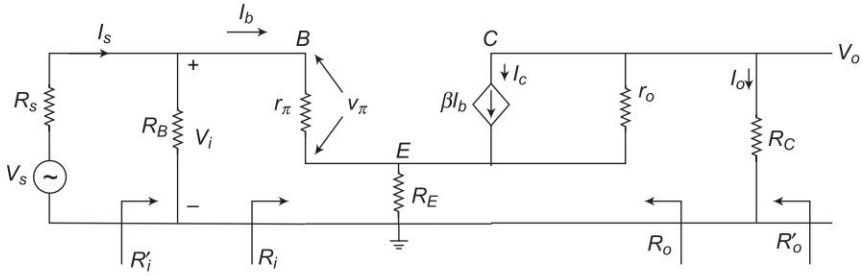



**Fig. 2.4** *Small signal hybrid-$\pi$ equivalent circuit for CE amplifier with unbypassed $R_E$*

***Current Gain*** The current gain is defined as

$$A_I = \frac{I_o}{I_b} = \frac{-I_c}{I_b} = \frac{-\beta I_b}{I_b} = -\beta$$

Here, the current gain equals the short circuit value and is unaffected by the addition of emitter resistor $R_E$.

***Input Resistance*** From loop equation, we have

$$V_i = I_b r_\pi + (I_b + \beta I_b) R_E$$

The input resistance is

$$R_i = \frac{V_i}{I_b} = r_\pi + (1+\beta) R_E$$

From the above equation, it is seen that the input resistance depends on the unbypassed emitter resistor $R_E$. Considering the bias resistors, the overall input resistance $R_i'$ becomes

$$R_i' = R_B \parallel R_i = R_1 \parallel R_2 \parallel R_i$$

***Voltage Gain*** By voltage divider rule, we have

$$V_i = \left(\frac{R_i'}{R_S + R_i'}\right) \cdot V_s$$

The small signal voltage gain is

$$A_V = \frac{V_o}{V_i} = \frac{I_o R_C}{I_b r_\pi + (I_b + \beta I_b) R_E}$$

$$= \frac{-(\beta I_b) R_C}{I_b r_\pi + (I_b + \beta I_b) R_E} = \frac{-\beta R_C}{r_\pi + (1+\beta) R_E} = \frac{-\beta R_C}{R_i}$$

The overall small signal voltage gain is

$$A_{Vs} = \frac{V_o}{V_s} = \frac{-(\beta I_b) R_C}{V_s} = \frac{-(\beta I_b) R_C}{V_i}\left(\frac{R_i'}{R_S + R_i'}\right)$$

$$= \frac{-\beta R_C}{r_\pi + (1+\beta) R_E}\left(\frac{R_i'}{R_S + R_i'}\right) \qquad \text{(since } V_i = [r_\pi + (1+\beta) R_E] I_b\text{)}$$

If $R_i' > R_S$ and if $(1 + \beta)R_E >> r_\pi$, then the above voltage gain is given by

$$A_{Vs} \cong \frac{-\beta R_C}{(1+\beta) R_E} \cong \frac{-R_C}{R_E} \qquad \text{(since } \beta >> 1\text{)}$$

The above approximate expression shows that the amplifier voltage gain is independent of the current gain $\beta$ and it is dependent on the emitter resistance $R_E$ and load resistance $R_C$.

***Output Resistance*** The output resistance is defined as the resistance of an amplifier without considering the source and load, i.e., $V_s = 0$ and $R_C = \infty$. Assuming $r_o = \infty$, the output resistance is

$$R_o = \left.\frac{V_o}{I_o}\right|_{V_S = 0} = \infty$$

Since $V_S = 0$, the current through the input loop $I_b$ will be zero. Hence, the output current $I_o$ will also be zero. Taking the load resistance $R_C$ into account, the overall output resistance is given by

$$R_o' = R_o \parallel R_C = \infty \parallel R_C \approx R_C$$

## EXAMPLE 2.2

Calculate the small signal voltage gain and input resistance for the CE amplifier with unbypassed $R_E$ shown in Fig. 2.3 with $R_S$ = 1 kΩ, $R_1$ = 75 kΩ, $R_2$ = 15 kΩ, $R_E$ = 400 Ω and $R_C$ = 3kΩ. Assume that the transistor parameters, $I_{CQ}$ = 2 mA, $\beta$ = 100 and Early voltage, $V_A = \infty$.

**Solution** Given that, for *CE* amplifier, $R_S$ = 1 kΩ, $R_1$ = 75 kΩ, $R_2$ = 15 kΩ, $R_E$ = 400 Ω and $R_C$ = 3kΩ. The small signal hybrid-$\pi$ parameters in the equivalent circuit of CE amplifier are given by

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 26 \times 10^{-3}}{2 \times 10^{-3}} = 1.3\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{2\times10^{-3}}{26\times10^{-3}} = 76.92\,\text{mA/V}$$

and $$r_o = \frac{V_A}{I_{CQ}} = \infty$$

*Input resistance*

$$R_i' = R_1 \| R_2 \| r_\pi + (1+\beta)R_E]$$

$$= (75\times10^3)\|(15\times10^3)\|\left[(1.3\times10^3)+(1+100)\times400\right] = 9.62\,\text{k}\Omega$$

*Small signal voltage gain*

$$A_V = \frac{-\beta R_C}{R_i} = \frac{-\beta R_C}{r_\pi + (1+\beta)R_E}$$

$$= \frac{-100\times3\times10^3}{41.7\times10^3} = -7.19$$

Using the exact expression for the small signal overall voltage gain, we obtain

$$A_{Vs} = \frac{-\beta R_C}{r_\pi + (1+\beta)R_E}\left(\frac{R_i'}{R_S + R_i'}\right)$$

$$= \frac{-100\times3}{1.3+(101)(0.4)}\times\left(\frac{9.62}{1+9.62}\right) = -6.55$$

If the approximate expression for the voltage gain is used, we get

$$A_{Vs} = \frac{-R_C}{R_E} = \frac{-3\times10^3}{400} = -7.5$$

## 2.3 SMALL SIGNAL ANALYSIS OF CB AMPLIFIER USING HYBRID-π EQUIVALENT CIRCUIT

Figure 2.5 shows the CB amplifier in which the base is at signal ground. Here, the input signal is applied to the emitter and the output signal is obtained at the collector.

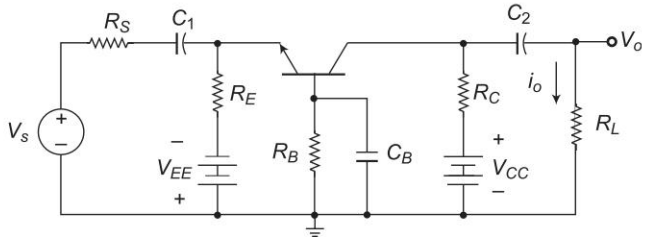



**Fig. 2.5** *CB amplifier*

Figure 2.6 shows the hybrid-$\pi$ model equivalent circuit for CB amplifier in which the output resistance $r_0$ is assumed to be infinite.

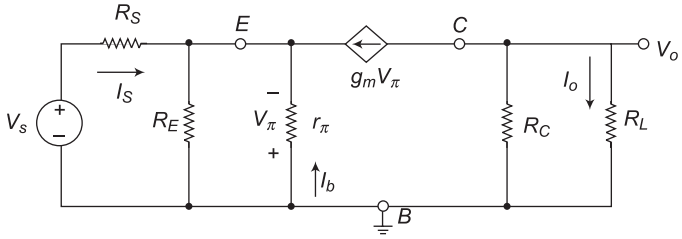



**Fig. 2.6** *Small signal hybrid-π equivalent circuit for CB amplifier*

***Voltage Gain*** The small signal output voltage is

$$V_o = -(g_m V_\pi)(R_C \parallel R_L)$$

Using KCL equation at the emitter node along with the source resistance $R_S$, we have

$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_S - (-V_\pi)}{R_S} = 0$$

Since $\beta = g_m r_\pi$, the above equation can be written as

$$V_\pi \left( \frac{1+\beta}{r_\pi} + \frac{1}{R_E} + \frac{1}{R_S} \right) = \frac{-V_S}{R_S}$$

Hence,

$$V_\pi = \frac{-V_s}{R_S} \left[ \left( \frac{r_\pi}{1+\beta} \right) \parallel R_E \parallel R_S \right]$$

Now, the small signal overall voltage gain is given by

$$A_{Vs} = \frac{V_o}{V_s} = \frac{-(g_m V_\pi)(R_C \parallel R_L)}{V_s} = g_m \frac{(R_C \parallel R_L)}{R_S} \left[ \left( \frac{r_\pi}{1+\beta} \right) \parallel R_E \parallel R_S \right]$$

When the source resistance $R_s$ approaches zero, the voltage gain becomes

$$A_{Vs} = g_m (R_C \parallel R_L)$$

***Current Gain*** The small signal current gain is defined as

$$A_{Is} = \frac{I_o}{I_s}$$

Again using KCL equation at the emitter node, we have

$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + I_S = 0$$

Solving for $V_\pi$, we get

$$V_\pi = -I_s \left[ \left( \frac{r_\pi}{1+\beta} \right) \parallel R_E \right]$$

From Fig. 2.6, the output load current is given by

$$I_o = -g_m V_\pi \left( \frac{R_C}{R_C + R_L} \right)$$

Hence, the small signal current gain is

$$A_{IS} = \frac{I_o}{I_s} = \frac{-g_m V_\pi \left( \frac{R_C}{R_C + R_L} \right)}{I_s} = g_m \left[ \left( \frac{r_\pi}{1+\beta} \right) \| R_E \right] \left( \frac{R_C}{R_C + R_L} \right)$$

If the emitter resistor $R_E$ approaches infinity and load resistor $R_L$ reaches zero, then the small signal current gain becomes the short circuit current gain $A_{I_o}$, is given by

$$A_{I_o} = \frac{g_m r_\pi}{1+\beta} = \frac{\beta}{1+\beta} = \alpha \qquad (\text{since } \beta = g_m r_\pi)$$

where $\alpha$ is the current gain of the CB transistor. In general, the small signal voltage gain is usually greater than 1 and the current gain is slightly less than 1 for common base circuit.

***Input Resistance*** The input resistance, by looking into the input emitter terminal, is given by

$$R_i = \frac{V_\pi}{I_s}$$

Writing KCL equation at the input, we have

$$I_s = I_b + g_m V_\pi = \frac{V_\pi}{r_\pi} + g_m V_\pi = V_\pi \left( \frac{1+\beta}{r_\pi} \right)$$

Hence,

$$R_i = \frac{V_\pi}{I_s} = \frac{r_\pi}{1+\beta}$$

***Output Resistance*** The output resistance is determined by short circuiting the source voltage i.e., $V_s = 0$ as shown in Fig. 2.7.

Using the KCL equation at the emitter node in Fig. 2.7, we obtain

$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_\pi}{R_S} = 0$$

This implies that $V_\pi = 0$ which means that the independent source $g_m V_\pi$ is also zero. Therefore, the output resistance, by looking into the output collector terminal, is given by

$$R_o = R_C$$

Since $r_o$ is assumed to be infinite, the output resistance looking into the collector terminal is also infinite. This shows that the common base circuit looks similar to an ideal current source.

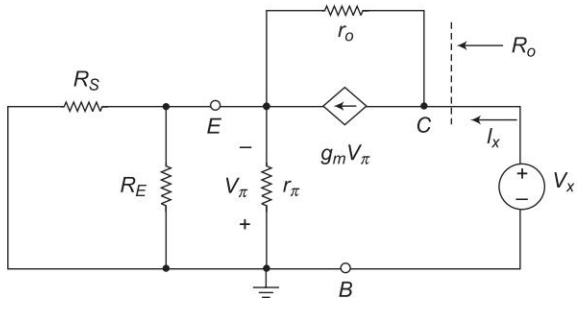



**Fig. 2.7** *CB equivalent circuit for calculating output resistance*

## EXAMPLE 2.3

For the CB amplifier circuit shown in Fig. 2.5, $R_S = 500\,\Omega$, $R_E = 10\,\text{k}\Omega$, $R_C = 5\,\text{k}\Omega$ and $R_L = 1\,\text{k}\Omega$. Assume the transistor parameters are $I_{CQ} = 0.921\,\text{mA}$, $\beta = 100$ and Early voltage $V_A = \infty$. Determine the small signal voltage gain, current gain, input resistance and output resistance.

**Solution** Given that, for CB amplifier, $R_S = 500\,\Omega$, $R_E = 10\,\text{k}\Omega$, $R_C = 5\,\text{k}\Omega$ and $R_L = 1\,\text{k}\Omega$. The small signal hybrid-$\pi$ parameters in the equivalent circuit of CB amplifier are given by

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 26 \times 10^{-3}}{0.921 \times 10^{-3}} = 2.82\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.921 \times 10^{-3}}{26 \times 10^{-3}} = 35.42\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \infty$$

*Small signal voltage gain*

$$A_{Vs} = g_m \frac{(R_C \parallel R_L)}{R_S}\left[\left(\frac{r_\pi}{1+\beta}\right) \parallel R_E \parallel R_S\right]$$

$$= 35.42 \times 10^{-3} \times \frac{\left[(5\times10^3) \parallel (1\times10^3)\right]}{0.5\times10^3} \times \left[\left(\frac{2.82\times10^3}{101}\right) \parallel 10\times10^3 \parallel 0.5\times10^3\right]$$

$$= 1.65$$

*Small signal current gain*

$$A_{Is} = g_m\left[\left(\frac{r_\pi}{1+\beta}\right) \parallel R_E\right]\left(\frac{R_C}{R_C + R_L}\right)$$

$$= 35.42 \times 10^{-3} \times \left[\left(\frac{2.82\times10^3}{101}\right) \parallel \left(10\times10^3\right)\right] \times \left(\frac{5\times10^3}{(5\times10^3)+(1\times10^3)}\right) = 0.796$$

*Input resistance*

$$R_i = \frac{r_\pi}{1+\beta} = \frac{2.82\times10^3}{101} = 27.92\,\Omega$$

*Output resistance*

$$R_o = R_C = 5\,\text{k}\Omega$$

## 2.4 SMALL SIGNAL ANALYSIS OF CC AMPLIFIER USING HYBRID-$\pi$ EQUIVALENT CIRCUIT

### 2.4.1 Common Collector Amplifier (Emitter follower)

Consider a common collector amplifier as shown in Fig. 2.8(a). The simplified ac equivalent circuit of CC amplifier is shown in Fig. 2.8(b). Here, the input signal is applied to the base, the output signal is taken at the

emitter, and the collector is connected directly to $V_{CC}$. This circuit is called common collector circuit since the collector supply $V_{CC}$ is at signal ground in the ac equivalent circuit shown in Fig. 2.8(b).

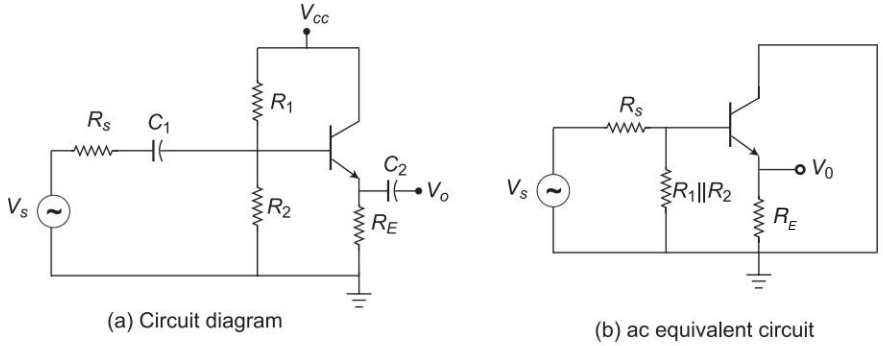



**Fig. 2.8** *CC amplifier*

The analysis of CC amplifier can be done using the hybrid-$\pi$ equivalent circuit with current gain parameter $\beta$ shown in Fig. 2.9.

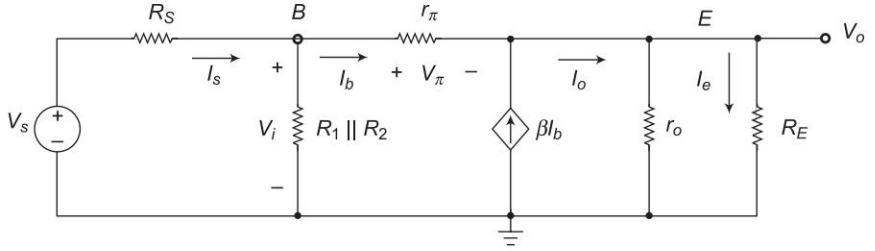



**Fig. 2.9** *Small signal hybrid-π equivalent circuit for CC amplifier*

***Input Resistance*** From Fig. 2.9, it is seen that the output current is

$$I_o = I_b + \beta I_b = (1+\beta) I_b$$

and the output voltage is

$$V_o = (r_o \parallel R_E) I_o = (r_o \parallel R_E)(1+\beta) I_b$$

Applying KVL to the emitter-base loop, we get

$$V_i = V_\pi + V_o = r_\pi I_b + (r_o \parallel R_E)(1+\beta) I_b$$

$$= I_b \left[ r_\pi + (r_o \parallel R_E)(1+\beta) \right]$$

Hence, the input resistance is given by

$$R_i = \frac{V_i}{I_b} = r_\pi + \left(r_o \parallel R_E\right)\left(1+\beta\right)$$

The overall input resistance can be written as

$$R_i = R_1 \parallel R_2 \parallel R_i$$

***Voltage Gain*** Using voltage divider rule in Fig. 2.9, we have

$$V_i = \frac{R_i'}{R_i' + R_S} V_s$$

Now, the overall small signal voltage gain is given by

$$A_{Vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = \frac{(r_o \parallel R_E)(1+\beta)}{\left[r_\pi + (r_o \parallel R_E)(1+\beta)\right]} \times \left(\frac{R_i'}{R_i' + R_S}\right)$$

If $r_\pi << (r_o \parallel R_E)(1+\beta)$ and $R_i >> R_s$, then the voltage gain of CC amplifier will be approximately equal to one i.e., $A_v \approx 1$. Hence, CC amplifier is also called *unit gain amplifier*.

***Current Gain*** From Fig. 2.9, it is seen that the emitter current is

$$I_e = \frac{r_o}{r_o + R_E} I_o$$

and $$I_o = (1+\beta) I_b$$

Using current divider rule, we get

$$I_b = \left(\frac{R_1 \parallel R_2}{(R_1 \parallel R_2) + R_i}\right) \cdot I_i$$

The small signal current gain is given by

$$A_i = \frac{I_e}{I_i} = \frac{I_e}{I_o} \times \frac{I_o}{I_b} \times \frac{I_b}{I_i} = \frac{r_o}{r_o + R_E} \cdot (1+\beta) \cdot \left(\frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_i}\right)$$

If $r_0 >> R_E$ and $R_1 \parallel R_2 >> R_i$, then the current gain is

$$A_i \approx (1+\beta)$$

From the above equation, it is seen that the small signal current gain is greater than 1 whereas the small signal voltage gain is slightly less than 1.

***Output Resistance*** The output resistance is determined by short circuiting the source voltage i.e., $V_s = 0$ as shown in Fig. 2.10. Here, a test voltage $V_x$ is applied to the output terminals and the resultant test current is $I_x$.

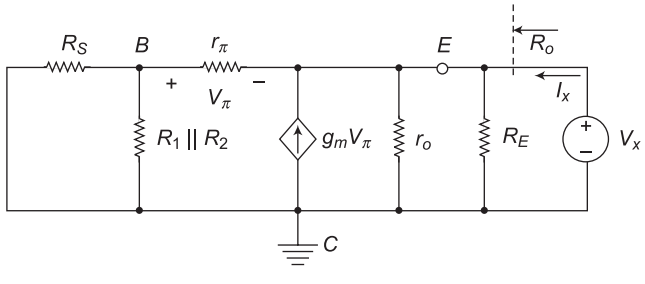



**Fig. 2.10** *CC equivalent circuit for calculating output resistance*

The output resistance is given by

$$R_o = \frac{V_x}{I_x}$$

From voltage divider rule, we have

$$V_\pi = \left( \frac{r_\pi}{r_\pi + R_1 \parallel R_2 \parallel R_S} \right) V_x$$

Using KCL equation at the emitter node in Fig. 9.24, we get

$$I_x + g_m V_\pi = \frac{V_x}{r_\pi + R_1 \parallel R_2 \parallel R_S} + \frac{V_x}{r_o} + \frac{V_x}{R_E}$$

Therefore,

$$I_x = -g_m V_\pi + \frac{V_x}{r_\pi + R_1 \parallel R_2 \parallel R_S} + \frac{V_x}{r_o} + \frac{V_x}{R_E}$$

$$= \left( \frac{g_m r_\pi}{r_\pi + R_1 \parallel R_2 \parallel R_S} \right) V_x + \frac{V_x}{r_\pi + R_1 \parallel R_2 \parallel R_S} + \frac{V_x}{r_o} + \frac{V_x}{R_E}$$

Since $g_m r_\pi = \beta$, we have

$$\frac{I_x}{V_x} = \left( \frac{1+\beta}{r_\pi + R_1 \parallel R_2 \parallel R_S} \right) + \frac{1}{r_o} + \frac{1}{R_E}$$

Hence, the output resistance is

$$R_o = \frac{V_x}{I_x} = \left( \frac{r_\pi + R_1 \parallel R_2 \parallel R_S}{1+\beta} \right) \parallel r_o \parallel R_E$$

In general, the CC amplifier has high input resistance and low output resistance. It is referred to as impedance transformer since the input impedance is large and the output impedance is small.

## EXAMPLE 2.4

For the circuit shown in Fig. 2.8(a), $R_S = 500\,\Omega, R_1 = 25\,\text{k}\Omega, R_2 = 50\,\text{k}\Omega$ and $R_E = 1\,\text{k}\Omega$. Assume the transistor parameters are $I_{CQ} = 0.7\,\text{mA}$, $\beta = 120$ and Early voltage $V_A = 100$. Determine the small signal voltage gain, current gain, input resistance and output resistance.

**Solution** Given that, for CC amplifier, $R_S = 500\,\Omega$, $R_1 = 25\,\text{k}\Omega, R_2 = 50\,\text{k}\Omega$ and $R_E = 1\,\text{k}\Omega$. The small signal hybrid-$\pi$ parameters in the equivalent circuit of CC amplifier are given by

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{120 \times 26 \times 10^{-3}}{0.7 \times 10^{-3}} = 4.46\,\text{k}\grave{\text{U}}$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.7 \times 10^{-3}}{26 \times 10^{-3}} = 26.92\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{100}{0.7 \times 10^{-3}} = 142.86\,\text{k}\Omega$$

*Input resistance*

$$R_i = R_1 \parallel R_2 \parallel R_i = R_1 \parallel R_2 \parallel \left[ r_\pi + (r_o \parallel R_E)(1+\beta) \right]$$

$$= (25\times10^3) \parallel (50\times10^3) \parallel \left[ (4.46\times10^3) + (142.86\times10^3 \parallel 1\times10^3)\times 121 \right]$$

$$= (16.67\times10^3) \parallel (124.61\times10^3) = 14.7\,\text{k}\Omega$$

*Small signal voltage gain*

$$A_{Vs} = \frac{(r_o \parallel R_E)(1+\beta)}{\left[ r_\pi + (r_o \parallel R_E)(1+\beta) \right]} \times \left( \frac{R_i'}{R_i' + R_S} \right)$$

$$= \frac{\left[ (142.86\times10^3) \parallel (1\times10^3) \right]\times 121}{\left[ 4.46\times10^3 + [(142.86\times10^3) \parallel (1\times10^3)]\times 121 \right]} \times \left( \frac{14.7}{14.7+0.5} \right) = 0.932$$

*Small signal current gain*

$$A_i = \frac{r_o}{r_o + R_E} \times (1+\beta) \times \left( \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_i} \right)$$

$$= \frac{142.86}{142.86+1} \times 120 \times \left( \frac{\left[ (25\times10^3) \parallel (50\times10^3) \right]}{\left[ (25\times10^3) \parallel (50\times10^3) \right] + (124.61\times10^3)} \right)$$

$$= 119.16 \times \left( \frac{16.67\times10^3}{(16.67\times10^3) + (124.61\times10^3)} \right) = 14.06$$

*Output resistance*

$$R_o = \left( \frac{r_\pi + R_1 \parallel R_2 \parallel R_S}{1+\beta} \right) \parallel r_o \parallel R_E$$

$$= \left( \frac{(4.46\times10^3) + \left[ (25\times10^3) \parallel (50\times10^3) \parallel (0.5\times10^3) \right]}{121} \right) \parallel (142.86\times10^3) \parallel (1\times10^3)$$

$$= \left( \frac{(4.46\times10^3) + (0.49\times10^3)}{121} \right) \parallel (0.993\times10^3) = 39.37\,\Omega$$

## 2.5 CASCADE AMPLIFIER CONFIGURATION

The most popular cascade amplifier is formed by cascading several CE amplifier stages. Before considering the analysis of any specific type of multistage amplifiers, the analysis of a general '*n*' stage CE amplifier shown in Fig. 2.11 is done in this section.

Biasing arrangements and coupling elements are omitted for simplicity. The expressions for quantities such as voltage gain, current gain, power gain, input impedance, and output impedance of this '*n*' stage CE amplifier are to be derived.

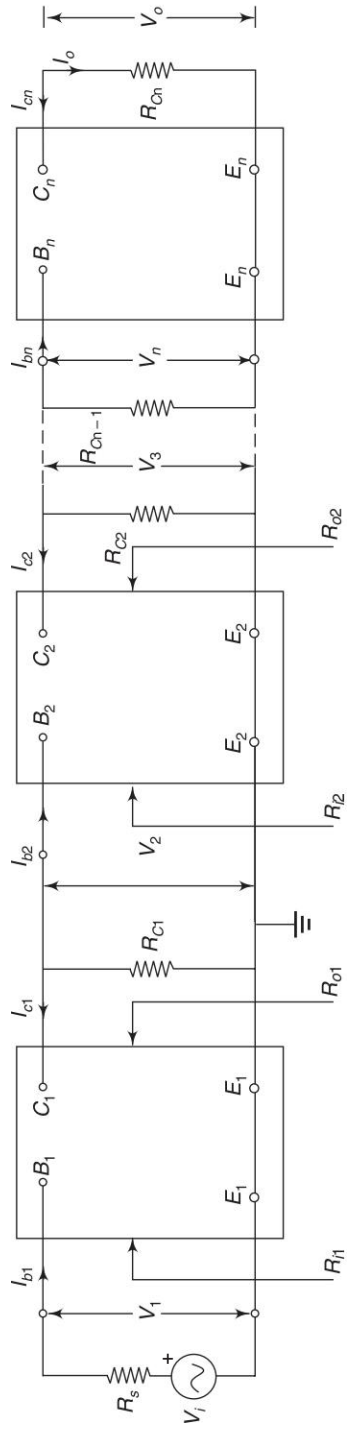



**Fig. 2.11** *'n' stage CE amplifier*

***Voltage Gain*** In a multistage amplifier, the output voltage of the first stage acts as the input voltage of second stage and so on. The voltage gain of the complete cascade amplifier is equal to the product of the voltage gains of the individual stages.

**Proof** The voltage gain of the first stage

$$\begin{aligned}\overline{A}_{V1} &= \frac{\overline{V}_2}{\overline{V}_1} = \frac{\text{Output voltage of the first stage}}{\text{Input voltage of the first stage}} \\ &= A_{V1} \angle \theta_1\end{aligned}$$

where $A_{V1}$ is the magnitude of voltage gain and $\theta_1$ is phase angle of the output voltage relative to input voltage. Similarly,

$$\begin{aligned}\overline{A}_{V2} &= \frac{\overline{V}_3}{\overline{V}_2} = \frac{\text{Output voltage of the second stage}}{\text{Input voltage of the second stage}} \\ &= A_{V2} \angle \theta_2\end{aligned}$$

Similar expressions can be written for all the '$n$' stages of the cascade amplifier. The resultant voltage gain,

$$\begin{aligned}\overline{A}_V &= \frac{\overline{V}_0}{\overline{V}_1} = \frac{\text{Output voltage of the } n^{\text{th}} \text{ stage}}{\text{Input voltage of the first stage}} \\ &= A_V \angle \theta\end{aligned}$$

But

$$\frac{\overline{V}_0}{\overline{V}_1} = \frac{\overline{V}_2}{\overline{V}_1} \times \frac{\overline{V}_3}{\overline{V}_2} \times \frac{\overline{V}_4}{\overline{V}_3} \cdots \frac{\overline{V}_n}{\overline{V}_{(n-1)}} \times \frac{\overline{V}_0}{\overline{V}_n}$$

Hence, it follows that

$$\begin{aligned}\overline{A}_V &= \overline{A}_{V1} \cdot \overline{A}_{V2} \cdot \overline{A}_{V3} \cdots \overline{A}_{Vn} \qquad (2.1) \\ &= A_{V1} \cdot A_{V2} \cdot A_{V3} \ldots A_{Vn} \ldots \angle\theta_1 + \angle\theta_2 + \angle\theta_3 + \cdots + \angle\theta_n \\ &= A_V \angle \theta\end{aligned}$$

Hence,

$$A_V = A_{V1} . A_{V2} . A_{V3} \ldots A_{Vn} \qquad (2.2)$$

and

$$\theta = \theta_1 + \theta_2 + \theta_3 + \cdots + \theta_n \qquad (2.3)$$

From Eqs. (2.2) and (2.3), one can conclude that (i) the magnitude of the resultant voltage gain equals the product of the magnitudes of the voltage gains of the individual stages, and (ii) the phase shift of the resultant voltage gain equals the sum of the phase shifts of the individual stages comprising the multistage cascade amplifier.

Figure 2.12 shows a particular stage, say, the $K^{\text{th}}$ stage, of the $n$-stage cascaded amplifier. From Eq. (2.3), the voltage gain of the $K^{\text{th}}$ stage is given by

$$\overline{A}_{VK} = \frac{\overline{A}_{IK}\, R_{LK}}{R_{iK}} \qquad (2.4)$$

where $R_{LK}$ is the effective load impedance at the collector of the $K^{\text{th}}$ stage and $R_{iK}$ is the input impedance of the $K^{\text{th}}$ stage.

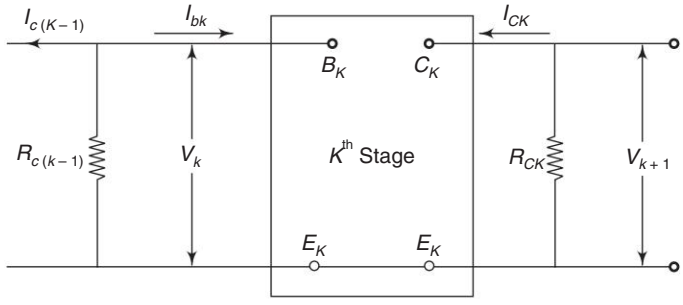



**Fig. 2.12** *$K^{th}$ stage of a cascaded amplifier*

The terms $\bar{A}_{IK}$, $R_{LK}$ and $R_{iK}$ may be evaluated by starting from the last stage and proceeding backward to the first stage.

From Eq. (2.5), the current gain

$$A_{In} = \frac{-h_{fe}}{1 + h_{oe}\, R_{Ln}}$$

and from Eq. (2.6),

$$R_{in} = h_{ie} + h_{re} A_{In} R_{Ln}$$

where $R_{Ln}$ is the effective load impedance for the last stage and equals $R_{Cn}$.

The effective load impedance $R_{L\,(n-1)}$ of the $(n-1)^{th}$ stage is equal to

$$R_{C\,(n-1)} \parallel R_{i(n)}$$

Thus,

$$R_{L(n-1)} = \frac{R_{C(n-1)} \times R_{i(n)}}{R_{C(n-1)} + R_{i(n)}} \tag{2.7}$$

Having known $R_{L(n-1)}$, $A_{I(n-1)}$ can be found out from

$$A_{I(n-1)} = \frac{-h_{fe}}{1 + h_{oe}\, R_{L(n-1)}} \tag{2.8}$$

and $R_{i(n-1)}$ can be found from

$$R_{i\,(n-1)} = h_{ie} + h_{re}\, A_{I(n-1)}\, R_{L(n-1)} \tag{2.9}$$

By proceeding in this manner, one can calculate the current gain and input impedance of each stage including the first. The voltage gain of each stage can be obtained from Eq. (2.4) for that stage.

***Current Gain*** In order to find the resultant voltage gain, the voltage gain of the individual stages can be found out and the product of these gains gives the resultant voltage gain. Alternatively, the resultant voltage gain can be found directly by the relation

$$\bar{A}_V = \frac{\bar{A}_I R_{Cn}}{R_{i1}}$$

where $\overline{A}_I$ is the current gain of the complete $n$-stage amplifier.

Now, $\overline{A}_I$ is given by

$$\overline{A}_I = \frac{\overline{I}_o}{\overline{I}_{b1}} = \frac{-\overline{I}_{Cn}}{\overline{I}_{b1}}$$

Now,
$$\frac{-\overline{I}_{Cn}}{\overline{I}_{b1}} = \frac{-\overline{I}_{c1}}{\overline{I}_{b1}} \cdot \frac{\overline{I}_{c2}}{\overline{I}_{c1}} \cdots \frac{\overline{I}_{Cn}}{\overline{I}_{C(n-1)}}$$

or

$$\overline{A}_I = \overline{A}_{I1} \cdot \overline{A}'_{I2} \cdot \overline{A}'_{I3} \cdots \overline{A}'_{In} \tag{2.10}$$

Here, $\overline{A}_{I1}$ is the base to collector gain of the first stage and equals $\frac{-\overline{I}_{c1}}{\overline{I}_{b1}}$, while $\overline{A}'_{I2}$, $\overline{A}'_{I3}$ are the collector-to-collector current gains of the second and third stages.

For the $K^{\text{th}}$ stage, the collector-to-collector current gain is given by

$$\overline{A}'_{IK} = \frac{\overline{I}_{CK}}{\overline{I}_{c(K-1)}}$$

For the same $K^{\text{th}}$ stage, the base-to-collector current gain is given by

$$\overline{A}_{IK} = \frac{\overline{I}_{CK}}{\overline{I}_{bK}}$$

These two current gains can be related by the equation,

$$\overline{A}'_{IK} = \overline{A}_{IK} \frac{R_{C(K-1)}}{R_{C(K-1)} + R_{iK}} \tag{2.11}$$

This may be substituted in Eq. (2.10) to give the resultant current gain $\overline{A}_I$.

The procedure for calculating the resultant current gain $\overline{A}_I$ is as follows.

(i) Find the base-to-collector current gain $\overline{A}_{In}$ for the last stage, i.e., $n^{\text{th}}$ stage using

$$\overline{A}_{In} = \frac{-h_{fe}}{1 + h_{oe} R_{Ln}}$$

(ii) Find input impedance,

$$R_{in} = h_{ie} + h_{re} A_{In} R_{Ln}$$

(iii) Calculate the effective load resistance $R_{L(n-1)}$ for the last stage.

$$R_{L(n-1)} = R_{C(n-1)} \parallel R_{i(n)}$$

(iv) Calculate

$$\overline{A}_{I(n-1)} = \frac{-h_{fe}}{1 + h_{oe} R_{L(n-1)}}$$

Proceed in this manner to find $\overline{A}_{IK}$.

(v) Find the collector-to-collector current gain $\overline{A}'_{IK}$ for the $K^{th}$ stage using

$$\overline{A}'_{IK} = \overline{A}_{IK} \frac{R_{C(K-1)}}{\overline{R}_{C(K-1)} + R_{iK}}$$

(vi) Find the resultant current gain $\overline{A}_I$ of the $n$-stage cascaded amplifier using

$$\overline{A}_I = \overline{A}_{I1} \cdot A'_{I2} \cdot A'_{I3} \ldots \overline{A}'_{In}$$

***Power Gain*** The power gain of an $n$-stage amplifier is given by

$$\overline{A}_P = \frac{\text{Ouput power of last stage}}{\text{Input power of first stage}}$$

$$= \frac{\overline{V}_o \overline{I}_o}{V_1 \overline{I}_{b1}} = \frac{\overline{V}_o \overline{I}_{cn}}{V_1 \overline{I}_{b1}}$$

$$= \overline{A}_V \, \overline{A}_I \tag{2.12}$$

Substituting $\overline{A}_V = \overline{A}_I \frac{R_{cn}}{R_{i1}}$

$$\overline{A}_P = (\overline{A}_I)^2 \frac{R_{cn}}{R_{i1}}$$

***Input Impedance*** By starting from the last stage and proceeding towards the first stage, the input impedance can be found out as follows.

Find (i) $\overline{A}_{In} = \dfrac{-h_{fe}}{1 + h_{oe} R_{Ln}}$

(ii) $\overline{R}_{in} = h_{ie} + h_{re} \overline{A}_{In} R_{Ln}$

(iii) $\overline{R}_{L(n-1)} = R_{C(n-1)} \parallel R_{i(n)}$

$\overline{R}_{L(n-1)}$ is the effective load impedance of the $(n-1)^{th}$ stage.

(iv) Calculate $\overline{A}_{I(n-1)}$, $\overline{R}_{i(n-1)}$ and $\overline{R}_{L(n-2)}$ from the above equations.

(v) Proceed in this manner to find the effective input impedance ($R_i$) of the first stage.

***Output Impedance*** The output impedance of each transistor amplifier stage and that of the complete multistage amplifiers may be calculated starting from the first stage. The output admittance of the first transistor,

$$Y_{o1} = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s} \tag{2.13}$$

$R_{o1} = \dfrac{1}{Y_{o1}}$ gives the output impedance of the first transistor.

Parallel combination of $R_{o1}$ with $R_{c1}$ forms the output impedance of the first stage.

$$R_{ot1} = \frac{R_{o1} R_{c1}}{R_{o1} + R_{c1}}$$

This $R_{ot1}$ forms the source impedance of the second-stage. Once again, use Eq. (2.13) to find $Y_{o2}$ with $R_s$ replaced by $R_{ot1}$.

Find $R_{ot2} = R_{o2} \parallel R_{c2}$, where $R_{o2} = \dfrac{1}{Y_{o2}}$.

Similarly, proceed to find the output impedance of the last stage.

The above methods can be used for common-base and common-collector configurations, also as well as for combination of these three configurations.

## EXAMPLE 2.5

For the two-stage CE-CC amplifier circuit shown in Fig. 2.13, find the input and output impedances and individual as well as overall current gains and voltage gains. The *h*-parameters of the transistors at the quiescent points are $h_{ie} = 1600\ \Omega$; $h_{fe} = 60$, $h_{re} = 5 \times 10^{-4}$, $h_{oe} = 25\ \mu A/V$, $h_{ic} = 1600\ \Omega$; $h_{fc} = -61$, $h_{rc} = 1$ and $h_{oc} = 25\ \mu A/V$.

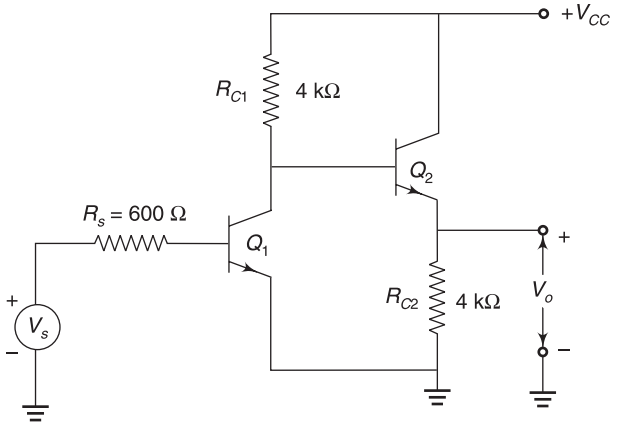



**Fig. 2.13** *CE–CC amplifier*

**Solution** The ac equivalent circuit of the CE-CC amplifier is shown in Fig. 2.14(a).

As shown in Fig. 2.14(b), the collector resistance of the first stage is shunted by the input impedance of the next stage. Compute the current gain, the input impedance and the voltage gain of the second-stage and then proceed towards the first stage. The output impedance can be calculated by starting the analysis with the first stage and proceeding towards the output stage, i.e., second stage.

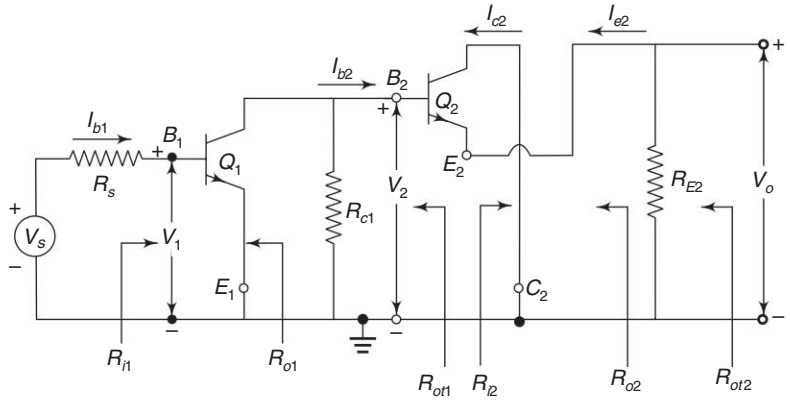
*The second stage*

The current gain of a particular stage is given by

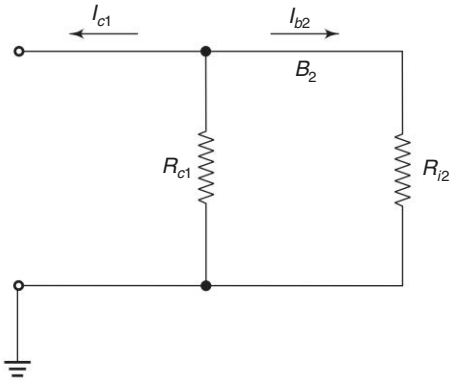
$$A_I = -\frac{h_f}{1 + h_o Z_L}$$

For the second stage $Z_L = R_{E_2}$ and the current gain of the second stage is

$$A_{I2} = \frac{-I_{e2}}{I_{b2}} = \frac{-h_{fc}}{1 + h_{oc} R_{E2}}$$




(a) ac equivalent circuit of CE-CC amplifier




(b) Relating to the calculation of overall current gain

**Fig. 2.14**

$$A_{I2} = \frac{61}{1 + 25 \times 10^{-6} \times 4000} = 55.45$$

The input impedance $R_i$ of a particular stage is given by

$$R_i = h_i + h_r A_I Z_L$$

For the second stage,

$$\begin{aligned} R_{i2} &= h_{ic} + h_{rc} A_{I_2} R_{E2} \\ &= 1600 + 1 \times 55.45 \times 4000 \\ &= 223.4 \text{ k}\Omega \end{aligned}$$

Thus, the CC stage has a high input impedance.

The voltage gain of a particular stage is

$$A_V = \frac{A_I Z_L}{Z_i}$$

For the second stage,

$$A_{V2} = \frac{V_o}{V_2} = \frac{A_{I2}\, R_{E2}}{R_{i2}}$$

$$= \frac{55.45 \times 4000}{223.4 \times 10^3} = 0.993$$

The first stage

$$R_{L1} = R_{c1} \parallel R_{i2}$$

$$= \frac{4000 \times 223.4 \times 10^3}{4000 + 223.4 \times 10^3} = 3.92\ \text{k}\Omega$$

Current gain,

$$A_{I1} = \frac{-I_{c1}}{I_{b1}} = \frac{-h_{fe}}{1 + h_{oe}\, R_{L1}}$$

$$= \frac{-60}{1 + 25 \times 10^{-6} \times 3.92 \times 10^3} = -54.6$$

The input impedance of the first stage, which is also the input impedance of the cascaded amplifier is

$$R_{i1} = h_{ie} + h_{re} A_{I1} R_{L1}$$
$$= 1600 + 5 \times 10^{-4} \times (-54.6) \times 3.92 \times 10^3$$
$$= 1.71\ \text{k}\Omega$$

The voltage gain of the first stage is

$$A_{V1} = \frac{V_2}{V_1} = \frac{A_{I1}\, R_{L1}}{R_{i1}}$$

$$= \frac{-54.6 \times 3.92 \times 10^3}{1.71 \times 10^3} = -125.16$$

The output admittance of the first transistor $Q_1$

$$Y_{o1} = h_{oe} - \frac{h_{fe}\, h_{re}}{h_{ie} + R_s}$$

$$= 25 \times 10^{-6} - \frac{60 \times 5 \times 10^{-4}}{1600 + 600} = 11.4\ \mu\text{A/V}$$

The output impedance of the first stage

$$R_{o1} = \frac{1}{Y_{o1}} = 87.72\ \text{k}\Omega$$

The output impedance taking $R_{c1}$ into account is

$$R_{ot1} = R_{o1} \parallel R_{c1}$$

$$= \frac{87.72 \times 10^3 \times 4 \times 10^3}{(87.72 \times 10^3) + (4 \times 10^3)} = 3.82\ \text{k}\Omega$$

This is the effective source resistance $R'_{s2}$ of the second stage.

The output admittance of the second stage

$$Y_{o_2} = h_{oc} - \frac{h_{fc}\, h_{rc}}{h_{ic} + R_{ot1}}$$

$$= (25 \times 10^{-6}) - \frac{(-61) \times (1)}{(1600) + (3.82 \times 10^{3})}$$

$$= 25 \times 10^{-6} + 11.5 \times 10^{-3}$$

$$= 11.525 \times 10^{-3}\ \text{A/V}$$

Output impedance,

$$R_{o2} = \frac{1}{Y_{o2}} = 87\ \Omega$$

The amplifier output impedance taking $R_{E2}$ into account is $R_{o2} \parallel R_{E2}$

Hence,

$$R_{o2} = \frac{R_{o2} \times R_{E2}}{R_{o2} + R_{E2}}$$

$$= \frac{87 \times 4000}{87 + 4000} = 85.15\ \Omega$$

*Overall current gain:* The overall or total current gain of both the stages is

$$A_I = \frac{-I_{e2}}{I_{b1}} = \frac{-I_{e2}}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}}$$

$$= -A_{12} \left( \frac{I_{b2}}{I_{c1}} \right) A_{I1}$$

From Fig. 2.14(b),

$$I_{b2} = (-I_{c1}) \frac{R_{c1}}{R_{c2} + R_{i2}}$$

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1} + R_{i2}}$$

$$= -\frac{4 \times 10^{3}}{4 \times 10^{3} + 223.4 \times 10^{3}} = -17.6 \times 10^{-3}$$

$$A_I = A_{I2}\, A_{I1} \frac{R_{c1}}{R_{i2} + R_{c1}}$$

$$= (55.45)\ (-54.6) \times 17.6 \times 10^{-3} = -53.23$$

The overall voltage gain of the amplifier,

$$A_V = \frac{V_o}{V_1} = \frac{V_o}{V_2} \cdot \frac{V_2}{V_1}$$

$$= A_{V2}\, A_{V1}$$

$$= (0.993)(-125.16) = -124.3$$

The overall voltage gain taking the source impedance into account,

$$A_{Vs} = \frac{V_o}{V_s} = A_V \frac{R_{i1}}{R_{i1} + R_s}$$

$$= (-124.3) \frac{1.71 \times 10^3}{1.71 \times 10^3 + 600} = -92$$

## 2.6 CHOICE OF TRANSISTOR CONFIGURATION IN A CASCADE AMPLIFIER

The choice of transistor configuration depends on the maximum voltage gain expected from the cascade amplifier. Thus, for intermediate stages in a cascade amplifier, the common-collector configuration cannot be used since such a stage has a voltage gain less than unity. The common-base configuration is also rarely used in the intermediate stages since the resultant voltage gain of such a cascade amplifier is also low and is almost equal to that of the last stage alone. The proof for this can be given as follows.

From Eq. (2.4), the voltage gain,

$$A_{VK} = \frac{A_{IK}\, R_{LK}}{R_{iK}}$$

But $R_{LK} = R_{CK} \parallel R_i(K + 1)$

Thus, $R_{LK} < R_i(K + 1)$

Assuming the stages to be identical $R_i(K + 1) = R_{iK}$, the effective load resistance $R_{LK} < R_{iK}$.

Further, the maximum value of current gain $A_{Ib}$ is $h_{fb}$ which is less than unity but only slightly less. Accordingly, the voltage gain of any stage ($A_{VK}$) except the output stage is less than unity. Hence, for intermediate stages common base configuration is not suitable.

The common-emitter configuration is popularly used in the intermediate stages since the short-circuit current gain $h_{fe}$ is very much greater than unity. Thus, it is possible to obtain a high voltage gain by cascading CE stages.

***Input and Output Stages*** Here, the consideration is not the maximum voltage gain but impedance matching of the source and the input circuit of the first stage. Thus, some transistors driving a cascade amplifier require almost open circuit, while others require an almost short-circuit operation. Accordingly, one may prefer CC or CB configurations as the input stage, thereby securing proper impedance match and sacrificing voltage or current gain. A similar choice is made for the output stage.

## 2.7 TWO-STAGE *RC* COUPLED AMPLIFIER

Figure 2.15 shows the two-stage *RC* coupled common-emitter amplifier. The two transistors are identical and a common power supply is used. $R_C$ is the collector (load) resistor. Resistors $R_1$, $R_2$ and $R_E$ provide the required bias. The bypass capacitor $C_E$ prevents loss of amplification due to negative feedback. The output of the first stage gets coupled to the input of the second-stage via coupling capacitor $C_C$ which also serves as the blocking capacitor to keep the dc component of the output of the first stage from reaching the input of the second-stage and to pass the ac component.

### *Operation*

The ac input signal applied at the base is amplified by the transistor $Q_1$ as shown in Fig. 2.15.

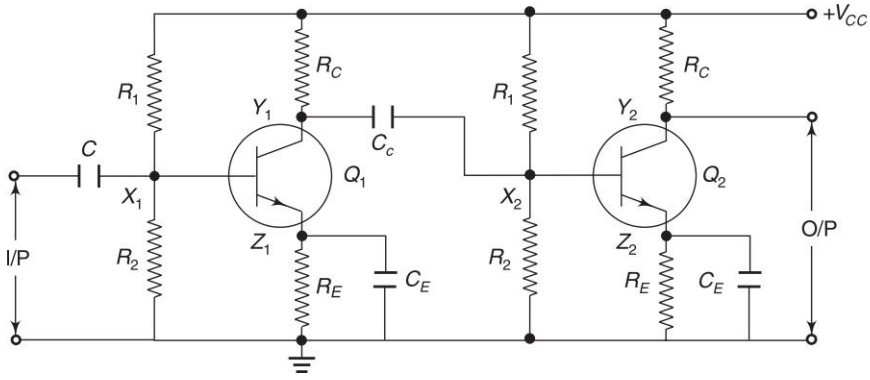



**Fig. 2.15** *A two-stage RC coupled amplifier*

Its phase is reversed and the amplified output appears across its collector load $R_C$. The output of the first stage across $R_C$ is given to the base of the second-stage transistor $Q_2$ through the coupling capacitor $C_c$. This signal at the base of $Q_2$ is further amplified and its phase is again reversed. Hence, the output signal is the twice amplified replica of the input signal. The output signal is in phase with the input signal because it has been reversed twice.

In the mid-frequency range, the gain is constant because the coupling and bypass capacitors are as good as short circuits. On both sides of the mid-frequency range, the gain decreases. At high frequencies, the value $\beta$ of the transistor decreases. Hence, the reactance of the capacitor $C_c$ increases with the reduction in frequency of the signal, the voltage gain of the amplifier reduces. At very low and very high frequencies, the gain of the amplifier reduces to almost zero.

#### Advantages of *RC* Coupling

1. It requires cheap components like resistors and capacitors and not expensive or bulky components. Hence, it is small, light, and inexpensive.
2. It gives uniform voltage amplification over a wide frequency range from a few Hz to a few MHz because resistor values are independent of frequency changes. Hence, *RC* coupled amplifier can be used to great advantage in speech, music, etc.
3. Since it does not use any coil or transformer which may pick up unwanted signals, it has minimum possible non-linear distortion. Hence, there is no magnetic field to interface with the signal.
4. Its overall amplification is higher than that of the other couplings.

### Disadvantages of *RC* Coupling

1. Due to large drop across collector-load resistors, the collectors work at relatively small voltages unless higher supply voltage is used to overcome this voltage drop.
2. It is noisy in humid weather.
3. The impedance matching is poor as the output impedance of the *RC* coupled amplifier is several hundred ohms while that of a speaker is only a few ohms. Hence, the amount of power transferred to the speaker is reduced.

### Differences in Performance of an *RC* Coupled Amplifier Over Single-Stage

1. Its overall amplification is higher.
2. Its non-linear distortion is less.
3. It has better fidelity over a wide frequency range.
4. Its frequency response is much better over the audio-frequency range.

**Applications** Since audio fidelity is excellent over a wide range of frequencies, the *RC* coupled amplifier is extensively employed as a voltage amplifier, e.g., in the initial stages of a public address system. However, as the impedance matching is poor, reduced power is transferred to the speaker.

***Analysis of RC Coupled CE Amplifier*** For finding the response of the *RC* coupled amplifier, in the three frequency ranges, the transistor $Q_1$ of Fig. 2.16 is replaced by its high-frequency $\pi$ model yielding the equivalent circuit of Fig. 2.17. Here, $C_{s1}$ and $C_{s2}$ represent stray capacitances caused by wiring, proximity of components to chassis, etc. $R_B = R_1 \parallel R_2$ is the biasing resistance of a particular stage.

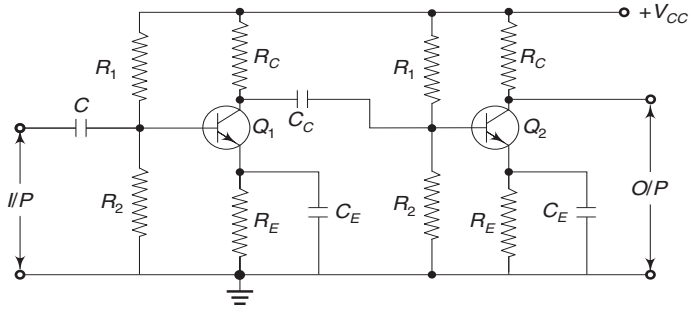



**Fig. 2.16** *A two-stage RC coupled amplifier*

The equivalent circuit of Fig. 2.17 may be modified by Miller's theorem by which the parallel combinations of $r_{b'c}$ and $C_{b'c}$ are replaced by the corresponding impedances in the input circuit and the output circuit. The modified equivalent circuit is shown in Fig. 2.18.

As the equivalent circuit of Fig. 2.18 is quite complicated, it may be simplified with a few assumptions as follows:

(i) Making use of the fact that in most cases, the time constant of the output shunt circuit is negligible as compared with that of the input circuit, the capacitances $\frac{C_{b'c}(A-1)}{A}$, $C_{b'e}$ and $C_{s2}$ may be omitted from the output circuit.

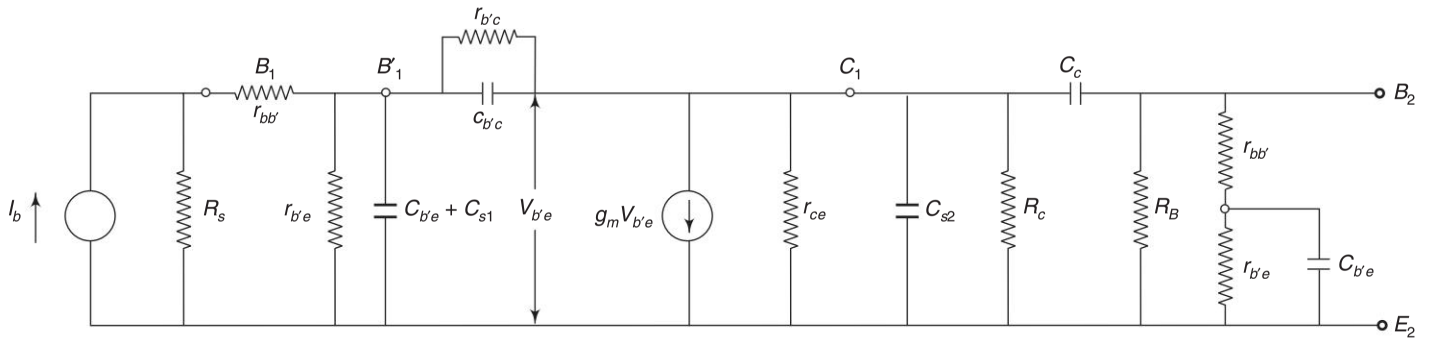



**Fig. 2.17** *Equivalent circuit of an RC coupled amplifier*

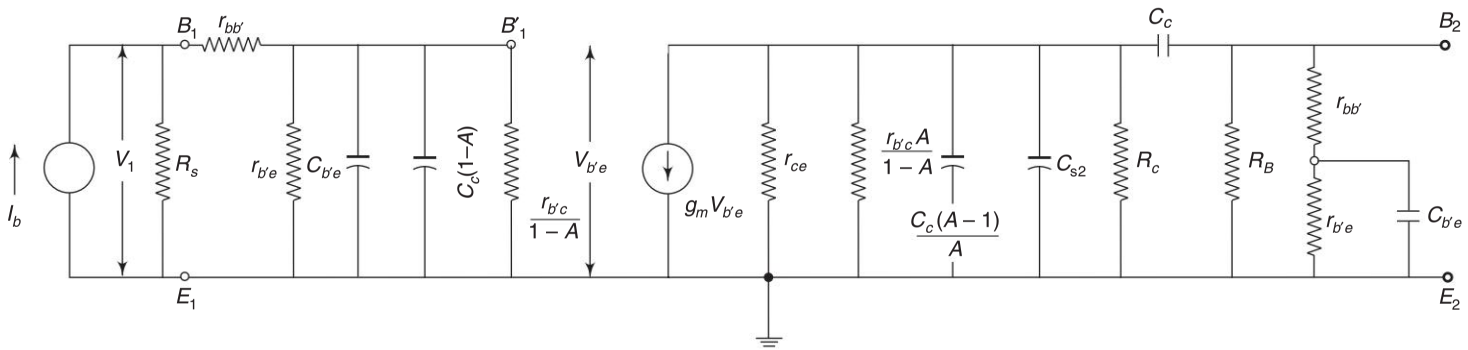



**Fig. 2.18** *Modified equivalent circuit of an RC coupled amplifier*

(ii) Since $A$ is equal to $\frac{V_{ce}}{V_{b'e}}, |A| >> 1$. Hence, $r_{b'c}\left(\frac{A}{A-1}\right) \approx r_{b'c}$. But $r_{b'c} >> r_{ce}$.

Hence, $r_{b'c}\left(\frac{A}{A-1}\right) \| r_{ce} \approx r_{ce}$ and $r_{b'c}\left(\frac{A}{A-1}\right)$ is omitted from the output circuit.

(iii) For typical values of transistor parameters and circuit components $\frac{r_{b'c}}{1-A} >> r_{b'e}$.

Hence, $\frac{r_{b'c}}{1-A} \| r_{b'e} \approx r_{b'e}$. Hence $\frac{r_{b'c}}{1-A}$ is neglected in the input circuit.

(iv) Referring to Table 4.2 of Chapter 4, we have

$$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - (1 + h_{fe})\, g_{b'c}$$
$$\approx h_{oe} - h_{fe}\, g_{b'c}$$
$$= h_{oe} - h_{fe}\left(\frac{h_{re}}{r_{b'e}}\right)$$

Thus,
$$g_{ce} = \frac{1}{r_{ce}} \approx h_{oe} - g_m\, h_{re}$$

It can be assumed that $\frac{1}{r_{ce}} \approx h_{oe}$ without introducing much error. Since $r_{ce}$ comes in shunt with much smaller load resistance $R_C$ (typically 250 Ω), $r_{ce}$ may be replaced by $\frac{1}{h_{oe}} = R_o$ (say).

(v) $r_{bb'}$ and $r_{b'e}$ can be combined to form $R_i = h_{ie}$.

(vi) $C$ is the parallel combination of $C_{b'e}$, $C_{S1}$ and $C_{b'c}\,(1 - A)$.

With the above simplifying assumptions, the circuit of Fig. 2.18 reduces to the equivalent circuit shown in Fig. 2.19.

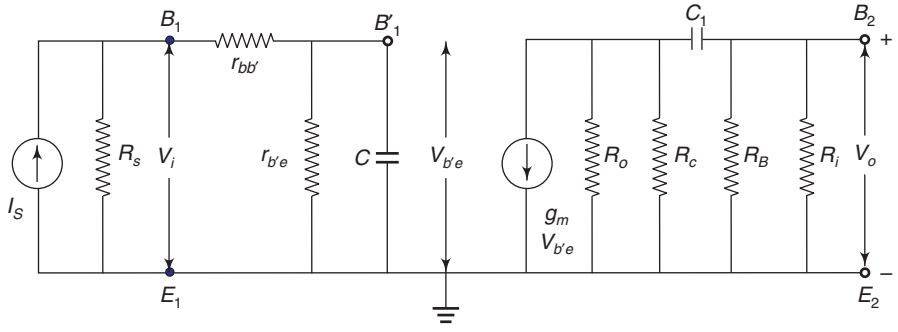



**Fig. 2.19** *Simplified equivalent circuit of an RC coupled amplifier*

Let $R'_C$ represent the parallel combination of $R_o$ and $R_C$, and similarly, let $R'_i$ represent the parallel combination of $R_i$ and $R_B$. Then the circuit reduces to that shown in Fig. 2.20.

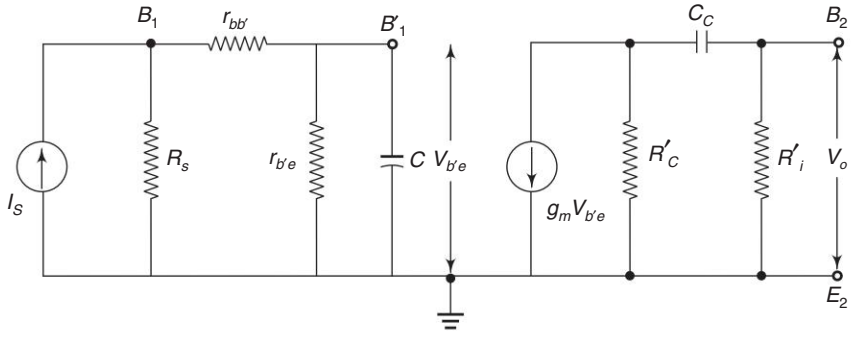



**Fig. 2.20** *Simplified equivalent circuit of an RC coupled amplifier*

In most cases, $R_o >> R_C$; hence, $R'_C = R_C \parallel R_o \approx R_C$. Similarly, $R_B >> R_i$; hence, $R'_i = R_i \parallel R_B \approx R_i$ leading to the circuit shown in Fig. 2.21. In those circuits where these approximations are not valid, $R'_c$ and $R'_i$ can be taken instead of $R_C$ and $R_i$.

The analysis of an *RC* coupled amplifier for the three frequency ranges can be done using the simplified equivalent circuit shown in Fig. 2.21.

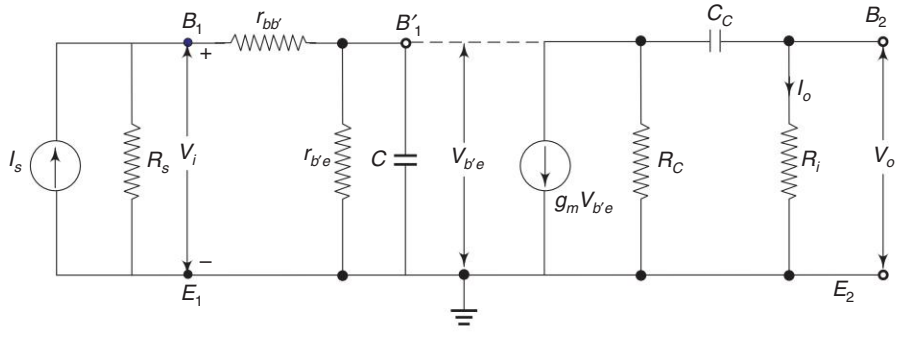



**Fig. 2.21** *Simplified equivalent circuit of an RC coupled amplifier*

***Middle Frequency Range or Mid-band*** In the mid-frequency range, the reactance offered by $C_c$ is small enough so that it can be omitted. Further, the frequency is small enough to make the shunt capacitor-reactance $\left( X_C = \frac{1}{\omega C} \right)$ extremely large. Hence, $C$ can be omitted in the equivalent circuit leading to the circuit shown in Fig. 2.22. Let $I_o$ be the current through the resistor $R_i$. This current $I_0$ is the useful output current from the first stage and hence, forms the input current for the next stage.

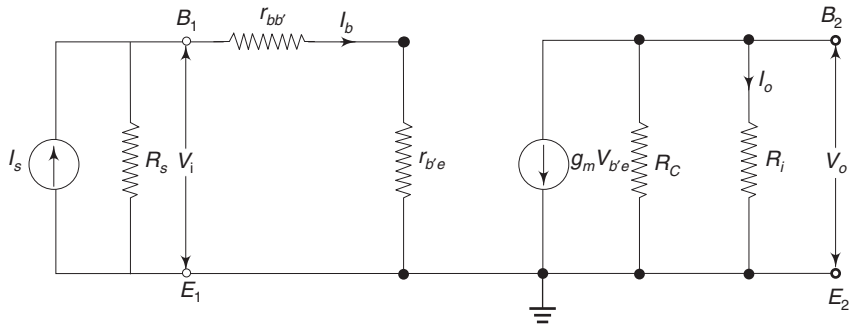



**Fig. 2.22** *Simplified equivalent circuit of an RC coupled amplifier for mid-band range*

***Current Gain, $A_{Im}$***

$$A_{Im} = \frac{I_o}{I_b}$$

$$I_o = -g_m V_{b'e} \frac{R_C}{R_C + R_i}$$

$$A_{Im} = -\frac{g_m V_{b'e}}{I_b} \frac{R_C}{R_C + R_i}$$

But $V_{b'e} = I_b r_{b'e}$

Hence,
$$A_{Im} = -g_m r_{b'e} \frac{R_C}{R_C + R_i} \tag{10.14}$$

As $g_m r_{b'e} = h_{fe}$,

$$A_{Im} = -h_{fe} \frac{R_C}{R_C + R_i} \tag{10.15}$$

Hence, current gain $A_{Im}$ in the mid-band is independent of frequency.

***Voltage Gain, $A_{Vm}$***

$$A_{Vm} = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{b'e} R_{ci} = -g_m I_b r_{b'e} R_{ci}$$

where $R_{ci} = R_C \parallel R_i$

$$V_i = I_b (r_{bb'} + r_{b'e}) = I_b h_{ie}$$

Hence,
$$A_{Vm} = \frac{V_o}{V_i} = \frac{-g_m I_b r_{b'e} R_{ci}}{I_b h_{ie}}$$

Substituting $g_m r_{b'e} = h_{fe}$,

$$A_{Vm} = \frac{-h_{fe} R_{ci}}{h_{ie}} \tag{10.16}$$

***Low-Frequency Range*** In the low frequency range, the capacitor $C$ is omitted since its reactance is extremely large as $X_C \parallel r_{b'e} \approx r_{b'e}$. However, the capacitor $C_c$ cannot be neglected leading to the equivalent circuit shown in Fig. 2.23.

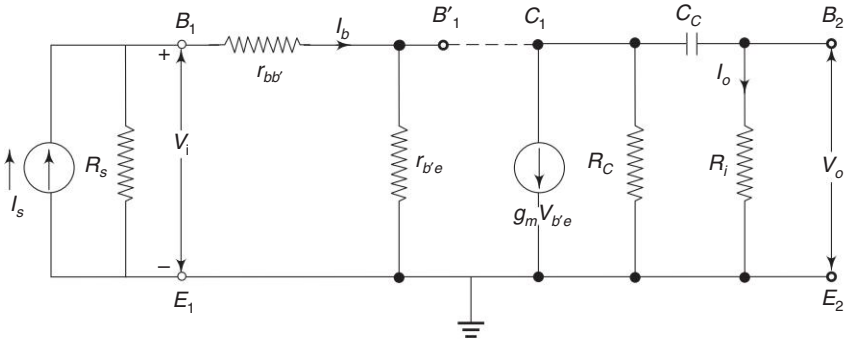



**Fig. 2.23** *Simplified equivalent circuit of an RC coupled amplifier in the low-frequency range*

***Current Gain, $A_{Il}$***

$$A_{Il} = \frac{I_o}{I_b}$$

From Fig. 10.18,

$$I_o = -g_m V_{b'e} \frac{R_C}{R_C + (R_i - jX_{C_c})}$$

$$= -g_m V_{b'e} \frac{R_C}{R_C + R_i + \dfrac{1}{j\omega C_c}}$$

$$= -g_m I_b r_{b'e} \frac{R_C}{R_C + R_i + \dfrac{1}{j\omega C_c}}$$

Hence, the current gain,

$$A_{Il} = \frac{I_o}{I_b} = -g_m r_{b'e} \frac{R_C}{R_C + R_i + \dfrac{1}{j\omega C_c}}$$

$$= -h_{fe} \frac{R_C}{R_C + R_i + \dfrac{1}{j\omega C_c}} \qquad (10.17)$$

or

$$= \frac{-h_{fe} R_C}{R_C + R_i} \frac{R_C + R_i}{R_C + R_i + \dfrac{1}{j\omega C_c}}$$

$$= A_{Im} \frac{R_C + R_i}{R_C + R_i + \dfrac{1}{j\omega C_c}}$$

$$= A_{Im} \frac{(R_C + R_i)}{(R_C + R_i)\left[1 + \dfrac{1}{j\omega C_c (R_C + R_i)}\right]}$$

$$= \frac{A_{Im}}{\left[1 - \dfrac{j}{2\pi f C_c (R_C + R_i)}\right]}$$

$$A_{Il} = \frac{A_{Im}}{1 - \dfrac{j f_L}{f}} \tag{2.18}$$

where

$$f_L = \frac{1}{2\pi C_c (R_C + R_i)} \tag{2.19}$$

$$|A_{Il}| = \frac{|A_{Im}|}{\sqrt{1 + (f_L/f)^2}}$$

The phase angle of current gain at any frequency $f$ is given by

$$\Phi_{Il} = \text{phase angle of } A_{Im} + \tan^{-1}\left(\frac{f_L}{f}\right)$$

$$= 180° + \tan^{-1}\left(\frac{f_L}{f}\right)$$

$$= 180° + \tan^{-1}\left(\frac{1}{2\pi f C_c (R_C + R_i)}\right)$$

At $f = f_L, |A_{IL}| = \dfrac{|A_{Im}|}{\sqrt{2}} = 0.707\,|A_{Im}|$

Thus, $f_L$ forms the lower 3 dB frequency for the current gain.

**Voltage Gain $A_{Vl}$**

$$A_{Vl} = \frac{V_o}{V_i}$$

$$V_o = I_o R_i = -g_m I_b r_{b'e} \frac{R_C R_i}{R_C + R_i + \dfrac{1}{j\omega C_c}}$$

$$V_i = I_b(r_{bb'} + r_{b'e}) = I_b h_{ie}$$

Hence, the voltage gain is given by

$$A_{Vl} = \frac{V_o}{V_i} = \frac{-g_m I_b r_{b'e} R_C R_i}{(I_b h_{ie})\left[R_C + R_i + \dfrac{1}{j\omega C_c}\right]}$$

$$= \frac{-h_{fe}}{h_{ie}} \frac{R_C R_i}{(R_C + R_i)\left[1 + \dfrac{1}{j\omega C_c (R_C + R_i)}\right]} \qquad (\text{since } h_{fe} = g_m r_{b'e})$$

$$= \frac{-h_{fe}}{h_{ie}} \frac{R_{ci}}{\left[1 - \dfrac{j}{2\pi f C_c (R_C + R_i)}\right]}$$

where $R_{ci} = R_C \parallel R_i$.

Therefore,
$$A_{Vl} = \frac{A_{Vm}}{1 - \dfrac{j}{2\pi f C_c (R_C + R_i)}}$$

$$= \frac{A_{Vm}}{1 - j\dfrac{f_L}{f}} \tag{2.20}$$

where
$$f_L = \frac{1}{2\pi C_c (R_C + R_i)} \tag{2.21}$$

Also,
$$|A_{Vl}| = \frac{|A_{Vm}|}{\sqrt{1 + (f_L/f)^2}}$$

Phase angle of the voltage gain $A_{Vl}$ is given by

$$\Phi_{Vl} = \text{phase angle of } A_{Vm} + \tan^{-1}\left(\frac{f_L}{f}\right)$$

$$= 180° + \tan^{-1} \frac{1}{2\pi f C_c (R_C + R_i)}$$

At $f = f_L$,

$$|A_{Vl}| = \frac{|A_{Vm}|}{\sqrt{2}} = 0.707 |A_{Vm}|$$

Thus, $f_L$ forms the lower 3 dB frequency for the voltage gain.

Since in both derivations for current gain and voltage gain

$$f_L = \frac{1}{2\pi C_c (R_C + R_i)}$$

the lower 3 dB frequencies are the same.

### *High-frequency Range*

In this frequency range, coupling capacitance $C_c$ can be omitted since its reactance is small, whereas the shunt capacitance $C$ cannot be neglected to the equivalent circuit of Fig. 2.24.

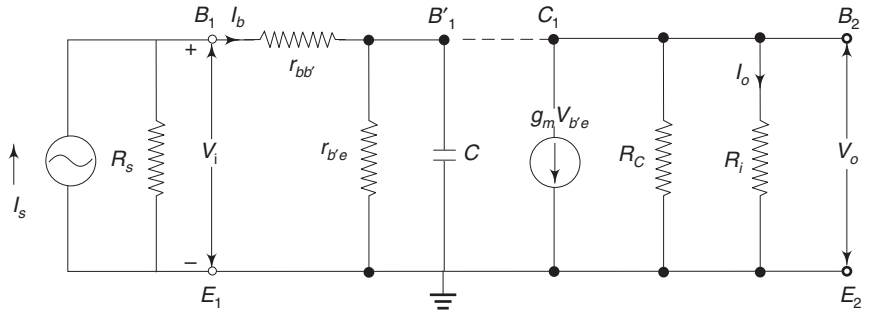



**Fig. 2.24** *Equivalent circuit of RC coupled amplifier in high-frequency range*

#### Current Gain, $A_{Ih}$

$$I_o = -g_m V_{b'e} \frac{R_C}{R_C + R_i}$$

But
$$V_{b'e} = \frac{I_b}{\frac{1}{r_{b'e}} + j\omega C}$$

$$= \frac{I_b r_{b'e}}{1 + j\omega C r_{b'e}}$$

Therefore,
$$I_o = -g_m \left( \frac{I_b r_{b'e}}{1 + j\omega C r_{b'e}} \right) \frac{R_C}{R_C + R_i}$$

Hence, the current gain in the high-frequency range,

$$A_{Ih} = \frac{I_o}{I_b} = -g_m r_{b'e} \frac{R_C}{R_C + R_i} \cdot \frac{1}{1 + j\omega C r_{b'e}}$$

$$A_{Ih} = \frac{A_{Im}}{1 + j\omega C r_{b'e}}$$

Let
$$f_H = \frac{1}{2\pi C r_{b'e}} \tag{2.22}$$

Therefore,
$$A_{Ih} = \frac{A_{Im}}{1 + j(f/f_H)} \tag{2.23}$$

$$|A_{Ih}| = \frac{|A_{Im}|}{\sqrt{1 + (f/f_H)^2}}$$

At $f = f_H$,

$$|A_{Ih}| = \frac{|A_{Im}|}{\sqrt{2}} = 0.707|A_{Im}|$$

Hence, $f_H$ forms the upper 3 dB frequency.

Phase angle of the current gain at any frequency $f$ is given by

$$\phi_{Ih} = \text{phase angle of } A_{Im} - \tan^{-1}(f/f_H)$$
$$= 180° - \tan^{-1}(2\pi f C r_{b'e}).$$

**Voltage Gain, $A_{vh}$**

$$V_o = -g_m V_{b'e}(R_{Ci})$$

where $R_{ci} = R_c \parallel R_i$

$$V_o = -g_m R_{ci} \frac{I_b}{\frac{1}{r_{b'e}} + j\omega C} = -g_m R_{ci} \frac{r_{b'e} I_b}{1 + j\omega C r_{b'e}}$$

Substituting $g_m r_{b'e} = h_{fe}$, we get

$$V_o = -h_{fe} \frac{R_{ci} I_b}{1 + j\omega C r_{b'e}}$$

$$V_i = I_b (r_{bb'} + r_{b'e})$$
$$= I_b h_{ie}$$

$$A_{Vh} = \frac{V_o}{V_i} = \frac{-h_{fe}}{h_{ie}} \cdot \frac{R_{ci}}{1 + j\omega C r_{b'e}} \tag{2.24}$$

Substituting $A_{Vm} = \frac{-h_{fe} R_{ci}}{h_{ie}}$ we get

$$A_{Vh} = \frac{A_{Vm}}{1 + j2\pi f C r_{b'e}} \tag{2.25}$$

$$= \frac{A_{Vm}}{1 + j(f/f_H)}$$

where $f_H = \frac{1}{2\pi C r_{b'e}}$ (2.26)

Also $|A_{Vh}| = \frac{|A_{Vm}|}{\sqrt{1 + (f/f_H)^2}}$

At $f = f_H$, $|A_{Vh}| = \frac{|A_{Vm}|}{\sqrt{2}} = 0.707\,|A_{Vm}|$

Thus, $f_H$ forms the upper 3 dB frequency.

Phase angle of the voltage gain at any frequency '$f$',

$$\phi_{Vh} = \text{phase angle of } A_{Vm} - \tan^{-1}(f/f_H)$$
$$= 180° - \tan^{-1}(2\pi f C r_{b'e})$$

Since $f_H = \dfrac{1}{2\pi C r_{b'e}}$ in both cases, the upper 3 dB frequencies of $A_{Ih}$ and $A_{Vh}$ are same.

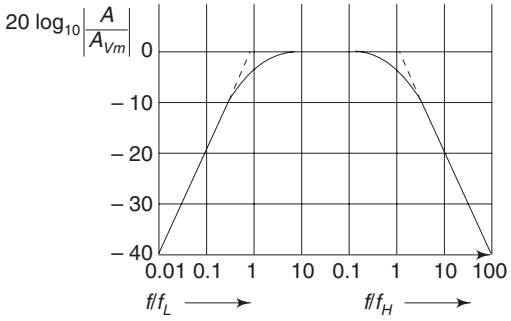



**Fig. 2.25** *Plot of gain versus frequency for an RC coupled amplifier*

***True Mid-band*** A plot of $\left|\dfrac{A}{A_{Vm}}\right|$ in dB against frequency $f$ on log scale is shown in Fig. 2.25.

From Fig. 2.25, the 3 dB bandwidth extends from $f_L$ to $f_H$. Thus, the 3 dB bandwidth is equal to $f_H - f_L \approx f_H$.

But the true mid-band in which the gain remains truly constant extends from $10\,f_L$ to $0.1\,f_H$. A plot of $\left|\dfrac{A_I}{A_{Im}}\right|$ in dB against frequency will result in a similar curve.

***Gain Bandwidth Product*** The gain-bandwidth product for the current gain is given by

$$|A_{Im} f_H| = h_{fe} \frac{R_C}{R_C + R_i} \cdot \frac{1}{2\pi C r_{b'e}}$$
$$= \frac{g_m r_{b'e}}{2\pi C r_{b'e}} \cdot \frac{R_C}{R_C + R_i}$$
$$= \frac{g_m}{2\pi C} \cdot \frac{R_C}{R_C + R_i} \tag{2.27}$$

Similarly, the gain-bandwidth product for the voltage gain is given by

$$|A_{Vm} f_H| = \frac{h_{fe}}{h_{ie}} \cdot R_{ci} \frac{1}{2\pi C r_{b'e}}$$
$$= \frac{g_m}{2\pi C} \frac{R_{ci}}{h_{ie}} \qquad (\text{since } h_{fe} = g_m r_{b'e}) \tag{2.28}$$

## EXAMPLE 2.6

A CE, *RC* coupled amplifier uses transistors with the following *h*-parameters: $h_{fe}$ = 50, $h_{ie}$ = 1200 Ω, $h_{oe} = 30 \times 10^{-6}$ mhos, $h_{re} = 2.5 \times 10^{-4}$. The value of $g_m$ at the operating point is 50 mmhos. The biasing resistor $R_1$ between $V_{CC}$ and the base is 100 kΩ and $R_2$ between the base and ground is 10 kΩ. The load resistor $R_C$ = 5 kΩ. Let ***C*** = 160 pF be the total shunt capacitance in the input circuit and the coupling capacitor $C_C$ = 6 μF. Calculate for one stage of the amplifier (a) mid-band current gain, (b) mid-band voltage gain (c) lower and higher 3 dB frequencies, and (d) gain-bandwidth product.

**Solution**

$$R_o = \frac{1}{h_{oe}} = \frac{10^6}{30} = 33.33 \text{ k}\Omega$$

$$R_B = R_1 \parallel R_2 = 100 \times 10^3 \parallel 10 \times 10^3 = 9.1 \text{ k}\Omega$$

$$R_i = h_{ie} = 1.2 \text{ k}\Omega$$

$$R'_C = R_C \parallel R_o = 5 \times 10^3 \parallel 33.33 \times 10^3 = 4.35 \text{ k}\Omega$$

$$R_i' = R_B \parallel R_i = 9.1 \times 10^3 \parallel 1.2 \times 10^3 = 1.1 \text{ k}\Omega$$

$$R'_{ci} = R'_c \parallel R'_i = 4.35 \times 10^3 \parallel 1.1 \times 10^3 = 0.87 \text{ k}\Omega$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{50}{50 \times 10^{-3}} = 1000 \ \Omega$$

(a) Mid-band current gain,

$$A_{Im} = \frac{-h_{fe} R'_C}{R'_C + R'_i}$$

$$= \frac{-50 \times 4.35 \times 10^3}{4.35 \times 10^3 + 1.1 \times 10^3} = -39.9$$

(b) Mid-band voltage gain,

$$A_{Vm} = -h_{fe} \frac{R'_{ci}}{h_{ie}}$$

$$= 50 \times \frac{0.87 \times 10^3}{1.2 \times 10^3} = -36.25$$

(c) Lower 3 dB frequency,

$$f_L = \frac{1}{2\pi C_C (R'_C + R'_i)}$$

$$= \frac{1}{2\pi \times 6 \times 10^{-6} (4.35 \times 10^3 + 1.1 \times 10^3)} = 4.87 \text{ Hz}$$

Higher 3 dB frequency,

$$f_H = \frac{1}{2\pi C r_{b'e}}$$

$$= \frac{1}{2\pi \times 160 \times 10^{-12} \times 1 \times 10^{3}} = 995.2 \text{ kHz}$$

(d) Voltage gain × Bandwidth

$$|A_{Vm} f_H| = |-36.25 \times 995.2 \times 10^3| = 36.07 \text{ MHz}$$

## 2.8 CASCODE AMPLIFIER CONFIGURATION

The cascode amplifier is a composite amplifier pair with a large bandwidth used for RF applications and as a video amplifier. It consists of a CE stage followed by a CB stage directly coupled to each other and combines some of the features of both the amplifiers.

For high-frequency applications, CB configuration has the most desirable characteristics. However, it suffers from low input impedance ($Z_i \approx h_{ib}$). The cascode configuration is designed to have the input impedance essentially that of CE amplifier, the current gain that of CE amplifier, the voltage gain that of CB amplifier and good isolation between the input and output. Figure 2.26 shows a cascode amplifier.

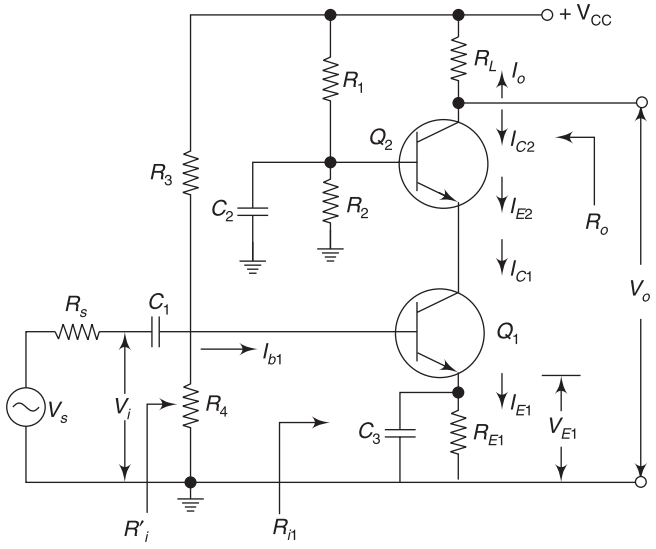



**Fig. 2.26** *Cascode amplifier*

The ac equivalent circuit for cascode amplifier is drawn by shorting the dc supply and coupling capacitors as shown in Fig. 2.27. The simplified *h*-parameter equivalent circuit for cascode amplifier is further drawn by replacing the transistors with their simplified equivalent circuits as shown in Fig. 2.28.

***Analysis of Second-Stage (CB Amplifier)*** From the approximate analysis of a single-stage CB amplifier, we know that

$$A_{i2} = \frac{I_{c2}}{I_{e2}} = \frac{h_{fe}}{1 + h_{fe}}$$

$$R_{i2} = \frac{h_{ie}}{1 + h_{fe}}$$

$$A_{V2} = \frac{V_o}{V_{e2}} = \frac{A_{i2}\, R_L}{R_{i2}}$$

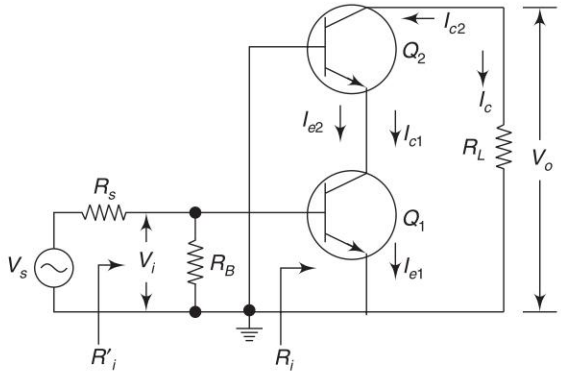



**Fig. 2.27** *ac equivalent circuit of cascode amplifier*

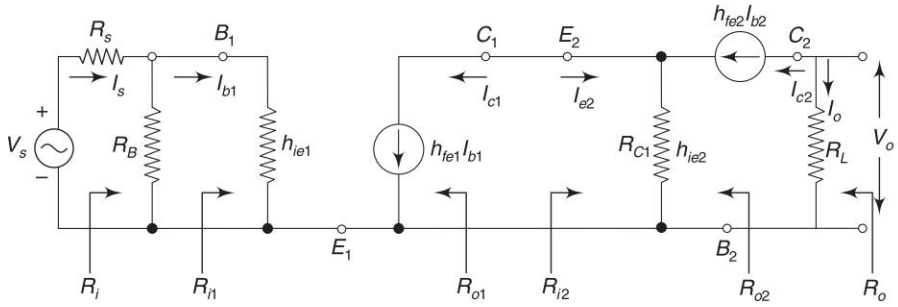



**Fig. 2.28** *Simplified h-parameter equivalent circuit of cascode amplifier*

***Analysis of First-stage (CE Amplifier)*** From the approximate analysis of a single-stage CE amplifier, we know that

$$A_{i1} = \frac{I_{c1}}{I_{b1}} = -h_{fe}$$

$$R_{i1} = h_{ie}$$

$$A_{V1} = \frac{V_{c1}}{V_{b1}} = \frac{A_{i1}\, R_{L1}}{R_{i1}}$$

where $R_{L1} = R_{i2}$

***Voltage Gain ($A_V$)*** The overall voltage gain is the product of individual gains and it is written as

$$A_V = A_{V1} \times A_{V2} = \frac{A_{i1}\, R_{L1}}{R_{i1}} \times \frac{A_{i2}\, R_L}{R_{i2}}$$

***Overall Input Resistance ($R_i$)*** From the simplified circuit, the overall input resistance is given by

$$R_i = R_{i1} \parallel R_B = R_{i1} \parallel R_3 \parallel R_4$$

***Overall Voltage Gain ($A_{vs}$)*** The overall voltage gain by considering the source is given by

$$A_{Vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = A_V \times \frac{R_i}{R_1 + R_s}$$

***Overall Current Gain ($A_{is}$)*** The overall current gain, by considering the source, is written as

$$A_{is} = \frac{I_o}{I_s} = \frac{I_o}{I_{c2}} \times \frac{I_{c2}}{I_{e2}} \times \frac{I_{e2}}{I_{c1}} \times \frac{I_{c1}}{I_{b1}} \times \frac{I_{b1}}{I_S}$$

where $$\frac{I_o}{I_{c2}} = -1, \frac{I_{c2}}{I_{e2}} = -A_{i2}, \frac{I_{e2}}{I_{c1}} = -1, \frac{I_{c1}}{I_{b1}} = -A_{i1}, \frac{I_{b1}}{I_S} = \frac{R_B}{R_B + R_{i1}}$$

***Output Resistance ($R_o$)*** The output resistance of individual stages is very high, i.e., $R_{o1} = R_{o2} = \infty$ and the overall output resistance is almost equal to the load resistance, i.e., $R_o = R_{o2} \parallel R_L \approx R_L$.

## EXAMPLE 2.7

The cascode amplifier shown in Fig. 2.26 makes use of identical transistors $Q_1$ and $Q_2$ with the following $h$-parameters: $h_{fe} = 50$, $h_{ie} = 1.1$ kΩ, $h_{oe} = 10 \times 10^{-6}$ mhos, $h_{re} = 2.5 \times 10^{-4}$. The circuit parameters are $R_s = 1$ kΩ, $R_3 = 200$ kΩ, $R_4 = 10$ kΩ and $R_L = 3$ kΩ. Calculate the overall current gain, voltage gain, input and output resistances.

**Solution** *To find overall input resistance*

Input resistance of the first stage (CE amplifier), $R_{i1} = h_{ie} = 1.1$ kΩ

Input resistance of the second-stage (CB amplifier), $R_{i2} = \frac{h_{ie}}{1 + h_{fe}} = \frac{1.1 \times 10^3}{1 + 50} = 21.56\ \Omega$

Overall input resistance is

$$R_i = R_{i1} \parallel R_B = R_{i1} \parallel R_3 \parallel R_4 = 1.1 \times 10^3 \parallel 200 \times 10^3 \parallel 10 \times 10^3 = 986.1\ \Omega$$

*To find overall current gain*

Current gain of first stage, $A_{i1} = -h_{fe} = -50$

Current gain of second-stage, $A_{i2} = \frac{h_{fe}}{1 + h_{fe}} = \frac{50}{1 + 50} = 0.98$

Overall current gain is $$A_{is} = \frac{I_o}{I_S} = \frac{I_o}{I_{c2}} \times \frac{I_{c2}}{I_{c2}} \times \frac{I_{e2}}{I_{c1}} \times \frac{I_{c1}}{I_{b1}} \times \frac{I_{b1}}{I_S}$$

where $$\frac{I_o}{I_{c2}} = -1, \frac{I_{c2}}{I_{c2}} = -A_{i2}, \frac{I_{e2}}{I_{c1}} = -1, \frac{I_{c1}}{I_{b1}} = -A_{i1}, \frac{I_{b2}}{I_S} = \frac{R_B}{R_B + R_{i1}}$$

and $$R_B = R_3 \parallel R_4 = 200 \times 10^3 \parallel 10 \times 10^3 = 9.5\ \text{k}\Omega$$

Therefore, $$A_{is} = -1 \times -A_{i2} \times -1 - A_{i1} \times \frac{R_B}{R_B + R_{i1}} = 43.9$$

*To find overall voltage gain*

Voltage gain of the first stage, $A_{V1} = \dfrac{A_{i1}\, R_{L1}}{R_{i1}}$

where $R_{L1} = R_{i2} = 21.56\ \Omega$

Therefore, $A_{V1} = \dfrac{-50 \times 21.56}{1.1 \times 10^3} = -0.98$

Voltage gain of the second-stage, $A_{V2} = \dfrac{A_{i2}\, R_{L2}}{R_{i2}} = \dfrac{0.98 \times 3 \times 10^3}{21.56} = 136.36$

Overall voltage gain is

$$A_V = A_{V1} \times A_{V2} = -0.98 \times 136.36 = -133.63$$

$$A_{Vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = A_V \times \frac{R_i}{R_i + R_s} = -66.35$$

*To find overall output resistance*

Output resistance of the first stage, $R_{o1} = \infty$

Output resistance of the second-stage, $R_{o2} = \infty$

Overall output resistance, $R_o = R_{o2} \parallel R_L = \infty \parallel 3 \times 10^3 = 3\ \text{k}\Omega$

## 2.9 DARLINGTON AMPLIFIER

A very popular connection of two bipolar junction transistors for operation as one "superbeta" transistor is the Darlington connection, which is shown in Fig. 2.29. The main feature of the Darlington connection is that the composite transistor acts as a single unit with a current gain that is the product of the current gains of the individual transistors. If the connection is made using two separate transistors having current gains of $\beta_1$ and $\beta_2$, the Darlington connection provides a current gain of

$$\beta_D = \beta_1 \beta_2$$

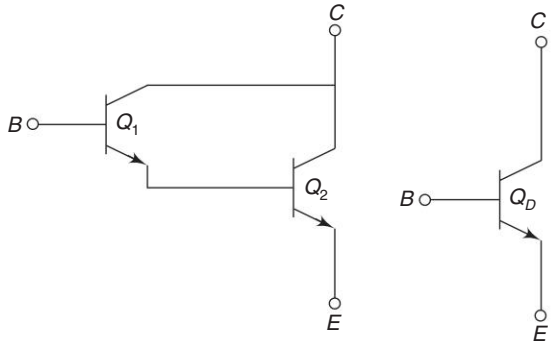



**Fig. 2.29** *(a) Darlington transistor connection (b) Single Darlington transistor*

If the two transistors are matched such that $\beta_1 = \beta_2 = \beta$, the Darlington connection provides a current gain of

$$\beta_D = \beta^2$$

When two transistors having high current gain are connected as a Darlington pair, the overall gain of the pair becomes very high.

For instance, let the current gain $\beta$ be 400. Then, the overall gain of the pair is 400 × 400 = 1,60,000. Darlington pairs are generally available in IC packages. The package has only three terminals, namely, base, emitter, and collector. In other words, it can be considered as a single Darlington transistor having very high current gain as compared to other typical single transistor. A Darlington transistor is commonly used in an emitter-follower circuit. This gives an equivalent circuit of two emitter followers in cascade, thereby increasing the input impedance.

***Biasing the Darlington Circuit*** In Fig. 2.30, a Darlington transistor having very high current gain $\beta_D$ is used. The base current is given by

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}$$

and the emitter current is given by

$$I_E = (\beta_D + 1)\, I_B \approx \beta_D I_B$$

The dc voltages are given by

$$V_E = I_E R_E$$

$$V_B = V_E + V_{BE}$$

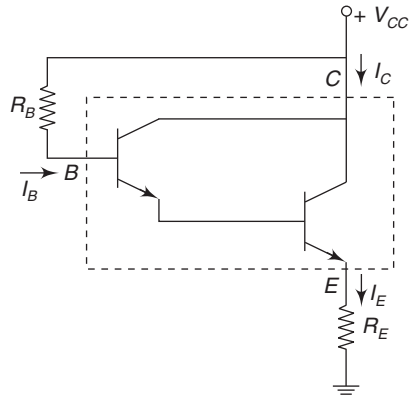



**Fig. 2.30** *Basic Darling bias circuit*

## 2.9.1 Darlington Composite Emitter Follower

For some applications, it is necessary to have an amplifier with high input impedance. Emitter follower may be used to have input resistances of about 500 kΩ. For achieving still higher input impedances, the Darlington connection shown in Fig. 2.30 is used. Darlington connection has two transistors forming a composite pair. The input resistance of the second transistor constitutes the emitter load for the first. The Darlington circuit consists of two cascaded emitter followers with infinite emitter resistance in the first stage, as shown in Fig. 2.31.

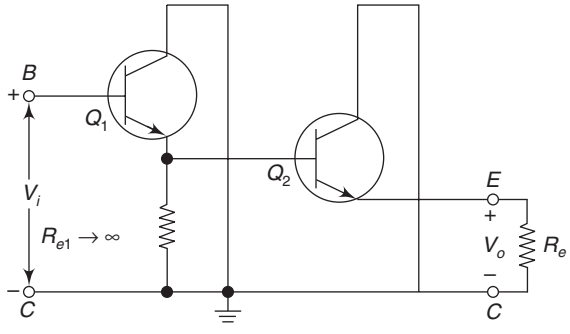



**Fig. 2.31** *Darlington circuit with two cascaded CC stages*

The Darlington composite emitter follower will be analyzed by referring to Fig. 2.32. Assume that $h_o R_e \leq 0.1$ and $h_{fe} R_e >> h_{ie}$.

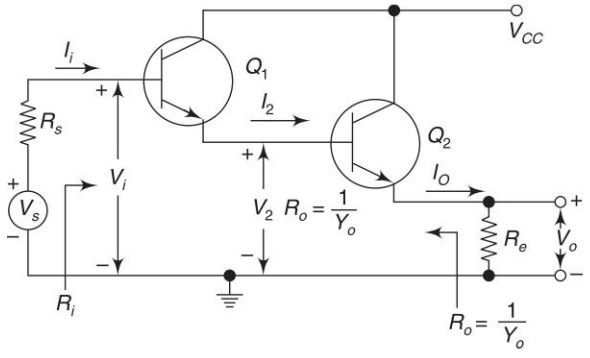



**Fig. 2.32** *Darlington composite emitter follower*

$$A_{I2} = \frac{I_o}{I_2} \approx 1 + h_{fe} \quad R_{i2} \approx (1 + h_{fe}) R_e$$

Since the effective load for transistor $Q_1$ is $R_{i2'}$ which does not meet the requirement $h_{oe} R_{i2} \leq 0.1$, the current gain of the first transistor becomes

$$A_{I1} = \frac{I_o}{I_2} = \frac{1 + h_{fe}}{1 + h_{oe} R_{i2}} = \frac{1 + h_{fe}}{1 + h_{oe} (1 + h_{fe}) R_e}$$

As $h_{oe} R_e \leq 0.1$, we get

$$A_{I1} \approx \frac{1 + h_{fe}}{h_{oe} h_{fe} R_e}$$

The overall current gain is

$$A_I = \frac{I_o}{I_i} = \frac{I_o}{I_2} \frac{I_2}{I_i} = A_{I2} A_{I1}$$

Therefore,

$$A_I = \frac{(1 + h_{fe})^2}{1 + h_{oe} h_{fe} R_e}$$

Similarly, the input resistance of $Q_1$ is

$$R_{iI} = h_{ie} + A_{I1} R_{i2} \approx \frac{(1 + h_{fe})^2 R_e}{1 + h_{oe} h_{fe} R_e}$$

This equation for the input resistance of the Darlington circuit is valid for $h_{oe} R_e \leq 0.1$.

The voltage gain of the Darlington circuit is close to unity, but its deviation from unity is slightly greater than that of the emitter follower. Then

$$1 - A_{V2} = 1 - \frac{h_{ie}}{R_{i1}} \approx \frac{h_{ie}}{A_{I1} R_{i2}}$$

where $A_{V2} = V_o/V_2$ and $A_{V1} = V_2/V_i$.

We know that, $A_V = V_o/V_i$

$$A_V = A_{V1}\,A_{V2} = \left[1 - \frac{h_{ie}}{R_{i2}}\right]\left[1 - \frac{h_{ie}}{A_{I1}\,R_{i2}}\right] \approx 1 - \frac{h_{ie}}{A_{I1}\,R_{i2}} - \frac{h_{ie}}{R_{i2}}$$

Since $A_{I1}R_{i2} >> R_{i2}$, the above equation becomes

$$A_V \approx 1 - \frac{h_{ie}}{R_{i2}}$$

This result indicates that the voltage gain of the Darlington circuit used as an emitter follower is essentially the same as the voltage gain of the emitter follower consisting of transistor $Q_2$ alone, but very slightly smaller.

The output resistance $R_{o1}$ of $Q_1$ is

$$R_{o1} = \frac{R_s + h_{ie}}{1 + h_{fe}}$$

Therefore, the output resistance of the $Q_2$ is

$$R_{o2} = \frac{\dfrac{R_s + h_{ie}}{1 + h_{fe}} + h_{ie}}{1 + h_{fe}} = \frac{R_s + h_{ie}}{(1 + h_{fe})^2} + \frac{h_{ie}}{1 + h_{fe}}$$

We can now conclude from the foregoing discussion that the Darlington emitter follower has higher current gain, a higher input resistance, a voltage gain less close to unity, and a lower output resistance than a single-stage emitter follower.

### *Practical Considerations*

In the Darlington pair, it is assumed that both the transistors $Q_1$ and $Q_2$ are identical, i.e., same value of *h*-parameters. In reality, this is usually not the case, because the *h*-parameters depend on the quiescent conditions of $Q_1$ and $Q_2$. Since the emitter current of $Q_1$ is the base current of $Q_2$, the quiescent current of the first stage is much smaller than that of the second-stage.

Hence, $h_{fe}$ may be much smaller for $Q_1$ than for $Q_2$ and $h_{ie}$ may be much larger for $Q_1$ than for $Q_2$. In order to have reasonable operating current in the first transistor $Q_1$, the second transistor $Q_2$ may have to be a power stage.

Another major drawback of the Darlington transistor pair is that the leakage current of the transistor $Q_1$ is amplified by the transistor $Q_2$, and hence, the overall leakage current may be high. For these two reasons, a Darlington connection of three or more transistors is usually impractical.

The composite transistor pair can be used as a common-emitter amplifier. The advantage of this pair is very high overall current gain, which is normally equal to the product of *CE* short-circuit current gains of the two transistors. In fact, Darlington integrated transistor pairs are commercially available with $h_{fe}$ as high as 30,000.

If $h_{oe}R_e << 1$ is not satisfied, an exact analysis of the Darlington circuit must be made. Using the *CC h*-parameters of each stage, the *h*-parameters of the composite pair are derived in terms of the *h*-parameters of $Q_1$ and $Q_2$, respectively.

## 2.9.2 Bootstrapped Emitter Follower

The main feature of a single-stage CC amplifier and two-stage CC amplifier (Darlington amplifier) is their high-input impedance. But this high input impedance is limited by the presence of biasing resistors $R_1$ and $R_2$. The input resistance $R_i$ of the emitter follower is given by $R_i \parallel R_1 \parallel R_2$.

To overcome the decrease in the input resistance due to the biasing resistors, the single-stage emitter follower circuit is modified by the addition of addition of a resistor $R_3$ and capacitor $C'$ between the emitter terminal and junction of $R_1$ and $R_2$. The bottom of $R_3$ is effectively connected to the output (the emitter) through $C'$, whereas the top of $R_3$ is at the input (the base). The modified circuit shown in Fig. 2.33 is called Bootstrapped emitter follower circuit. This capacitance $C'$ is chosen large enough to act as a short circuit even for the lowest frequency of operation. Thus, one end of $R_3$ is effectively connected to the input (base) and the other end to the output (emitter). Using Miller's theorem, the effective input resistance is found as

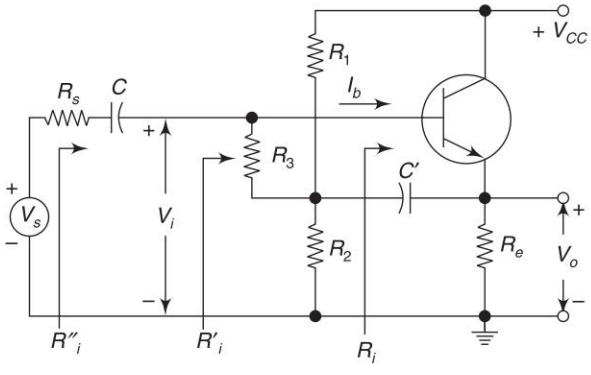



**Fig. 2.33** *Bootstrapped emitter follower*

$$R_{\text{eff}} = \frac{R_3}{1 - A_V}$$

where voltage gain $A_V$ is equal to $\dfrac{V_o}{V_i}$.

Since, for an emitter follower, $A_V$ is approximately equal to unity and $R_{\text{eff}}$ becomes extremely large. For example, with $A_V = 0.995$ and $R_3 = 100$ kΩ, we get $R_{\text{eff}} = 20$ MΩ. Hence, the high input resistance is maintained by the addition of resistor $R_3$.

The effect of increasing the input resistance when $A_V$ approaches unity is called *bootstrapping*. The term arises from the fact that, if one end of the resistor $R_3$ changes in voltage, the other end of $R_3$ moves through the same potential difference; it is as if $R_3$ were "pulling itself up by its bootstraps."

## 2.9.3 Bootstrapped Darlington Amplifier

In a Bootstrapped emitter-follower circuit, even after neglecting the effect of the resistors $R_1$, $R_2$ and $R_3$ and assuming infinite emitter resistance, the maximum input resistance is limited to $1/h_{ob} = 2$ MΩ. Since $1/h_{ob}$ is the resistance between base and collector, the input resistance can be greatly increased by bootstrapping the Darlington circuit through the addition of $C_o$ between the first transistor collector terminal $C_1$ and the second transistor emitter terminal $E_2$, as shown in Fig. 2.34(a). Note that the collector resistor $R_{c1}$ is essential because, without it, $R_{e2}$ would be shorted to ground. If the input signal changes by $V_i$, then $E_2$ changes by $A_V V_i$ and (assuming that the reactance of $C_0$ is negligible) the collector $C_1$ changes by the same amount. Hence $1/h_{ob}$ is now effectively increased to $(1/h_{ob})/(1 - A_V) = 400$ MΩ, for a voltage gain of 0.995.

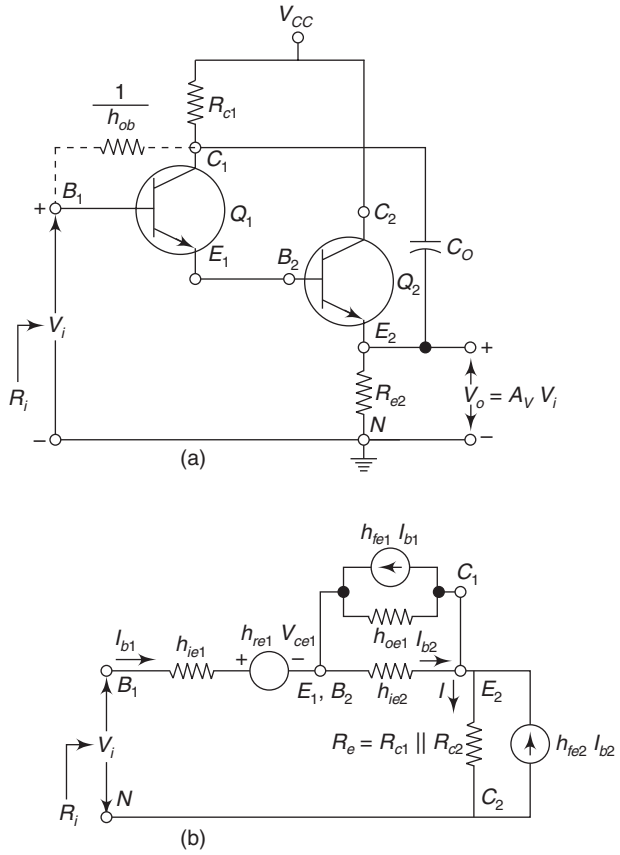



**Fig. 2.34** *(a) Bootstrapped Darlington circuit (b) Its equivalent circuit*

An expression for the input resistance $R_i$ of the bootstrapped Darlington pair can be obtained using the equivalent circuit of Fig. 2.34(b). The effective resistance $R_e$ between $E_2$ and ground is $R_e = Rc_1 \parallel R_{e2}$. If $h_{oe}R_e \leq 0.1$, then the transistor $Q_2$, may be replaced by the approximate $h$-parameter model. However, the exact hybrid model as indicated in Fig. 2.34(b) must be used for $Q_2$. Since $1/h_{oe1} >> h_{ie2}$, then $h_{oe1}$ may be neglected from this circuit and solving for $V_i/I_{b1}$ results in the input resistance of bootstrapped Darlington pair as

$$R_i = h_{fe1}h_{fe2}R_e$$

The above expression shows that the input resistance of the bootstrapped Darlington emitter follower is essentially equal to the product of the *short-circuit* current gains and the effective emitter resistance. If $h_{fe1} = h_{fe2} = 50$ and $R_e = 4$ kΩ, then $R_i = 10$ MΩ. If transistors with current gains of the order of magnitude of 100 instead of 50 were used, an input resistance of 40 MΩ would be obtained. If the biasing arrangement is considered for the bootstrapped pair shown in Fig. 2.34(a) then the input resistance, taking into account the bootstrapping both at the base and at the collector of $Q_1$, would be $R_{\text{eff}} \parallel h_{fe1}h_{fe2}R_e$, where $R_{\text{eff}}$ is given by

$$R_{\text{eff}} = \frac{R_3}{1 - A_V}.$$

## 2.10 DIFFERENTIAL AMPLIFIERS

The function of a differential amplifier is to amplify the difference between two signals. The need for a differential amplifier arises in many physical measurements where response from dc to many megahertz is required. Moreover, it is the basic input stage of an integrated amplifier.

Figure 2.35 shows the basic block diagram of a differential amplifier in which there are two input terminals and one output terminal.

The output signal in a differential amplifier is proportional to the difference between the two input signals.

$$V_o = A_d (V_1 - V_2) \qquad (2.29)$$

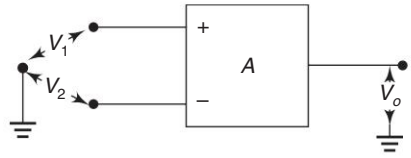



**Fig. 2.35** *Block diagram of a differential amplifier*

If $V_1 = V_2$, the output voltage is zero. A non-zero output voltage is obtained if $V_1$ and $V_2$ are not equal. The difference-mode input voltage is defined as $V_d = (V_1 - V_2)$ and the common-mode input voltage is defined as $V_{cm} = \dfrac{(V_1 + V_2)}{2}$.

These equations show that if $V_1 = V_2$, the differential-mode input signal is zero and common mode input signal is $V_{cm} = V_1 = V_2$. For example, if $V_1 = +20\ \mu V$ and $V_2 = -20\ \mu V$, then the differential mode voltage is $V_d = 40\ \mu V$ and the common voltage is $V_{cm} = 0$. However, if $V_1 = 120\ \mu V$ and $V_2 = 80\ \mu V$, then the differential-mode input signal is still $V_d = 40\ \mu V$, but the common mode input signal is $V_{cm} = 100\ \mu V$. For both the sets of input voltages, the output voltage of an ideal differential amplifier would be exactly the same. However, in practice, the common mode input signal will affect the output. In the design of differential amplifier, one goal is to minimize the effect of common mode input signal.

### 2.10.1 Differential Amplifier using Operational Amplifier

The basic differential amplifier is shown in Fig. 2.36(a). The amplifier has two input signals $V_1$ and $V_2$ and a single output $V_o$. For the purpose of signal analysis, they can be represented by its input resistance $R_{id}$, output resistance $R_o$, and controlled voltage source as shown in Fig. 2.36(b). Here, $A$ is the open-circuit voltage gain, $V_{id} = (V_1 - V_2)$ is the differential-mode input voltage.

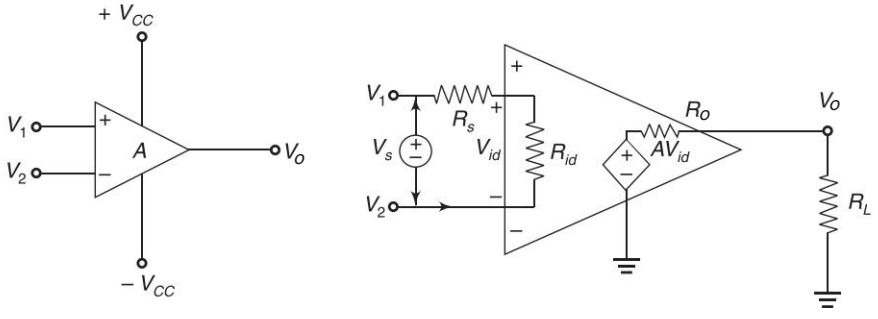



**Fig. 2.36** *(a) Schematic form of basic differential amplifier (b) For signal analysis*

The signal voltage developed at the output of the amplifier is in phase with the voltage applied to the positive input terminal and 180° out of phase with the signal applied to the negative input terminal. The $V_1$ and $V_2$

terminals are therefore referred to as non-inverting input and inverting input respectively. Hence, the output of the differential amplifier is written as

$$V_o \propto (V_1 - V_2)$$

i.e., $$V_o = A\,(V_1 - V_2)$$

From Fig. 2.36(b), the Thevenin resistance and output voltage are

$$R_{th} = \frac{R_L}{R_o + R_L}$$

$$V_o = AV_{id}\,\frac{R_L}{R_o + R_L} \tag{2.30}$$

and $$V_{id} = V_s\,\frac{R_{id}}{R_{id} + R_s}$$

$$V_o = AV_s\,\frac{R_{id}}{R_{id} + R_s}\,\frac{R_L}{R_o + R_L}$$

$$A_V = \frac{V_o}{V_s} = \frac{AR_{id}}{R_{id} + R_s}\,\frac{R_L}{R_o + R_L}$$

The operational amplifier circuits are dc-coupled amplifiers and the signals $V$ and $V_s$ may have a dc component that represents a dc shift of the input away from $Q$-point. The op-amp amplifies not only the ac components of the signal but also the dc component, and hence, the amplitude and phase of the signal determine $A_V$.

An ideal differential amplifier produces an output that depends purely on the voltage difference ($V_{id}$) between its two input terminals, and this voltage would be independent of the source and load resistance. Therefore,

$$\frac{R_L}{R_o + R_L} = 1 \quad \text{and} \quad \frac{R_{id}}{R_{id} + R_s} = 1$$

From Eq. (2.30), $$V_o = AV_{id}$$

Therefore, $$A_V = \frac{V_o}{V_{id}} = A_d$$

where $A_d$ is the *differential voltage gain.*

Therefore, $$V_o = A_V(V_1 - V_2)$$

Hence, if $V_1 = V_2$, the output voltage is zero; if $V_1$ and $V_2$ are not equal, a non-zero output voltage is obtained. However, a practical differential amplifier cannot be described by the above equation because the output voltage depends on the *average level* called *common-mode signal,* which is given by

$$V_c = \frac{V_1 + V_2}{2}$$

Considering the common mode alone, the output of the differential amplifier can be given as

$$V_o = A_c V_c$$

where $A_c$ is the *common mode gain.*

Hence, the total output of any differential amplifier can be given as

$$V_o = A_d V_{id} + A_c V_c \tag{2.31}$$

***Common Mode Rejection Ratio*** The differential amplifier is said to be operated in a common mode configuration when the same voltage is applied to both the inputs, i.e., $V_1 = V_2$. One of the main requirements of the differential amplifier is to cancel or reject the noise signal that appears as a common input signal to both the input terminals of the differential amplifier. Hence, a *figure of merit* called *Common-Mode Rejection Ratio* (*CMRR*) is introduced to define the ability of a differential amplifier to reject a common mode signal. CMRR is defined as the ratio of the differential voltage gain $A_d$ to common mode gain $A_c$ and is generally expressed in dB.

$$\text{CMRR} = 20 \log_{10} \left| \frac{A_d}{A_c} \right| \tag{2.32}$$

In ideal cases, since $A_c = 0$, CMRR = ∞ and in practical cases, since $A_d >> A_c$, CMRR is high, though finite. Therefore,

$$\begin{aligned} V_o &= A_d V_{id} + A_c V_c \\ &= A_d V_{id} \left[ 1 + \frac{A_c V_c}{A_d V_{id}} \right] \\ &= A_d V_{id} \left[ 1 + \frac{1}{(A_d / A_c)} \frac{V_c}{V_{id}} \right] \\ V_o &= A_d V_{id} \left[ 1 + \frac{1}{\text{CMRR}} \frac{V_c}{V_{id}} \right] \end{aligned} \tag{2.33}$$

where CMRR is not expressed in (dB). As CMRR approaches ∞, the output voltage becomes

$$V_o = A_d V_{id}$$

Here, the common mode voltage is nullified to a greater extent.

## 2.10.2 Differential Amplifiers Using BJT

The differential amplifiers using BJT are broadly classified into two types, namely, (i) differential BJT amplifier with resistive loading, and (ii) differential BJT amplifier with active loading.

***Differential BJT Amplifier with Resistive Load*** The emitter-coupled or source-coupled differential amplifier forms the input stage of most analog ICs. The emitter-coupled differential amplifier circuit is shown in Fig. 2.37. It is important to note that the performance of a differential amplifier depends on the ideal matching of the transistor pair, $Q_1$ and $Q_2$.

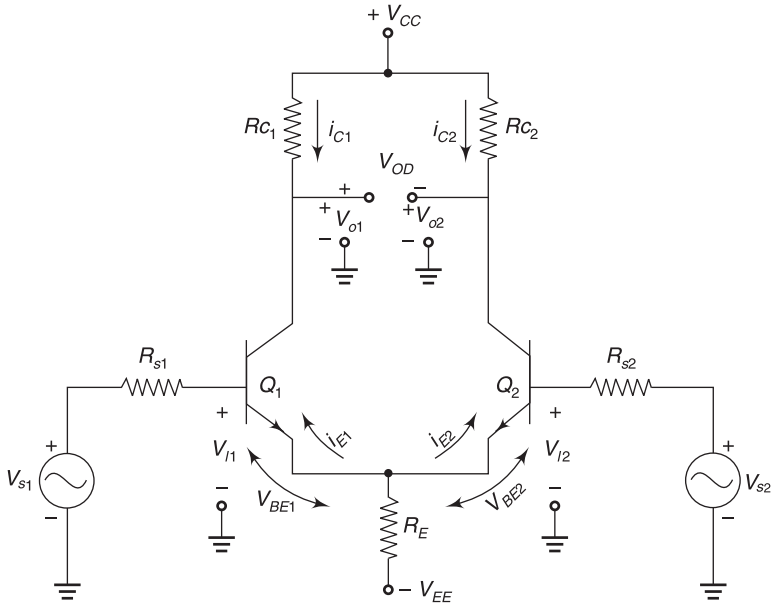



**Fig. 2.37** *Circuit diagram of emitter-coupled differential amplifier*

The amplifier uses both a positive power supply $+V_{CC}$ and a negative power supply $-V_{EE}$. Though in practical situations, the power supplies are equal in magnitude, it need not be the case always. It is to be mentioned that these amplifiers operate even at dc, because appropriate dc level shifting could be obtained without the use of coupling capacitors.

***dc Analysis of an Emitter-Coupled Pair*** The dc analysis begins with the assumption that $Q_1$ and $Q_2$ are ideally matched, and the mismatching effects will be considered later. Here, we consider $\beta >> 1$ so that

$$-i_{E1} \approx i_{C1} \quad \text{and} \quad -i_{E2} \approx i_{C2}$$

and hence,

$$V_{I1} = V_{BE1} - V_{BE2} + V_{I2}$$

In the dc analysis, the operating point values, i.e., $I_{CQ}$ and $V_{CEQ}$ can be obtained for $Q_1$ and $Q_2$. The dc equivalent circuit can be derived by making ac inputs zero as shown in Fig. 2.38.

For matched transistor pairs, we have

- since $R_{E1} = R_{E2}$, $R_E = R_{E1} \| R_{E2}$
- $R_{C1} = R_{C2} = R_C$
- $|V_{CC}| = |V_{EE}|$

For a symmetrical circuit with matched transistors, $I_{C1Q} = I_{C2Q}$ and $V_{CE1Q} = V_{CE2Q}$.

Hence, it is enough finding out the operating points $I_{CQ}$ and $V_{CEQ}$ for any one of the two transistors. Any symmetrical circuit as shown in Fig. 2.39 will be suitable for ac analysis.

Consider Fig. 2.38 for dc analysis. Applying KVL to base-emitter loop of $Q$, we get

$$I_B R_s + V_{BE} + 2I_E R_E = V_{EE}$$

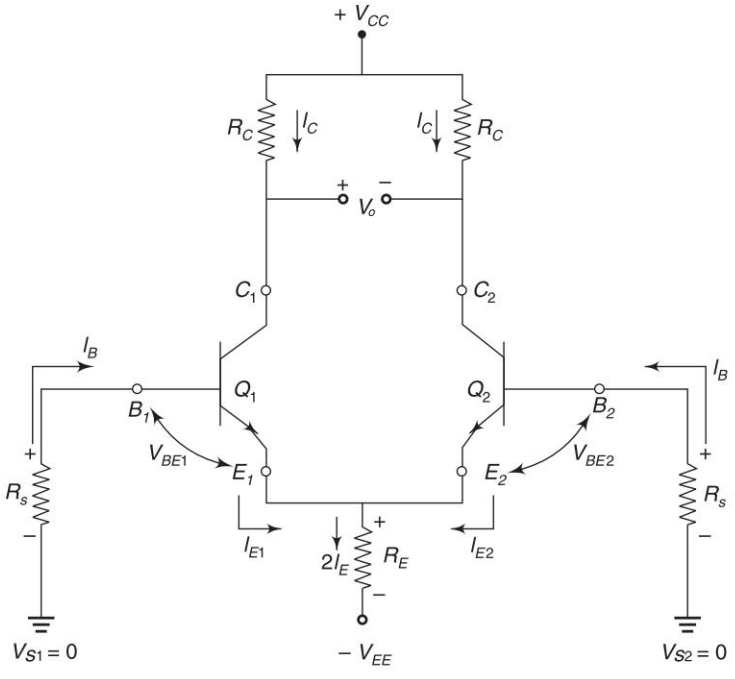



**Fig. 2.38** *dc equivalent circuit*

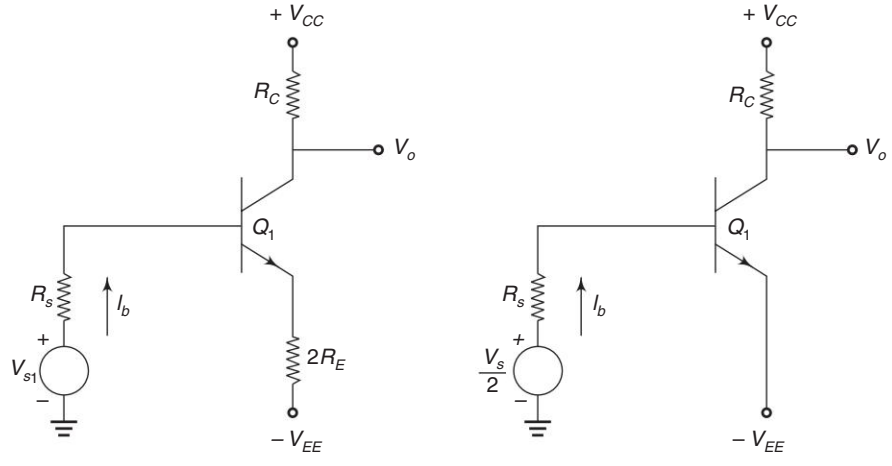



**Fig. 2.39** *Emitter-coupled pair for (a) $A_c$ analysis, and (b) $A_d$ analysis*

As $\beta = \dfrac{I_C}{I_B}$ for common emitter and $I_C \approx I_E, \beta = \dfrac{I_E}{I_B}$

Therefore,

$$\frac{I_E}{\beta} R_s + V_{BE} + 2I_E R_E = V_{EE}$$

$$I_E\left[\frac{R_s}{\beta}+2R_E\right]=V_{EE}-V_{BE}$$

$$I_E=\frac{V_{EE}-V_{BE}}{\left(\frac{R_s}{\beta}+2R_E\right)}$$

In practical conditions, $\frac{R_s}{\beta}\ll 2R_E$. Therefore,

$$I_E=\frac{V_{EE}-V_{BE}}{2R_E}$$

From the above equation, it can be inferred that

(i) for a known value of $V_{EE}$, the emitter current of $Q_1$ and $Q_2$ are determined by $R_E$, and
(ii) the emitter current $I_E$ is independent of $R_C$ when $I_E \approx I_C$.

Neglecting drop across $R_s$ and applying KVL to the collector-base loop, we get

$$V_C = V_{CC} - I_C R_C$$

and

$$\begin{aligned} V_{CE} &= V_C - V_E \\ &= V_{CC} - I_C R_C - V_E \end{aligned}$$

But $V_E = -V_{BE}$ (voltage at the emitter of $Q_1$). Thus

$$V_{CE} = V_{CC} - I_C R_C + V_{BE}$$

The above equation gives $V_{CEQ} = V_{CE}$ when $I_E \cong I_C = I_{CQ}$, for the given values of $V_{CC}$ and $V_{EE}$.

***The ac Analysis of an Emitter-Coupled Pair*** The differential gain $A_d$, common mode gain $A_c$, input, and output resistances $R_i$ and $R_o$ can be obtained using the $h$-parameter model.

**Differential Mode Gain ($A_d$)** For the analysis, let the two input signals have a magnitude of $V_s/2$ and differ from each other by 180° phase shift, as shown in Fig. 2.39(b). In Fig. 2.38, since $I_{E1} = I_{E2}$ and out of phase by 180°, they cancel each other. The ac equivalent circuit of Fig. 2.39(b) is shown in Fig. 9.83 and a similar structure may be realized for $Q_2$ also.

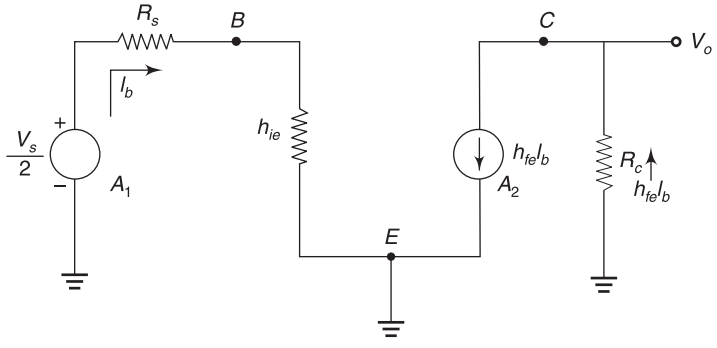



**Fig. 2.40** *Approximate hybrid model, neglecting $h_{oe}$*

Applying KVL to the loop $A_1$, the input loop

$$I_b(R_s + h_{ie}) = \frac{V_s}{2}$$

$$I_b = \frac{V_s}{2(R_s + h_{ie})}$$

Applying KVL to the loop $A_2$, the output voltage is

$$V_o = -h_{fe} I_b R_C$$

Therefore,

$$V_o = -h_{fe} R_C \frac{V_s}{2(R_s + h_{ie})}$$

$$\frac{V_o}{V_s} = \frac{-h_{fe} R_C}{2(R_s + h_{ie})} \tag{2.34}$$

It should be noted that the minus sign in Eq. (2.34) indicates 180° phase difference between input and output. As the magnitude of the input signals are equal, viz., $\left(\frac{V_s}{2}\right)$ and are out of phase by 180°, we have

$$V_{id} = V_1 - V_2 = \frac{V_s}{2} - \left(-\frac{V_s}{2}\right) = V_s$$

Therefore,

$$A_d = \frac{V_o}{V_{id}} = \frac{V_o}{V_s} = \frac{+h_{fe} R_C}{2(R_s + h_{ie})} \tag{2.35}$$

where $V_s$ is the differential input voltage.

When the output of a differential amplifier is measured with reference to the ground point, it is called *unbalanced output*. However, $A_d$ for a balanced case can be derived by considering the balanced output across the two collectors of $Q_1$ and $Q_2$, which are assumed to be perfectly matched. $A_d$ for such a condition is twice than that of $A_d$ obtained for a unbalanced output. Therefore,

$$A_d = \frac{2 h_{fe} R_C}{2(R_s + h_{ie})} = \frac{h_{fe} R_C}{(R_s + h_{ie})} \tag{2.36}$$

**Common-Mode Gain ($A_c$)** For common mode analysis, consider that the input signals are having the same magnitude $V_s$ and are in same phase. Therefore,

$$V_c = \frac{V_1 + V_2}{2} = \frac{V_s + V_s}{2} = V_s$$

We know that $V_o = A_c V_c$. Hence, $A_c = \frac{V_o}{V_s}$

Unlike the previous case, the emitter current is considered for the analysis. The current through $R_E$ is 2 $I_E$. The emitter resistance is assumed to be $2R_E$ and emitter current to be $I_E$ instead of $2I_E$ as shown in Fig. 2.39(a).

The appropriate hybrid model is shown in Fig. 2.41.

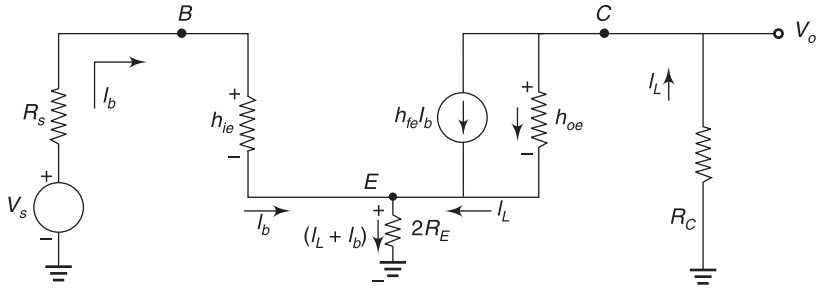



**Fig. 2.41** *Approximate hybrid model*

Current through $R_C = I_L$ (Load Current)

Effective emitter resistance = $2R_E$

Current through emitter resistance = $I_L + I_b$

Current through $h_{oe} = (I_L - h_{fe}I_b)$

Applying KVL to the input side,

$$I_bR_s + I_bh_{ie} + 2R_E(I_L + I_b) = V_s$$

Therefore, $$V_s = I_b(R_s + h_{ie} + 2R_E) + I_L(2R_E)$$

and $$V_o = -I_LR_C$$

As in dc analysis, let us now apply KVL to the output loop.

$$I_LR_C + 2R_E(I_L + I_b) + \frac{(I_L - h_{fe}I_b)}{h_{oe}} = 0$$

i.e., $$I_LR_C + 2R_EI_L + 2R_EI_b + \frac{I_L}{h_{oe}} - \frac{h_{fe}I_b}{h_{oe}} = 0$$

Therefore,

$$I_b\left[2R_E - \frac{h_{fe}}{h_{oe}}\right] + I_L\left[R_C + 2R_E + \frac{1}{h_{oe}}\right] = 0$$

i.e., $$I_L\left[R_C + 2R_E + \frac{1}{h_{oe}}\right] = -I_b\left[2R_E - \frac{h_{fe}}{h_{oe}}\right]$$

i.e.,
$$\frac{I_L}{I_b} = \frac{\left[\frac{h_{fe}}{h_{oe}} - 2R_E\right]}{\left[R_C + 2R_E + \frac{1}{h_{oe}}\right]}$$

$$\frac{I_L}{I_b} = \frac{h_{fe} - 2R_E h_{oe}}{1 + h_{oe}(2R_E + R_C)}$$

Therefore,

$$I_b = \frac{I_L[1 + h_{oe}(2R_E + R_C)]}{h_{fe} - 2R_E h_{oe}}$$

Substituting for $I_b$,

$$V_s = \frac{I_L[1 + h_{oe}(2R_E + R_C)](R_s + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + I_L(2R_E)$$

$$\frac{V_s}{I_L} = \frac{[1 + h_{oe}(2R_E + R_C)](R_s + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + 2R_E$$

i.e.,
$$= \frac{[1 + h_{oe}(2R_E + R_C)](R_s + h_{ie} + 2R_E) + 2R_E(h_{fe} - 2R_E h_{oe})}{(h_{fe} - 2R_E h_{oe}]}$$

Simplifying the above equation, we get

$$\frac{V_s}{I_L} = \frac{h_{oe} R_C[R_s + h_{ie} + 2R_E] + 2R_E(1 + h_{fe}) + R_s(1 + 2R_E h_{oe}) + h_{ie}(1 + 2R_E h_{oe})}{(h_{fe} - 2R_E h_{oe})}$$

Rearranging the last two terms in the numerator, we get

$$\frac{V_s}{I_L} = \frac{h_{oe} R_C[2R_E + R_s + h_{ie}] + 2R_E(1 + h_{fe}) + (R_s + h_{ie})(1 + 2R_E h_{oe})}{(h_{fe} - 2R_E h_{oe})}$$

In practical cases, $h_{oe} R_c << 1$.

$$\frac{V_s}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_s + h_{ie})(1 + 2R_E h_{oe})}{(h_{fe} - 2R_E h_{oe})}$$

Therefore,

$$A_c = \frac{V_o}{V_s} = \frac{-I_L R_C}{V_s}$$

$$= \frac{-(h_{fe} - 2R_E h_{oe})R_C}{2R_E(1 + h_{fe}) + (R_s + h_{ie})(1 + 2R_E h_{oe})}$$

$$= \frac{R_C(2R_E h_{oe} - h_{fe})}{2R_E(1 + h_{fe}) + (R_s + h_{ie})(1 + 2R_E h_{oe})}$$

As shown in Fig. 9.83, $h_{oe}$ is generally neglected in practical designs.

Therefore,

$$A_c = \frac{-R_C\, h_{fe}}{R_s + h_{ie} + 2\,R_E\,(1 + h_{fe})}$$

Hence, unlike $A_d$, $A_c$ is the same for both balanced and unbalanced outputs.

### *Common-Mode Rejection Ratio (CMRR)*

$$\text{CMRR} = 20 \log_{10} \left| \frac{A_d}{A_c} \right|$$

Substituting the results of $A_d$ and $A_c$, we get

$$\text{CMRR} = 20 \log_{10} \left| \frac{R_s + h_{ie} + 2\,R_E\,(1 + h_{fe})}{R_s + h_{ie}} \right| \text{(dB)} \quad \text{for balanced case.}$$

And,

$$\text{CMRR} = 20 \log_{10} \left| \frac{R_s + h_{ie} + 2\,R_E\,(1 + h_{fe})}{2\,(R_s + h_{ie})} \right| \text{(dB)} \quad \text{for unbalanced output.}$$

***Input Impedance ($R_i$) and Output Impedance ($R_o$)*** The input impedance, $R_i$, can be defined as the equivalent resistance existing between any one of the inputs and the ground when the other input is grounded. From Fig. 2.41,

$$R_i = \frac{V_s}{I_b}$$

From Fig. 2.41, for a single input

$$R_i = R_s + h_{ie}$$

$$R_i = 2\,(R_s + h_{ie})$$

which is common for both balanced and unbalanced output. Further, it can be seen that $R_o = R_c$.

***Differential BJT Amplifiers with Active Loading*** The term *active load* refers to the use of a current source in place of the resistor as a load in the amplifier configuration. The current source is a transistor circuit, as shown in Fig. 2.42, in which $R_1$, $R_2$, and $R_3$ can be adjusted to give the same quiescent conditions for transistors $Q_1$ and $Q_2$ as in the circuit of Fig. 2.38.

This circuit offers a very high effective emitter resistance $R_E$ for the two transistors $Q_1$ and $Q_2$. The transistor $Q_3$ can be analyzed to form a constant current source, subject to the condition that the base current of $Q_3$ is negligible.

Applying KVL to the base circuit of $Q_3$, we have

$$V_{BE3} + I_3 R_3 = V_D + (V_{EE} - V_D)\,\frac{R_2}{R_1 + R_2}$$

where $V_D$ is the diode-voltage drop.

Therefore,

$$I_o \approx I_3 = \frac{1}{R_3} \left[ \frac{V_{EE}\,R_2}{R_1 + R_2} - \frac{V_D\,R_2}{R_1 + R_2} + V_D - V_{BE3} \right]$$

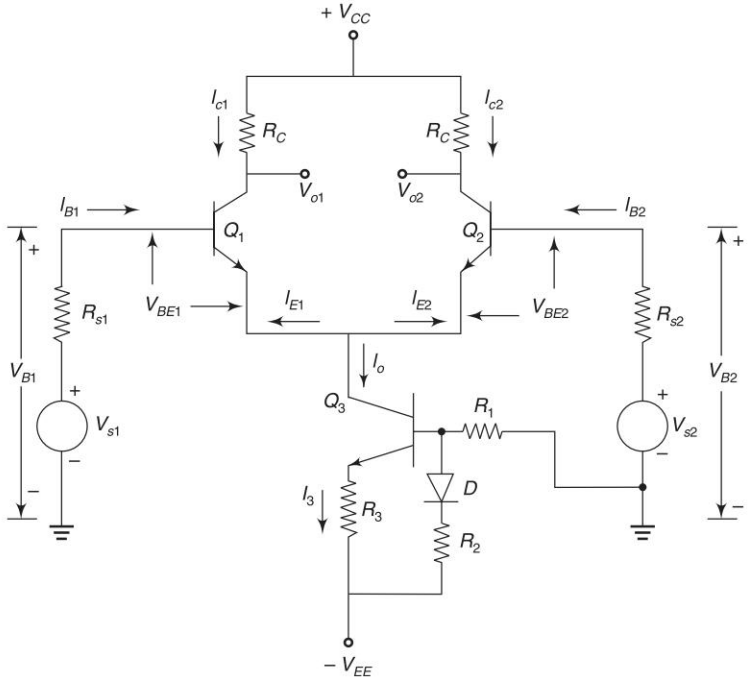



**Fig. 2.42** *Differential BJT amplifier with active loading*

$$= \frac{1}{R_3}\left[\frac{V_{EE}\,R_2}{R_1+R_2} - \frac{V_D\,R_1 + V_D\,R_2 - V_D\,R_2}{R_1+R_2} - V_{BE3}\right]$$

$$= \frac{1}{R_3}\left[\frac{V_{EE}\,R_2}{R_1+R_2} + \frac{V_D\,R_1}{R_1+R_2} - V_{BE3}\right]$$

If $R_1$, $R_2$, and $V_D$ are chosen so that $\dfrac{V_D\,R_1}{R_1+R_2} = V_{BE3}$, we have

$$I_o = \frac{1}{R_3}\left[\frac{V_{EE}\,R_2}{R_1+R_2}\right]$$

From the above equation, it can be inferred that $I_o$ is independent of the signal voltages $V_{s1}$ and $V_{s2}$. Hence, $Q_3$ acts to supply the differential amplifier consisting of $Q_1$ and $Q_2$ with a constant current $I_o$. Here, $I_o$ has been considered independent of temperature because of the presence of diode $D$. The diode has the same temperature dependence as that of $Q_3$ and hence, the two variations cancel out each other and $I_o$ is maintained independent of temperature. The cut-in voltage $V_D$ of the diode has approximately the same value as $V_{BE3}$ of $Q_3$. This being the case, the equation for $V_{BE3}$ cannot be satisfied with a single diode. Hence, two diodes in series are used for $V_D$ as shown in Fig. 2.43.

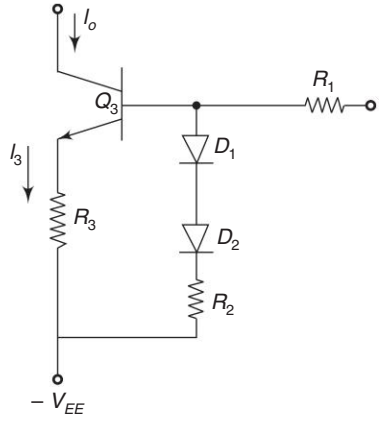



**Fig. 2.43** *Modified constant current source using two diodes*

So far it is assumed that the resistance does not vary with temperature $T$. If its negative temperature coefficient effect is taken into account, the above equation for $V_{BE3}$ is not satisfied. Hence, $R_1/(R_1 + R_2)$ is chosen such that $I_o$ is almost independent of $T$.

### *Practical Considerations to be Observed*

1. In certain applications, the assumption of $V_{s1}$ and $V_{s2}$ as the inputs are not realistic because of the effect of $R_{s1}$ and $R_{s2}$, which are the inherent resistances of the voltage sources $V_{s1}$ and $V_{s2}$ respectively. In such cases, the base-to-ground voltages $V_{B1}$ and $V_{B2}$ are considered as input voltages.
2. In general, the differential amplifier is used for dc applications. It is not so easy to design dc amplifiers using transistors because of drift due to variations of $h_{FE}$, $V_{BE}$, and $I_{CBO}$ with temperature. A shift in any of these quantities may change the output voltage which may not be distinguished from a change in the input signal voltage. If $Q_1$ and $Q_2$ are almost identical, then any parameter change due to temperature will get cancelled out and the output will not vary.
3. For high gain, the differential amplifiers may be cascaded to obtain larger amplification for difference signals. In this case, the outputs $V_{o1}$ and $V_{o2}$ are taken from the collector of $Q_1$ and $Q_2$ respectively as shown in Fig. 2.42 and are coupled directly to the two bases of the next stage.
4. The differential amplifier may also be used as an emitter coupled phase inverter. In this case, the signal is applied to one base, whereas the second base is not excited, but properly biased. The output voltages $V_{o1}$ and $V_{o2}$ are equal in magnitude and 180° out of phase.

## 2.10.3 Transfer Characteristics of a Differential Amplifier

Having analyzed the differential amplifier using BJT, its transfer characteristics could be examined to appreciate the advantages and comment on the limitations. A qualitative approach of Fig. 9.85 helps us to study the transfer characteristics of the same.

***Analysis*** When $V_{B1}$ is below the cut-off point of $Q_1$, all the current $I_o$ flows through $Q_2$ (under assumption that $V_{B2}$ is constant). As $V_{B1}$ increases above cut-off, the current in $Q_1$ increases, while the current in $Q_2$ decreases, and the sum of the currents in the two transistors remain constant which is equal to $I_o$. The total range $\Delta V_o$ over which the output can follow the input is $R_C I_o$ and is therefore, adjustable with $I_o$.

Applying KCL in Fig. 2.43, we have

$$I_{E1} + I_{E2} + I_o = 0$$

Applying KVL, we get

$$V_{B1} - V_{B2} = V_{BE1} - V_{BE2}$$

By *V-I* characteristics of a diode, the emitter current $I_E$ of each transistor is related to the voltage $V_{BE}$ as

$$I_E = I_o e^{(V_{BE}/\eta V_T)}$$

where $I_o$ is the diode reverse saturation current and $\eta = 1$ for silicon.

When $Q_1$ and $Q_2$ are matched, we have

$$I_{C1} \approx -I_{E1} = \frac{I_o}{1 + \exp[-(V_{B1} - V_{B2})/V_T]}$$

and

$$I_{C2} \approx -I_{E2} = \frac{I_o}{1 + \exp[-(V_{B2} - V_{B1})/V_T]}$$

Now, the transfer characteristics can be drawn for the normalized collector current $I_C/I_o$ with the normalized differential input $(V_{B1} - V_{B2})/V_T$ as shown in Fig. 2.44.

Differentiating the above equation for $I_{C1}$ with respect to $(V_{B1} - V_{B2})$, we get the transconductance $g_{md}$ of the differential amplifier with respect to the input differential voltage, or

$$\frac{dI_{C1}}{d(V_{B1} - V_{B2})} \approx g_{md} = \frac{I_o}{4V_T} \tag{2.37}$$

From the above equation, it is clear that for the same value of $I_o$, the effective transconductance of the differential amplifier is one-fourth of that of a single transistor.

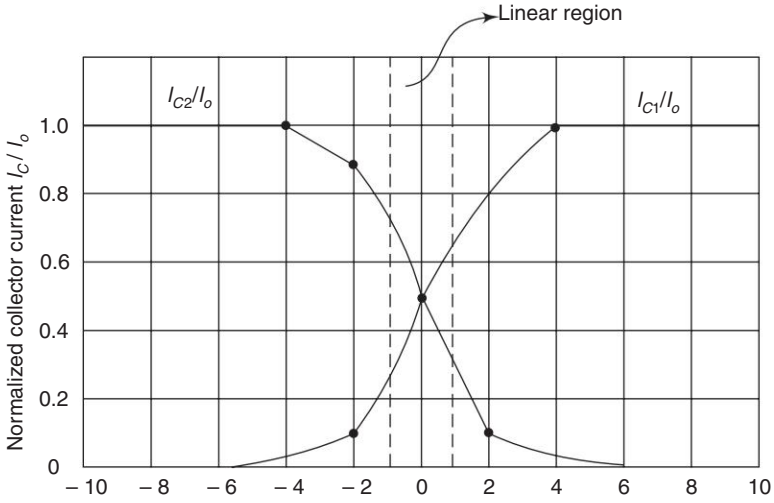



**Fig. 2.44** *Transfer characteristics of the basic transistor based differential amplifier circuit (when Q1 is identically equal to Q2)*

From Fig. 2.44, the following conclusions are made.

(i) The differential amplifier is a very good limiter. When the input $(V_{B1} - V_{B2})$ exceeds $\pm 4V_T$, the output becomes nearly a constant.

(ii) The slope of these curves ($I_{C2}/I_o$ and $I_{C1}/I_o$) defines the transconductance and from the graph, it can be seen that $g_{md}$ starts from zero, and reaches a maximum of $I_o/4\ V_T$ at $I_{C1} = I_{C2} = (1/2)\ I_o$ and again approaches zero.

(iii) The value of $g_{md}$ is proportional to $I_o$. The output voltage change $V_{o2}$ can be modelled as

$$V_{o2} = g_{md}\, R_C \Delta(V_{B1} - V_{B2}) = g_{md}\, R_C\, (V_{b1} - V_{b2})$$

Hence, it is possible to change the differential gain by varying the values of the current $I_o$. and Automatic Gain Control (AGC) is possible with the differential amplifier.

(iv) In the linear region, the transfer characteristics are linear around the operating points, where the input varies approximately by $\pm V_T$. At room temperature, this range is found to be ± 26 mV.

## EXAMPLE 2.8

A differential amplifier has (a) CMRR = 1000, and (b) CMRR = 10000. The first set of inputs is $V_1 = +100\ \mu V$ and $V_2 = -100\ \mu V$. The second set of inputs is $V_1 = 1100\ \mu V$ and $V_2 = 900\ \mu V$. Calculate the percentage difference in output voltage obtained for the two sets of input voltages and also comment on this.

**Solution** In the first set,

$$V_{id} = V_d = V_1 - V_2 = [100 - (-100)]\ \mu V = 200\ \mu V$$

$$V_c = \frac{1}{2}(V_1 + V_2) = \frac{1}{2}\ [100 + (-100)]\ \mu V = 0$$

$$V_o = A_d V_{id}\left[1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_{id}}\right]$$

$$= A_d \times 200\left[1 + \frac{1}{1000}\frac{0}{200}\right] = 200\ A_d\ \mu V \tag{2.38}$$

In the second set,

$$V_d = V_1 - V_2 = 1100\ \mu V - 900\ \mu V = 200\ \mu V$$

$$V_c = \frac{1}{2}(V_1 + V_2) = \frac{1}{2}(1100 + 900)\ \mu V = 1000\ \mu V$$

Hence,

$$V_o = A_d V_{id}\left[1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_{id}}\right] = A_d \times 200\left[1 + \frac{1}{1000}\frac{1000}{200}\right]$$

$$= A_d\,(201)\ \mu V \tag{2.39}$$

Comparing (9.102) and (9.103), the output voltages for the two sets of input signals result in a 0.5% difference.

Though the difference voltage $V_d = 200\ \mu V$ in both the cases, the output is not the same and hence the effect of common mode voltage $V_c$ has same influence in the output voltage and it decreases with increase in CMRR.

When CMRR = 10000, a similar analysis as that of case (a) gives

$$V_o = 200\ A_d\left(1 + \frac{1}{10{,}000}\frac{1000}{200}\right) = 200.1\ A_d\ \mu V$$

Here, the output voltages differ by 0.05%. Hence, as the CMRR increases, the difference between the output voltages decreases.

## EXAMPLE 2.9

Find the Q-point, $V_C$ and $I_B$ for the differential amplifier shown in Fig. 2.45.

**Solution** The emitter current can be found by writing a loop equation starting at the base of $Q_1$.

$V_{BE} + 2I_E R_E - V_{EE} = 0$. Here $\alpha_F = \dfrac{\beta_F}{1+\beta_F} = \dfrac{100}{101}$.

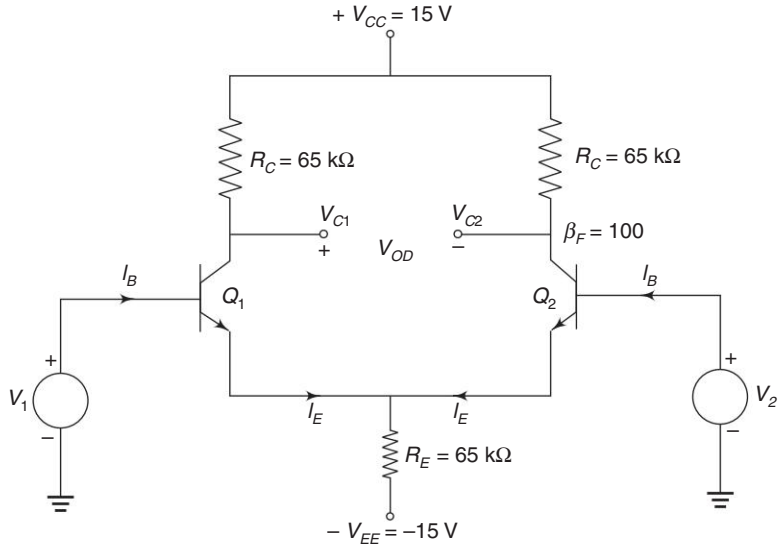



**Fig. 2.45**

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} = \frac{(15 - 0.7)}{2(65 \times 10^3)} = 110\ \mu\text{A}$$

$$I_C = \alpha_F I_E = \frac{100}{101} I_E = \frac{100}{101} \times 110 \times 10^{-6}\ \text{A} = 108.9\ \mu\text{A}$$

$$I_B = \frac{I_C}{\beta_F} = \frac{108.9 \times 10^{-6}\ \text{A}}{100} = 1.089\ \mu\text{A}$$

$$V_C = V_{CC} - I_C R_C$$

$$= 15 - (108.9 \times 10^{-6} \times 65 \times 10^3) = 7.922\ \text{V}$$

$$V_{CE} = V_C - V_E = 7.922 - (-0.7) = 8.622\ \text{V}$$

Both transistors of the differential amplifier are biased at a $Q$-point (108.9 μA, 8.622 V) with $I_B$ = 1.089 μA and $V_C$ = 7.922 V.

As $V_{EE} >> V_{BE}$, $I_E$ can be approximated by

$$I_E \approx \frac{V_{EE}}{2R_E} = \frac{15}{2 \times 65 \times 10^3} = 115.38\ \mu\text{A}$$

## EXAMPLE 2.10

Calculate the operating point values, differential gain, common-mode gain, CMRR, output if $V_{s1}$ = 60 mV (peak to peak) at 1 kHz and $V_{s2}$ = 40 mV (peak to peak) at 1 kHz for the differential amplifier shown in Fig. 2.46. Assume the transistor is made of silicon with $h_{ie}$ = 3.2 kΩ.

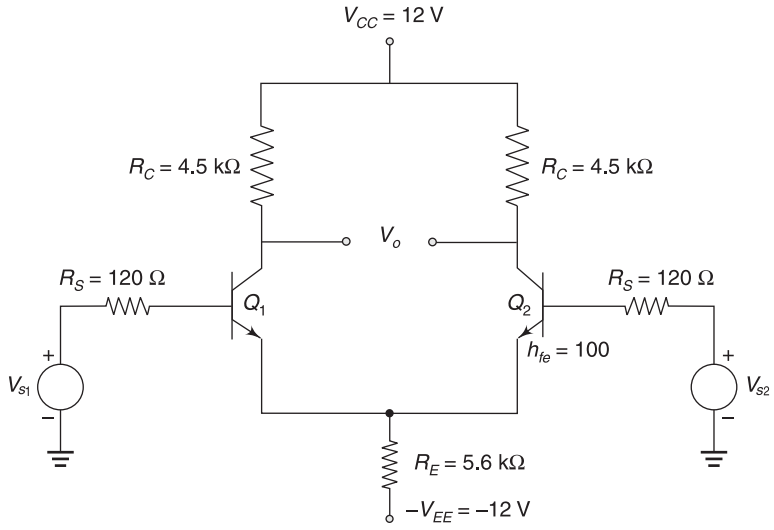



**Fig. 2.46**

**Solution**

$$\beta = h_{fe} = 100$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \dfrac{R_s}{\beta}} = \frac{12 - 0.7}{2 \times 5.6 \times 10^3 + \dfrac{120}{100}} = 1.009 \text{ mA}$$

$$I_C \approx I_E = 1.009 \text{ mA}$$

Therefore, $I_{CQ} = 1.009$ mA

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C = 12 + 0.7 - (1.009 \times 10^{-3} \times 4.5 \times 10^{-5}) = 8.16 \text{ V}$$

and $V_{CEQ} = 8.16$ V

The differential gain is

$$A_d = \frac{h_{fe} R_C}{R_S + h_{ie}} = \frac{100 \times 4.5 \times 10^3}{120 + 3.2 \times 10^3} = 135.54$$

Common-mode gain is

$$A_c = \frac{h_{fe} R_C}{2R_E (1 + h_{fe}) + R_s + h_{ie}}$$

$$= \frac{100 \times 4.5 \times 10^3}{2 \times 5.6 \times 10^3 (1 + 100) + 120 + 3.2 \times 10^3} = 0.3966$$

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{135.54}{0.3966} = 341.755$$

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_c} \right| = 50.674 \text{ dB}$$

The output voltage is $V_o = A_d V_d + A_c V_c$.

Here, $A_d = V_{s1} - V_{s2} = 60 \times 10^{-3} - 40 \times 10^{-3} = 20 \text{ mV } (p - p)$

Then, $V_c = \dfrac{V_{s1} + V_{s2}}{2} = \dfrac{60 \times 10^{-3} + 40 \times 10^{-3}}{2} = 50 \text{ mV } (p - p)$

Therefore,

$$V_o = 135.54 \times 20 \times 10^{-3} + 0.3966 \times 50 \times 10^{-3} = 2.73 \text{ V } (p - p)$$

## EXAMPLE 2.11

In the circuit shown in Fig. 2.47(a), the transistor has $h_{ie}$ = 400 Ω, $h_{re}$ = 2.1 × $10^{-4}$, $h_{fe}$ = 40, and $h_{oe} = 25 \times 10^{-6}$. Calculate $R_i$, $R_L'$, $A_V$, $A_{Vs}$, $R_o$.

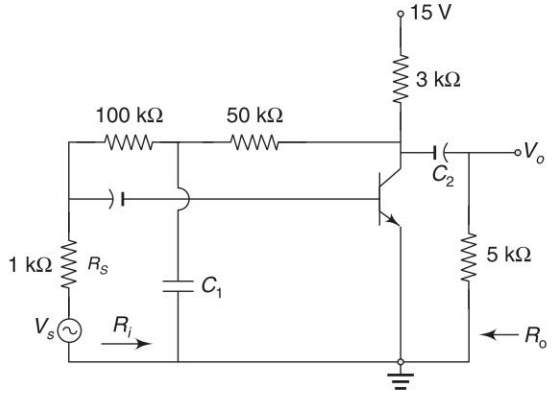



**Fig. 2.47 (a)**

**Solution** In this circuit,

$$R_L' = h_{oe}(R_L \| R_C) = 25 \times 10^{-6} \times (5 \text{ k}\Omega \parallel 3 \text{ k}\Omega) = 0.047 \text{ }\Omega$$

Here, $R_L'$ is less than 0.1 Ω. So, the *h*-parameter equivalent circuit is used to analyze the given circuit. It is obtained by replacing all capacitors and the dc source with short circuits and replacing the transistor with its *h*-parameter equivalent circuit shown in Fig. 2.47(b).

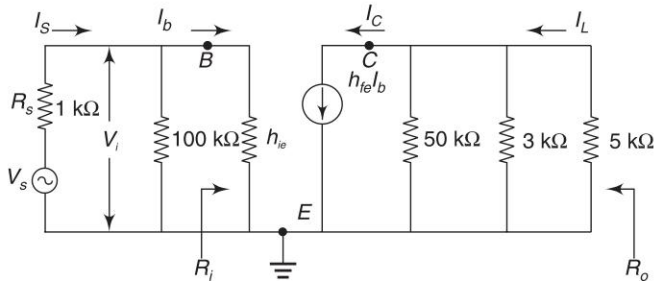



**Fig. 2.47(b)**

Input resistance, $R_i = h_{ie} \parallel 100\text{ k} = 400 \parallel 100\text{ k} = 398.4\ \Omega$

Output resistance, $R_o = 50\text{ k} \parallel 3\text{ k} \parallel 5\text{ k} = 1807.2\ \Omega$

$$\frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s}$$

$$\frac{V_o}{V_i} = \frac{-h_{fe} R'_L}{h_{ie}}$$

Therefore, $$A_V = \frac{V_o}{V_i} \frac{-h_{fe}(R_o)}{h_{ie}} = \frac{-40 \times 1807.2}{400} = -180.72$$

In the equivalent circuit,

$$V_i = \frac{V_s R_i}{R_i + R_s}$$

$$\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s} = \frac{398.4}{398.4 + (1 \times 10^3)} = 0.2849$$

Hence, $$A_{Vs} = \frac{V_o}{V_s} = \frac{V_o V_i}{V_i V_s} = -180.72 \times 0.2849 = -51.48$$

## REVIEW QUESTIONS

1. Draw the ac equivalent circuit of a CE amplifier with bypassed and unbypassed emitter resistor $R_E$ using hybrid-$\pi$ model and derive the expressions for input impedance, output impedance, voltage gain, and current gain.
2. Draw the ac equivalent circuit of a CB amplifier using hybrid-$\pi$ model and derive the expressions for input impedance, output impedance, voltage gain, and current gain.
3. Draw the ac equivalent circuit of a CC amplifier using hybrid-$\pi$ model and derive the expressions for input impedance, output impedance, voltage gain, and current gain.
4. Discuss briefly the choice of transistor configuration in a cascade amplifier.
5. Draw the equivalent circuit of *RC* coupled amplifier in the mid frequency range, high-frequency range, and low-frequency range and derive the equations for current gain, voltage gain, upper 3 dB frequency, and lower 3 dB frequency.
6. A CE–*RC* coupled amplifier uses transistors with the following *h*-parameters: $h_{fe} = 50$, $h_{ie} = 1100\ \Omega$, $h_{oe} = 10 \times 10^{-6}$ mhos, $h_{re} = 2.5 \times 10^{-4}$. The value of $g_m$ at the operating point is 200 mmhos. The biasing resistor $R_1$ and $R_2$ may be neglected being large in comparison with $R_i$. The load resistor $R_C = 5\ \text{k}\Omega$. Let the total shunt capacitance $C = 200\ \mu\text{F}$ in the input circuit and the coupling capacitor $C_C = 7\ \mu\text{F}$. Calculate for one stage of the amplifier (i) mid band current gain, (ii) mid-band voltage gain, (iii) lower and higher 3 dB frequencies, and (iv) gain-bandwidth product.

   [*Ans*. (i) –40.6 (ii) –40.6 (iii) 3.88 MHz and 3.18 MHz (iv) 129.29 MHz]
7. A CE–*RC* coupled amplifier uses transistors with the following *h*-parameters: $h_{ie} = 1200\ \Omega$, $h_{oe} = 25 \times 10^{-6}$ mhos. The biasing resistor $R_1$ between $V_{CC}$ and base is 100 kΩ and the resistor $R_2$ between base and ground is 10 kΩ. The load resistor is $R_C = 2000\ \Omega$. What should be the minimum value of coupling capacitor $C_C$ in order to have lower 3 dB frequency $f_L$ not exceeding 10 Hz? [*Ans.* 5.38 μF]
8. What is a Darlington transistor? What are its salient features?

**9.** Draw a biasing circuit of Darlington emitter follower circuit and derive expressions for voltage gain, current gain, input impedance and output impedance.

**10.** Explain the bootstrapping principle in emitter follower circuit and Darlington amplifier.

**11.** Explain how the number of stages in a multistage amplifier influences the cut-off frequency and bandwidth.

**12.** Draw the cascode amplifier circuit and derive expressions for voltage gain, current gain, input impedance, and output impedance.

**13.** The cascode amplifier shown in Fig. 2.26 makes use of identical transistors $Q_1$ and $Q_2$ with the following $h$-parameters: $h_{fe} = 100$, $h_{ie} = 1.1$ kΩ, $h_{oe} = 5 \times 10^{-6}$ mhos, $h_{re} = 2 \times 10^{-4}$. The circuit parameters are $R_s = 1$ kΩ, $R_3 = 100$ kΩ, $R_4 = 10$ kΩ and $R_L = 2$ kΩ. Calculate the overall current gain, voltage gain, input and output resistances.

**14.** What is a differential amplifier?

**15.** What are common-mode and differential-mode inputs in a differential amplifier?

**16.** Define differential gain, common-mode gain, and CMRR. Derive the relationship between them.

**17.** Draw the circuit diagram of an emitter-coupled BJT differential amplifier and derive expressions for differential gain, common-mode gain, CMRR, input impedance, and output impedance.

**18.** What is meant by active loading? How is it effective in differential amplifiers.

CHAPTER

# 3

# Single Stage FET, MOSFET Amplifiers

## 3.1 INTRODUCTION

The small-signal models for the common source FET can be used for analyzing the three basic FET amplifier configurations: (i) Common source (CS), (ii) Common drain (CD) or *source-follower*, and (iii) Common gate (CG). The CS amplifier which provides good voltage amplification is most frequently used. The CD amplifier with high input impedance and near-unity voltage gain is used as a buffer amplifier and the CG amplifier is used as a high-frequency amplifier. The small-signal current-source model for the FET in CS configuration is redrawn in Fig. 3.1(a) and the voltage-source model shown in Fig. 3.1(b) can be derived by finding the Thevenin's equivalent for the output part of Fig. 3.1(a). $\mu$, $r_d$ and $g_m$ are the amplification factor, drain resistance, and mutual conductance of the FET.

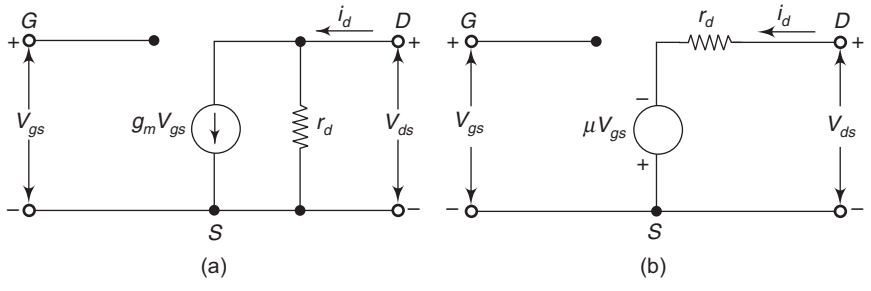



**Fig. 3.1** *(a) Small-signal current-source model for FET in CS configuration (b) Voltage-source model for FET in CS configuration*

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain with the added feature of high input impedance. They have low power consumption with a good frequency range, and minimal size and weight. The noise output level is low. This feature makes them very useful in the amplifier circuits meant for very small-signal amplifications. JFETs, depletion MOSFETs and enhancement MOSFETs are used in the design of amplifiers having comparable voltage gains. However, the depletion MOSFET circuit realizes much higher input impedance than the equivalent JFET configuration. Because of the high input impedance characteristic

of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. The common-source configuration is the most popular one, providing an inverted and amplified signal. However, one also finds the common drain (source follower) circuits providing unity gain with no inversion and common gate circuits providing gain with no inversion. Due to very high input impedance, the input current is generally assumed to be negligible, and it is of the order of few microamperes and the current gain is an undefined quantity. Output impedance values are comparable for both the BJT and FET circuits.

In this chapter, small signal analysis of MOSFET amplifier with common source, common drain and common gate configurations, and by CMOS circuits are also discussed

## 3.2 SMALL SIGNAL ANALYSIS OF CS AMPLIFIER

A simple common-source amplifier is shown in Fig.3.2(a), and the associated small-signal equivalent circuit using the voltage-source model of FET is shown in Fig. 3.2(b).

***Voltage Gain*** Source resistor ($R_s$) is used to set the $Q$-point but is bypassed by $C_S$ for mid-frequency operation. From the small-signal equivalent circuit, the output voltage,

$$V_o = \frac{-R_D}{R_D + r_d}\,\mu V_{gs} \tag{3.1}$$

where $V_{gs} = V_i$, the input voltage.

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d} \tag{3.2}$$

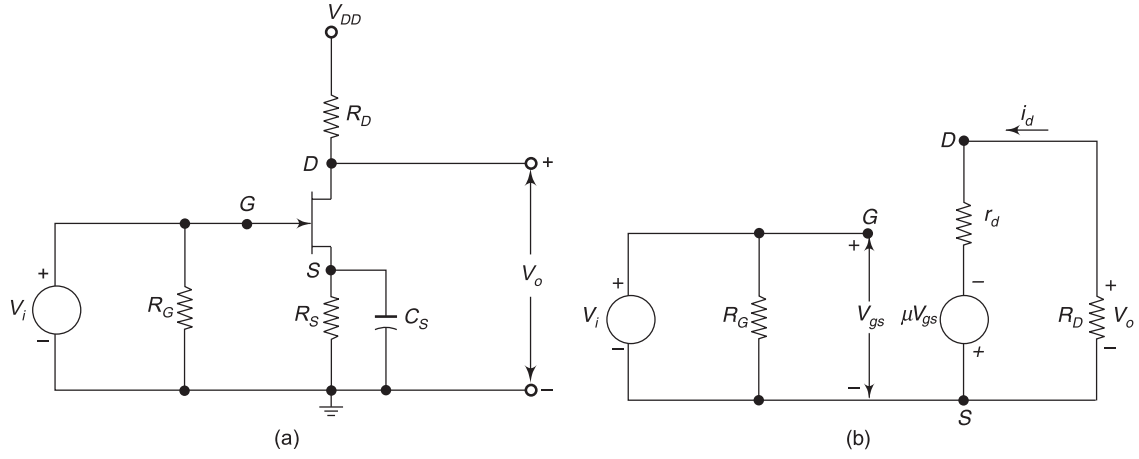



**Fig. 3.2** *(a) Common source amplifier (b) Small-signal equivalent circuit of CS amplifier*

***Input Impedance*** From Fig. 3.2(b), the input impedance is given by

$$Z_i = R_G$$

For voltage divider bias as in *CE* amplifiers of BJT,

$$R_G = R_1 \parallel R_2$$

***Output Impedance*** Output impedance is the impedance measured at the output terminals with the input voltage $V_i = 0$.

From Fig. 3.2(b), when $V_i = 0$, $V_{gs} = 0$ and hence,

$$\mu V_{gs} = 0$$

Then the equivalent circuit for calculating output impedance is given in Fig. 3.2 (c).

Output impedance $Z_o = r_d \parallel R_D$

Normally, $r_d$ will be far greater than $R_D$.

Hence, $Z_o \approx R_D$

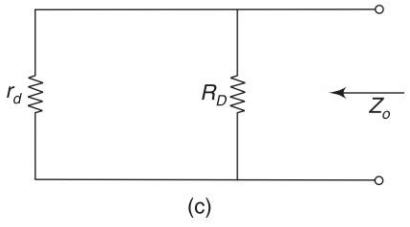



**Fig. 3.2** *(c) Calculation of output impedance*

## EXAMPLE 3.1

In the CS amplifier of Fig. 3.2(a), let $R_D = 5$ kΩ, $R_G = 10$ MΩ, μ = 50, and $r_d = 35$ kΩ. Evaluate the voltage gain $A_V$, input impedance $Z_i$, and output impedance $Z_o$.

**Solution** The voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d}$$

$$= \frac{-50 \times 5 \times 10^3}{5 \times 10^3 + 35 \times 10^3}$$

$$= \frac{-250 \times 10^3}{40 \times 10^3} = -6.25$$

The minus sign indicates a 180° phase shift between $V_i$ and $V_o$.

Input impedance $Z_i = R_G = 10$ MΩ

Output impedance $Z_o \approx R_D = 5$ kΩ

## EXAMPLE 3.2

A FET amplifier in the common-source configuration uses a load resistance of 500 kΩ. The ac drain resistance of the device is 100 kΩ and the transconductance is 0.8 $mAV^{-1}$. Calculate the voltage gain of the amplifier.

**Solution**

Given load resistance, $R_L = R_D = 500$ kΩ, $r_d = 100$ kΩ, $g_m = 0.8$ $mAV^{-1}$

The transconductance $\mu = g_m r_d = 0.8 \times 10^{-3} \times 100 \times 10^3 = 80$

The voltage gain, $A_V = -\frac{\mu R_D}{R_D + r_d} = \frac{-80 \times 500 \times 10^3}{500 \times 10^3 + 100 \times 10^3} = -\frac{40 \times 10^6}{600 \times 10^3} = -66.67$

## 3.3 SMALL SIGNAL ANALYSIS OF CD AMPLIFIER

A simple common-drain amplifier is shown in Fig. 3.3(a) and the associated small-signal equivalent circuit using the voltage-source model of FET is shown in Fig. 3.3(b). Since voltage $V_{gd}$ is more easily determined than $V_{gs}$, the voltage source in the output circuit is expressed in terms of $V_{gd}$ using Thevenin's theorem. The output voltage,

$$V_o = \frac{R_S}{R_S + \dfrac{r_d}{\mu + 1}} \times \frac{\mu}{\mu + 1} V_{gd} = \frac{\mu R_S V_{gd}}{(\mu + 1) R_S + r_d} \tag{3.3}$$

where $V_{gd} = V_i$, the input voltage.

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_S}{(\mu + 1) R_S + r_d} \tag{3.4}$$

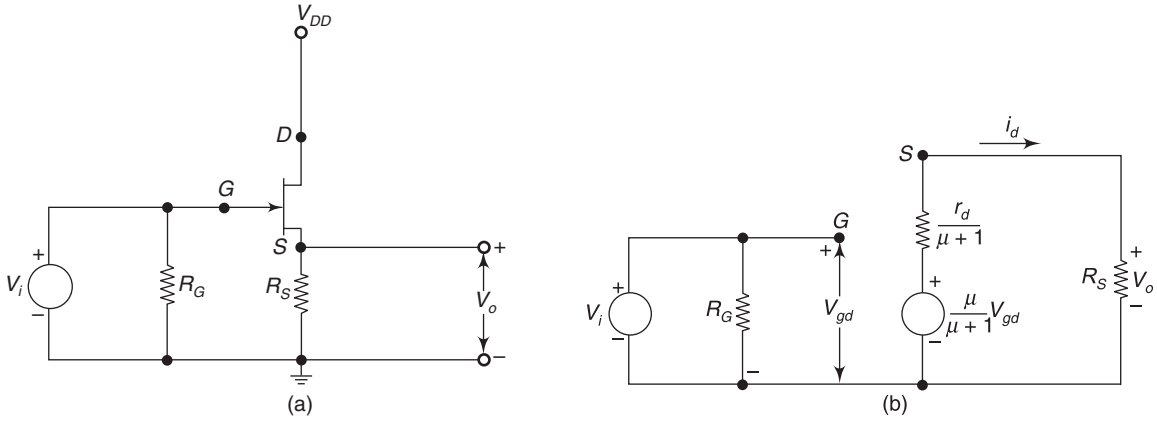



**Fig. 3.3** *(a) Common drain amplifier (b) Small-signal equivalent circuit of a CD amplifier*

***Input Impedance*** From Fig. 3.3(b), input impedance $Z_i = R_G$

***Output Impedance*** From Fig. 3.3(b), output impedance measured at the output terminals with input voltage $V_i = 0$ can be simply calculated from the following equivalent circuit.

As $V_i = 0$, $V_{gd} = 0$; $\dfrac{\mu}{\mu + 1} V_{gd} = 0$

Output impedance $Z_o = \dfrac{r_d}{\mu + 1} \| R_S$

when $\mu >> 1$ (typical value of $\mu = 50$)

$$Z_o \approx \frac{r_d}{\mu} \| R_S = \frac{1}{g_m} \| R_S$$

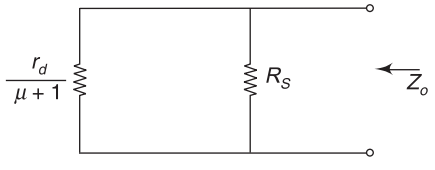



**Fig. 3.3** *(c) Calculation of output impedance*

## EXAMPLE 3.3

In the CD amplifier of Fig. 3.3(b), let $R_s = 4\ \text{k}\Omega$, $R_G = 10\ \text{M}\Omega$, $\mu = 50$, and $r_d = 35\ \text{k}\Omega$. Evaluate the voltage gain $A_V$, input impedance $Z_i$ and output impedance $Z_o$.

**Solution** The voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_S}{(\mu + 1) R_S + r_d}$$

$$= \frac{50 \times 4 \times 10^3}{(50 + 1) \times 4 \times 10^3 + 35 \times 10^3} = 0.836$$

The positive value indicates that $V_o$ and $V_i$ are in-phase and further note that $A_V < 1$ for CD amplifier.

Input impedance $Z_i = R_G = 10\ \text{M}\Omega$

Output impedance $Z_o = \frac{1}{g_m} \| R_S$

$$= \left(\frac{r_d}{\mu}\right) \| R_S$$

$$Z_o = \frac{35 \times 10^3}{50} \| 4 \times 10^3 = 595.7\ \Omega$$

## 3.4 SMALL SIGNAL ANALYSIS OF CG AMPLIFIER

A simple common-gate amplifier is shown in Fig. 3.4(a) and the associated small-signal equivalent circuit using the current-source model of FET is shown in Fig. 3.4(b).

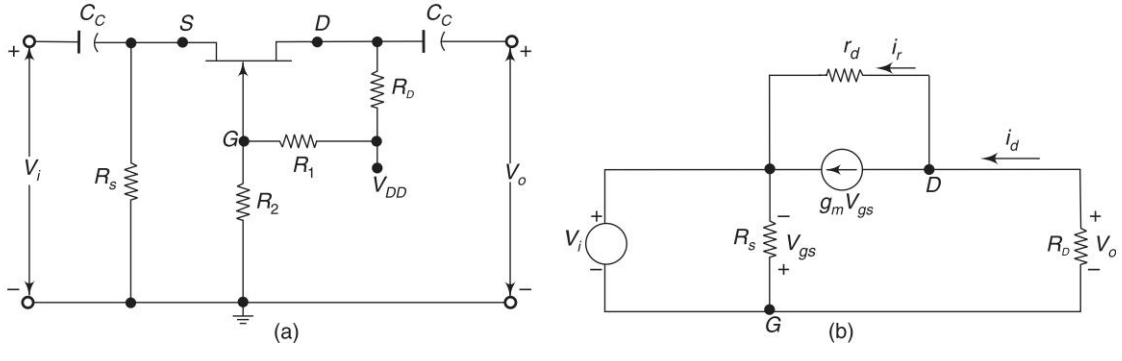



**Fig. 3.4** *(a) Common-gate amplifier (b) Small-signal equivalent circuit of a CG amplifier*

***Voltage Gain*** From the small-signal equivalent circuit by applying KCL, $i_r = i_d - g_m V_{gs}$. Applying KVL around the outer loop gives

$$V_o = (i_d - g_m V_{gs})\, r_d - V_{gs}$$

But $V_i = -V_{gs}$ and $i_d = \dfrac{-V_o}{R_D}$

Thus, $V_o = \left(\dfrac{-V_o}{R_D} + g_m V_i\right) r_d + V_i$

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{(g_m r_d + 1) R_D}{R_D + r_d} \tag{3.5}$$

***Input Impedance*** Figure 3.4(b) is modified for calculation of input impedance as shown in Fig. 3.4(c).

Current through $r_d$ is given by

$$I_{rd} = -I_r = I_1 + g_m V_{gs}$$

$$I_1 = I_{rd} - g_m V_{gs}$$

where $$I_{rd} = \frac{V_i - V_o}{r_d}$$

$$= \frac{V_i - I_{RD} R_D}{r_d}$$

Hence, $$I_1 = \frac{V_i - I_{RD} R_D}{r_d} - g_m V_{gs}$$

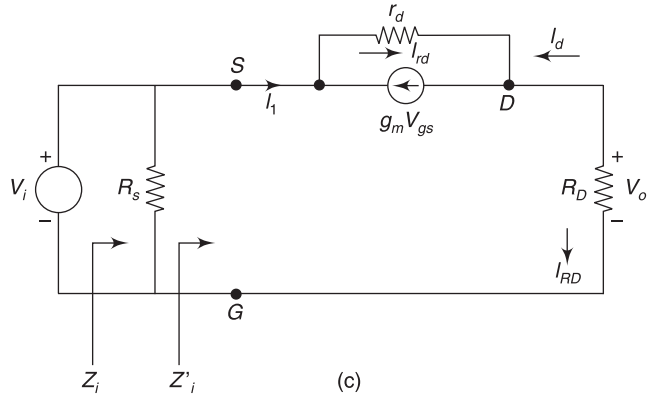



**Fig. 3.4** *(c) Modified equivalent circuit*

From Fig. 3.4(c),

$$V_i = -V_{gs}$$

$$I_1 = \frac{V_i - I_{RD} R_D}{r_d} + g_m V_i$$

$$= \frac{V_i}{r_d} - \frac{I_{RD} R_D}{r_d} + g_m V_i$$

$$I_1 + \frac{I_{RD} R_D}{r_d} = \frac{V_i}{r_d} + g_m V_i$$

From Fig. 3.4(c),

$$I_1 = I_{RD}$$

Therefore, $$I_1 \left[\frac{r_d + R_D}{r_d}\right] = V_i \left[\frac{1}{r_d} + g_m\right]$$

$$\frac{V_i}{I_1} = \frac{r_d + R_D}{1 + g_m r_d} = Z_i'$$

From Fig. 3.4(c),

$$Z_i = R_s \parallel Z_i'$$

$$= R_s \| \frac{r_d + R_D}{1 + g_m r_d}$$

In practice, $r_d >> R_D$ and $g_m r_d >> 1$.

Therefore, $$Z_i = R_s \| \frac{r_d}{g_m r_d}$$

or $$Z_i = R_s \| \frac{1}{g_m}$$

***Output Impedance*** It is the impedance seen from the output, terminals with input short-circuited.

From Fig. 3.4(c), when $V_i = 0$, $V_{sg} = 0$, the resultant equivalent circuit is shown in Fig. 3.4(d).

$$Z_o = r_d \| R_D$$

as $$r_d >> R_D$$

$$Z_o \approx R_D$$

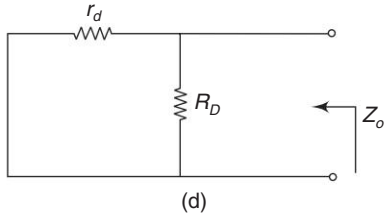



**Fig. 3.4** *(d) Equivalent circuit for output impedance*

## EXAMPLE 3.4

In the CG amplifier of Fig. 3.4(b), let $R_D = 2$ kΩ, $R_s = 1$ kΩ, $g_m = 1.43 \times 10^{-3}$ mho, and $r_d = 35$ kΩ. Evaluate the voltage gain $A_V$, input impedance $Z_i$, and output impedance $Z_o$.

**Solution** The voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{(g_m r_d + 1) R_D}{R_D + r_d} = \frac{(1.43 \times 10^{-3} \times 35 \times 10^3 + 1)\, 2 \times 10^3}{2 \times 10^3 + 35 \times 10^3} = 2.75$$

Input impedance, $$Z_i = R_s \| \frac{1}{g_m} = 1 \times 10^3 \| \frac{10^3}{1.4} = 0.41 \text{ kΩ}$$

Output impedance, $$Z_o \approx R_D = 2 \text{ kΩ}$$

## 3.5 FET SMALL-SIGNAL MODEL

From the drain and transfer characteristics of the field effect transistor, the drain current of an FET is a function of drain-to-source voltage ($v_{DS}$) and gate-to-source voltage ($v_{GS}$). The linear small-signal equivalent circuit for FET can be drawn analogous to the BJT.

Assuming varying currents and voltages for an FET,

$$i_D = f\,(v_{GS,}\, v_{DS}) \tag{3.6}$$

If both gate and drain voltages are varied, the change in drain current is given approximately by first two terms in the Taylor's series expansion of Eq. (3.6)

$$\Delta i_D = \left(\frac{\partial_{i_D}}{\partial v_{GS}}\right)_{V_{DS}} \Delta V_{GS} + \left(\frac{\partial_{i_D}}{\partial v_{DS}}\right)_{V_{GS}} \Delta v_{DS} \tag{3.7}$$

In small-signal notation, as for BJT,

$$\Delta i_D = i_d,\ \Delta v_{GS} = v_{gs} \text{ and } \Delta v_{DS} = v_{ds}$$

so that Eq. (3.7) can be written as

$$i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds} \tag{3.8}$$

where mutual conductance or transconductance of the FET is defined as

$$g_m = \left(\frac{\partial i_D}{\partial v_{GS}}\right)_{V_{DS}} \approx \left(\frac{\Delta i_D}{\Delta v_{GS}}\right)_{V_{DS}} = \left(\frac{i_d}{v_{gs}}\right)_{V_{DS}} \tag{3.9}$$

and drain (or output) resistance of the FET is defined as

$$r_d = \left(\frac{\partial v_{DS}}{\partial i_D}\right)_{V_{GS}} \approx \left(\frac{\Delta v_{DS}}{\Delta i_D}\right)_{V_{GS}} = \left(\frac{v_{ds}}{i_d}\right)_{V_{GS}} \tag{3.10}$$

The reciprocal of $r_d$ is the drain conductance $g_d$.

An amplification factor $\mu$ for an FET may be defined as

$$\mu = \left(-\frac{\partial v_{DS}}{\partial v_{GS}}\right)_{I_D} \approx \left(-\frac{\Delta v_{DS}}{\Delta v_{GS}}\right)_{I_D} = \left(-\frac{v_{ds}}{v_{gs}}\right)_{i_d = 0} \tag{3.11}$$

From Eq. (3.8) by setting $i_d = 0$, it can be verified that $\mu$, $r_d$ and $g_m$ are related by

$$\mu = g_m r_d \tag{3.12}$$

A small-signal model for FET in common-source configuration can be drawn by satisfying Eq. (3.8) as shown in Fig. 3.5.

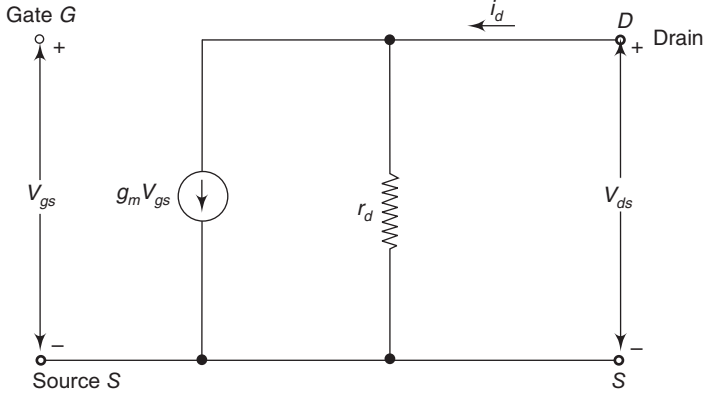



**Fig. 3.5** *Small-signal model for FET in CS configuration*

This low-frequency model for FET has a Norton's output circuit with a dependent current generator whose magnitude is proportional to the gate-to-source voltage. The proportionality factor is the transconductance '$g_m$'. The output resistance is $r_d$. The input resistance between the gate and source is infinite, since it is assumed that the reverse-biased gate draws no current. For the same reason, the resistance between gate and drain is assumed to be infinite.

### 3.5.1 Comparison of FET Model with *h*-Parameter Model of BJT

The *h*-parameter model of a BJT in CE configuration is redrawn in Fig. 3.6 for comparison.

Comparing circuits of Figs 3.6 and 3.6, the BJT also has a Norton's output circuit, but the current generated depends on the input current and not on the input voltage as in FET. There is no feedback from output to input in the FET, whereas a feedback exists in the BJT through the parameter $h_{re}$. The high (almost infinite) input resistance of the FET is replaced by an input resistance of about 1 kΩ for a CE amplifier.

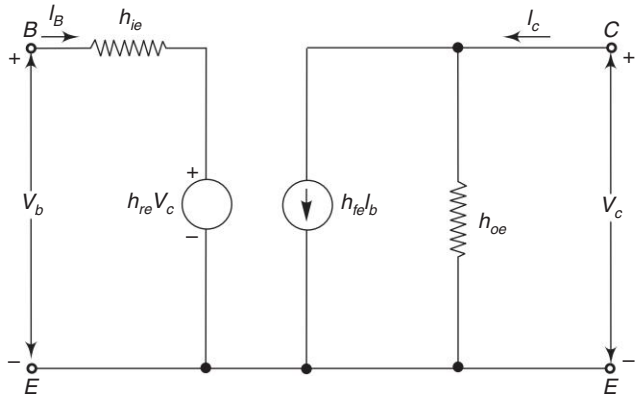



**Fig. 3.6** *h-parameter model of BJT in CE configuration*

Due to the high input impedance and the absence of feedback from output to input, FET is a much more ideal amplifier than the BJT at low frequencies. This becomes invalid beyond the audio range as the low frequency model of FET shown in Fig. 3.5 is not valid in the high frequency range.

### 3.5.2 High-Frequency Model of FET taking the Various Capacitors into Account

The high-frequency model of an FET is shown in Fig. 3.7.

This high-frequency model is identical with the low-frequency model except that the capacitances between the various terminals (gate, source, and drain) have been added. The capacitor $C_{gs}$ represents the barrier capacitance between the gate and source and $C_{gd}$ represents the barrier capacitance between the gate and drain. The capacitor $C_{ds}$ is the drain-to-source capacitance of the channel. Because of these internal capacitances, feedback exists between the output and input circuits of the FET and the voltage amplification drops drastically with increase in frequency.

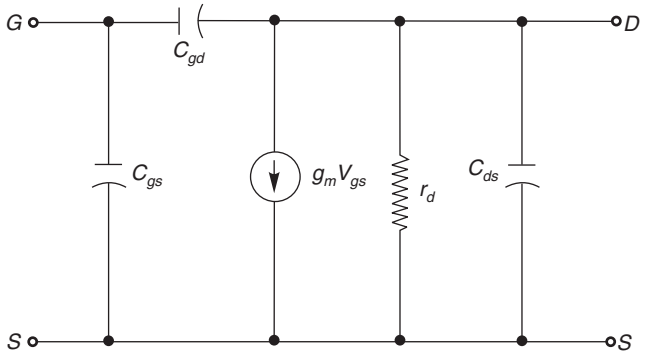



**Fig. 3.7** *High-frequency model of FET*

## 3.6 SMALL SIGNAL ANALYSIS OF MOSFET AMPLIFIER

The ac equivalent circuit for the NMOS amplifier circuit can be developed from small signal equivalent circuit for the transistor

We assume that the signal frequency is sufficiently low so that any capacitance at the gate terminal can be neglected. The input to the gate thus appears as an open circuit, or an infinite resistance. Equation (3.13) relates the small signal drain current to the small signal input voltage, and the transconductance $g_m$ is a function of the $Q$ point. The resulting simplified small signal equivalent circuit for the NMOS device is shown in Fig. 3.8.

$$i_d = g_m v_{gs} \tag{3.13}$$

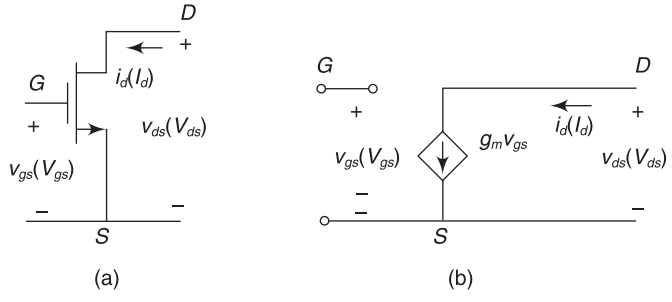



**Fig. 3.8** *(a) Common source NMOS transistor with small signal parameters (b) Simplified small signal equivalent circuit for NMOS Transistor*

This finite output resistance of a MOSFET biased in the saturation region, as a result of the non zero slope in the $i_D$ versus $v_{DS}$ curve, can also be included in small signal equivalent circuit.
We know that

$$i_D = K_N[(v_{GS-V_{TN}})^2(1 + \lambda v_{DS})] \tag{3.14}$$

where $\lambda$ is the channel length modulation parameter and is a positive quantity, The small signal output resistance, as previously defined, is

$$r_d = \left( \frac{\partial i_D}{\partial v_{DS}} \right)^{-1} \Bigg|_{v_{GS} = V_{GSQ} = \text{Const.}}$$

$$r_d = [\lambda K_N (V_{GSQ} - V_{TN})]^{-1} \cong [\lambda I_{DQ}]^{-1}$$

This small signal output resistance is also a function of the $Q$ point parameters.

The expanded small signal equivalent circuit of the $N$ channel MOSFET is shown in Fig. 3.9. This equivalent circuit is that of a transconductance amplifier in that the input signal is a voltage and output signal is a current. This equivalent circuit is inserted into the amplifier ac equivalent circuit in Fig. 3.8 to produce the circuit in Fig. 3.10.

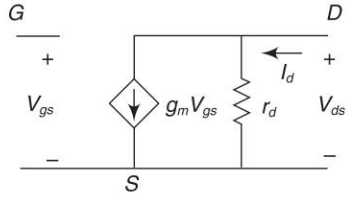



**Fig. 3.9** *Expanded small signal Equivalent circuit, including output resistance for NMOS Transistor*

From Fig 3.10, the voltage gain $A_V = \dfrac{V_o}{V_i} = -g_m (r_d \parallel R_D)$

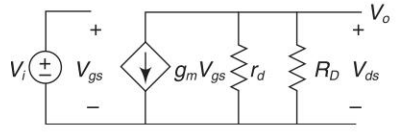



**Fig. 3.10** *Small Signal equivalent circuit of common source circuit with NMOS transistor model*

## 3.6.1 MOSFET AC Analysis

For linear amplifiers, superposition applies, so that dc and ac analyses can be done separately. The analysis of the MOSFET Amplifier proceeds as follows:

1. Analyze the circuit with only the dc sources present. This solution is the dc or quiescent solution. The transistor must be biased in the saturation region in order to produce a linear amplifier
2. Replace each element in the circuit with its small signal model, which means replacing the transistor by its small signal equivalent circuit
3. Analyse the small signal equivalent circuit setting dc source components equal to zero, to produce the response of the circuit to the time varying input

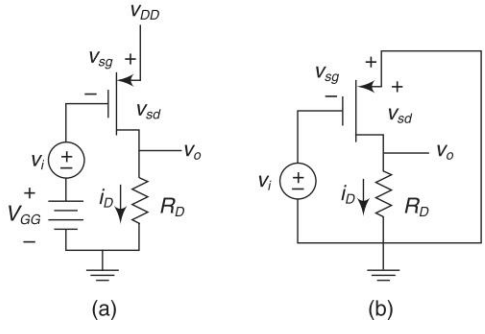



**Fig. 3.11** *(a) Common Source circuit with PMOS transistor and (b) corresponding ac equivalent circuit.*

The previous discussion was for an $N$ channel MOSFET amplifier. The same basic analysis and equivalent circuit also applies to the $P$-channel device. Figure 3.11(a) shows a circuit containing a $P$ channel MOSFET. Note that the power supply voltage $V_{DD}$ is connected to the source. Also note the change in current directions and voltage polarities compared to the circuit containing the NMOS transistor. Figure 9.65(b) shows the ac equivalent circuit with the dc voltage sources replaced by ac short circuits, all currents and voltages shown are the time varying components.

The circuit of Fig. 3.12 for $P$ channel MOSFET is the same as that of the $N$ channel device, except that all current directions and voltage polarities are reversed.

The final small signal equivalent circuit of the $P$ channel MOSFET amplifier is shown in Fig. 3.13.

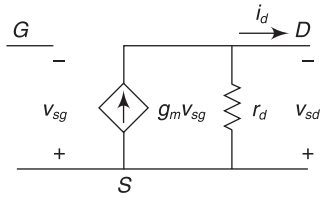



**Fig 3.12** *Small Signal equivalent circuit of PMOS Transistor*

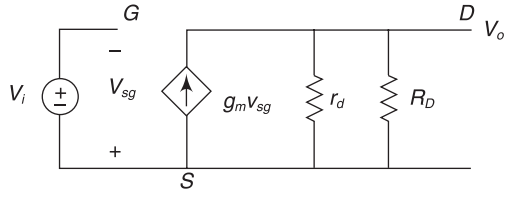



**Fig. 3.13** *Small signal equivalent circuit of common source amplifier with PMOS transistor model*

The output voltage is

$$V_o = g_m V_{sg}(r_d \| R_D)$$

The control voltage $V_{sg}$, given in terms of the input signal voltage, is

$$V_{sg} = -V_i$$

And the small signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

This expression for the small signal voltage gain of the *P* channel MOSFET amplifier is exactly the same as that for the *N* channel MOSFET amplifier. The negative sign indicates that a 180 degree phase reversal between the output and input signals, for both PMOS and NMOS circuits.

If the polarity of voltage and current in the small signal equivalent circuit of the PMOS device is made exactly identical to that of the NMOS device, the equivalent circuit is the same as that of the NMOS transistor as shown in Fig 3.14.

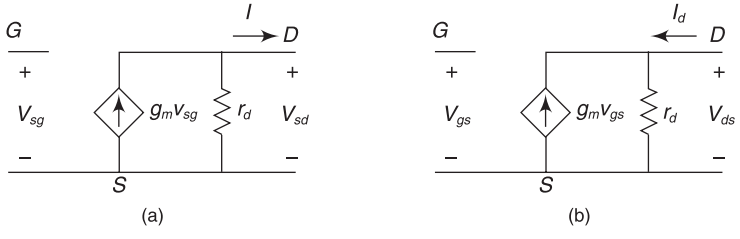



**Fig. 3.14** *Small signal equivalent circuit of a P-Channel MOSFET showing (a) the conventional voltage polarities and current directions and (b) the case when the voltage polarities and current directions are reversed.*

## 3.7 SMALL SIGNAL ANALYSIS OF DEPLETION MOSFET (D-MOSFET) AMPLIFIER

The small signal analysis of Depletion MOSFET amplifier is exactly the same as that of the JFET amplifier analysis because Shockley's equation is also applicable to Depletion MOSFET resulting in the same equation for $g_m$. The ac equivalent circuit model for D-MOSFET is also the same as that used for JFET as shown in Fig. 3.5. The only difference is that $V_{GSQ}$ is positive for *N*-channel and negative for *P*-channel in Depletion MOSFET, as compared to JFET.

## 3.8 SMALL SIGNAL ANALYSIS OF CS ENHANCEMENT MOSFET (E-MOSFET) AMPLIFIER

Figure 3.15 shows the ac small signal equivalent circuit model of *N*-channel and *P*-channel enhancement MOSFET. Here, there is an open circuit between gate and drain source channel and also a current source $g_m V_g$ from drain to source dependent on the gate source voltage.

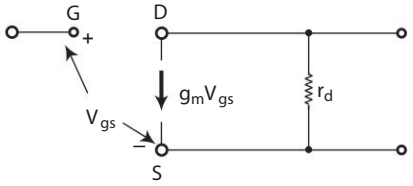



**Fig. 3.15** *Equivalent circuit model of Enhancement MOSFET*

### 3.8.1 Common Source E-MOSFET Amplifier

The common source *N*-channel E-MOSFET amplifier with voltage divider bias configuration is shown in Fig. 3.16. Assume that the MOSFET is biased in the saturation region by bias resistors $R_1$ and $R_2$. The signal frequency is considered to be high in order to make the coupling capacitor to act as a short circuit.

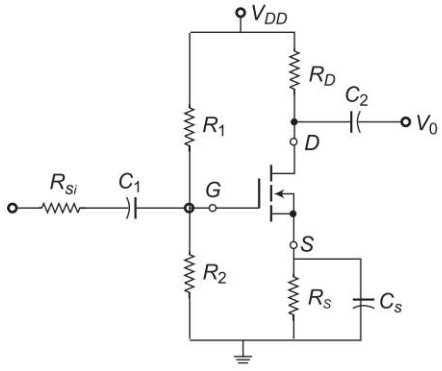



**Fig. 3.16** *Common source E-MOSFET amplifier*

Figure 3.17 shows the small signal equivalent circuit of common source amplifier with voltage divider bias configuration. Since the source is at ground potential, there is no body effect.

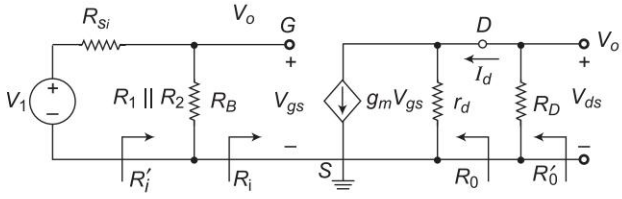



**Fig. 3.17** *Small signal equivalent circuit of common source amplifier*

***Input Resistance*** The input resistance $R_i$ looking into the gate of the E-MOSFET amplifier is infinite i.e., $R_i = \infty$. Hence, the overall input resistance by considering the bias resistors $R_1$ and $R_2$ is

$$R_i' = R_i \parallel R_B \approx R_1 \parallel R_2$$

***Voltage Gain*** The output voltage is given by

$$V_o = I_0(r_d \parallel R_D) = -I_d(r_d \parallel R_D) = -g_m V_{gs}(r_d \parallel R_D)$$

where $r_d$ is the internal drain resistance and $R_D$ is the load resistance. Using voltage divider rule, the input gate to source voltage is

$$V_{gs} = \left(\frac{R_i'}{R_{Si} + R_i'}\right) \cdot V_i$$

where $R_{Si}$ is the input signal source resistance. The small signal voltage gain ($A_V$) is the ratio of output voltage ($V_o$) to input voltage ($V_i$) as given by

$$A_V = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \parallel R_D) R_i'}{V_{gs}(R_{Si} + R_i')} = -g_m(r_d \parallel R_D)\left(\frac{R_i'}{R_{Si} + R_i'}\right)$$

***Output Resistance*** The output resistance, by looking into the output terminals without considering the load resistance ($R_D$) is

$$R_o = r_d$$

With load resistance, the output resistance becomes $R_o' = R_o \parallel R_D = r_d \parallel R_D$.

## EXAMPLE 3.5

For the common source E-MOSFET amplifier shown in Fig. 3.16, $R_{Si}$ = 0, $R_1$ = 520 kΩ, $R_2$ = 320 kΩ, $R_S$ = 5 kΩ, $R_D$ = 10 kΩ, $g_m$ = 0.442 mA/V and $r_d = \infty$. Determine the small signal voltage gain, input resistance and output resistance.

**Solution**

Given $R_{Si} = 0, R_1 = 520\,\text{k}\Omega, R_2 = 320\,\text{k}\Omega, R_S = 5\,\text{k}\Omega, R_D = 10\,\text{k}\Omega, g_m = 0.442\,\text{mA/V}$ and $r_d = \infty$.

*Input resistance*

$$R_i' = R_1 \parallel R_2 = (520 \times 10^3) \parallel (320 \times 10^3) = 198\,\text{k}\Omega$$

*Small signal voltage gain*

$$A_V = \frac{V_o}{V_i} = -g_m (r_d \parallel R_D)\left(\frac{R_i'}{R_{Si} + R_i'}\right)$$

$$= -0.442 \times 10^{-3} \times 10 \times 10^3 \left(\frac{198 \times 10^3}{0 + (198 \times 10^3)}\right) = -4.42$$

*Output resistance*

$$R_o' = r_d \parallel R_D = \infty \parallel 10 \times 10^3 \approx 10\,\text{k}\Omega$$

## 3.9 SMALL SIGNAL ANALYSIS OF CD ENHANCEMENT MOSFET (E-MOSFET) AMPLIFIER

The common drain *N*-channel E-MOSFET amplifier is shown in Fig. 3.18. Here, the output signal is taken from the source and the drain is directly connected to drain voltage $V_{DD}$. Since $V_{DD}$ is the signal ground in the ac equivalent circuit, it is known as *common drain amplifier*. Here, the output voltage at the source terminal follows the input signal and hence, it is also called *source follower.*

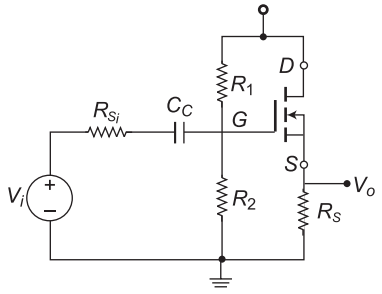



**Fig. 3.18** *Common drain E-MOSFET amplifier*

Figure 3.19(a) shows the small signal equivalent circuit of common drain amplifier with the coupling capacitor short circuited. Here, the drain terminal is at signal ground and the internal drain resistance $r_d$ is in parallel to the current source $g_m V_{gs}$. The equivalent circuit of the amplifier with all signal grounds connected to a common point is shown in Fig. 3.19(b).

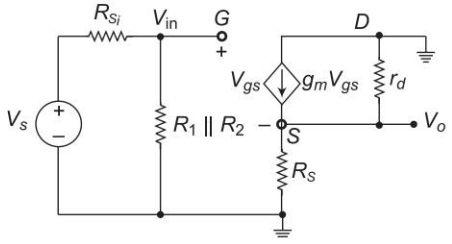



**Fig. 3.19 (a)** *Small signal equivalent circuit of common drain amplifier*

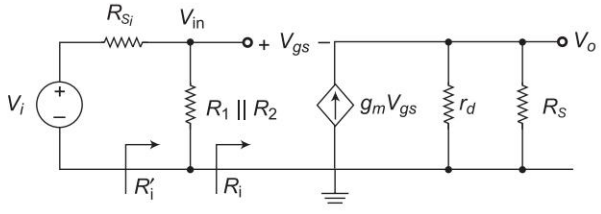



**Fig. 3.19 (b)** *Equivalent circuit with all signal grounds connected to a common point*

***Input Resistance*** The input resistance $R_i$ looking into the gate input of the E-MOSFET amplifier is infinite i.e., $R_i = \infty$. Hence, the overall input resistance by considering the bias resistors $R_1$ and $R_2$ is

$$R_i' = R_i \parallel R_B \approx R_1 \parallel R_2$$

***Voltage Gain*** The output voltage is given by

$$V_o = g_m V_{gs}(r_d \parallel R_S)$$

where $r_d$ is the internal drain resistance and $R_S$ is the source resistance or load resistance. Using KVL equation from input terminal to output terminal, we get

$$V_{in} = V_{gs} + V_o = V_{gs} + g_m V_{gs}(r_d \parallel R_S)$$

Hence, the gate to source voltage is

$$V_{gs} = \frac{V_{in}}{1 + g_m(r_d \parallel R_S)} = \left( \frac{\frac{1}{g_m}}{\frac{1}{g_m} + (r_d \parallel R_S)} \right) V_{in}$$

The voltage $V_{in}$ is related to the source input voltage $V_i$ by

$$V_{in} = \left( \frac{R_i'}{R_{Si} + R_i'} \right) \cdot V_i$$

The small signal voltage gain ($A_V$) is the ratio of output voltage ($V_o$) to input voltage ($V_i$) as given by

$$A_V = \frac{V_o}{V_i} = \frac{g_m V_{gs}(r_d \parallel R_S) R_i'}{(R_S + R_i) V_{in}}$$

$$= \frac{g_m (r_d \parallel R_S)}{\left[1 + g_m (r_d \parallel R_S)\right]} \left( \frac{R_i'}{R_{Si} + R_i'} \right)$$

$$= \frac{r_d \parallel R_S}{\left[ \frac{1}{g_m} + (r_d \parallel R_S) \right]} \left( \frac{R_i'}{R_{Si} + R_i'} \right)$$

The above equation shows that the magnitude of the voltage gain is always less than unity like BJT emitter follower.

***Output Resistance*** The output resistance is determined by short circuiting the input voltage i.e., $V_i = 0$ and by applying a test voltage $V_x$ as shown in Fig. 3.20.

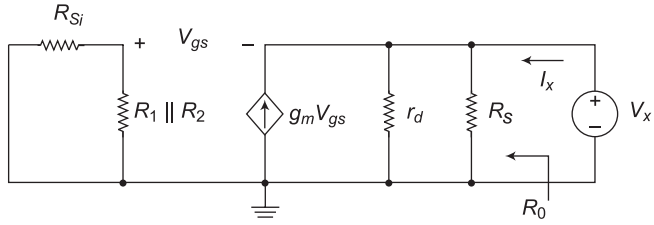



**Fig. 3.20** *Equivalent circuit of common drain amplifier to determine the output resistance*

Using KCL equation at the output source node of Fig. 3.20, we get

$$I_x + g_m V_{gs} = \frac{V_x}{r_d} + \frac{V_x}{R_S}$$

Here, $V_{gs} = -V_x$. Therefore,

$$I_x = g_m V_x + \frac{V_x}{r_d} + \frac{V_x}{R_S}$$

i.e.,

$$\frac{I_x}{V_x} = g_m + \frac{1}{r_d} + \frac{1}{R_S}$$

The output resistance can be defined as

$$R_o = \left. \frac{V_x}{I_x} \right|_{V_i = 0} = \frac{1}{g_m} \parallel r_d \parallel R_S$$

## EXAMPLE 3.6

For the common drain E-MOSFET amplifier shown in Fig. 3.18, $R_{Si}$ = 200 Ω, $R_1$ = 119 kΩ, $R_2$ = 281 kΩ, $R_S$ = 3.3 kΩ, $g_m$ = 11.3 mA/V and $r_d$ = 12.5 kΩ. Determine the small signal voltage gain, input resistance and output resistance.

**Solution** Given $R_{Si}$ = 200 Ω, $R_1$ = 119 kΩ, $R_2$ = 281 $k$Ω, $R_S$ = 3.3 kΩ, $g_m$ = 11.3 mA/V and $r_d$ = 12.5 kΩ.

*Input resistance*

$$R_i' = R_1 \parallel R_2 = (119\times10^3) \parallel (281\times10^3) = 83.6\,\text{k}\Omega$$

*Small signal voltage gain*

$$A_V = \frac{r_d \parallel R_S}{\left[\frac{1}{g_m} + (r_d \parallel R_S)\right]}\left(\frac{R_i'}{R_{Si} + R_i'}\right)$$

$$= \frac{12.5\times10^3 \parallel 3.3\times10^3}{\left[\frac{1}{11.3\times10^{-3}} + (12.5\times10^3 \parallel 3.3\times10^3)\right]}\left(\frac{83.6\times10^3}{(0.2\times10^3) + (83.6\times10^3)}\right)$$

$$= \frac{2.61\times10^3}{[0.088\times10^3 + 2.61\times10^3]}\times 0.997 = 0.964$$

*Output resistance*

$$R_o = \frac{1}{g_m} \parallel r_d \parallel R_S = \frac{1}{11.3\times10^{-3}} \parallel (12.5\times10^3) \parallel (3.3\times10^3) = 0.085\,\Omega$$

## 3.10 SMALL SIGNAL ANALYSIS OF CG ENHANCEMENT MOSFET (E-MOSFET) AMPLIFIER

The common gate *N*-channel E-MOSFET amplifier is shown in Fig. 3.21. Here, the input signal is given to the source terminal and the output signal is taken from the drain terminal. Since the gate terminal is at signal ground, it is called *common gate amplifier*.

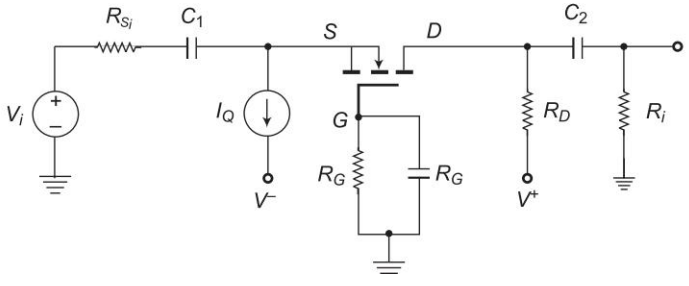



**Fig. 3.21** *Common gate E-MOSFET amplifier*

Figure 3.22 shows the small signal equivalent circuit of common gate amplifier with the coupling capacitors $C_1$, $C_2$ and $G_G$ short circuited. Here, the gate terminal is at signal ground and the internal drain resistance $r_d$ is assumed to be ∞.

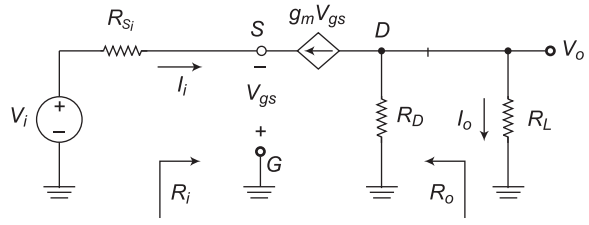



**Fig. 3.22** *Small signal equivalent circuit of common gate amplifier*

***Voltage Gain*** From Fig. 3.22, it is seen that the output voltage is

$$V_o = -g_m V_{gs}(R_D \parallel R_L)$$

Applying KVL equation to the input loop, we get

$$V_i = R_S I_i - V_{gs} = -V_{gs}(1 + g_m R_S) \qquad (\text{since } I_i = -g_m V_{gs})$$

Therefore, the gate to source voltage is given by

$$V_{gs} = \frac{-V_i}{(1 + g_m R_S)}$$

Now, the small signal voltage gain is

$$A_V = \frac{V_o}{V_i} = \frac{g_m(R_D \parallel R_L)}{(1 + g_m R_S)}$$

Here, the voltage gain is positive, and the input and output signals are in phase.

***Current Gain*** Referring to Fig. 3.23, the current gain for common gate amplifier can be determined by the small signal equivalent circuit with Norton current circuit as the signal source.

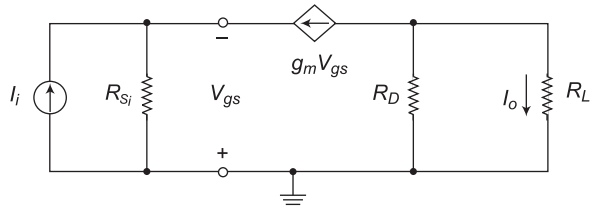



**Fig. 3.23** *Small signal equivalent circuit of common gate amplifier with Norton current source*

Using current divider rule, the output current is given by

$$I_o = \left(\frac{R_D}{R_D + R_L}\right)(-g_m V_{gs})$$

Using KCL at the input node, we have

$$I_i + g_m V_{gs} + \frac{V_{gs}}{R_S} = 0$$

i.e.,
$$V_{gs} = -I_i \left( \frac{R_S}{1 + g_m R_S} \right)$$

The small signal current gain ($A_I$) is the ratio of output current ($I_o$) to input current ($I_i$) as given by

$$A_I = \frac{I_o}{I_i} = \left( \frac{g_m R_S}{(1 + g_m R_S)} \right) \left( \frac{R_D}{R_D + R_L} \right)$$

If $R_D >> R_L$ and $g_m R_S >> 1$, then the current gain of common gate E-MOSFET amplifier becomes unity which is similar to that of common base amplifier of BJT.

***Input Resistance*** The common gate amplifier has low input resistance compared to common source and common drain amplifiers. Since the input signal is current, a low input resistance is an advantage. The input resistance for common gate amplifier can be defined as

$$R_i = \frac{-V_{gs}}{I_i} = \frac{1}{g_m} \qquad (\text{since } I_i = -g_m V_{gs})$$

***Output Resistance*** The output resistance can be obtained by short circuiting the input signal voltage i.e., $V_i = 0$. Applying KVL to the input loop of Fig. 3.22, we get

$$V_{gs} + g_m V_{gs} R_S = 0$$

i.e.,
$$V_{gs} = 0$$

Therefore,
$$g_m V_{gs} = 0$$

Now, the output resistance by looking into the drain terminal can be written as

$$R_o = R_D$$

## EXAMPLE 3.7

For the common gate E-MOSFET amplifier shown in Fig. 3.21, $R_S$ = 4 kΩ, $R_D$ = 10 kΩ, $R_L$ = 2 kΩ, $R_G$ = 50 kΩ, and $g_m$ = 2 mA/V, Determine the small signal voltage gain, current gain, input resistance and output resistance.

**Solution** Given $R_S = 4\,\text{k}\Omega, R_D = 10\,\text{k}\Omega, R_L = 2\,\text{k}\Omega, R_G = 50\,\text{k}\Omega$ and $g_m = 2\,\text{mA/V}$.

*Input resistance*

$$R_i = \frac{1}{g_m} = \frac{1}{2 \times 10^{-3}} = 500\,\Omega$$

*Small signal voltage gain*

$$A_V = \frac{g_m(R_D \parallel R_L)}{(1+g_m R_S)} = \frac{2\times10^{-3}\left[(10\times10^3)\parallel(2\times10^3)\right]}{(1+2\times10^{-3}\times4\times10^3)} = 0.37$$

*Small signal current gain*

$$A_I = \left(\frac{g_m R_S}{(1+g_m R_S)}\right)\left(\frac{R_D}{R_D+R_L}\right)$$

$$= \left(\frac{2\times10^{-3}\times4\times10^3}{(1+2\times10^{-3}\times4\times10^3)}\right)\left(\frac{10\times10^3}{10\times10^3+2\times10^3}\right) = 0.74$$

*Output resistance*

$$R_o = R_D = 10\,\text{k}\Omega$$

## 3.11 BASIC FET DIFFERENTIAL PAIR

As in the analysis of BJT-based differential amplifiers with resistive loading and active loading, the JFET based differential amplifiers can also be analyzed. The JFET differential amplifier with resistive loading only is considered below for the ac and dc analysis because of the fact that JFET differential amplifier with active loading is quite complex. MOSFETs are widely used in the input stages of the differential amplifiers for better stability.

***JFET Source-Coupled Pair: dc Analysis*** The source-coupled differential amplifier is shown in Fig. 3.24. The circuit is initially studied for its dc operation, which will set the stage for the small-signal model. Here, $J_1$ and $J_2$ are assumed identical with matched drain resistors.

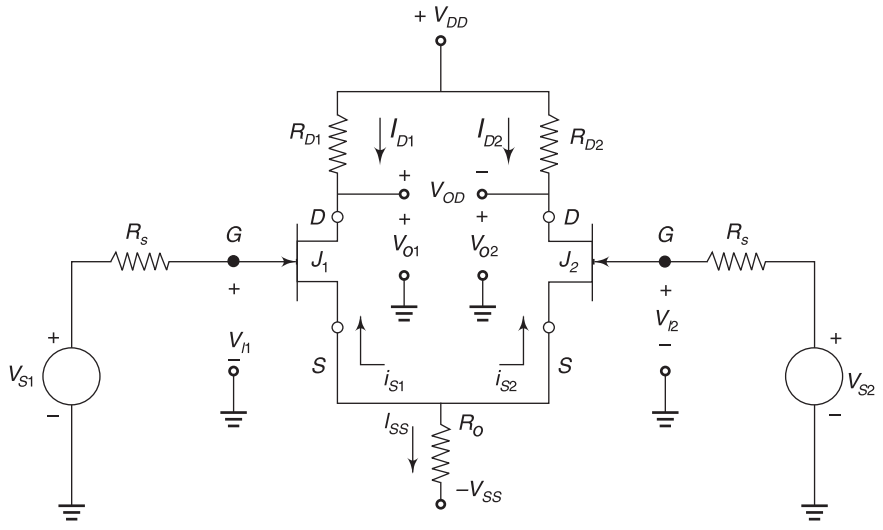



**Fig. 3.24** *Source coupled differential amplifier*

Considering the input loop, we get

$$V_{I1} = V_{GS1} - V_{GS2} + V_{I2}$$

We know that

$$V_{GS} = V_P \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

where $I_D$ is the saturation drain current and $I_{DSS}$ is the value of $I_{DS}$ when $V_{GS} = 0$ and $V_P$ is the pinch-off voltage. The input differential voltage is

$$V_{ID} = V_{I1} - V_{I2}$$

Considering $J_1$ and $J_2$ to be ideal,

$$V_{P1} = V_{P2}$$

and

$$I_{SS} = I_{D1} + I_{D2}$$

By mathematical analysis of the above equations, we get

$$I_{D1} = \frac{I_{SS}}{2}\left[1 - \frac{V_{ID}}{V_P}\sqrt{2\left(\frac{I_{DSS}}{V_{SS}}\right) - \left(\frac{V_{ID}}{V_P}\right)^2\left(\frac{I_{DSS}}{I_{SS}}\right)^2}\right]$$

and

$$I_{D2} = \frac{I_{SS}}{2}\left[1 + \frac{V_{ID}}{V_P}\sqrt{2\left(\frac{I_{DSS}}{V_{SS}}\right) - \left(\frac{V_{ID}}{V_P}\right)^2\left(\frac{I_{DSS}}{I_{SS}}\right)^2}\right]$$

The above equations are graphed in Fig. 3.25 for the case $I_{SS} = I_{DSS}$ (or) $I_D = I_{DSS}/2$.

These transfer functions resemble the corresponding result for the bipolar-based differential amplifier as shown in Fig. 3.25, but with the linear region around $V_{ID} = 0$ much wider for the JFET. However the JFET differential amplifier can handle much larger input signals than its bipolar counterpart, which is an important advantage.

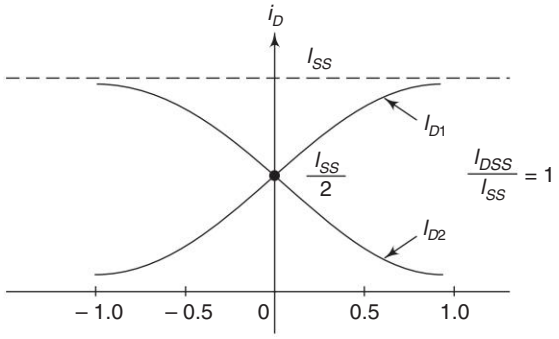



**Fig. 3.25** *Drain current of a source-coupled pair as a function of the differential input voltage $I_{SS} = I_{DSS}$*

The drain output voltage is

$$V_{o1} = V_{DD} - I_{D1}R_{D1}$$

$$V_{o2} = V_{DD} - I_{D2}R_{D2}$$

When $R_{D1} = R_{D2} = R_D$, the output differential voltage is given by

$$V_{OD} = (V_{DD} - I_{D1}R_D) - (V_{DD} - I_{D2}R_D) = -I_{D1}R_D + I_{D2}R_D$$

Therefore,

$$V_{OD} = \frac{I_{SS}\,R_D\,V_{ID}}{V_P}\sqrt{2\left(\frac{I_{DSS}}{I_{SS}} - \left(\frac{V_{ID}}{V_P}\right)^2\left(\frac{I_{DSS}}{I_{SS}}\right)^2\right)}$$

Again, the output differential voltage is shown to be a function of the input differential voltage, and this is plotted in Fig. 3.26. For small $V_{ID}$, the transfer function is approximately linear.

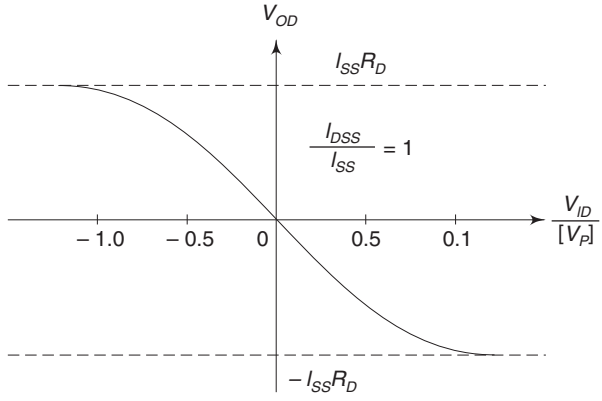



**Fig. 3.26** *Differential output voltage of a common-source amplifier as a function of the differential input voltage ($I_{SS} = I_{DSS}$)*

The differential voltage gain is found by differentiating the above equation with respect to $V_{ID}$ and letting $V_{ID} = 0$,

$$A_{dm} = \left.\frac{dV_{OD}}{dV_{ID}}\right|_{V_{ID}=0} = \frac{I_{SS}\,R_D}{V_P}\sqrt{\frac{2\,I_{DSS}}{I_{SS}}}$$

and

$$A_d = \frac{R_D}{V_P}\sqrt{2\,I_{SS}\,I_{DSS}}$$

At $V_{ID} = 0$, $I_{SS} = 2I_D$ (Refer to Fig. 3.26) and since $g_m = \frac{2}{V_P}\sqrt{I_D\,I_{DSS}}$, we get

$$A_{dm} = -\,g_m R_D$$

This is the same as voltage gain of a single-ended common source amplifier, which means that there is zero dc voltage offset as input to the next stage.

***JFET Common-Source Amplifier—ac Analysis*** The small-signal models for both BJT and FET based differential amplifiers are modeled using voltage-controlled current generators. However, the transconductance and output resistance have different physical basis and are computed differently. It should be noted that the FET input resistance is essentially infinite, but the manipulation of the model is the same.

Figure 3.27 shows the small-signal representation of the JFET source-coupled amplifier. By applying a differential input voltage, the circuit can be simplified as shown in Fig. 3.28. However, the analysis part remains the same as that of BJT.

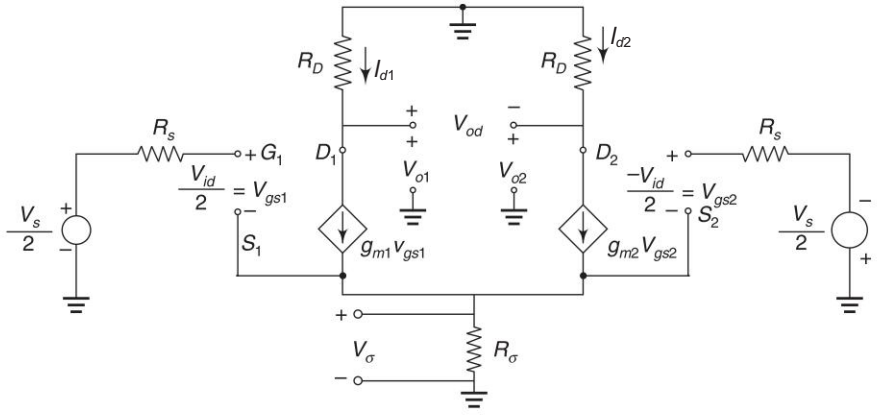



**Fig. 3.27** *Small-signal mode with differential input*

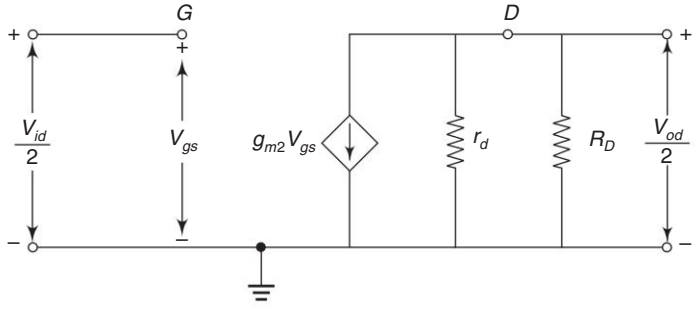



**Fig. 3.28** *Half-circuit model with differential mode*

Here,

$$A_{dm} = \frac{V_{od}}{V_{id}} = -g_m (R_D \parallel r_d)$$

## EXAMPLE 3.8

Find the $Q$-point for the MOSFETS in the differential amplifier shown in Fig. 3.29 with $V_{DD} = V_{SS} = 12$ V, $I_{SS} = 175$ μA, $R_D = 65$ kΩ, $K_N = 3$ mA/V$^2$ and $V_{TN} = 1$ V. What is the maximum $V_{IC}$ for which $M_1$ remains saturated?

**Solution**

$$I_{DS} = \frac{I_{SS}}{2} = \frac{175 \times 10^{-6}}{2} = 87.5\ \mu\text{A}$$

$$V_{GS} = V_{TN} + \sqrt{\frac{I_{SS}}{K_N}} = 1 + \sqrt{\frac{175 \times 10^{-6}}{3 \times 10^{-3}}} = 1.242\ \text{V}$$

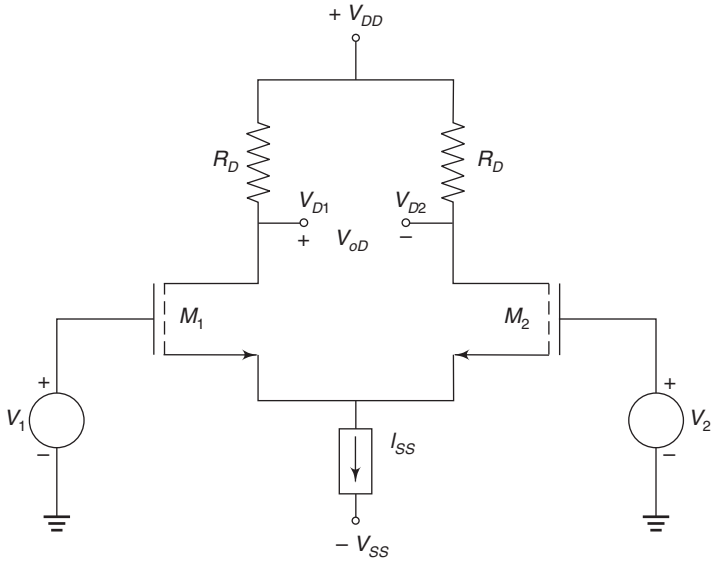



**Fig. 3.29**

$$V_{DS} = V_{DD} - I_{DS}R_D + V_{GS} = 12 - (87.5 \times 10^{-6}\text{ A})$$
$$(65 \times 10^{+3}) + 1.242 = 7.55\text{ V}$$

Checking for saturation,

$$V_{GS} - V_{TN} = 0.242\text{ V}$$

and $V_{DS} \geq 0.2$. Thus, both transistors in the differential amplifier are biased at the $Q$-point of (87.5 μA, 7.55 V).

Requiring saturation of $M_1$ for non-zero $V_{IC}$,

$$V_{GD} = V_{IC} - (V_{DD} - I_{DS}R_D) \leq V_{TN}$$
$$V_{IC} \leq V_{DD} - I_DR_D + V_{TN}$$
$$= 12 - (87.5 \times 10^{-6})(65 \times 10^3) + 1 = 7.31\text{ V}$$

## 3.12 BiCMOS CIRCUITS

The bipolar technology using NPN and PNP bipolar junction transistors and the MOS technology using NMOS and PMOS field-effect transistors are utilized to design basic amplifier. When both BJT and MOSFET are biased at the same current levels, comparing to MOSFETS, the BJTs have a larger transconductance and the BJT amplifiers have larger voltage gains. The MOSFET circuits have very high (infinite) input impedance at low frequencies and the zero input bias current.

The advantages of the above technologies can be obtained by combining BJTs and MOSFETs in the same integrated circuit. Such a technology is called BiCMOS. This technology is useful in digital circuit design and analog circuits. The basic BiCMOS analog circuit configurations are discussed in this section.

### 3.12.1 Basic Amplifier Stage-BiCMOS Darlington Pair

A modified bipolar multitransistor Darlington pair configuration is shown in Fig. 3.30(a). The bias current $I_{Bias}$ is used to control the quiescent current in $Q_1$. This Darlington pair circuit is used to improve the effective current gain of bipolar transistors. A BiCMOS circuit in which transistor $Q_1$ in the Darlington pair is replaced with a MOSFET is shown in Fig. 3.30(b). Infinite input resistance due to MOSFET $M_1$, and large transconductance due to BJT $Q_2$ are the main advantages.

The small-signal equivalent circuit of Fig. 3.31 is used to analyze the BiCMOS Circuit.

Assume $r_0 = \infty$ in both MOSFET and BJT.

Using KCL, we get the output signal current as

$$I_o = g_{m1}V_{gs} + g_{m2}V_{\pi} \tag{3.15}$$

where

$$V_i = V_{gs} + V_{\pi} \tag{3.16}$$

and $V_{\pi}$ is the voltage drop across $r_{\pi}$

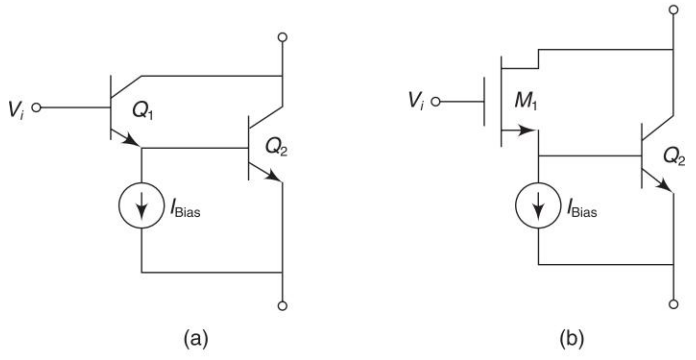



**Fig. 3.30** *(a) Darlington pair configuration using BJTs and (b) Darlington pair configuration of BiCMOS*

Hence,

$$V_{\pi} = g_{m1}V_{gs}r_{\pi} \tag{3.17}$$

Substituting Eq. (3.17) in (3.16) gives

$$V_i = V_{gs} + g_{m1}V_{gs}r_{\pi}$$

Hence,

$$V_{gs} = \frac{V_i}{1 + g_{m1}r_{\pi}} \tag{3.18}$$

The output current becomes

$$I_o = g_{m1}V_{gs} + g_{m2}(g_{m1}r_{\pi})V_{gs}$$

$$= (g_{m1} + g_{m2}g_{m1}r_{\pi})V_{gs} \tag{10.19}$$

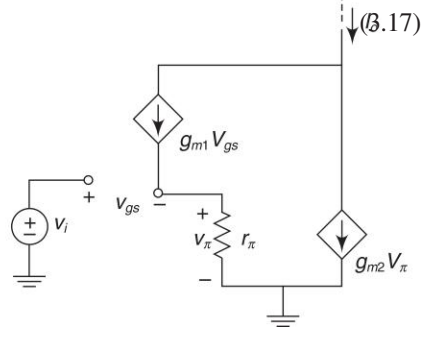



**Fig. 3.31** *Small signal equivalent circuit, BiCMOS Darlington pair configuration*

Substituting for $V_{gs}$ from Eq. (10.38) into Eq. (10.39) we get

$$I_o = \frac{g_{m1}(1 + g_{m2}r_\pi)}{(1 + g_{m1}r_\pi)} \cdot V_i = g_m^c \cdot V_i$$

where $g_m^c$ is the *composite transconductance*. Since $g_{m2}$ of the BJT is greater than $g_{m1}$ of the MOSFET, the composite transconductance is larger than the transconductance of the MOSFET alone. The resulting advantages are large transconductance and an infinite input resistance.

### 3.12.2 BiCMOS Cascode Configuration

Figures 3.32(a) and (b) show a basic bipolar cascode circuit and the corresponding BiCMOS configuration respectively. The cascode circuit offers very high output resistance and the BiCMOS cascode amplifier offers wider frequency bandwidth than the common-emitter circuit, since the input resistance looking into the emitter of $Q_2$ is very low.

The advantage of the BiCMOS circuit is the infinite input resistance of $M_1$.

The equivalent resistance looking into the emitter of a BJT is less than the resistance looking into the source of a MOSFET. Therefore, the frequency response of a BiCMOS cascode circuit is superior when compared to that of all-MOSFET cascode circuit.

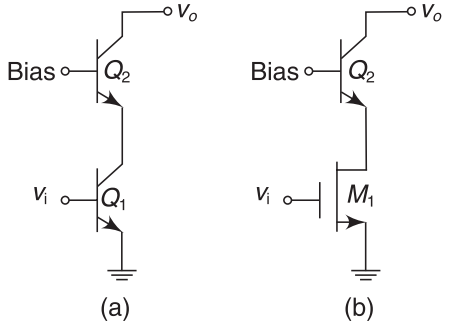



**Fig. 3.32** *(a) Bipolar cascode configuration (b) BiCMOS cascode configuration*

### 3.12.3 Current Sources

Biasing in integrated-circuit design is based on the use of constant-current sources. On an IC chip with a number of amplifier stages, a constant dc current (called a reference current) is generated at one location and is then replicated at various other locations for biasing the various amplifier stages through a process known as *current steering*.

The cascode current sources increase the output resistance, as well as the stability of the bias current. A BiCMOS double cascode constant-current source is shown in Fig. 3.33. The small-signal equivalent circuit to find the output resistance is shown in Fig. 3.34(a). The gate voltage to $M_6$ and the base voltages to $Q_2$ and $Q_4$ are constants, equivalent to signal ground. As $V_{\pi 2} = 0$, then $g_{m6}V_{\pi 2} = 0$, and its equivalent circuit is shown in Fig. 3.34(b).

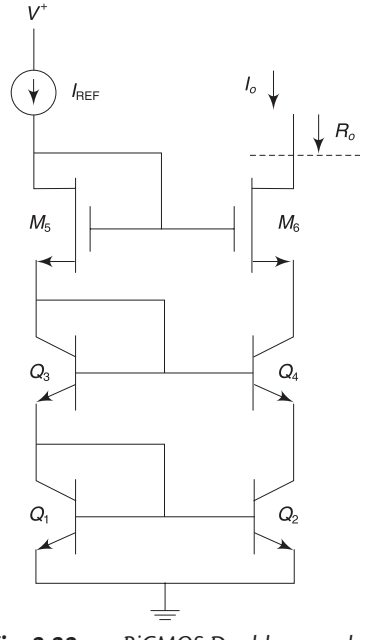



**Fig. 3.33** *BiCMOS Double cascade constant current source*

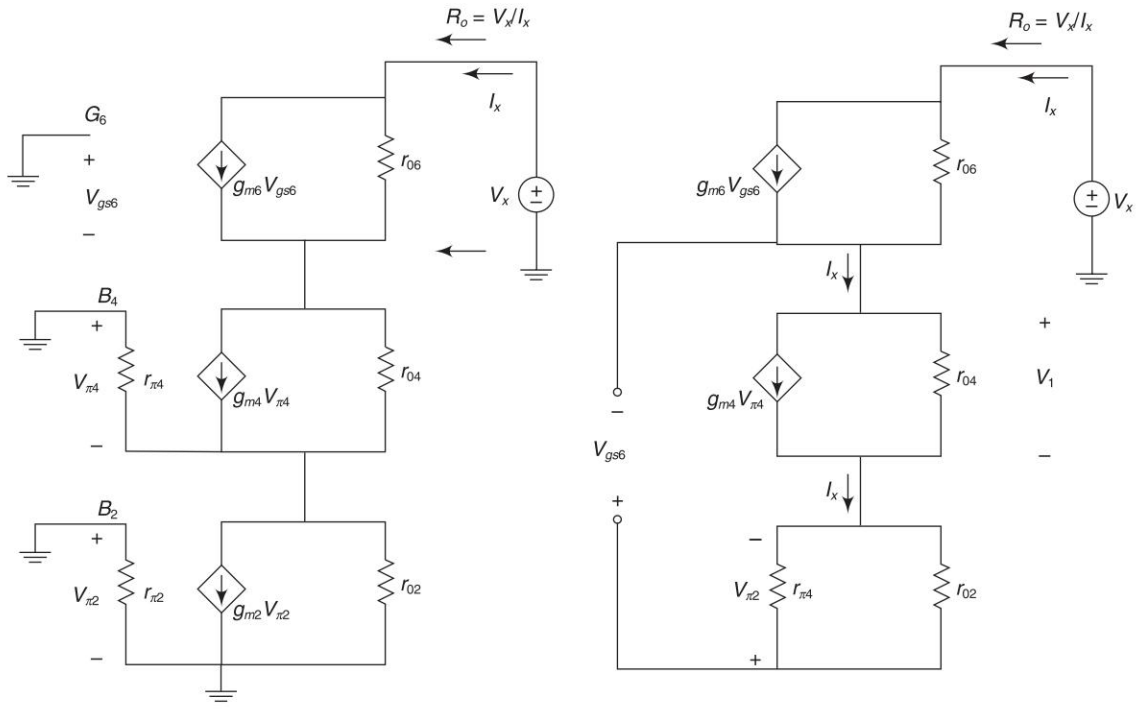



**Fig. 3.34** *(a) Equivalent circuit to find output impedance of BiCMOS double cascade source and (b) its equivalent circuit*

The output resistance of this circuit is very high. Here, the output resistance is approximately given by

$$R_o = (g_{m6}r_{o6})\,(\beta r_{o4})$$

The output resistance is increased by a factor, $g_m r_{o6}$, compared to the bipolar cascode circuit.

## REVIEW QUESTIONS

1. Draw the small-signal model of FET for low-frequency and high-frequency regions and compare them with the BJT models.
2. Draw the small-signal equivalent circuit of FET amplifier in CS connection and derive the equations for voltage gain, input impedance, and output impedance.
3. In the CS amplifier of Fig. 3.2(a), let $R_D = 4$ kΩ, $R_G = 50$ MΩ, μ = 40, $r_d = 40$ kΩ. Evaluate $A_V$, $Z_i$ and $Z_o$. [*Ans.* $A_V = -3.64$, $Z_i = 50$ MΩ $Z_o = 4$ kΩ]
4. Draw the small-signal equivalent circuit of FET amplifier in CD connection and derive the equation for voltage gain, input impedance, and output impedance.
5. In the CD amplifier of Fig. 3.3(a), let $R_s = 2$ kΩ, $R_G = 10$ MΩ, μ = 40, $r_d = 40$ kΩ. Calculate $A_v$, $Z_i$, and $Z_o$. [*Ans.* $A_V = 0.66$, $Z_i = 10$ MΩ $Z_o = 0.67$ kΩ]
6. Draw the small-signal equivalent circuit of a FET amplifier in CG connection and derive the equation for voltage gain, input impedance and output impedance.

7. In the CG amplifier of Fig. 3.4(b), let $R_D = 4$ kΩ, $R_s = 2$ kΩ, $g_m = 2 \times 10^{-3}$ mho, $r_d = 40$ kΩ. Calculate $A_V$, $Z_i$ and $Z_o$. [*Ans.* $A_V = 7.36$, $Z_i = 0.4$ kΩ, $Z_o = 4$ kΩ]
8. Draw the small-signal equivalent circuit of E-MOSFET amplifier in CS configuration and derive the expressions for voltage gain, input resistance and output resistance.
9. Draw the small-signal equivalent circuit of E-MOSFET amplifier in CD configuration and derive the expressions for voltage gain, input resistance and output resistance.
10. Draw the small-signal equivalent circuit of E-MOSFET amplifier in CG configuration and derive the expressions for voltage gain, current gain, input resistance and output resistance.
11. Draw the transfer characteristics of a differential amplifier and explain its salient features. Draw the circuit diagram of a FET-source coupled differential amplifier and derive the expression for differential voltage gain.
12. Explain the ac analysis of JFET common source differential amplifier.
13. What do you mean by BiCMOS technology?
14. Draw the BiCMOS Darlington pair configuration and derive the expression for Transconductance.
15. Draw the circuit diagram for BiCMOS double cascode constant current source and mention its advantages.

CHAPTER

4

# Frequency Response of Amplifiers

## 4.1 INTRODUCTION

The gain factors such as voltage, current, transconductance, and transresistance of amplifiers are functions of signal frequency. In the amplifier gain versus frequency plot, the gain factor is plotted in terms of decibels and frequency in terms of hertz on logarithmic scales. The main purpose is to determine the frequency response of amplifier circuits due to circuit capacitors and transistor capacitances. The frequency response will be useful to determine bandwidth of the circuit.

The transfer function is derived by using the complex frequency, of several passive circuits. With the help of Bode plots of the transfer function, the magnitude response, phase response, time constant, and 3 dB cut-off frequencies are calculated. In this chapter, the frequency responses of transistor circuits including BJTs and FETs are studied. The effects due to circuit capacitors including coupling, bypass, and load capacitors, and internal-transistor capacitances are analyzed. The *RF* amplifier and video amplifier circuits used in high-frequency applications are discussed.

## 4.2 LOGARITHMS

The analysis of amplifiers normally extends over a wide frequency range. Use of logarithmic scale makes it comfortable plotting the response between wide limits.

Logarithm taken to the base 10 is common logarithm. For example, the logarithm of a variable $a$ is $\log_{10} a$. Logarithm taken to the base $e$ is the natural logarithm. For example, logarithm of a variable $a$ is $\log_e a$.

Common logarithm: $u = \log_{10} a$

Natural logarithm: $v = \log_e a$

Natural logarithm can be written as $\ln a (= \log_e a)$. Numerically, $e = 2.71828$ and $\log_e a = 2.3 \log_{10} a$.

In amplifier analysis, a frequency of 10,000 Hz becomes $\log_{10} 10^4 = 4 \log_{10} 10 = 4$ in logarithmic scale. Thus, the frequency plot is compressed without major class of information and the problem of dealing with huge numbers is overcome.

In a semilog graph shown in Fig. 4.1 (a), only one of the two scales is a log scale. In a double-log graph shown in Fig. 4.1 (b), both the scales are log scales.

Figure 4.2 indicates how a linear scale is converted into a log scale. Thus, logarithmic scale helps to explain variations of parameters over a wide range by a simple graph.

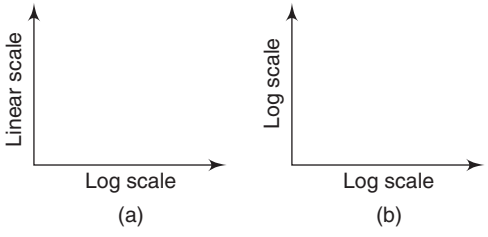



**Fig. 4.1** *(a) Semilog graph and (b) Double-log graph*

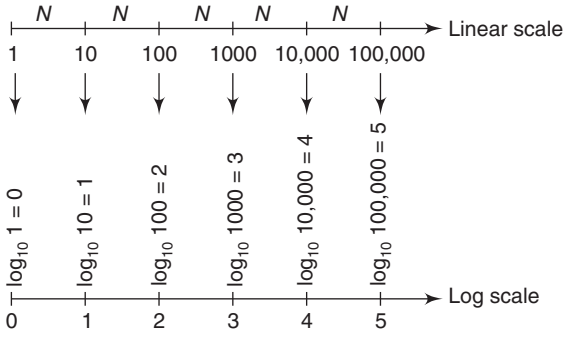



**Fig. 4.2** *Conversion from linear scale to logarithmic scale*

Common Mathematical Equations

1. If $a = b^u$ then $u = \log_b a$
   For example, if $\log_{10} 1 = y$, then $1 = 10^y$. Hence $y = 0$.
2. $\log_{10} \dfrac{u}{v} = \log_{10} u - \log_{10} v$
3. $\log_{10} uv = \log_{10} u + \log_{10} v$

Table 4.1 clearly shows how the logarithm of a number increases only as the exponent of the number.

**Table 4.1** *Increase in the logarithm of a number*

| |
|---|
| $\log_{10} 10^0 = 0 \times \log_{10} 10 = 0$ |
| $\log_{10} 10^1 = 1 \times \log_{10} 10 = 1$ |
| $\log_{10} 10^2 = 2 \times \log_{10} 10 = 2$ |
| $\log_{10} 10^3 = 3 \times \log_{10} 10 = 3$ |
| and so on. |

## 4.3 DECIBELS

Decibel is used to compare two power levels on a logarithmic basis. The term "bel" is derived from the name of the telephone inventor, Alexander Graham Bell. The unit "bel" (B) is defined relating two power levels $P_1$ and $P_2$ as

$$G = \log_{10}\left(\frac{P_2}{P_1}\right) \text{bel}$$

As "bel" was found to be a large unit for measurement, the "decibel" (dB) is defined where 10 decibels = 1 bel.

Hence,

$$G_{\text{dB}} = 10 \log_{10} \left( \frac{P_2}{P_1} \right) \text{dB}$$

The above equations indicate that dB is a measure of difference in magnitude between two power levels, say output power level and input power level (or some reference level).

Quite often the input power level (or reference power level) is taken as 1 milliwatt in electronics. Then "decibel" symbol can be written as dBm, where

$$G_{\text{dBm}} = 10 \log_{10} \frac{P_2}{1\,\text{mW}} \text{dBm}$$

In terms of voltage, $P_1 = \dfrac{V_1^2}{R_i}$ and $P_2 = \dfrac{V_2^2}{R_o}$ where $R_i$ is input resistance of the system, where output resistance $R_o$ is assumed to be equal to input resistance.

Hence,

$$G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} = 10 \log_{10} \frac{V_2^2 / R_o}{V_1^2 / R_i}$$

$$= 10 \log_{10} \left( \frac{V_2}{V_1} \right)^2$$

$$G_{\text{dB}} = 20 \log_{10} \left( \frac{V_2}{V_1} \right) \text{dB}$$

The advantage of logarithmic relationship is that the overall gain of a cascaded system is simply the sum of individual gains. Overall gain for a "$n$" stage system is given by

$$G = G_1 \times G_2 \times G_3 \times \ldots \times G_{n-1} \times G_n$$

$$\frac{V_{o/p}}{V_1} = \frac{V_2}{V_1} \times \frac{V_3}{V_2} \times \frac{V_4}{V_3} \times \cdots \times \frac{V_n}{V_{n-1}} \times \frac{V_{o/p}}{V_n}$$

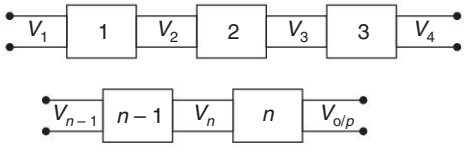



**Fig. 4.3** *n-stage cascaded system*

In a logarithmic relationship,

$$G_{\text{dB}} = 20 \log_{10} \left( \frac{V_{o/p}}{V_1} \right) = 20 \log_{10} \left( \frac{V_2}{V_1} \right) + 20 \log_{10} \left( \frac{V_3}{V_2} \right) + 20 \log_{10} \left( \frac{V_4}{V_3} \right) + \cdots$$

$$\ldots + 20 \log_{10} \left( \frac{V_n}{V_{n-1}} \right) + 20 \log_{10} \left( \frac{V_{o/p}}{V_n} \right)$$

where $G_{\text{dB}} = G_1 + G_2 + G_3 + \ldots G_{n-1} + G_n$

and $G_1$, $G_2$, $G_3$, … are voltage gains of stages 1, 2, 3, … respectively in decibels.

## EXAMPLE 4.1

Calculate the magnitude gain corresponding to a voltage gain of 200 dB.

**Solution**

$$G_{dB} = 20 \log_{10} \left( \frac{V_2}{V_1} \right) = 200 \text{ dB}$$

$$\log_{10} \left( \frac{V_2}{V_1} \right) = 10$$

$$\text{Gain} = \frac{V_2}{V_1} = 10^{10}$$

## EXAMPLE 4.2

A three-stage amplifier has a first stage-voltage gain of 30, second stage voltage gain of 200 and third stage gain of 400. Find the total voltage gain in dB.

**Solution** First-stage voltage gain in dB,

$$G_1 = 20 \log_{10} 30 = 20 \times 1.477 = 29.54$$

Second-stage voltage gain in dB,

$$G_2 = 20 \log_{10} 200 = 20 \times 2.3 = 46$$

Third-stage voltage gain in dB,

$$G_3 = 20 \log_{10} 400 = 20 \times 2.6 = 52$$

Therefore, the total voltage gain

$$G = G_1 + G_2 + G_3 = 29.54 + 46 + 52 = 127.54 \text{ dB}$$

## EXAMPLE 4.3

(a) A multistage amplifier employs five stages each of which has a power gain of 30. What is the total gain of the amplifier in dB? (b) If a negative feedback of 20 dB is employed, find the resultant gain.

**Solution** Given the gain of each stage = 30 and number of stages = 5.

(a) Power gain of one stage = $10 \log_{10} 30 = 10 \times 1.477 = 14.77$ dB
Total power gain = $5 \times 14.77 = 73.85$ dB

(b) The resultant power gain with negative feedback = $73.85 - 20 = 63.85$ dB

## EXAMPLE 4.4

In an amplifier, the output power is 1.5 W at 2 kHz and 0.3 W at 20 Hz, while the input power is constant at 10 mW. Determine by how many decibels is the gain at 20 Hz below that at 2 kHz?

**Solution** *To determine power gain at 2 kHz*

At 2 kHz, the output power is 1.5 W and input power is 10 mW.

Therefore, power gain in $\text{dB} = 10 \log_{10} \dfrac{1.5}{10 \times 10^{-3}} = 10 \log_{10} 150 = 21.76$

*To determine power gain in dB at 20 Hz*

At 20 Hz, the output power is 0.3 W and input power is 10 mW.

Therefore, power gain in $\text{dB} = 10 \log_{10} \dfrac{0.3}{10 \times 10^{-3}} = 10 \log_{10} 30 = 14.77$

Fall in gain from 2 kHz to 20 Hz = 21.76 – 14.77 = 6.99 dB

## EXAMPLE 4.5

An amplifier has a voltage gain of 15 dB. If the input signal voltage is 0.8 V, determine the output voltage.

**Solution** Voltage gain in dB = $20 \log_{10} V_2/V_1$

Therefore, $15 = 20 \log_{10} V_2/V_1$

$15/20 = \log_{10} V_2/V_1$

$0.75 = \log_{10} V_2/0.8$

Taking antilogarithm, we get

$10^{0.75} = V_2/0.8$

Hence, $V_2 = 10^{0.75} \times 0.8 = 4.5$ V

## Half-Power Bandwidth

In amplifier analysis, half-power gain is found out as follows:

$$\text{Half-power gain in dB} = 10 \log_{10} \frac{P_{\text{output max}}/2}{P_{\text{output max}}} = 10 \log_{10} \left(\frac{1}{2}\right) = 10 \log_{10} (0.5) = -3 \text{ dB}$$

Hence, the half-power gain is maximum gain minus three decibels.

As shown in Fig. 4.4, half-power bandwidth, i.e., ($f_2 \sim f_1$), is the frequency range over which gain is more than half-power gain.

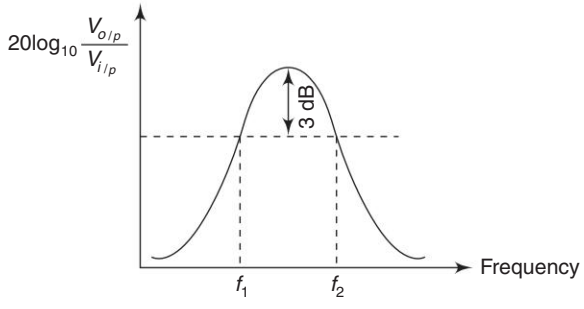



**Fig. 4.4** *Power gain frequency to determine half-power bandwidth*

## 4.4 AMPLIFIER FREQUENCY RESPONSE

The response of any single-stage (or) multistage network is highly influenced by the frequency of the applied signal. At low frequencies, the effect of capacitors (coupling and bypass) cannot be neglected due to their high value of capacitive reactance under these conditions. Moreover, any fluctuations in the number of stages of a cascaded system will also affect the frequency response of that system.

While plotting the frequency response of a circuit, it is conventional to use a logarithmic scale along the *X*-axis (horizontal axis), so as to permit a plot extending from low to the high-frequency regions. In general, any frequency response curve can be split into three regions, namely.

(i) Low-frequency region
(ii) Mid-frequency region
(iii) High-frequency region

In general, the frequency response curve is a plot between magnitudes of gain and logarithmic frequencies.

A typical frequency response curve of an *RC*-coupled amplifier is shown in Fig. 4.5.

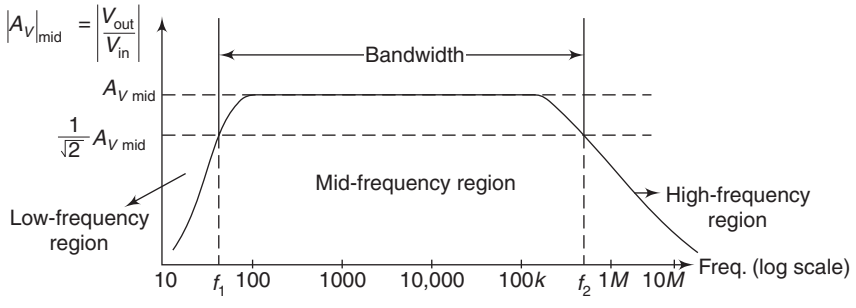



**Fig. 4.5** *Gain vs frequency (logarithmic scale) of an RC-coupled amplifier*

The main reason for the drop in gain at the low-frequency region and the high-frequency region is due to the increase in capacitive reactance in the low-frequency region and due to the parasitic capacitive elements (or) the frequency dependence of the network's gain on the active devices, in the high-frequency region.

The frequency boundaries of relatively high-gain region is determined by choosing "$\frac{1}{\sqrt{2}} A_{V\,\text{mid}}$" to be the gain at the cut-off levels. The frequencies corresponding to such values ($f_1$ and $f_2$) are called cut-off frequencies (or) band frequencies (or) corner frequencies (or) half-power frequencies.

At cut-off frequencies, the output power is half the mid-band power output.

$$P_{\text{out (mid)}} = \frac{|V_{\text{out}}^2|}{R_o} \tag{4.1}$$

But
$$|A_v|_{\text{mid}} = \left|\frac{V_{\text{out}}}{V_{\text{in}}}\right| \tag{4.2}$$

Therefore,
$$P_{\text{out}} = \frac{|A_{V_{\text{mid}}} V_{\text{in}}|^2}{R_o} \tag{4.3}$$

at half-power frequencies, $f_1$ and $f_2$ (Ref to Fig. 4.4).

$$P_{\text{out HPF}} = \frac{|0.707\ A_{V_{\text{mid}}} V_{\text{in}}|^2}{R_o} = 0.5\ \frac{|A_{V_{\text{mid}}} V_{\text{in}}|^2}{R_o} \tag{4.4}$$

Comparing Eqs (4.1) and (4.4),

$$P_{\text{out HPF}} = 0.5\ P_{\text{out (mid)}} \tag{4.5}$$

The bandwidth of each system is, hence, given by

$$\text{Bandwidth} = f_2 - f_1 \tag{4.6}$$

However, in most applications, it is preferable to have the plot of gains in (dB) and it is also conventional to use a normalized plot for such analysis. A normalized plot is a plot of gain vs log frequencies, with the gain values divided by the gain in the mid-frequency ranges (i.e., the maximum gain)

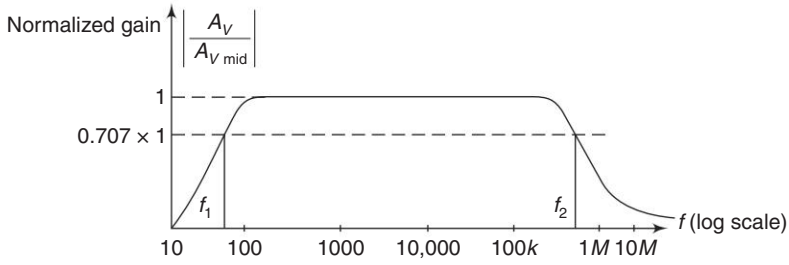



**Fig. 4.6** *Normalized plot for Fig. 4.5*

A decibel plot can now be obtained by using the following transformation:

$$\left.\frac{A_V}{A_{V_{\text{mid}}}}\right|_{\text{dB}} = 20 \log_{10} \frac{A_V}{A_{V_{\text{mid}}}} \tag{4.7}$$

Hence, the gain at half-power point becomes

$$20 \log_{10} \left(\frac{1}{\sqrt{2}}\right) = -3 \text{ dB}$$

The plot is as shown in Fig. 4.7.

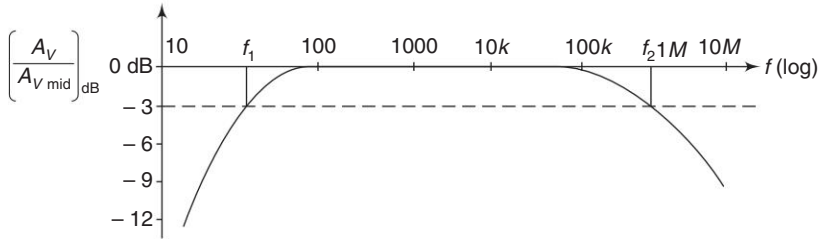



**Fig. 4.7** *Decibel plot of the normalized gain versus frequency (logarithmic) of Fig. 4.6*

**Note:** Figures (4.3 to 4.7), do not consider the 180° phase shift introduced by an *RC* coupled amplifier.

## 4.5 GENERAL FREQUENCY CONSIDERATIONS (LOW-FREQUENCY ANALYSIS)

The cut-off frequencies of single-stage BJT/FET amplifiers are influenced by the *RC* combinations formed by the network capacitors $C_C$, $C_E$, etc., and the resistive parameters that are present in the network.

For the purpose of analysis, each capacitive element can be modelled as one shown in Fig. 4.8 and its frequency response can be studied. Once the cut-off frequencies due to individual capacitors are studied, they can be compared to establish, which will determine the cut-off frequency (lower cut-off) for the system.

In this section, a methodology for determining the lower cut-off frequency ($f_1$) will be presented. However, a straightforward mechanism can be employed to find the upper cut-off frequency ($f_2$), with some extension in the frequency response region $f_1$ and $f_2$ are also referred to as $\alpha$ and $\beta$ cut-off frequencies.

From Figs. 4.9 and 4.10, it is seen that,

at high frequencies $$X_C = \frac{1}{2\pi fC} \approx 0\ \Omega$$

at low frequencies $$X_C = \frac{1}{2\pi fC} \approx \infty\ \Omega$$

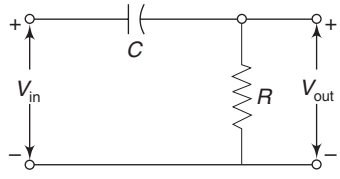



**Fig. 4.8** *Equivalent circuit for lower cut-off frequency analysis*

Figure 4.9 can be approximated as

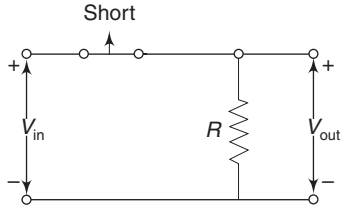



**Fig. 4.9** *At very high frequencies*

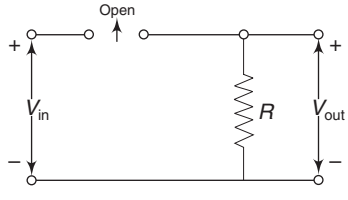



**Fig. 4.10** *At very low frequencies*

A typical frequency response between the above two extremes is shown in Fig. 4.11.

Applying the voltage divider rule in Fig. 4.8,

$$V_{out} = \frac{RV_{in}}{R - jX_C} \tag{4.8}$$

where, magnitude of $V_{out}$ is given by

$$|V_{out}| = \frac{RV_{in}}{\sqrt{R^2 + X_C^2}} \tag{4.9}$$

***Case:*** When $X_C = R$

$$|V_{out}| = \frac{RV_{in}}{\sqrt{R^2 + R^2}}$$

$$|V_{out}| = \frac{1}{\sqrt{2}} V_{in} \tag{4.10}$$

From Eq. (4.2),

$$|A_V| = \frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{2}} \frac{V_{in}}{V_{in}} = 0.707 \text{ at } X_C = R \tag{4.11}$$

which is shown in Fig. 4.11.

Now, as per the assumption

$$X_C = R$$

$$\frac{1}{2\pi f_1 C} = R$$

Therefore,

$$f_1 = \frac{1}{2\pi RC} \tag{4.12}$$

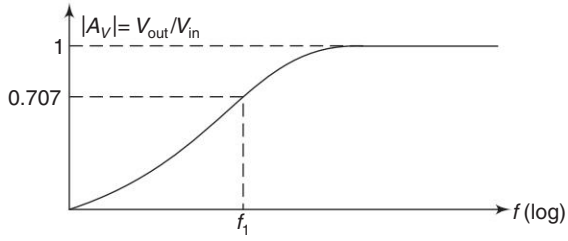



**Fig. 4.11** *$A_v$ vs frequency of a typical RC network*

In terms of dBs, 0.707 corresponds to 3 dB from Eq. (4.8),

$$A_V = \frac{V_{out}}{V_{in}} = \frac{R}{R - jX_C} \tag{4.13}$$

$$A_V = \frac{R}{R - jX_C} = \frac{1}{1 - j(X_C/R)} = \frac{1}{1 - j\left(\frac{1}{2\pi fCR}\right)} \tag{4.14}$$

Substituting Eq. (4.12) into Eq. (4.14), we get

$$A_V = \frac{1}{1 - j(f_1/f)} \tag{4.15}$$

When $f = f_1$,

$$|A_V| = \frac{1}{\sqrt{1 + (1)^2}} = \frac{1}{\sqrt{2}} = 0.707 \text{ , that corresponds to (–3 dB)} \tag{4.16}$$

In general, "$A_V$" can be written in magnitude and phase form.

$$A_V = \frac{V_{out}}{V_{in}} = \frac{\tan^{-1}(f_1/f)}{\sqrt{1 + (f_1/f)^2}} \tag{4.17}$$

In the logarithmic form (dB),

$$|A_V|_{dB} = 20 \log_{10} \frac{1}{\sqrt{1 + (f_1/f)^2}} \tag{4.18}$$

$$= -10 \log_{10} \left[1 + \left(\frac{f_1}{f}\right)^2\right] \tag{4.19}$$

If $f_1 >> f$, $(f_1/f)^2 >> 1$,

$$\left.\begin{aligned} |A_V|_{dB} &= -10 \log_{10} \left(\frac{f_1}{f}\right)^2 \\ &= -20 \log_{10} \frac{f_1}{f} \end{aligned}\right\} \quad (4.20)$$

Equation (4.20) can be used to find the future decibel plots, by ignoring the condition

$$f << f_1$$

Hence,

When $f = f_1; \quad \frac{f_1}{f} = 1$

Therefore, $|A_V|_{\text{dB}} = -20 \log_{10} 1 = 0 \text{ dB}$

When $f = \frac{1}{2} f_1; \quad \frac{f_1}{f} = 2$

Therefore, $|A_V|_{\text{dB}} = -20 \log_{10} 2 = -6 \text{ dB}$

When $f = \frac{1}{4} f_1; \quad \frac{f_1}{f} = 4$

Therefore, $|A_V|_{\text{dB}} = -20 \log_{10} 4 = -12 \text{ dB}$

and so on …

A plot of these values is shown in Fig. 4.12 for ranges $\frac{f_1}{10}$ to $f_1$.

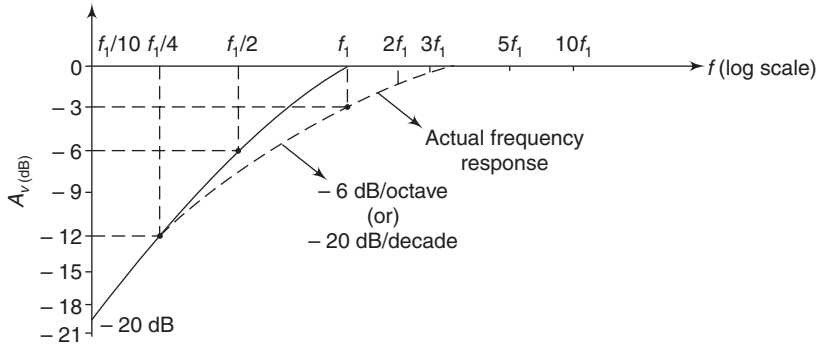



**Fig. 4.12** *Bode plot for the low-frequency region*

When $f = \frac{1}{10} f_1; \; \frac{f_1}{f} = 10$

$$|A_V|_{\text{dB}} = -20 \log_{10} 10 = -20 \text{ dB}$$

It could be noted from the figure that the plot of these values forms a straight line. However, for $f >> f_1$ a straight line is obtained only for the "0 dB" value, and hence, it could be said that sloped line for such low-frequency response can be obtained only when $f << f_1$. To add, at $f = f_1$ there is a 3 dB drop as given by Eq. (4.16).

Considering the above statements, a fairly accurate plot of the frequency response can be obtained as shown in Fig. 4.8. Such a plot is said to be a *bode plot*.

From the graph,

(i) A change in frequency by a factor of '2', (equivalent to octave) results in a 6 dB change in the ratio as noted in figure from $\frac{f_1}{2}$ to $f_1$.

(ii) For a 10 : 1 change (i.e., $f_1 \leftrightarrow f_{1/10}$) in frequency (equivalent to 1 decade), there is a 20dB change in the ratio.

Now, the exact procedure for finding the actual frequency response can be explained by considering an illustration.

## EXAMPLE 4.6

For the given network, perform the following:

(a) Determine the cut-off frequency (break frequency).
(b) Sketch the asymptotes.
(c) Locate the 3 dB point.
(d) Draw the actual frequency response curve.

**Solution**

(a) $f_1 = \dfrac{1}{2\pi RC} = \dfrac{1}{2\pi \times 10 \times 10^3 \times 0.2 \times 10^{-6}} = 79.57 \text{ Hz}$

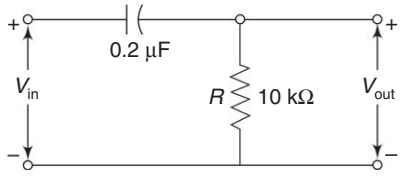



**Fig. 4.13**

For (b), (c), and (d):

Sketch the asymptotes, one along the 0 dB line and the other sloped at 6 dB/octave (or) 20 dB/decade

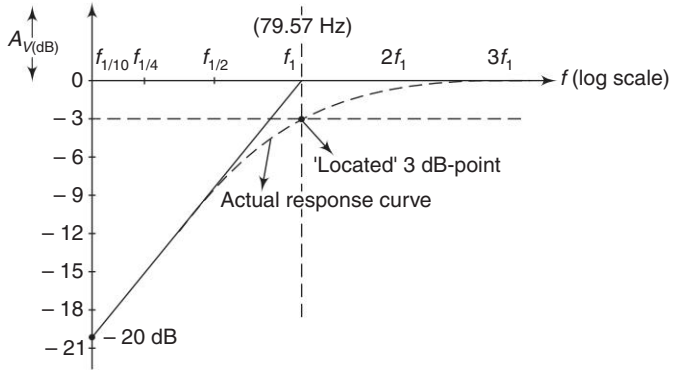



**Fig. 4.14**

## 4.6 TRANSIENT RESPONSE

The transient response of an amplifier can be defined as the output waveform that results when the input is a pulse (or) a sudden change in level. It is represented as a plot of voltage versus time in contrast to frequency response, which is plotted for frequency.

The transient response of an amplifier is completely dependent on its frequency response and vice versa and hence, if two amplifiers have identical frequency responses, they will have identical transient responses and vice versa. A pulse can be considered, as one that consists of an infinite number of frequency components, so the transient waveform represents the amplifier's ability (or inability) to amplify all frequency components equally and to phase shift all components equally. It is not possible for an amplifier to have infinite bandwidth, and hence, the transient response is always a distorted version of the input pulse.

To study the relationship between the frequency response and the time response, the simple *RC* network (low-pass) of Fig. 4.17 can be considered.

The transient response and the frequency response of such a circuit for a step input is given in Fig. 4.15 and Fig. 4.16 respectively.

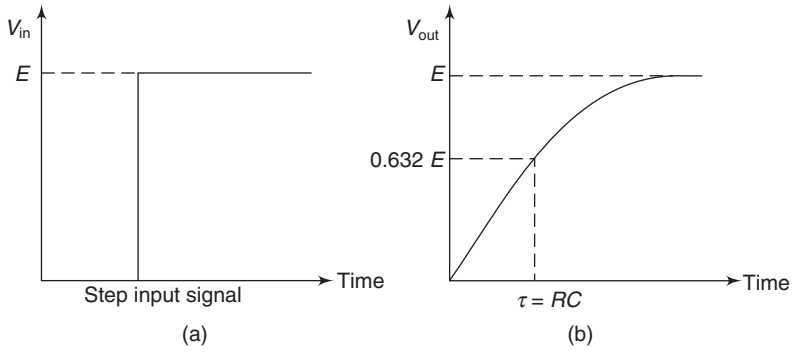



**Fig. 4.15** *Transient response (LPF)*

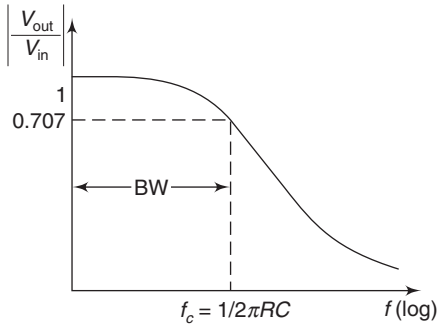



**Fig. 4.16** *Frequency response (LPF)*

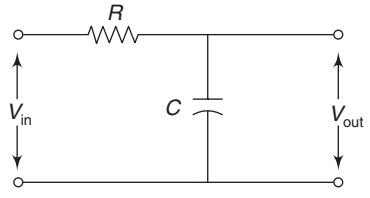



**Fig. 4.17** *Typical low pass RC network*

***Time Constant ($\tau$)*** ($\tau = RC$ seconds)

It is the time required for the transient output to reach 63.2% of its final value.

The upper cut-off frequency

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau} \text{ Hz}$$

Since it is a low-pass filter,

$$BW = f_2 - f_1$$
$$= f_2 - 0 = f_2 = \frac{1}{2\pi\tau} \text{ Hz}$$

It could be inferred that time required for the transient response to rise to a certain level is inversely proportional to bandwidth.

***Rise Time ($t_r$)*** It is the time required for a waveform to change from 10% of its *final value* to 90% of its *final value*.

For a Gaussian shaped response, it can be given that

$$t_r \approx \frac{0.35}{\text{BW}} \text{ second}$$

The above equation gives the relationship between rise time and bandwidth.

**EXAMPLE 4.7**

The rise time of a certain amplifier is 10*n*s. Calculate the approximate bandwidth of the amplifier.

**Solution**

$$BW \approx \frac{0.35}{t_r} = \frac{0.35}{10 \times 10^{-9}} = 0.035 \times 10^9 = 35 \text{ MHz}$$

## 4.7 LOW-FREQUENCY RESPONSE OF A TRANSISTOR AMPLIFIER WITH CIRCUIT CAPACITORS

In the earlier chapter, the equations for current and voltage gains for a small-signal amplifier have been derived. They are applicable in the mid-frequency region where it is assumed that reactances of coupling and bypass capacitors are negligible in this frequency region. In this section, the effect of these capacitors on the frequency response of the amplifier are discussed.

### 4.7.1 Effect of Emitter Bypass Capacitor ($C_E$) on Low-frequency Response

Consider the single-stage CE amplifier shown in Fig. 4.18. The emitter resistor $R_E$ contributes to biasing and thermal stability, and the bypass capacitor $C_E$ is connected across $R_E$ to avoid a degenerative effect due to negative feedback.

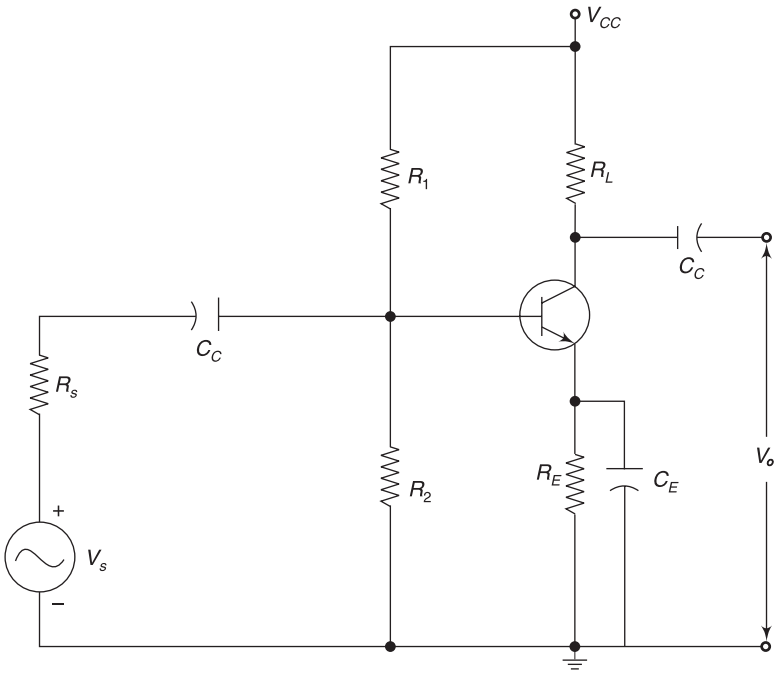



**Fig. 4.18** *Single-stage CE amplifier*

***Voltage Gain in the Low-frequency Region ($A_{V(LF)}$)*** $A_{V(LF)}$ is defined as the ratio of output voltage $V_o$ to the source voltage $V_s$.

$$A_{V(LF)} = \frac{V_o}{V_s} \tag{4.21}$$

It is assumed that in the low-frequency region, the coupling capacitor $C_C$ is sufficiently large so that its reactance is small and it does not have any effect on the response. Further, it is assumed that $R_1 \parallel R_2$ is much larger than input resistance $R_i$ so that they may be neglected in the *h*-parameter equivalent circuit shown in Fig. 4.19.

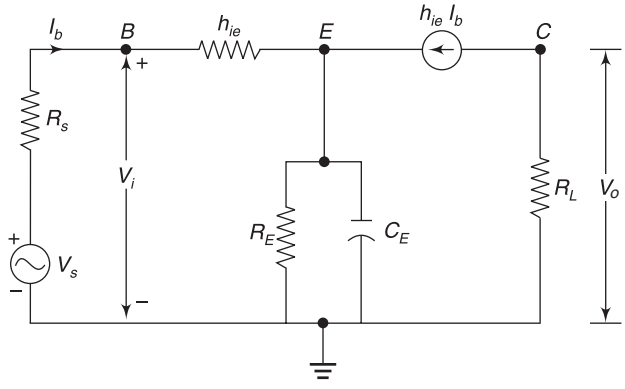



**Fig. 4.19** *Simplified h-parameter equivalent circuit for CE amplifier*

From Fig. 4.19,

$$V_o = -h_{fe} I_b R_L$$

where $$I_b = \frac{V_s}{R_s + R_i}$$

For a CE amplifier from Eq. (9.71),

$$R_i = h_{ie} + (1 + h_{fe})\, Z_E \tag{4.22}$$

where $$Z_E = R_E \parallel X_{CE}$$

$$= \frac{R_E}{1 + j\omega C_E R_E}$$

Substituting in Eq. (4.22),

$$R_i = h_{ie} + \frac{(1 + h_{fe})\, R_E}{1 + j\omega C_E\, R_E} \tag{4.23}$$

Hence, $$I_b = \frac{V_s}{R_s + h_{ie} + \dfrac{(1 + h_{fe})\, R_E}{1 + j\omega C_E\, R_E}} \tag{4.24}$$

and $$V_o = -h_{fe} R_L \frac{V_s}{R_s + h_{ie} + \dfrac{(1 + h_{fe})\, R_E}{1 + j\omega C_E R_E}}$$

$$A_{V(LF)} = \frac{V_o}{V_s} = \frac{-h_{fe} R_L}{R_s + h_{ie} + \dfrac{(1 + h_{fe})\, R_E}{1 + j\omega C_E R_E}} \tag{4.25}$$

When '$\omega$' is large, in the mid-frequency range,

$$A_{V(MF)} = \frac{V_o}{V_s} = \frac{-h_{fe}\, R_L}{R_s + h_{ie}} \tag{4.26}$$

The ratio of the gain at low frequencies to the gain at mid-frequencies,

$$\frac{A_{V(LF)}}{A_{V(MF)}} = \frac{R_s + h_{ie}}{R_s + h_{ie} + \dfrac{(1 + h_{fe})\, R_E}{1 + j\omega C_E R_E}} \tag{4.27}$$

$$= \frac{1}{1 + \dfrac{(1 + h_{fe})\, R_E}{R_s + h_{ie}}} \times \frac{1 + j\dfrac{f}{f_o}}{1 + j\dfrac{f}{f_p}} \tag{4.28}$$

where $f_o = \dfrac{1}{2\pi C_E R_E}$ and $f_p = \dfrac{1 + \dfrac{(1 + h_{fe})\, R_E}{R_s + h_{ie}}}{2\pi C_E\, R_E}$

If $\frac{(1+h_{fe})R_E}{R_s+h_{ie}} \gg 1$, then

$$f_p \approx \frac{\frac{(1+h_{fe})R_E}{R_s+h_{ie}}}{2\pi C_E R_E} \tag{4.29}$$

From Eqs (4.28) and (4.29), $f_p \gg f_o$.

If $\frac{A_{V(LF)}}{A_{V(MF)}}$ at $f = f_p$ is considered,

$$\frac{A_{V(LF)}}{A_{V(MF)}} = \frac{R_s+h_{ie}}{(1+h_{fe})R_E} \times \frac{1+j\frac{f_p}{f_o}}{1+j1}$$

$$\approx \frac{R_s+h_{ie}}{(1+h_{fe})R_E} \times \frac{j\frac{f_p}{f_o}}{1+j1}$$

The magnitude of this ratio is

$$\left|\frac{A_{V(LF)}}{A_{V(MF)}}\right| = \frac{R_s+h_{ie}}{(1+h_{fe})R_E} \times \frac{\frac{f_p}{f_o}}{\sqrt{2}}$$

But $$\frac{f_p}{f_o} \approx \frac{(1+h_{fe})R_E}{R_s+h_{ie}}$$

Therefore, $$\left|\frac{A_{V(LF)}}{A_{V(MF)}}\right| = \frac{1}{\sqrt{2}} \tag{4.30}$$

As the ratio of voltage gain has dropped by $\frac{1}{\sqrt{2}}$, the power gain at this low-frequency will be having a drop of $\frac{1}{2}$ or 3 dB form the gain at mid-frequency.

Thus, the lower 3 dB frequency is

$$f_1 \approx f_p = \frac{1+\frac{(1+h_{fe})R_E}{R_s+h_{ie}}}{2\pi C_E R_E}$$

$$\approx \frac{(1+h_{fe})R_E}{(R_s+h_{ie})2\pi C_E R_E}$$

$$= \frac{(1 + h_{fe})}{(R_s + h_{ie}) 2\pi C_E} \tag{4.31}$$

when $f_p = f_o$. If this condition is not met, $f_1 \neq f_p$ and there may not be a 3 dB point. From Eq. (4.31),

$$C_E = \frac{1 + h_{fe}}{2\pi f_1 (R_s + h_{ie})} \tag{4.32}$$

Thus, $C_E$ determines the lower 3 dB frequency $f_1$. Further, the equation for $f_1$ does not include $R_E$ so that the choice of $C_E$ for a given $f_1$ is dependent only upon the transistor and the source resistance.

**Note:**

(i) The use of electrolytic capacitors for $C_E$ cause reduction in the lower 3 dB frequency and the mid-frequency gain. If $R_{CE}$ represents the series resistance of $C_E$,

$$A_{V(MF)} = \frac{-h_{fe} R_L}{R_s + h_{ie} + (1 + h_{fe}) R_{CE}} \tag{4.33}$$

(ii) If the effect of biasing resistors $R_1$ and $R_2$ are taken into account,

$$A_{V(MF)} = \frac{-h_{fe} R_L}{R_s + h_{ie} + \dfrac{h_{fe} R_s}{R_B}} \tag{4.34}$$

where $R_B = R_1 \parallel R_2$.

## EXAMPLE 4.8

For the CE amplifier in Fig. 4.18, calculate the mid-frequency voltage gain and lower 3 dB point. The transistor has $h$-parameters of $h_{fe}$ = 400 and $h_{ie}$ = 10 kΩ. The circuit details are $R_s$ = 600 Ω, $R_L$ = 5 kΩ, $R_E$ = 1 kΩ, $V_{CC}$ = 12 V, $R_1$ = 15 kΩ, $R_2$ = 2.2 kΩ, and $C_E$ = 50 μF.

**Solution**

$$A_{V(MF)} = \frac{-h_{fe} R_L}{R_s + h_{ie} + \dfrac{h_{fe} R_s}{R_B}}$$

$$= \frac{-400 \times 5 \times 10^3}{600 + 10 \times 10^3 + \dfrac{400 \times 600}{15 \times 10^3 \parallel 2.2 \times 10^3}} = -145.69$$

Lower 3 dB point,

$$f_1 = \frac{(1 + h_{fe})}{(R_s + h_{ie}) 2\pi C_E}$$

$$= \frac{1 + 400}{(600 + 10 \times 10^3) \times 2\pi \times 50 \times 10^{-6}} = 120 \text{ Hz}$$

### 4.7.2 Effect of Coupling Capacitor $C_C$ on Low-Frequency response

In the CE amplifier of Fig. 4.18, it is desired to study the effect of coupling capacitor $C_C$ on the low-frequency response.

It is assumed that $C_E$ is large enough to cause no reduction in low-frequency gain. With $R_E$ effectively bypassed, the low-frequency model for the CE amplifier with the coupling capacitor $C_C$ is shown in Fig. 4.20.

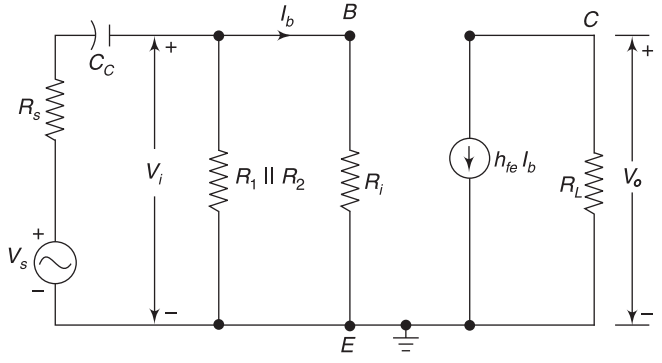



**Fig. 4.20** *Low-frequency model for CE amplifier with coupling capacitor*

In the mid-frequency range, reactance of $C_C$ is negligible. Hence, the equations for $A_{V(MF)}$ given in Eqs (4.33) and (4.34) are valid.

The lower 3 dB frequency

$$f_1 = \frac{1}{2\pi (R_s + R_i')C_C} \tag{4.35}$$

where $R_i' = R_1 \parallel R_2 \parallel R_i$

$R_i = h_{ie}$ for an ideal emitter-bypass capacitor

$R_i \approx h_{ie} + (1 + h_{fe})R_{CE}$, if capacitor's series resistance is taken into account.

Thus, from Eqs (4.31) and (4.35) for good low-frequency response (for lower $f_1$), the capacitors $C_C$ and $C_E$ should be large.

**EXAMPLE 4.9**

Calculate the coupling capacitor $C_C$ required in Fig. 4.20 to provide a low-frequency 3 dB point at 125 Hz if $R_s$ = 600 Ω, $h_{ie}$ = 1 kΩ, $h_{fe}$ = 60, $R_1$ = 5 kΩ and $R_2$ = 1.25 kΩ. For (a) an ideal bypass capacitor $C_E$ and (b) a practical bypass capacitor with $R_{CE}$ = 25 Ω.

**Solution** The lower 3 dB frequency, $f_1 = \dfrac{1}{2\pi (R_s + R_i')C_C}$

(a) $R_i' = R_1 \parallel R_2 \parallel h_{ie}$

$$C_C = \frac{1}{2\pi f_1 (R_s + R_i')} = \frac{1}{125 \times 2\pi \times [600 + 5000 \parallel 1.25 \times 10^3 \parallel 1000]}$$

$$= \frac{1}{125 \times 2\pi \times [600 + 500]} = 1.15\ \mu\text{F}$$

(b) $R_i' = R_1 \parallel R_2 \parallel [h_{ie} + (1 + h_{fe})\, R_{CE}]$

$= 5000 \parallel 1.25 \times 10^3 \parallel [1000 + (61)\,(25)] = 716.31\ \Omega$

$$C_C = \frac{1}{2\pi f_1 (R_S + R_i')}$$

$$= \frac{1}{125 \times 2\pi \times [600 + 716.31]} = 0.97\ \mu\text{F}$$

## 4.8 HIGH FREQUENCY $\pi$ MODEL FOR A TRANSISTOR

At high frequencies, the capacitive effects of the transistor junctions and the delay in response of the transistor caused by the process of diffusion of carriers should be taken into account in determining the high-frequency model of a transistor.

A high-frequency-$\pi$ or Giacoletto model for a transistor is shown in Fig. 4.21. Here, $r_{bb'}$ is the base spreading resistance between the actual base $B$ and virtual base $B'$. It represents the bulk resistance of the base. Its typical value is 100 Ω. Also, $r_{b'e}$ is the resistance between the virtual base $B'$ and the emitter terminal $E$. The typical value is 1 kΩ.

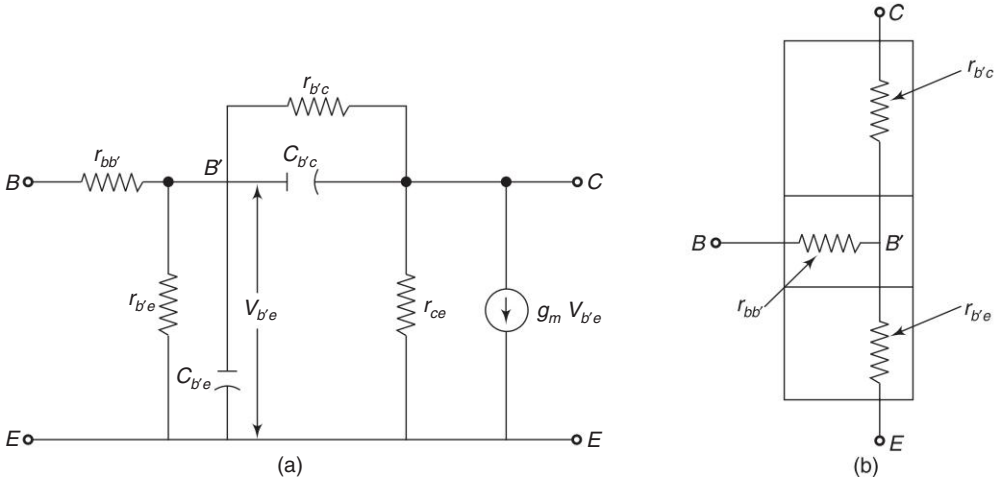



**Fig. 4.21** *(a) Hybrid-$\pi$ model for a transistor in the CE connection and (b) Virtual base B′ and ohmic base-spreading resistance $r_{bb'}$*

Input resistance from base to emitter with the output shorted is simply $r_{bb'} + r_{b'e}$ and this is the same as $h_{ie}$. Hence, $h_{ie} = r_{bb'} + r_{b'e}$.

$r_{b'c}$—resistance between the virtual base $B'$ and the collector terminal $C$. It has a large value (typical value = 4 MΩ).

$C_{b'e}$—diffusion capacitance of the normally forward biased base-emitter junction. It has a typical value of 100 pF.

$C_{b'c}$—transistor capacitance of the normally reverse biased collector-base junction. It has a typical value of 3 pF.

$r_{ce}$ — output resistance with a typical value of 80 kΩ. Since $r_{ce} \gg R_L$, if a load $R_L$ is connected $r_{ce}$ can be neglected.

$g_m V_{b'e}$ — output current generator value where $g_m$ is the transconductance of the transistor.

## 4.8.1 Hybrid-$\pi$ Conductances

The hybrid-$\pi$ model for the CE transistor at low frequencies is shown in Fig. 4.22(a). The *h*-parameter model for the same is shown in Fig. 4.22(b). As the hybrid-$\pi$ model is drawn for low frequencies, the capacitive elements are considered as open circuit.

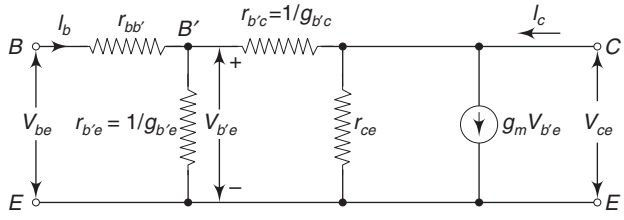



**Fig. 4.22 (a)** *Hybrid-$\pi$ model for a common-emitter transistor at low-frequency*

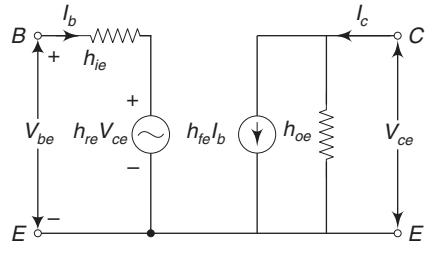



**Fig. 4.22 (b)** *h-parameter model for a common-emitter transistor at low-frequency*

***Base Spreading Resistance ($r_{bb'}$)*** In the circuit shown in Fig. 4.22(b), the value of input resistance is equal to $h_{ie}$ when the output terminals are short circuited, i.e., $V_{ce} = 0$. Under these conditions for the circuit in Fig. 4.22(a), the input resistance is given by

$$Z_i\big|_{V_{ce}=0} = r_{bb'} + r_{b'e} \parallel r_{b'c}$$

Therefore,

$$h_{ie} = r_{bb'} + r_{b'e} \parallel r_{b'c}$$

As $r_{b'c} \gg r_{b'e}$, the above equation can be written as

$$h_{ie} = r_{bb'} + r_{b'e}$$

***Conductance between Terminals B′ and C or the Feedback Conductance ($g_{b'c}$)*** In the circuit shown in Fig. 4.22(b), if the input terminals are open-circuited, then the reverse voltage gain $h_{re}$ can be written in terms of the circuit in Fig. 4.22(a), and it is given by

$$h_{re} = \frac{V_{b'e}}{V_{ce}} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}$$

Rearranging the above equation, we get

$$r_{b'e}\,(1 - h_{re}) = h_{re}\,r_{b'c}$$

As the value of $h_{re}$ is in the range of $10^{-4}$, the above equation can be approximated by

$$r_{b'e} = h_{re}\,r_{b'c} \quad \text{or} \quad g_{b'c} = h_{re}\,g_{b'e}$$

The equation also shows that the value of the resistance $r_{b'c}$ is much larger than resistance ($r_{b'e}$), i.e., $r_{b'c} \gg r_{b'e}$.

***Conductance between Terminals C and E ($g_{ce}$)*** In the circuit shown in Fig. 4.22(b), if the input terminals are open-circuited, then

$$V_{b'e} = h_{re}\,V_{ce}$$

For the circuit in Fig. 4.22(a), with the input terminals open, i.e., $I_b = 0$, the collector current $I_c$ is given by

$$I_c = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'e} + r_{b'c}} + g_m\,V_{b'e}$$

The value of output admittance $h_{oe}$ is given by

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b = 0} = \frac{1}{r_{ce}} + \frac{1}{r_{b'e} + r_{b'c}} + \frac{g_m\,V_{b'e}}{V_{ce}}$$

Substituting the value of $V_{be}$ in the above equation, we get the following:

Assuming that $r_{b'c} \gg r_{b'e}$, the above equation can be rewritten in terms of conductance as

$$h_{oe} = g_{ce} + g_{b'c} + g_m\,\frac{g_{b'c}}{g_{b'e}}$$

Substituting $g_m = h_{fe}\,g_{b'e}$ in the equation, we get

$$h_{oe} = g_{ce} + g_{b'c} + g_{b'c}\,h_{fe}$$

Rearranging the terms in the above equation, we get

$$g_{ce} = h_{oe} - (1 + h_{fe})\,g_{b'c}$$

Since $h_{fe} \gg 1$, the above equation can be written as

$$g_{ce} \cong h_{oe} - h_{fe}\,g_{b'c} \cong h_{oe} - g_m\,h_{re}$$

***Conductance between Terminals B′ and E or the Input Conductance ($g_{b'e}$)*** As the value of $r_{b'c}$ is much greater than $r_{b'e}$, most of the current $I_b$ flow through $r_{b'e}$ in the circuit shown in Fig. 4.22(b) and the value of $V_{b'e}$ is given by

$$V_{b'e} \cong I_b\,r_{b'e}$$

The short-circuit collector current, $I_c$, is given by

$$I_c = g_m\,V_{b'e} \cong g_m\,I_b\,r_{b'e}$$

The short-circuit current gain, $h_{fe}$ is defined as

$$h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce}} = g_m\,r_{b'e}$$

Rearranging the above equation, we get

$$r_{b'e} = \frac{h_{fe}}{g_m} \text{ or } g_{b'e}\,\frac{g_m}{h_{fe}}$$

***Transistor's Transconductance ($g_m$)*** The transconductance of a transistor ($g_m$) is defined as the ratio of change in $I_c$ to change in $V_{b'e}$ for constant value of collector-emitter voltage. For common-emitter transistor configuration, the expression for collector current is given by

$$I_c = I_{CO} + \alpha I_e$$

The value of $g_m$ is given by

$$g_m = \left.\frac{\partial I_c}{\partial V_{b'e}}\right|_{V_{CE}} = \text{constant} = \alpha\frac{\partial I_e}{\partial V_{b'e}} = \alpha\frac{\partial I_e}{\partial V_e}$$

The partial derivative emitter voltage with respect to the emitter current $\left(\text{i.e., } \frac{\partial V_e}{\partial I_e}\right)$ can be represented as the emitter diode ($r_e$) and the dynamic resistance of a forward-biased ($r_d$) is given as

$$r_d = \frac{V_T}{I_D}$$

where $V_T$ is the volt equivalent of temperature and $I_D$ is the diode current. Therefore, the value of $g_m$ can be generalized as

$$g_m = \frac{\alpha I_e}{V_T} = \frac{I_c - I_{CO}}{V_T}$$

As $I_c \gg I_{CO}$, the value of $g_m$ for a *NPN* transistor is positive. For a *PNP* transistor, the analysis can be carried out on similar lines and the value of $g_m$ in the case of a *PNP* transistor is also positive. Therefore, the above expression for $g_m$ is written as

$$g_m = \frac{|I_c|}{V_T}$$

## 4.8.2 Hybrid-$\pi$ Capacitances

In the hybrid $\pi$ model shown in Fig. 4.22(b), there are two capacitances, namely, the collector-junction barrier capacitance ($C_c$) and the emitter-junction diffusion capacitance ($C_e$).

***Collector-Junction Capacitance ($C_c$)*** The capacitance $C_c$ is the output capacitance of the common-base transistor configuration with the input open ($I_e = 0$). As the collector-base junction is reverse biased, $C_c$ is the transition capacitance and it varies as $(V_{CB})^{-n}$, where $n$ is 1/2 for abrupt junction and 1/3 for a graded junction.

***Emitter-Junction Capacitance ($C_e$)*** The capacitance $C_e$ is the diffusion capacitance of the forward-biased emitter junction and is proportional to the emitter current $I_e$ and is almost independent of temperature.

For a given collector current, the conductances and resistances of the hybrid-$\pi$ circuit calculated from the low-frequency $h$-parameter values from the equations are given in Table 4.2.

**Table 4.2** *Relationship between low-frequency h-parameters and high-frequency parameters*

| | |
|---|---|
| (i) | $g_m = \dfrac{\lvert I_C \rvert}{V_T}$ |
| | where $V_T = \dfrac{T}{11{,}600}$ with $T$ in K. At room temperature (300 K), $V_T = 0.026$ V so that $g_m = \dfrac{I_C(\text{in mA})}{26 \text{ mV}}$ |
| (ii) | $r_{b'e} = \dfrac{h_{fe}}{g_m}$ |
| (iii) | $r_{bb'} = h_{ie} - r_{b'e}$ |
| (iv) | $r_{b'c} = \dfrac{1}{g_{b'c}} = \dfrac{r_{b'e}}{h_{re}}$ |
| (v) | $g_{ce} = \dfrac{1}{r_{ce}} = h_{oe} - (1 + h_{fe}) g_{b'c}$ |

## EXAMPLE 4.10

A BJT has $h_{ie} = 6$ kΩ and $h_{fe} = 224$ at $I_C = 1$ mA, with $f_T = 80$ MHz and $C_{b'c} = 12$ pF. Determine the parameters, $g_m$, $r_{b'e}$ $r_{bb'}$ and $C_{b'e}$ of the small-signal high-frequency model of the BJT.

**Solution**

*To determine the parameters of the small signal high frequency model parameters of the BJT*

$$g_m = \frac{I_C(\text{mA})}{26 \text{ mV}} = \frac{1}{26} = 38.46 \text{ m mho}$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{224}{38.46 \times 10^{-3}} = 5.824 \text{ k}\Omega$$

$$r_{bb'} = h_{ie} - r_{b'e} = 6000 - 5824 = 176 \ \Omega$$

$$C_{b'e} = \frac{g_m}{2\pi f_T} - C_{b'c}$$

$$= \frac{38.46 \times 10^{-3}}{2\pi \times 80 \times 10^6} - 12 \times 10^{-12}$$

$$= 76.5 \times 10^{-12} - 12 \times 10^{-12} = 64.5 \text{ pF}$$

## 4.9 CE SHORT-CIRCUIT CURRENT GAIN

The transistor's high-frequency capability can be known, if its CE short-circuit forward-current transfer ratio or current gain is found as a function of frequency.

As $R_L$ is short-circuited, the approximate high-frequency model becomes as shown in Fig. 4.23, where $C_{b'e}$ is in parallel with $C_{b'c}$.

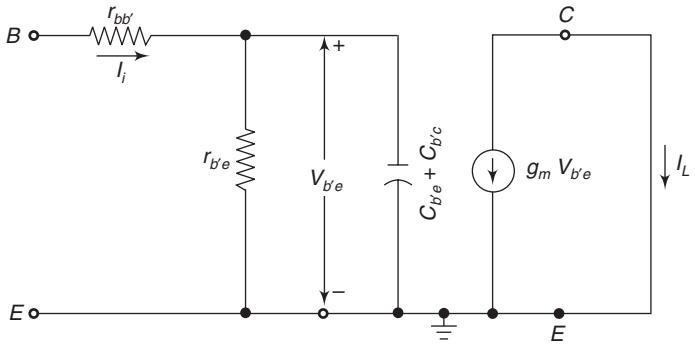



**Fig. 4.23** *Approximate high-frequency circuit for determination of short-circuit current gain*

The short-circuit current gain is given by

$$A_i = \frac{I_L}{I_i}$$

From the circuit of Fig. 4.23,

$$I_L = -g_m V_{b'e}$$

$$I_i = \frac{V_{b'e}}{r_{b'e} \parallel (-jX_C)}$$

$$= \frac{V_{b'e}}{r_{b'e} \parallel \dfrac{-j}{\omega(C_{b'e} + C_{b'c})}}$$

$$= \frac{\dfrac{V_{b'e}}{\dfrac{-jr_{b'e}}{\omega(C_{b'e} + C_{b'c})}}}{r_{b'e} - \dfrac{j}{\omega(C_{b'e} + C_{b'c})}}$$

$$= \frac{\dfrac{V_{b'e}}{\dfrac{-j(r_{b'e})^2 f_\beta}{f}}}{r_{b'e} - \dfrac{jr_{b'e} f_\beta}{f}} \qquad \left[\text{Let } f_\beta = \frac{1}{2\pi r_{b'e}(C_{b'e} + C_{b'c})}\right]$$

$$= \frac{V_{b'e}}{\dfrac{-jr_{b'e} f_\beta}{f - j f_\beta}}$$

Current gain,

$$A_I = \frac{-g_m V_{b'e}}{\dfrac{V_{b'e}}{\dfrac{-jr_{b'e}f_\beta}{f - j f_\beta}}} = \frac{jg_m r_{b'e} f_\beta}{f - j f_\beta}$$

$$= \frac{jh_{f_e} f_\beta}{f - j f_\beta}$$

$$= \frac{h_{fe} f_\beta}{-(f_\beta + jf)}$$

$$A_I = \frac{-h_{fe}}{1 + j\dfrac{f}{f_\beta}} \tag{4.36}$$

where $$f_\beta = \frac{1}{2\pi r_{b'e}(C_{b'e} + C_{b'c})}$$ is the $\beta$ cut-off frequency. (4.37)

## 4.10 CUT OFF FREQUENCY – $f_\alpha$, $f_\beta$ AND UNITY GAIN BANDWIDTH

### 4.10.1 $\beta$ Cut-off Frequency

The $\beta$ cut-off frequency $f_\beta$, also referred to as $f_{h_{fe}}$, is the CE short-circuit small-signal forward-current-transfer-ratio cut-off frequency.

Here, $f_\beta$ is the frequency at which a transistor's CE short-circuit current gain drops 3 dB from its value at lower (mid) frequencies. $f_\beta$ represents the maximum attainable bandwidth for the current gain of a CE amplifier with a given transistor.

### 4.10.2 $\alpha$ Cut-Off Frequency

A CB amplifier has a much higher 3 dB frequency than a CE amplifier. The short-circuit current gain for CB amplifier which can be derived from the approximate high-frequency circuit of the CB amplifier with output shorted is given by

$$A_i = \frac{I_L}{I_i} = \frac{-h_{fb}}{1 + j\left(\dfrac{f}{f_\alpha}\right)} \tag{4.38}$$

where $$f_\alpha = \frac{1}{2\pi r_{b'e}(1 + h_{fb})C_{b'e}} \approx \frac{h_{fe}}{2\pi r_{b'e} C_{b'e}}$$ (4.39)

Substituting Eq. (4.37) in Eq. (4.39),

$$f_\alpha = \frac{h_{fe} f_\beta (C_{b'e} + C_{b'c})}{C_{b'e}} \tag{4.40}$$

$f_\alpha$ is the '$\alpha$' (alpha) cut-off frequency at which the CB short-circuit small-signal forward-current transfer ratio ($A_i$) drops 3 dB from its value at low frequencies (≈ 1 kHz). Figure 4.24 shows the variation of $A_i$ with frequency for CE and CB amplifiers and $f_\alpha$ and $f_\beta$.

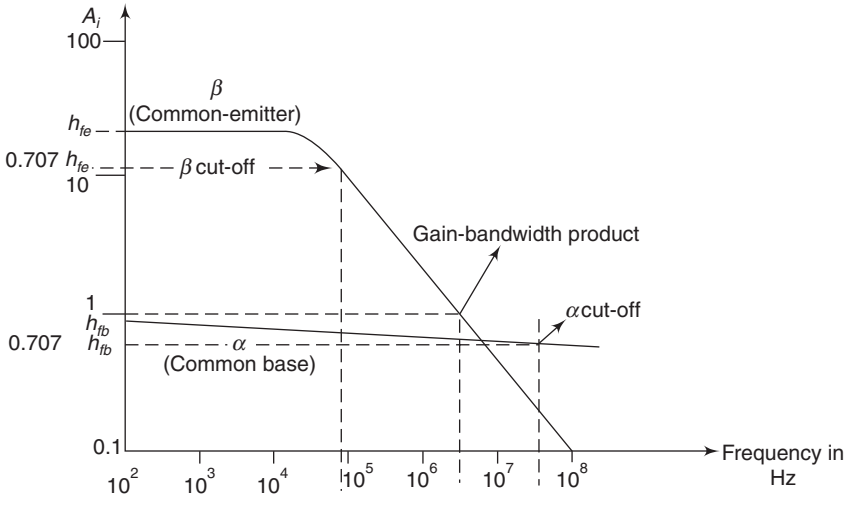



**Fig. 4.24** *Variation of $A_i$ with frequency for CE and CB amplifiers*

## 4.10.3 Gain-Bandwidth Product

$f_\alpha$ and $f_\beta$ defined in the last section gives an idea about the high-frequency capability of a transistor. An even more important characteristic is $f_T$, which is defined as the frequency at which the short-circuit common-emitter current gain has a magnitude of unity.

From Eq. (4.36), $$|A_i| = \frac{h_{fe}}{\sqrt{1 + (f/f_\beta)^2}} \tag{4.41}$$

and at $f = f_T$, $|A_i| = 1$

From Fig. 4.17, $f_T$ is less than $f_\alpha$ but much greater than $f_\beta$ and $\left(\frac{f_T}{f_B}\right)^2 >> 1$.

Hence, Eq. (4.41) reduces to

$$1 \approx \frac{h_{fe}}{\frac{f_T}{f_\beta}}$$

Then $$\frac{f_T}{f_\beta} \approx h_{fe} \tag{4.42}$$

$$f_T \approx h_{fe} f_\beta \tag{4.43}$$

Here, $f_T$ is the product of low-frequency current gain '$h_{fe}$' and $\beta$ cut-off frequency, $f_\beta$, or CE bandwidth.

Similarly, it can be proved that

$$f_T \approx h_{fb} f_\alpha \tag{4.44}$$

Value of $f_T$ range from 1 MHz for audio transistor up to 1 GHz for high-frequency transistors. Typical values of $f_\beta, f_\alpha$, and $f_T$ are 0.36 MHz, 95.9 MHz and 80.63 MHz.

Substituting for $f_\beta$ from Eq. (4.37) in (4.43),

$$f_T = h_{fe} \frac{1}{2\pi r_{b'e}(C_{b'e} + C_{b'e})} = \frac{h_{fe}}{r_{b'e}} \times \frac{1}{2\pi(C_{b'e} + C_{b'c})}$$

$$= \frac{g_m}{2\pi(C_{b'e} + C_{b'c})} \tag{4.45}$$

Since $C_{b'c} >> C_{b'e}$,

$$f_T \approx \frac{g_m}{2\pi C_{b'e}} \text{ or } C_{b'e} = \frac{g_m}{2\pi f_T}$$

Substituting $f_\beta = \frac{f_T}{h_{fe}}$ in Eq. (4.36),

$$A_i = \frac{-h_{fe}}{1 + jh_{fe}\left(\frac{f}{f_T}\right)} \tag{4.46}$$

This equation shows the dependence of the transistor's short-circuit current gain on the transistor's gain at low frequencies "$h_{fe}$" and the high-frequency characteristics "$f_T$".

## EXAMPLE 4.11

A BJT has $g_m$ = 38 mhos, $r_{b'e}$ = 5.9 kΩ, $h_{ie}$ = 6 kΩ, $r_{bb'}$ = 100 Ω, $C_{b'c}$ = 12 pF, $C_{b'e}$ = 63 pF, and $h_{fe}$ = 224 at 1 kHz. Calculate $\alpha$ and $\beta$ cut-off frequencies and $f_T$.

**Solution**

$$f_\alpha \approx \frac{h_{fe}}{2\pi r_{b'e} C_{b'e}} = \frac{224}{2\pi \times 5.9 \times 10^3 \times 63 \times 10^{-12}} = 95.9 \text{ MHz}$$

$$f_\beta = \frac{1}{2\pi r_{b'e}(C_{b'e} + C_{b'c})} = \frac{1}{2\pi \times 5.9 \times 10^3 \times (63 \times 10^{-12} + 12 \times 10^{-12})} = 0.359 \text{ MHz}$$

$$f_T = \frac{g_m}{2\pi(C_{b'e} + C_{b'c})} = \frac{38 \times 100^{-3}}{2\pi(63 \times 10^{-12} + 12 \times 10^{-12})} = 80.63 \text{ MHz}$$

## EXAMPLE 4.12

A certain BJT transistor has $r_\pi$ = 2 kΩ and $\beta$ = 100 at 1 MHz and $\beta$ = 5 at 20 MHz. Determine the value of $f_T, f_\beta$, and $C_\pi$.

**Solution** We know that $f_T = \beta f_\beta$

or $$f_T = 5 \times 20 \times 10^6 = 100 \text{ MHz}$$

Therefore, $$f_\beta = \frac{f_T}{\beta} = \frac{100 \times 10^6}{100} = 1 \text{ MHz}$$

We know that $$f_\beta = \frac{1}{2\pi C_\pi r_\pi}$$

$$1 \times 10^6 = \frac{1}{2\pi C_\pi \times 2 \times 10^3}$$

Hence, $$C_\pi = \frac{1}{2\pi \times 2 \times 10^3 \times 1 \times 10^6} = 80 \text{ pF}$$

## 4.11 HIGH-FREQUENCY CURRENT GAIN WITH RESISTIVE LOAD

With a resistive load connected in the output, the high-frequency equivalent circuit of a CE transistor amplifier is shown in Fig. 4.25.

By using Miller's theorem, the circuit of Fig. 4.25 can be modified as described below.

From Fig. 4.25, the voltage gain,

$$A = \frac{V_{CE}}{V_{b'e}} = \frac{-g_m V_{b'e} R_L}{V_{b'e}} = -g_m R_L$$

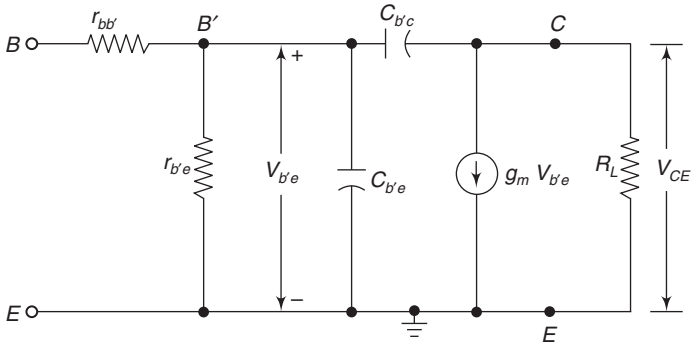



**Fig. 4.25** *High-frequency equivalent circuit with resistive load*

$$1 - A = 1 - (-g_m R_L) = 1 + g_m R_L$$

Since the impedance at the input gets decreased by a factor of $(1 - A)$, the capacitance will be increased by a factor of $(1 - A)$ or $1 + g_m R_L$.

The capacitance that is to be included in the output circuit will not make any significant change in the performance and may be neglected. This results in the modified equivalent circuit of Fig. 4.26.

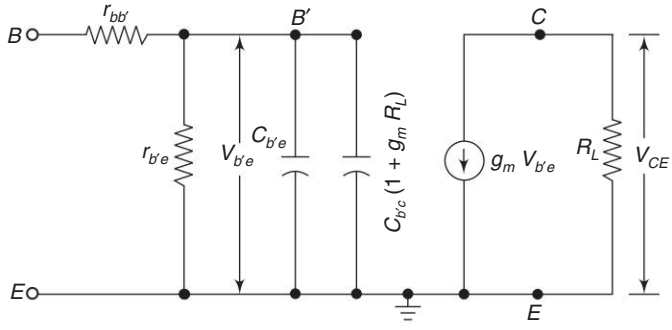



**Fig. 4.26** *Modified equivalent circuit*

The total input capacitance between $B'$ and $E$ is

$$C = C_{b'e} + (1 + g_m R_L) C_{b'c} \tag{4.47}$$

Since the circuit of Fig. 4.26 is essentially the same as that of Fig. 4.23, Eq. (4.37) can be used to find the upper 3 dB frequency. Hence, the upper dB frequency,

$$f_2 = \frac{1}{2\pi r_{b'e} C} \tag{4.48}$$

As $C$ has an increased value, $f_2$ is appreciably lower than that calculated for $f_\beta$.

***Effect of Source Resistance on Frequency Response*** If the effect of source resistance $R_s$ is also taken into account, the upper 3 dB frequency $f_2$ is given by

$$f_2 = \frac{1}{2\pi R' C} \tag{4.49}$$

where $$R' = (R_s + r_{bb'}) \parallel r_{b'e}$$

$$= \frac{(R_s + r_{bb'}) r_{b'e}}{R_s + r_{bb'} + r_{b'e}} = \frac{(R_s + r_{bb'}) r_{b'e}}{R_s + h_{ie}}$$

and $C$ is the total input capacitance given by

$$C = C_{b'e} + (1 + g_m R_L)\, C_{b'c}$$

If the effect of biasing resistors $R_1$ and $R_2$ are also taken into account then

$$R' = \frac{(R'_s + r_{bb'}) r_{b'e}}{R'_s + h_{ie}} \tag{4.50}$$

where $$R'_s = R_s \parallel R_B \quad \text{and} \quad R_B = R_1 \parallel R_2$$

Thus, the source and biasing resistors have a strong influence in determining the upper 3 dB frequency $f_2$.

## EXAMPLE 4.13

Consider a cascode amplifier with transistor and the circuit parameters are $r_\pi = 2$ kΩ, $g_m = 0.05$ Ω, $\beta = 100$, $C_\pi = 19.5$ pF, $C_\mu = 0.5$ pF, $R_s = 300$ Ω, and $R_C = 1.5$ kΩ. Determine $f_H$ and mid-band gain $G$ of cascode amplifier and CE amplifier.

**Solution** Here, $R_s' = R_s \parallel r_\pi = 300 \parallel 2000 = 260$ Ω.

*For cascode amplifier*

We know that $$\omega_H = \frac{1}{R_s'(C_\pi + 2C_\mu)}$$

Here, $$C_\pi + 2C_\mu = 19.5 + 2 \times 0.5 = 20.5 \text{ pF}$$

Therefore, $$f_H = \frac{\omega_H}{2\pi} = \frac{1}{2\pi \times R_s'(C_\pi + 2C_\mu)} = \frac{1}{2\pi \times 260 \times (20.5 \times 10^{-12})} \approx 30 \text{ MHz}$$

The mid-band gain,

$$G = \frac{R_C \beta}{r_\pi} = \frac{1.5 \times 10^3 \times 100}{2 \times 10^3} = 75$$

*For CE amplifier*

Considering the CE amplifier with same transistor and gain, $G = 75$

$$C_T = C_\pi + GC_\mu = 19.5 \times 10^{-12} + 75 \times 0.5 \times 10^{-12} = 57 \text{ pF}$$

$$f_H = \frac{1}{2\pi R_s' C_T} = \frac{1}{2\pi \times 0.26 \times 10^3 \times 57 \times 10^{-12}} = 10.7 \text{ MHz}$$

It is inferred that with the same mid-band gain, the cascade configuration has a bandwidth three times that of CE configuration.

## EXAMPLE 4.14

A BJT transistor amplifier shown in Fig. 4.27 has $R_E = R_C = 1$ kΩ, $R_S = 600$ Ω, $R_L = 2$ kΩ, and transistor parameters as $\beta = 100$ and $r_\pi = 1$ kΩ. Determine the values of $C_{C1}$, $C_{C2}$ and $C_E$ needed to obtain $f_L = 50$ Hz.

**Solution**

$$\omega_{1p} = 2\pi f_L = 100\,\pi \text{ rad/s}$$

We know that $$\omega_{1p} = \frac{1}{C_E'(R_s + r_\pi)},$$

Therefore, $$C_E' = \frac{1}{\omega_{1p}(R_s + r_\pi)}$$

$$C_E' = \frac{1}{100\,\pi \times 1.6} = 1.99\ \mu\text{F}$$

We know that $$C_E = (1 + \beta)C_E'$$

$$C_E = 101 \times 1.99 \times 10^{-6} = 201\ \mu\text{F}$$

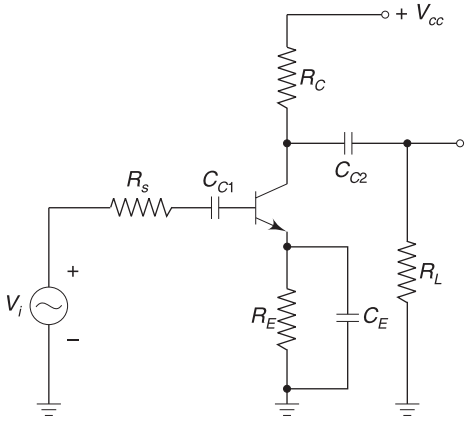



**Fig. 4.27**

We know that $$\omega_{1l} = \frac{\omega_{1p}}{10} = \frac{100\,\pi}{10} = 10\,\pi = \frac{1}{(R_s + R_\pi)C_{C1}}$$

$$C_{C1} = \frac{1}{10\pi \times 1.6} = 19.9\ \mu\text{F}$$

We choose $$\omega_{12} = \frac{\omega_{1p}}{20} = \frac{100\,\pi}{20} = 5\pi$$

Therefore, $$\omega_{12} = 5\pi = \frac{1}{(R_C + R_L)C_{C2}}$$

Hence, $$C_{C2} = \frac{1}{\omega_{12}\,(R_C + R_L)} = \frac{1}{5\pi \times 3 \times 10^3} = 21.23\ \mu\text{F}$$

Since $\omega_{12}$ is inversely proportional to $C_{C2}$, we can choose any value $C_{C2} > 21.23\ \mu$F. Hence, let us choose $C_{C2} = 22\ \mu$F.

## EXAMPLE 4.15

A silicon BJT small-signal amplifier shown in Fig. 4.28 has the circuit parameters as follows:

$$V_{CC} = 10\text{ V},\ R_1 = 11.5\ \text{k}\Omega,\ R_2 = 41.4\ \text{k}\Omega,\ R_C = 5\ \text{k}\Omega,\ R_E = 1\ \text{k}\Omega$$

$$R_s = 1\ \text{k}\Omega,\ C_E = 150\ \mu\text{F},\ C_{C1} = C_{C2} = 20\ \mu\text{F and } \beta = 50$$

$$C_\pi = 100\ \text{pF},\ C_\mu = 5\ \text{pF},\ C_W + C_L = 5\ \text{pF and } R_L = 10\ \text{k}\Omega.$$

Determine (a) dc bias values, (b) mid-frequency gain, (c) low-frequency cut-off and (d) high-frequency cut-off.

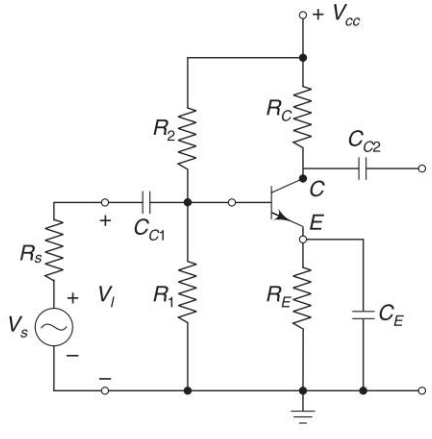



**Fig. 4.28**

**Solution**

*(a) To determine dc bias values*

$$R_B = R_1 \parallel R_2 = 11.5 \times 10^3 \parallel 41.4 \times 10^3 = 9\ \text{k}\Omega$$

$$V_{BB} = \frac{R_1}{R_1 + R_2} V_{CC} = \frac{11.5 \times 10^3}{(11.5 + 41.4) \times 10^3} \times 10 = 2.174 \text{ V}$$

$$I_B = \frac{V_{BB} - 0.7}{R_B + R_E (1 + \beta)} = \frac{2.174 - 0.7}{9 \times 10^3 + 1 \times 10^3 \times 51} \approx 0.0246 \text{ mA}$$

$$I_C = \beta I_B = 50 \times 0.0246 \times 10^{-3} = 1.23 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C - (I_C + I_B) R_E$$

$$= 10 - 1.23 \times 10^{-3} \times 5 \times 10^3 - (1.23 + 0.0246) \times 10^{-3} \times 1 \times 10^3 = +2.595 \text{ V}$$

*(b) To determine mid-frequency gain*

The mid-frequency circuit model is shown in Fig. 4.29.

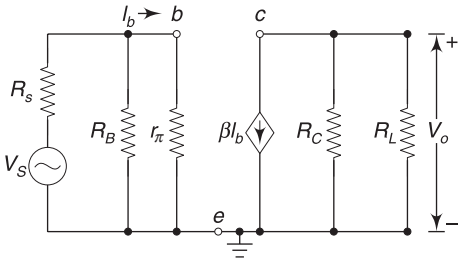



**Fig. 4.29**

Assume $V_s = 1 \text{ V}$

$$r_\pi = \frac{25\beta}{I_C \text{ (mA)}} = \frac{25 \times 50}{1.23} = 1 \text{ k}\Omega$$

$$V_{be} = \frac{V_s \times (R_B \parallel r_\pi)}{R_s + (R_B \parallel r_\pi)}$$

$$R_B \parallel r_\pi = \frac{9 \times 10^3 \times 1 \times 10^3}{9 \times 10^3 + 1 \times 10^3} = 0.9 \text{ k}\Omega$$

Given $R_s = 1 \text{ k}\Omega$

Therefore, $$V_{be} = \frac{1 \times 0.9 \times 10^3}{(1 + 0.9) \times 10^3} = 0.474 \text{ V}$$

$$I_b = \frac{V_{be}}{r_\pi} = \frac{0.474}{1 \times 10^3} = 0.474 \text{ mA}$$

$$\beta I_b = 50 \times 0.474 \times 10^{-3} = 23.7 \text{ mA}$$

$$R_o = R_C \parallel R_L = 5 \times 10^3 \parallel 10 \times 10^3 = \frac{10}{3} \text{ k}\Omega$$

$$V_o = -\beta I_b R_o = -23.7 \times 10^3 \times \frac{10}{3} \times 10^3 = -79 \text{ V}$$

$$A_{Vo} = \frac{V_o}{V_s} = -79$$

*(c) To determine low-frequency cut-off*

$$\omega_{11} = \frac{1}{C_{C1}[R_s + (r_\pi \parallel R_B)} = \frac{1}{20 \times 10^{-6} (1 + 0.9) \times 10^3} = 26.3 \text{ rad/s}$$

$$\omega_{12} = \frac{1}{C_{C2} (R_C + R_L)} = \frac{1}{20 \times 10^{-6} (5 + 10) \times 10^3} = 3.3 \text{ rad/s}$$

$$\omega_{1p} = \frac{1}{C_E [R_s \parallel R_B) + r_\pi]} = \frac{1}{(150/51) \times 10^{-6} \times (0.9 + 1) \times 10^3} = 179 \text{ rad/s}$$

As $\omega_{1p} > \omega_{11} > \omega_{12}$, $\omega_L = \omega_{1p} = 179$ rad/s = 28.5 Hz

*(d) To determine high-frequency cut-off*

$$\omega_{21} = \frac{1}{C_{eq}(R_s \parallel R_B \parallel r_\pi)}$$

$$\omega_{22} = \frac{1}{C_o R_o}$$

where $C_{eq} = C_\pi + C_\mu (1 + g_m R_o)$

$$C_o = C_o' + C_\mu \left(1 + \frac{1}{g_m R_o}\right)$$

where $C_o' = C_W + C_L = 5$ pF

$C_\pi = 100$ pF

$$g_m = \frac{\beta}{r_\pi} = \frac{50}{1} = 50 \text{ mS}$$

$$R_o = \frac{10}{3} \text{ k}\Omega$$

$$g_m R_o = 50 \times 10^{-3} \times \frac{10}{3} \times 10^3 = \frac{500}{3}$$

Substituting the values,

$$C_{eq} = 100 \times 10^{-12} + 5 \times 10^{-12} \left(1 + \frac{500}{3}\right) \approx 938.3 \text{ pF}$$

$$C_o = 5 \times 10^{-12} + 5 \times 10^{-12} \left(1 + \frac{3}{500}\right) \approx 10 \text{ pF}$$

$$R_s' = R_B \parallel R_s = 9 \times 10^3 \parallel 1 \times 10^3 = 0.9 \text{ k}\Omega$$

$$R_s' \parallel r_\pi = 0.9 \times 10^3 \parallel 1 \times 10^3 = 0.474 \text{ k}\Omega$$

Therefore, $$\omega_{21} = \frac{1}{C_{eq}(R_s \parallel R_B \parallel r_\pi)}$$

$$= \frac{1}{938.3 \times 10^{-12} \times 0.474 \times 10^3} = 2.25 \times 10^6 \text{ rad/s or } 0.358 \text{ MHz}$$

$$\omega_{22} = \frac{1}{C_o R_o} = \frac{1}{10 \times 10^{-12} \left(\frac{10}{3}\right) \times 10^3} = 30 \times 10^6 \text{ rad/s or } 4.77 \text{ MHz}$$

Thus, $\omega_H = 0.358$ MHz, since $f_{21} < f_{22}$.

## EXAMPLE 4.16

An *RC* coupled amplifier has equal input and output-circuit corner frequencies in the high-frequency band as given by

$$\omega_{21} = \omega_{22} = \omega_2 = 250 \times 10^3 \text{ rad/s}$$

Calculate the cut-off frequency of this band.

**Solution**

$$A_{VH} = \frac{A_{V0}}{1 + j(\omega/\omega_2)}$$

$$|A_{VH}| = \frac{A_{V0}}{\sqrt{1 + j(\omega/\omega_2)}}$$

The gain at 3 dB cut-off frequency is $1/\sqrt{2}$ of its mid-frequency gain. Therefore,

$$A_{VH}(\omega_H) = \frac{A_{V0}}{\sqrt{1 + (\omega_H/\omega_2)^2}} = \frac{A_{V0}}{\sqrt{2}}$$

Solving for $\omega_H$, we have

$$\omega_H = \omega_2 = 250 \times 10^3 \text{ rad/s}$$

## 4.12 MILLER EFFECT

***Miller's Theorem*** Miller's theorem states that if an impedance $Z$ is connected between the input and output terminals of a network which provides a voltage gain $A$, an equivalent circuit that gives the same effect can be drawn by removing $Z$ and connecting an impedance $Z_i = \frac{Z}{1+A}$ across the input and $Z_o = \frac{Z}{1-\frac{1}{A}} = \frac{ZA}{A-1}$ across the output as shown in Fig. 4.30.

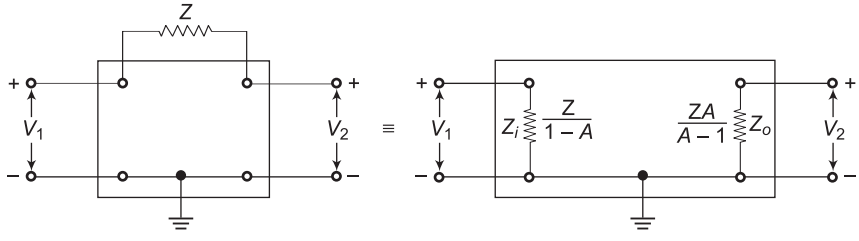



**Fig. 4.30** *Miller's theorem*

***Miller-Effect Capacitance*** In inverting amplifiers, the capacitive element, $C_f$ is connected between input and output terminals of the active device, i.e., $X_{C_f} = \frac{1}{j\omega C_f}$. The large capacitors will control the low-frequency response due to their low reactance levels.

Therefore, the Miller-effect input capacitance $C_{Mi}$, is derived as

$$Z_i = \frac{Z}{(1-A)}$$

i.e., $$\frac{1}{j\omega C_{Mi}} = \frac{1}{j\omega C_f (1-A)}$$

Therefore, $$C_{Mi} = (1-A)C_f$$

Hence, it is evident that, in any inverting amplifier, the input capacitance will be increased by a Miller effect capacitance sensitive to the gain of the amplifier and the interelectrode capacitance, $C_f$, between the input and output terminals of the active device.

The Miller output capacitance, $C_{Mo}$ is derived as

$$Z_o = \frac{Z}{\left(1-\frac{1}{A}\right)}$$

i.e., $$\frac{1}{j\omega C_{Mo}} = \frac{1}{j\omega C_f \left(1-\frac{1}{A}\right)}$$

Therefore, $$C_{Mo} = \left(1-\frac{1}{A}\right) C_f$$

If $A >> 1$, $C_{Mo} = C_f$.

***Dual of Miller's Theorem*** The dual of Miller's theorem states that if an impedance $Z$ connected as shunt element between input and output terminals, as shown in Fig. 4.31(a) can be replaced by an impedance $Z_i = Z(1 - A_I)$ at the input side and $Z_o = Z\left(1-\frac{1}{A_I}\right) = Z\frac{(A_I - 1)}{A_I}$ at the output side. Where the current ratio, $A_I = \frac{I_2}{I_1}$. This can be verified by finding that the voltage across $Z_i$ is $I_1 Z_i$ which is equal to the voltage drop $(I_1 + I_2)Z$ across $Z$ if $Z_i = Z(1 - A_I)$. Hence, the input voltage $V_i$ is the same in the two circuits in Fig. 4.31(a) and (b).

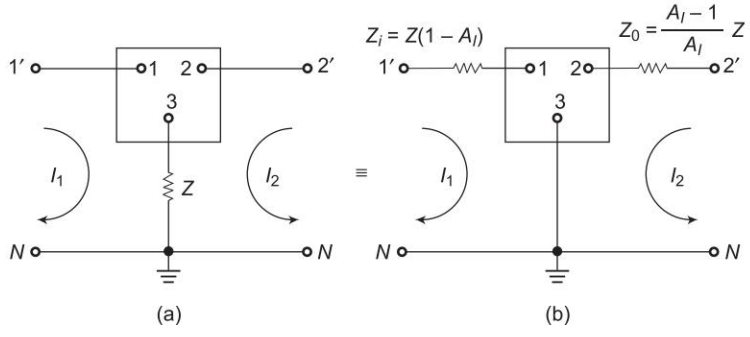



**Fig. 4.31** *Dual of Miller's theorem*

Similarly, the voltage $V_2$ has the same value in the two circuits if the impedance $Z_o = \left[\frac{A_I - 1}{A_I}\right] Z$. Therefore, the two networks are identical. This transformation is useful in the analysis of electric circuits.

## 4.13 FET MODEL AT HIGH FREQUENCY

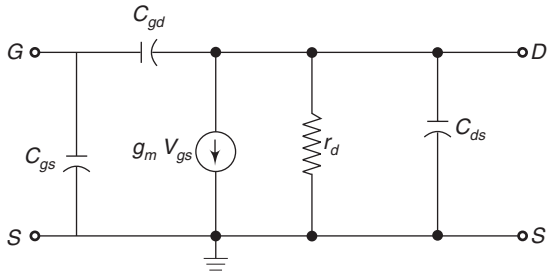



**Fig. 4.32** *The high-frequency model of FET*

In the high-frequency model of FET, the capacitances between nodes have to be added in the low-frequency model. The resulting equivalent circuit is shown in Fig. 4.32.

Here, $C_{gs}$ represents the barrier capacitance between gate and source. $C_{gd}$ is the barrier capacitance between gate and drain. $C_{ds}$ is the drain-to-source capacitance of the channel. These interval capacitances leads to feedback from output to input and the voltage amplification decreases at higher frequencies.

The parameters of FET shown in Fig. 4.32 will have their magnitudes as given in Table 4.3.

**Table 4.3** *Parameter values of FET*

| Parameter | $g_m$ | $r_d$ | $c_{ds}$ | $C_{gs}$, $C_{gd}$ | $r_{gs}$ | $r_{gd}$ |
|---|---|---|---|---|---|---|
| Range | 0.1 – 10 mA/V | 0.1 – 1 MΩ | 0.1 – 1 pF | 1 – 10 pF | $>10^8$ Ω | $>10^8$ Ω |

## 4.14 HIGH FREQUENCY ANALYSIS OF FET CS AMPLIFIER

The circuit of Fig. 4.33 shows the CS amplifier.

The equivalent circuit at high frequencies is shown in Fig. 4.35.

The Norton's equivalent circuit between $D$ and $S$ can be obtained by finding the short-circuit current from $D$ to $S$ and impedance $Z$ seen from output point with independent voltage sources short-circuited and independent current sources open-circuited. With $V_i = 0$, current $g_m V_i = 0$, the circuit of Fig. 4.34 reduces to circuit of Fig. 4.35.

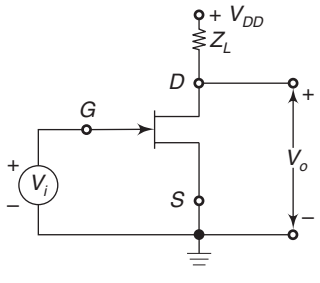



**Fig. 4.33** *CS amplifier circuit*

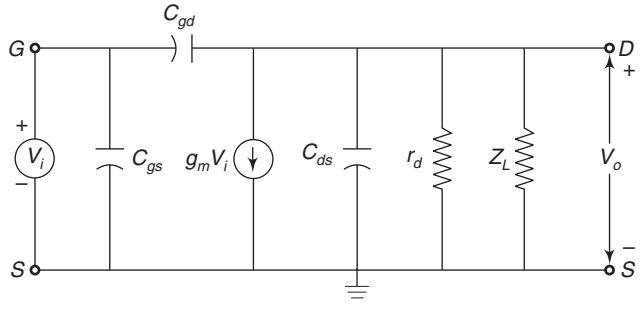



**Fig. 4.34** *Small-signal equivalent circuit of a CS amplifier at high frequencies*

Hence, admittance at the output point

$$Y = \frac{1}{Z} = Y_L + g_d + Y_{ds} + Y_{gd} \qquad (4.51)$$

where $Y_L = \dfrac{1}{Z_L}$ is admittance corresponding to $Z_L$

$g_d = \dfrac{1}{r_d}$ is conductance corresponding to $r_d$

$Y_{ds} = j\omega C_{ds}$ is admittance corresponding to $C_{ds}$

$Y_{gd} = j\omega C_{gd}$ is admittance corresponding to $C_{gd}$.

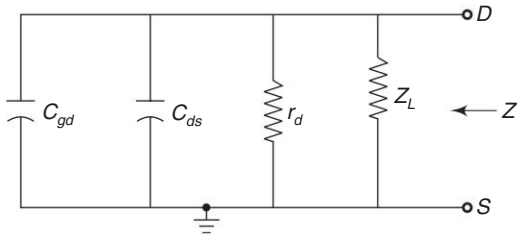



**Fig. 4.35** *Equivalent circuit to find Z*

The equivalent circuit to find the short-circuit current from $D$ to $S$ is shown in Fig. 4.36.

Hence, current $$I = -g_m V_i + V_i Y_{gd} \qquad (4.52)$$

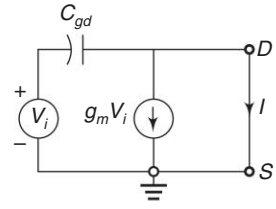



**Fig. 4.36** *Equivalent circuit to find I*

***Voltage Gain, $A_V$*** Voltage gain (amplification) $A_V$ with load $Z_L$ included is given by

$$A_V = \frac{V_o}{V_i} = \frac{IZ}{V_i} = \frac{I}{V_i Y}$$

From Eqs (4.51) and (4.52),

$$A_V = \frac{-g_m + Y_{gd}}{Y_L + g_d + Y_{ds} + Y_{gd}} \qquad (4.53)$$

At low frequencies, FET capacitances can be neglected and hence,

$$Y_{ds} = Y_{gd} = 0$$

Equation (4.53) at low frequencies reduces to

$$A_V = \frac{-g_m}{Y_L + g_d} = \frac{-g_m}{\dfrac{1}{Z_L} + \dfrac{1}{r_d}}$$

$$A_V = \frac{-g_m r_d Z_L}{r_d + Z_L} = -g_m Z_L' \qquad (4.54)$$

where $Z' = Z_L \parallel r_d$

***Input Admittance*** From Fig. 4.34, it is found that the gate circuit is not isolated from the drain circuit, but connected by $C_{gd}$.

According to Miller's theorem, an impedance $Z'$ connected between the input and output terminals of a circuit can be replaced by $Z_L = \dfrac{Z'}{1 - A_V}$ from the input terminal to ground and $Z_2 = \dfrac{Z' A_V}{A_V - 1}$ from the output terminal to ground, where $A_V$ is the voltage gain $V_2/V_1$.

Applying Miller's theorem to the circuit of Fig. 4.34, the circuit of Fig. 4.37 is obtained, where capacitances are replaced by equivalent admittances.

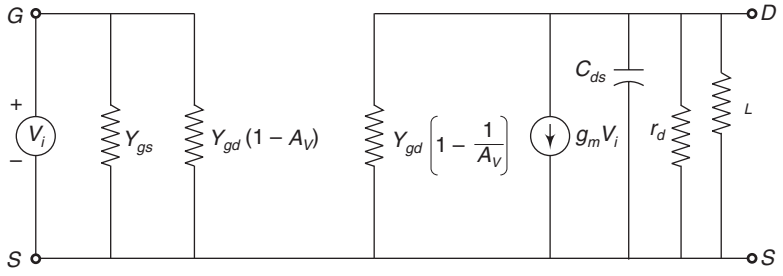



**Fig. 4.37** *CS amplifier equivalent circuit after applying Miller's theorem*

Hence, the input admittance is given by

$$Y_i = Y_{gs} + (1 - A_V)Y_{gd} \tag{4.55}$$

As $Y_{gs} = j\omega C_{ds}$ and $Y_{gd} = j\omega C_{gd}$ for an FET to possess negligible input admittance over a wide range of frequencies, the gate-source and gate-drain capacitances must be negligible.

***Input Capacitance (Miller Effect)*** From Eq. (4.54), the voltage gain $A_V = -g_m Z'_L$ where $Z'_L = Z_L \| r_d$. For an FET with drain-circuit resistance $R_d$, the voltage gain $A_V = -g_m R'_d$ where $R'_d = R_d \| r_d$.

From Eq. (4.55),

$$Y_i = Y_{gs} + (1 + g_m R'_d)\, Y_{gd}$$

$$Y_i = j\omega C_{gs} + (1 + g_m R'_d)\, j\omega C_{gd}$$

$$\frac{Y_i}{j\omega} = C_i = C_{gs} + (1 + g_m R'_d)\, C_{gd} \tag{4.56}$$

The increase in input capacitance $C_i$ over the capacitance from gate to source is the Miller effect.

In multistage (cascaded amplifiers), this input capacitance appears in shunt with the output impedance of the previous stage. As capacitive reactance decreases with increase in frequency, the resultant output impedance will be lower at higher frequencies, thereby reducing the gain.

***Output Admittance*** The output impedance for the CS amplifier of Fig. 4.35 is obtained by setting input voltage $V_i = 0$ and looking from the output point. The resulting equivalent circuit is shown in Fig. 4.38.

The output admittance with $Z_L$ considered external to the CS amplifier circuit is given by

$$Y_o = g_d + Y_{ds} + Y_{gd} \tag{4.57}$$

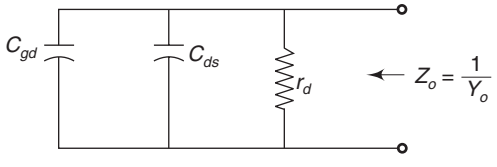



**Fig. 4.38** *Calculation of output impedance*

## 4.15 HIGH FREQUENCY ANALYSIS OF FET CD AMPLIFIER

The common-drain amplifier (source-follower) circuit is shown in Fig. 4.39 and its high-frequency equivalent circuit is shown in Fig. 4.40.

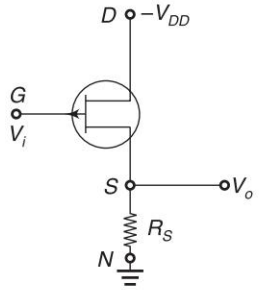



**Fig. 4.39** *Common-drain amplifier*

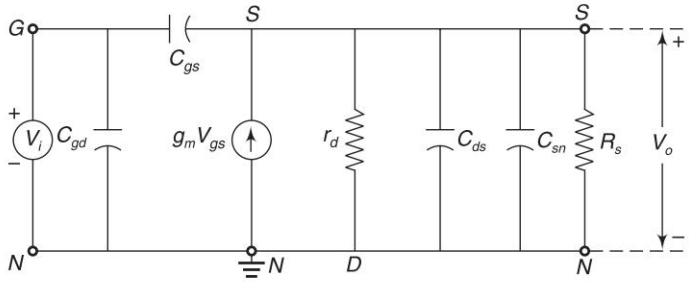



**Fig. 4.40** *Small-signal high-frequency equivalent circuit of common-drain amplifier*

The small-signal high-frequency equivalent circuit of the CD amplifier is shown in Fig. 4.40.

***Voltage Gain*** The output voltage $V_o$ is the product of the short-circuit current and the impedance between terminals $S$ and $N$. It is found to be, voltage gain

$$A_V = \frac{(g_m + j\omega C_{gs})R_s}{1 + (g_m + g_d + j\omega C_T)R_s} \tag{4.58}$$

where $C_T \equiv C_{gs} + C_{ds} + C_{sn}$

$C_{gs}$ is the capacitance from gate to source, $C_{ds}$ is the capacitance from drain to source, and $C_{sn}$ is the capacitance from source to ground.

At low frequencies, the voltage gain reduces to

$$A_V \approx \frac{g_m R_s}{1 + (g_m + g_d)R_s}$$

The amplification is positive and has a value less than unity. If $g_m R_s >> 1$, then

$$A_V \approx \frac{g_m R_s}{g_m R_s + g_d R_s} = \frac{g_m}{g_m + g_d} = \frac{\mu}{\mu + 1}$$

***Input Admittance*** The input admittance $Y_i$ is obtained by applying Miller's theorem to $C_{gs}$.

$$Y_i = j\omega C_{gd} + j\omega C_{gs}(1 - A_V)$$

$$Y_i \approx j\omega C_{gd} \text{ as } A_V \approx 1$$

The CD amplifier offers the important advantage of lower input capacitance than the CS amplifier.

***Output Admittance*** The output admittance with input voltage set to zero is given by

$$Y_o = g_m + g_d + j\omega C_T$$

where $R_s$ is considered external to the amplifier. At low frequencies, the output admittance $Y_o \approx g_m + g_d$ and output resistance $R_o = \dfrac{1}{g_m + g_d} = \dfrac{1}{g_m}$ since $g_m \gg g_d$.

The CD amplifier (source-follower) is used for the same application as the emitter follower, in applications requiring high input impedance and low output impedance.

## 4.16 FREQUENCY RESPONSE OF A FET AMPLIFIER

In the case of a FET amplifier, the high-frequency characteristic of the amplifier is determined by the interelectrode and wiring capacitances. The capacitors $C_{gs}$ and $C_{gd}$ typically vary from 1–10 pF, while the capacitances $C_{ds}$ is usually quite a bit smaller, ranging from 0.1–1 pF. At high frequencies, $C_i$ (miller capacitance) will approach a short-circuit equivalent and $V_{gs}$ will drop and in value and reduce the overall gain.

The cut-off frequencies defined by the input and output circuits can be obtained by first finding the Thevenin equivalent circuits for each section as shown in Fig. 4.41.

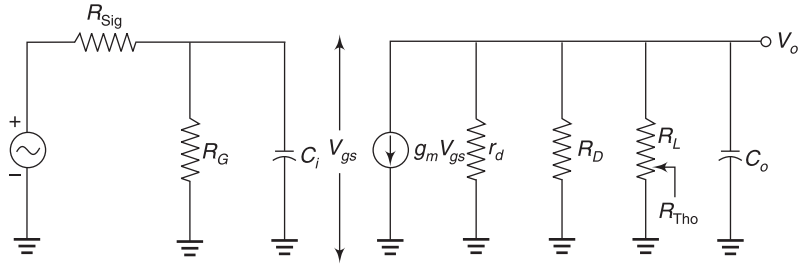



**Fig. 4.41(a)** *Modified high-frequency ac equivalent circuit (CS amplifier)*

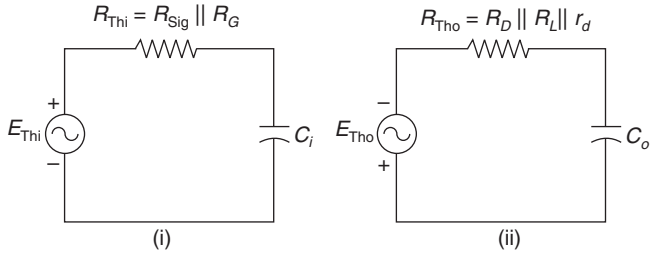



**Fig. 4.41(b)** *Thevenin equivalent circuit for (i) Input circuit, and (ii) Output circuit*

For the input circuit shown in Fig. 4.41(b),

$$f_{Hi} = 1/(2\pi R_{Thi} C_i)$$

where

$$R_{Thi} = R_{Sig} \| R_G$$

$$C_i = C_{gs} + (1 + g_m R_d) C_{gd}$$

and for the output circuit shown in Fig. 4.42(b),

$$f_{Ho} = 1/(2\pi R_{\text{Tho}} C_o)$$

where $R_{\text{Tho}} = R_D \| R_L \| r_d$

## 4.17 TRANSISTOR SWITCHING TIMES

### 4.17.1 Storage, Delay and Calculation of Transistor-Switching Times

When a pulse is applied to the input of a transistor, the output current does not directly follow the input waveform as shown in Fig. 4.42. Instead, there will always be some delay because the transistor operates from cut-off to saturation and then returns to cut-off. Figure 4.42(b) shows the waveform of the input pulse applied to the transistor and Fig. 4.42(c) shows the resulting waveform of collector current ($i_C$) along with different time delays involved.

***Delay Time ($t_d$)*** The collector current does not immediately respond to the input pulse. There is a delay and the time that elapses during this delay, together with time needed for the current to rise to 10% of its maximum (saturation) value, i.e., $I_{C(\text{sat})} = \dfrac{V_{CC}}{R_C}$ is called the delay time ($t_d$). The reason for delay is that the transistor requires a non-zero time to charge up the emitter-junction transistor capacitance in order to bring the transistor to the active region from the cut-off region.

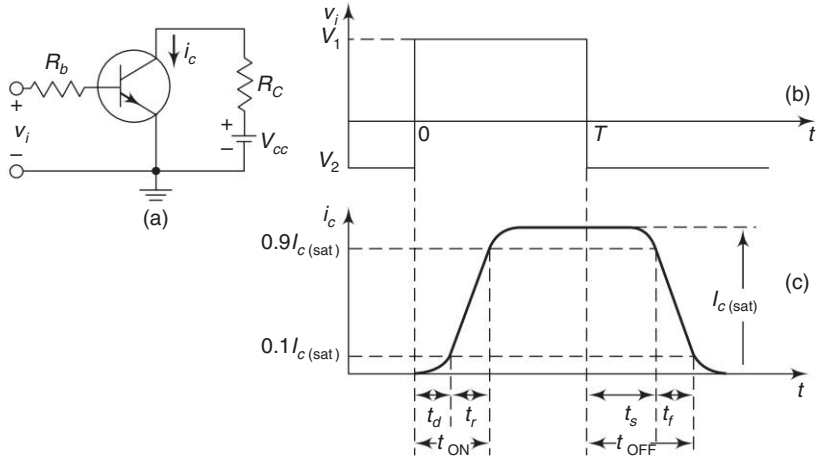



**Fig. 4.42** *(a) Transistor-switching circuit (b) Input-pulse waveform (c) Collector-current response*

***Rise Time ($t_r$)*** The time required for the collector current to rise from 10% to 90% of the maximum value is called rise time ($t_r$).

***Turn-ON Time ($t_{ON}$)*** The sum of the delay time ($t_d$) and the rise time ($t_r$) is called the turn-ON time ($t_{\text{ON}}$), i.e., $t_{ON} = t_d + t_r$

***Storage Time ($t_s$)*** When the input signal returns back to its initial state at $t = T$, the collector current again fails to respond immediately. The interval which elapses between the transition of the input voltage waveform and the time when collector current ($i_C$) dropped to 90% of its maximum value is called the storage time.

***Fall Time ($t_f$)*** The time required for the collector current to fall from 90% to 10% of its maximum value is called fall-time ($t_f$).

***Turn-off Time ($t_{OFF}$)*** The sum of the storage time ($t_s$) and the fall time ($t_f$) is called the turn-OFF time ($t_{OFF}$), i.e., $t_{OFF} = t_s + t_f$.

## 4.17.2 Switching Time Improvement

Speed-up capacitor is used to improve the switching times. If the base-emitter junction of the transistor is reverse-biased before switch-on, the delay is longer compared to the case when $V_{BE}$ is initially zero. This is because the transistor input capacitance needs to charge to the reverse-bias voltage and allowed to discharge before $V_{BE}$ becomes positive. Hence, to minimize the turn-on time, $V_{BE}$ should have a very small reverse-bias value before switch-on.

The delay time and the rise time can be reduced if the transistor is overdriven, i.e., if $I_B$ is made larger than the minimum required for saturation. With a larger $I_B$, the junction capacitance charges faster, thus reducing the turn-on time.

A major disadvantage of overdriving is that the storage time is extended by the larger current flow across the forward-biased collector-base junction when the transistor is in saturation. Hence, although an overdriven transistor will turn on faster, it will lead to a longer turn-off time than a transistor which has sufficient base current for saturation.

The turn-off time may be reduced by providing a large negative input voltage during switch-off. This produces a reverse base current flow which causes the junction capacitance to discharge rapidly. This, on the other hand, increases the turn-on time because of the initial large reverse-bias required for the base-emitter junction.

For faster switching, $V_{BE}$ preferably is to be fixed at zero volt and $I_B$ is to be made large at switch-on and it should be rapidly allowed to settle down to the minimum value required for saturation.

Additionally, switch-off should be accomplished by a large reverse-bias voltage which rapidly returns to zero. These conditions are ideally achieved when a capacitor is connected in parallel with $R_B$ as shown in Fig. 4.43. This capacitor is called a speed-up capacitor or commutating capacitor.

The speed-up capacitor tends to reduce $t_d$ and $t_s$ as well as $t_r$ and $t_f$. However, if $C$ is made very small, it becomes completely charged within the delay time and hence it will not have any effect on rise time. Similarly, if $C$ is totally discharged during the storage time, it will not result in a significant improvement of the fall time.

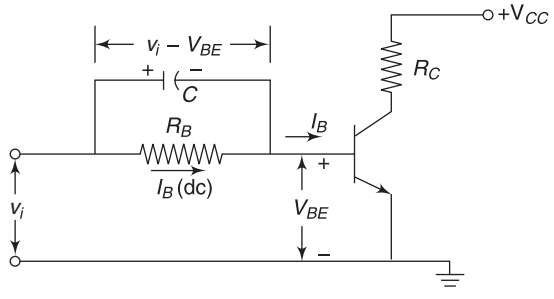



**Fig. 4.43** *Transistor circuit with the speed-up capacitor*

***Calculation of the Speed-up Capacitor*** The capacitor charging current drops by 10% from its maximum level with the capacitor is permitted to charge by 10% during the turn-on time. We know that $C$ charges by 10% during the time of 0.1 $R_S C$. Hence, $t_{on} = 0.1\ R_S C$, i.e., $C = \dfrac{t_{on}}{0.1\ R_s}$.

The maximum value of $C$ is dependent on the maximum frequency of the signal. When the transistor is switched off, $C$ discharges through $R_B$. For perfect switching, $C$ must be at least 90% discharged during the time interval between transistor switch-off and switch-on. Therefore, the time needed for the capacitor to return to its discharged condition is called settling time or the recovery time $t_{re}$ of the circuit. Here, the transistor is off and the capacitor discharges through $R_B$ by 90% in a time $t = 2.3\ R_B C$.

Therefore, $t_{re} = 2.3\ R_B C$ (or) maximum $C = \dfrac{t_{re}}{2.3\ R_B}$.

## EXAMPLE 4.17

An inverter circuit using 2N3904 transistor with $t_{on}$ = 70 ns has $R_s$ = 600 Ω and $R_B$ = 5.6 kΩ. Determine the size of the speed-up capacitor to give maximum improvement in transistor turn-on-time. Also find the maximum square wave input frequency that may be used with the circuit.

**Solution** Given $t_{on} = 70$ ns

$$C = \frac{t_{on}}{0.1 \times R_s} = \frac{70 \times 10^{-9}}{0.1 \times 600} = 1167 \text{ pF} \approx 1200 \text{ pF}$$

$$t_{re} = 2.3\ R_B C = 2.3 \times 5.6 \times 10^3 \times 1200 \times 10^{-12} = 15\ \mu\text{s}$$

$$f = \frac{1}{2T} = \frac{1}{2t_{re}} = \frac{1}{2 \times 15 \times 10^{-6}} = 33.33 \text{ kHz}$$

# REVIEW QUESTIONS

1. What is the significance of logarithmic scale?
2. Define "bel" and "decibel".
3. What is dBm?
4. How is half-power bandwidth calculated?
5. Explain in detail about logarithms and decibels.
6. What are half-power frequencies?
7. "The cut-off frequencies of single-stage amplifiers are influenced by RC combinations." Justify the statement.
8. How does time constant '$\tau$' and rise time '$t_r$' influence the bandwidth of amplifiers.
9. Discuss the effect of emitter bypass capacitor on low-frequency response of BJT amplifiers.
10. Explain the effect of coupling capacitor on low-frequency response of BJT amplifiers.
11. Draw the high-frequency $\pi$ model of a transistor and explain it.
12. Derive the expression for CE short-circuit current gain as a function of frequency and hence, define the $\alpha$ and $\beta$ cut-off frequencies.
13. Derive the expression for 3 dB upper cut-off frequency of emitter follower with the help of its equivalent circuit.
14. Calculate the 3 dB upper cut-off frequency $f_H$ of BJT emitter follower as shown in Fig. 4.30, whose parameters are $C_{b'e}$ = 35 pF, $C_{b'c}$ = 4 pF, $g_m$ = 39.2 mmho, $\beta$ = 150, $R_s$ = 100 Ω, $r_{b'e}$ = 3.82 kΩ.

[*Ans.* $f_H = 281$ MHz]

**15.** Derive the relationship between low-frequency *h*-parameters and high-frequency hybrid π parameters for a transistor in CE configuration.

**17.** Explain how the source resistance influence the frequency response of amplifiers.

**18.** Draw the equivalent circuit of common-source amplifier at high frequencies and derive expressions for voltage gain, input admittance, and output admittance.

**19.** Draw the equivalent circuit of common-drain amplifier (source follower) at high frequencies and derive expressions for voltage gain, input admittance, and output admittance.

**20.** What are the parameters that will influence the frequency response of FET amplifiers? Justify your answer.

**31.** Discuss in detail the Miller's theorem and its dual.

**32.** With the help of waveforms, explain the terms: (i) Delay time (ii) Rise time (iii) Turn-on time (iv) Storage time (v) Fall time and (vi) Turn-off time.

**33.** Explain how the transistor switching time can be improved using speed-up capacitor.

CHAPTER

5

# Power Supplies and Electronic Device Testing

## 5.1 INTRODUCTION

All electronic circuits need dc power supply either from a battery or power-pack units. It may not be economical and convenient to depend upon battery power supply. Hence, many electronic equipment contain circuits which convert the ac supply voltage into dc voltage at the required level. The unit containing these circuits is called the *Linear-Mode Power Supply* (LPS). In the absence of ac mains supply, the dc supply from a battery can be converted into required ac voltage which may be used by computers and other electronic systems for their operation. Also, in certain applications, dc to dc conversion is required. Such a power supply unit that converts dc into ac or dc is called *Switched-Mode Power Supply* (SMPS).

1. Linear power supply (LPS): ac/dc power supply—Converter
2. Switched mode power supply (SMPS):
   (i) dc/dc power supply—Converter
   (ii) dc/ac power supply—Inverter

An ac/dc power supply converts ac mains (230 V, 50 Hz) into required dc voltages and is found in all mains operable system.

The dc/dc power supplies or dc/dc converters are used in portable systems. The dc/ac power supplies or inverters are used in portable mains operable systems and as a supplement to ac mains in non-portable mains operable system, where a disruption in the power supply can affect the job being done by the system.

Based on the regulator concept, power supplies are classified as either ***linear or switched-mode power supply***. The main difference between LPS and SMPS is seen from their block diagrams given in Figs 18.1(a) and (b).

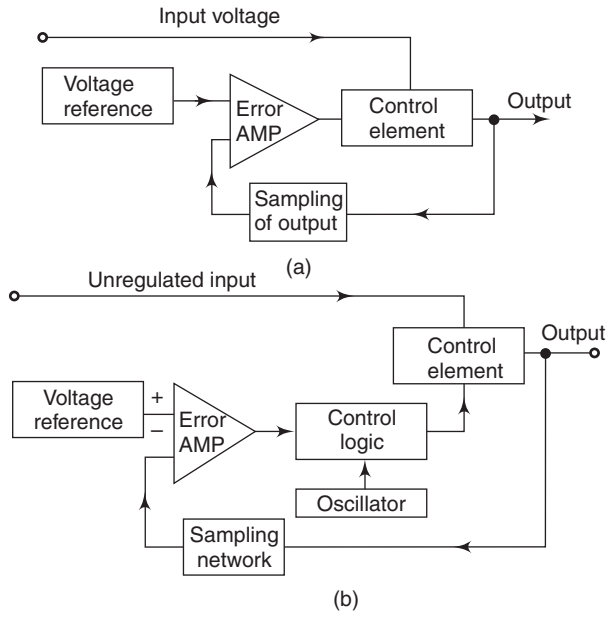



**Fig. 5.1** *(a) Principle of a normal linear mode power supply, (b) Block diagram of a switched mode power supply*

## 5.2 LINEAR MODE POWER SUPPLY

The basic building blocks of the linear power supply are shown in Fig. 5.2. A transformer supplies ac voltage at the required level. This bidirectional ac voltage is converted into a unidirectional pulsating dc using a rectifier. The unwanted ripple contents of this pulsating dc are removed by a filter to get pure dc voltage. The output of the filter is fed to a regulator which gives a steady dc output independent of load variations and input supply fluctuations.

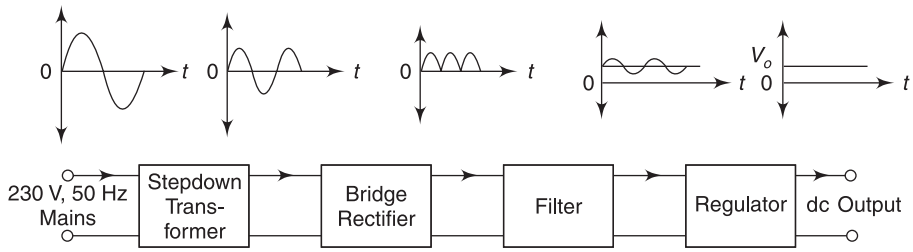



**Fig. 5.2** *Basic building block of linear-mode power supply*

### 5.2.1 Requirements of Linear-Mode Power Supply

1. The most important consideration in designing a power supply is the dc voltage at the output. It should be able to give minimum operable dc voltage at the rated current.

2. It should be able to furnish the maximum current needed for the unit, maintaining the voltage constant. In other words, the regulation of the power supply should be good.
3. The ac ripple should be low.
4. The power supply should be protected in the event of short-circuit on the load side.
5. Overvoltage (spike and surges) protection must be incorporated.
6. The response of the power supply to temperature changes should be minimum.

## 5.3 RECTIFIERS

Rectifier is defined as an electronic circuit used for converting ac voltage into unidirectional voltage. A rectifier utilizes unidirectional conduction device like a vacuum diode or *PN* junction diode. Rectifiers are classified depending upon the period of conduction as half-wave rectifier and full-wave rectifier.

## 5.4 HALF-WAVE RECTIFIER

It converts an ac voltage into a pulsating dc voltage using only one half of the applied ac voltage. The rectifying diode conducts only during one half of the ac cycle only. Figure 5.3 shows the basic circuit and waveforms of a half-wave rectifier (HWR).

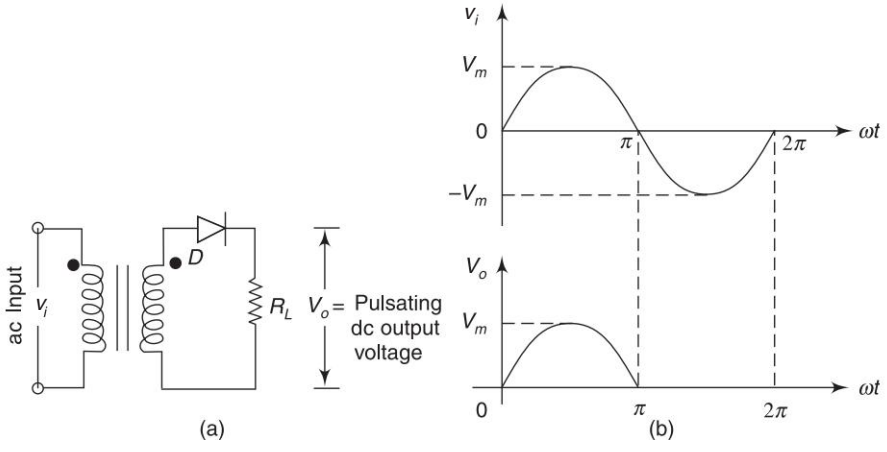



**Fig. 5.3** *(a) Basic structure of a half-wave rectifier (b) Input output waveforms of half-wave rectifier*

Let $v_i$ be the voltage applied to the primary of the transformer and given by the equation

$$v_i = V_m \sin \omega t;\ V_m >> V_\gamma$$

where $V_\gamma$ is the cut-in voltage of the diode. During the positive half cycle of the input signal, the anode of the diode becomes more positive with respect to the cathode and hence, the diode *D* conducts. For an ideal diode, the forward voltage drop is zero. So, the whole input voltage will appear across the load resistance, $R_L$.

During negative half cycle of the input signal, the anode of the diode becomes negative with respect to the cathode and hence, diode *D* does not conduct. For an ideal diode, the impedance offered by the diode is infinity. So the whole input voltage appears across diode *D*. Hence, the voltage drop across $R_L$ is zero.

***Ripple Factor ($\Gamma$)*** The ratio of rms value of ac component to the dc component in the output is known as ripple factor ($\Gamma$).

$$\Gamma = \frac{\text{rms value of ac component}}{\text{dc value of component}} = \frac{V_{r,\text{rms}}}{V_{\text{dc}}}$$

where $V_{r,\text{rms}} = \sqrt{V_{\text{rms}}^2 - V_{\text{dc}}^2}$.

Therefore, $$\Gamma = \sqrt{\left(\frac{V_{\text{rms}}}{V_{\text{dc}}}\right)^2 - 1}$$

The rms value of a continuous-time periodic waveform is the square root of the ratio of the square of the area under the curve for on cycle to the time period $T$, as given by

$$V_{\text{rms}} = \sqrt{\frac{\text{Square of the area under the curve for one cycle}}{\text{Time period}}}$$

$$= \sqrt{\frac{1}{T}\int_0^T [x(t)]^2\, dt}$$

The average or the dc content of the voltage across the load is given by

$$V_{av} = V_{\text{dc}} = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin \omega t\, d(\omega t) + \int_{\pi}^{2\pi} 0.d(\omega t)\right]$$

$$= \frac{V_m}{2\pi}[-\cos \omega t]_0^{\pi} = \frac{V_m}{\pi}$$

Therefore, $$I_{\text{dc}} = \frac{V_{\text{dc}}}{R_L} = \frac{V_m}{\pi R_L} = \frac{I_m}{\pi}$$

If the values of diode forward resistance ($r_f$) and the transformer secondary winding resistance ($r_s$) are also taken into account, then

$$V_{\text{dc}} = \frac{V_m}{\pi} - I_{\text{dc}}(r_s + r_f)$$

$$I_{\text{dc}} = \frac{V_{\text{dc}}}{(r_s + r_f) + R_L} = \frac{V_m}{\pi(r_s + r_f + R_L)}$$

The rms voltage at the load resistance can be calculated as

$$V_{\text{rms}} = \left[\frac{1}{2\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t\, d(\omega t)\right]^{\frac{1}{2}}$$

$$= V_m\left[\frac{1}{4\pi}\int_0^{\pi} (1 - \cos 2\omega t)\, d\omega t\right]^{\frac{1}{2}} = \frac{V_m}{2}$$

Therefore, $$\Gamma = \sqrt{\left[\frac{V_m/2}{V_m/\pi}\right]^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21$$

From this expression, it is clear that the amount of ac present in the output is 121% of the dc voltage. So the half-wave rectifier is not practically useful in converting ac into dc.

***Efficiency ($\eta$)*** The ratio of dc output power to ac input power is known as rectifier efficiency ($\eta$).

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{\frac{(V_{dc})^2}{R_L}}{\frac{(V_{rms})^2}{R_L}} = \frac{\left(\frac{V_m}{\pi}\right)^2}{\left(\frac{V_m}{2}\right)^2} = \frac{4}{\pi^2} = 0.406 = 40.6\%$$

The maximum efficiency of a half-wave rectifier is 40.6%.

***Peak Inverse Voltage (PIV)*** It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half cycle. For half-wave rectifier, PIV is $V_m$.

***Transformer Utilization Factor (TUF)*** In the design of any power supply, the rating of the transformer should be determined. This can be done with a knowledge of the dc power delivered to the load and the type of rectifying circuit used.

$$\text{TUF} = \frac{\text{dc power delivered to the load}}{\text{ac rating of the transformer secondary}}$$

$$= \frac{P_{dc}}{P_{ac}\ \text{rated}}$$

In the half-wave rectifying circuit, the rated voltage of the transformer secondary is $V_m/\sqrt{2}$, but the actual rms current flowing through the winding is only $\frac{I_m}{2}$, not $I_m/\sqrt{2}$.

$$\text{TUF} = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{2}} = \frac{\frac{V_m^2}{\pi^2}\frac{1}{R_L}}{\frac{V_m}{\sqrt{2}}\frac{V_m}{2R_L}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

The TUF for a half-wave rectifier is 0.287.

**Form Factor**

$$\text{Form factor} = \frac{\text{rms value}}{\text{average value}} = \frac{V_m/2}{V_m/\pi} = \frac{\pi}{2} = 1.57$$

### Peak Factor

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}} = \frac{V_m}{V_m/2} = 2$$

## EXAMPLE 5.1

A half-wave rectifier, having a resistive load of 1000 Ω, rectifies an alternating voltage of 325 V peak value and the diode has a forward resistance of 100 Ω. Calculate (a) peak, average and rms value of current (b) dc power output (c) ac input power and (d) efficiency of the rectifier.

**Solution**

(a) Peak value of current, $I_m = \dfrac{V_m}{r_f + R_L} = \dfrac{325}{100 + 1000} = 295.45 \text{ mA}$

Average current, $I_{dc} = \dfrac{I_m}{\pi} = \dfrac{295.45}{\pi} \text{ mA} = 94.046 \text{ mA}$

RMS value of current, $I_{rms} = \dfrac{I_m}{2} = \dfrac{295.45}{2} = 147.725 \text{ mA}$

(b) The dc power output, $P_{dc} = I_{dc}^2 \times R_L$

$= (94.046 \times 10^{-3})^2 \times 1000 = 8.845 \text{ W}$

(c) The ac input power, $P_{ac} = (I_{rms})^2 \times (r_f + R_L)$

$= (147.725 \times 10^{-3})^2 \, (1100) = 24 \text{ W}$

(d) Efficiency of rectification, $\eta = \dfrac{P_{dc}}{P_{ac}} = \dfrac{8.845}{24} = 36.85\%$.

## EXAMPLE 5.2

A half-wave rectifier is used to supply 24 V dc to a resistive load of 500 Ω and the diode has a forward resistance of 50 Ω. Calculate the maximum value of the ac voltage required at the input.

**Solution** Average value of load current,

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{24}{500} = 48 \text{ mA}$$

Maximum value of load current, $I_m = \pi \times I_{dc} = \pi \times 48 \text{ mA} = 150.8 \text{ mA}$

Therefore, maximum ac voltage required at the input,

$$V_m = I_m \times (r_f + R_L)$$

$$= 150.8 \times 10^{-3} \times 550 = 82.94 \text{ V}$$

## EXAMPLE 5.3

An ac supply of 230 V is applied to a half-wave rectifier circuit through transformer of turns ratio 5:1. Assume the diode is an ideal one. The load resistance is 300 Ω. Find (a) dc output voltage, (b) PIV, (c) maximum, and

(d) average values of power delivered to the load.

**Solution**

(a) The transformer secondary voltage = $\frac{230}{5} = 46$ V

Maximum value of secondary voltage, $V_m = \sqrt{2} \times 46 = 65$ V

Therefore, dc output voltage, $V_{dc} = \frac{V_m}{\pi} = \frac{65}{\pi} = 20.7$ V

(b) PIV of a diode $V_m = 65$ V

(c) Maximum value of load current, $I_m = \frac{V_m}{R_L} = \frac{65}{300} = 0.217$ A

Therefore, maximum value of power delivered to the load,

$$P_m = I_m^2 \times R_L = (0.217)^2 \times 300 = 14.1 \text{ W}$$

(d) The average value of load current, $I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.7}{300} = 0.069$ A

Therefore, average value of power delivered to the load,

$$P_{dc} = I_{dc}^2 \times R_L = (0.069)^2 \times 300 = 1.43 \text{ W}$$

## EXAMPLE 5.4

A HWR has a load of 3.5 kΩ. If the diode resistance and secondary coil resistance together have a resistance of 800 Ω and the input voltage has a signal voltage of peak value 240 V. Calculate

(a) peak, average and rms value of current flowing
(b) dc power output
(c) ac power input
(d) efficiency of the rectifier

**Solution** Load resistance in a HWR, $R_L = 3.5$ kΩ

Diode resistance and secondary coil resistance, $r_f + r_s = 800$ Ω

Peak value of input voltage = 240 V

(a) Peak value of current, $I_m = \frac{V_m}{r_s + r_f + R_L} = \frac{240}{4300} = 55.81$ mA

Average value of current, $I_{dc} = \frac{I_m}{\pi} = \frac{55.81 \times 10^{-3}}{\pi} = 17.77$ mA

The rms value of current, $I_{rms} = \frac{I_m}{2} = \frac{55.81 \times 10^{-3}}{2} = 27.905$ mA

(b) The dc power output is

$$P_{dc} = (I_{dc})^2 R_L = (17.77 \times 10^{-3})^2 \times 3500 = 1.105 \text{ W}$$

(c) The ac power input is

$$P_{ac} = (I_{rms})^2 \times (r_f + R_L) = (27.905 \times 10^{-3})^2 \times 4300 = 3.348 \text{ W}$$

(d) Efficiency of the rectifier is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{1.105}{3.348} \times 100 = 33\%$$

## EXAMPLE 5.5

A HWR circuit supplies 100 mA dc to a 250 Ω load. Find the dc output voltage, PIV rating of a diode and the rms voltage for the transformer supplying the rectifier.

**Solution** Given $I_{dc} = 100$ mA, $R_L = 250\ \Omega$

(a) The dc output voltage,

$$V_{dc} = I_{dc} \times R_L = 100 \times 10^{-3} \times 250 = 25 \text{ V}$$

(b) The maximum value of secondary voltage,

$$V_m = \pi \times V_{dc} = \pi \times 25 = 78.54 \text{ V}$$

(c) PIV rating of a diode, $V_m = 78.54$ V

(d) The rms voltage for the transformer supplying the rectifier,

$$V_{rms} = \frac{V_m}{2} = \frac{78.54}{2} = 39.27 \text{ V}$$

## EXAMPLE 5.6

A voltage of 200 cos $\omega t$ is applied to HWR with load resistance of 5 kΩ. Find the maximum dc current component, rms current, ripple factor, TUF and rectifier efficiency,

**Solution** Given applied voltage = 200 cos$\omega t$, $V_m = 200$ V, $R_L = 5$ kΩ

(a) *To find dc current:*

$$I_m = \frac{V_m}{R_L} = \frac{200}{5 \times 10^3} = 40 \text{ mA}$$

Therefore, $$I_{dc} = \frac{I_m}{\pi} = \frac{40 \times 10^{-3}}{\pi} = 12.73 \text{ mA}$$

(b) *To find rms current:*

$$I_{rms} = \frac{I_m}{2} = \frac{40 \times 10^{-3}}{2} = 20 \text{ mA}$$

(c) *Ripple factor:* $$\Gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{20 \times 10^{-3}}{12.73 \times 10^{-3}}\right)^2 - 1} = 1.21$$

(d) *To determine TUF:*

$$\text{TUF} = \frac{P_{dc}}{P_{ac(\text{rated})}}$$

$$P_{dc} = I_{dc}^2 R_L = (12.73 \times 10^{-3})^2 \times 5 \times 10^3 = 0.81 \text{ W}$$

$$P_{\text{ac (rated)}} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{2} = \frac{200}{\sqrt{2}} \times \frac{40 \times 10^{-3}}{2} = 2.828$$

Therefore, $$\text{TUF} = \frac{P_{\text{dc}}}{P_{\text{ac (rated)}}} = \frac{0.81}{2.828} = 0.2863$$

(e) *Rectifier efficiency:* $$\eta = \frac{P_{\text{dc}}}{P_{\text{ac}}}$$

$$P_{\text{dc}} = 0.81 \text{ W}$$

$$P_{\text{ac}} = I_{\text{rms}}^2 R_L = (20 \times 10^{-3})^2 \times 5 \times 10^3 = 2 \text{ W}$$

Therefore, $$\eta = \frac{P_{\text{dc}}}{P_{\text{ac}}} \times 100 = \frac{0.81}{2} \times 100 = 40.5\%$$

## EXAMPLE 5.7

A diode has an internal resistance of 20 Ω and 1000 Ω load from a 110 V rms source of supply. Calculate (a) the efficiency of rectification and (b) the percentage regulation from no load to full load.

**Solution** Given $r_f = 20\ \Omega$, $R_L = 1000\ \Omega$ and $V_{\text{rms}}$ (secondary) = 110 V

The half-wave rectifier uses a single diode.

Therefore, $$V_m = \sqrt{2}\, V_{\text{rms}}(\text{secondary}) = \sqrt{2} \times 110 = 155.56 \text{ V}$$

$$I_m = \frac{V_m}{r_f + R_L} = \frac{155.56}{20 + 1000} = 0.1525 \text{ A}$$

$$I_{\text{dc}} = \frac{I_m}{\pi} = \frac{0.1525}{\pi} = 0.04854 \text{ A}$$

$$V_{\text{dc}} = I_{\text{dc}} R_L = 0.04854 \times 1000 = 48.54 \text{ V}$$

$$P_{\text{dc}} = V_{\text{dc}} I_{\text{dc}} = 48.54 \times 0.04854 = 2.36 \text{ W}$$

$$P_{\text{ac}} = I_{rms}^2 (r_f + R_L) = \left(\frac{I_m}{2}\right)^2 (r_f + R_L) \qquad \left(\text{since } I_{\text{rms}} = \frac{I_m}{2} \text{ for half-wave}\right)$$

$$= \left(\frac{0.1525}{2}\right)^2 (20 + 1000) = 5.93 \text{ W}$$

Efficiency, $$\eta = \frac{P_{\text{dc}}}{P_{\text{ac}}} \times 100 = \frac{2.36}{5.93} \times 100 = 39.7346\%$$

Percentage of line regulation $$= \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{\frac{V_m}{\pi} - V_{\text{dc}}}{V_{\text{dc}}} \times 100$$

$$= \frac{\frac{155.56}{\pi} - 48.54}{48.54} \times 100 = 2\%$$

## EXAMPLE 5.8

Show that maximum dc output power $P_{dc} = V_{dc} \times I_{dc}$ in a half-wave single-phase circuit occurs when the load resistance equals diode resistance $r_f$.

**Solution** For a half-wave rectifier,

$$I_m = \frac{V_m}{r_f + R_L}$$

$$I_{dc} = \frac{I_m}{\pi} = \frac{V_m}{\pi (r_f + R_L)}$$

and $$V_{dc} = I_{dc} \times R_L$$

Therefore, $$P_{dc} = V_{dc} \times I_{dc} = I_{dc}^2 R_L = \frac{V_m^2 R_L}{\pi^2 (r_f + R_L)^2}$$

For this power to be maximum,

$$\frac{dP_{dc}}{dR_L} = 0$$

$$\frac{d}{dR_L}\left[\frac{V_m^2 R_L}{\pi^2 (r_f + R_L)^2}\right] = \frac{V_m^2}{\pi^2}\left[\frac{(r_f + R_L)^2 - R_L \times 2(r_f + R_L)}{(r_f + R_L)^4}\right] = 0$$

$$(r_f + R_L)^2 - 2R_L(r_f + R_L) = 0$$

$$r_f^2 + 2r_f R_L + R_L^2 - 2r_f R_L - 2R_L^2 = 0$$

$$r_f^2 - R_L^2 = 0$$

$$R_L^2 = r_f^2$$

Thus, the power output is maximum if $R_L = r_f$

## EXAMPLE 5.9

The transformer of a half-wave rectifier has a secondary voltage of 30 $V_{rms}$ with a winding resistance of 10 Ω. The semiconductor diode in the circuit has a forward resistance of 100 Ω. Calculate (a) no load dc voltage (b) dc output voltage at $I_L = 25$ mA (c) % regulation at $I_L = 25$ mA (d) ripple voltage across the load (e) ripple frequency (f) ripple factor (g) dc power output and (h) PIV of the semiconductor diode.

**Solution**

$V_{rms}$ (secondary) = 30 V, $r_s = 10$ Ω, $r_f = 100$ Ω

$$V_m = \sqrt{2} \times V_{rms} = \sqrt{2} \times 30 = 42.4264 \text{ V}$$

(a) $$V_{dc} = \frac{V_m}{\pi} = \frac{42.4264}{\pi} = 13.5047 \text{ V}$$

(b) $$I_L = I_{dc} = 25 \text{ mA}$$

$$V_{dc} = I_{dc} R_L = \frac{I_m}{\pi} R_L = \frac{V_m}{\pi (r_f + r_s + R_L)} \times R_L$$

Here, $$R_L = \frac{V_{dc}}{I_{dc}}$$

Therefore, $$V_{dc} = \frac{V_m}{\pi \left( r_f + r_s + \frac{V_{dc}}{I_{dc}} \right)} \times \frac{V_{dc}}{I_{dc}}$$

$$V_{dc} = \frac{42.426\, V_{dc}}{\pi \left( 100 + 10 + \frac{V_{dc}}{25 \times 10^{-3}} \right)} \times \frac{1}{25 \times 10^{-3}}$$

$$V_{dc} (110 + 40 V_{dc}) = 540.1897\, V_{dc}$$

$$V_{dc} = \frac{540.1897 - 110}{40} = 10.7547 \text{ V}$$

(c) Percentage of regulation $$= \frac{V_{dc(NL)} - V_{dc(FL)}}{V_{dc(FL)}} \times 100$$

$$= \frac{13.5047 - 10.7547}{10.7547} \times 100 = 25.569\%$$

(d) $$I_m = \frac{V_m}{r_f + r_s + R_L}, \text{ where } R_L = \frac{V_{dc}}{I_{dc}} = \frac{10.7547}{25 \times 10^{-3}} = 430.188 \text{ V}$$

Therefore, $$I_m = \frac{42.4264}{100 + 10 + 430.188} = 0.07854 \text{ A}$$

$$I_{rms} = \frac{I_m}{2} = 0.03927 \text{ A}$$

$$\Gamma = \sqrt{\left( \frac{I_{rms}}{I_{dc}} \right)^2 - 1} = \sqrt{\left( \frac{0.03927}{25 \times 10^{-3}} \right)^2 - 1} = 1.21$$

Ripple voltage $\Gamma \times V_{dc} = 1.21 \times 10.7547 = 13.02791$ V

(e) Ripple frequency, $f = 50$ Hz

(f) $\Gamma$ = ripple factor = 1.21

(g) $P_{dc} = V_{dc} I_{dc} = 10.7547 \times 25 \times 10^{-3} = 0.2688$ W

(h) PIV $= V_m = 42.4264$ V

## 5.5 FULL-WAVE RECTIFIER

It converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. It uses two diodes of which one conducts during one half-cycle while the other diode conducts during the other half-cycle of the applied ac voltage. There are two types of full-wave rectifiers, viz., (i), full-wave rectifier with centre tapped transformer, and (ii) full-wave rectifier without transformer (bridge rectifier).

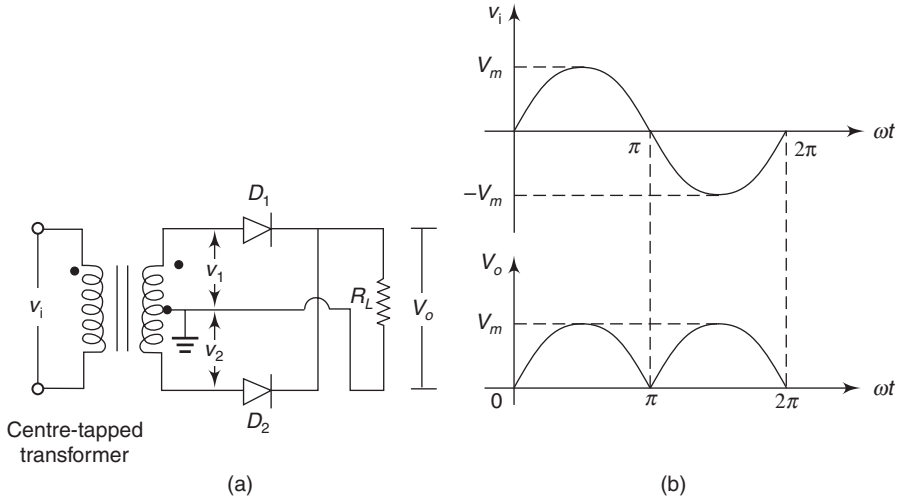



**Fig. 5.4** *Full-wave rectifier*

Figure 5.4 shows the basic circuit and waveforms of full-wave rectifier with a center tap transformer. During positive half of the input signal, the anode of the diode $D_1$ becomes positive and at the same time, the anode of diode $D_2$ becomes negative. Hence, $D_1$ conducts and $D_2$ does not conduct. The load current flows through $D_1$ and the voltage drop across $R_L$ will be equal to the input voltage.

During the negative half-cycle of the input, the anode of $D_1$ becomes negative and the anode of $D_2$ becomes positive. Hence, $D_1$ does not conduct and $D_2$ conducts. The load current flows through $D_2$ and the voltage drop across $R_L$ will be equal to the input voltage.

### *Ripple Factor ($\Gamma$)*

$$\Gamma = \sqrt{\left(\frac{V_{\text{rms}}}{V_{\text{dc}}}\right)^2 - 1}$$

The average voltage or dc voltage available across the load resistance is

$$V_{\text{dc}} = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \, \mathrm{d}(\omega t)$$

$$= \frac{V_m}{\pi}[-\cos \omega t]_0^{\pi} = \frac{2V_m}{\pi}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \text{ and } I_{rms} = \frac{I_m}{\sqrt{2}}$$

If the diode forward resistance ($r_f$) and the transformer secondary winding resistance ($r_s$) are included in the analysis, then

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc}\,(r_s + r_f)$$

$$I_{dc} = \frac{V_{dc}}{(r_s + r_f) + R_L} = \frac{2V_m}{\pi(r_s + r_f + R_L)}$$

The rms value of the voltage at the load resistance is

$$V_{rms} = \sqrt{\left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \, \mathrm{d}(\omega t)\right]} = \frac{V_m}{\sqrt{2}}$$

Therefore,

$$\Gamma = \sqrt{\left(\frac{V_m/\sqrt{2}}{2V_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.482$$

***Efficiency ($\eta$)*** The ratio of dc output power to ac input power is known as rectifier efficiency ($\eta$).

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{(V_{dc})^2/R_L}{(V_{rms})^2/R_L} = \frac{\left[\frac{2V_m}{\pi}\right]^2}{\left[\frac{V_m}{\sqrt{2}}\right]^2}$$

$$= \frac{8}{\pi^2} = 0.812 = 81.2\%$$

The maximum efficiency of a full-wave rectifier is 81.2%.

***Transformer Utilization Factor (TUF)*** The average TUF in a full-wave rectifying circuit is determined by considering the primary and secondary windings separately and it gives a value of 0.693.

**Form Factor**

$$\text{Form factor} = \frac{\text{rms value of the output voltage}}{\text{average value of the output voltage}} = \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

**Peak Factor**

$$\text{Peak factor} = \frac{\text{peak value of the output voltage}}{\text{rms value of the output voltage}} = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$$

Peak inverse voltage for full-wave rectifier is $2V_m$ because the entire secondary voltage appears across the non-conducting diode.

## EXAMPLE 5.10

A 230 V, 60 Hz voltage is applied to the primary of a 5:1 step-down, centre-tap transformer use in a full-wave rectifier having a load of 900 Ω. If the diode resistance and secondary coil resistance together has a resistance of 100 Ω, determine (a) dc voltage across the load, (b) dc current flowing through the load, (c) dc power delivered to the load, (d) PIV across each diode, (e) ripple voltage and its frequency and (f) rectification efficiency.

**Solution** The voltage across the two ends of secondary $= \frac{230}{5} = 46$ V

Voltage from centre tapping to one end, $V_{\text{rms}} = \frac{46}{2} = 23$ V

(a) The dc voltage across the load, $V_{\text{dc}} = \frac{2V_m}{\pi} = \frac{2 \times 23 \times \sqrt{2}}{\pi} = 20.7$ V

(b) The dc current flowing through the load, $I_{\text{dc}} = \frac{V_{\text{dc}}}{(r_s + r_f + R_L)} = \frac{20.7}{1000} = 20.7$ mA

(c) The dc power delivered to the load,

$$P_{\text{dc}} = (I_{\text{dc}})^2 \times R_L = (20.7 \times 10^{-3})^2 \times 900 = 0.386 \text{ W}$$

(d) PIV across each diode $= 2V_m = 2 \times 23 \times \sqrt{2} = 65$ V

(e) Ripple voltage, $V_{r,\text{rms}} = \sqrt{(V_{\text{rms}})^2 - (V_{\text{dc}})^2}$

$$= \sqrt{(23)^2 - (20.7)^2} = 10.05 \text{ V}$$

Frequency of ripple voltage $= 2 \times 60 = 120$ Hz

(f) Rectification efficiency, $\eta = \frac{P_{\text{dc}}}{P_{\text{ac}}} = \frac{(V_{\text{dc}})^2 / R_L}{(V_{\text{rms}})^2 / R_L} = \frac{(V_{\text{dc}})^2}{(V_{\text{rms}})^2}$

$$= \frac{(20.7)^2}{(23)^2} = \frac{428.49}{529} = 0.81$$

Therefore, percentage of rectification efficiency = 81%

## EXAMPLE 5.11

A full-wave rectifier has a centre-tap transformer of 100-0-100 V and each one of the diodes is rated at $I_{\text{max}} = 400$ mA and $I_{\text{av}} = 150$ mA. Neglecting the voltage drop across the diodes, determine (a) the value of load resistor that gives the largest dc power output, (b) dc load voltage and current, and (c) PIV of each diode.

**Solution**

(a) We know that the maximum value of current flowing through the diode for normal operation should not exceed 80% of its rated current.

Therefore, $I_{\text{max}} = 0.8 \times 400 = 320$ mA

The maximum value of the secondary voltage,

$$V_m = \sqrt{2} \times 100 = 141.4 \text{ V}$$

Therefore, the value of load resistor that gives the largest dc power output

$$R_L = \frac{V_m}{I_{\max}} = \frac{141.4}{320 \times 10^{-3}} = 442\ \Omega$$

(b) The dc (load) voltage, $V_{\text{dc}} = \dfrac{2V_m}{\pi} = \dfrac{2 \times 141.4}{\pi} = 90 \text{ V}$

The dc load current, $I_{\text{dc}} = \dfrac{V_{\text{dc}}}{R_L} = \dfrac{90}{442} = 0.204 \text{ A}$

(c) PIV of each diode = $2V_m = 2 \times 141.4 = 282.8$ V

## EXAMPLE 5.12

A full-wave rectifier delivers 50 W to a load of 200 Ω. If the ripple factor is 1%, calculate the ac ripple voltage across the load.

**Solution** The dc power delivered to the load,

$$P_{\text{dc}} = \frac{V_{\text{dc}}^2}{R_L}$$

Therefore, $V_{\text{dc}} = \sqrt{P_{\text{dc}} \times R_L} = \sqrt{50 \times 200} = 100 \text{ V}$

The ripple factor, $\Gamma = \dfrac{V_{\text{ac}}}{V_{\text{dc}}}$

i.e., $0.01 = \dfrac{V_{\text{ac}}}{100}$

Therefore, the ac ripple voltage across the load, $V_{\text{ac}} = 1$ V

## EXAMPLE 5.13

In a full-wave rectifier, the transformer rms secondary voltage from centre tap to each end of the secondary is 50 V. The load resistance is 900 Ω. If the diode resistance and transformer secondary winding resistance together has a resistance of 100 Ω, determine the average load current and rms value of load current?

**Solution** Voltage from centre tapping to one end, $V_{\text{rms}} = 50$ V

Maximum load current, $I_m = \dfrac{V_m}{r_s + r_f + R_L} = \dfrac{V_{\text{rms}} \times \sqrt{2}}{r_s + r_f + R_L} = \dfrac{70.7}{1000} = 70.7 \text{ mA}$

Average load current, $I_{\text{dc}} = \dfrac{2I_m}{\pi} = \dfrac{2 \times 70.7 \times 10^{-3}}{\pi} = 45 \text{ mA}$

RMS value of load current, $I_{\text{rms}} = \dfrac{I_m}{\sqrt{2}} = \dfrac{70.7 \times 10^{-3}}{\sqrt{2}} = 50 \text{ mA}$

## EXAMPLE 5.14

A full-wave rectifier circuit uses two silicon diodes with a forward resistance of 20 Ω each. A dc voltmeter connected across the load of 1 kΩ reads 55.4 volt. Calculate

(a) $I_{rms}$
(b) average voltage across each diode
(c) ripple factor and
(d) transformer secondary voltage rating.

**Solution** Given $V_{dc} = 55.4$ V and $R_L = 1$ kΩ

(a) $$I_{dc} = \frac{V_{dc}}{(r_f + R_L)} = \frac{55.4}{20 + 1000} = 54.31 \text{ mA}$$

We know that $$I_{dc} = \frac{2I_m}{\pi} \text{ and } I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$I_m = I_{dc} \times \frac{\pi}{2} = 54.31 \times 10^{-3} \times \frac{\pi}{2} = 85.31 \text{ mA}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{85.31 \times 10^{-3}}{\sqrt{2}} = 60.32 \text{ mA}$$

(b) The average voltage across each silicon diode will be 0.72 V.

(c) *To find ripple factor Γ*

$$\Gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{60.32 \times 10^{-3}}{54.31 \times 10^{-3}}\right) - 1} = 0.4833$$

To find transformer secondary voltage rating

We know that, $$V_{dc} = \frac{2V_m}{\pi} - I_{dc}\,(r_s + r_f)$$

where $r_f$ is the diode forward resistance and $r_s$ is the transformer secondary winding resistance.

$$55.4 = \frac{2V_m}{\pi} - 54.31 \times 10^{-3} \times 20 = \frac{2V_m}{\pi} - 1.086$$

$$56.49 = \frac{2V_m}{\pi}$$

Therefore, $$V_m = 56.49 \times \frac{\pi}{2} = 88.73 \text{ V}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{88.73}{\sqrt{2}} = 62.74 \text{ V}$$

Hence, transformer secondary voltage rating is 65 V

## 5.6 BRIDGE RECTIFIER

The need for a centre-tapped transformer in a full-wave rectifier is eliminated in the bridge rectifier. As shown in Fig. 5.5, the bridge rectifier has four diodes connected to form a bridge. The ac input voltage is applied to the diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge.

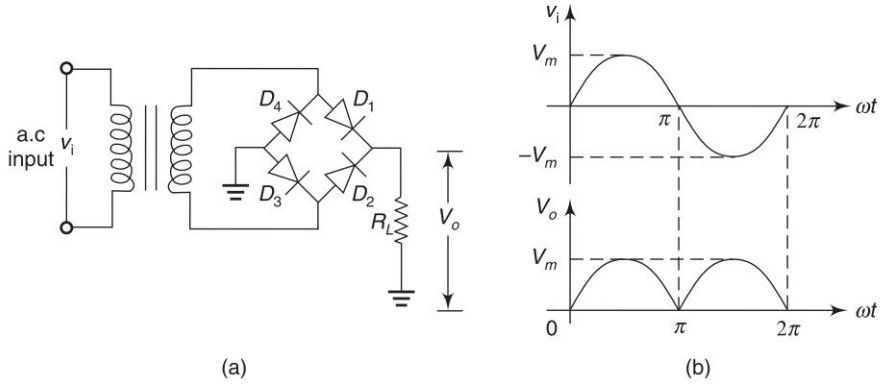



**Fig. 5.5** *Bridge rectifier*

For the positive half-cycle of the input ac voltage, diodes $D_1$ and $D_3$ conduct, whereas diodes $D_2$ and $D_4$ do not conduct. The conducting diodes will be in series through the load resistance $R_L$. So the load current flows through $R_L$.

During the negative half-cycle of the input ac voltage, diodes $D_2$ and $D_4$ conduct, whereas diodes $D_1$ and $D_3$ do not conduct. The conducting diode $D_2$ and $D_4$ will be in series through the load $R_L$ and the current flows through $R_L$ in the same direction as in the previous half-cycle. Thus, a bidirectional wave is converted into an unidirectional one.

The average values of output voltage and load current for bridge rectifier are the same as for a centre-tapped full-wave rectifier. Hence,

$$V_{dc} = \frac{2V_m}{\pi} \quad \text{and} \quad I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi}$$

If the values of the transformer secondary winding resistance ($r_s$) and diode forward resistance ($r_f$) are considered in the analysis, then

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc}\,(r_s + r_f)$$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi\,(r_s + r_f + R_L)}$$

The maximum efficiency of a bridge rectifier is 81.2% and the ripple factor is 0.48. The PIV is $V_m$.

**Advantages of the Bridge Rectifier** In the bridge rectifier, the ripple factor and efficiency of the rectification are the same as for the full-wave rectifier. The PIV across either of the non-conducting diodes is equal to the

peak value of the transformer secondary voltage, $V_m$. The bulky centre-tapped transformer is not required. Transformer utilization factor is considerably high. Since the current flowing in the transformer secondary is purely alternating, the TUF increases to 0.812, which is the main reason for the popularity of a bridge rectifier. The bridge rectifiers are used in applications allowing floating output terminals, i.e., no output terminal is grounded.

The bridge rectifier has only one disadvantage that it requires four diodes as compared to two diodes for centre-tapped full-wave rectifier. But the diodes are readily available at cheaper rate in the market. Apart from this, the PIV rating required for the diodes in a bridge rectifier is only half of that for a centre tapped full-wave rectifier. This is a great advantage, which offsets the disadvantage of using extra two diodes in a bridge rectifier.

***Comparison of Rectifiers*** The comparison of rectifiers is given in Table 18.1.

**Table 5.1** *A comparison of rectifiers*

| Particulars | Type of rectifier | | |
|---|---|---|---|
| | Half-wave | Full-wave | Bridge |
| No. of diodes | 1 | 2 | 4 |
| Maximum efficiency | 40.6% | 81.2% | 81.2% |
| $V_{dc}$ (no load) | $V_m/\pi$ | $2V_m/\pi$ | $2V_m/\pi$ |
| Average current/diode | $I_{dc}$ | $I_{dc}/2$ | $I_{dc}/2$ |
| Ripple factor | 1.21 | 0.48 | 0.48 |
| Peak inverse voltage | $V_m$ | $2V_m$ | $V_m$ |
| Output frequency | $f$ | $2f$ | $2f$ |
| Transformer utilisation factor | 0.287 | 0.693 | 0.812 |
| Form factor | 1.57 | 1.11 | 1.11 |
| Peak factor | 2 | $\sqrt{2}$ | $\sqrt{2}$ |

## EXAMPLE 5.15

A 230 V, 50 Hz voltage is applied to the primary of a 4:1 step-down transformer used in a bridge rectifier having a load resistance of 600 Ω. Assuming the diodes to be ideal, determine (a) dc output voltage, (b) dc power delivered to the load, (c) PIV, and (d) output frequency.

**Solution**

(a) The rms value of the transformer secondary voltage,

$$V_{\text{rms (secondary)}} = \frac{V_{\text{rms(primary)}}}{\text{Turns ratio}} = \frac{230}{4} = 57.5$$

The maximum value of the secondary voltage

$$V_m = \sqrt{2} \times 57.5 = 81.3 \text{ V}$$

Therefore, dc output voltage,

$$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 81.3}{\pi} = 52 \text{ V}$$

(b) The dc power delivered to the load,

$$P_{dc} = \frac{V_{dc}^2}{R_L} = \frac{52^2}{600} = 2.704 \text{ W}$$

(c) PIV across each diode, $V_m = 81.3$ V

(d) Output frequency = 2 × 50 = 100 Hz

## EXAMPLE 5.16

In a bridge rectifier, the transformer is connected to 200 V, 60 Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diode is ideal, find (a) $V_{dc}$ (b) $I_{dc}$ and (c) PIV.

**Solution** Given in a bridge rectifier, input voltage = 200 V, 60 Hz and turns ratio = 11:1

(a) *To find the voltage across load,* $V_{dc}$

$$V_{dc} = \frac{2V_m}{\pi}$$

where $$V_m = \sqrt{2}\, V_{rms(secondary)}$$

$$V_{rms(secondary)} = \frac{V_{rms(primary)}}{\text{Turns ratio}} = \frac{200}{11} = 18.18 \text{ V}$$

Therefore, $$V_m = 18.18 \times \sqrt{2} = 25.7 \text{ V}$$

Hence, $$V_{dc} = \frac{2 \times 25.7}{\pi} = 16.36 \text{ V}$$

(b) *To find* $I_{dc}$

Assuming that $R_L = 600\ \Omega$, then

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{16.36}{600} = 27.26 \text{ mA}$$

(c) *To find PIV*

$$PIV = V_m = 25.7 \text{ V}$$

## EXAMPLE 5.17

A bridge rectifier uses four identical diodes having forward resistance of 5 Ω and the secondary voltage is 30 V(rms). Determine the dc output voltage for $I_{dc} = 200$ mA and value of the output ripple voltage.

**Solution** Given, transformer secondary resistance = 5 Ω

Secondary voltage $V_{rms} = 30$ V, $I_{dc} = 200$ mA

Since only two diodes of the bridge rectifier circuit will conduct during positive of negative half cycle of the input signal, the diode forward resistance, $r_f = 2 \times 5\ \Omega = 10\ \Omega$.

We know that,

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc}\,(r_f + r_s) \text{ where } V_m = \sqrt{2}V_{rms} = \sqrt{2} \times 30 \text{ V}$$

Therefore,
$$V_{dc} = \frac{2 \times \sqrt{2} \times 30}{\pi} - 200 \times 10^{-3}\,(10 + 5) = 24 \text{ V}$$

$$\text{Ripple factor} = \frac{\text{rms value of ripple at the output}}{\text{average value of output voltage}}$$

Therefore,
$$0.48 = \frac{\text{rms value of ripple at the output}}{24}$$

Hence, rms value of ripple at the output = 0.48 × 24 = 11.52 V

## EXAMPLE 5.18

In a full-wave rectifier, the required dc voltage is 9 V and the diode drop is 0.8 V. Calculate ac rms input voltage required in centre-tapped full-wave rectifier and bridge rectifier circuits.

**Solution** (a) The dc voltage across the load of the center tapped full-wave rectifier circuit,

$$V_{dc} = 9 = \frac{2V_m}{\pi} - 0.8 = \frac{2\sqrt{2} \times V_{rms}}{\pi} - 0.8$$

where $V_{rms}$ is the rms input voltage from centre tapping to on end. That is,

$$9.8 = \frac{2\sqrt{2}\,V_{rms}}{\pi}$$

Therefore,
$$V_{rms} = \frac{9.8\,\pi}{2\sqrt{2}} = 10.885 \text{ V}$$

Hence, the voltage across the two ends of the secondary = 2 × 10.885 = 21.77 V

(b) In the bridge rectifier, $V_{dc} = 9 = \frac{2\sqrt{2}V_{rms}}{\pi} - 2 \times 0.8$

Therefore, the voltage across two ends of secondary, $V_{rms} = \frac{10.6\,\pi}{2\sqrt{2}} = 11.77 \text{ V}$

## 5.7 HARMONIC COMPONENTS IN A RECTIFIER CIRCUIT

The term *harmonic* is defined as "a sinusoidal component of a periodic waveform or quantity possessing a frequency, which is an integral multiple of the fundamental frequency." By definition, a perfect sine wave has no harmonics, except fundamental component at one frequency. Harmonics are present in waveforms that are not perfect sine waves due to distortion from nonlinear loads. The French mathematician Fourier discovered that a distorted waveform can be represented as a series of sine waves, with each being an integer multiple of the fundamental frequency and each with a specific magnitude.

That is, the harmonic frequencies are integer multiples [2, 3, 4,….] of the fundamental frequency. For example, the second harmonic on a 50 Hz system is 2 × 50 or 100 Hz. The sixth harmonic in a 50 Hz system, or the fifth harmonic in a 60 Hz system is 300 Hz. There are a number of different types of equipment that may experience faulty operations or failures due to high harmonic voltage and/ or current levels. The amount of the harmonic voltage and current levels that a system can tolerate is dependent on the equipment and the source.

The sum of the fundamental and all the harmonics is called the ***Fourier series***. This series can be viewed as a spectrum analysis where the fundamental frequency and the harmonic component are identified.

The result of such an analysis for the current waveform of a half-wave rectifier circuit using a single diode is given by

$$i = I_m \left[ \frac{1}{\pi} + \frac{1}{2} \sin \omega t - \frac{2}{\pi} \sum_{k=2,4,6} \frac{\cos k\omega t}{(k+1)(k-1)} \right]$$

The angular frequency of the power supply is the lowest angular frequency present in the above expression. All the other terms are the even harmonics of the power frequency.

The full-wave rectifier consists of two half-wave rectifier circuits, arranged in such a way that one circuit conducts during one half cycle and the second circuit operates during the second half cycle. Therefore, the currents are functionally related by the expression $i_1(\alpha) = i_2(\alpha + \pi)$. Thus, the total current of the full-wave rectifier is $i = i_1 + i_2$ as expressed by

$$i = I_m \left[ \frac{2}{\pi} - \frac{4}{\pi} \sum_{\substack{k=\text{even} \\ k \neq 0}} \frac{\cos k\omega t}{(k+1)(k-1)} \right]$$

From the above equation, it can be seen that the fundamental angular frequency is eliminated and the lowest frequency is the second harmonic term $2\omega$. This is the advantage that the full-wave rectifier presents in filtering of the output. Additionally, the current pulses in the two halves of the transformer winding are in such directions that the magnetic cycles formed through the iron core is essentially that of the alternating current. This avoids any dc saturation of the transformer core that could give rise to additional harmonics at the output.

## 5.8 FILTERS

The output of a rectifier contains dc component as well as ac component. Filters are used to minimise the undesirable ac, i.e., ripple leaving only the dc component to appear at the output.

The ripple in the rectified wave being very high, the factor being 48% in the full-wave rectifier; majority of the applications which cannot tolerate this, will need an output which has been further processed.

Figure 5.6 shows the concept of a filter, where the full-wave rectified output voltage is applied at its input. The output of a filter is not exactly a constant dc level. But it also contains a small amount of ac component. Some important filters are

(i) Inductor filter
(ii) Capacitor filter
(iii) LC or L-section filter
(iv) CLC or $\pi$-type filter

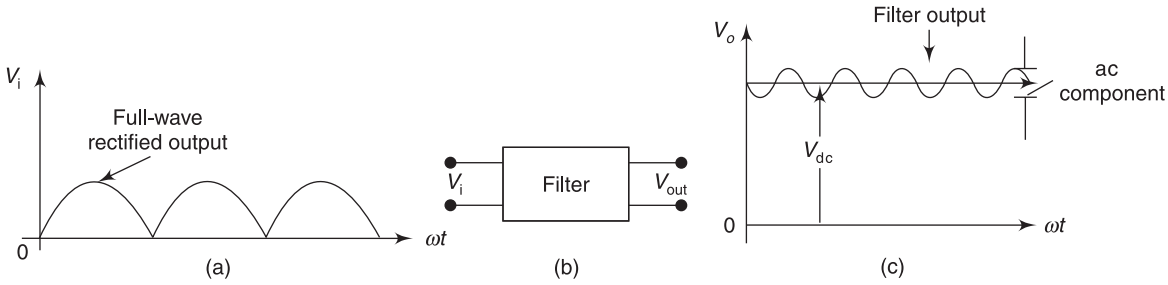



**Fig. 5.6** *Concept of a filter*

***Inductor Filter*** Figure 5.7 shows the inductor filter. When the output of the rectifier passes through an inductor, it blocks the ac component and allows only the dc component to reach the load.

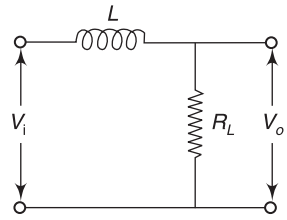



**Fig. 5.7** *Inductor filter*

The ripple factor of the inductor filter is given by

$$\Gamma = \frac{R_L}{3\sqrt{2}\ \omega L}$$

It shows that the ripple factor will decrease when $L$ is increased and $R_L$ is decreased. Clearly, the inductor filter is more effective only when the load current is high (small $R_L$). The larger value of the inductor can reduce the ripple and at the same time the output dc voltage will be lowered as the inductor has a higher dc resistance.

The operation of the inductor filter depends on its well known fundamental property to oppose any change of current passing through it.

To analyse this filter for a full-wave, the Fourier series can be written as

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left[\frac{1}{3}\cos 2\,\omega t + \frac{1}{15}\cos 4\omega t + \frac{1}{35}\cos 6\,\omega t + \cdots\right]$$

The dc component is $\dfrac{2V_m}{\pi}$.

Assuming the third and higher terms contribute little output, the output voltage is

$$V_o = \frac{2V_m}{2\pi} - \frac{4V_m}{3\pi}\cos 2\,\omega t$$

The diode, choke and transformer resistances can be neglected since they are very small as compared with $R_L$. Therefore, the dc component of current $I_m = \dfrac{V_m}{R_L}$. The impedance of series combination of $L$ and $R_L$ at $2\omega$ is

$$Z = \sqrt{R_L^2 + (2\,\omega L)^2} = \sqrt{R_L^2 + 4\omega^2\, L^2}$$

Therefore, for the ac component,

$$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2\ L^2}}$$

Therefore, the resulting current $i$ is given by,

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi} \frac{\cos(2\omega t - \varphi)}{\sqrt{R_L^2 + 4\omega^2 L^2}}$$

where $\varphi = \tan^{-1}\left(\frac{2\omega L}{R_L}\right)$.

The ripple factor, which can be defined as the ratio of the rms value of the ripple to the dc value of the wave, is

$$\Gamma = \frac{\frac{4V_m}{3\pi\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}} = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

If $\frac{4\omega^2 L^2}{R_L^2} >> 1$, then a simplified expression for $\Gamma$ is

$$\Gamma = \frac{R_L}{3\sqrt{2}\,\omega L}$$

In case, the load resistance is infinity, i.e., the output is an open circuit, then the ripple factor is

$$\Gamma = \frac{2}{3\sqrt{2}} = 0.471$$

This is slightly less than the value of 0.482. The difference being attributable to the omission of higher harmonics as mentioned. It is clear that the inductor filter should only be used where $R_L$ is consistently small.

## EXAMPLE 5.19

Calculate the value of inductance to use in the inductor filter connected to a full-wave rectifier operating at 60 Hz to provide a dc output with 4% ripple for a 100 Ω load.

**Solution** We know that the ripple factor for inductor filter is $\Gamma = \frac{R_L}{3\sqrt{2}\,\omega L}$

Therefore,
$$0.04 = \frac{100}{3\sqrt{2}\,(2\pi \times 60 \times L)} = \frac{0.0625}{L}$$

$$L = \frac{0.0625}{0.04} = 1.5625 \text{ H}$$

***Capacitor Filter*** An inexpensive filter for light loads is found in the capacitor filter which is connected directly across the load, as shown in Fig. 5.8(a). The property of a capacitor is that it allows ac component and blocks the dc component. The operation of a capacitor filter is to short the ripple to ground but leave the dc to appear at the output when it is connected across a pulsating dc voltage.

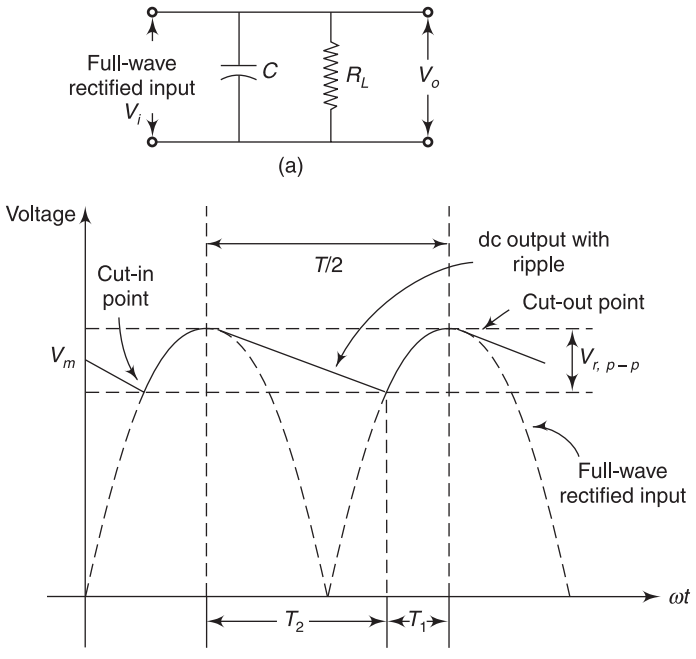



**Fig. 5.8** *(a) Capacitor filter (b) Ripple voltage triangular waveform*

During the positive half-cycle, the capacitor charges up to the peak value of the transformer secondary voltage, $V_m$, and will try to maintain this value as the full-wave input drops to zero. The capacitor will discharge through $R_L$ slowly until the transformer secondary voltage again increases to a value greater than the capacitor voltage (equal to the load voltage). The diode conducts for a period which depends on the capacitor voltage. The diode will conduct when the transformer secondary voltage becomes more than the 'cut-in' voltage of the diode. The diode stops conducting when the transformer voltage becomes less than the diode voltage. This is called cut-out voltage.

Referring to Fig. 5.8(b) with slight approximation, the ripple voltage waveform can be assumed as triangular. From the cut-in point to the cut-out point, whatever charge the capacitor acquires is equal to the charge the capacitor has lost during the period of non-conduction, i.e., from cut-out point to the next cut-in point.

The charge it has acquired = $V_{r,\,p-p} \times C$

The charge it has lost = $I_{dc} \times T_2$

Therefore, $V_{r,\,p\text{-}p} \times C = I_{dc} \times T_2$

If the value of the capacitor is fairly large, or the value of the load resistance is very large, then it can be assumed that the time $T_2$ is equal to half the periodic time of the waveform,

i.e., $$T_2 = \frac{T}{2} = \frac{1}{2f}, \quad \text{then} \quad V_{r,p-p} = \frac{I_{dc}}{2fC}$$

With the assumptions made above, the ripple waveform will be triangular in nature and the rms value of the ripple is given by

$$V_{r,\text{rms}} = \frac{V_{r,p-p}}{2\sqrt{3}}$$

Therefore, from the above equation, we have

$$V_{r,\text{rms}} = \frac{I_{\text{dc}}}{4\sqrt{3}\ fC}$$

$$= \frac{V_{\text{dc}}}{4\sqrt{3}\ fCR_L}, \text{ since } I_{\text{dc}} = \frac{V_{\text{dc}}}{R_L}$$

Therefore, ripple factor $\Gamma = \dfrac{V_{r,\text{rms}}}{V_{\text{dc}}} = \dfrac{1}{4\sqrt{3}\ fCR_L}$

The ripple may be decreased by increasing $C$ or $R_L$ (or both) with a resulting increase in dc output voltage.

If $f = 50$ Hz, $C$ in μF and $R_L$ in Ω, $\Gamma = \dfrac{2890}{CR_L}$.

## EXAMPLE 5.20

Calculate the value of capacitance to use in a capacitor filter connected to a full-wave rectifier operating at a standard aircraft power frequency of 400 Hz, if the ripple factor is 10% for a load of 500 Ω.

**Solution** We know that the ripple factor for capacitor filter is

$$\Gamma = \frac{1}{4\sqrt{3}\ fCR_L}$$

Therefore, $$0.01 = \frac{1}{4\sqrt{3} \times 400 \times C \times 500} = \frac{0.722 \times 10^{-6}}{C}$$

$$C = \frac{0.722 \times 10^{-6}}{0.01} = 72.2\ \mu\text{F}$$

## EXAMPLE 5.21

A15-0-15 volt (rms) 50 Hz ideal transformer is used with a full-wave rectifier circuit with diodes having forward drop of 1 volt. The load is a resistance of 100 Ω and a capacitor of 10,000 μF is used as a filter across the load resistance. Calculate the dc load current and voltage.

**Solution** Given transformer secondary voltage = 15-0-15 V (rms);
Diode forward drop = 1 V; $R_L = 100\ \Omega$; $C = 10{,}000\ \mu\text{F}$

We know that, $$V_{\text{dc}} = V_m - \frac{V_{r,p-p}}{2} = V_m - \frac{I_{\text{dc}}}{4\,fC}$$

Therefore, $$V_{\text{dc}} = V_m - \frac{V_{\text{dc}}}{R_L\,4\,fC}, \left[\text{since } I_{\text{dc}} = \frac{V_{\text{dc}}}{R_L}\right]$$

Simplifying, we get $$V_{dc} = \left[\frac{4 f R_L C}{4 f R_L C + 1}\right] V_m$$

We know that $$V_m = V_{rms} \times \sqrt{2} = 15 \times \sqrt{2}$$

Therefore, $$V_{dc} = \left[\frac{4 \times 50 \times 100 \times 10000 \times 10^{-6}}{4 \times 50 \times 100 \times 10000 \times 10^{-6} + 1}\right] \times 15 \times \sqrt{2} = 21.105 \text{ V}$$

Considering the given voltage drop of 1 volt due to diodes,

$$V_{dc} = 21.105 - 1 = 20.105 \text{ V}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.105}{100} = 0.20105 \text{ A}$$

## EXAMPLE 5.22

A full-wave rectified voltage of 18 V peak is applied across a 500 μF filter capacitor. Calculate the ripple and dc voltages if the load takes a current of 100 mA.

**Solution**

Given $$V_m = 18 \text{ V}, C = 500 \text{ μF and } I_{dc} = 100 \text{ mA}$$

$$V_{dc} = V_m - \frac{I_{dc}}{4fC} = 18 - \frac{100 \times 10^{-3}}{4 \times 50 \times 500 \times 10^{-6}} = 17 \text{ V}$$

$$V_{r,rms} = \frac{I_{dc}}{4\sqrt{3} fC} = \frac{100 \times 10^{-3}}{4\sqrt{3} \times 50 \times 500 \times 10^{-6}} = 0.577 \text{ V}$$

Therefore, ripple, $$\Gamma = \frac{V_{r,rms}}{V_{dc}} = \frac{0.577}{17} \times 100 = 3.39\%$$

## EXAMPLE 5.23

A bridge rectifier with capacitor filter is fed from 220 V to 40 V step down transformer. If average dc current in load is 1 A and capacitor filter of 800 μF, calculate the load regulation and ripple factor. Assume power line frequency of 50 Hz. Neglect diode forward resistance and dc resistance of secondary of transformer.

**Solution**

$$V_{rms\ (secondary)} = 40 \text{ V}, I_{dc} = 1\text{A}, C = 800 \text{ μF, and } f = 50 \text{ Hz}$$

$$V_m = \sqrt{2} V_{rms} = \sqrt{2} \times 40 = 56.5685 \text{ V}$$

$$V_{dc\,(FL)} = V_m - \frac{I_{dc}}{4fC} = 56.5685 - \frac{1}{4 \times 50 \times 800 \times 10^{-6}} = 50.3185 \text{ V}$$

On no load, $$I_{dc} = 0$$

Hence, $$V_{dc\,(NL)} = V_m = 56.5685 \text{ V}$$

Therefore, percentage of regulation $= \dfrac{V_{dc(NL)} - V_{dc\,(NL)}}{I_{dc(NL)}} \times 100 = \dfrac{56.5685 - 50.3185}{50.1385} \times 100 = 12.42\%$

$$R_L = \frac{V_{dc}}{I_{dc}} = \frac{50.1385}{1} = 50.1385\ \Omega$$

$$\Gamma = \frac{1}{4\sqrt{3}\, fCR_L} = \frac{1}{4\sqrt{3} \times 50 \times 800 \times 10^{-6} \times 50.3185} = 0.0717, \text{ i.e., } 7.17\%$$

***LC Filter*** We know that the ripple factor is directly proportional to the load resistance $R_L$ in the inductor filter and inversely proportional to $R_L$ in the capacitor filter. Therefore, if these two filters are combined as *LC* filter or L-section filter as shown in Fig. 5.9, the ripple factor will be independent of $R_L$.

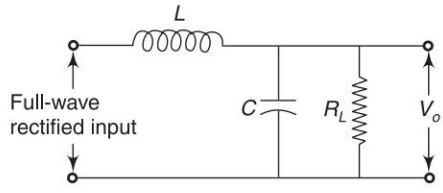



**Fig. 5.9** *LC filter*

If the value of the inductance is increased, it will increase the time of conduction. At some critical value of inductance, one diode, either $D_1$ or $D_2$ in full-wave rectifier, will always be conducting.

From Fourier series, the output voltage can be expressed as

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi} \cos 2\,\omega t$$

The dc output voltage, $V_{dc} = \dfrac{2V_m}{\pi}$

Therefore, $I_{rms} = \dfrac{4V_m}{3\pi\sqrt{2}} \cdot \dfrac{1}{X_L} = \dfrac{\sqrt{2}}{3} \cdot \dfrac{V_{dc}}{X_L}$

This current flowing through $X_C$ creates the ripple voltage $V_{r,\,rms}$ in the output.

Therefore, $V_{rms} = I_{rms} \cdot X_C = \dfrac{\sqrt{2}}{3} \cdot V_{dc} \cdot \dfrac{X_C}{X_L}$

The ripple factor, $\Gamma = \dfrac{V_{rms}}{V_{dc}} = \dfrac{\sqrt{2}}{3} \cdot \dfrac{X_C}{X_L} = \dfrac{\sqrt{2}}{3} \cdot \dfrac{1}{4\omega^2 C_L}$, since $X_C = \dfrac{1}{2\omega C}$ and $X_L = 2\omega L$

If $f = 50$ Hz, $C$ is in μF and $L$ is in Henry, ripple factor, $\Gamma = \dfrac{1.194}{LC}$.

***Bleeder Resistor*** It was assumed in the analysis given above that for a critical value of inductor, either of the diodes is always conducting, i.e., current does not fall to zero. The incoming current consists of two components:

(i) $I_{dc} = \dfrac{V_{dc}}{R_L}$, and (ii) a sinusoidal varying components with peak value of $\dfrac{4V_m}{3\pi X_L}$. The negative peak of the ac current must always be less than dc, i.e., $\sqrt{2}\, I_{rms} \le \dfrac{V_{dc}}{R_L}$.

We know that for *LC* filter, $I_{rms} = \frac{\sqrt{2}}{3} \times \frac{V_{dc}}{X_L}$

Hence, $\frac{2V_{dc}}{X_L} \leq \frac{V_{dc}}{R_L}$, i.e., $X_L \geq \frac{2}{3} R_L$

i.e., $L_C = \frac{R_L}{2\omega}$, where $L_C$ is the critical inductance.

It should be noted that the condition $X_L \geq \frac{2}{3} R_L$ cannot be satisfied for all load requirements. At no load, i.e., when the load resistance is infinity, the value of the inductance will also tend to be infinity. To overcome this problem, a bleeder resistor $R_B$ is connected in parallel with the load resistance as shown in Fig. 5.10. Therefore, a minimum current will always be present for optimum operation of the inductor. It improves voltage regulation of the supply by acting as the pre-load on the supply. Also, it provides safety by acting as a discharging path for capacitor.

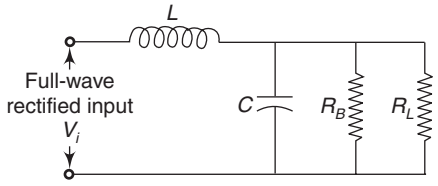



**Fig. 5.10** *Bleeder resistor connected at the filter output*

## EXAMPLE 5.24

Design a filter for full-wave circuit with *LC* filter to provide an output voltage of 10 V with a load current of 200 mA and the ripple is limited to 2%.

**Solution** The effective load resistance, $R_L = \frac{10}{200 \times 10^{-3}} = 50\ \Omega$

We know that the ripple factor,

$$\Gamma = \frac{1.194}{LC}$$

i.e., $$0.02 = \frac{1.194}{LC}$$

i.e., $$LC = \frac{1.194}{0.02} = 59.7$$

Critical value of $L = \frac{R_L}{3\omega} = \frac{50}{3 \times 2\pi f} = 53$ mH

Taking $L = 60$ mH (about 20% higher), $C$ will be about 1000 μF.

## EXAMPLE 5.25

A full-wave rectifier (FWR) supplies a load requiring 300 V at 200 mA. Calculate the transformer secondary voltage for (a) a capacitor input filter using a capacitor of 10 mF, and (b) a choke input filter using a choke of 10 H and a capacitance of 10 μF. Neglect the resistance of choke.

**Solution** Given $V_{dc} = 300$ V; $I_{dc} = 200$ mA

(a) For the capacitor filter with $C = 10\ \mu F$,

$$V_{dc} = V_m - \frac{I_{dc}}{4fC}$$

$$300 = V_m - \frac{200 \times 10^{-3}}{4(50)(10 \times 10^{-6})} = V_m - 100$$

Therefore, $V_m = 400\ V_{(p-p)}$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = 282.84\ V$$

(b) For the choke, i.e., *LC* filter with $L = 10$ H; $C = 10\ \mu F$

$$V_{dc} = \frac{2V_m}{\pi}$$

$$300 = \frac{2V_m}{\pi}$$

Therefore, $V_m = 471.23$ V

$$V_{rms} = \frac{V_m}{\sqrt{2}} = 333.21\ V$$

## EXAMPLE 5.26

Determine the ripple factor of a *L*-type choke input filter comprising a 10 H choke and 8 μF capacitor used with a FWR. Compare with a simple 8 μF capacitor input filter at a load current of 50 mA and also at 150 mA. Assume the dc voltage of 50 V.

**Solution** $V_{dc} = 50$ V, $L = 10$ H, $C = 8\ \mu F$

Assume $f = 50$ Hz, i.e., $\omega = 2\pi f = 100\pi$ rad/sec.

For *LC* filter, the ripple factor is

$$\Gamma = \frac{1}{6\sqrt{2}\omega^2 LC} = \frac{1}{6\sqrt{2} \times (100\pi)^2 \times 10 \times 8 \times 10^{-6}} = 0.01492 \text{ i.e., } 1.492\%$$

For the simple capacitor filter, $C = 8\ \mu F$.

(a) At $I_L = 50$ mA,

$$R_L = \frac{V_{dc}}{I_L} = \frac{50}{50 \times 10^{-3}} = 1000\ \Omega$$

$$\Gamma = \frac{1}{4\sqrt{3}fCR_L} = \frac{1}{4\sqrt{3} \times 50 \times 8 \times 10^{-6} \times 1000} = 0.3608, \text{ i.e., } 36.08\%$$

(b) At $I_L = 150$ mA,

$$R_L = \frac{V_{dc}}{I_L} = \frac{50}{150 \times 10^{-3}} = 333.33\ \Omega$$

$$\Gamma = \frac{1}{4\sqrt{3}fCR_L} = \frac{1}{4\sqrt{3} \times 50 \times 8 \times 10^{-6} \times 333.33} = 1.082, \text{ i.e., } 108.2\%$$

Thus, it is inferred that the *LC* choke input filter is more effective than capacitor input filter and the ripple factor of *LC* choke input filter does not depend on the load resistance.

## EXAMPLE 5.27

In a full-wave rectifier using an *LC* filter, $L = 10$ H, $C = 100$ μF, and $R_L = 500$ Ω. Calculate $I_{dc}$,$V_{dc,}$ and ripple factor for an input of $v_i = 30 \sin (100\ \pi t)$V.

**Solution** Comparing the input with $v_i = V_m \sin \omega t$

$V_m$ (secondary) $= V_m = 30$ V

$$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 30}{\pi} = 19.0985 \text{ V}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{19.0985}{500} = 0.03819 \text{ A} = 38.19 \text{ mA}$$

$$\text{Ripple factor} = \frac{1}{6\sqrt{2}\,\omega^2 LC} = \frac{1}{6\sqrt{2} \times (100\pi)^2 \times 10 \times 100 \times 10^{-6}} = 1.194 \times 10^{-3}$$

***Multiple L-section Filter*** The filtering level can be improved by using two of more L-section filters in series, as shown in Fig. 5.11. It is assumed that the reactance of all the inductances are much larger than the reactance of the capacitors and the reactance of the last capacitor is small compared with the resistance of the load. Under these conditions, the impedance between 3 and 3′ is $X_{C2}$, the impedance between 2 and 2′ is $X_{C1}$, and the impedance between 1 and 1′ is $X_{L1}$. The alternating current $I_1$ through $L_1$ is, given by

$$I_1 = \frac{\sqrt{2}\,V_{dc}}{3} \frac{1}{X_{L1}}$$

The ac voltage across $C_1$ is given by

$$V_{22'} = I_1 X_{C1}$$

The alternating current $I_2$ through $L_2$ is given by

$$I_2 = \frac{V_{22'}}{X_{L2}}$$

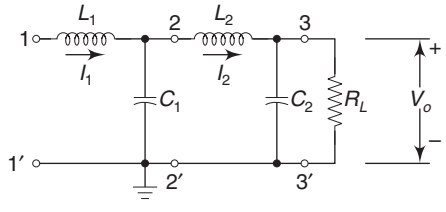



**Fig. 5.11** *A multiple (two-section) L-section filter*

The ac voltage across $C_2$ and hence, across the load is given by

$$V_{33'} = I_2 X_{C2} = I_1 \frac{X_{C2} X_{C1}}{X_{L2}} = \frac{\sqrt{2}\,V_{d.c.}}{3} \frac{X_{C2} X_{C1}}{X_{L2} X_{L1}}$$

The ripple factor is obtained by dividing the above equation by $V_{dc}$. Hence,

$$\Gamma = \frac{\sqrt{2}}{3} \frac{X_{C1} X_{C2}}{X_{L1} X_{L2}}$$

The generalized expression for any number of sections can be obtained by comparing the above equation with that of a single L-section. For example, the ripple factor of a multiple L-section filter ($\Gamma_n$) is given by

$$\Gamma_n = \frac{\sqrt{2}}{3}\left(\frac{X_C}{X_L}\right)^n = \frac{\sqrt{2}}{3}\frac{1}{(16\pi^2 f^2 LC)^n}$$

where $n$ is the number of similar $L$-sections.

***CLC or π-section Filter*** Figure 5.12 shows the CLC or $\pi$-type filter which basically consists of a capacitor filter followed by an $LC$ section. This filter provided a fairly smooth output, and is characterized by a highly peaked diode currents and poor regulation.

The action of a $\pi$-section filter can best be understood by considering the inductor and the second capacitor as an L-section filter that acts upon the triangular output-voltage wave from the first capacitor. The output voltage is then approximately that from the input capacitor, decreased by the dc voltage drop in the inductor. The ripple contained in this output is reduced by the L-section filter.

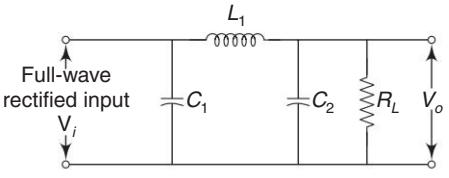



**Fig. 5.12** *CLC or π-type filter*

The ripple voltage can be calculated by analyzing the triangular wave into a Fourier series and then multiplying each component by $X_{C2}/X_{L1}$ for this harmonic. The Fourier analysis of this waveform is given by

$$v = V_{\text{dc}} - \frac{V_r}{\pi}\left(\sin 2\,\omega t - \frac{\sin 2\omega t}{2} + \frac{\sin 6\omega t}{3} - \cdots\right)$$

We know that

$$V_r = \frac{I_{\text{dc}}}{2fC_1}$$

The rms second-harmonic voltage is

$$V_{\text{rms}} = V_2' = \frac{V_r}{\pi\sqrt{2}} = \frac{I_{\text{dc}}}{2\pi fC_1\sqrt{2}} = \sqrt{2}I_{\text{dc}}X_{C1}$$

where $X_{C1}$ is the reactance of $C_1$ at the second-harmonic frequency.

The voltage $V_2'$ is impressed on an L-section, and the output ripple is $V_2'X_{C2}/X_{L1}$.

Hence, the ripple factor is

$$\Gamma = \frac{V_{\text{rms}}}{V_{\text{dc}}} = \frac{\sqrt{2}\,I_{\text{dc}}X_{C1}}{V_{\text{dc}}}\frac{X_{C2}}{X_{L1}} = \sqrt{2}\,\frac{X_{C1}}{R_L}\frac{X_{C2}}{X_{L1}}$$

where all reactance are calculated at the second-harmonic frequency.

For $f = 60$ Hz, the above equation reduces to

$$\Gamma = \frac{3{,}300}{C_1C_2L_1R_L}$$

***Multiple π-section Filter*** In order to obtain pure dc at the output, more number of $\pi$-sections may be used in series. Such a filter using more than one $\pi$-section, as shown in Fig. 5.13, is called a multiple $\pi$-section filter.

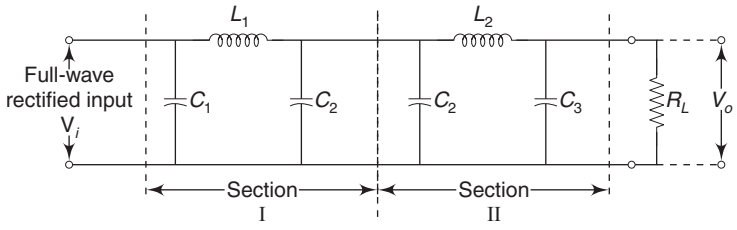



**Fig. 5.13** *Multiple π-section filter*

The ripple factor for multiple $\pi$-section filler is given by

$$\Gamma = \frac{X_{C1}}{R_L} \cdot \frac{X_{C2}}{X_{L1}} \cdot \frac{X_{C3}}{X_{L2}} \cdots \frac{X_{Cn}}{X_{L(n-1)}}$$

where $n$ is the number of $\pi$-sections.

## EXAMPLE 5.28

Design a CLC or $\pi$-section filter for $V_{dc} = 10$ V, $I_L = 200$ mA, and $\Gamma = 2\%$.

**Solution**

$$R_L = \frac{10}{200 \times 10^{-3}} = 50\ \Omega$$

$$0.02 = \frac{5700}{LC_1C_2 \times 50} = \frac{114}{LC_1C_2}$$

If we assume $L = 10$ H and $C_1 = C_2 = C$, we have

$$0.02 = \frac{114}{LC^2} = \frac{11.4}{C^2}$$

$$C^2 = 570; \text{ therefore, } C = \sqrt{570} \approx 24\ \mu\text{F}$$

## EXAMPLE 5.29

A full-wave single-phase rectifier employs a $\pi$-section filter consisting of two 4 μF capacitances and a 20 H choke. The transformer voltage to the centre tap is 300 V rms. The load current is 500 mA. Calculate the dc output voltage and the ripple voltage. The resistance of the choke is 200 Ω.

**Solution**

$$C_1 = C_2 = 4\ \mu\text{F}, L = 20\ \text{H}$$

$$I_{dc} = 500\ \text{mA}, R_x = 200\ \Omega$$

Maximum value of secondary voltage,

$$V_{s(\max)} = \sqrt{2} \times 300 = 424.2\ \text{V}$$

$$R_L = \frac{V_{dc}}{I_{dc}} = \frac{270.19}{500 \times 10^{-3}} = 540\ \Omega$$

$$V_{dc} = V_{s(max)} - \frac{V_r}{2} - I_{dc} R_x$$

Ripple voltage, $$V_r = \frac{I_{dc}}{2fC}$$

$$= \frac{500 \times 10^{-3}}{2 \times 50 \times 4 \times 10^{-6}} = 1.25 \text{ mV}$$

The dc output voltage, $$V_{dc} = 424.2 - \frac{1.25 \times 10^{-3}}{2} - (500 \times 10^{-3} \times 200) = 324.19 \text{ V}$$

***RC Filters*** Consider the *CLC* filter with the inductor *L* replaced by a resistor *R*. This type of filter called *RC* filter is shown in Fig. 5.14. The expression for the ripple factor can be obtained by replacing $X_L$ by *R*. Then,

$$\Gamma = \sqrt{2} \frac{X_{C1}}{R_L} \cdot \frac{X_{C2}}{R}$$

Therefore, if resistor *R* is chosen equal to the reactance of the inductor which it replaces, the ripple remains unchanged.

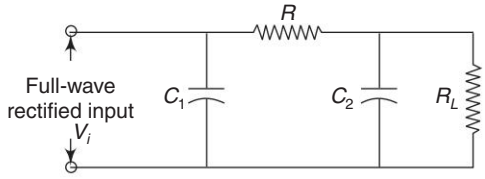



**Fig. 5.14** *RC filter*

The resistance *R* will increase the voltage drop and hence, the regulation will be poor. This type of filters are often used for economic reasons, as well as the space and weight requirement of the iron-cored choke for the *LC* filter. Such *RC* filters are often used only for low current power supplies.

***Comparison of Filters*** Table 5.2 shows the comparison of various types of filters, when used with full-wave circuits. In all these filters, the resistances of diodes, transformer and filter elements are considered negligible and a 60 Hz power line is assumed.

**Table 5.2** *Comparison of various types of filters*

| Particulars | Type of Filter | | | | |
|---|---|---|---|---|---|
| | None | L | C | L-Section | π-Section |
| $V_{dc}$ at no load | 0.636 $V_m$ | 0.636 $V_m$ | $V_m$ | $V_m$ | $V_m$ |
| $V_{dc}$ at load $I_{dc}$ | 0.636 $V_m$ | 0.636 $V_m$ | $V_m - \frac{4170 I_{dc}}{C}$ | 0.636 $V_m$ | $V_m - \frac{4170 I_{dc}}{C}$ |
| Ripple factor Γ | 0.48 | $\frac{R_L}{16000 L}$ | $\frac{2410}{CR_L}$ | $\frac{0.83}{LC}$ | $\frac{3330}{LC_1C_2R_L}$ |
| Peak inverse voltage (PIV) | 2 $V_m$ | 2 $V_m$ | 2 $V_m$ | 2 $V_m$ | 2 $V_m$ |

## 5.9 VOLTAGE REGULATORS: VOLTAGE REGULATION

In an unregulated power supply, the output voltage changes whenever the input voltage or load changes. An ideal regulated power supply is an electronic circuit designed to provide a predetermined dc voltage $V_o$ which is independent of the load current and variations in the input voltage. A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations.

***Factors Determining the Stability*** The output dc voltage $V_o$ depends on the input unregulated dc voltage $V_i$, load current $I_L$ and temperature $T$. Hence, the change in output voltage of power supply can be expressed as follows:

$$\Delta V_o = \frac{\partial V_o}{\partial V_i}\Delta V_i + \frac{\partial V_o}{\partial I_L}\Delta I_L + \frac{\partial V_o}{\partial T}\Delta T$$

or $$\Delta V_o = S_V \Delta V_i + R_o \Delta I_L + S_T \Delta T$$

where the three coefficients are defined as

Input regulation factor, $$S_V = \frac{\Delta V_o}{\Delta V_i}\Big|\, \Delta I_L = 0; \Delta T = 0$$

Output resistance, $$R_o = \frac{\Delta V_o}{\Delta I_L}\Big|\, \Delta V_i = 0; \Delta T = 0$$

Temperature coefficient, $$S_T = \frac{\Delta V_o}{\Delta T}\Big|\, \Delta V_i = 0; \Delta I_L = 0$$

Smaller the value of the three coefficients, better the regulation of the power supply.

***Line Regulation*** Line regulation is defined as the change in output voltage for a change in line supply voltage, keeping the load current and temperature constant. Line regulation is given by

$$\text{Line regulation} = \frac{\text{Change in output voltage}}{\text{Change in input voltage}} = \frac{\Delta V_o}{\Delta V_i}$$

***Load Regulation*** Load regulation is defined as a change in regulated output voltage as the load current changes from no load to full load. It is expressed as a percentage of no-load voltage or full-load voltage.

$$\%\ \text{Load regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{no load}}} \times 100$$

or $$\%\ \text{Load regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{full load}}} \times 100$$

where $V_{\text{no load}}$ is the output voltage at zero load current and $V_{\text{full load}}$ is the output voltage at rated load current. This is usually denoted in percentage. The plot of the output voltage $V_o$ versus the load current $I_L$ for a full-wave rectifier is given in Fig. 5.15. The drop in the characteristics is a measure of the internal resistance of the power supply.

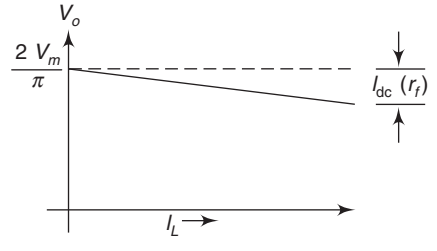



**Fig. 5.15** *Load regulation characteristics*

***Zener Diode Shunt Regulator*** A Zener diode, under reverse bias breakdown condition, can be used to regulate the voltage across a load, irrespective of the supply voltage or load current variations. A simple Zener voltage regulator circuit is shown in Fig. 5.16. The Zener diode is selected with $V_Z$ equal to the voltage desired across the load. The Zener diode has a characteristic that under reverse bias condition, the voltage across it practically remains constant, even if the current through it changes by a large extent. Under normal conditions, the input current $I_i = I_L + I_Z$ flows through resistor $R$. The input voltage $V_i$ can be written as $V_i = I_iR + V_Z = (I_L + I_Z)\,R + V_Z$.

When the input voltage $V_i$ increases (say due to supply voltage variations), as the voltage across Zener diode remains constant, the drop across resistor $R$ will increase with a corresponding increase in $I_L + I_Z$. As $V_Z$ is a constant, the voltage across the load will also remain constant and hence, $I_L$ will be a constant. Therefore, an increase in $I_L + I_Z$ will result in an increase in $I_Z$ which will not alter the voltage across the load.

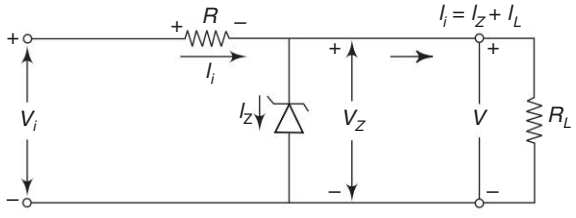



**Fig. 5.16** *Zener voltage regulator*

It must be ensured that the reverse voltage applied to the Zener diode never exceeds PIV of the diode and at the same time, the applied input voltage must be greater than the breakdown voltage of the Zener diode for its operation. The Zener diodes can be used as 'stand-alone' regulator circuits and also as reference voltage sources.

## EXAMPLE 5.30

Design a Zener shunt voltage regulator with the following specifications: $V_o$ = 10 V; $V_{\text{in}}$ = 20–30 V; $I_L$ = (30–50) mA; $I_Z$ = (20–40) mA

**Solution** Refer Fig. 5.16.

*Selection of Zener diode*

$$V_Z = V_o = 10 \text{ V}$$

$$I_{Z\,(\max)} = 40 \text{ mA}$$

$$P_Z = V_Z \times I_{Z(\max)} = 10 \times 40 \times 10^{-3} = 0.4 \text{ W}$$

Hence, a 0.5 WZ 10 Zener can be selected

*Value of load resistance, $R_L$*

$$R_{L\,(\min)} = \frac{V_o}{I_{L(\max)}} = \frac{10}{50 \times 10^{-3}} = 200\ \Omega$$

$$R_{L\,(\max)} = \frac{V_o}{I_{L(\min)}} = \frac{10}{30 \times 10^{-3}} = 333\ \Omega$$

*Value of input resistance, R*

$$R_{\max} = \frac{V_{\text{in}(\max)} - V_o}{I_{L(\min)} + I_{Z(\max)}} = \frac{30 - 10}{(30 + 40) \times 10^{-3}} = 286\ \Omega$$

$$R_{\min} = \frac{V_{\text{in(min)}} - V_o}{I_{L(\max)} + I_{Z(\min)}} = \frac{20 - 10}{(50 + 20) \times 10^{-3}} = 143\ \Omega$$

Therefore, $$R = \frac{R_{\max} + R_{\min}}{2} = 215\ \Omega$$

## EXAMPLE 5.31

In a Zener regulator, the dc input is 10 V ± 20%. The output requirements are 5 V, 20 mA. Assume $I_{Z(\min)}$ and $I_{Z(\max)}$ as 5 mA and 80 mA. Design the Zener regulator.

**Solution** The minimum Zener current is $I_{Z(\min)}$ = 5 mA when the input voltage is minimum. Here the input voltage varies between 10 V ± 20%, i.e., 8 V and 12 V.

Therefore, the input voltage $V_{i(\min)}$ = 8 V

Given load current $I_L$ = 20 mA and the voltage across the load, $V_o$ = 5 V.

Therefore,

$$R_L = \frac{V_o}{I_L} = \frac{5\ \text{V}}{20 \times 10^{-3}} = 250\ \Omega$$

Hence, the series resistance $$R = \frac{V_{i(\min)} - V_o}{(I_{Z(\min)} + I_L)}$$

$$= \frac{(8 - 5)}{(5 + 20) \times 10^{-3}} = 120\ \Omega$$

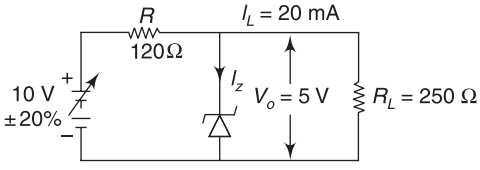



**Fig. 5.17**

The various values are given in the Zener regulator shown in Fig. 5.17.

## EXAMPLE 5.32

If dc unregulated input is 20 V, $V_o$ = 10 V and load current is 0–20 mA, design the Zener voltage regulator. Assume for the Zener, $I_{Z(\min)}$ = 10 mA and $I_{Z(\max)}$ = 100 mA.

**Solution** Given input voltage, $V_i$ = 20 V

Output voltage $V_o$ = 10 V

Load current varies from 0 to 20 mA

$I_{Z(\min)}$ = 10 mA, $I_{Z(\max)}$ = 100 mA

Here, $V_Z = V_o$ = 10 V (constant)

Applying KVL to a closed-loop circuit, $V_i = IR + V_Z$

Hence, $20 = IR + 10$

or $IR = 10$

Therefore, $R = \frac{10}{I}\ \Omega$, where $I$ is the loop current in ampere

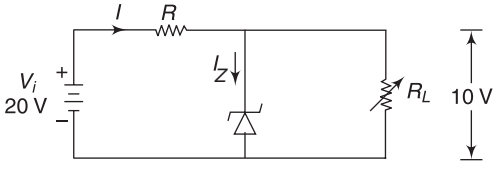



**Fig. 5.18**

(i) For $I_Z = I_{Z(\min)}$ = 10mA and $I_L = 0$

The total current $I = I_L + I_Z$ = 10 mA

Therefore, $$R_{\max} = \frac{V_o}{I_{Z(\min)}} = \frac{10}{10 \times 10^{-3}} = 1000\ \Omega$$

(ii) For $I_Z = I_{Z(\max)} = 100$ mA and $I_L = 20$ mA

$$I = I_L + I_{Z(\max)} = 20 \times 10^{-3} + 100 \times 10^{-3} = 120 \text{ mA}$$

Therefore, $$R_{\min} = \frac{V_o}{I} = \frac{10}{120 \times 10^{-3}} = 83.33\ \Omega$$

(iii) The range of $R$ varies from 83.33 Ω to 1000 Ω.

## EXAMPLE 5.33

Design a Zener voltage regulator to meet the following specifications: Output voltage = 5 V, Load current = 10 mA, Zener wattage = 400 mW and input voltage = 10 V ± 2 V.

**Solution** Given $V_o = 5$ V, $I_L = 10$ mA

Here, load resistance is $$R_L = \frac{V_o}{I_L} = \frac{5}{10 \times 10^{-3}} = 500\ \Omega$$

Maximum Zener current $$I_{Z(\max)} = \frac{400 \text{ mW}}{5 \text{ V}} = 80 \text{ mA}$$

The minimum input voltage required will be when $I_z = 0$. Under this condition,

$$I = I_L = 10 \text{ mA}$$

Minimum input voltage $V_{i(\min)} = V_o + IR$

Hence, $V_{i(\min)} = 10 - 2 = 8$ V

or $8 = 5 + (10 \times 10^{-3})\, R$

Therefore, $$R_{\max} = \frac{3}{10 \times 10^{-3}} = 300\ \Omega$$

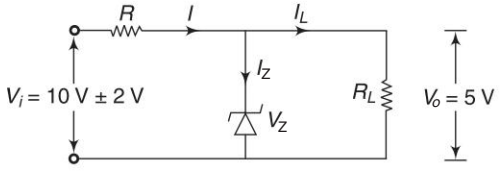



**Fig. 5.19**

Now, maximum input voltage, $V_{i(\max)} = V_o + \lfloor I_{Z(\max)} + I_L \rfloor R = 5 + [(80 + 10)10^{-3}]R$

or $12 = 5 + (90 \times 10^{-3})R$

$$R_{\min} = \frac{7}{90 \times 10^{-3}} = 77.77\ \Omega$$

The value of $R$ is chosen between 77.77 Ω and 300 Ω.

## EXAMPLE 5.34

A 24 V, 600 mW Zener diode is used for providing a 24 V stabilized supply to a variable load. If the input voltage is 32 V, calculate (a) the value of series resistance required and (b) diode current when the load is 1200 Ω.

**Solution** Given $V_o = 24$ V, $V_i = 32$ V, $P_Z = 600$ mW and $R_L = 1200\ \Omega$

The load current, $$I_L = \frac{V_o}{R_L} = \frac{24}{1200} = 20 \text{ mA}$$

Maximum Zener current, $I_{Z(\max)} = \dfrac{P_Z}{V_o} = \dfrac{600 \times 10^{-3}}{24} = 25 \text{ mA}$

$$R_{\max} = \frac{V_i - V_o}{I_{L(\min)} + I_{Z(\max)}}$$

$$= \frac{32 - 24}{(20 + 25) \times 10^{-3}} = \frac{8}{45 \times 10^{-3}} = 177.78\ \Omega$$

## EXAMPLE 5.35

A Zener voltage regulator circuit is to maintain constant voltage at 60 V, over a current range from 5 to 50 mA. The input supply voltage is 200 V. Determine the value of the resistance $R$ to be connected in the circuit, for voltage regulation from load current $I_L = 0$ mA to $I_L$ max, the maximum possible value of $I_L$. What is the value of $I_L$ max?

**Solution** Given $V_Z = V_o = 60$ V and $V_i = 200$ V

(a) *To find the value of resistance* ($R$):

$$R = \frac{V_i - V_o}{I_{Z(\max)} + I_{L(\min)}}$$

$$= \frac{200 - 60}{50 \times 10^{-3}} = \frac{140}{50 \times 10^{-3}} = 2.8 \text{ k}\Omega$$

(b) *To find the value of* $I_{L(\max)}$:

If $I_{Z(\max)} = 50$ mA, $I_{L(\min)} = 0$ mA

If $I_{Z(\min)} = 5$ mA, $I_{L(\max)} = 45$ mA

Therefore, $I_{L(\max)} = 45$ mA

## EXAMPLE 5.36

For the Zener voltage regulation shown, determine the range of $R_L$ and $I_L$ that gives the stabilizer voltage of 10 V.

**Solution** From the circuit, $I = I_Z + I_L$

But from $R$, $I = \dfrac{V_i - V_o}{R} = \dfrac{40 - 10}{1 \times 10^3} = 30 \text{ mA}$

When $I_L$ is minimum, $I_Z$ is maximum and vice versa.

$$I = I_{Z(\max)} + I_{L(\min)}$$

$$30 \text{ mA} = 24 \text{ mA} + I_{L(\min)}$$

Therefore, $I_{L(\min)} = 6$ mA

But $I_{L(\min)} = \dfrac{V_o}{R_{L(\max)}}$

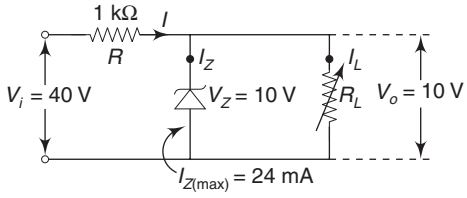



**Fig. 5.20**

$$R_{L(\max)} = \frac{V_o}{I_{L(\min)}} = \frac{10}{6 \times 10^{-3}} = 1.667 \text{ k}\Omega$$

and
$$I = I_{Z(\min)} + I_{L(\max)}$$
$$30 \text{ mA} = 5 \text{ mA} + I_{L(\max)}$$
$$I_{L(\max)} = 25 \text{ mA}$$

But
$$I_{L(\max)} = \frac{V_o}{R_{L(\min)}}$$
$$R_{L(\min)} = \frac{V_o}{I_{L(\max)}} = \frac{10}{25 \times 10^{-3}} = 400 \ \Omega$$

Hence, the range of $I_L$ is 6 mA to 25 mA and that of $R_L$ is 400 W to 1.667 kW.

## EXAMPLE 5.37

Determine the range of input voltage that maintains the output voltage of 10 V, for the regulator circuit shown.

**Solution** As $V_o = 10$ V constant and $R_L = 10$ kΩ constant, we have

$$I_L = \frac{V_o}{R_L} = \frac{10}{10 \times 10^3} = 1 \text{ mA}$$

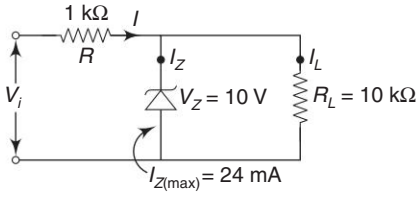



**Fig. 5.21**

When $V_i = V_{i(\max)}$, $I_Z = I_{Z(\max)}$

Now $I = I_Z + I_L$

Therefore, $I_{(\max)} = I_{Z(\max)} + I_L = 24 \text{ mA} + 1 \text{ mA} = 2 \text{ mA}.$

$$\frac{V_{i(\max)} - V_Z}{R} = 25 \text{ mA}$$

Therefore, $V_{i(\max)} - 10 = 1 \times 10^3 (25 \times 10^{-3})$

$$V_{i(\max)} = 35 \text{ V}.$$

When $V_i = V_{i(\min)}$, $I_Z = I_{Z(\min)} = 5$ mA

Therefore, $I_{\min} = I_{Z(\min)} + I_L = 5 \text{ mA} + 1 \text{ mA} = 6 \text{ mA}$

$$\frac{V_{i(\min)} - V_Z}{R} = 6 \times 10^{-3}$$
$$V_{i(\min)} - 10 = 1 \times 10^3 (6 \times 10^{-3})$$
$$V_{i(\min)} = 16 \text{ V}$$

Thus, range of input voltage is 16 V to 35 V for which the output voltage will be of 10 V.

***Emitter-Follower Type Regulator*** In the Zener voltage regulator, the Zener current varies over a wide range as the input voltage and load current vary. As a result, the output voltage which is equal to $V_z$ also changes by a small amount. This change in the output voltage can be minimized by reducing the change in the Zener current with the help of a circuit called emitter-follower type regulator as shown in Fig. 5.22.

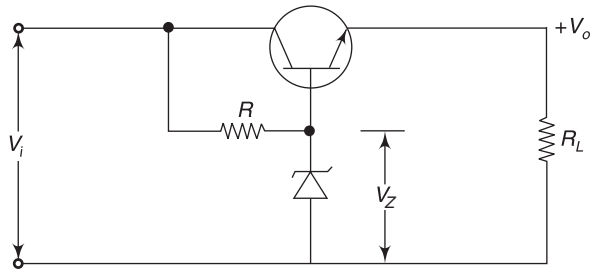



**Fig. 5.22** *Emitter-follower type regulator*

Here, the load resistance, $R_L$, is not connected across the Zener directly as in the Zener regulator, but is connected through an amplifier/buffer circuit. The transistor is connected as an emitter-follower. As can be seen, the output voltage, $V_o = (V_Z - V_{BE})$.

However, the load current $I_L$ is supplied by the transistor from the input voltage $V_i$, deriving its base current from the Zener circuit. The base current $I_B$ is equal to $\frac{I_L}{\beta}$, where $\beta$ is the current-gain of the transistor. As far as the Zener circuit is concerned, it is supplying only the base current. Any change in the load current is reduced by $\beta$ times, i.e., change in the Zener current.

***Overload Protection*** Figure 5.23(a) shows overload protection circuit in which a small sensing resistance $R_{SC}$ is added in series with the load resistance and two diodes are connected from the base of the transistor to the output.

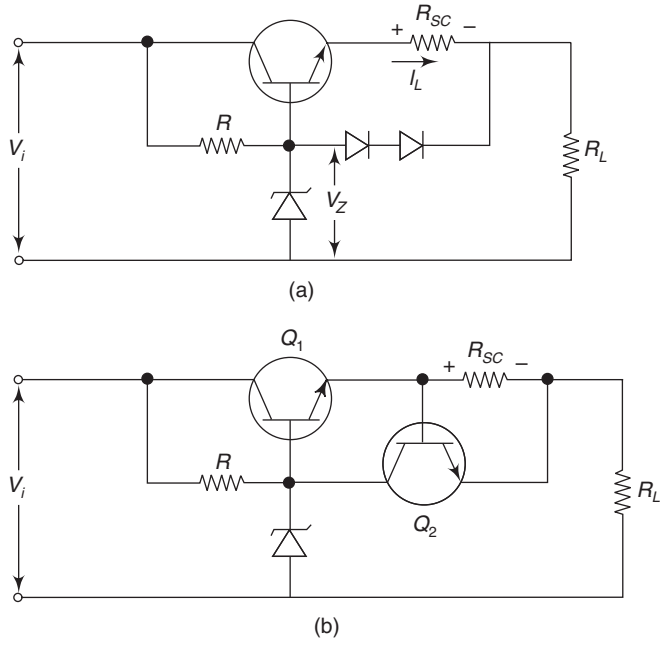



**Fig. 5.23** *(a) and (b) Overload protection circuit*

The emitter voltage is equal to $(V_Z - V_{BE})$. The voltage drop across the sensing resistance $R_{SC}$ is equal to $(I_L \times R_{SC})$. As long as the voltage drop across $R_{SC}$ is less than twice the cut-in voltage of the diode, the diodes are effectively as good as not connected in the circuit. If the voltage drop across $R_{SC}$ increases suddenly due to overcurrent in the load, then the diodes will be forward biased and will start conducting. This will divert a part of the base current, which will be directly led to the output, thus restricting the base current and hence, the transistor current. With proper design, the transistor can be turned off in the case of a short circuit.

The protective diodes can be replaced by another transistor $Q_2$ as shown in Fig. 5.23(b). In this case, the voltage across $R_{SC}$ is used in turning ON transistor $Q_2$, giving the same effect as before.

***Principle of Obtaining a Regulated Power Supply*** If the control element of a regulator operates in its linear region, then the regulator is called a linear regulator. Linear regulators are generally of series mode type. The regulator circuit using a Zener diode is vulnerable to the variations in supply voltage since the current through the Zener diode also changes correspondingly. Hence, the linear regulator uses an op-amp as an error amplifier, and a pass transistor as a control element. The error output from the op-amp drives the control element, which allows current to the load accordingly and keeps the output voltage constant.

The basic circuit of a linear voltage regulator is shown in Fig. 5.24. The regulating circuit consists of a voltage reference ($V_{\text{ref}}$), a differential amplifier called *error amplifier* using op-amp and a series regulating element $Q_1$ connected as an emitter-follower. The output voltage is sampled and fed back to the inverting input of the error amplifier through the potential divider $R_2 - R_3$. The error amplifier produces an output voltage that is proportional to the difference between the reference voltage and the sampled output voltage and it may be written as $V_o' = A[V_{\text{ref}} - \beta V_o]$, where $A$ is the gain of the amplifier and $\beta$ is the feedback factor which is equal to $R_3/(R_2 + R_3)$. Since the drop across the base-emitter junction of transistor $Q_1$ is small, the output $V_o$ can be approximated to $V_o'$.

Thus, $$V_o' = V_o = A[V_{\text{ref}} - \beta V_o]$$

That is, $$V_o = AV_{\text{ref}}/(1 + A\beta)$$

This equation implies that the output voltage is determined by the reference voltage and the feedback factor.

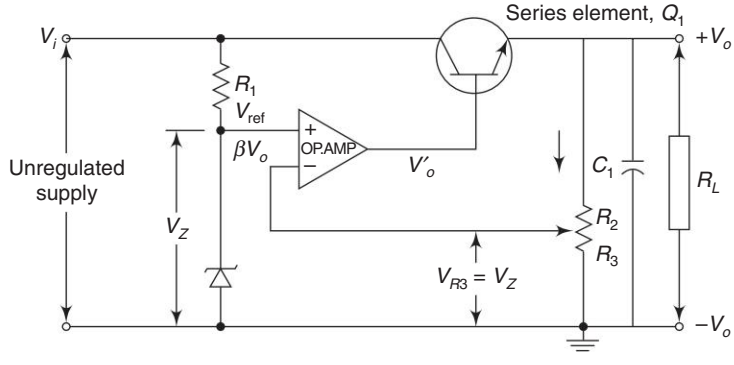



**Fig. 5.24** *Basic circuit of a linear voltage regulator*

The output voltage thus, obtained is kept at a constant level by the control of a series element connected with the error-amplifier. For instance, an increase in output voltage causes a corresponding decrease in the error

amplifier output, which biases the series control transistor with reduced base current. This action causes an increase in collector-to-emitter voltage and thus the increase in the output is reduced.

On the other hand, when the output voltage reduces, the output of the differential amplifier increases. Then, the series transistor is biased heavily at its base and as a consequence, the collector-to-emitter voltage decreases. Thus, the reduction in output is compensated and the output voltage is maintained constant.

## EXAMPLE 5.38

Referring to Fig. 5.24, design a linear voltage regulator to produce an output of 15 V with a maximum load current of 50 mA.

**Solution** Refer to Fig. 5.24. We know that,

$$V_{i(\min)} = V_o + 3\text{ V} = 15 + 3 = 18\text{ V}$$

Assuming the ripple voltage $V_r = 2$ V (max), the input voltage is

$$V_i = V_{i(\min)} + \frac{V_r}{2} = 18 + 1 = 19\text{ V}$$

Therefore, the input voltage, $V_i = 19$ V with a 2 V (max.) ripple superimposed

Then $$V_Z = \frac{V_i}{2} = \frac{19}{2} = 9.5\text{ V}$$ (use the Zener diode 1N758 for 10 V)

Therefore, $$V_Z = 10\text{ V}$$

$$I_z \approx 20\text{ mA}$$

$$R_1 = \frac{V_i - V_Z}{I_Z} = \frac{19 - 10}{20 \times 10^{-3}} = 450\ \Omega$$

Let $$I_2 = I_{B(\max)} = 50\ \mu\text{A}$$

$$R_2 = \frac{V_o - V_Z}{I_2} = \frac{15 - 10}{50 \times 10^{-6}} = 100\ \text{k}\Omega$$

$$R_3 = \frac{V_Z}{I_2} = \frac{10}{50 \times 10^{-6}} = 200\ \text{k}\Omega$$

Select $$C_1 = 50\ \mu\text{F}.$$

*Specification of Transistor* $Q_1$

$$V_{CE(\max)} = V_{i(\max)} = V_i + V_r/2 = 19 + 2/2 = 20\text{ V}$$

$$I_E = I_L = 50\text{ mA}$$

$$P = V_{CE} \times I_L = (V_i - V_o) \times I_L$$

$$= (16 - 15) \times 50 \times 10^{-3} = 200\text{ mW}$$

Use the transistor 2N718 for $Q_1$.

***Principle of Obtaining a Dual-Tracking Voltage Regulator*** The circuit diagram of a dual-tracking voltage regulator using op-amps is shown in Fig. 5.25. The top half of the circuit is similar to the single polarity positive voltage regulator shown in Fig. 5.24. The bottom half of the circuit consisting of the components op-

amp $A_2$, *PNP* transistor $Q_2$, resistors $R_4$ and $R_5$, and capacitor $C_2$ constitutes a negative voltage regulator. The reference voltage for the negative voltage regulator is provided by the output of the positive voltage-regulator circuit. The potential divider $R_4$ and $R_5$ is connected between the positive and negative output terminals. Any change in the negative voltage output is applied to the op-amp $A_2$, which amplifies and inverts to correct the change accordingly. When the resistors $R_4$ and $R_5$ are made equal, the output voltage between the positive and negative terminals is exactly twice the positive voltage. This gives a negative output that is equal to the positive output. This type of negative voltage regulator is called a *tracking regulator*, since the negative voltage output tracks the change in the positive output voltage.

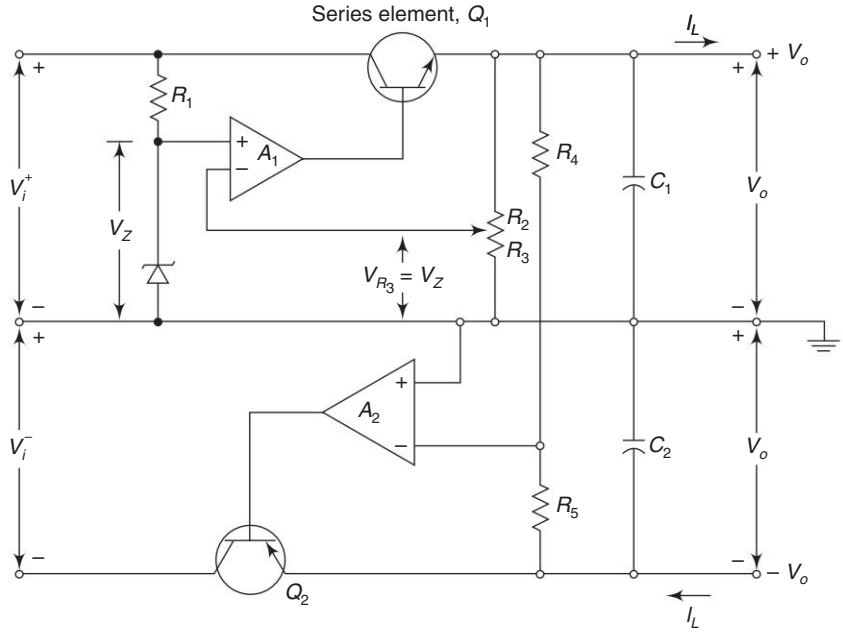



**Fig. 5.25** *Dual-tracking voltage regulator using op-amps*

The arrangement of this type of *plus-minus* power supply is possible only when there is no ground connection in the unregulated power supply.

## 5.10 LINEAR SHUNT AND SERIES VOLTAGE REGULATOR

***Transistorized Shunt Regulator*** In the transistorized shunt voltage regulator shown in Fig. 5.26, the output voltage is determined by the voltage drop across series resistor $R_s$. If $I_L$ increases due to a load change, $V_o$ will tend to decrease. However, the voltage across $R_2$ will also decrease, thereby reducing the forward bias on the transistor and driving it to cut-off. This results in less current flow through the transistor, thereby maintaining $I_s$ almost constant, which keeps the voltage drop across $R_s$ relatively unchanged. Thus, for a given input voltage, output voltage $V_o = V_i - I_s R_s$, remains substantially constant. The major drawback in this circuit is the large amount of power dissipated in $R_s$.

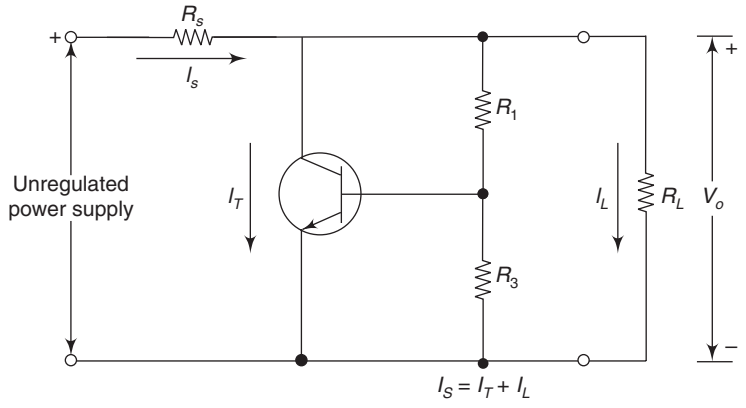



**Fig. 5.26** *Transistorized shunt regulator*

***Transistorized Series Regulator*** If $R_s$ is replaced by a transistor as shown in Fig. 5.27, a more efficient circuit results which is more sensitive to voltage changes and provides better regulation.

Transistor $Q_2$ actually serves as a differential amplifier in which the fraction of the output voltage $\beta V_o$ is compared with reference voltage $V_Z$. The difference ($\beta V_o - V_Z$) is amplified by $Q_2$ and appears at the base of $Q_1$. This in turn determines the voltage drop that will occur across $Q_1$. Because of the gain of $Q_2$, it requires only a small change in $V_o$ to have a large effect on $Q_1$. Further, the output voltage may be varied over a wide range using $R_2$. The Zener diode and transistor $Q_2$ can be chosen so that the temperature coefficients practically cancel.

If $R_2$ is adjusted for a lower output voltage, a greater voltage drop occurs across $Q_1$. Maximum dissipation in $Q_1$ thus takes place at high load currents and low-output voltage in variable regulated power supplies employing a series regulator.

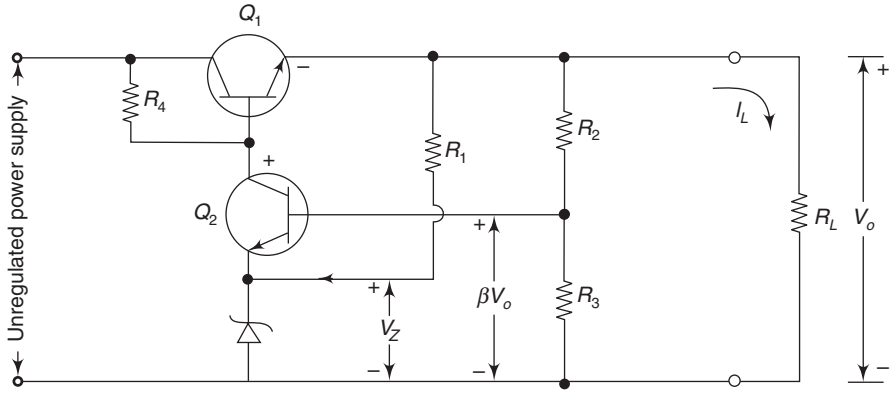



**Fig. 5.27** *Transistorized series regulator*

***Drawback of Transistorized Series Regulator*** The transistorized series voltage regulator has the limitation that the output voltage available is restricted by the $V_{CEO}$ of the series transistor used. The power rating of the transistor used, as a series loser, depends on the voltage difference between the input and

output voltages. This difficulty can be minimized to a great extent by using thyristors. Thyristors have the ability to control large power with minimal control power, and this control power does not have to remain continuous as in the case of the base current of a transistor. Transistors for a relatively high-voltage, high power operations are rarely available.

## EXAMPLE 5.39

Design a series voltage regulator with the following specifications: $V_o$ = 20 V; $V_i$ = (22 – 30) V; $I_{L\,(max)}$ = 50 mA.

**Solution** Refer Fig. 5.27.

Selection of Zener diode

$$R_{L\,min} = \frac{V_o}{I_{L(max)}} = \frac{20}{50 \times 10^{-3}} = 400\ \Omega$$

$$V_Z \approx \frac{V_o}{2} = \frac{20}{2} = 10\ \text{V}$$

Hence, the Zener diode 0.5 Z10 is chosen.

Since $$I_{R1} > I_{B2},\ I_{R1} > \frac{I_{C2}}{\beta}, I_{R1} > \frac{10 \times 10^{-3}}{150}$$

$$I_{R1} > 66.7\ \mu\text{A}$$

Let $$I_{R1} \approx I_{R2} \approx I_{R3} = 10\ \text{mA (neglecting } I_{B2})$$

and $$I_{C2} \approx I_{E2} = 10\ \text{mA}$$

So, the current flowing through the Zener,

$$I_Z = I_{E2} + I_{R1} = 20\ \text{mA}$$

$$P_Z = V_Z I_Z = 10 \times 20 \times 10^{-3}$$

$$= 0.2\ \text{W} < 0.5\ \text{W}$$

Hence, selection of the 0.5 WZ10 Zener diode is confirmed.

*Selection of Transistor $Q_1$*

$$I_{E1} = I_{R1} + I_{R2} + I_L$$

$$= (10 + 10 + 50)\ \text{mA} = 70\ \text{mA}$$

$$V_{i\,(max)} - V_0 = 30 - 20 = 10\ \text{V}$$

For the transistor SL100, the ratings are

$$I_{C(max)} = 500\ \text{mA}$$

$$V_{CE(max)} = 50\ \text{V}$$

$$h_{FE} = 50 \text{ to } 280$$

Hence, SL100 can be chosen for $Q_1$.

*Selection of Transistor $Q_2$*

From the figure, $V_{CE2(\max)} + V_Z = (V_o + V_{BE1})$

Therefore, $V_{CE2(\max)} = (V_o + V_{BE1}) - V_Z = 20.6 - 10 = 10.6$ V

For the transistor BC107, the ratings are

$$V_{CEO(\max)} = 45 \text{ V}$$

$$I_{C(\max)} = 200 \text{ mA}$$

$$h_{FE} = 125 - 300$$

Hence, the transistor BC107 is selected for $Q_2$.

*Selection of resistors $R_1$, $R_2$, and $R_3$*

$$V_{R1} = V_o - V_Z = 20 - 10 = 10 \text{ V}$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{10}{10 \times 10^{-3}} = 1 \text{ k}\Omega$$

$$V_{R2} = V_o - V_{R3} = 20 - 10.6 = 9.4 \text{ V}$$

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{9.4}{10 \times 10^{-3}} = 940 \ \Omega$$

$$V_{R3} = V_Z + V_{BE2(\text{sat})} = 10 + 0.6 = 10.6 \text{ V}$$

$$R_3 = \frac{V_{R3}}{I_{R3}} = \frac{10.6}{10 \times 10^{-3}} = 1060 \ \Omega$$

*Selection of Resistor $R_4$*

$$V_{B1} = V_{C2} = V_o + V_{BE1} = 20 + 0.6 = 20.6 \text{ V}$$

$$I_{B1} = \frac{I_{C1}}{\beta} = \frac{70 \times 10^{-3}}{50} = 1.4 \text{ mA}$$

$$I_{R4} = I_{B1} + I_{C2} = 11.4 \text{ mA}$$

$$R_{4(\max)} = \frac{V_{R4(\max)}}{I_{R4}} = \frac{V_{i(\max)} - V_{B1}}{I_{R4}}$$

$$= \frac{30 - 20.6}{11.4 \times 10^{-3}} = 825 \ \Omega$$

$$R_{4(\min)} = \frac{V_{R4(\min)}}{I_{R4}} = \frac{V_{i(\min)} - V_{B1}}{I_{R4}}$$

$$= \frac{22 - 20.6}{11.4 \times 10^{-3}} = 123 \ \Omega$$

$$R_4 = \frac{R_{4(\max)} + R_{4(\min)}}{2} = 474 \ \Omega$$

## 5.11 IC VOLTAGE REGULATOR

Although voltage regulators can be designed using op-amps, it is quicker and easier to use IC voltage regulators. Furthermore, the IC voltage regulators are versatile, relatively inexpensive and are available with features such as programmable output, current/voltage boosting and floating operation for high-voltage application. Some important types of linear IC voltage regulators are:

1. Fixed positive/negative output voltage regulators
2. Adjustable output voltage regulators

***Fixed Voltage Regulators*** 78XX series are three terminal, positive fixed voltage regulators. There are seven output voltage options available such as 5, 6, 8, 12, 15, 18, and 24 V. In 78XX, the last two numbers (XX) indicate the output voltage.

79XX series are negative fixed voltage regulators which are complements to the 78XX series devices. There are two extra voltage options of –2 V and –5.2 V available in 79XX series.

Figure 5.28 shows the standard representation of a monolithic voltage regulator. The input capacitor $C_i$ is used to cancel the inductive effects due to long distribution leads and the output capacitor $C_o$ improves the transient response.

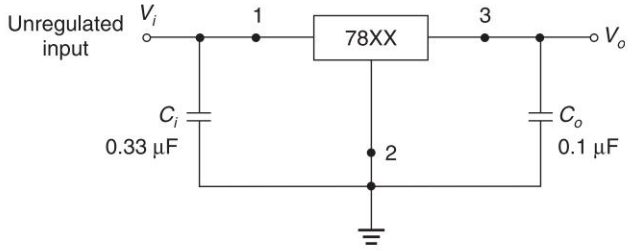



**Fig. 5.28** *Monolithic voltage regulator*

Dual-tracking regulated voltage supplies can be obtained using 7815 and 7915 chips as shown in Fig. 5.29. Type 7815 provides +15 V output and type 7915 provides –15 V output. The advantage of this method is that it can supply a wide range of voltages at much higher currents.

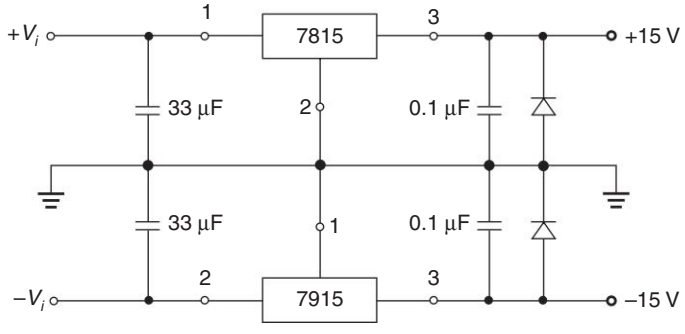



**Fig. 5.29** *Dual-tracking regulator*

***Adjustable Voltage Regulators*** LM 723C is the general-purpose adjustable voltage regulator. The output voltage is adjustable from 2 to 37 V. It will supply output currents up to 150 mA without external pass transistor and output currents excess of 10 A by adding external transistors. It can be used as either a linear or a switching regulator. Also, it can be used as a negative voltage regulator.

***Regulated Function of LM 723C*** The regulating function of this chip will be best understood by considering its internal circuit which is shown in Fig. 5.30.

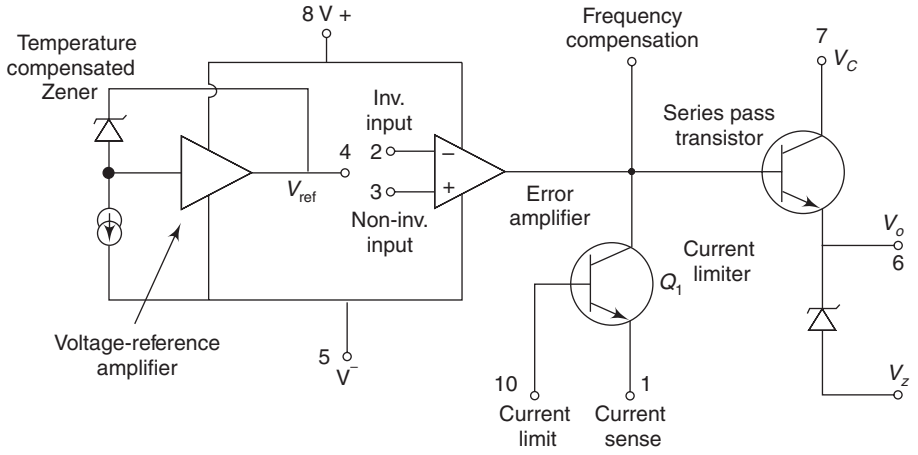



**Fig. 5.30** *Internal circuit of LM 723C*

A reference voltage is developed across the Zener diode which is temperature compensated. The reference amplifier acts as a buffer and so the constant reference voltage is available at its output. The control amplifier has two inputs, one inverting and the other non-inverting. This amplifier compares the reference with a fixed part of the feedback output voltage and the resultant error is amplified. This error voltage controls the series transistor such that the output voltage remains at a constant level. Transistor $Q_1$ is used for current limiting.

The load current can be limited by providing a small resistance $R_{sc}$ between the current limit and current sense terminals. The voltage across $R_{sc}$ is used to bias the current limiting transistor, present inside the chip. Hence, $V_{BE} = I_{\text{limit}} R_{sc}$, where $V_{BE}$ is the bias voltage and $I_{\text{limit}}$ is the limiting current

$$R_{sc} = \frac{V_{BE}}{I_{\text{limit}}}$$

***Short-Circuit Protection*** When the output terminals of a power supply are short-circuited, the load current becomes too high and the power supply unit may be damaged. To guard against such an occurrence, current limiters have to be included in the regulator circuit. Current limiting can be provided by means of a fuse or a resistor ($R_{sc}$), rated for desired value of current. Figure 5.31 shows the regulator with current limiting. The resistance $R_{sc}$ has to be chosen for the desired current limit.

$$R_{sc} = \frac{0.7}{I_{\text{limit}}}$$

By doing this, it is ensured that the power supply is being operated safely.

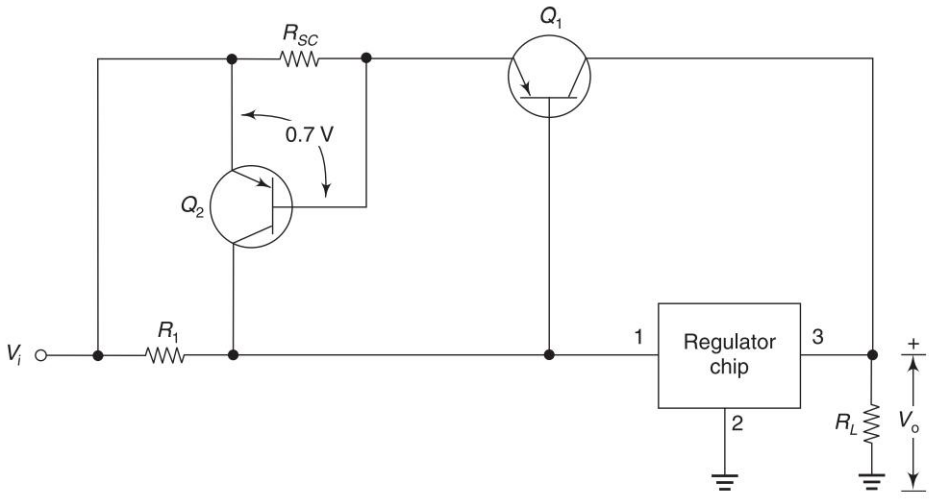



**Fig. 5.31** *Regulator with current limiting*

***Overvoltage Protection*** The overvoltage problems are divided into two types, namely, (i) *spikes* and (ii) *surges*. Spikes are high-voltage transients which last for short duration of few µs. Surges are high-voltage transients which will last for longer duration and will stretch for many ms.

Spike and surge protectors are designed to prevent overvoltages from reaching the system. They absorb excess voltages before they enter the system. Surge protectors are connected between the system and the power line.

The most common overvoltage protection devices are the metal oxide varistors. The varistors can chop and shunt away all voltages above a certain level. These devices are designed to accept voltages as high as 6000 V and divert any voltage above 200 V to ground.

The excess energy does not disappear but turns into heat possibly destroying the varistors. The most important characteristic of overvoltage protection devices are how fast they work and how much energy they can dissipate. Other than varistors, semiconductors, ionized spark-gaps, and ferro-resonant transformers are also used as surge protectors.

## 5.12 SWITCHING VOLTAGE REGULATOR

A switching regulator converts a dc input voltage to another dc output voltage, either lower or higher. But the switching regulator does voltage regulation i.e., pulse width modulation controls the ON-OFF time of the transistor. By varying the duty cycle, it maintains the output voltage constant at different line and load conditions. The larger the duty cycle, the larger will be the dc voltage.

Similar to a linear voltage regulator, a switching voltage regulator with the series-pass transistor efficiently transfers power to the load. This pass transistor is switched ON and OFF. The switching regulator passes voltage to the load in pulses. The LC filter provides a smooth dc voltage.

The switching voltage regulator may be classified as

(i) Forward, step-down, or buck converter (output voltage is lower than the input voltage)
(ii) Step-up or boost converter (output voltage is higher than the input voltage)
(iii) Inverting or flyback converter (polarity of output voltage is opposite to the input voltage)

The basic components of a step-down switching voltage regulator are shown in Fig. 5.32. The regulating circuit consists of an oscillator, voltage reference, a differential amplifier called error amplifier or voltage comparator using op-amp, a diode D, a filter and a series regulating element $Q_1$, connected as an emitter follower.

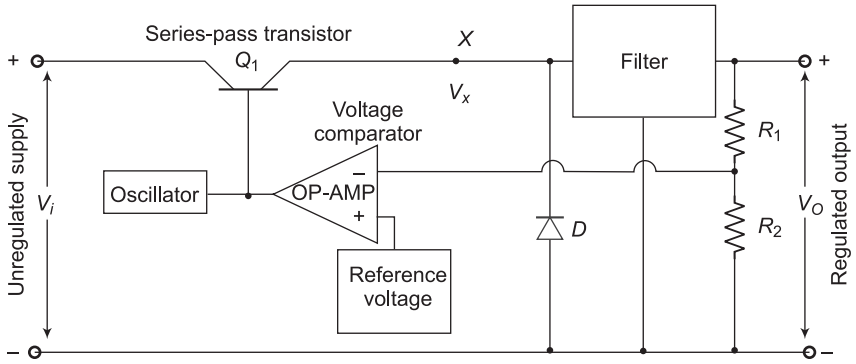



**Fig. 5.32** *Switching voltage regulator*

The output voltage is sampled and fedback to the inverting input of the error amplifier through the potential divider $R_1 - R_2$. The voltage comparator and oscillator control the duty cycle of the pulses. The oscillator and error input from the op-amp drive the control element, which allows current to the load accordingly and keeps the output voltage constant.

The switching regulator waveforms are shown in Fig. 5.33. The dc input voltage, $V_i$, is converted into a pulse waveform $V_x$ by the control of a series element $Q_1$ which acts as a switch turning ON and OFF. The oscillator switches $Q_1$ ON which makes current to flow to the filter and the output voltage to rise.

The error amplifier compares the sampled output voltage to the reference voltage and $Q_1$ will be ON until the voltage feedback equals the reference voltage. Then, $Q_1$ is turned OFF again. A pulse waveform $V_x$ is generated at the input of the filter by $Q_1$ turning ON and OFF. The filter consisting of an inductor and capacitor smooths the pulse waveform to produce a dc output voltage $V_O$ with ripple.

The controlling element acts as a pulse width modulator.

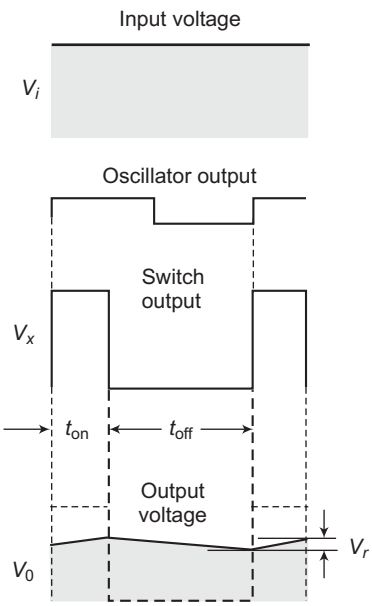



**Fig. 5.33** *Switching voltage waveforms*

## 5.13 OVER-VOLTAGE PROTECTION USING BJT AND MOSFET

When the input voltage exceeds the normal value, the peak current of the step-down converter type switching regulator becomes high for the internal transistor and an external device may be employed using BJT or MOSFET. Figure 5.34 shows the over-voltage protection circuit for switching regulator using BJT and MOSFET. Figure 5.34(a) shows the connection of external BJT with a step-down converter. Here, proper value of base resistor $R_B$ is chosen for transistor $Q_2$ such that $Q_2$ is biased OFF, when the internal transistor $Q_1$ is turned OFF.

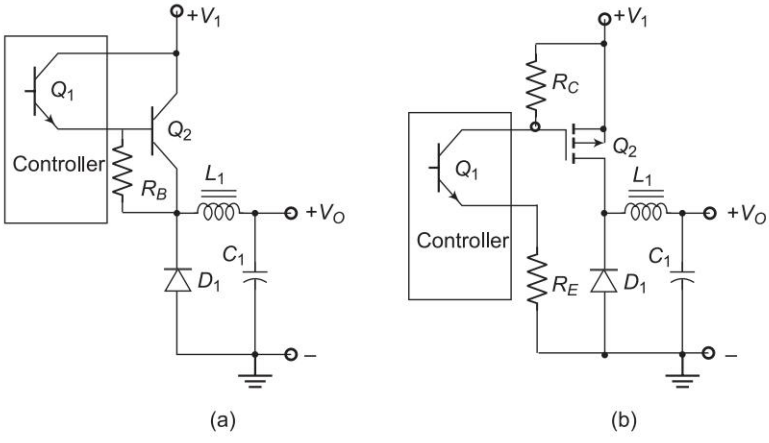



**Fig. 5.34** *Over-voltage protection circuit of step-down converter using (a) BJT and (b) MOSFET*

Figure 5.34(b) shows the connection of external P-channel enhancement MOSFET with switching controller. Here, proper value of collector resistor $R_C$ for transistor $Q_2$ and emitter resistor $R_E$ for transistor $Q_1$ should be chosen to provide gate-channel voltage such that transistor $Q_2$ switches ON when transistor $Q_1$ is turned ON.

## 5.14 SWITCHED MODE POWER SUPPLY (SMPS)

The dc to dc converters and dc to ac converters belong to the category of Switched Mode Power Supplies (SMPS). The SMPS operating from mains, without using an input transformer at line frequency 50 Hz is called "off-line switching supply". In off-line switching supply, the ac mains is directly rectified and filtered and the dc voltage so obtained is then used as an input to a switching type dc to dc converter.

The various types of voltage regulators used in LPS, fall in the category of dissipative regulator, as it has a voltage control element (transistor or Zener diode) which dissipates the power equal to the voltage difference between an unregulated input voltage and a fixed output voltage multiplied by the current flowing through it. The switching regulators solve the above problem. The switching regulator acts as a continuously variable power converter and hence, its efficiency is negligibly affected by the voltage difference. Therefore, the switching regulator is also known as *non-dissipative regulator*.

In a switching power supply, the active device that provides regulation is always operated in a switched mode, i.e., it is operated either in cut-off or in saturation. The input dc is chopped at a high frequency (15 to 50 kHz) using an active device (bipolar transistor, power MOSFET, or SCR) and the converter transformer. Here, the size of the ferrite core reduces inversely with frequency. The lower limit is defined at about 15 kHz by the requirement for silent operation and the upper limit of 50 kHz is to limit losses in the choke and in the active switching elements. The transformed chopped waveform is rectified and filtered. A sample of the output voltage is used as the feedback signal for the drive circuit for the switching transistor to achieve regulation.

Figure 5.1(b) shows the concept of a switching regulator in simple form. The added elements are control logic and oscillator. The oscillator allows the control element to be switched ON and OFF. The control element usually consists of a transistor switch, an inductor and a diode. For each switch ON, energy is pumped into the magnetic field associated with the inductor which is a transformer winding in practice. This energy is then released to the load at the desired voltage level. By varying the duty cycle or frequency of switching, one can vary the stored energy in each cycle and thus, control the output voltage. As a switch can only be ON or OFF, it either allows energy to pass or stop, but does not dissipate energy itself. Since only the energy required to maintain the output voltage at a load current is drawn, there is no dissipation and hence, a higher efficiency is obtained. Energy is pumped in discrete lumps, but the output voltage is kept steady by capacitor storage.

The major feature of SMPS is the elimination of physically massive power transformers and other power line magnetics. The net result is a smaller, lighter package and reduced manufacturing cost, resulting primarily from the elimination of the 50 Hz components.

***dc to dc Converter*** The block diagram of dc to dc converter (SMPS) is shown in Fig. 5.36(a). Here, the primary power received from ac main is rectified and filtered as high-voltage dc. It is then switched at a high rate of speed approximately 15 kHz to 50 kHz and fed to the primary side of a step-down transformer. The step-down transformer is only a fraction of the size of a comparable 50 Hz unit thus, relieving the size and weight problems. The output at the secondary side of the transformer is rectified and filtered. Then it is sent to the output of the power supply. A sample of this output is sent back to the switch to control the output voltage.

SMPS rely on PWM to control the average value of the output voltage. The average value of a repetitive pulse waveform depends on the area under the waveform. If the duty cycle is varied as illustrated in Fig. 5.35, the average value of the voltage changes proportionally.

As the load increases, output voltage tends to fall. Most switching power supplies regulate their output using a method called *Pulse-Width Modulation (PWM)*. The power switch which feeds the primary side of the step-down transformer is driven by a pulse-width modulated oscillator. When the duty cycle is at 50%, the maximum amount of energy will be passed through the step-down transformer. As the duty cycle is decreased, less energy will be passed through the transformer.

The width or ON time of the oscillator is controlled by the voltage feedback from the secondary rectifier output, and forms a closed loop regulator. As shown in Fig. 5.36(b), the pulse width given to the power switch is inversely proportional to the output voltage. When the output voltage drops, the switch is ON for longer time, resulting in more energy delivered to the transformer and a higher output voltage. As the output voltage raises, the ON time becomes shorter until the loop stabilises.

Since the switching regulator circuit is complex, modern IC packages like Motorola MC 3420/3520 or Silicon General SG 1524 can be used instead of discrete components.

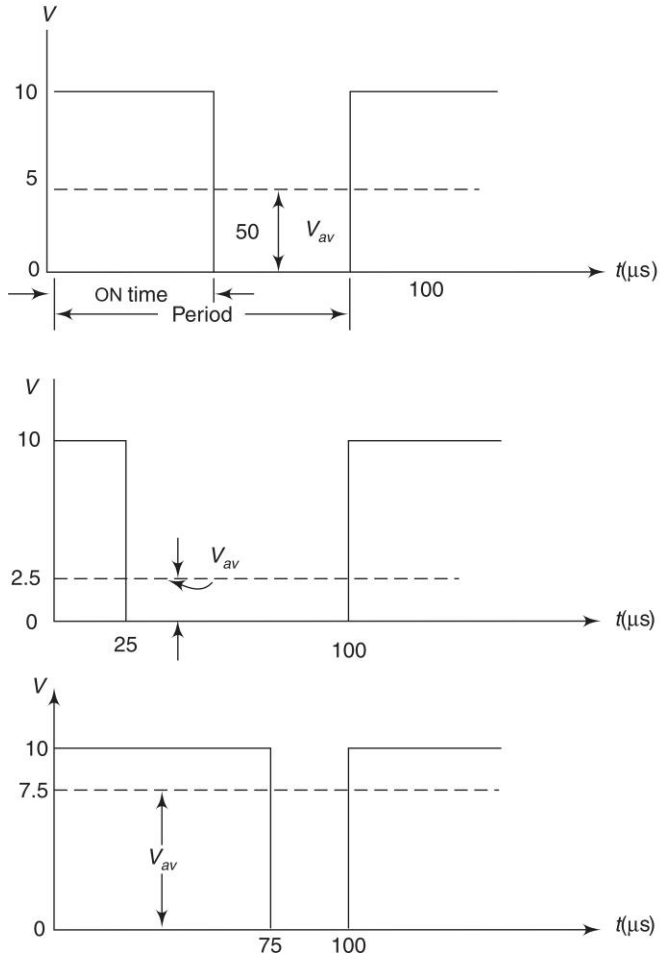



**Fig. 5.35** *Pulse width modulation and average value*

### *Different Types of SMPS*

The four types of switched mode power supplies commonly employed, depending upon the intended application, are (a) forward or step-down converter, (b) step-up converter (c) flyback converter, and (d) push–pull converter.

**Forward Converter** In the forward step-down or buck converter, as shown in Fig. 5.37, the choke carries current when the transistor is conducting or not. The diode carries the current during the OFF period of the transistor. Therefore, energy flows into load during both periods. The output voltage $V_o$ can only be less than $V_s$ in this circuit. The choke stores energy during the ON period and also passes some energy into the output load. The diode serves two functions: (i) It provides a discharge path for the choke so that, when the transistor switch opens, there is no arcing due to induced high-voltage, and (ii) it provides a path for the current in the coil to decay.

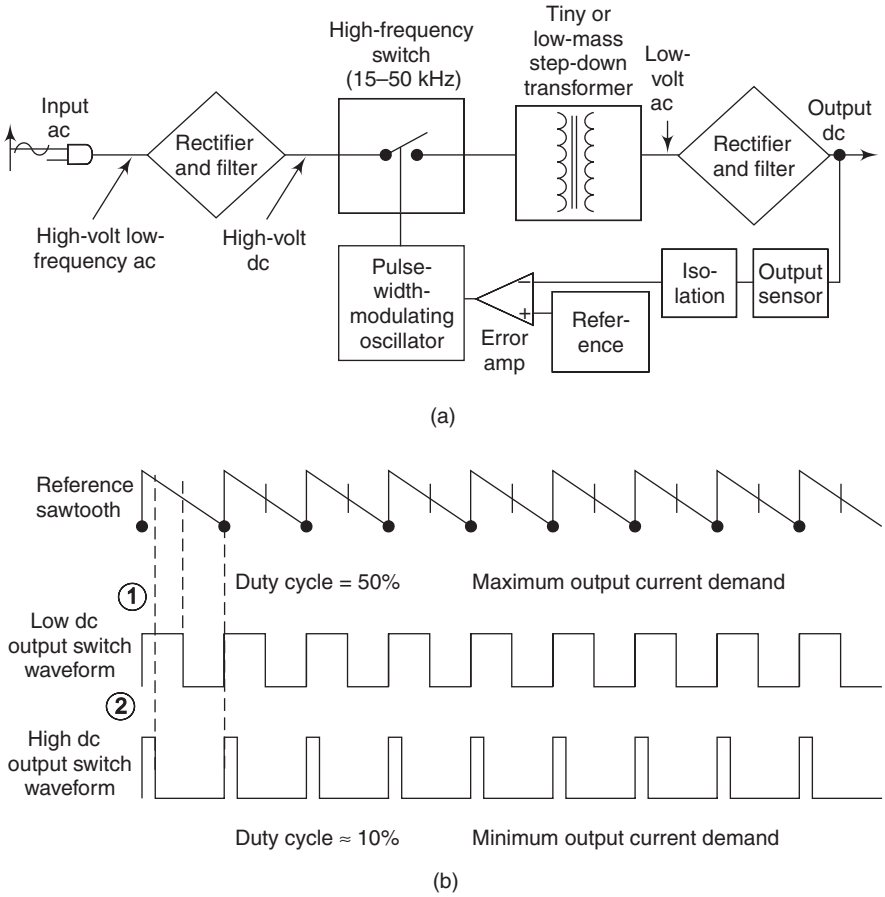



**Fig. 5.36** *(a) Block diagram of switching power supply (b) Switching power supply waveforms*

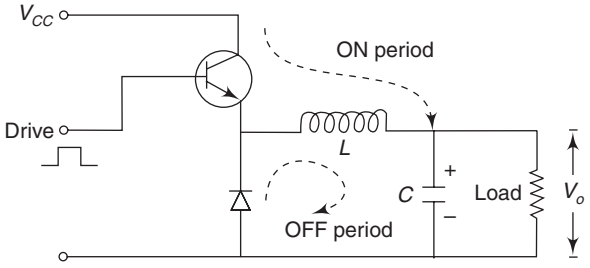



**Fig. 5.37** *Circuit diagram of a forward step down converter*

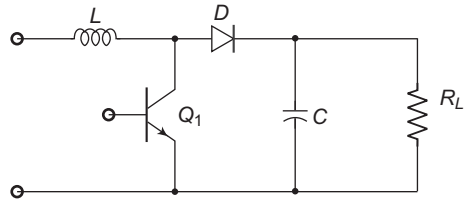



**Fig. 5.38** *Circuit of step-up converter*

**Step-up Converter** A step-up converter or boost converter shown in Fig. 5.38 produces a dc output voltage larger than its input voltage. Here, the inductor $L$ is connected to the supply voltage and diode $D$ is connected in series with inductor $L$ and capacitor $C$. The collector of transistor $Q$ is connected to the junction of inductor $L$ and diode $D$ and its emitter is grounded.

When $Q_1$ is ON, the diode $D$ is reverse biased. Therefore, the output voltage across inductor is

$$V_L = V_i - V_{sat}$$

When $Q_1$ is OFF, the output voltage is

$$V_0 = V_i + V_L - V_F$$

Hence, the output voltage is higher than the input voltage.

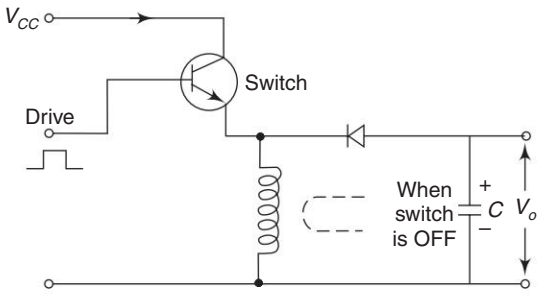



**Fig. 5.39** *Circuit diagram of a flyback converter*

**Flyback Converter** In the flyback converter type as shown in Fig. 5.39, the energy is stored entirely in the magnetic flux of the inductor during the ON period of the switch. The energy is emptied (discharged) into the output voltage circuit when the switch is in the open state. The output voltage depends upon the duty cycle.

***Self-oscillating Flyback Converter*** Figure 5.40 shows the self-oscillating type flyback converter which is the most basic and simple converter based on the flyback principle. A switching transistor, a converter transformer, a fast-recovery rectifier and an output filter capacitor make up a complete dc to dc converter. It is a constant output power converter and so are all other dc to dc converters based on flyback principle.

During the conduction time of the switching transistor, the current through the transformer primary starts ramping up linearly with a slope equal to $V_i/L_p$. The voltage induced in the secondary and the feedback windings make the fast-recovery rectifier reverse biased and hold the conducting transistor ON.

When the primary current reaches a peak value $I_p$, where the core begins to saturate, the current tends to rise very sharply. This sharp rise in current cannot be supported by the fixed base drive provided by the feedback winding. As a result, the switching transistor begins to come out of saturation.

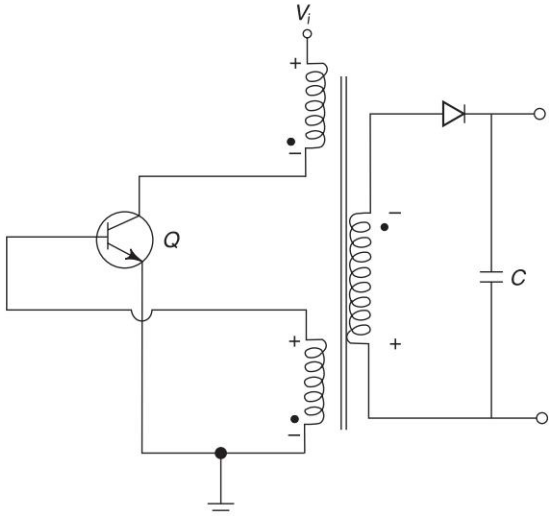



**Fig. 5.40** *Self-oscillating flyback converter*

This is a regenerative process with the transistor getting switched OFF. The magnetic field due to the current flowing in the primary winding collapses, thus, reversing the polarities of the induced voltages. The fast-recovery rectifier is forward biased and the stored energy is transferred to the capacitor and load through the secondary winding. Thus, energy is stored during the ON time and transferred during OFF time.

The output capacitor supplies the load current during the ON time of the transistor when no energy is being transferred from the primary side. It is constant output power converter. The output voltage reduces as the load increases and vice versa.

Utmost care should be taken to ensure that the load is not accidentally taken off the converter. In that case, the output voltage would rise without limit till any converter component gets damaged.

It is suitable for low-output power applications due to its inherent nature of operation and may be used with advantage up to an output power of 150 W. It has high output voltage ripple.

**Push–pull Converter** A push–pull converter is the most widely used switching supply belonging to the family of forward converters. There are several different circuit configurations within the push–pull converter sub-family. This circuit differ only in the mode in which the transformer primary is driven.

Figure 5.41 shows the conventional self-oscillating push–pull converter. Its operation can be explained by considering it equivalent to two self-oscillating flyback converters operating alternately.

When the transistor $Q_1$ is in saturation, energy is stored in the upper half of the primary winding when the linearly rising current reaches a value where the transformer core begins to saturate. The current tends to rise sharply which is not supported by a more or less fixed base bias. The transistor starts coming out of saturation.

This is a regenerative process and ends up in switching OFF transistor $Q_1$ and switching ON transistor $Q_2$. Thus, transistors $Q_1$ and $Q_2$ switch ON and OFF alternately. When $Q_1$ is ON, energy is being stored in the upper half of the primary and the energy stored in the immediately preceding half cycle in the lower half of the primary winding (when the transistor $Q_2$ was ON) is getting transferred. Thus, energy is stored and transferred at the same time. The voltage across secondary is a symmetrical square waveform which is then rectified and filtered to get the dc output.

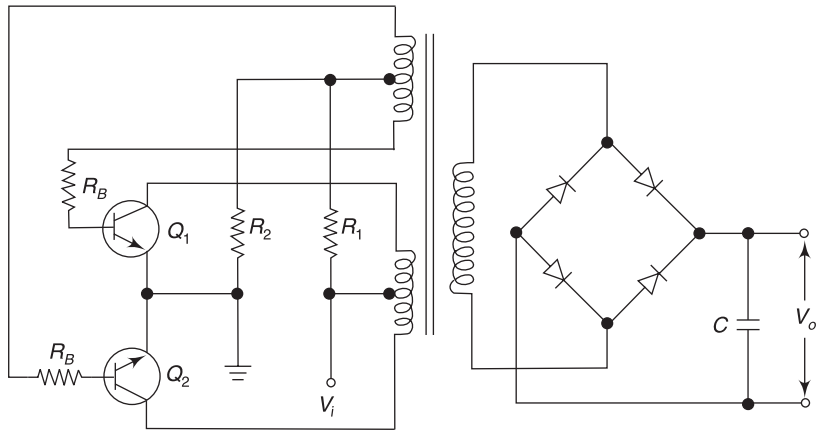



**Fig. 5.41** *Push-pull converter*

***dc to ac Inverter/Uninterrupted Power Supply (UPS)*** The block diagram of *Standby Power Supply* (*SPS*), otherwise called as *off-line UPS* is shown in Fig. 5.42. It is a system that uses a special circuit that senses the ac line current. If the sensor detects a loss of power on the line, the system quickly switches over to a standby power system.

The SPS transfers the load to the inverter which draws its power from the attached batteries. The switching process requires a small but measurable amount of time. First, the failure of the electrical supply must be sensed. Even the fastest electronic voltage sensors take a finite time to detect a power failure. Even after a power failure is detected, there is another slight pause before the computer receives its fresh supply of electricity. If the switch is not fast enough, the system shuts down and reboots which defeats the purpose of the use of the backup power supply.

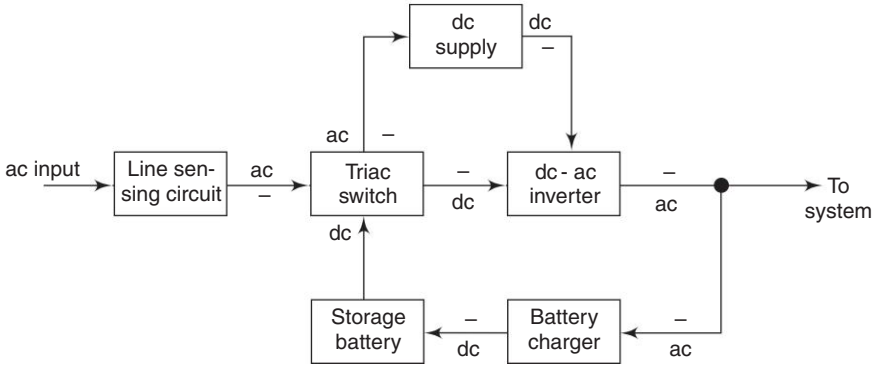



**Fig. 5.42** *Block diagram of standby power supply*

The name *Uninterrupted Power Supply* is self-explanatory. Its output is never interrupted because it does not need to switch its output from linepower to battery. Rather, its battery is constantly and continuously connected to the output of the system through its inverter. It is always supplying power from the battery to the computer. While ac power is available to the UPS, it keeps the UPS battery charged through the rectifier circuits. When the power fails, the charging of the battery is stopped, but the system gets continuous supply from the battery.

It is independent of all the variations of the electrical lines. It is the computer's own generating station keeping it safe from the polluting effects of lightning and load transients. Dips and surges can never reach the computer. The computer gets a smooth, constant electrical supply. The duration for which the UPS powers a system depends not on the rating of the UPS in volt-ampere, but that of the rating of the batteries powering it in ampere-hours. Normally, the UPS comes with a by-pass switch. It helps to directly connect the system to the incoming ac supply if there is any problem with the UPS.

### *Advantages of SMPS*

1. Efficiency is high because of less heat dissipation.
2. As the transformer size is very small, it will have a compact unit.
3. Protection against excessive output voltage by quick acting guard circuits.
4. Reduced harmonic feedback into the supply main.
5. Isolation from main supply without the need of large mains transformer.
6. Generation of low and medium voltage supplies are easy.
7. Switching supplies can change an unregulated input of 24 V into a regulated output of 1000 V dc
8. Though RF interference can be a problem in SMPS unless properly shielded, SMPS in TV sets is in synchronization with the line frequency (15.625 kHz) and thus, switching effects are not visible on the screen.
9. SMPS are also used in personal computers, video projectors, and measuring instruments.

***Comparison between SMPS and Linear Supply*** Table 5.3 gives the comparison between SMPS and linear supply.

**Table 5.3** *Comparison between SMPS and linear supply*

| Feature | SMPS | Linear power supply |
|---|---|---|
| Efficiency | 65–75 per cent | 25–50 per cent |
| Temperature rise | 20–40 °C | 50–100 °C |
| Ripple value | Higher 25 to 50 mV | Even 5 mV possible |
| Overall regulation (percentage drop in volt on load) | 0.3 per cent is common, tighter regulation is difficult to get | Even 0.1 per cent is possible |
| RF interference | Can be a problem unless properly shielded | None |
| Magnetic material | Uses ferrite core | Uses stalloy or CRGO core |
| Weight | About 60 W/kg | 20–30 W/kg |
| Cost | More parts, special ones, increase the cost | Advantage for smaller units up to 10–15 W, but cost is higher if bigger |
| Reliability | Depends upon availability of suitable transistors | More reliable |
| Transient response | Slower (in ms) | Faster (in μs) |
| Complexity | More | Less |

### *Component Selection for SMPS*

**Inductor** In SMPS, the energy conversion is done through storage of energy in the magnetic field of a choke coil (inductor). Energy is stored only during the conduction period of the switching transistor. The amount of energy decides the power capacity of an SMPS. In order to increase energy, large current must be pumped into high inductance. The inductance $L$ is a measure of the flux per ampere of current in the coil. So the energy stored in a coil is given by

$$1/2\ LI^2 = 1/2(\Phi/I)I^2 = 1/2\ \Phi I$$

where $L$ is the inductance of the coil in henry, $\Phi$ is flux linking the coil in weber, and $I$ is current in ampere.

**Core** The flux, $\Phi$, is supported by the magnetic core of the coil. Iron core cannot be used above 400 Hz due to increased core heating. The core material chosen is generally ferrite as it can work at the frequencies which are employed in SMPS. Any frequency above 15 kHz is employed in these supplies, but as frequency increases, the core material must have low energy loss due to hysteresis. At lower frequencies, i.e., below 10 kHz, it is not advantageous to make use of switched mode power supplies. The size of core reduces inversely with frequency. Some companies in the USA are making even 300 kHz SMPS units which need special ferrite material for the core.

The core size decides the value of flux. The core should not be allowed to get saturated by-passing too much direct current around its core. It is advisable to work well below saturation level.

**Transistor** When used as a switch, a transistor internally has a fast switch-on time, ample current rating to withstand surges and a high breakdown voltage rating to withstand the peak induced voltage in the coil at switch off. Switching time should be very small, below 1 μs, comprising turn-on delay, rise time and fall times of current.

**Diode** When used at frequencies of 15 kHz and above, diodes are generally different from the common diffused junction types used at mains frequency. In SMPS, generally one employs switching diodes with either gold-doped junctions or the Schottky barrier diodes which have metal semiconductor junctions. There is not much charge storage in the junction in such switching diodes. The difference between an ordinary diode and a switching diode is apparent in the rectifier waveforms shown in Fig. 5.43.

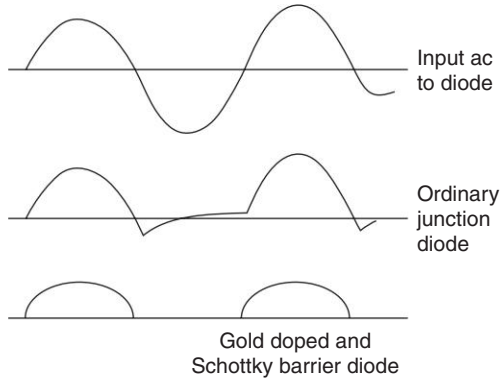



**Fig. 5.43** *Behaviour of ordinary junction and gold-doped diodes at high frequency*

**Capacitor** Electrolytic capacitors used for filtering ripples are necessary for any type of power supply. With power frequency rectifiers, the ripples are at 100 Hz but in SMPS, the frequency of switching is high, of the order of several kHz.

At such frequencies, electrolytic capacitors invariably have a series inductance and a resistance effect. The Equivalent Series Resistance (ESR) of the capacitor is about 0.05 to 0.1 Ω. It grows with frequencies above 10 kHz. The impedance of a capacitor becomes minimum at about 20 kHz, whereupon it increases further as shown in Fig. 5.44. In order to decrease the resistance, it is advisable to employ 2 or 3 capacitors of similar type in parallel rather than use a single one. This reduces the ESR.

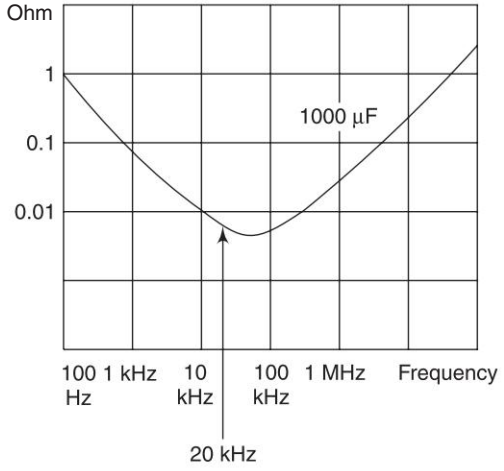



**Fig. 5.44** *Variation of impedance of capacitor*

## 5.15 POWER SUPPLY PERFORMANCE AND TESTING

The basic linear power supply shown in Fig. 5.45 consists of a transformer, bridge rectifier, capacitive filter and zener diode voltage regulator. The transformer reduces the primary line voltage to a lower secondary voltage. The bridge rectifier converts the secondary ac voltage into a positive pulsating dc voltage. The capacitive filter reduces the ripple in the rectifier in dc output voltage. Then the zener voltage regulator

reduces the ripple voltage and keeps the output voltage constant despite variations in load current. Thus, the combination of the above four circuits has converted an ac line voltage to a steady dc output voltage.

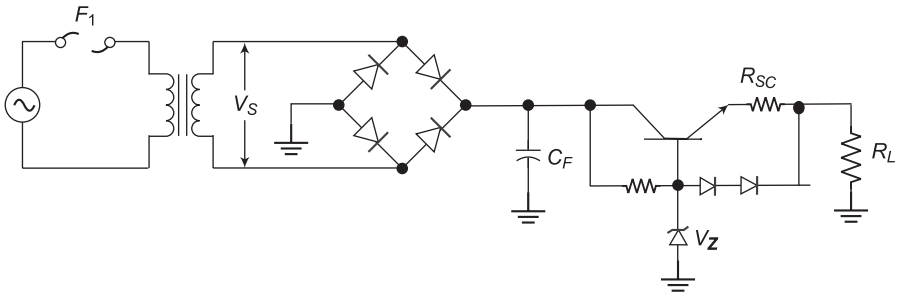



**Fig. 5.45** *Basic linear power supply circuit diagram*

If there is any fault in the performance of the power supply, then an appropriate testing can be done with the help of measurement of voltages at different points by using voltmeter and measurement of resistances at component level by using Ohmmeter. Thus the fault in transformer, rectifier, filter, or voltage regulator can be identified as discussed in the following section.

## 5.16 POWER SUPPLY TROUBLESHOOTING AND FAULT ANALYSIS

The power supply equipment has a rectifier driving a capacitor-input filter followed by a voltage regulator. If the power supply equipment is not functioning properly, then troubleshooting may be started, with the equipment. There are different troubles, including open ground, diodes, filter capacitor, shorted loads and blown fuses.

The faults may occur in the transformer, rectifier diodes, filter, or voltage regulator in power supply unit. When fault occurs in a power supply, the fault can be identified at block level or component level using Ohm's law based on the type of symptom and simple tests.

### *Primary Fuse*

Each power supply unit contains a fuse connected in the series with the primary of the transformer. The primary fuse will blow (open) when the transformer draws the high amount of current. This eliminates the excessive current and protects the power supply. When the fuse is blown, the diodes may be checked for a possible damage and the load resistance for a possible short. The blown fuse must be replaced with the same current rating, voltage rating and original type of body.

The resistance of the primary winding will be around 10 to 50Ω and the resistance of the secondary winding will be 10Ω or less. If the transformer primary is shorted, the primary resistance will be very low and hence, the transformer must be replaced.

### *Transformer Faults*

In a power supply, the transformer may develop a shorted primary or secondary winding, an open primary or secondary winding, or a short between the primary or secondary winding and the transformer frame.

When the primary or secondary winding of the transformer is shorted, the fuse will be blown. In case, if the fuse does not blow, the dc output voltage will be very low and the transformer will be very hot. If the primary or secondary winding reads a very low resistance, then it is found that the winding is shorted.

If the primary or secondary winding of the transformer opens, the output voltage of the power supply will become zero. If the primary or secondary winding reads a very high resistance, then it is found that the winding is open.

If there is a short between the primary or secondary winding and the transformer casing, the fuse will be blown and it measures a low resistance.

If the measurement proves that the transformer is faulty, the transformer must be replaced with the specified ratings.

### *Rectifier Faults*

In power supply, the half-wave rectifier, full-wave rectifier, or bridge rectifier is placed in between the transformer and filter. Rectifiers are generally high-current circuits.

If the diode in the half-wave rectifier opens, the output voltage will be zero. When the diode is shorted, the secondary voltage of the transformer will appear at the output of the half-wave rectifier.

If the diode in the full-wave rectifier is shorted, then the primary fuse will blow. If a diode in the full-wave rectifier opens, the output from the rectifier will be similar to output from a half-wave rectifier.

The symptoms for the diodes in bridge rectifier are shorted or opened are similar to that of full-wave rectifier. The ripple frequency should be 100Hz for a full-wave or bridge rectifier. If the ripple is 50Hz, one of the diodes may be open. If the diodes in any type of rectifier are found faulty, then the diodes must be replaced.

### *Filter Faults*

In the capacitive filter, the capacitor stores an electrical charge and it can retain that charge even after power switch is turned OFF. Before taking out the capacitor for any measurement, the capacitor should be discharged by sorting the terminals with a shorting tool. Hence, for discharging the charge, bleeder resistors are connected across the capacitor. If the filter capacitor is shorted, the primary fuse will blow and it measures a very low resistance. When the electrolyte in the electrolytic capacitors tends to dry out, the capacitor tends to lose capacity and value of capacitor will decrease and hence, the ripple voltage will increase.

When the power supply has a dc output voltage that is approximately half its rated value and a large amount of ripple voltage occurs, which is a symptom caused by an open filter capacitor. Hence, the capacitor filter must be replaced.

### *Zener Regulator Faults*

If a zener diode is shorted, the power supply output will be similar to that of a filtered rectifier. If the zener diode opens, both the peak output voltage and ripple will increase. Hence, there is a loss in voltage regulation and the output voltage will not be maintained constant.

### *Secondary Fuses*

A fuse is installed in the secondary output of the transformer. A main purpose of using multiple fuses in the secondary is that if one section of a power supply fails causing a blown fuse, then the rest of the system will remain working.

## 5.17 DESIGN OF REGULATED DC POWER SUPPLY

In the previous sections, the design of different regulated dc power supplies has been discussed. The design of dc power supply using zener diode is given in Examples 5.30 to 5.37. The design of a linear voltage regulator

is given in Example 5.38 and the design of a series voltage regulator is given in Example 5.39.

The following example provides an overall idea for the design of a linear mode power supply using transformer, bridge rectifier, capacitor filter and series voltage regulator with short-circuit protection to convert the available domestic 230 V, 50 Hz ac to 9 V, 100 mA dc power supply.

## EXAMPLE 5.40

A system needs to be powered with 9 V dc source of maximum load current 100 mA. Design a circuit to supply power with the available domestic ac line. Assume any data required, but reasonably. Provide short circuit protection.

**Solution** The secondary output of step-down transformer is $\sqrt{2}$ times the output dc voltage required. Therefore, the step-down transformer is wound to have 230 V:13 V.

*Given data:* The dc output voltage = 9 V and Load current = 100 mA

The current rating is 1.5 times the maximum load current, i.e., 150 mA.

A bridge rectifier or full-wave rectifier is used to get the pulsating dc output.

$$R_L = \frac{V_{\text{dc}}}{I_L} = \frac{9}{100 \times 10^{-3}} = 90\ \Omega$$

A capacitor filter is used to remove the ripple and get a smooth output.

$$\text{Ripple factor } \Gamma = \frac{1}{4\sqrt{3}\, fC R_L}$$

Assume the ripple factor to be 0.03.

$$C = \frac{1}{4\sqrt{3} \times 50 \times 0.03 \times 90} = 1069\ \mu\text{F} \approx 1000\ \mu\text{F}$$

The short-circuit resistance $R_{sc}$ connected with the series pass transistor is

$$R_{sc} = \frac{V_{BE}}{I_{\text{limit}}} = \frac{0.7}{150 \times 10^{-3}} \approx 4.7\ \Omega$$

Assume 7.6 V Zener diode in series with 1.5 kΩ.

The designed circuit is shown in Fig. 5.46.

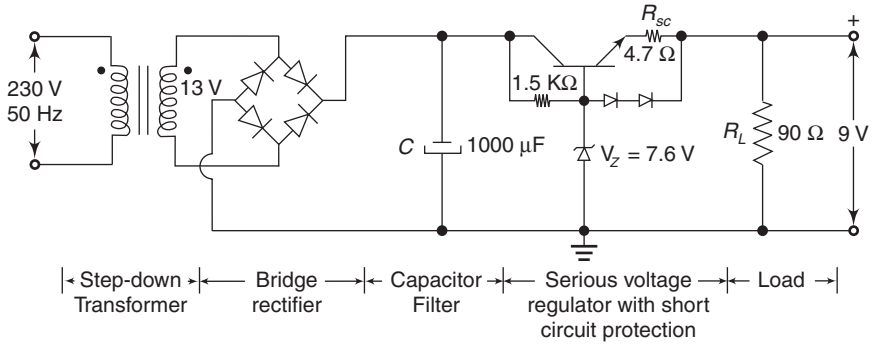



**Fig. 5.46** *Designed circuit for 9 V, 100 mA output with short-circuit protection*

## REVIEW QUESTIONS

**1.** What are the different types of power supplies?
**2.** What is the main difference between LPS and SMPS?
**3.** Briefly explain the operation of linear power supply.
**4.** What are the requirements of the LPS?
**5.** What is a rectifier?
**6.** Show that a *PN* diode works as rectifier.
**7.** Define the following terms:
(i) ripple factor (ii) peak inverse voltage (iii) efficiency (iv) transformer utilization factor (v) form factor (vi) peak factor.
**8.** Draw the circuit diagram of an half-wave rectifier, and explain its operation.
**9.** Derive expressions for rectification efficiency, ripple factor, transformer utilization factor, form factor, and peak factor of an half-wave rectifier with resistive load.
**10.** A half-wave rectifier has a load of 3.5 kΩ. If the diode resistance and secondary coil resistance together have a resistance of 800 Ω and the input voltage has a signal voltage of peak value 240 V, calculate
(i) Peak, average and rms value of current flowing
(ii) dc power output
(iii) ac power input
(iv) Efficiency of the rectifier
[*Ans.* (i) 55.81 mA, 17.78 mA and 27.9 mA (ii) 1.1 W (iii) 3.35 W (iv) 32.9%]
**11.** Explain the action of a full-wave rectifier and give waveforms of input and output voltages.
**12.** Derive expressions of dc or average value of voltage and rms value of voltage of a full-wave rectifier with resistive load.
**13.** Derive an expression for a ripple factor in a full-wave rectifier with resistive load.
**14.** Determine the value of ripple factor in the full-wave rectifier operating at 50 Hz with a 100 μF capacitor filter and 100 Ω load. [*Ans.* 29%]
**15.** Show that a full-wave rectifier is twice as efficient as a half-wave rectifier.
**16.** Describe the action of a full-wave bridge rectifier.
**17.** What are the advantages of a bridge rectifier?
**18.** Compare half-wave, full-wave and bridge rectifiers.
**19.** What is the need for filters in power supplies?
**20.** Explain the various types of filters used in power supplies.
**21.** Obtain the ripple factor of a full-wave rectifier with shunt capacitor filter.
**22.** Derive an expression for the ripple factor in a full-wave rectifier using inductor filter.
**23.** Compare the performance of inductive, L-section and $\pi$-section filters.
**24.** An $L-C$ filter is to be used to provide a dc output with 1% ripple from a full-wave rectifier operating at 50 Hz. Assuming $L/C = 0.01$, determine the required values of $L$ and $C$. [*Ans.* 1.093 H, 109.27 μF]
**25.** In a full-wave rectifier using an $L-C$ filter, it is known that $L = 10$ H, $C = 100$ μF, and $R_L = 500$ Ω. Calculate $I_{dc}$, $V_{dc}$, $I_{ac}$, $V_{ac}$ if $V_m = 30$ V and $f = 50$ Hz. [*Ans.* 38.2 mA, 19.1 V, 1.43 mA, 22.7 mV]
**30.** List three reasons why an unregulated supply is not good enough for some applications.
**31.** Define line regulation and load regulation in a voltage regulator.
**32.** How does a Zener diode maintain constant output voltage?
**33.** Design a Zener shunt regulation with the following specifications:
$V_o = 15$ V, $V_i = 20$–$25$ V, $I_L = 25$–$50$ mA, $I_Z = 20$–$45$ mA
**34.** Describe the operation of emitter-follower type voltage regulator.
**35.** Explain the principles of obtaining regulated power supply.

**36.** Describe the operation of transistorized shunt regulator.

**37.** Describe the operation of transistorized series regulator.

**38.** Design a series voltage regulator to provide an output voltage of 30 V and supply a load current up to 1 A. The input voltage varies from 40 to 50 V.

**39.** Draw the short-circuit, overload protection circuit and explain its operation.

**40.** How is short-circuit current protection provided for an IC voltage regulator?

**41.** Mention the advantages of IC voltage regulators.

**42.** Explain the operation of switched-mode power supply in detail with a block diagram.

**43.** What are the two methods of conversion techniques used in SMPS/Uninterrupted power supply?

**44.** List out the advantages of SMPS.

**45.** Compare linear and switched-mode power supplies.

**46.** The turns ratio of the transformer used in a half-wave rectifier is 2:1 and the primary is connected to 230 V, 50 Hz power mains. Assuming the diodes to be ideal, determine (i) dc voltage across the load, (ii) PIV of each diode, and (iii) medium and average values of power delivered to the load having a resistance of 200 Ω. Also find the efficiency of the rectifier and output ripple frequency.

[*Ans.* 51.7 V, 162.2 V, 132.2 W, 13.5 W, 10.21%, 50 Hz]

**47.** In a full-wave rectifier, the voltage applied to each diode is 240 sin 377*t*, the load resistance is $R_L$ = 2000 Ω and each diode has a forward resistance of 400 Ω. Determine the (i) peak value of current, (ii) dc value of current, (iii) rms value of current, (iv) rectifier efficiency, (v) ripple factor, and (vi ) output ripple frequency. [*Ans.* 100 mA, 63.8 mA, 70.7 mA, 67.6%, 0.482, 120 Hz]

**48.** In a bridge rectifier, the transformer is connected to 220 V, 60 Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diodes to be ideal, find (i) the voltage across the load, (ii) $I_{dc}$ and (iii) PIV. [*Ans.* 18 V, 18 mA, 28.28 V]

**49.** In a full-wave rectifier, the transformer rms secondary voltage from centre tap to each end of secondary is 50 V. The load resistance is 900 Ω. If the diode resistance and transformer secondary winding resistance together has a resistance of 100 Ω. Determine the average load current and rms value of load current. [*Ans.* 45 mA, 50 mA]

**50.** A Zener diode shunt regulator circuit is to be designed to maintain a constant load current of 400 mA and voltage of 40 V. The input voltage is 90 ± 5 V. The Zener diode voltage is 40 V and its dynamic resistance is 2.5 Ω. Find the following quantities for the regulator: (i) the series dropping resistance, (ii) Zener power dissipation, and (iii) load resistance. Assume the Zener current to be 10% of load current.

[*Ans.* 112.5 Ω, 3.6 Ω, 100 Ω]

**51.** In a half-wave rectifier, an ac voltage of peak value 24 V is connected in series with a silicon diode and load resistance of 480 Ω. If the forward resistance of the diode is 20 Ω, find the peak current flowing through the diode.

[*Ans.* 46.6 mA]

**52.** A Zener diode voltage regulator shown in Fig. 5.18 has the following specifications:
$V_z$ = 15 V, $I_{z(\min)}$ = 2 μA, $P_z$ = 120 W, $R_z$ = 40 Ω, $R_L$ = 5 kΩ and $V_i$ = 18–24 V.
Determine the minimum and maximum value of series dropping resistance *R*. [*Ans.* 158 Ω, 1 kΩ]

**53.** Design a Zener regulator for the following specifications: Output voltage, $V_o$ = 5 V, Load current, $I_L$ = 20 mA, Input voltage, $V_i$ = 12 V ± 3V, Zener wattage, $P_z$ = 500 mW.

[*Ans.* $R_L$ = 250 Ω, *R* = 83.33 Ω to 200 Ω]

**54.** How will you select the inductor, core, and transistor for SMPS?

**55.** Why special type of diodes are selected as switching diodes in the rectifier circuits of SMPS?

**56.** Explain the effect of impedance of capacitor at higher frequencies in filter circuits of SMPS.

**57.** What is a UPS? How does it operate?

**50.** Explain the operation of a switching regulator with a neat block diagram and suitable waveforms.

**51.** Describe the operation of over-voltage protection circuit of switching regulator with a neat block diagram using BJT and MOSFET.

**56.** What is the condition of the primary or secondary fuse in a dc power supply?

**57.** Give the common transformer faults and their symptoms.
**58.** When a fault in rectifier diode is diagnosed, how will you troubleshoot?
**59.** Mention the common filter faults and their symptoms.
**60.** Write about the common voltage regulator faults and their symptoms.