Analog Electronic Circuits

EC 304/EC (EE) 301/EC (EI) 302

Third Edition

WBUT–2015

About the Author

Soumitra Kumar Mandal obtained a BE (Electrical Engineering) from Bengal Engineering College, Shibpur, Calcutta University, and an MTech (Electrical Engineering) with specialization in Power Electronics from Institute of Technology, Banaras Hindu University, Varanasi. Thereafter, he obtained a PhD degree from Panjab University, Chandigarh. He started his career as a lecturer of electrical engineering at SSGM College of Engineering, Shegaon. Later he joined Punjab Engineering College, Chandigarh, as a lecturer and served there from March 1999 to January 2004. In February 2004, he joined National Institute of Technical Teachers' Training and Research, Kolkata, and is presently Professor of electrical engineering at this institute. Prof. Mandal is also a life member of ISTE and a member of IE. Throughout his academic career, he has published over twenty research papers in national and international journals and presented many papers in national and international conferences. His research interests are in the field of computer-controlled drives, microprocessor-and-microcontroller-based system design, embedded system design and neuro-fuzzy computing.

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Soumitra Kumar Mandal

Professor

National Institute of Technical Teachers' Training and Research
Kolkata

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In the memory of
My youngest son, the late ***Gajanan Mandal***
and to
My parents, ***Smt. Arati Mandal*** *and* ***Shri Prokash Mandal***
My Wife, ***Malvika****, and*
My children, ***Om*** *and* ***Puja***

Contents

Preface

Analog Electronics Circuits is written for engineering students of West Bengal University of Technology (WBUT). Since almost none of the existing textbooks have syllabus compatibility and right pedagogy, many students find it difficult to conceptualize the subject. As per the feedback I have received from both students and teachers, there is need for a single textbook covering all the topics as per WBUT university curricula. This book is an outcome of my teaching experience at SSGM College of Engineering, Shegaon, Punjab Engineering College, Chandigarh, and National Institute of Technical Teachers Training and Research, Kolkata.

This book is designed for third-semester students of Electronics and Communication Engineering, Electrical Engineering, Electrical and Electronics Engineering, Instrumentation and Control Engineering, and Applied Electronics and Instrumentation Engineering taking the course Analog Electronic Circuits at WBUT. It will help students develop good understanding of the basic concepts of analog electronic circuits and their applications. Lucid coverage of the complete WBUT syllabus of these streams in this book with WBUT exam-oriented pedagogical features will help students excel in their examinations and also build a strong foundation for higher courses.

Salient Features

- Full coverage of the latest WBUT syllabus for the following courses: ECE as EC304–Analog Electronic Circuits (ECE), EC (EE) 301–Analog Electronic Circuits (EE/EEE/ICE), and EC (EI) 302–Analog Electronic Circuits (AEIE)
- Comprehensive coverage of regulators, oscillators, operational amplifiers, power amplifiers
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  - *Illustrations: 620*
  - *Solved Examples: 210*
  - *Multiple-Choice Questions: 215*
  - *Short-Answer Questions: 140*
  - *Review Questions: 335*

Chapter Organization

This book consists of 10 chapters. **Chapter 1** covers filters and regulators, capacitor filters, π-section filter, ripple factor, series and shunt voltage regulator, percentage regulation, concept of SMPS in detail. **Chapter 2** describes transistor biasing and stability, *Q*-point, self-bias CE, compensation techniques, *h*-model of transistor, expression of voltage gain, current gain, input and output impedance, trans-resistance and trans-conductance, emitter follower circuits, and high-frequency model of transistor. **Chapter 3** covers transistor amplifier, *RC* coupled amplifier, function of all components, equivalent circuits, derivation of voltage gain, current gain, input impedance and output impedance, frequency response characteristics, lower and upper half frequencies, bandwidth, and the concept of wide band amplifiers.

Chapters 4 and 5 cover feedback amplifiers and oscillators, respectively. **Chapter 4** presents the basic concept of positive and negative feedback amplifiers, classification of amplifiers, different topologies of feedback amplifier and properties of a feedback amplifier. **Chapter 5** describes the basic concept of oscillators, Barkhausen criteria, classification of oscillators, phase-shift oscillation, Wein bridge oscillator, tuned collector oscillator, LC oscillators, Colpitts, Hartley and crystal oscillators.

Chapter 6 deals with operational amplifiers, ideal OP-AMP, differential amplifier, constant current source (current mirror, etc.), level shifter, CMRR, open- and closed-loop circuits, importance of feedback loop (positive and negative), inverting and non-inverting amplifiers, voltage follower/buffer circuits. **Chapter 7** describes applications of operational amplifiers, adder, integrator and differentiator, comparator, Schmitt trigger, instrumentation amplifiers, log and antilog amplifiers, trans-conductance multiplier, precision rectifier, voltage-to-current and current-to-voltage converter. **Chapter 8** elaborates on topics like power amplifiers, Class A, B, AB, C, conversion efficiency and tuned amplifier. **Chapter 9** covers multivibrator, monostable, bistable multivibrator, monostable and astable operation using 555 timer. **Chapter 10** describes phase locked loop (PLL) and voltage controlled oscillator (VCO).

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I have received immense cooperation and inspiration for writing this book from Dr S K Bhattachariya, Director, NITTTR, Kolkata; Professor R Shrinivasan, NITTTR, Kolkata; Dr Gurnam Singh, PEC, Chandigarh; Dr S Chatterjee, NITTTR, Chandigarh; Dr C K Chanda and Dr P Shyam, Professors of Electrical Enginerring, IIEST, Shibpur; Dr P Sarkar, Professor of Electrical Engineering; Dr S Chattopadhay, Associate Professor of Electrical Engineering; Dr S Pal, Assistant Professor of Electrical Engineering, NITTTR, Kolkata.

I am also thankful to other staff members of Electrical Engineering Department, Mr A K Das, Mr N K Sarkar, Mr S Roy Choudhury, and Mr Surojit Mallick who helped me complete the manuscript of this book.

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I would also like to thank the editorial team at McGraw Hill Education (India) for helping me in bringing out this book in a short span of time.

Constructive criticism and suggestions are always welcome, which can be sent to *mandal_soumitra@yahoo.com*

Soumitra Kumar Mandal

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ROADMAPS TO THE SYLLABUS

This text is useful for ECE subject code:

EC304—Analog Electronic Circuits

Module 1

1. **Filters and Regulators:** Capacitor filter, π-section filter, Ripple factor, Series and shunt voltage regulator, Percentage regulation, 78xx and 79xx series, Concept of SMPS.
2. **Transistor Biasing and Stability:** *Q*-point, Self Bias-CE, Compensation techniques, *h*-model of transistors, Expression for voltage gain, Current gain, Input and output impedance, Trans-resistance and trans-conductance, Emitter follower circuits, High-frequency model of transistors.

GO TO:
CHAPTER 1. Rectifiers, Filters and Voltage Regulators
CHAPTER 2. Transistor Biasing and Stability

Module 2

1. **Transistor Amplifiers:** *RC* coupled amplifier, Functions of all components, Equivalent circuit, Derivation of voltage gain, Current gain, Input impedance and output impedance, Frequency response characteristics, Lower and upper half frequencies, Bandwidth, Concept of wideband amplifier.
2. **Feedback Amplifiers and Oscillators:** Feedback concept, Negative and positive feedback, Voltage/current, Series/shunt feedback, Barkhausen criterion, Colpitts, Hartley's, Phase shift, Wein bridge, Crystal oscillators.

GO TO:
CHAPTER 3. Transistor Amplifier
CHAPTER 4. Feedback Amplifier
CHAPTER 5. Oscillators

Module 3

1. **Operational Amplifier:** Ideal OPAMP, Differential amplifier, Constant current source (current mirror etc.), Level shifter, CMRR, Open and closed loop circuits, Importance of feedback loop (positive and negative), Inverting and non-inverting amplifiers, Voltage follower/buffer circuit.
2. **Applications of Operational Amplifiers:** Adder, Integrator and differentiator, comparator, Schmitt trigger, Instrumentation amplifier, Log and anti-log amplifiers, Trans-conductance multiplier, Precision rectifier, Voltage-to-current and current-to-voltage converter, Free running oscillator.

GO TO:
CHAPTER 6. Operational Amplifier
CHAPTER 7. Applications of Operational Amplifiers

Module 4

1. **Power amplifiers:** Class A, B, AB, C, Conversion efficiency, Tuned amplifier.
2. **Multivibrator:** Monostable, Bistable, Astable multivibrators. Monostable and astable operation using 555 timer.
3. **Special Functional Circuits:** VCO and PLL.

GO TO:
CHAPTER 8. Power Amplifier
CHAPTER 9. Multivibrators
CHAPTER 10. Phase Locked Loops and VCO

This text is useful for EE, EEE, ICE subject code:

EC(EE)301—Analog Electronic Circuits

Module 1

Filters and Regulators: Capacitor filters, π-section filter, Ripple factor, Series and shunt voltage regulator, Percentage regulation, Concept of SMPS.

GO TO:
CHAPTER 1. Rectifiers, Filters and Voltage Regulators

Module 2

Transistor Biasing and Stability: *Q* point, Self-bias CE, Compensation techniques, *h*-model of transistor, Expression of voltage gain, Current gain, Input and output impedance, Trans-resistance and Trans-conductance, Emitter follower circuits, High-frequency model of transistor.

GO TO:
CHAPTER 2. Transistor Biasing and Stability

Module 3

Transistor Amplifier: *RC* coupled amplifier, Function of all components, Equivalent circuit, Derivation of voltage gain, Current gain, Input impedance and output impedance, Frequency response characteristics, Lower and upper half frequencies, Bandwidth, Concept of wideband amplifier.

GO TO:
CHAPTER 3. Transistor Amplifier

Module 4

Feedback Amplifier and Oscillators: Concept of feedback, Negative and positive feedback, Voltage/current, Series/shunt feedback, Berkhausen criterion, Colpitts, Hartley's, Phase shift, Wien bridge, Crystal oscillators.

GO TO:
CHAPTER 4. Feedback Amplifier
CHAPTER 5. Oscillators

Module 5

Operational Amplifier: Ideal-OPAMP, Differential amplifier, Constant current source (Current mirror, etc), Level shifter, CMRR, Open and closed-loop circuits, Importance of feedback loop (positive and negative), Inverting and non-inverting amplifiers, Voltage follower/Buffer circuits.

GO TO:
CHAPTER 6. Operational Amplifier

Module 6

Application of Operational Amplifiers: Adder, Integrator and differentiator, Comparator, Schmitt trigger, Instrumentation amplifier, Log and anti-log amplifier, Trans-conductance multiplier, Precision rectifier, Voltage-to-current and Current-to-voltage converter.

GO TO:
CHAPTER 7. Applications of Operational Amplifiers

Module 7

Power amplifier: Class A, B, AB, C, Conversion efficiency, Tuned amplifier.

GO TO:
CHAPTER 8. Power Amplifier

Module 8

Multivibrator : Monostable, Bistable multivibrator. Monostable and astable operation using 555 timer.

GO TO:
CHAPTER 9. Multivibrators

Module 9

Special Function Circuits: VCO and PLL

GO TO:
CHAPTER 10. Phase Locked Loops and VCO

This text is useful for AEIE subject code: EC(EI)302—Analog Electronic Circuits

Module 1

1. **Filters and Regulators:** Capacitor filter, π-section filter, Ripple factor, Series and shunt voltage regulator, Percentage regulation, 78xx and 79xx series, Concept of SMPS.
2. **Transistor Biasing and Stability:** *Q* point, Self-bias CE, Compensation techniques, *h*-model of transistor, Expression of voltage gain, Current gain, Input and output impedance, Trans-resistance and Trans-conductance, Emitter follower circuits, High-frequency model of transistor.

GO TO:
CHAPTER 1. Rectifiers, Filters and Voltage Regulators
CHAPTER 2. Transistor Biasing and Stability

Module 2

1. **Transistor Amplifiers:** *RC* coupled amplifier, Functions of all components, Equivalent circuit, Derivation of voltage gain, Current gain, Input impedance and output impedance, Frequency response characteristics, Lower and upper half frequencies, Bandwidth, Concept of wideband amplifier.
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GO TO:
CHAPTER 6. Operational Amplifier
CHAPTER 7. Applications of Operational Amplifiers
CHAPTER 9. Multivibrators

CHAPTER

1

Rectifiers, Filters and Voltage Regulators

1.1 INTRODUCTION TO FILTER

The output voltage of a rectifier is a pulsating dc voltage, which consists of dc as well as ac components. Due to the presence of ac components, ripple exists in the output voltage. To get a smooth dc output voltage, the ac components must be removed. This is only possible by using *filter*.

The basic concept of a filter is shown in Fig. 1.1. A full-wave rectified output voltage is used as an input of a filter and the output voltage of the filter is a dc voltage with very less ripple. The filter is a circuit used to remove the unwanted ac components from the rectified output voltage allowing the passage of only dc components.

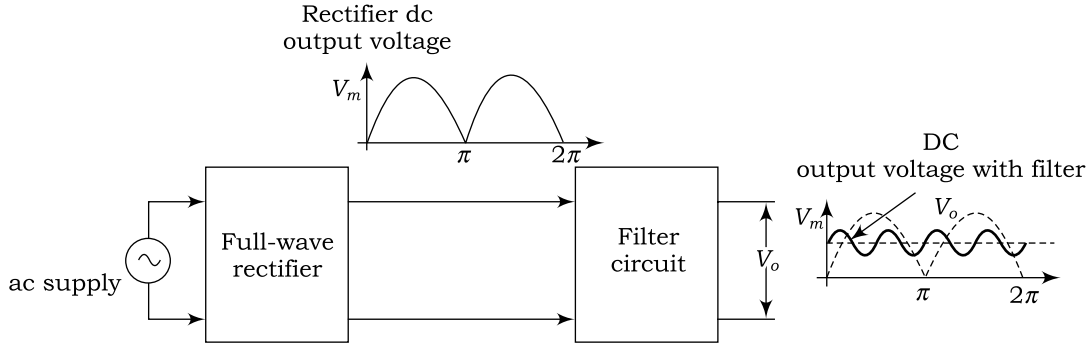


Fig. 1.1 dc output voltage of a filter

Usually, a filter circuit contains inductors, capacitors and resistances. The filter operation depends on the properties and values of passive circuit elements. The inductors allows the passage of dc signal and block the ac signal. On the other hand, the capacitors allow the ac signal to pass and block the dc signal. There

are different type of filters, which are used in electronic circuits. The most commonly used filters are given below:

1. Inductor filter
2. Capacitor filter
3. Inductor-capacitor filter
4. π-filter

1.2 INDUCTOR FILTER

Figure 1.2 shows an inductor filter which consists of an inductor (L). Actually, inductor is placed in between the rectifier and load resistance R_L. The rectifier output voltage contains dc as well as ac components. If the ac signal is passed through an inductor, it provides high impedance and consequently blocks the ac signal. When a dc signal is passed through an inductor, it provides very low impedance and allows the passage of dc signal. Accordingly, the ac component of rectifier output voltage is removed and only the dc component will be available at the output terminals. In an ideal case, the output voltage across the load is constant dc voltage. However, in reality, the output voltage has small amount of ripple as shown in Fig. 1.2.

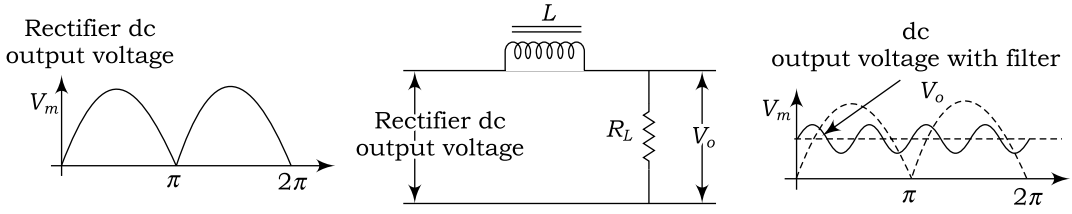


Fig. 1.2 Inductor filter circuit and its output voltage waveform

The ripple factor of an inductor filter is

$$\gamma = \frac{R_L}{3\sqrt{3}\omega L} \tag{1.1}$$

where, R_L is the load resistance in ohms,
L is the inductance in Henry, and
ω is frequency in rad/s.

It is clear from the above equation that the ripple factor increases with decreasing inductance and increasing R_L. Similarly, the ripple factor decreases with increasing inductance and decreasing R_L. The inductor filter is suitable for heavy load currents only.

1.3 CAPACITOR FILTER

Figure 1.3 shows a *capacitor filter* circuit which contain a capacitor (C). The capacitor is connected in parallel to the rectifier output voltage and load resistance R_L. When a pulsating dc voltage is applied across the capacitor, the capacitor filter removes the voltage ripples upto a certain extent. If a half-wave rectifier output voltage is fed to a capacitor filter, the resulting output voltage is better than half-wave rectifier output voltage as shown in Fig. 1.4.

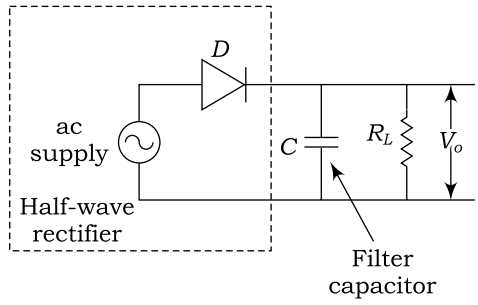


Fig. 1.3 Half-wave rectifier with capacitor filter

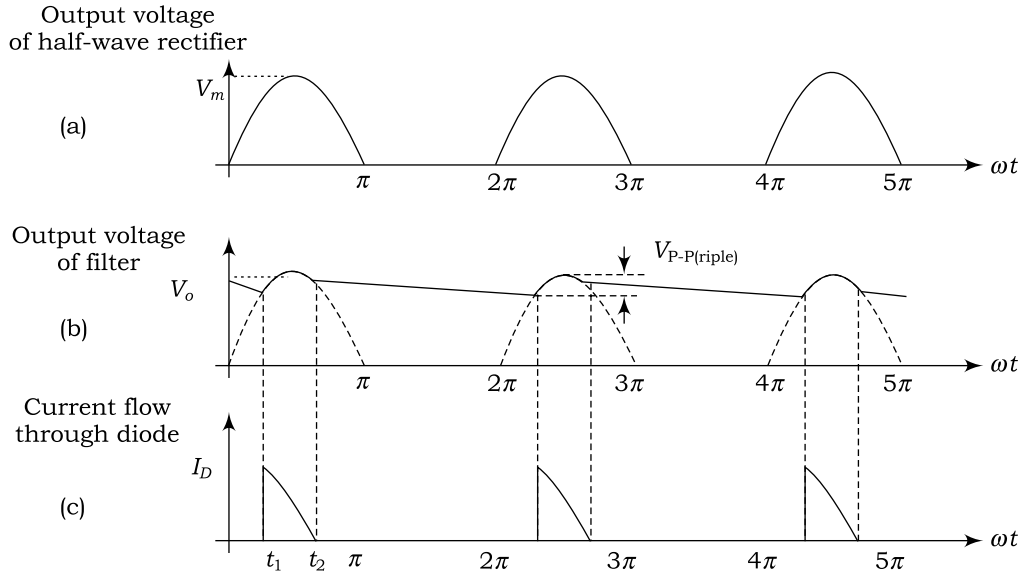


Fig. 1.4 (a) Output voltage of half-wave rectifier (b) Output voltage of filter (c) Current flow through diode

In the positive half-cycle of output voltage, the capacitor gets charged very quickly to the maximum value V_m. As there is no resistance , the charging time is almost zero and it is negligible. Hence, the capacitor follows the charging voltage. While ac voltage starts to decrease from its maximum value V_m, the capacitor returns its charge.

During the negative half-cycle of input ac voltage, output voltage of the rectifier is zero. Therefore, in the negative half-cycle, the capacitor discharges through the load resistance. The discharging time constant is R_LC. With increase in the time constant, discharge voltage of the capacitor will be less. Practically, the discharging time constant is about 100 times larger than charging time. As the capacitor has less time to discharge, it can maintain a constant voltage across the load resistance R_L as shown in Fig. 1.4.

Due to charging and discharging of capacitor, there is a small ripple in the output voltage. The ripple factor of capacitor filter can be expressed as

$$\gamma = \frac{1}{4\sqrt{3} f C R_L} \tag{1.2}$$

where, C is the capacitor in μF,
R_L is the resistance in ohms, and
f is the frequency.

1.4 *LC* FILTER

In an inductor filter, the ripple factor is directly proportional to the load resistance R_L and in the capacitor filter, the ripple factor is inversely proportional to the load resistance R_L. When both the inductor and capacitor filter are present in a filter circuit, the ripple factor is almost independent of the load resistance. This type of filter circuit is called *LC filter* as shown in Fig. 1.5. The *LC* filter is also called as choke input filter or *LC* section. The ripple factor of an *LC* filter is given by the equation

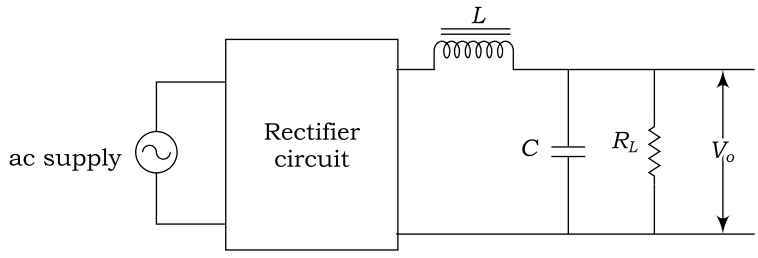


Fig. 1.5 LC filter circuit

$$\gamma = \frac{\sqrt{2}}{12\omega^2 LC} \tag{1.3}$$

where L is the inductance in henrys and capacitance C in μF.

In practice, a resistance is connected in parallel with capacitor and load resistance in a *LC* filter circuit as shown in Fig. 1.6. This resistance is called *bleeder resistance*. The advantages of the bleeder resistance are the following:

1. The bleeder resistance maintains minimum current for optimum operation of inductor.
2. This resistance provides better voltage regulation
3. It provides safety to handle the electronic equipments and also provide a discharging path for capacitors.

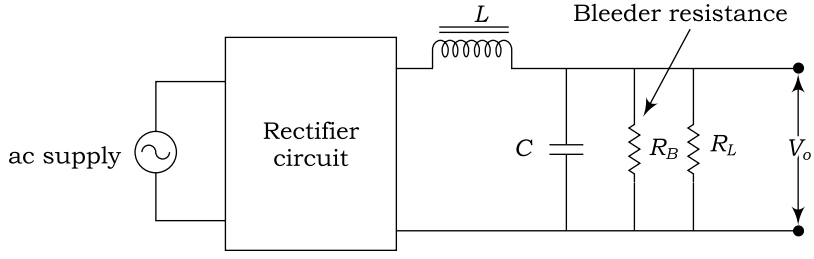


Fig. 1.6 LC filter circuit with bleeder resistance

1.5 π-FILTER

Figure 1.7 shows a π-filter circuit which consists of two capacitors C_1, C_2 and an inductor L. This filter is used when a high dc voltage at low load current is required. The pulsating output voltage of rectifier is fed to the input terminals of the π-filter circuit. The capacitor C_1 provides a low reactance to the ac components as it passes a certain amount of ac component to the ground. The capacitor C_1 provides very high resistance to the dc component. The dc components pass and flow through the inductor.

The inductor L provides a high impedance to ac components and very low impedance to the dc components. The dc component passes through but it blocks the ac component.

The capacitor C_2 operates in the similar way of the capacitor C_1 and it can pass ac components Therefore, the dc component is available at the output terminals. The ripple factor of π-filter is given by

$$\gamma = \frac{1}{4\sqrt{2}\omega^3 LC_1C_2R_L} \tag{1.4}$$

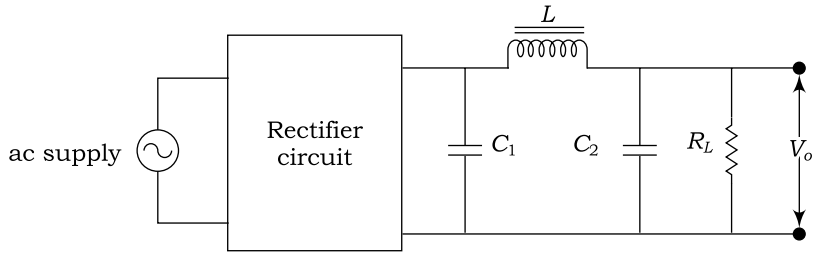


Fig. 1.7 π-filter circuit

where, C_1 and C_2 are capacitors in μF,
L is the inductance in henrys, and
R_L is load resistance in ohms.

Example 1.1 The output voltage of a full-wave rectifier circuit is fed into an inductor filter. Design the inductor filter if the ripple factor of filter output voltage is 4% for a load resistance 100 Ω and the supply frequency is 50 Hz.

Sol. Given: the ripple factor $\gamma = 4\% = 0.04$, the load resistance $R_L = 100\ \Omega$ and frequency $f = 50$ Hz

The ripple factor of an inductor filter is

$$\gamma = \frac{R_L}{3\sqrt{3}\omega L} = \frac{R_L}{3\sqrt{3} \times 2\pi f L} \quad \text{as } \omega = 2\pi f$$

or
$$0.04 = \frac{100}{3\sqrt{3} \times 2\pi \times 50 \times L}$$

The value of inductance $L = 1.53$ H

Example 1.2 The output voltage of a half-wave rectifier circuit is fed into a capacitor filter. Design the capacitor filter if the ripple factor of filter output voltage is 1% for a load resistance 1000 Ω and the supply frequency is 50 Hz.

Sol. Given: the ripple factor $\gamma = 1\% = 0.01$, the load resistance $R_L = 1000\ \Omega$ and frequency $f = 50$ Hz

The ripple factor of a capacitor filter is

$$\gamma = \frac{1}{4\sqrt{3} f C R_L}$$

or
$$0.01 = \frac{1}{4\sqrt{3} \times 50 \times C \times 1000}$$

The value of capacitance $C = 288.68\ \mu$F

Example 1.3 Design an LC filter when the output voltage of a full-wave rectifier circuit is fed to filter circuit and the ripple factor is 0.01 and the supply frequency is 50 Hz. Assume $L = 1$ H

Sol. Given: the ripple factor $\gamma = 1\% = 0.01$, $L = 1$ H and frequency $f = 50$ Hz

The ripple factor of an inductor filter is

$$\gamma = \frac{\sqrt{2}}{12\omega^2 LC} = \frac{\sqrt{2}}{12 \times (2\pi f)^2 LC} \quad \text{as } \omega = 2\pi f$$

or, $$0.01 = \frac{\sqrt{2}}{12 \times (2\pi \times 50)^2 \times 1 \times C}$$

The value of capacitance $C = 119.52\ \mu F$

Example 1.4 A 100 μF capacitor when used as a filter has 12 V dc across it with a terminal load resistor of 2.5 kΩ. If the rectifier is full wave and supply frequency is 50 Hz, what is the percentage of ripple in the output?

Sol. Given $C = 100\ \mu F$, $R_L = 2.5\ k\Omega$, $V_{dc} = 12$, $f = 50$ Hz

$$V_{rms} = \frac{V_{dc}}{4\sqrt{3} f C R_L} = \frac{12}{4\sqrt{3} \times 50 \times 100 \times 10^{-6} \times 2.5 \times 10^3} = 0.13856\ V$$

$$\text{Percentage of ripple in the output} = \frac{\text{RMS value of ripple voltage}}{\text{Average load voltage}} \times 100 = \frac{0.13856}{12} \times 100 = 1.154\%$$

1.6 ZENER DIODE

The operating principle of a zener diode has been explained in this section. When the reverse-bias voltage across a *PN*-junction diode is increased beyond the breakdown voltage (V_Z), the reverse current increases abruptly as shown in Fig. 1.8. Then the diode operates in breakdown region. A special diode, which has been designed to operate in breakdown region, is called *zener diode*. The zener diode is also known as *breakdown diode* or *voltage regulator diode*. Figure 1.9 shows the circuit symbol of zener diode.

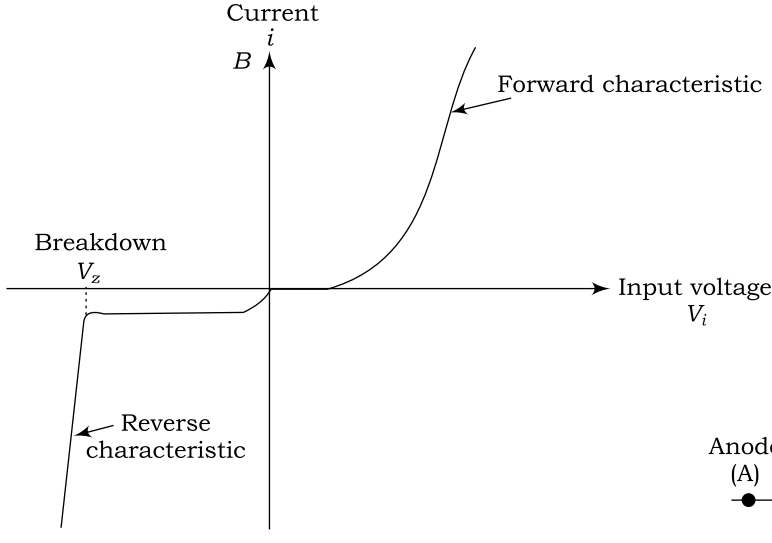


Fig. 1.8 V-I characteristics of zener diode

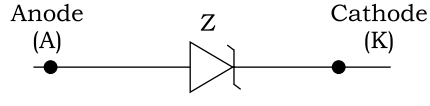


Fig. 1.9 Circuit symbol of zener diode

The zener diode is a *PN*-junction device and it always operates in the reverse breakdown region. The breakdown voltage is controlled by the doping level during manufacturing of zener diode. The reverse breakdown of a *PN*-junction occurs due to *avalanche* or *zener breakdown*. When the *PN*-junction is reverse biased, the free electrons are energised and accelerated by the reverse electric field. These electrons collide with

atoms and ionise them. Therefore, more electrons are created and they are accelerated by the reverse electric field, resulting in more atoms being ionised. Due to multiplication of number of free electrons, the reverse current increases abruptly.

When the *PN*-junction is highly reverse biased, the electric field across the junction is very high and the zener breakdown occurs. Actually, the electric field exerts a force on electrons of the outermost shell of the atom. As the force is so high, the electrons are pulled away from the outermost shell of atom and become free from nuclei. Then ionisation of atoms occurs due to this electrostatic force and the reverse current increases rapidly. This breakdown is called *zener breakdown*.

1.6.1 Characteristic of Zener Diode

The reverse portion of *V-I* characteristic of a zener diode is shown in Fig. 1.10. It is clear from Fig. 1.10 that if the reverse voltage (V_R) is gradually increased, the reverse current increases slowly. When the reverse voltage is just V_Z, the reverse current I_R ($I_{Z\min}$) flows. The operating point "*A*" is known as the *knee of the curve*. The breakdown process starts at this point. Below the knee voltage, the reverse current is negligible. When the voltage is more than V_Z, zener breakdown happens, and the current increases abruptly as shown in Fig. 1.10. During zener breakdown, the breakdown voltage (V_Z) remains constant. Hence, the zener diode has the regulating ability to maintain constant voltage with variable current. This is the most important feature of a zener diode. However, the voltage across the terminals of a zener diode is constant for a specified range of current values. Consequently, a zener diode is able to operate in a specified range of current values $I_{Z(\min)}$ to $I_{Z(\max)}$ as depicted in Fig. 1.10.

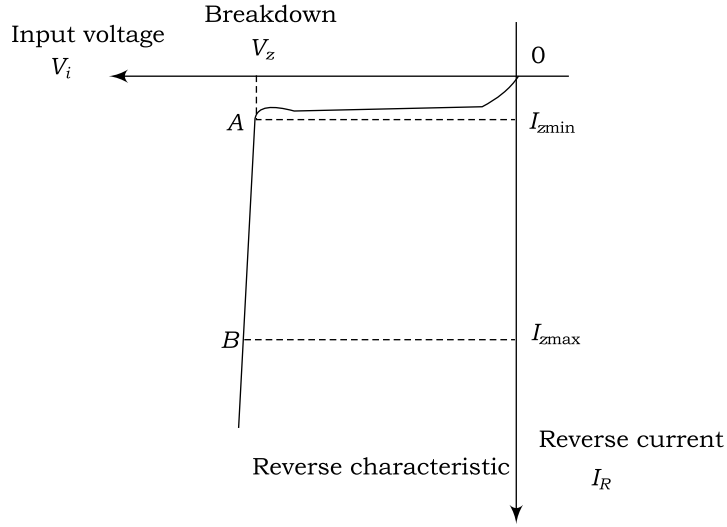


Fig. 1.10 The reverse portion of V-I characteristic of a zener diode

The minimum value of zener current $I_{Z(\min)}$ is called the *break-over current*. This current must be maintained to operate the diode in breakdown region. If the current is just below $I_{Z(\min)}$ and the device operates below the knee point (*A*), the voltage is reduced significantly and the regulation effect will be lost.

The zener diode is able to operate in breakdown region with a maximum current $I_{Z(\max)}$. If the current flow through zener diode is more than $I_{Z(\max)}$, the diode may get entirely damaged due to very high power dissipation. Thus, the zener diode must operate within a certain range of current.

1.6.2 Specification of Zener Diodes

The specification of zener diodes has the following terms:

1. Zener Voltage (V_Z)

The range of zener breakdown voltage (V_Z) is 1.8 V to 2000 V depending on the type of zener diode.

2. Break-over Current (I_{Zmax})

The value of maximum current is computed from the equation

$$I_{Z\max} = \frac{P_{Z\max}}{V_Z}$$

where, $P_{Z\max}$ = Maximum power dissipation,
V_Z = Zener voltage
$I_{Z\max}$ = Zener current

3. Maximum Power Dissipation ($P_{Z\,max}$)

The power dissipation of a zener diode is given by

$$P_{Z\max} = V_Z \times I_{Z\max}$$

where, $P_{Z\max}$ = Maximum power dissipation
V_Z = Zener voltage
$I_{Z\max}$ = Zener current

Usually the power rating of a zener diode varies from 150 mW to 50 W.

4. Zener Resistance

The range of zener resistance varies within few ohms.

The most commonly used zener diodes are 1N4370 to 1N4372, 1N957A to 1N986A and 1N1746 to 1N1759. For example, the specification of 1N4370 is given below:

- Normal zener voltage, V_Z = 2.4 V
- The zener current, I_Z = 20 mA
- The maximum zener impedance is 30 ohms
- The maximum power rating is 50 mW

1.6.3 Applications of Zener Diode

Applications of Zener diode are as follows:

1. Voltage regulator
2. Provide fixed reference voltage in a transistor biasing circuit
3. Used as clipper or limiter in wave shaping circuits
4. Over voltage protection of electronics instrument

1.6.4 Ideal and Real Zener Diodes

Figure 1.11(a) shows the symbol of an *ideal zener diode* and its equivalent circuit. An ideal zener diode is equivalent to a battery with the zener voltage (V_Z). However, the *real zener diode* is equivalent to a battery with the zener voltage (V_Z) in series with a resistance R_Z as depicted in Fig. 1.11(b). The R_Z is called *zener resistance* and it is also known as *dynamic resistance of zener diode*.

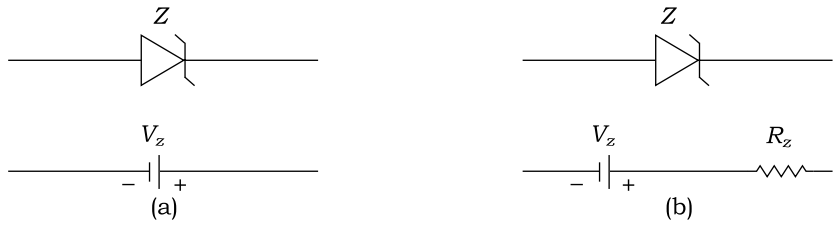


Fig. 1.11 (a) Ideal zener diode (b) Real zener diode

Figure 1.10 shows the *V-I* characteristics of an ideal zener diode where the curve *AB* is vertical. Due to the presence of zener resistance R_Z, the *V-I* curve is slightly tilted as depicted in Fig. 1.12. The value of dynamic resistance is computed from the *V-I* characteristics of zener diode and it is given by

$$R_Z = \frac{\Delta V_Z}{\Delta I_Z} \tag{1.5}$$

where, ΔV_Z is the change in zener voltage, and
ΔI_Z is the change in zener current.

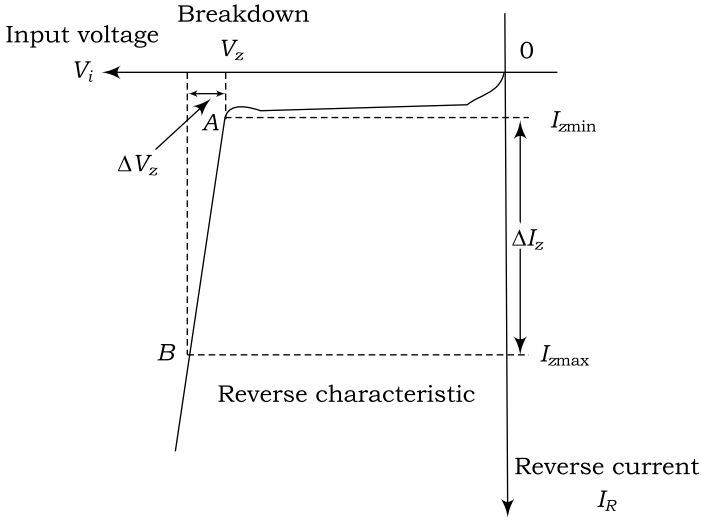


Fig. 1.12 Determination of R_Z from V-I characteristic of zener diode

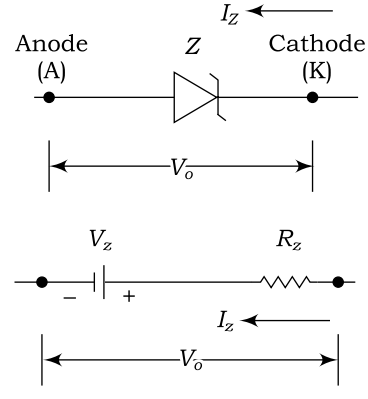


Fig. 1.13 Voltage across the zener diode

When a current I_Z flows through the zener diode as shown in Fig. 1.13, the output voltage of a practical zener diode is given by

$$V_O = V_Z + I_Z R_Z \tag{1.6}$$

If R_Z is very small, the output voltage across the zener diode is $V_O = V_Z$.

Example 1.5 If the reverse saturation current in a zener diode changes from 25 mA to 50 mA corresponding to the change in reverse voltage from 4.7 V to 4.75 V, determine the dynamic resistance of zener diode.

Sol. The dynamic resistance of a zener diode is

$$R_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

where, ΔV_Z is the change in zener voltage, and
ΔI_Z is the change in zener current.

$\Delta V_Z = 4.75 - 4.7 = 0.05$ V and $\Delta I_Z = 50 - 25 = 25$ mA

Therefore, $R_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{0.05}{25 \times 10^{-3}} = 2\ \Omega$

1.7 VOLTAGE REGULATOR

A voltage regulator maintains a constant dc output voltage irrespective of the changes in either ac input voltage or the load current. For example, the output voltage should be maintained within ±1% of the specified voltage. An ideal regulated power supply is an electronic circuit, which is able to provide a constant output voltage during the following conditions:

1. Change in input voltage
2. Change in load current due to variation of load
3. Change in temperature

Figure 1.14(a) shows the block-diagram representation of voltage regulation due to change in input voltage. The change in input voltage of a voltage regulator is ΔV_i, which will be either positive or negative. As the input voltage has a ripple voltage, there will be certain change in output voltage. In case of an ideal voltage regulator, the change in output voltage must be zero ($\Delta V_O = 0$) even if there is a change in input voltage. Figure 1.14(b) shows that the load is varied and load current changes due to variation in load resistance. Consequently, the output voltage V_O will be changed. However, the voltage regulator should maintain the output voltage. Regulation of a voltage regulator can be specified by two ways such as

1. Line regulation
2. Load regulation

In this section, line regulation and load regulation are explained in detail.

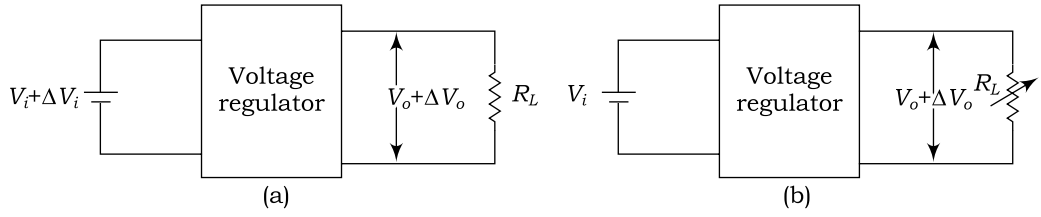


Fig. 1.14 (a) Voltage regulation due to change in input voltage (b) Voltage regulation due to change in load

1.7.1 Line Regulation

Due to change in input voltage, there will be a change in output voltage. The line regulation represents the change in output voltage per unit change in input voltage. The line regulation can be expressed as

$$\text{Line regulation} = \frac{\Delta V_O}{\Delta V_i} \tag{1.7}$$

where, ΔV_O is the change in output voltage, and
ΔV_i is the change in input voltage.

The unit of line regulation is μV/V.

1.7.2 Load Regulation

Generally, there will be a slight change in output voltage when load current changes. The load regulation means that the change in output voltage per unit change in load current. The load regulation can be expressed as

$$\text{Load regulation} = \frac{V_{\text{No Load}} - V_{\text{Full Load}}}{\Delta I_L} = \frac{V_{\text{NL}} - V_{\text{FL}}}{\Delta I_L} \tag{1.8}$$

where, V_{NL} is no load output voltage,
V_{FL} is full load output voltage, and
ΔI_L is the change in load current.

The unit of load regulation is μV/mA.

Sometimes voltage regulation is represented by percentage (%) regulation. The regulation should maintain a constant output voltage though there is a change in voltage and in the load current and it is given by

$$\%\ \text{regulation} = \frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \tag{1.9}$$

1.8 CLASSIFICATION OF VOLTAGE REGULATORS

There are different types of voltage regulators depending upon the applications of different devices. The most commonly used voltage regulators are given below:

1. Zener diode shunt regulator
2. Transistor shunt regulator
3. Transistor series regulator
4. Transistor current regulator
5. Transistor controlled series regulator
6. Operational amplifier (OPAMP) shunt regulator
7. Operational amplifier (OPAMP) series regulator
8. Switching voltage integrated circuit regulator
9. Monolithic regulator

In this section, zener diode shunt regulator, transistor shunt regulator and transistor series regulator are explained in detail.

1.9 ZENER DIODE SHUNT REGULATOR

Figure 1.15 shows a zener diode shunt regulator circuit. In this circuit, zener is connected in parallel with the load. Therefore, this circuit is called *shunt regulator*. A resistance R_S is connected in series with the voltage source (V) and zener diode to limit the current flow in the circuit. Hence, R_S is known as *series current limiting resistance*. R_L is the load resistance. The output voltage across R_L is V_O. The input voltage V is always greater than the zener voltage (V_Z) and the zener operates in the reverse breakdown region.

The current flow through the resistance R_S is given by

$$I_S = \frac{V - V_Z}{R_S} \tag{1.10}$$

where, V is the input voltage, and

V_Z is the zener voltage.

Usually, an ideal zener diode behaves as a constant source of voltage (V_z). But a real zener diode has a finite value of resistance called zener resistance (R_Z). Due to presence of zener resistance (R_Z), there is a voltage drop across it and it is expressed as $I_Z R_Z$

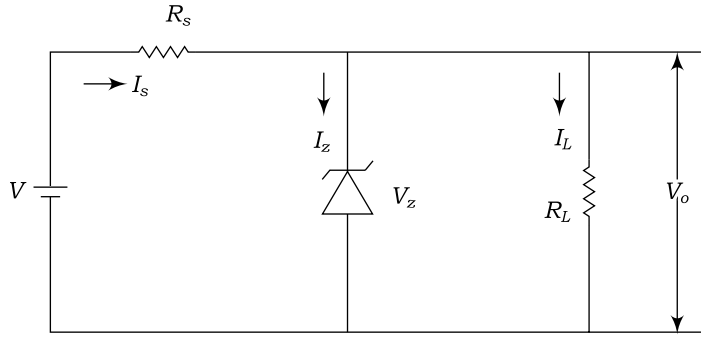


Fig. 1.15 Zener diode shunt regulator

The voltage drop across zener diode is

$$V_O = V_Z + I_Z R_Z$$

When R_Z is negligible, the output voltage $V_O = V_Z$

The current flow through load resistance is

$$I_L = \frac{V_O}{R_L}$$

Applying the KCL at the point A, we get

$$I_S = I_Z + I_L \tag{1.11}$$

where, I_S is the current through R_S,

I_Z is the zener current, and

I_L is the load current.

1.9.1 Working Principle of Zener Shunt Regulation

The zener shunt regulation can be operated properly in the following conditions:

1. Voltage regulation due to change in input voltage.
2. Voltage regulation due to change in load current.

Figure 1.16 shows a regulator circuit where the load resistance R_L is constant and the input voltage V changes within specified limit. When the input voltage increases, the input current increases. Therefore, current flow through the zener diode increases but the current flow through the load is constant. Due to increase in input current (I_S), the voltage drop across R_S increases maintaining the output voltage (V_O) as constant.

If the input voltage decreases, the input current also decreases. Consequently, the current flow through zener diode also decreases. Hence, the voltage drop across resistance R_S decreases and the output voltage remains constant.

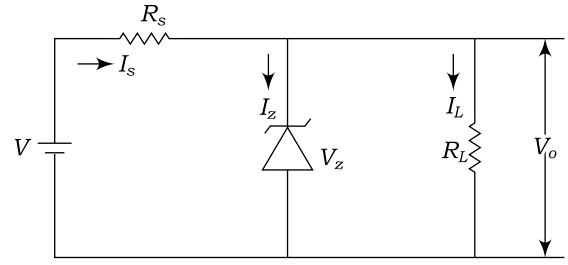


Fig. 1.16 The voltage regulation with change in input voltage

Figure 1.17 shows a voltage regulator circuit where the input voltage V is constant and the load resistance R_L varies within a limit. Due to variation in load resistance (R_L), the load current (I_L) changes. Therefore, the output voltage (V_O) across R_L can be changed. If the R_L decreases, the load current increases and the zener current decreases. Therefore, the input current (I_S) and voltage drop across R_S remain constant. Hence, the output voltage (V_O) is also constant. When the load resistance increases, the load current decreases and the zener current increases. Again, the input current and voltage drop across resistance R_S remain constant. As a result, the output voltage is constant.

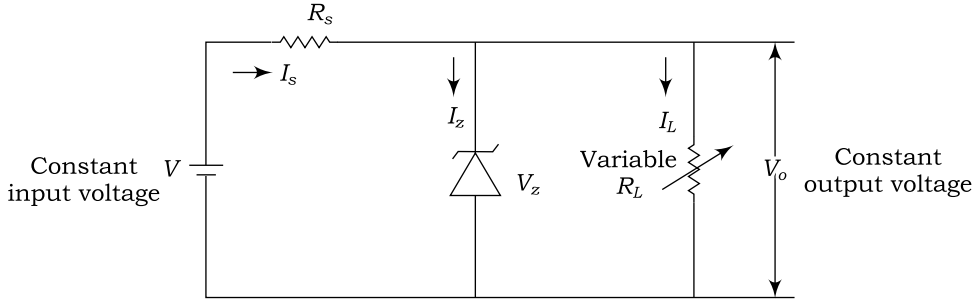


Fig. 1.17 The voltage regulation with change in load

1.9.2 Current Limiting Resistance

In a zener shunt regulator, the value of series resistance (current limiting resistance) must be selected for the following purposes.

1. If the input voltage is minimum and load current is maximum, adequate current must flow to the zener diode.
2. When the input voltage is maximum and load current is minimum, the current flow through zener diode must not be increased above the maximum rated value.

Then the maximum and minimum zener current can be expressed as

$$I_{Z(\max)} = \frac{V_{(\max)} - V_Z}{R_S} - I_{L(\min)} \quad \text{and} \tag{1.12}$$

$$I_{Z(\min)} = \frac{V_{(\min)} - V_Z}{R_S} - I_{L(\max)} \tag{1.13}$$

Based on the above equations, the maximum and minimum current limit resistance are given by

$$R_{S(\min)} = \frac{V_{(\max)} - V_Z}{I_{Z(\max)} + I_{L(\min)}} \quad \text{and} \tag{1.14}$$

$$R_{S(\max)} = \frac{V_{(\min)} - V_Z}{I_{Z(\min)} + I_{L(\max)}} \tag{1.15}$$

The value of R_S must be in between $R_{S(\max)}$ and $R_{S(\min)}$ for proper operation of zener shunt regulator and it is represented by

$$R_{S(\min)} < R_S < R_{S(\max)} \tag{1.16}$$

1.9.3 Disadvantage of Zener Shunt Regulation

The zener shunt regulator has the following disadvantages:

1. The load current must be within limit value $I_{Z(\max)}$ and $I_{Z(\min)}$. The $I_{Z(\max)}$ and $I_{Z(\min)}$ are in the order of few mA.
2. A large amount of power is dissipated in the series resistance R_S and zener diode in comparison with the output power.
3. Output resistance is not very low.
4. Regulation factor is high.

1.10 TRANSISTOR SHUNT REGULATOR

The circuit diagram of a transistor shunt regulator is shown in Fig. 1.18. As the transistor T_1 is connected in parallel (shunt) with load, this circuit is called *shunt regulator*. The output voltage (V_O) is the sum of zener voltage (V_Z) and the base emitter voltage (V_{BE}) of transistor T_1.

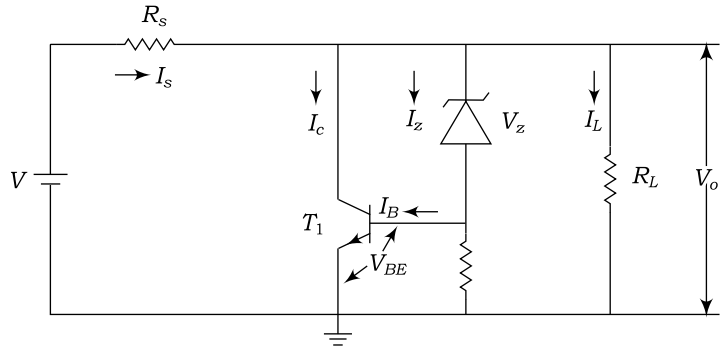


Fig. 1.18 The transistor shunt regulator

Therefore, we can write

$$V_O = V_Z + V_{BE}$$

or

$$V_{BE} = V_O - V_Z$$

As the voltage across zener diode is constant, any increase or decrease in output voltage, will have an effect on the base-emitter voltage. When there is increase in input voltage, the output voltage increases.

Therefore, the base-emitter voltage and hence, the base current and also the collector current of transistor increases. As a result, the input current (I_S) and the voltage across R_S increases. Consequently, the load voltage decreases.

The input voltage (V) is equal to the sum of the voltage drop across R_S and the output voltage and it can be expressed as

$$V = I_S R_S + V_O$$

or,
$$V_O = V - I_S R_S \tag{1.17}$$

1.11 TRANSISTOR SERIES REGULATOR

The transistor series regulator circuit is shown in Fig. 1.19. As the transistor is connected in series with the load, the circuit is called a *series regulator*. In this circuit, the transistor T_1 behaves as a variable resistance and the value of resistance depends on base current. The output voltage is equal to the difference between the zener voltage(Vz) and base emitter voltage (V_{BE}) and it can be expressed as

$$V_O = V_Z - V_{BE}$$

or
$$V_{BE} = V_Z - V_O$$

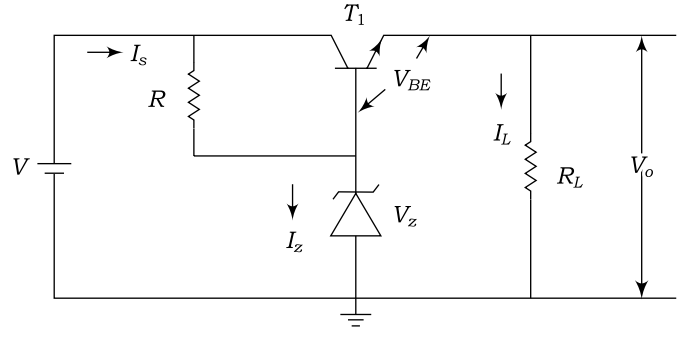


Fig. 1.19 The transistor series regulator

When load voltage increases, the base-to-emitter voltage (V_{BE}) decreases, and the voltage across zener diode remains constant. Then the forward bias and the level of conduction of the transistor decrease. As a result, the collector-to-emitter voltage of the transistor increases. Then the input current decreases to compensate the increase in the value of load current.

Example 1.6 A 5 V dc regulated power supply has a regulation 1%. Determine the magnitude of change in output voltage.

Sol. The change in output voltage is = $0.01 \times 5 = 0.05$ V

The variation in output voltage is ±0.05 V

Example 1.7 A dc regulated power supply has a line regulation of 2.5 μV/V. Determine the change in output voltage when change in input voltage is 2 V.

Sol. The line regulation = $\dfrac{\Delta V_O}{\Delta V_i}$

where, ΔV_O is the change in output voltage, and
ΔV_i is the change in input voltage.

Line regulation = 2.5 μV/V and ΔV_i = 2 V

The change in output voltage = 2.5 μV/V × 2 V = 5 μV

Example 1.8 A dc voltage regulator power has a load regulation of 5 μV/mA. At no load, the output voltage is 10 V. Calculate the output voltage at full load when the full load current is 100 mA.

Sol. The load regulation = $\dfrac{V_{NL} - V_{FL}}{\Delta I_L}$

where, V_{NL} is no load output voltage, V_{FL} is full load output voltage and ΔI_L is the change in load current.

Load regulation = 5 μV/mA, V_{NL} = 10 V, ΔI_L = 100 mA.

Therefore, 5 μV/mA = $\dfrac{10 - V_{FL}}{100}$

The output voltage at full load = 9.9995 V

Example 1.9 A zener diode shunt regulated power supply is depicted in Fig. 1.20. Determine (a) the output voltage, (b) source current, and (c) current through the zener diode. Assume that the zener resistance is equal to zero.

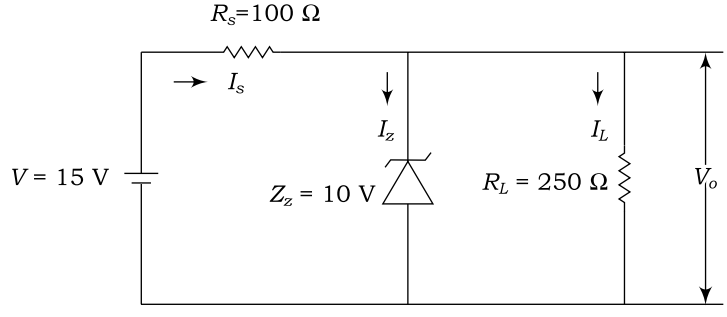


Fig. 1.20

Sol. The input voltage V = 15 V, Zener voltage V_Z = 10 V, R_S = 100 Ω and R_L = 250 Ω

(a) The output voltage is

$$V_O = V_Z + I_Z R_Z = V_Z = 10 \text{ V} \quad \text{as } R_Z = 0$$

(b) The current flows through the resistance R_S is

$$I_S = \frac{V - V_Z}{R_S} = \frac{15 - 10}{100} \text{ A} = 0.05 \text{ A}$$

(c) The current flow through load resistance is

$$I_L = \frac{V_O}{R_L} = \frac{10}{250} \text{ A} = 0.04 \text{ A}$$

As $I_S = I_Z + I_L$, the zener current is

$$I_Z = I_S - I_L = 0.05 \text{ A} - 0.04 \text{ A} = 0.01 \text{ A}$$

Example 1.10 Design a zener diode shunt regulated power supply (Fig. 1.21) with the following specifications:

(a) the output voltage is 5 V, (b) load current is 50 mA, (c) maximum zener power dissipation 500 mW, and (d) input voltage 10 ± 2V.

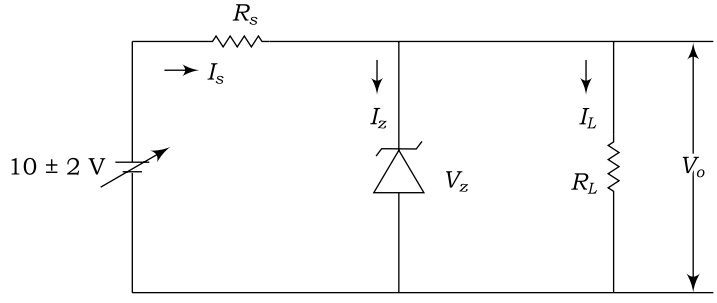


Fig. 1.21

Sol. Given: $V_O = 5$ V, $I_L = 50$ mA, $P_{Z(\max)} = 500$ mW and $V = 10 \pm 2$ V

The Zener voltage is $V_Z = V_O = 5$ V

The maximum zener current $I_{Z(\max)} = \dfrac{P_{Z(\max)}}{V_Z} = \dfrac{500 \times 10^{-3}}{5} = 100$ mA

The minimum value of current limit resistance is

$$R_{S(\min)} = \frac{V_{(\max)} - V_Z}{I_{Z(\max)} + I_{L(\min)}} = \frac{12-5}{100+50} \times 10^3 = 46.66\ \Omega$$

The minimum value of zener current is

$$I_{Z(\min)} = \frac{V_{(\min)} - V_Z}{R_S} - I_{L(\max)} = \frac{8-5}{46.66} - 50 \times 10^{-3} = 14.29\ \text{mA}$$

Example 1.11 In a zener diode shunt regulated power supply, $V_O = 10$ V, $I_L = 50$ mA, $P_{Z(\max)} = 1000$ mW and V varies from 20 V to 30 V. Determine the maximum and minimum value of zener current.

Sol. Given: $V_O = 10$ V, $I_L = 50$ mA, $P_{Z(\max)} = 1000$ mW and $V = 20$ V to 30 V

The Zener voltage is $V_Z = V_O = 10$ V

The maximum zener current $I_{Z(\max)} = \dfrac{P_{Z(\max)}}{V_Z} = \dfrac{1000 \times 10^{-3}}{10} = 100$ mA

The minimum value of current limit resistance is

$$R_{S(\min)} = \frac{V_{(\max)} - V_Z}{I_{Z(\max)} + I_{L(\min)}} = \frac{30-10}{100+50} \times 10^3 = 133.33\ \Omega$$

The minimum value of zener current is

$$I_{Z(\min)} = \frac{V_{(\min)} - V_Z}{R_S} - I_{L(\max)} = \frac{20-10}{133.33} - 50 \times 10^{-3} = 25\ \text{mA}$$

Example 1.12 A transistor shunt regulated power supply is shown in Fig. 1.22. Determine (a) the output voltage, (b) load current, and (c) source current. Assume zener resistance is equal to zero, $V_{BE} = 0.7$ V and $R_B = \infty$.

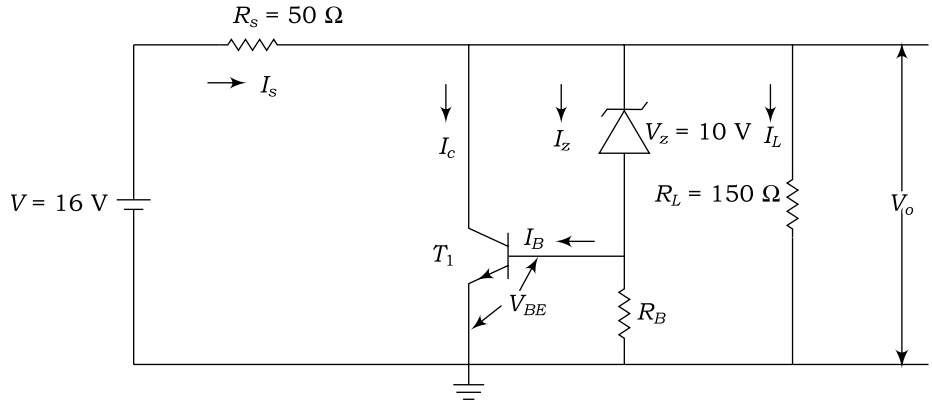


Fig. 1.22

Sol. The output voltage is

$$V_O = V_Z + V_{BE} = (10 + 0.7)\text{ V} = 10.7\text{ V}$$

The load current is equal to

$$I_L = \frac{V_O}{R_L} = \frac{10.7}{150}\text{ A} = 71.33\text{ mA}$$

The current through R_S is

$$I_S = \frac{V - V_O}{R_S} = \frac{16 - 10.7}{50}\text{A} = 106\text{ mA}$$

Example 1.13 A transistor series regulated power supply is shown in Fig. 1.24. Determine (a) the output voltage, (b) load current, and (c) zener current. Assume zener resistance is equal to zero, and $V_{BE} = 0.7$ V.

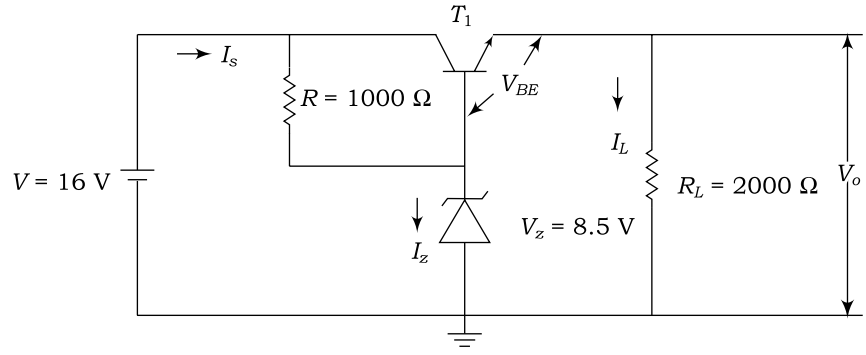


Fig. 1.23

Sol. The output voltage is equal to

$$V_O = V_Z - V_{BE} = (8.5 - 0.7)\text{ V} = 7.8\text{ V}$$

The collector-to-emitter voltage is

$$V_{CE} = V - V_O = (16 - 7.8)\text{ V} = 8.2\text{ V}$$

The current flows through resistance R is

$$I_R = \frac{V - V_Z}{R} = \frac{16 - 8.5}{1000}\text{ A} = 7.5\text{ mA}$$

The load current is

$$I_L = \frac{V_O}{R_L} = \frac{7.8}{2000}\text{ A} = 3.9\text{ mA}$$

The base current is

$$I_B = \frac{I_L}{\beta} = \frac{3.9}{100} = 0.039\text{ mA} \qquad \text{Assume } \beta = 100$$

The zener current is

$$I_Z = I_R - I_B = (7.5 - 0.039)\text{ mA} = 7.461\text{ mA}$$

Example 1.14 Determine minimum and maximum load currents for which the zener diode in Fig. 1.24 will maintain regulation. What is the minimum R_L that can be used?

Given: V_z = 12 V, I_{zk} = 1 mA, I_{zm} = 50 mA. Assume Z_z = 0 Ω over the range of current values.

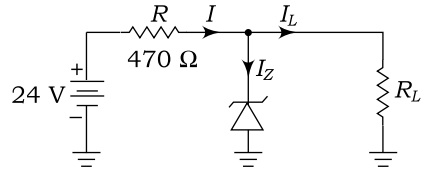


Fig. 1.24

Sol. Current $I = \dfrac{V_{in} - V_z}{R} = \dfrac{24 - 12}{470}\text{ A} = 25.5319\text{ mA}$

Applying KCL, we can write $I = I_L + I_Z$.

Since I is constant, $I = I_{zk} + I_{L(\max)}$ or $25.5319\text{ mA} = 1\text{ mA} + I_{L(\max)}$

Therefore, $I_{L(\max)} = 24.5319\text{ mA}$

Resistance $R_L = \dfrac{V_o}{I_{L(\max)}} = \dfrac{12}{24.53 \times 10^{-3}} = 489.196\ \Omega$

Current $I_{L(\min)} = I - I_z = 0$ as I_L will be minimum when $I_z = I$

Example 1.15 For zener voltage regulator, if $I_{Z\min}$ = 2 mA, $I_{Z\max}$ = 20 mA, V_z = 4.7 V. Determine the range of input voltage over which output voltage remains constant. R_S = 1 kΩ, R_L = 1 kΩ, Z_Z = 0 Ω.

Sol. Given: $I_{Z\min}$ = 2 mA, $I_{Z\max}$ = 20 mA, V_z = 4.7 V, R_S = 1 kΩ, R_L = 1 kΩ, Z_Z = 0 Ω

Load current $I_L = \dfrac{V_Z}{R_L} = \dfrac{4.7}{1 \times 10^3} = 4.7\text{ mA}$

When the minimum input voltage $V_{in(\min)}$ is applied, the output voltage is constant and the zener current is $I_z = I_{z(\min)}$

Current $I = I_L + I_{z(\min)} = (4.7 + 2)\text{ mA} = 6.7\text{ mA}$

Voltage $V_{in(\min)} = V_Z + IR_S = 4.7 + 6.7 \times 10^{-3} \times 1 \times 10^3 = 11.4$ V

When the maximum input voltage $V_{in(\max)}$ is applied, the output voltage is constant and the zener current is $I_z = I_{z(\max)}$

Current $I = I_L + I_{z(\max)} = (4.7 + 20)$ mA $= 24.7$ mA

Voltage $V_{in(\max)} = V_Z + IR_S = 4.7 + 24.7 \times 10^{-3} \times 1 \times 10^3 = 29.4$ V

To obtain constant output voltage, the range of input voltage is 11.4 to 29.4 V

Example 1.16 When the reverse current in a particular zener diode increases from 20 mA to 30 mA, the zener voltage changes from 5.6 V to 5.65 V. What is the impedance of this device?

Sol. Given: $I_{z1} = 20$ mA, $V_{z1} = 5.6$ V, $I_{z2} = 30$ mA, $V_{z2} = 5.65$ V

The zener impedance $R_z = \dfrac{\Delta V_z}{\Delta I_z} = \dfrac{5.65 - 5.6}{30 \times 10^{-3} - 20 \times 10^{-3}} = \dfrac{0.05}{10 \times 10^{-3}} = 5\ \Omega$

Example 1.17 Design a zener regulator (Fig. 1.25) for the following specifications: load current $I_L = 20$ mA, output voltage $V_o = 5$ V, zener wattage $P_z = 500$ mW, input voltage $V_i = 12 \pm 2$ V and $I_{z(\min)} = 8$ mA.

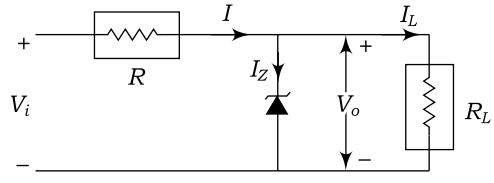


Fig. 1.25

Sol. Given: $I_L = 20$ mA, $V_o = 5$ V, $P_z = 500$ mW, $I_{z(\min)} = 8$ mA, $V_i = 12 \pm 2$ V

Load resistance $R_L = \dfrac{V_o}{I_L} = \dfrac{5}{20 \times 10^{-3}}\ \Omega = 250\ \Omega$

The zener diode voltage V_z will be equal to V_o. Then $V_z = V_o = 5$ V

$$I_{z(\max)} = \frac{P_z}{V_z} = \frac{500 \times 10^{-3}}{5} = 100 \times 10^{-3}\ \text{A} = 100\ \text{mA}$$

$$R_{s(\min)} = \frac{V_{i(\max)} - V_z}{I_L + I_{z(\max)}} = \frac{14 - 5}{20 \times 10^{-3} + 100 \times 10^{-3}} = 75\ \Omega$$

$$R_{s(\max)} = \frac{V_{i(\min)} - V_z}{I_L + I_{z(\min)}} = \frac{10 - 5}{20 \times 10^{-3} + 8 \times 10^{-3}} = 178.57\ \Omega$$

Therefore, $75 \le R_s \le 178.57$. We can select, $R_s = 150\ \Omega$

Example 1.18 Figure 1.26 shows an electronic voltage regulator. The zener diode may be assumed to require a minimum current of 25 mA for satisfactory operation. Find the value of R required for satisfactory voltage regulation of the circuit. Assume $V_Z = 10$ V.

Sol. Given: $I_z = 25$ mA and $V_z = 10$ V

The current flow through load is $I_L = \dfrac{V_Z}{R_L} = \dfrac{10}{100} = 100$ mA

Here, $I = I_Z + I_L$

or $I = 25\ \text{mA} + 100\ \text{mA} = 125\ \text{mA}$

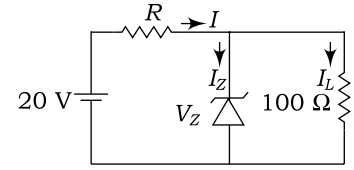


Fig. 1.26

We can write the KVL equation, $20 = IR + V_Z$

or, $$R = \frac{20 - V_Z}{I} = \frac{20 - 10}{125 \times 10^{-3}} \text{A} = 80\ \Omega$$

Example 1.19 For the circuit of Fig. 1.27, find the voltage drop across the 5 kΩ resistance.

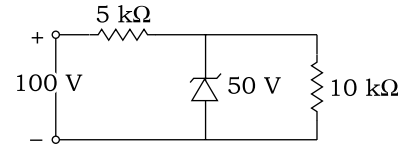


Fig. 27

Sol. Current through 5 kΩ resistance is $I_S = \frac{100 - 50}{5 \times 10^3} = 10 \text{ mA}$

The voltage drop across the 5 kΩ resistance is $I_S R = 10 \times 10^{-3} \times 5 \times 10^3 = 50 \text{ V}$

1.12 SWITCHING MODE POWER SUPPLY (SMPS)

A regulated linear power supply provides a constant voltage by varying their resistance to cope with input voltage changes or load current demand changes. The regulated linear power supply is an inefficient design. In order to improve the efficient, designers tried to rectify the circuit design. Therefore Switching Mode Power Supply (SMPS) is developed to improve efficiency.

Switching Mode Power Supplys (SMPSs) are smaller in size and more efficient than linear regulator power supplies. Usually, in SMPS the input is A.C. mains but the output is to be D.C. The isolation between input and output is required. Figure 1.28 shows the block diagram of a typical SMPS.

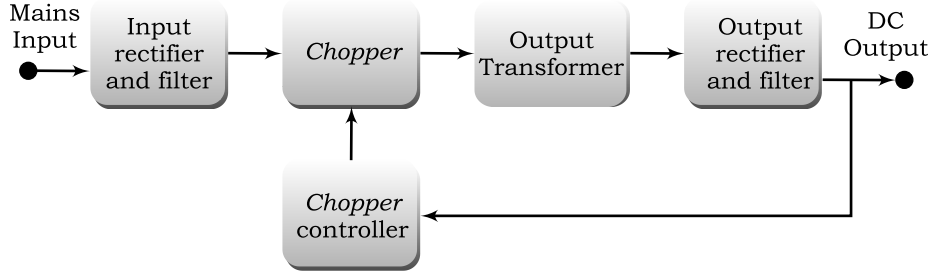


Fig. 1.28 Block diagram of a mains operated SMPS with output voltage regulation

The ac mains are first rectified and the rectifier output is smoothed by using filter. After that the smoothed D.C. is switched at a high frequency, i.e., typically about 50 KHz. SMPS uses a high-frequency MOSFET as a switching transistor with varying duty cycle of chopper to maintain the output voltage. The switched current flows in the primary of a ferrite cored transformer. The corresponding secondary current of ferrite cored transformer is rectified and smoothed. The control of output voltage is obtained by adjustment of the chopper duty cycle.

A switching-mode power supply (SMPS) is also represented by switched-mode power supply. Actually SMPS is an electronic power supply which incorporates a switching regulator to convert electrical power efficiently. Just like other linear power supplies, an SMPS transfers power from a source (ac mains) to a load, such as a personal computer.

SMPSs can also be used as linear supplies to step-down a supply voltage. Unlike a linear regulator, an SMPS can also provide a step-up function and an inverted output function.

1.12.1 Types of SMPS

Most commonly used types of SMPS are

- Buck or forward converter
- Boost or flyback converter
- Bbuck-boost converter
- Cuk converter
- Push-pull converter
- Resonant converter
- Half-bridge and full-bridge converters

The choice of the type of SMPS to use is made on the simplicity of the drive and control circuitry and the power output requirements. A switching mode power supply desires a load to operate. Without load, the SMPS will not be able to regulate properly . When testing an SMPS on the bench, either use any value high wattage resistor from +5V to ground which will draw an amp of current or *trash* computer hard drive as a load. In this section the operation of buck converter is explained briefly.

1.12.2 Buck converter (Forward converter)

Figure 1.29 shows the simplified circuit diagram of a Buck converter. The buck converter or forward converter is used to transfer energy to the output capacitor (C_1) and load when the switching transistor is switched on. In Fig. 1.29, a buck converter is connected at the secondary side of transformer, but a demagnetisation circuit is to be connected at primary side.

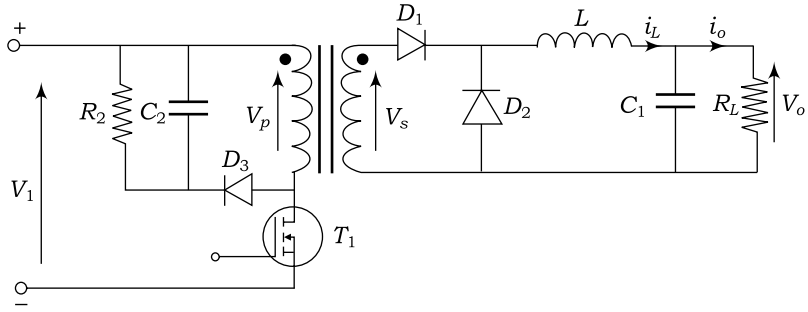


Fig. 1.29 Buck converter

When transistor T_1 is on, diode D_1 is forward-biased. Due to secondary induced voltage, and the current flow through inductor L increases (ramp-up). When transistor T_1 is off, voltage V_L is reversed, diode D_2 becomes forward-biased and current flows start from L, C_1 or R_L, D_2 and then back to L. Consequently, the charge on the C_1 is replenishing and the current flow through inductor L decreases (ramp-down). At the same time, the reversed primary voltage is to keep the current flowing, diode D_3 is forward-biased and capacitor C_2 is charged up allowing the demagnetization of the transformer core. As soon as the current becomes zero, diode D_3 will be reverse-biased and turns off. Then capacitor C_2 will be discharge through R_2. Figure 1.30 shows the waveforms of V_L and i_L during continuous conduction mode operation of buck converter.

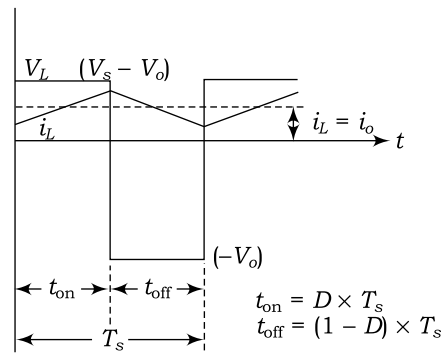


Fig. 1.30 Waveforms of V_L and i_L during Continuous-Conduction Mode

1.12.3 Advantages and Disadvantages of SMPS

The main *advantage* of SMPS is greater efficiency because the switching transistor dissipates little power when it operates outside of its active region. If the transistor operates just like a switch, there is a negligible voltage drop across it and a negligible current flow through it.

The other advantages of SMPS are smaller size and lighter weight compared to linear power supply and lower heat generation due to higher efficiency.

The *disadvantages* of SMPS are:

- greater complexity
- the generation of high-amplitude
- high-frequency energy that the low-pass filter must block to avoid electromagnetic interference (EMI)
- a ripple voltage at the switching frequency and the harmonic frequencies thereof.

1.12.4 Comparison Between Linear Regulated Power Supply and SMPS

Generally, two main types of regulated power supplies are available such as linear power supply and switch mode power supply (SMPS). The comparison between linear regulated power supply and SMPS i.e.unregulated AC-to-DC supplies with switching regulators in general is shown in Table 1.1.

Table 1.1 Comparison Between Linear Regulated Power Supply and SMPS

Parameter	*Linear Regulated Power Supply*	*SMPS*
Size and weight	Heatsinks are used in linear regulated power supply. Due to large size of heatsinks, size and weight of linear regulated power supply increases. Transformers, if used, are large due to low operating frequency, i.e., 50 Hz.	Smaller transformer are used in SMPS due to higher operating frequency, i.e., 50 kHz – 1 MHz. Size and weight of adequate RF shielding may be significant.
Output voltage	When transformer used in linear regulated power supply, any voltages available at output. If unregulated, voltage varies significantly with load.	Any voltages available at output, but the output voltage is limited only by transistor breakdown voltages in circuits. The output voltage varies little with load.
Efficiency	Efficiency largely depends on voltage difference between input and output. Since output voltage is regulated by dissipating excess power as heat resulting in a typical efficiency of 30–40%.	Output voltage of SMPS is regulated using duty cycle control. As the transistors are switched fully on or fully off, there will be very little resistive losses between input and the load. Hence, the efficiency of SMPS is very high compared to linear regulated power supply.
Complexity	Usually Liner regulated power supply is a simpler circuit than switched-mode circuits. than switched-mode circuits.	Since SMPS consists of a controller IC, one or several power transistors and diodes, inductors, and filter capacitors, SMPS is a complex circuit than Linear regulated power supply.
Radio Frequency Interference	*Mild* high-frequency interference may be generated by AC rectifier diodes under heavy current loading.	EMI/RFI produced due to the current being switched on and off sharply. Therefore, EMI filters and RF shielding are needed to reduce the disruptive interference.

1.13 78XX AND 79XX VOLTAGE REGULATOR ICs

The 78XX (L78XX, LM78XX, MC78XX) and 79XX (L79XX, LM79XX, MC79XX) are a family of self-contained fixed linear voltage regulator integrated circuits.

The 78XX and 79XX family ICs are commonly used in electronic circuits requiring a regulated power supply due to their ease-of-use and low cost. These voltage regulated ICs have only three pins: one for the regulated output voltage, one for the unregulated input voltage and one for ground. These ICs are able to supply load current from 100 mA to about 5 A. These devices are available in plastic or metal packages.

Figure 1.31 shows the basic connection of a three terminal voltage regulator IC to a load. In this figure V_{in} is an unregulated dc input voltage which is applied to input terminal (terminal-1), V_o is the regulated output dc voltage which is available from output terminal (terminal-2) and the terminal-3 is connected to ground.

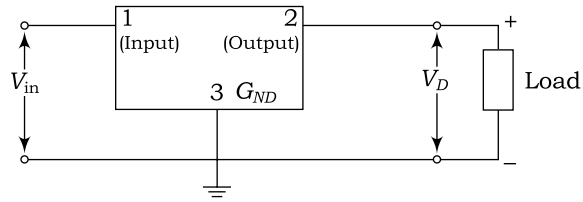


Fig. 1.31 Block diagram representation of voltage regulated IC.

For the ICs in 78XX and 79XX family, XX is replaced with two digit numbers, indicating the output voltage. For example, the 7805 IC has a 5 V output voltage, while the 7812 IC generates a 12 V output. Table 1.2 shows the positive voltage regulators in 78XX series.

Table 1.2 Positive voltage regulators in 78XX series

IC Number	*Output Voltage (V_o) in Volts*	*Maximum Input Voltage $V_{in\ (max)}$*	*Minimum Input Voltage $V_{in\ (min)}$*
7805	+5 V	35 V	7.3 V
7806	+6 V	35 V	8.3 V
7808	+8 V	35 V	10.5 V
7810	+10 V	35 V	12.5 V
7812	+12 V	35 V	14.6 V
7815	+15 V	35 V	17.5 V
7818	+18 V	35 V	21.0 V
7824	+24 V	40 V	27.2 V

These IC regulators have too much improved performances compared to voltage regulators using discrete components. These ICs have the following features:

- Current limiting
- Remote control operation over a wide range of input voltage
- Self-protection against over temperature

78XX ICs are designed as fixed voltage regulators and with adequate heat sinking can deliver output current 1 A or 1.5 A. These ICs do not require any external component to provide output voltage, but components can be employed for providing adjustable voltages and currents.

Figure 1.32 shows how an IC 7812 is connected to provide voltage regulation with output of +12 V dc. The unregulated input voltage V_{in} is filtered by capacitor C_1 and is connected to the IN terminal (pin – 1). The out terminal of IC provides a regulated +12 V which is filtered by capacitor C_2 and the pin-3 of the IC is connected to ground. When the input voltage may vary with a permissible voltage limit and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation range. These variations are usually mentioned in the manufacturer's data sheet. The difference between input and output voltages ($V_{in} - V_o$) is called the *dropout voltage* and its value is typically 20 V, even during the low ripple input voltage. The capacitor C_1 is used when the regulator is located at appreciable distance from a power supply filter. Though C_2 is not required, it can be used to improve the transient response of the regulator. The value of C_1 is typically 0.33 μF and the value of C_2 is typically 0.01 μF.

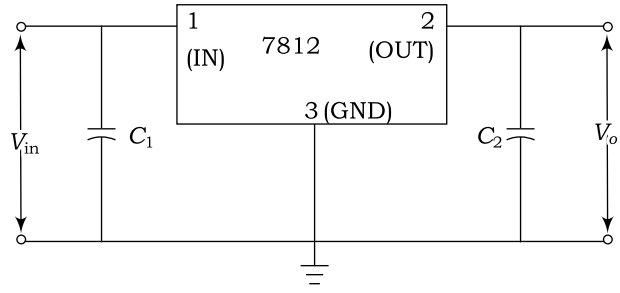


Fig. 1.32 Connection of 7812 voltage regulator IC

Figure 1.33 shows a circuit indicating the application of 78XX as an adjustable voltage regulator. The output voltage can be expressed by the equation

$$V_o = V_{\text{fixed}} + \left(\frac{V_{\text{fixed}}}{R_1} + I_Q \right) R_2$$

For example, if the IC is 7805, $V_{\text{fixed}} = 5$ V.

When $R_1 = R_2 = 1$ kΩ and I_Q is quiescent current in amperes (2 mA), the output voltage is equal to

$$V_o = 5 + \left(\frac{5}{1\ \text{k}\Omega} + 2\ \text{mA} \right) \times 1\ \text{k}\Omega = 15\ \text{V}.$$

Hence the output of IC 7805 regulator can be adjusted any value in between 5 V to 15 V. This example proves that the output of IC 7805 is adjusted to 15 V using external resistances R_1 and R_2.

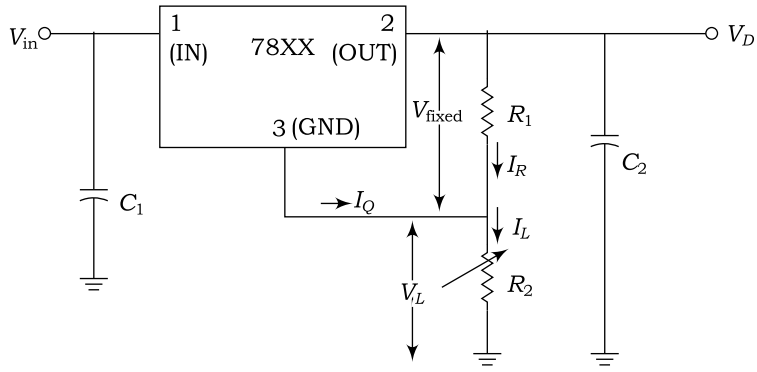


Fig. 1.33 78XX IC as an adjustable voltage regulator

The current flows though R_1 is $\frac{V_{\text{fixed}}}{R_1}$ and the current flows through load is $I_L = I_R + I_Q = \frac{V_{\text{fixed}}}{R_1} + I_Q$.

The output voltage with respect to ground is

$$V_o = V_{\text{fixed}} + V_L$$

The minimum input voltage required,

$$V_{in} = V_o + \text{drop out voltage}$$

The advantages and disadvantages of 78XX series ICs are given below:

Advantages of 78XX ICs

1. 78XX series ICs do not require any additional components to provide constant, regulated source of power, making them easy to use. These ICs are economical and efficient uses of space.
2. 78XX series ICs are built-in protection against a circuit drawing too much power. In some cases, the current limiting features of 78XX ICs can provide protection not only for the 78XX itself, but also other parts of the circuit.

Disadvantages of 78XX ICs

1. Always the input voltage must be higher than the output voltage by some minimum amount (typically 2 volts). This can make these ICs unsuitable for powering some devices from certain types of power sources.
2. Since these ICs are based on a linear regulator design, the input current required is always the same as the output current. As the input voltage must be greater than the output voltage, the total power input into the 78XX will be more than the output power. The extra input power is dissipated as heat. Therefore, in some applications, an adequate heatsink must be provided. As certain portion of input power is wasted during the process, these power supplies are less efficient compared to other power supplies.

79XX series ICs are complementary negative voltage regulators. 79XX IC has three terminals: terminal-1 is used for input voltage V_{in}, output voltage V_o is obtained from terminal-2 and terminal-3 is the ground. This IC provides a fixed negative output voltage. This IC has most of the same features, characteristics and package types of 78XX ICs. Figure 1.34 shows the circuit configuration of 79XX. The negative voltage regulators are available in the eight voltage options. In addition to first eight options, two extra voltage options –2 V and –5.2 V are also available in the negative 7900 series as depicted in Table 1.3.

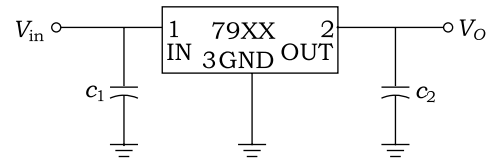


Fig. 1.34 Connection of 79XX voltage regulator

Table 1.3 Negative voltage regulators in 79XX series

IC Number	*Output Voltage (V_o) in volts*	*Maximum Input Voltage $V_{in\ (max)}$*	*Minimum Input Voltage $V_{in\ (min)}$*
7905	–5	–35	–7.3
7906	–6	–35	–8.4
7908	–8	–35	–10.5
7909	–9	–35	–11.5
7912	–12	–35	–14.6
7915	–15	–35	–17.7
7918	–18	–35	–20.8
7924	–24	–40	–27.1
7902	–2	–35	–4.1
7905.2	–5.2	–35	–7.5

In Fig. 1.34, the typical value of capacitor C_1 is 0.22 μF and C_1 is required if the power supply filter is located more than 3 inches away from the voltage regulated ICs. The typical value of C_2 is 1 μF, and C_2 is required for stability of the output voltage. Figure 1.35 shows the application of 79XX IC to provide an adjustable output voltage. The typical value of capacitor C_3 is 25 μF and C_3 is used to improve the transient response of the output voltage. The output voltage can be expressed by the equation.

$$V_o = V_{\text{fixed}}\left(\frac{R_1 + R_2}{R_2}\right)$$

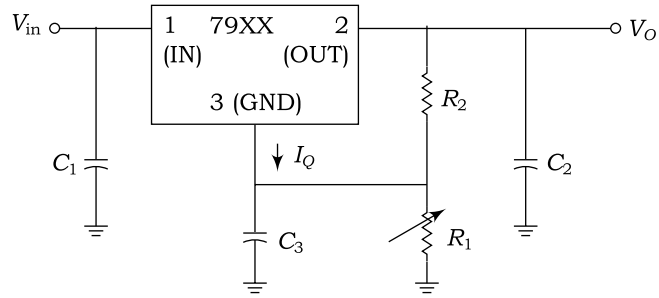


Fig. 1.35 79XX IC as an adjustable voltage regulator

Example 1.20 Figure 1.36 shows a voltage regulator circuit which will deliver a 0.5 A to a 25 Ω low load. Design the voltage regulator.

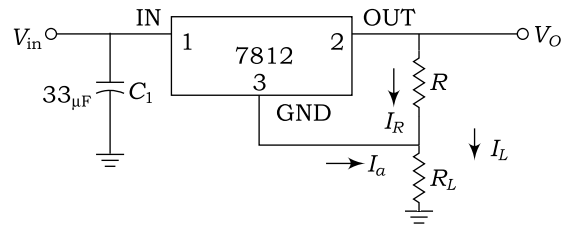


Fig. 1.36

Sol. When the quiescent current I_Q is neglected,

Current I_L = Current I_R.

The value of Resistance $R = \dfrac{V_{\text{fixed}}}{I_L}$

$$= \frac{12}{0.5}\ \Omega = 24\ \Omega$$

The output voltage is equal to

$$V_o = V_{\text{fixed}} + V_L = V_{\text{fixed}} + I_L R_L$$
$$= 12 + 0.5 \times 25 = 24.5\ \text{V}$$

The input voltage (minimum)

$$V_{in} = V_o + \text{minimum dropout voltage}$$
$$= 24.5 + 2 = 26.5\ \text{V}$$

Example 1.21 Find the regulated output voltage of the circuit diagram as shown in Fig. 1.37.

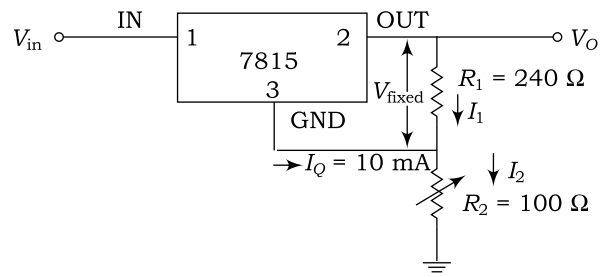


Fig. 1.37

Sol. Current flow through R_1 is

$$I_1 = \frac{V_{\text{fixed}}}{R_1}$$
$$= \frac{15}{240} = 0.0625\ \text{A}$$

Current flow through R_2 is

$$I_2 = I_1 + I_Q$$
$$= 0.0625 + 0.01 = 0.0725\ \text{A}$$

The output voltage is equal to

$$V_o = V_{\text{fixed}} + I_2 R_2$$
$$= 15 + 0.0725 \times 100\ \text{V} = 22.25\ \text{V}$$

Review Exercises

Short-Answer Questions

1. The output of a 50 Hz full-wave rectifier has a 50 Hz ripple. Does the circuit work properly?

Ans. When a full-wave rectifier operates with 50 Hz input, the lowest ripple frequency is equal to twice the input frequency, i.e., 100 Hz. Since the ripple frequency given here is 50 Hz, this circuit will not work properly.

2. What is a filter?

Ans. A filter is a circuit which converts the pulsating output voltage of rectifier into a smooth dc voltage.

3. Why is π-filter not suitable for time-varying load?

Ans. Since the voltage regulation of a π-filter is very poor, it is not suitable for time-varying load.

4. What is the importance of a bleeder resistance in a rectifier circuit using *LC* filter?

Ans. Bleeder resistance is connected in parallel with the load to maintain the minimum current through the choke and so the performance of the filter improves.

5. Define voltage regulation of a power supply.

Ans. Voltage regulation is the change in voltage from no load to full load and usually it is expressed by % regulation $= \dfrac{V_{NL} - V_{FL}}{V_{FL}} \times 100$.

6. What is the main drawback of a full-wave voltage double?

Ans. The main drawback of a full-wave voltage doubler is that there is no common ground between the input and output.

7. Why is a zener diode used as a voltage regulator?

Ans. The voltage across a zener diode remains constant until it gets lesser than the zener voltage V_Z. This property of a zener diode makes it useful as a voltage regulator.

8. What happens in series current, load current and zener current when the dc input voltage of a zener regulator increases?

Ans. Zener current and series current increases but the load current remains unchanged.

9. Explain how a zener diode maintains constant voltage across the load.

Ans. A zener diode behaves as battery during ON state. When a zener diode is connected with a shunt resistance R_L and if the voltage across the zener diode is greater than zener voltage V_Z, the zener diode is in ON state. Due to change in input voltage or in load resistance, the output voltage across the zener diode does not change. Hence, the zener diode provides constant voltage across load.

10. What is percentage regulation?

Ans. The change of dc output voltage is a function dc load current. The percentage regulation is equal to

$$\% \text{ regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 .$$

Multiple-Choice Questions

1. The function of a filter in a dc power supply is to
   (a) remove ripples from the rectified output signal
   (b) minimise voltage variations in ac input signal
   (c) reduce harmonics in rectified output signal
   (d) introduce more ripples into the rectified output signal
2. When a 50 Hz ac signal is fed to a rectifier, the ripple frequency of output voltage waveform for full bridge rectifier is
   (a) 25 Hz (b) 50 Hz (c) 100 Hz (d) 150 Hz
3. A half-wave rectifier is equivalent to
   (a) a clipping circuit (b) a clamper circuit
   (c) a clamper circuit with negative bias (c) a clamper circuit with positive bias
4. If the peak value of an applied voltage in a half-wave rectifier is V_m, the peak-inverse voltage of diode is
   (a) V_m (b) $2V_m$ (c) $\sqrt{2}V_m$ (d) $2\sqrt{2}V_m$
5. A full-wave rectifier has a twice the efficiency of a half-wave rectifier as
   (a) a full-wave rectifier uses a transformer
   (b) ripple factor of a full-wave rectifier is less
   (c) a full-wave rectifier utilises both half-cycle of the input signal
   (d) output frequency is equal to the line frequency
6. If the peak value of an applied voltage in a full-wave rectifier is V_m, the peak-inverse voltage of diode is
   (a) V_m (b) $2V_m$ (c) $\sqrt{2}V_m$ (d) $2\sqrt{2}V_m$
7. If the peak value of an applied voltage of each half of secondary winding of centre-tap transformer is V_m, the peak inverse voltage of each diode in a full-wave rectifier using centre tap transformer is
   (a) V_m (b) $2V_m$ (c) $\sqrt{2}V_m$ (d) $2\sqrt{2}V_m$
8. In an *LC* filter, the ripple factor
   (a) increases with the load current (b) increases with the load resistance
   (c) remains constant with the load current (d) decreases with the load current
9. The bleeder resistor is used in the filter circuit of a dc power supply to
   (a) reduce voltage regulation
   (b) improve voltage regulation
   (c) improve filtering action
   (d) improve voltage regulation and filtering action
10. Which rectifier requires four diodes?
    (a) Half-wave rectifier
    (b) Full-wave bridge circuit
    (c) Full-wave rectifier circuit using centre-tap transformer
    (d) Voltage clipping circuit

11. Which rectifier requires two diodes?
    (a) Half-wave rectifier
    (b) Full-wave bridge circuit
    (c) Full-wave rectifier circuit using centre-tap transformer
    (d) Voltage clipping circuit
12. Which circuit requires one diode?
    (a) Half-wave rectifier
    (b) Full-wave bridge circuit
    (c) Full-wave rectifier circuit using centre-tap transformer
    (d) Voltage clipping circuit
13. When 220 V dc voltage is connected to a bridge rectifier in place of an ac source, the bridge rectifier will be damaged due to short circuit of
    (a) one diode (b) two diodes
    (c) three diodes (d) four diodes
14. The polarity of dc output voltage of a half-wave rectifier can be reversed by reversing
    (a) transformer primary (b) the diode
    (c) transformer secondary (d) None of these
15. A capacitor filter as rectifier provides
    (a) poor voltage regulation (b) good voltage regulation
    (c) voltage regulation remain constant (d) None of these
16. In a dc regulated power supply, the ripple factor is a measure of
    (a) voltage regulation (b) filter efficiency
    (c) diode rating (d) quality of power output
17. A zener diode is invariably used
    (a) in reverse breakdown region (b) as an amplifier
    (c) as a voltage regulator (d) in forward bias region
18. When a zener diode is reverse biased,
    (a) it acts as a constant resistance (b) it acts as a constant voltage source
    (c) it acts as a constant current source (d) it acts as a variable voltage source
19. Which of the following elements is not an essential element of a dc power supply?
    (a) Voltage amplifier (b) Filter
    (c) Voltage regulator (d) Rectifier
20. A voltage regulator is a circuit which can be used
    (a) to convert the ac voltage to dc voltage
    (b) to provide a constant dc output voltage in spite of the fluctuations in ac input voltage or load current
    (c) to regulate the ac input voltage
    (d) All of these

21. The use of a capacitor filter in a rectifier circuit provides satisfactory performance only while
    (a) the load current is high (b) the load voltage is high
    (c) the load current is low (d) the load voltage is low
22. Which of the following voltage regulators is preferred to provide a large value of load current?
    (a) Zener diode shunt regulator (b) Transistor series regulator
    (c) Transistor shunt regulator (d) All of these
23. In a zener diode shunt voltage regulator, the diode regulates the output voltage when the zener diode
    (a) is forward biased (b) reverse biased
    (c) operates at no load (d) operates at any load
24. A 5 V dc regulated power supply has a regulation of 0.05 per cent. Its output voltage will vary within the range of
    (a) 4.9975 to 5.0025 V (b) 4.95 to 5.05 V
    (c) 4.995 to 5.00 V (d) 4.5 to 5. 5 V
25. The ripple factor in case of half-wave rectifier is
    (a) 0 (b) 0.75 (c) 1.21 (d) 1.5
26. The output voltage of IC 7915 is
    (a) 15 V (b) –15 V (c) 5 V (d) –5 V
27. The output voltage of IC 7815 is
    (a) 15 V (b) –15 V (c) 5 V (d) –5 V
28. A three-terminal monolithic IC regulator can be used as
    (a) a current regulator
    (b) an adjustable output voltage regulator
    (c) a current regulator and a power switch
    (d) an adjustable output voltage regulator and a current regulator
29. IC regulators have the inherent advantages compared to voltage regulators made by discrete components
    (a) current limiting (b) self protection against high temperature
    (c) remote control (d) All of these
30. A switching voltage regulator can be _____ types.
    (a) step-up (b) step-down
    (c) inverting (d) step-up or step-down or inverting
31. In a SMPS, after conversion of ac supply to dc voltage, a transistor is switched ON and OFF at high speed using a PWM. The frequency of PWM is about
    (a) 20 kHz – 50 kHz (b) 2 kHz – 5 kHz
    (c) 500 Hz – 1 kHz (d) 100 Hz – 200 Hz

Review Questions

1. Define filter. Why are filters used in a dc power supply?
2. What is filter? Explain the working principle of a capacitive filter with a suitable diagram.
3. What are the types of filters? Explain any two types with circuit diagram and wave form.
   What is the function of bleeder resistance in filter?

4. Explain *LC* filter and Π-filter with suitable diagram.
5. Draw the *V-I* characteristic of a zener diode and explain the working principle of zener diode.
6. What is a zener diode? Explain the symbol and equivalent circuits of an ideal and a real zener diode. How does a zener diode maintain constant output voltage?
7. Explain a zener shunt regulator circuit. What are the disadvantages of zener shunt regulator?
8. Draw circuit diagram of transistor shunt regulator. Explain its operation briefly.
9. Draw circuit diagram of a transistorised series voltage regulator. Explain its operation briefly.
10. What is ripple factor? Why is ripple factor so important in power supply? Derive the expression of ripple factor of a half-wave rectifier and full-wave rectifier using centre-tap transformer.
11. Sketch a two-diode full-wave rectifier circuit for producing a positive output voltage. Sketch the input and output waveforms and explain the circuit operation.
12. (a) What is voltage regulator? What are the types of voltage regulators?
    (b) Draw the circuit diagram of a regulated power supply and explain its operating principle in detail.
13. Define line regulation and load regulation in a voltage regulator.
14. The output voltage of a full-wave rectifier circuit is fed to an inductor filter. Design the inductor filter if the ripple factor of filter output voltage is 2% for a load resistance 100 Ω and the supply frequency is 50 Hz.
15. The output voltage of a half-wave rectifier circuit is fed to a capacitor filter. Design the capacitor filter if the ripple factor of filter output voltage is 1.5% for a load resistance 1500 Ω and the supply frequency is 50 Hz.
16. Design an *LC* filter when the output voltage of a full-wave rectifier circuit is fed to filter circuit and the ripple factor is 0.015 and the supply frequency is 50 Hz. Assume $L = 1.1$ H.
17. If the reverse saturation current in a zener diode changes from 35 mA to 60 mA corresponding to change in reverse voltage 4.8 V to 4.85 V, determine the dynamic resistance of zener diode.
18. A 10 V dc regulated power supply has a regulation of 2%. Determine the magnitude of change in output voltage.
19. A dc regulated power supply has a line regulation of 5 μV/V. Determine the change in output voltage when change in input voltage is 4 V.
20. A dc voltage regulator power has a load regulation of 2.5 V/mA. At no load, the output voltage is 12 V. Calculate the output voltage at full load when the full-load current is 200 mA.
21. A zener diode shunt regulated power supply is depicted in Fig. 1.38. Determine (a) the output voltage, (b) source current, and (c) current through the zener diode. Assume zener resistance is equal to zero.

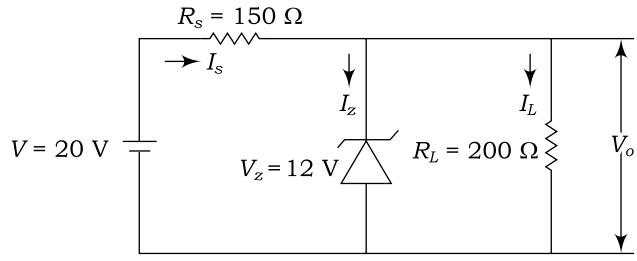


Fig. 1.38

22. Design a zener diode shunt regulated power supply with the following specifications: (a) the output voltage is 10 V, (b) load current is 50 mA, (c) maximum zener power dissipation 500 mW, and (d) input voltage 15 ± 2 V.
23. In a zener diode shunt regulated power supply, V_O = 10 V, I_L = 50 mA, $P_{Z(max)}$ = 1000 mV and input voltage varies from 20 V to 30 V. Determine the maximum and minimum value of zener current.
24. A transistor shunt regulated power supply is shown in Fig. 1.39. Determine (a) the output voltage, (b) load current, and (c) source current. Assume zener resistance is equal to zero, V_{BE} = 0.7 V and $R_B = \infty$.

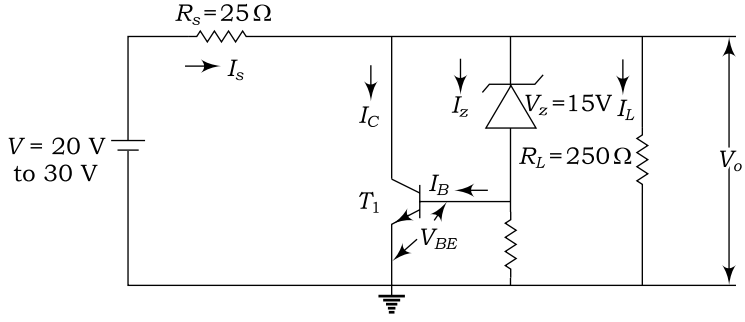


Fig. 1.39

25. A transistor series regulated power supply is shown in Fig. 1.40. Determine (a) the output voltage, (b) load current, and (c) zener current. Assume zener resistance is equal to zero, and V_{BE} = 0.7 V.

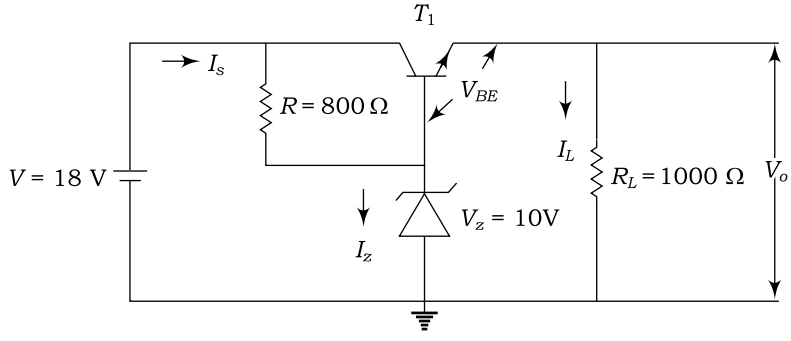


Fig. 1.40

26. Write short notes on the followings: (a) Switched Mode Power Supply, (b) 78XX Voltage Regulator IC, (c) 79XX Voltage Regulator IC
27. Figure 1.41 shows a circuit of a current regulator. What is the value of R_1 to provide a constant current of 1 A. Assume I_Q = 10 mA.

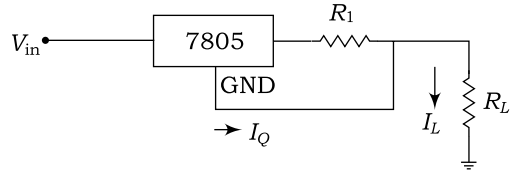


Fig. 1.41

28. (a) What are the merits of switched mode power supply over regulated power supply? (b) With the help of a neat circuit diagram briefly explain the operation of a switched mode power supply.

ANSWERS

Multiple-Choice Questions

1. (a)	2. (c)	3. (a)	4. (a)	5. (c)	6. (a)	7. (b)
8. (c)	9. (d)	10. (b)	11. (c)	12. (a,d)	13. (d)	14. (b)
15. (b)	16. (d)	17. (a,c)	18. (b)	19. (a)	20. (b)	21. (c)
22. (b)	23. (b)	24. (a)	25. (c)	26. (b)	27. (a)	28. (a)
29. (d)	30. (d)	31. (a)				

CHAPTER

2

Transistor Biasing and Stability

2.1 INTRODUCTION

In reality, a transistor is the solid-state version of a vacuum triode, which was initially known as *semiconductor triode*. The *terminology* transistor is attributed to John R Pierce. Initially, the point-contact transistor was invented by J Bardeen, W Brattain and W Shockley in the Bell laboratories in 1947. After that, the bipolar junction transistor (BJT) was developed in 1950 and it was commercially used in the telephone switching circuits in 1952.

A bipolar junction transistor (BJT) has three differently doped semiconductor regions. Two of these regions are doped with either acceptor or donor atoms and the third region is doped with another type of atoms. Actually, a BJT consists of two *PN*-junctions which are placed back to back. The word "bipolar" is used to state the role of both charge carriers (electrons and holes). In this chapter, bipolar junction transistors and its associated topics are discussed elaborately.

2.2 BIPOLAR JUNCTION TRANSISTOR

A bipolar junction transistor (BJT) has a silicon or germanium crystal. It would either have a layer of *N*-type semiconductor sandwiched between two layers of *P*-type semiconductor or a layer of *P*-type semiconductor between two layers of *N*-type semiconductor materials. The first type of transistor is called a *PNP* transistor, and the second one is called an *NPN* transistor. The sandwich of semiconductor is very small and sealed inside either a metal or plastic case to protect it from moisture.

Figure 2.1(a) shows a *PNP* transistor and Fig. 2.1(b) shows an *NPN* transistor. It is clear from Fig. 2.1 that transistors have three regions known as Emitter (E), Base (B) and Collector (C).

1. Emitter (E)

The emitter region is placed on one side of the transistor. This region provides charge carriers (either electrons or holes) to the base and collector regions. The emitter region is always heavily doped (about 10^{19} per cm^3) with donor or acceptor atoms.

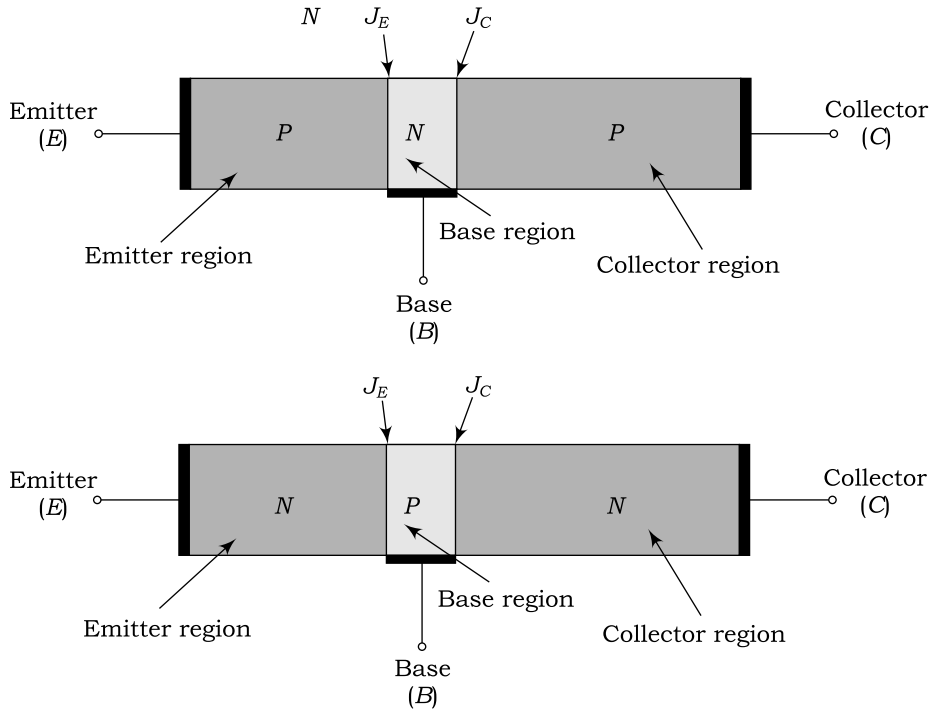


Fig. 2.1 Construction of (a) PNP transistors (b) NPN transistors

2. Base (B)

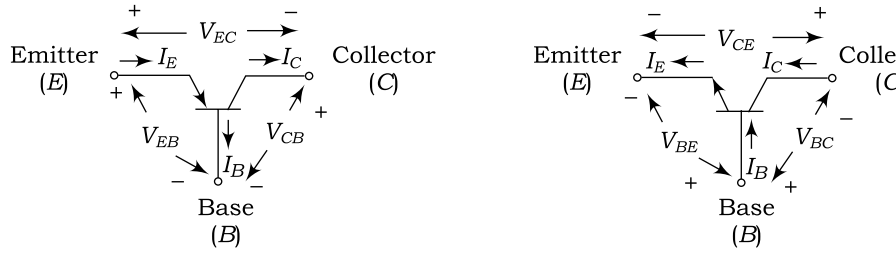
The base region is situated in the middle of two *N*- or *P*-regions and forms two *PN*-junctions in the transistor. Usually, the base of a transistor is thin compared to the emitter and collector region and this region is lightly doped (about 10^{16} per cm^3).

3. Collector (C)

The collector region is placed on the opposite side of the emitter and it collects charge carriers (either electrons or holes). The collector region of a transistor is always larger than the emitter region and base region of the transistor. The doping level of a collector is less than the doping level of an emitter, but greater than the doping level of base region (about 10^{17} per cm^3).

The transistor has two *PN*-junctions, namely *emitter-base junction* (J_E) and *collector-base junction* (J_C). The junction between emitter and base regions is known as emitter-base junction (J_E). Similarly, the junction between collector and base regions is known as collector-base junction (J_C).

The symbols of *PNP* and *NPN* transistors are depicted in Fig. 2.2. The arrow on the emitter terminal represents the direction of current flow while the base emitter junction is forward biased. The emitter, base and collector currents are represented by I_E, I_B and I_C respectively as shown in Fig. 2.2. The V_{BE} represents the voltage drop across base to emitter of transistor. Similarly, V_{CB} and V_{CE} are the voltage drops across the collector base and collector emitter respectively.



$V_{EB} = V_E - V_B$ $\quad V_{EC} = V_E - V_C = V_{EB} - V_{CB}$
$V_{CB} = V_C - V_B$

(a)

$V_{BE} = V_B - V_E$ $\quad V_{CE} = V_C - V_E = V_{CB} - V_{EB}$
$V_{BC} = V_B - V_C$

(b)

Fig. 2.2 Symbol of (a) PNP transistors (b) NPN transistors

2.3 BIASING OF BIPOLAR JUNCTION TRANSISTOR (BJT)

Actually, there is no use of unbiased bipolar junction transistor. The dc voltage source or battery is connected across the terminals of BJT for proper operation of transistor. When dc voltages are applied across the emitter (E), base (B) and collector (C) terminals of a bipolar junction transistor, this connection is called *biasing*. There are three different biasing methods of a transistor such as *forward active*, *saturation* and *cut-off*.

1. Forward Active

Figure 2.3 shows the forward active mode of transistor biasing. In this mode of operation, the emitter-base junction (J_E) of transistor is forward biased and the collector-base junction (J_C) is reverse biased. During forward active biasing, the negative terminal of dc voltage source or battery is connected to the N-type region and positive terminal is connected to the P-type region. During reverse biasing, the connections will be opposite of forward biasing.

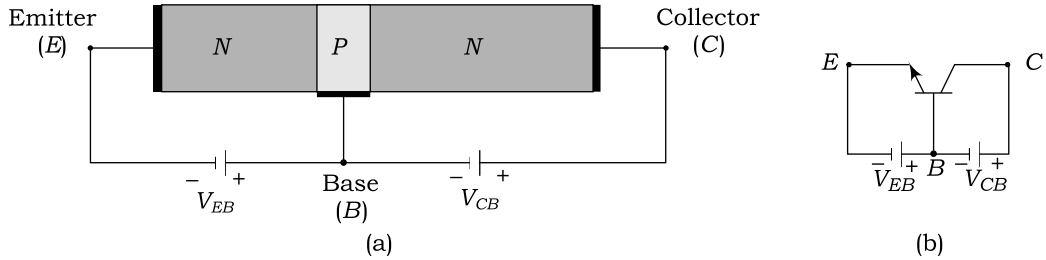


Fig. 2.3 (a) and (b): Forward active mode of transistor biasing

2. Saturation

Figure 2.4 shows the saturation mode of transistor biasing. In this mode, the emitter-base junction and the collector-base junction of a transistor are forward biased. During this mode of operation, the transistor has very high value of current. When the transistor operates in saturation mode, it behaves as a closed switch.

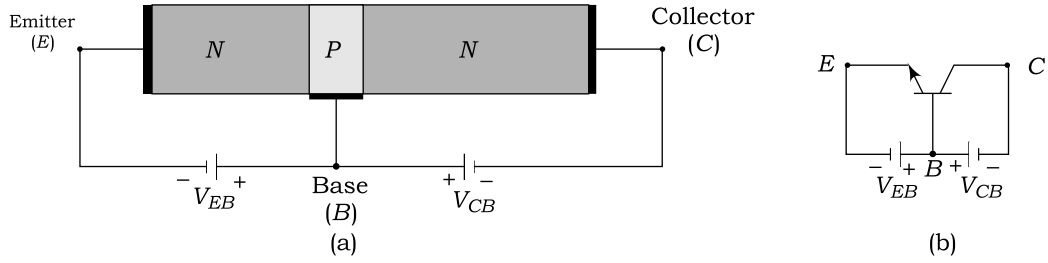


Fig. 2.4 (a) and (b): Saturation mode of transistor biasing

3. Cut-off

Figure 2.5 shows the cut-off mode of transistor biasing. In this mode, the emitter-base and collector-base junction of a transistor are reverse biased. During this mode of operation, the current flow through the transistor is zero and it acts as an open switch.

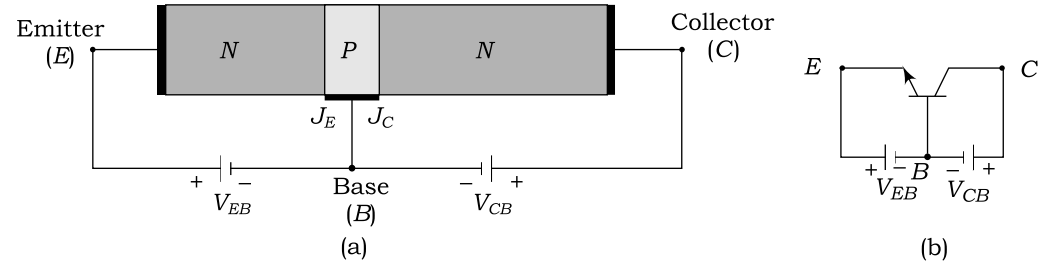


Fig. 2.5 (a) and (b): Cut-off mode of transistor biasing

Table 2.1 shows the junction biasing conditions of a transistor for three different operating modes. A transistor is used as an amplifier in the forward active mode. The transistor acts as a switch during saturation and cut-off modes. In saturation mode, transistor behaves as a closed switch and it acts as an open switch during cut-off mode operation.

Table 2.1 Operating modes of a transistor

Operating Modes	*Emitter-base Junction*	*Collector-base Junction*
Forward active	Forward biased	Reverse biased
Saturation	Forward biased	Forward biased
Cut-off	Reverse biased	Reverse biased

2.4 CURRENT IN A BIPOLAR JUNCTION TRANSISTOR

The direction of current flow in an *NPN* transistor is always in opposite direction of the flow of electrons as shown in Fig. 2.6. In a *PNP* transistor, the direction of current flow is always in the same direction of the flow of holes as shown in Fig. 2.7.

In Figs 2.6 and 2.7, I_E is the emitter current, I_B is the base current and I_C is the collector current. If we apply Kirchhoff's Current Law (KCL), the emitter current is equal to the sum of the collector and base currents and it can be expressed as

$$I_E = I_B + I_C \tag{2.1}$$

Usually, I_B is very small and it can be neglected. Then the emitter current is equal to the base current ($I_E = I_C$).

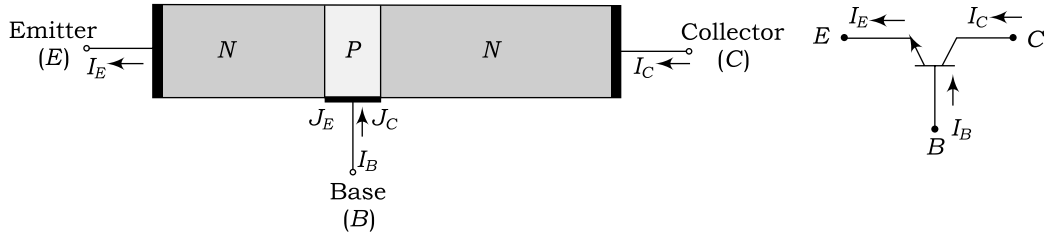


Fig. 2.6 Current flows through NPN transistor

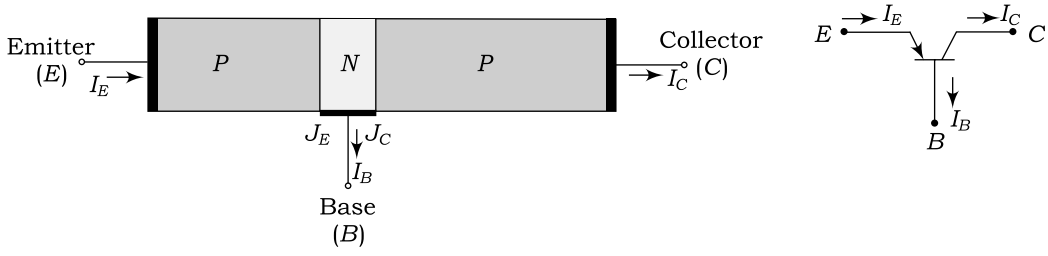


Fig. 2.7 Current flows through PNP transistor

2.5 CIRCUIT CONFIGURATION OF A BIPOLAR JUNCTION TRANSISTOR

A transistor has three terminals: emitter (*E*), base (*B*) and collector (*C*) and two junctions such as emitter-base junction (J_E) and collector-base junction (J_C). Each of these junctions (J_E and J_C) requires two terminals for a biasing arrangement. When a transistor is connected in a circuit, it requires four terminals, i.e., two input terminals and two output terminals. Therefore, one of the three transistor terminals (emitter, base and collector) is used as a common terminal between input and output. Depending upon the common terminal, the transistor may be connected into the three different configurations such as common emitter (*CE*), common base (*CB*) and common collector (*CC*) configurations.

2.5.1 Common Emitter (CE) Configuration

In common-emitter configuration, the emitter of a transistor is connected as a common terminal between input and output as shown in Fig. 2.8. The input signal is applied between the emitter and base terminals. The output will be obtained from the collector and emitter terminals. The common emitter configuration of transistor is the most commonly used one in circuits.

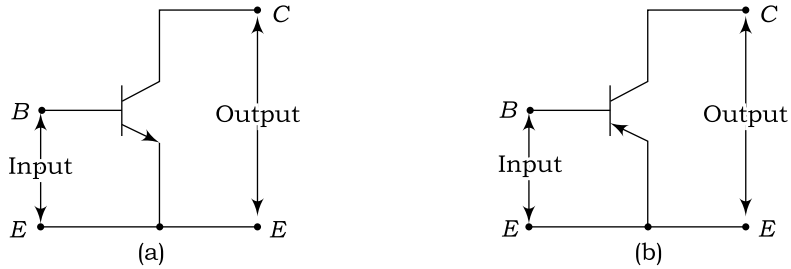


Fig. 2.8 Common emitter configuration of (a) NPN transistor (b) PNP transistor

2.5.2 Common-Base (CB) Configuration

In this circuit configuration of a transistor, the base terminal is used as a common terminal between input and output as depicted in Fig. 2.9. The input signal is applied between the emitter and base terminals. The output will be taken from the collector and base terminals. To explain the operation of *NPN* and *PNP* transistors, the common base configuration is used.

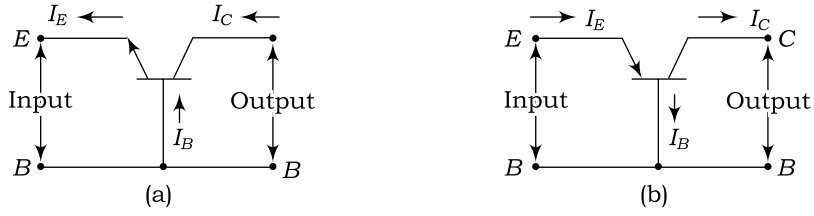


Fig. 2.9 Common-base configuration of (a) NPN transistor (b) PNP transistor

2.5.3 Common-Collector (CC) Configuration

In common-collector configuration, the collector terminal of a transistor is connected as common terminal between input and output as depicted in Fig. 2.10. The base and collector terminals are used to apply input signal whereas the output signal is obtained from the emitter and collector terminal.

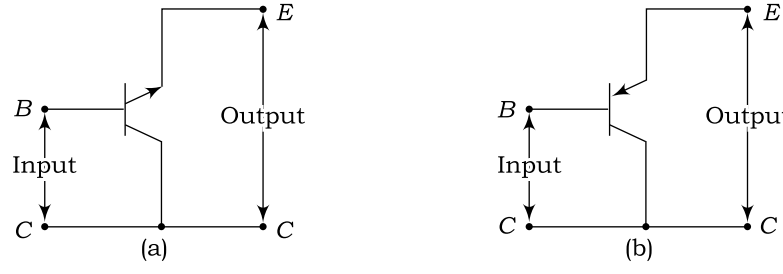


Fig. 2.10 Common-collector configuration of (a) NPN transistor (a) PNP transistor

2.6 CURRENT GAIN OF A BJT IN COMMON-BASE CONFIGURATION

Figure 2.11(a) shows a common-base configuration of a *NPN* transistor. *I*n this circuit configuration, the emitter current is the input current and the collector current is the output current. The current gain of a transistor in the common-base configuration is the ratio of collector current I_C (output current) to the emitter current I_E (input current). Since the input and output currents are either dc or ac, there are two types of current gains known as dc current gain and ac current gain.

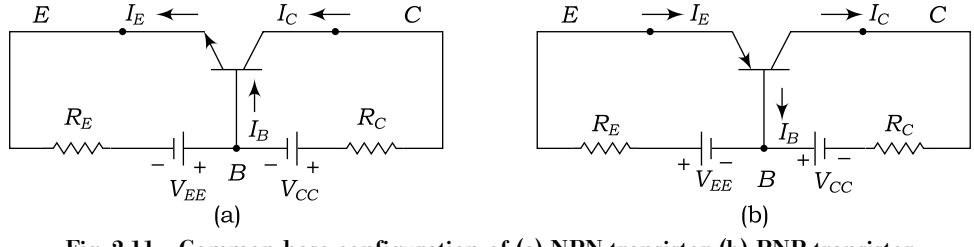


Fig. 2.11 Common-base configuration of (a) NPN transistor (b) PNP transistor

2.6.1 Common-Base dc Current Gain

The common-base dc current gain (α) is defined as the ratio of the collector current (I_C) and the emitter current (I_E) and it is represented by α or h_{FB} or α_{dc}. The dc current gain α can be expressed as

$$\alpha = \frac{I_C}{I_E} \tag{2.2}$$

Since the collector current is always less than the emitter current, the dc current gain α is always less than unity. Usually, the value of α is about 0.98. The dc current can be made closer to unity by controlling the width and doping level of base region as less as possible. Practically, α varies in between 0.95 to 0.998.

From the above equation, we get

the collector current $I_C = \alpha I_E$

The emitter current is

$$I_E = I_B + I_C$$

or

$$I_E = I_B + \alpha I_E \qquad \text{as } I_C = \alpha I_E$$

Then the base current is

$$I_B = (1 - \alpha) I_E \tag{2.3}$$

2.6.2 Common-Base ac Current Gain

The ac current gain can be defined by the ratio of small change in collector current (ΔI_C) to the small change in the emitter current (ΔI_E) when the collector to base voltage (V_{CB}) remain constant. The ac current gain is represented by α_0 or h_{fb} or α_{ac} and it is given by

$$\alpha_0 = \frac{\Delta I_C}{\Delta I_E} \tag{2.4}$$

This current is also known as *small-signal common-base current gain* or *common-base short-circuit current gain*. Normally, α_0 is less than unity and it is equal to α. Therefore, for practical applications, the dc current gain is equal to the ac current gain ($\alpha = \alpha_0$).

2.7 CURRENT GAIN OF A BJT IN COMMON-EMITTER CONFIGURATION

Figure 2.12(a) shows a common-emitter configuration of an *NPN* transistor. In this configuration, the base current is the input current and the collector current is the output current. The current gain of a transistor is the ratio of collector current I_C (output current) to the base current I_B (input current). As the input and output currents are either dc or ac, there are two types of current gains such as dc current gain and ac current gain.

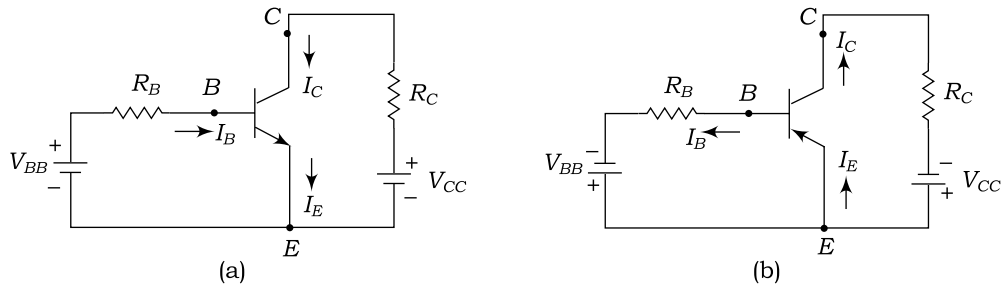


Fig. 2.12 Common-emitter configuration of (a) NPN transistor (b) PNP transistor

2.7.1 Common-Emitter dc Current Gain

The common-emitter dc current gain (β) is defined as the ratio of the collector current (I_C) and the base current (I_B). It is represented by β or h_{FE} or β_{dc} and it can be expressed as

$$\beta = \frac{I_C}{I_B} \tag{2.5}$$

The common-emitter dc current gain β of a transistor is also known as *large-signal common emitter current gain*. Since the collector current of a bipolar junction transistor is always greater than the base current, the value of dc current gain (β) must be greater than unity. For example, when the collector current $I_C = 4$ mA and the base current $I_B = 0.04$ mA, the common-emitter dc current gain β is equal to 100. Hence, the collector current is 100 times that of base current. Usually, β varies in the range from 20 to 250.

2.7.2 Common-Emitter ac Current Gain

The common-emitter ac current gain is defined as the ratio of small change in collector current (ΔI_C) to the small change in the base current (ΔI_B) when the collector to emitter voltage (V_{CE}) is constant. The ac current gain is represented by β_0 or h_{fe} or β_{ac} and it can be expressed as

$$\beta_0 = \frac{\Delta I_C}{\Delta I_B} \tag{2.6}$$

This current is also known as *small-signal common-emitter current gain* or *common-emitter short circuit current gain*. Usually, the β_0 or h_{fe} is used in the analysis of small signal transistor amplifier circuits. In all practical applications, the dc current gain is equal to the ac current gain ($\beta = \beta_0$).

Generally, the common-collector current gain β varies with the collector current (I_C) and junction temperature (T_j). Figure 2.13 shows the variation of β with temperature and collector current (I_C) in mA. β is maximum at a certain value of collector current I_C. At constant collector current, β increases with increase in junction temperature as depicted in Fig. 2.13.

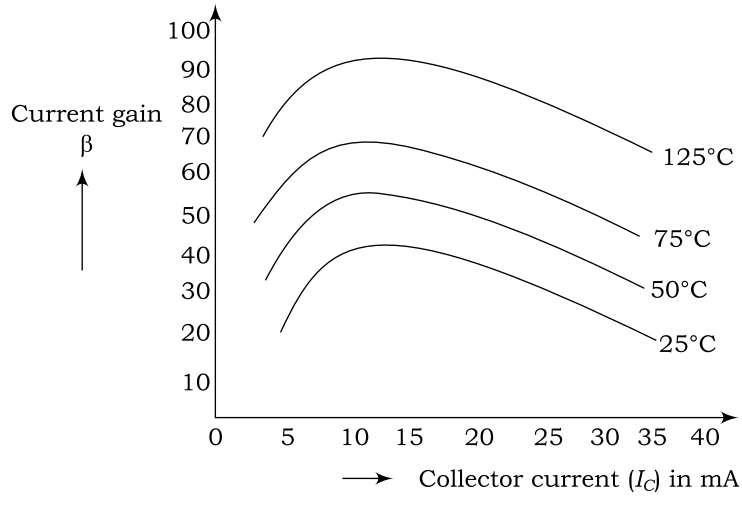


Fig. 2.13 The variation of β with respect of collector current and temperature

2.8 RELATION BETWEEN α AND β

It is well known that the emitter current (I_E) of a transistor is the sum of the base current (I_B) and collector current (I_C) and it can be expressed as

$$I_E = I_B + I_C$$

After dividing both sides of above equation by I_C, we get

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

As current gain $\alpha = \frac{I_C}{I_E}$ and the current gain $\beta = \frac{I_C}{I_B}$, the above equation can be written as

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 = \frac{1+\beta}{\beta}$$

or

$$\alpha = \frac{\beta}{\beta + 1}$$

The above expression can also be written as

$$\beta = \alpha(\beta + 1) = \alpha\beta + \alpha$$

or

$$\beta = \frac{\alpha}{1 - \alpha} \tag{2.7}$$

2.9 CURRENT GAIN OF A BJT IN COMMON-COLLECTOR CONFIGURATION

The common-collector configuration of a BJT is shown in Fig. 2.14. The emitter-base junction is forward biased by voltage V_{BB} and the collector-base junction is reverse biased by V_{CC}. As the voltage of dc supply source V_{CC} has zero resistance to ac signal, an external resistance R_E is connected between the emitter and ground. The output voltage is obtained from the voltage across the external resistance R_E.

In a common-collector transistor configuration, the input current is the base current (I_B) and the output current is the emitter current (I_E). Consequently, the common collector current gain is given by the equation

$$\frac{I_E}{I_B} = \frac{I_E}{I_C} \times \frac{I_C}{I_B}$$

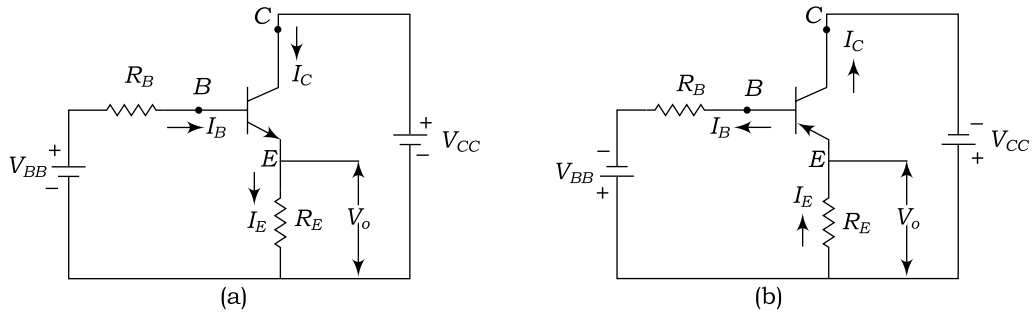


Fig. 2.14 Common collector configuration of (a) NPN transistor (b) PNP transistor

or
$$\frac{I_E}{I_B} = \frac{1}{\alpha} \times \beta \qquad \text{as } \alpha = \frac{I_C}{I_E} \text{ and } \beta = \frac{I_C}{I_B} \tag{2.8}$$

We know that $\alpha = \frac{\beta}{\beta + 1}$. After substituting the value of α in the above equation, we get

$$\frac{I_E}{I_B} = \frac{1}{\alpha} \times \beta = \frac{\beta + 1}{\beta} \times \beta = \beta + 1 \tag{2.9}$$

Hence, the common-collector current gain is equal to $\beta + 1$. Therefore, the emitter current in a common-collector transistor circuit is $\beta + 1$ times that of the base current. As $\beta >> 1$, the common-collector gain is equal to β.

Example 2.1 A transistor has an α of 0.98. Determine the value of β.

Sol. Given**:** $\alpha = 0.98$

The value of $\beta = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = 49$

Example 2.2 A transistor has a β of 100. Find the value of α.

Sol. Given: $\beta = 100$

The value of $\alpha = \frac{\beta}{\beta + 1} = \frac{100}{100 + 1} = 0.99$

Example 2.3 The collector current of a transistor is 100 mA and its β is 75. Calculate the value of base current and emitter current.

Sol. Given: $I_C = 100$ mA, and $\beta = 75$

The value of $\alpha = \frac{\beta}{\beta + 1} = \frac{75}{75 + 1} = 0.986$

As the current gain $\alpha = \frac{I_C}{I_E}$, the emitter current is

$$I_E = \alpha I_C = 0.986 \times 100 \text{ mA} = 98.6 \text{ mA}$$

Since the current gain $\beta = \frac{I_C}{I_B}$, the base current is

$$I_B = \frac{I_C}{\beta} = \frac{100}{75} \text{mA} = 1.33 \text{ mA}$$

Example 2.4 A transistor has $\beta = 90$ and the emitter current is 80 mA. Determine the value of base current and collector current.

Sol. Given: $\beta = 90$ and $I_E = 80$ mA

The value of $\alpha = \frac{\beta}{\beta + 1} = \frac{90}{90 + 1} = 0.989$

Since the current gain $\alpha = \frac{I_C}{I_E}$, the collector current is

$$I_C = \alpha I_E = 0.989 \times 80 \text{ mA} = 79.12 \text{ mA}$$

As the current gain $\beta = \frac{I_C}{I_B}$, the base current is

$$I_B = \frac{I_C}{\beta} = \frac{79.12}{90}\text{mA} = 0.879\text{ mA}$$

Example 2.5 A transistor has a base current $I_B = 100\ \mu A$ and the collector current (I_C) is equal to 5 mA. (a) Determine the value of β, α and emitter current. (b) If the base current changes by 25 μA and the corresponding collector current change is 0.5 mA, calculate the new value of β.

Sol. Given $I_B = 100\ \mu A$ and $I_C = 5$ mA

(a) The current gain $\beta = \frac{I_C}{I_B} = \frac{5 \times 10^{-3}}{100 \times 10^{-6}} = 50$

The value of $\alpha = \frac{\beta}{\beta + 1} = \frac{50}{50 + 1} = 0.98$

The emitter current is

$$I_E = I_B + I_C = 100\ \mu A + 5\text{ mA} = 5.1\text{ mA}$$

(b) The change in base current is $\Delta I_B = 25\ \mu A$ and the change in collector current is $\Delta I_C = 0.5$ mA
The new base current is $I_B = 100\ \mu A + 25\ \mu A = 125\ \mu A$
The new collector current is $I_C = 5\text{ mA} + 0.5\text{ mA} = 5.5\text{ mA}$
The new value of β is

$$\beta = \frac{I_C}{I_B} = \frac{5.5 \times 10^{-3}}{125 \times 10^{-6}} = 44$$

Example 2.6 A transistor has a base current $I_B = 150\ \mu A$, $I_{C0} = 10\ \mu A$ and $\alpha = .98$. Calculate the collector current (I_C) and emitter current (I_E).

Sol. Given: $I_B = 150\ \mu A$, $I_{C0} = 10\ \mu A$ and $\alpha = .98$

The collector current is

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{C0}}{1-\alpha}$$

$$= \frac{0.98}{1-0.98} \times 150 + \frac{10}{1-0.98}\mu A = 7850\ \mu A = 7.85\text{ mA}$$

The emitter current is

$$I_E = I_B + I_C = 150\mu A + 7850\ \mu A = 8000\ \mu A = 8.0\text{ mA}$$

Example 2.7 The common-base dc current gain of a transistor is 0.97. When the emitter current is 150 mA, determine the base current and collector current.

Sol. Given: $\alpha = 0.95$, and $I_E = 150$ mA

The common-base dc current gain is

$$\alpha = \frac{I_C}{I_E}$$

The collector current is $I_C = \alpha I_E = 0.97 \times 150 \text{ mA} = 145.5 \text{ mA}$

The value of $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.97}{1-0.97} = 32.33$

The base current is equal to

$$I_B = \frac{I_C}{\beta} = \frac{145.5}{32.33} = 4.5 \text{ mA}$$

2.10 TRANSISTOR BIASING AND BIAS STABILITY

Transistors are used in different applications such as small-signal amplifier, large-signal amplifier, voltage-amplifier, power amplifier, common-base (*CB*) amplifier, common-emitter (*CE*) amplifier, common-collector (*CC*) amplifier, direct coupled amplifier, *R*C coupled amplifier and transformer coupled amplifier, etc. To use a transistor as an amplifier, it is necessary to bias the transistor to operate in active region where it can provide a constant voltage gain for proper amplification.

Actually, the biasing arrangement of a transistor can turn the transistor ON and place it in the active region where it can operate linearly. The biasing means that a fixed current should flow through the transistor with a constant voltage drop across the transistor junctions. Generally, the collector current I_C, base current I_B, collector-to-emitter voltage V_{CE} and base to emitter voltage V_{BE} are set by the biasing circuit. When the adequate or required voltages and currents exist in a transistor, the small-signal voltages will be amplified and the transistor can amplify the small-signal voltage without changing the shape. Usually, the transistor operates at the quiescent operating point in the active region of output characteristics. The operating point changes with temperature variation, as the transistor parameters such as current gain β, reverse saturation current $I_{C0,}$ and the base to emitter voltage V_{BE} are functions of temperature T. In this section, the stability of different biasing circuits and the compensation techniques to improve the stability of biasing circuits are discussed elaborately.

2.11 *Q*-POINT AND LOAD LINE

The different biasing arrangements of transistors are already explained in detail. When the biasing voltages are applied in a transistor and a fixed value of currents (base current I_B, collector current I_C and emitter current I_E) flow through the transistor, the transistor operates in a point with these current and voltages. This point is called the *operating point* or *quiescent point* or *Q-point*. As the amplitude of voltages and currents are constant due to biasing, the operating point is called the *dc operating point*.

Figure 2.15 shows a common-emitter configuration of a transistor. The transistor is biased by the voltages V_{BB} and V_{CC} and the fixed currents I_B and I_C flow through the transistor. The base-to-emitter voltage V_{BE} and collector-to-emitter voltage V_{CE} of the transistor are constant. The output characteristics of a common-emitter configuration is shown is Fig. 2.16 at different values of base current.

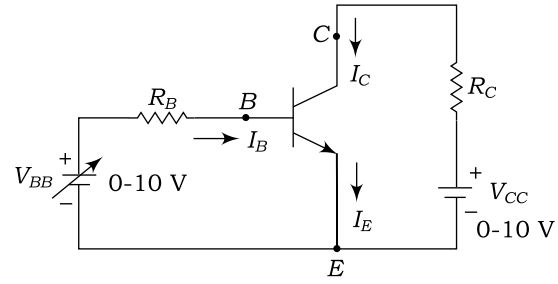


Fig. 2.15 Common-emitter configuration of a transistor

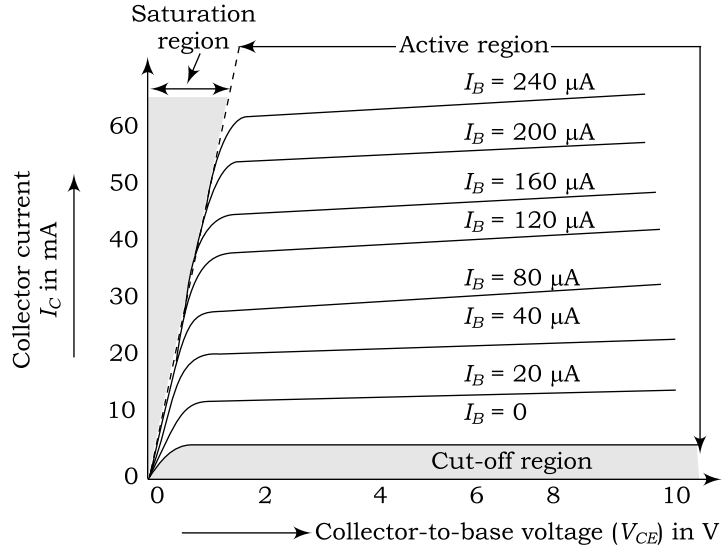


Fig. 2.16(a) Output characteristics of a common-emitter transistor configuration

For example, if the V_{BB} provides a base current of 200 μA, the corresponding collector current is

$$I_C = \beta I_B = 250 \times 200 \times 10^{-6} = 50 \text{ mA and}$$

the corresponding collector-to-emitter voltage

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 10 - 50 \times 10^{-3} \times 160 = 2\text{V}$$

As V_{CC} = 10 V, I_C = 50 mA and R_C = 160 Ω

The values of collector current (I_C) and the collector-to-emitter voltage V_{CE} describe the Q-point as Q_1 on the characteristics curves. The Q_1 point is represented by 2 V, 50 mA.

Similarly, if the base current is 160 μA, I_C = 40 mA and V_{CE} = 3.6 V, the new operating point is Q_2. In the same way, another operating point Q_3 is marked on the characteristics curves.

When the Q points Q_1, Q_2 and Q_3 are joined, a straight line is obtained and this line is called *dc load line.* It is clear from the Fig. 2.16(b) that the base current (I_B) and the collector current (I_C) increases when the collector to emitter voltage (V_{CE}) decreases. Similarly, when the collector to emitter voltage (V_{CE}) increases, the base current (I_B), and the collector current (I_C) decreases. Therefore, the voltage V_{BB} can be increased or decreased; the operating point of a transistor can be shifted in upward or downward along a straight line which is the connection of Q points.

The values of collector current (I_C), and collector-to-emitter voltage (V_{CE}) are obtained from any operating point of the dc load line. When the base current is zero, the collector current is about zero. Actually, a very small reverse saturation current (I_{CB0}) flows at cut-off point of transistor. Therefore, the collector-to-emitter voltage is less than the V_{CC}.

The load line intersects horizontal axis as well as vertical axis. The intersect point on vertical axis is I_C = 65 mA and V_{CE} = 0 V. This point is called the *saturation point*. In this point, the collector current (I_C) is maximum and the collector-to-emitter voltage (V_{CE}) is about zero. Similarly, the intersect point on horizontal axis is V_{CE} = 10 V, I_C = 0 mA. This point is called the *cut-off point*.

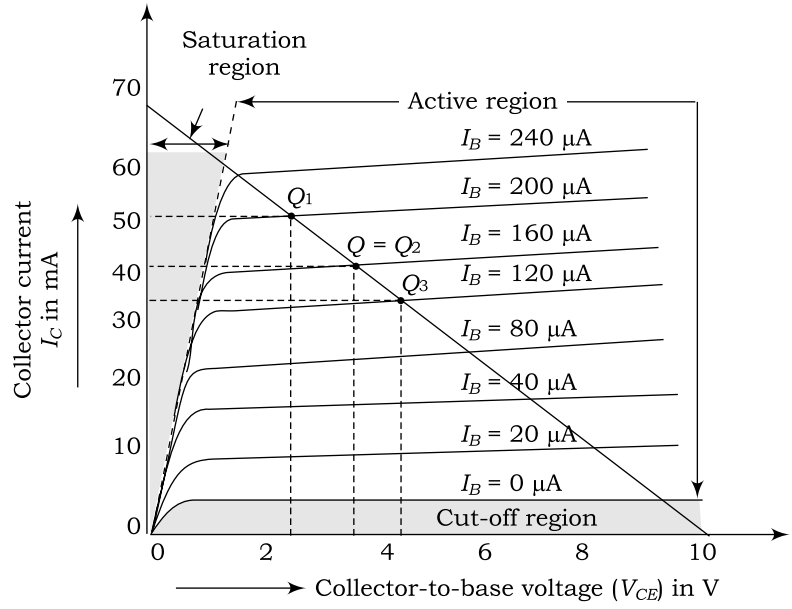


Fig. 2.16(b) Q points on the output characteristics of a common-emitter transistor

When the V_{CC}, the collector resistance R_C, and V_{CE} are known, the collector current can determined from

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \tag{2.10}$$

where, V_{CC} is the supply voltage, V_{CE} is the voltage across the collector to emitter of a transistor and R_C is the collector resistance.

When the value of the collector-to-emitter voltage (V_{CE}) is very small at saturation point, then the collector current is equal to

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \tag{2.11}$$

where, $I_{C_{sat}}$ is the maximum current and it is indicated by the upper end of the load line.

At cut-off point, the collector current is equal to zero, then Eq. (2.10) can be written as

$$0 = \frac{V_{CC} - V_{CE}}{R_C}$$

or
$$V_{CE} = V_{CC} \tag{2.12}$$

The value of the collector-to-emitter voltage at cut-off point is represented by $V_{CE(\text{cut-off})}$ and this provides the lower end of the load line. The region in between the saturation and cut-off points of the load line is called active region. The *Q*-point of the transistor will be in the midway of the saturation point and cut-off point as indicated in Fig. 2.17.

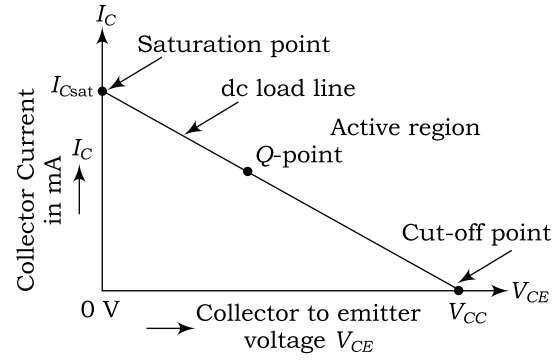


Fig. 2.17 The simplified representation of a dc load line

2.12 *Q*-POINT AND OUTPUT OF BIPOLAR JUNCTION TRANSISTOR

The output signal of a transistor amplifier circuit depends on the *Q*-point in output characteristics. When the *Q*-point is located at the centre of the load line, the transistor amplifier circuit operates in linear zone and the undistorted signal will be output from the amplifier. Figure 2.18 shows that the transistor circuit is used as an amplifier.

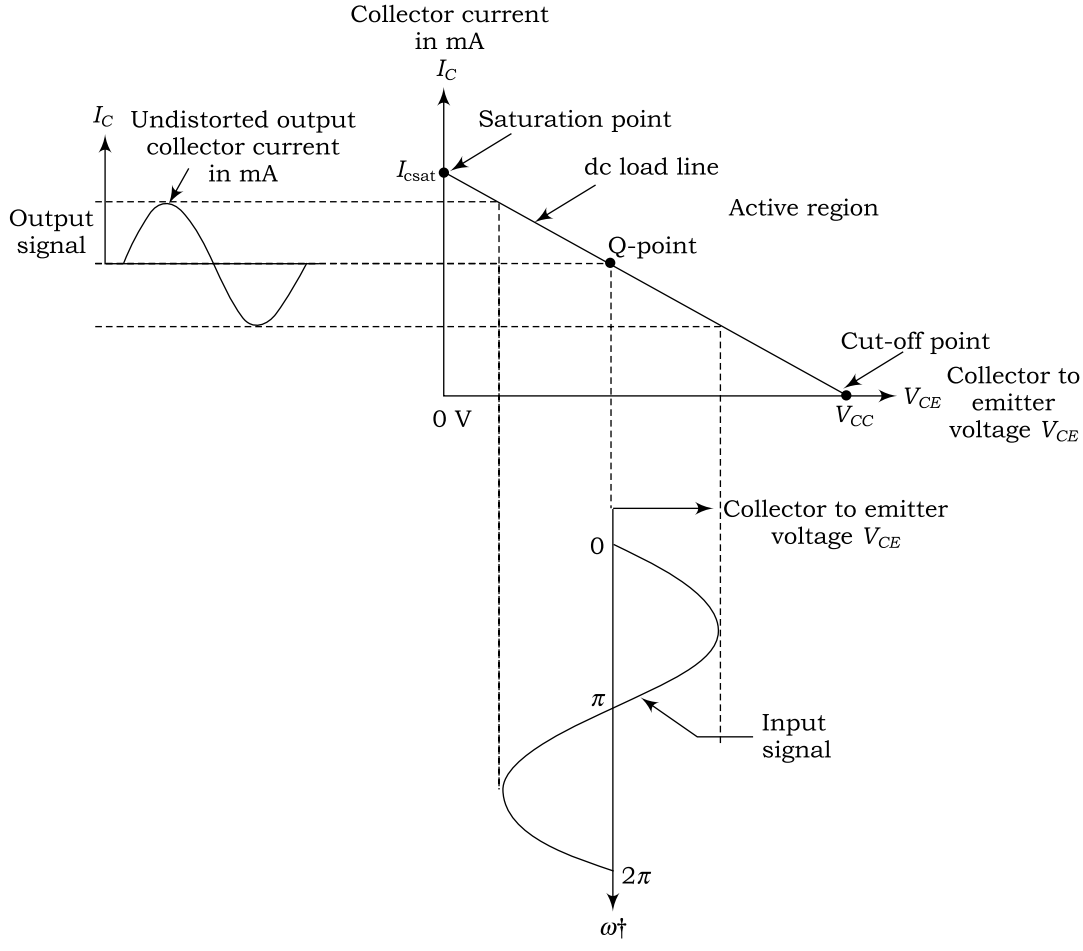


Fig. 2.18 Transistor circuit is used as an amplifier with undistorted output

When the *Q*-point is located near the saturation point, one peak of the output signal will be clipped. During the negative half-cycle of the input signal, the transistor is driven into saturation. Therefore, the negative peak of the input signal is clipped at the output signal as depicted in Fig. 2.19.

When the *Q*-point is located near the cut-off point, the transistor operates in cut-off region. Therefore, the positive peak of the input signal is clipped at the output as shown in Fig. 2.20.

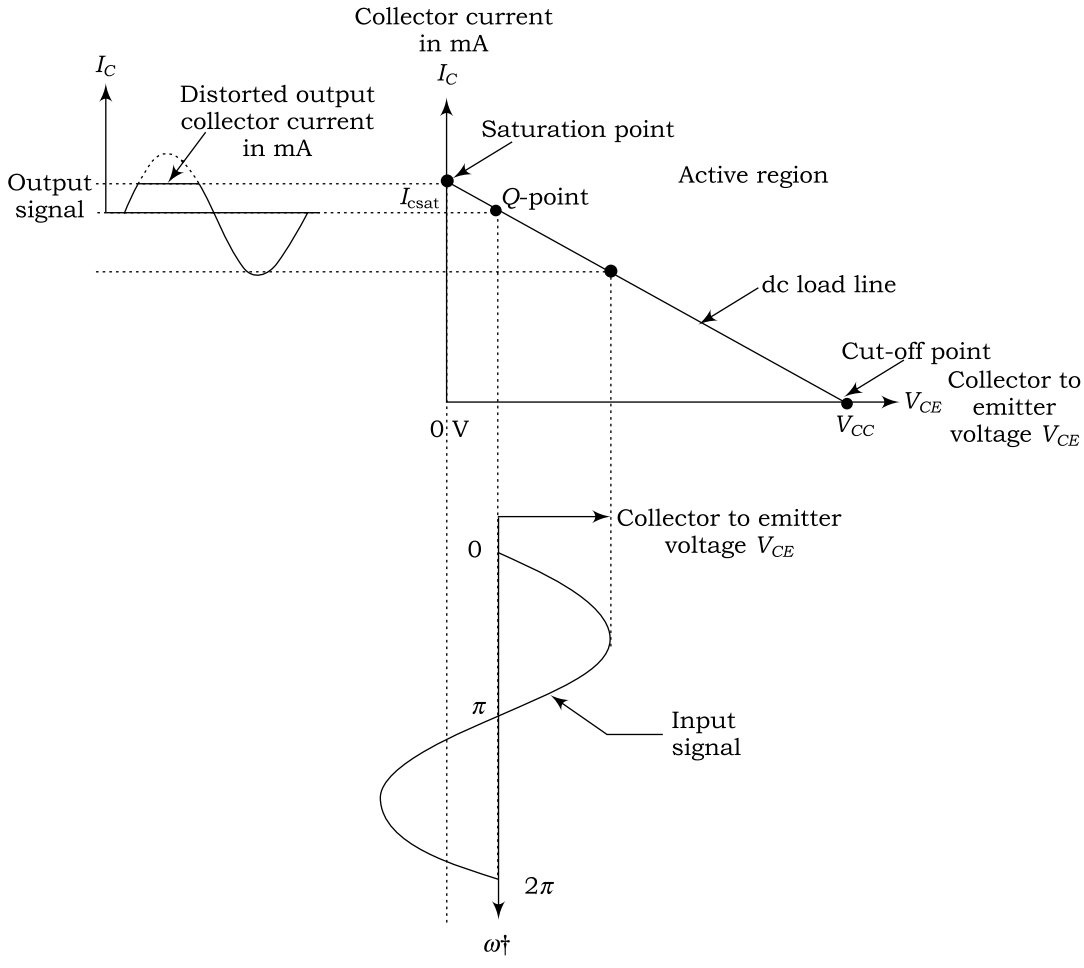


Fig. 2.19 Transistor circuit is used as an amplifier with distorted output when the negative peak of the input signal is clipped

2.13 STABILITY FACTOR

The stability factor is the rate of change of collector current with respect to the reverse saturation current when the collector-emitter current gain (β) and base current is constant. The stability factor can be expressed as

$$S = \frac{dI_C}{dI_{C0}} \tag{2.112}$$

The stability factor can be used to measure the bias stability of a transistor circuit. When a transistor circuit has a high stability factor, the circuit has poor stability. However, the low value of stability factor represents the very good stability of a circuit.

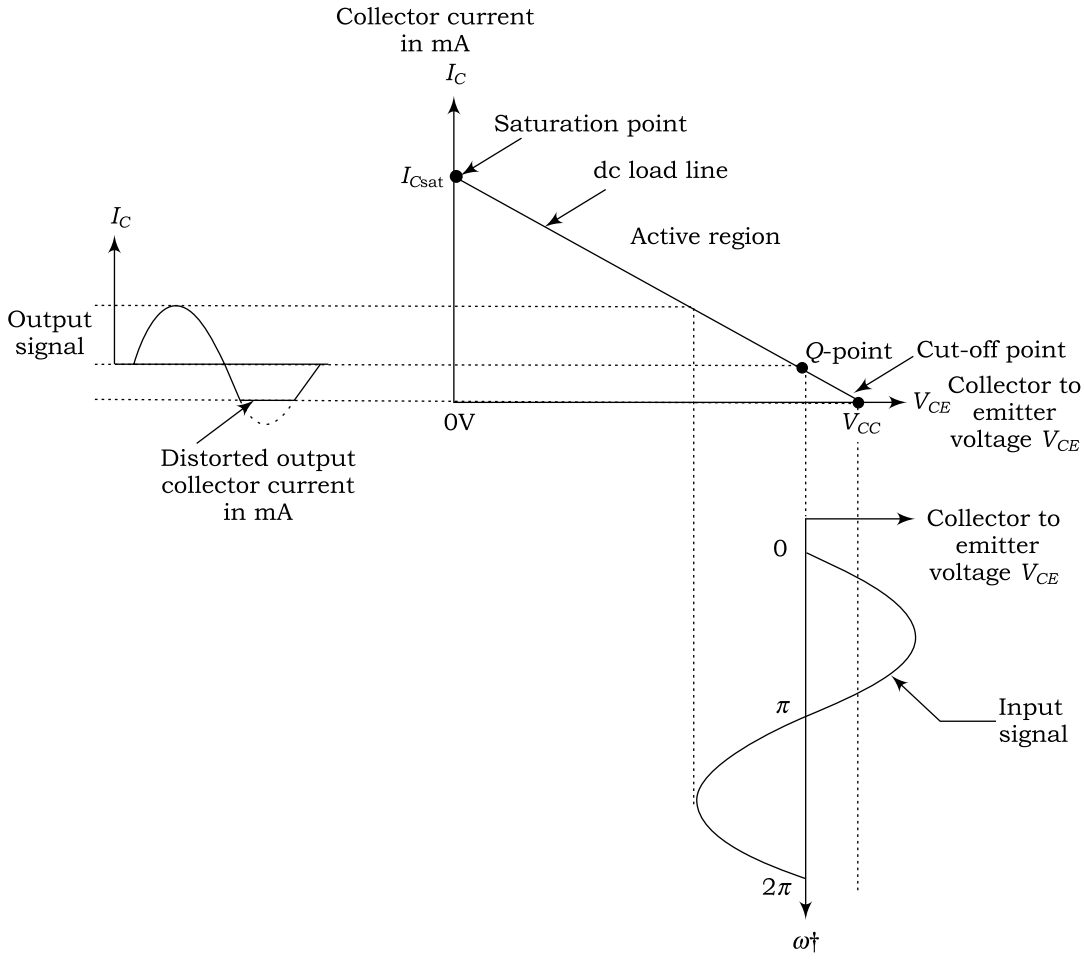


Fig. 2.20 Transistor circuit is used as an amplifier with distorted output when the positive peak of the input signal is clipped

If the rate of change of collector current (dI_C) is equal to the rate of change of reverse saturation current (dI_{C0}), the stability factor is about unity. As there is very small change in collector current with temperature, there will be very small variation in the Q point.

The stability factor (S) can be expressed as a function of the base current (I_B), collector current (I_C) and reverse saturation current (I_{C0}). The value of collector current (I_C) in transistor is equal to

$$I_C = \beta I_B + (1+\beta) I_{C0} \tag{2.13}$$

After differentiating the above equation with respect to I_C, we obtain

$$1 = \frac{d(\beta I_B)}{dI_C} + \frac{d\{(1+\beta) I_{C0}\}}{dI_C}$$

or $$1 = \beta \frac{dI_B}{dI_C} + (1+\beta)\frac{dI_{C0}}{dI_C} \quad \text{as } \beta \text{ is constant}$$

or $$1 = \beta \frac{dI_B}{dI_C} + (1+\beta)\frac{1}{S} \qquad \text{as } S = \frac{dI_C}{dI_{C0}}$$

Therefore, the stability factor is given by

$$S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)} \tag{2.14}$$

The above equation is used to determine the stability factor (S) of any transistor biasing circuit. Initially, find the relationship between the base current (I_B) and collector current (I_C) and then derive the stability factor using the above equation.

For example, the collector current of common-base (*CB*) transistor circuit is given by

$$I_C = \alpha I_E + I_{C0}$$

After differentiating the above equation with respect to I_{C0}, we get

$$\frac{dI_C}{dI_{C0}} = \frac{d(\alpha I_E)}{dI_{C0}} + 1 = 0 + 1 = 1 \qquad \text{as } \frac{d(\alpha I_E)}{dI_{C0}} = 1 \tag{2.15}$$

Therefore, the stability factor $S = 1$. The *common-base circuit is highly stable* and there is no requirement of bias stabilisation in this circuit.

In case of common-emitter (*CE*) circuit, the collector current of the common emitter transistor circuit is given by

$$I_C = \beta I_B + (1+\beta) I_{C0}$$

After differentiating the above equation with respect to I_{C0}, we get

$$\frac{dI_C}{dI_{C0}} = \frac{d(\beta I_B)}{dI_{C0}} + (1+\beta) = 0 + (1+\beta) = 1 + \beta \qquad \text{when} \quad \frac{d(\beta I_B)}{dI_{C0}} = 0 \tag{2.16}$$

Therefore, the stability factor is $S = 1 + \beta$.

If $\beta = 50$, the stability factor is equal to $S = 1 + \beta = 1 + 50 = 51$. Hence, the change in collector current is 51 times the change in reverse saturation current. Since the collector current depends on the reverse saturation current and the collector current changes with temperature as I_{C0} depends upon temperature. Therefore, there is a requirement of bias stabilisation in common emitter circuit to improve the stability.

The collector current not only depends on the reverse saturation current (I_{C0}) but also depends on the current gain (β) and the base emitter voltage (V_{BE}). Therefore, the stability factors are function of $I_{C0,}$ β and V_{BE} and can be expressed as

$$S = \frac{\Delta I_C}{\Delta I_{C0}},\ S' = \frac{\Delta I_C}{\Delta V_{BE}} \quad \text{and} \quad S'' = \frac{\Delta I_C}{\Delta \beta}$$

The stability factor S is the rate of change of the collector current with respect to the reverse saturation current (I_{C0}) when the base emitter voltage (V_{BE}) and the common emitter current gain (β) are constant and it can be expressed as

$$S = \frac{\Delta I_C}{\Delta I_{C0}} \tag{2.17}$$

The stability factor S' is the rate of change of the collector current with respect to the base emitter voltage (V_{BE}) when the common-emitter current gain (β) and the reverse saturation current (I_{C0}) are constant and it is given by

$$S' = \frac{\Delta I_C}{\Delta V_{BE}} \tag{2.18}$$

Similarly, the stability factor S'' is the rate of change of the collector current with respect to the current gain when the base-emitter voltage (V_{BE}) and the reverse saturation current are constant (I_{C0}) and it can be expressed as

$$S'' = \frac{\Delta I_C}{\Delta \beta} \tag{2.19}$$

The total change in collector current is the sum of the individual changes due to the above three stability factors. As $I_C = I(I_{C0}, V_{BE}, \beta)$, the total differentiation of I_C is equal to

$$\Delta I_C = \frac{\partial I_C}{\partial I_{C0}} \Delta I_{C0} + \frac{\partial I_C}{\partial V_{BE}} \Delta V_{BE} + \frac{\partial I_C}{\partial \beta} \Delta \beta$$

or

$$\Delta I_C = S \times \Delta I_{C0} + S' \times \Delta V_{BE} + S'' \times \Delta \beta \tag{2.20}$$

2.14 TRANSISTOR BIASING

For any transistor amplifier circuit, the transistor must be biased properly and it has the following conditions:

- The base-emitter junction must be forward biased. V_{BE} = 0.7 V for silicon transistor and V_{BE} = 0.3 V for germanium transistor.
- The collector emitter junction must be reverse biased. V_{CE} = 1 V for silicon transistor and V_{CE} = 0.5 V for germanium transistor.

Generally, transistors are biased by two voltage sources, V_{BB} and V_{CC}. The V_{BB} is applied across the base-emitter junction (J_E) whereas the V_{CC} is used for biasing the collector-base junction (J_C). Usually, only one power supply is used for biasing the base-emitter junction (J_E) as well as collector-emitter junction (J_C). The following biasing arrangements are most commonly used in transistor circuits.

1. Fixed bias
2. Fixed bias with emitter feedback
3. Fixed bias with collector feedback
4. Voltage divider or self-bias
5. Emitter bias

2.15 FIXED BIAS

Figure 2.21 shows a *fixed bias* for a transistor. This biasing circuit is also called *base bias*. In this circuit, two power supplies, V_{BB} and V_{CC} are used. Figure 2.22 shows a fixed bias of a transistor using single power supply V_{CC}.

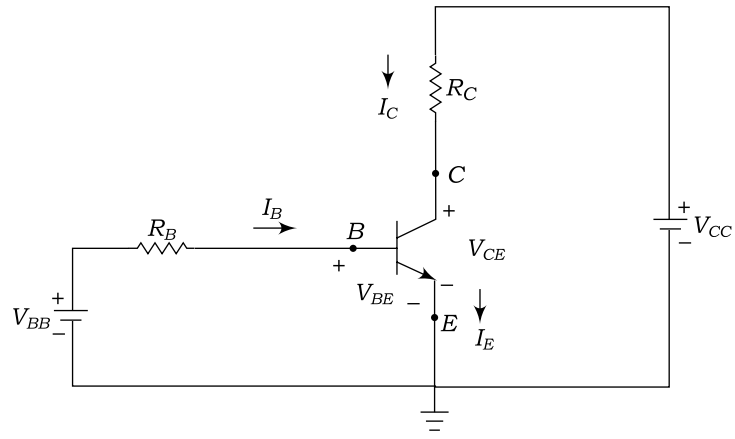


Fig. 2.21 Fixed-bias circuit of a transistor with two power supplies

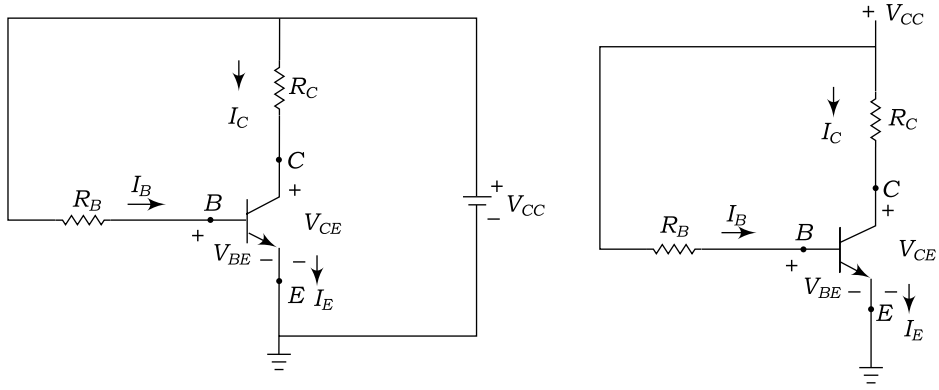


Fig. 2.22 Fixed-bias circuit of a transistor with one power supply

The current flow through the base is I_B and the voltage drop across the base emitter junction is V_{BE}. Applying the Kirchhoff's Voltage Law (KVL) in base-emitter circuit, we get

$$I_B R_B + V_{BE} = V_{CC}$$

or

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

As V_{CC} and V_{BE} are constant, the base current depends on the base resistance R_B. Since V_{CC}>>V_{BE}, the base current is equal to

$$I_B = \frac{V_{CC}}{R_B} \tag{2.21}$$

Applying the Kirchhoff's Voltage Law (KVL) in collector-emitter circuit, we obtain

$$I_C R_C + V_{CE} = V_{CC} \tag{2.22}$$

Therefore, the voltage drop across the collector-emitter junction is equal to

$$V_{CE} = V_{CC} - I_C R_C \tag{2.23}$$

The collector current is given by

$$I_C = \beta I_B = \beta \frac{V_{CC}}{R_B} \tag{2.24}$$

The collector current (I_C) and collector-to-emitter voltage are function of β. The value of β depends on the temperature (T). Consequently, the collector current (I_C) and collector-to-emitter voltage (V_{CE}) of a fixed-bias circuit can change with variation of β due to change in temperature (T). Hence, the operating Q-point of a transistor changes with temperature. Therefore, it is not possible to obtain a stable Q-point in a fixed-bias circuit. As a result, the fixed-bias circuit is never used as an amplifier, but this transistor circuit is most commonly used as a switch where the transistor operates in between saturation and cut-off regions.

In case of fixed-bias circuit, the collector current of common emitter transistor circuit is given by

$$I_C = \beta I_B + (1 + \beta) I_{C0}$$

After differentiating the above equation with respect to I_{C0}, we get

$$\frac{dI_C}{dI_{C0}} = \frac{d(\beta I_B)}{dI_{C0}} + (1 + \beta) = 0 + (1 + \beta) = 1 + \beta \quad \text{as} \quad \frac{d(\beta I_B)}{dI_{C0}} = 0 \tag{2.25}$$

Therefore, the stability factor is equal to $S = 1 + \beta$.

2.15.1 Fixed Bias with Emitter Feedback

Figure 2.23 shows the fixed bias with emitter feedback with two power supplies. The fixed bias with emitter feedback circuit of a transistor with one power supply is illustrated in Fig. 2.24. In this circuit, an emitter resistance R_E is connected in between emitter and ground. The resistance R_E provides the better stability compared to fixed-bias circuit.

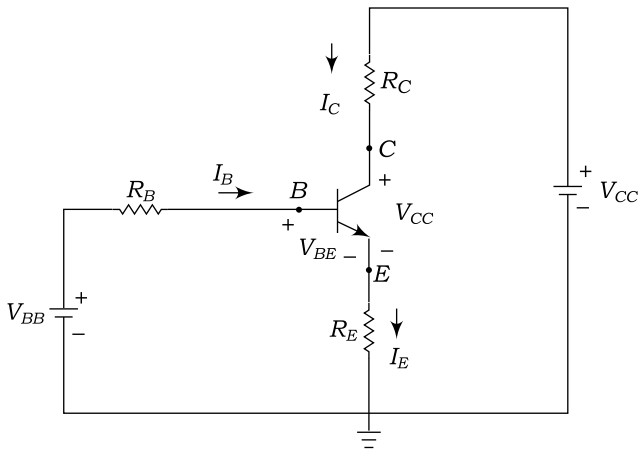


Fig. 2.23 Fixed bias with emitter feedback circuit of a transistor with two power supplies

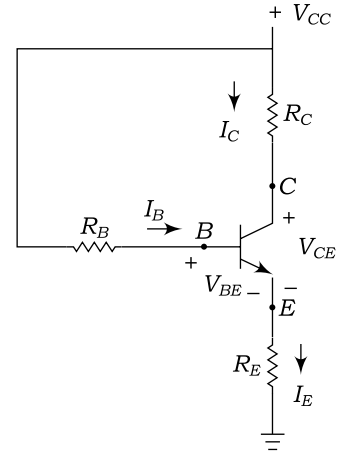


Fig. 2.24 Fixed bias with emitter feedback circuit of a transistor with a power supply

Applying Kirchhoff's Voltage Law (KVL) in base-emitter circuit, we obtain

$$I_B R_B + V_{BE} + I_E R_E = V_{CC}$$

After substituting the value of I_E in the above equation, we get

$$I_B R_B + V_{BE} + (1+\beta) I_B R_E = V_{CC} \quad \text{as } I_E = (1+\beta) I_B$$

or

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \tag{2.26}$$

The collector current is

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

or

$$I_C = \frac{V_{CC} - V_{BE}}{(R_B/\beta) + \left(1 + \frac{1}{\beta}\right) R_E} = \frac{V_{CC} - V_{BE}}{(R_B/\beta) + R_E} \text{ as } 1 >> \frac{1}{\beta} \tag{2.27}$$

It is clear from the above equation that when the emitter resistance (R_E) is large compared to R_B/β, the bias circuit is independent of β. Actually, in practical circuits, it is impossible to make the emitter resistance very large to compensate the effect of current gain.

Applying Kirchhoff's Voltage Law (KVL) in the collector-emitter circuit, we obtain

$$I_C R_C + V_{CE} + I_E R_E = V_{CC}$$

If $I_E = I_C$, we can write,

$$I_C R_C + V_{CE} + I_C R_E = V_{CC}$$

Therefore, the voltage drop across the collector-emitter junction is equal to

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \tag{2.28}$$

The voltage across the resistance R_E is given by

$$V_E = I_E R_E = I_C R_E \qquad \text{assuming } I_E = I_C \tag{2.29}$$

The voltage across the collector to ground is

$$V_C = V_{CC} - I_C R_C \tag{2.30}$$

The KVL equation in base-emitter loop is

$$I_B R_B + V_{BE} + I_E R_E = V_{CC}$$

After substituting the emitter current $I_E = I_C + I_B$ in the above equation, we obtain

$$I_B R_B + V_{BE} + (I_C + I_B) R_E = V_{CC} \tag{2.31}$$

The base current is equal to

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_E + R_B}$$

After differentiating the above equation with respect to I_C, we get

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B} \tag{2.32}$$

We know that the general expression of stability factor is

$$S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$$

After substituting the value of $\frac{dI_B}{dI_C}$ in the above equation, we obtain

$$S = \frac{1+\beta}{1-\beta\left(-\frac{R_E}{R_E+R_B}\right)} = \frac{1+\beta}{1+\beta\frac{R_E}{R_E+R_B}} \tag{2.33}$$

2.15.2 Fixed Bias with Collector Feedback

Figure 2.25 shows the fixed bias with collector feedback where the base resistance R_B is connected in between the base and collector terminals of a transistor. The collector voltage provides the biasing of base emitter junction. In this circuit, the resistance R_B is used as a feedback resistance and provides a stable Q-point.

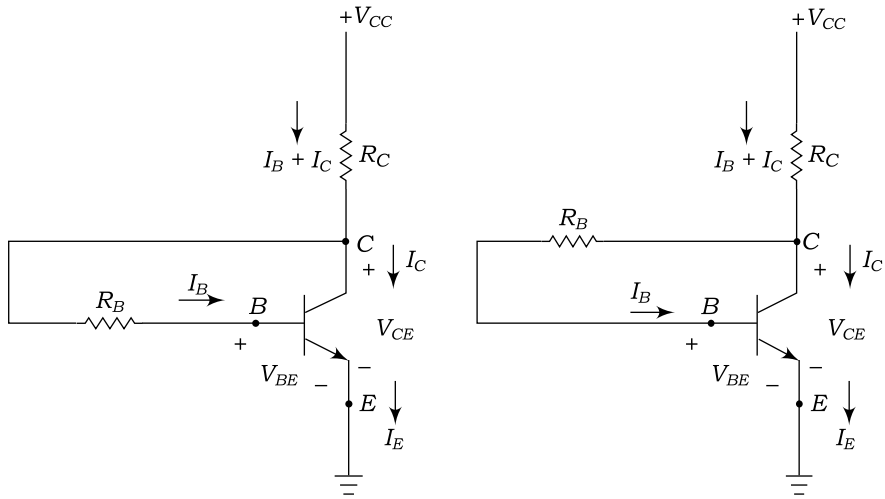


Fig. 2.25 Fixed bias with collector feedback circuit of a transistor

Applying Kirchhoff's Voltage Law (KVL) in the base-emitter circuit, we obtain

$$(I_C + I_B)R_C + I_B R_B + V_{BE} = V_{CC} \tag{2.34}$$

After substituting the value of I_C in the above equation, we get

$$(\beta I_B + I_B)R_C + I_B R_B + V_{BE} = V_{CC} \quad \text{as } I_C = \beta I_B$$

or

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_C} \tag{2.35}$$

The collector current is

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_C}$$

or

$$I_C = \frac{V_{CC} - V_{BE}}{(R_B/\beta) + \left(1 + \frac{1}{\beta}\right)R_C} = \frac{V_{CC} - V_{BE}}{(R_B/\beta) + R_C} \quad \text{as } 1 >> \frac{1}{\beta} \tag{2.36}$$

It is clear from the above equation that when the collector resistance (R_C) is large compared to R_B/β, the bias circuit is independent of β. Actually, in practical circuits, it is impossible to make the collector resistance very large to compensate the effect of current gain.

Applying Kirchhoff's Voltage Law (KVL) in the collector-emitter circuit, we obtain

$$(I_C + I_B)R_C + V_{CE} = V_{CC} \tag{2.37}$$

Therefore, the voltage drop across the collector-emitter junction is equal to

$$V_{CE} = V_{CC} - (I_C + I_B)R_C \tag{2.38}$$

Applying KVL in base-emitter circuit, we can write

$$(I_C + I_B)R_C + I_B R_B + V_{BE} = V_{CC} \tag{2.39}$$

The base current is equal to

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \tag{2.40}$$

After differentiating the above equation with respect to I_C, we get

$$\frac{dI_B}{dI_C} = -\frac{R_C}{R_C + R_B}$$

We know that the general expression of *stability factor* is

$$S = \frac{1 + \beta}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

After substituting the value of $\frac{dI_B}{dI_C}$ in the above equation, we obtain

$$S = \frac{1 + \beta}{1 - \beta\left(-\frac{R_C}{R_C + R_B}\right)} = \frac{1 + \beta}{1 + \beta\frac{R_C}{R_C + R_B}} \tag{2.41}$$

It is clear from the above equation that the *stability factor* of the collector feedback circuit is less than $(1 + \beta)$. Hence, the collector feedback circuit has better stability compared to fixed-bias circuit.

2.16 VOLTAGE DIVIDER OR SELF-BIAS

The value of bias current and the voltage across the collector emitter junction depends on the current gain β. Actually, the value of β varies with temperature. As the value of β is not well defined, it is required to provide a dc biasing circuit which is independent of the current gain β. Figure 2.26 shows the *voltage divider biasing* circuit. This circuit is also called *self-bias* circuit.

The resistances R_1 and R_2 are used as voltage dividers across the power supply V_{CC}. The voltage drop across the resistance R_2 is used for the forward biasing of base-emitter junction of a transistor. The emitter resistance can be used to improve stability of the circuit.

The voltage at the base terminal of the transistor is

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} \tag{2.42}$$

When the base-emitter junction is forward biased, the voltage V_{BE} is very small. Therefore, the voltage V_B is equal to the voltage across the resistance R_E.

Hence, $V_B = V_E = I_E R_E$

Then emitter current is given by

$$I_E = \frac{V_E}{R_E} \tag{2.43}$$

The value of the collector current is

$$I_C = I_E \tag{2.44}$$

The voltage drop across the resistance R_C is

$$V_{R_C} = I_C R_C \tag{2.45}$$

The voltage drop across the collector-emitter is given by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = V_{CC} - I_E (R_C + R_E) \tag{2.46}$$

$$V_{R_C} = I_C R_C \tag{2.47}$$

The voltage at the collector terminal is

$$V_C = V_{CC} - I_C R_C$$

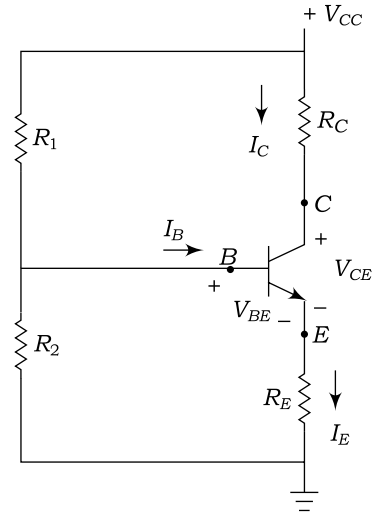


Fig. 2.26 Voltage divider or self-bias circuit

The equivalent circuit of voltage divider is shown in Fig. 2.27 where V_{th} is the Thevenin's voltage and R_{th} is Thevenin's resistance. The values of V_{th} and R_{th} are given below:

$$V_{th} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{2.48}$$

$$R_{th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{2.49}$$

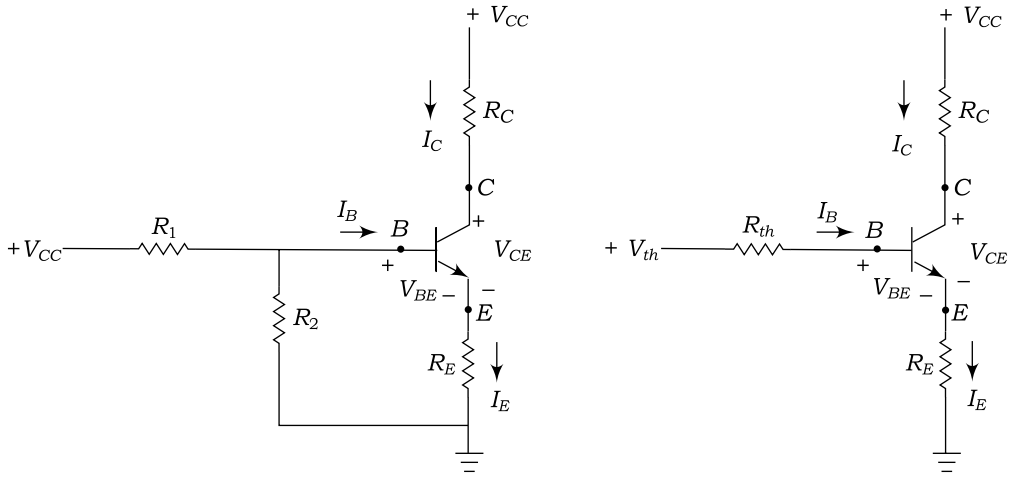


Fig. 2.27 (a) Voltage divider or self-bias circuit (b) Thevenin's equivalent circuit

Applying KVL in the base-emitter circuit, we can write

$$I_B R_{\text{th}} + V_{BE} + I_E R_E = V_{\text{th}} \tag{2.50}$$

As $I_B = \frac{I_E}{\beta}$, the emitter current is equal to

$$I_E = \frac{V_{\text{th}} - V_{BE}}{R_E + \frac{R_{\text{th}}}{\beta}} = \frac{V_{\text{th}} - V_{BE}}{R_E} \quad \text{as } R_E >> \frac{R_{\text{th}}}{\beta} \tag{2.51}$$

It is clear from the above equation that the emitter current is independent of β. It is only possible when the emitter resistance is more than ten times of $\frac{R_{\text{th}}}{\beta}$. If the value of R_2 is very small compared to R_1, R_{th} is equal to R_2.

Therefore, $R_E \geq 10\frac{R_{\text{th}}}{\beta}$

or $$R_E \geq 10\frac{R_2}{\beta}$$

or $$0.1\beta R_E \geq R_2 \tag{2.52}$$

Applying KVL in the base-emitter circuit, we can write

$$I_B R_{\text{th}} + V_{BE} + I_E R_E = V_{\text{th}}$$

As $I_E = I_B + I_C$, the above equation can be written as

$$I_B R_{\text{th}} + V_{BE} + (I_B + I_C) R_E = V_{\text{th}} \tag{2.53}$$

The base current is equal to

$$I_B = \frac{V_{\text{th}} - V_{BE} - I_C R_E}{R_{\text{th}} + R_E}$$

After differentiating the above equation with respect to I_C, we get

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_{\text{th}} + R_E} \tag{2.54}$$

We know that the general expression of *stability factor* is

$$S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$$

After substituting the value of $\frac{dI_B}{dI_C}$ in the above equation, we obtain

$$S = \frac{1+\beta}{1-\beta\left(-\frac{R_E}{R_{th}+R_E}\right)} = \frac{1+\beta}{1+\beta\frac{R_E}{R_{th}+R_E}} \tag{2.55}$$

After substituting the value of $R_{th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$ in the above equation, we get

$$S = \frac{R_E(R_1+R_2)+R_1R_2}{R_E(R_1+R_2)+R_1R_2(1-\alpha)} \tag{2.56}$$

It is clear from the above equation that the stability factor of voltage-divider biasing circuit is less than (1 + β). Hence, the voltage-divider biasing circuit has better stability compared to fixed-bias circuit.

2.17 EMITTER BIAS

Figure 2.28 shows the emitter-bias circuit. In this circuit, the V_{CC} and $-V_{EE}$ are applied to the collector and emitter terminals. The base resistance R_B is very small as the base voltage V_B is about zero. The base emitter junction is forward biased by $-V_{EE}$ voltage and the voltage at the emitter terminal is equal to

$$V_E = -V_{BE}$$

The emitter current is

$$I_E = \frac{V_E - V_{EE}}{R_E} = \frac{-V_{BE} - V_{EE}}{R_E}$$

As V_{EE} is negative, the emitter current is

$$I_E = \frac{-V_{BE} + V_{EE}}{R_E} \tag{2.57}$$

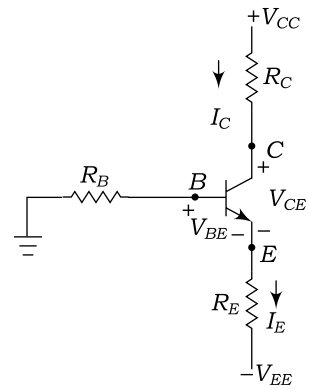


Fig. 2.28 Emitter-bias circuit

The collector current is equal to the emitter current and $I_E = I_C$

The voltage at the collector terminal is

$$V_C = V_{CC} - I_C R_C \tag{2.58}$$

The collector-to-emitter voltage is

$$V_{CE} = V_C - V_E \tag{2.59}$$

Applying KVL in the base-emitter circuit, we can write

$$I_B R_B + V_{BE} + I_E R_E = V_{EE}$$

After substituting $I_B = \frac{I_E}{\beta}$ in the above equation, we get

$$I_E\left(\frac{R_B}{\beta} + R_E\right) + V_{BE} = V_{EE}$$

Then the emitter current is equal to

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta}} = \frac{V_{EE} - V_{BE}}{R_E} \qquad \text{as } R_E >> \frac{R_B}{\beta} \tag{2.60}$$

It is clear from the above equation that the emitter current I_E is independent of β and base-to-emitter voltage. It is only possible when the emitter resistance is more than 100 times of $\frac{R_B}{\beta}$.

Therefore, $R_E \geq 100\frac{R_B}{\beta}$

or $$0.01\beta R_E \geq R_2$$

As I_E is independent of β and V_{BE}, the Q-point does not get affected by these parameter variations significantly. Hence the emitter bias can provide a reasonably stable *Q*-point.

Applying the KVL in base-emitter circuit, we can write

$$I_B R_B + V_{BE} + I_E R_E = V_{EE}$$

As $I_E = I_B + I_C$, the above equation can be written as

$$I_B R_B + V_{BE} + (I_B + I_C) R_E = V_{EE}$$

The base current is equal to

$$I_B = \frac{V_{EE} - V_{BE} - I_C R_E}{R_B + R_E} \tag{2.61}$$

After differentiating the above equation with respect to I_C, we get

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_B + R_E}$$

We know that the general expression of *stability factor* is

$$S = \frac{1 + \beta}{1 - \beta\left(\frac{dI_B}{dI_C}\right)} \tag{2.62}$$

After substituting the value of $\frac{dI_B}{dI_C}$ in the above equation, we obtain

$$S = \frac{1+\beta}{1-\beta\left(-\frac{R_E}{R_B+R_E}\right)} = \frac{1+\beta}{1+\beta\frac{R_E}{R_B+R_E}} \tag{2.63}$$

Example 2.8 Figure 2.29 shows a transistor amplifier circuit. Determine the value of saturation current and the collector-emitter cut-off voltage. Draw the dc load line.

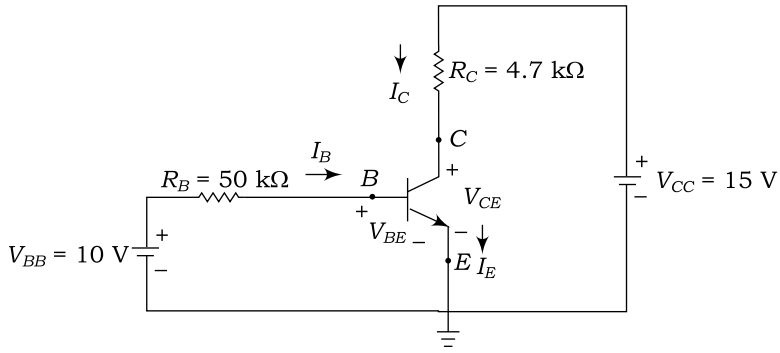


Fig. 2.29

Sol. Given: $V_{BB} = 10$ V, $V_{CC} = 15$ V, $R_B = 50$ kΩ, $R_C = 4.7$ kΩ

The value of saturation current is

$$I_{C(\text{Sat})} = \frac{V_{CC}}{R_C} = \frac{15}{4.7\times10^3} = 3.1914 \text{ mA}$$

The collector-to-emitter cut-off voltage is

$$V_{CE(\text{Cut-off})} = V_{CC} = 15V$$

The lower end of dc load line is (15 V, 0) and the upper end of dc load line is (0, 3.19 mA). By using the two points (15 V, 0) and (0, 3.19 mA), the dc load line is drawn as shown in Fig. 2.30.

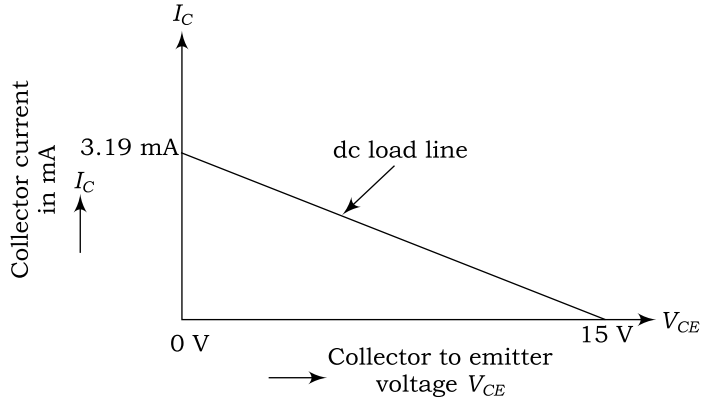


Fig. 2.30 dc load line

Example 2.9 A transistor amplifier circuit is shown in Fig. 2.31. Draw the dc load line and locate the Q-point on the dc load line. Assume $V_{BE} = 0.7$ V and $\beta = 50$.

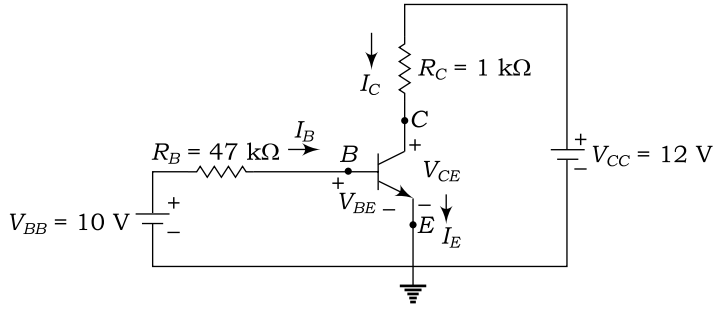


Fig. 2.31

Sol. Given: $V_{BB} = 10$ V, $V_{CC} = 12$ V, $R_B = 47$ kΩ, $R_C = 1$ kΩ, $V_{BE} = 0.7$ V and $\beta = 50$

The value of saturation current is

$$I_{C(\text{Sat})} = \frac{V_{CC}}{R_C} = \frac{12}{1 \times 10^3} = 12 \text{ mA}$$

The collector-to-emitter cut-off voltage is

$$V_{CE(\text{Cut-off})} = V_{CC} = 12 \text{ V}$$

The lower end of dc load line is (12 V, 0) and the upper end of dc load line is (0, 12 mA). By using the two points (12 V, 0) and (0, 12 mA), the dc load line is drawn as shown in Fig. 2.32.

Applying the Kirchhoff's voltage law in the base emitter circuit, we get

$$V_{BB} = I_B R_B + V_{BE}$$

or $$10 = I_B \times 47 \times 10^3 + 0.7$$

Then the base current is

$$I_B = \frac{10 - 0.7}{47 \times 10^3} = 0.1978 \text{ mA}$$

The collector current is

$$I_C = \beta I_B = 50 \times 0.1978 = 9.89 \text{ mA}$$

The collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 12 - 9.89 \times 10^{-3} \times 1 \times 10^3 = 2.11 \text{V}$$

Then Q point (2.11V, 9.89 mA) is located on the dc load line as depicted in Fig. 2.32.

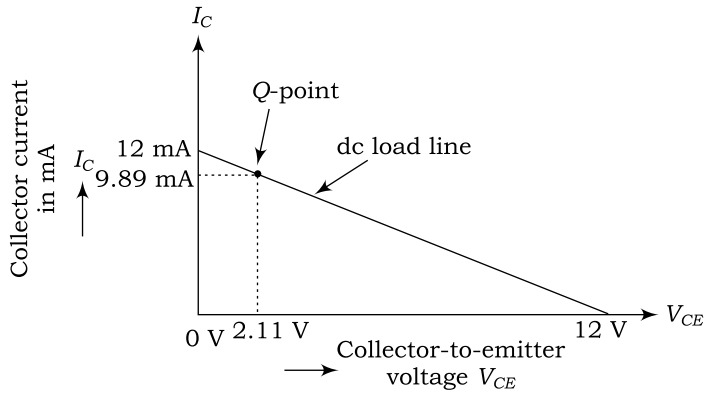


Fig. 2.32 dc load line and Q-point

Example 2.10 Figure 2.33 shows a biasing circuit of an *NPN* transistor amplifier circuit. Calculate the base current, collector current, emitter current and collector-to-emitter voltage. Assume V_{BE} = 0.7 V and $\beta = 50$.

Sol. Given: $V_{CC} = 20$ V, $R_B = 100$ kΩ, $R_C = 1.2$ kΩ,
$V_{BE} = 0.7$ V and $\beta = 50$

Applying the Kirchhoff's voltage law in the base-emitter circuit, we obtain

$$V_{CC} = I_B R_B + V_{BE}$$

or $$20 = I_B \times 100 \times 10^3 + 0.7$$

Then the base current is

$$I_B = \frac{20 - 0.7}{100 \times 10^3} = 0.193 \text{ mA}$$

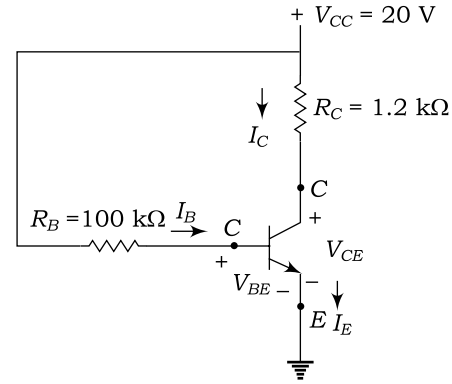


Fig. 2.33

The collector current is

$$I_C = \beta I_B = 50 \times 0.193 = 9.65 \text{ mA}$$

The emitter current is

$$I_E = I_C + I_B = 9.65 \text{ mA} + 0.193 \text{ mA} = 9.843 \text{ mA}$$

The collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 20 - 9.65 \times 10^{-3} \times 1.2 \times 10^3 = 8.42 \text{ V}$$

Example 2.11 Determine the biasing resistance R_B of a biasing circuit of an *NPN* transistor as depicted in Fig. 2.34 when the base current is 0.2 mA. Calculate the collector current, collector-to-emitter voltage and stability factor. Assume $V_{BE} = 0.7$ V and $\beta = 90$.

Sol. Given: $V_{CC} = 15$ V, $I_B = 0.2$ mA, $R_C = 800$ Ω, $V_{BE} = 0.7$ V and $\beta = 90$

Applying the Kirchhoff's voltage law in the base-emitter circuit, we obtain

$$V_{CC} = I_B R_B + V_{BE}$$

or $15 = 0.2 \times 10^{-3} \times R_B + 0.7$

Then the base resistance is

$$R_B = \frac{15 - 0.7}{0.2 \times 10^{-3}} = 71.5 \text{ k}\Omega$$

The collector current is

$$I_C = \beta I_B = 90 \times 0.2 \text{ mA} = 18 \text{ mA}$$

The collector to emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 15 - 18 \times 10^{-3} \times 800 = 0.6 \text{ V}$$

Figure 2.102 is the fixed-bias circuit, the stability factor is

$$S = 1 + \beta = 1 + 90 = 91$$

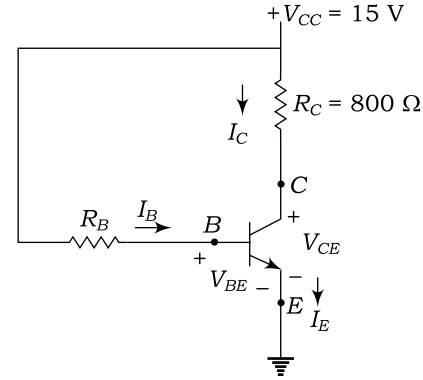


Fig. 2.34

Example 2.12 Determine the base current, collector current and collector-to-emitter voltage of a biasing circuit as shown in Fig. 2.35. Assume $V_{BE} = 0.7$ V and $\beta = 100$.

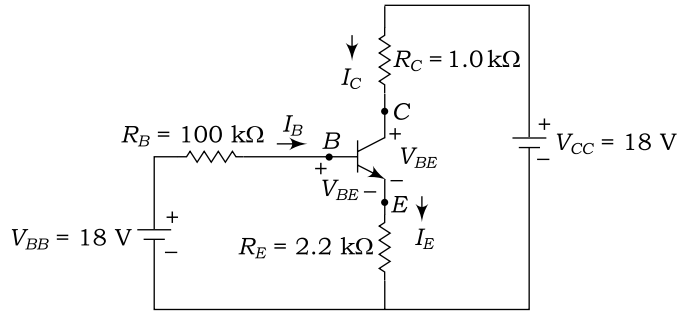


Fig. 2.35

Sol. Given: $V_{BB} = 18$ V, $V_{CC} = 18$ V, $R_B = 100$ kΩ, $R_C = 1.0$ kΩ, $V_{BE} = 0.7$ V and $\beta = 100$

Applying the Kirchhoff's voltage law in the base-emitter circuit, we obtain

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

Since $I_E = (1 + \beta) I_B$, $I_E = (1 + 100) I_B$ as $\beta = 100$

or $18 = I_B \times 100 \times 10^3 + 0.7 + (1 + 100) I_B \times 2.2 \times 10^3$

Then the base current is

$$I_B = \frac{18 - 0.7}{100 \times 10^3 + 101 \times 2.2 \times 10^3} = 0.05369 \text{ mA}$$

The collector current is

$$I_C = \beta I_B = 100 \times 0.0536 \text{ mA} = 5.369 \text{ mA}$$

The emitter current is

$$I_B = I_C + I_B = 5.369 \text{ mA} + 0.05369 \text{ mA} = 5.423 \text{ mA}$$

The collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$
$$= 18 - 5.369 \times 10^{-3} \times 1.0 \times 10^3 - 5.423 \times 10^{-3} \times 2.2 \times 10^3$$
$$= 0.7 \text{ V}$$

Example 2.13 Figure 2.36 shows the fixed bias with emitter feedback circuit. Determine the base current, collector current, collector-to-emitter voltage and stability factor of a biasing circuit as shown in Fig. 2.36. Assume $V_{BE} = 0.7$ V and $\beta = 50$.

Sol. Given: $V_{CC} = 20$ V, $R_B = 200$ kΩ, $R_C = 900$ Ω, $R_E = 350$ Ω, $V_{BE} = 0.7$ V and $\beta = 50$

Applying Kirchhoff's voltage law in the base-emitter circuit, we obtain

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

Since $I_E = (1 + \beta) I_B$, $I_E = (1 + 50) I_B$ as $\beta = 50$

or $\quad 20 = I_B \times 200 \times 10^3 + 0.7 + (1 + 50) I_B \times 350$

Then the base current is

$$I_B = \frac{20 - 0.7}{200 \times 10^3 + 51 \times 350} = 8.8593 \times 10^{-5} \text{ A}$$

The collector current is

$$I_C = \beta I_B = 50 \times 8.8593 \times 10^{-5} \text{ A} = 4.4296 \text{ mA}$$

The emitter current is

$$I_E = I_C + I_B = 4.4296 \text{ mA} + 8.8593 \times 10^{-5} \text{A}$$
$$= 4.518193 \text{ mA}$$

The collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$
$$= 20 - 4.4296 \times 10^{-3} \times 900 - 4.5181 \times 10^{-3} \times 350$$
$$= 14.4323 \text{ V}$$

The stability factor is

$$S = \frac{1 + \beta}{1 + \beta \dfrac{R_E}{R_E + R_B}}$$

$$= \frac{1 + 50}{1 + 50 \dfrac{350}{350 + 200 \times 10^3}} = 46.90$$

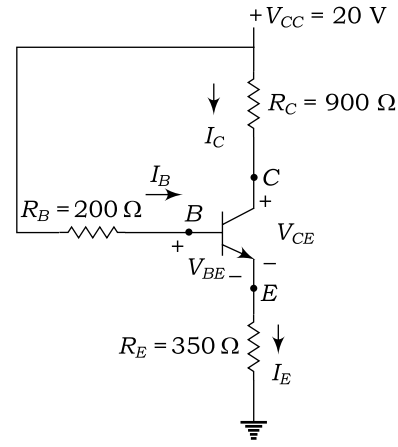


Fig. 2.36

Example 2.14 Figure 2.37 shows the fixed bias with collector feedback circuit. Calculate the base current, collector current, collector-to-emitter voltage and stability factor. Assume $V_{BE} = 0.7$ V and $\beta = 50$.

Sol. Given: $V_C = 12$ V, $R_B = 200$ kΩ, $R_C = 800$ Ω, $V_{BE} = 0.7$ V and $\beta = 55$

Applying Kirchhoff's voltage law in the base-emitter circuit, we obtain

$$V_{CC} = I_C R_C + I_B R_B + V_{BE}$$

Since $I_C = \beta I_B$, we can write

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE}$$

or $\quad 12 = 55 \times I_B \times 800 + I_B \times 200 \times 10^3 + 0.7$

Then the base current is

$$I_B = \frac{12 - 0.7}{55 \times 800 + 200 \times 10^3} = 4.631 \times 10^{-5}\,\text{A}$$

The collector current is

$$I_C = \beta I_B = 55 \times 4.631 \times 10^{-5}\text{A} = 2.547\ \text{mA}$$

The emitter current is

$$I_E = I_C + I_B = 2.547\ \text{mA} + 4.631 \times 10^{-5}\,\text{A} = 2.59331\ \text{mA}$$

The collector-to-emitter voltage is

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_C \\ &= 12 - 2.547 \times 10^{-3} \times 800 \\ &= 9.9624\ \text{V} \end{aligned}$$

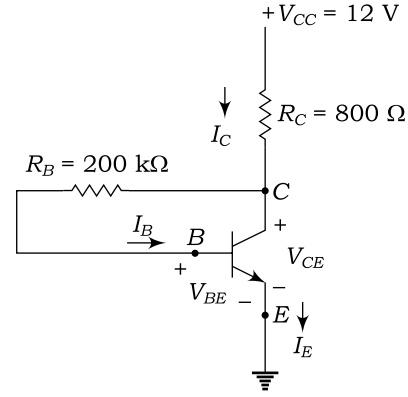


Fig. 2.37

The stability factor is

$$\begin{aligned} S &= \frac{1+\beta}{1+\beta\dfrac{R_C}{R_C + R_B}} \\ &= \frac{1+55}{1+55\dfrac{800}{800 + 200 \times 10^3}} = 45.93 \end{aligned}$$

Example 2.15 Determine the biasing resistance R_B of a collector feedback biasing circuit of an *NPN* transistor as depicted in Fig. 2.38 when the base current is 0.2 mA. Calculate the collector current, collector-to-emitter voltage and stability factor. Assume $V_{BE} = 0.7$ V and $\beta = 90$.

Sol. Given: $V_{CC} = 15$ V, $R_C = 800\ \Omega$, $V_{BE} = 0.7$ V, $V_{CE} = 5$ V and $\beta = 90$

Applying Kirchhoff's voltage law, we can write

$$V_{CC} = I_C R_C + V_{CE}$$

or

$$25 = I_C \times 800 + 5$$

Then the collector resistance is

$$I_C = \frac{25 - 5}{800} = 0.025\ \text{A}$$

The base current is

$$I_B = \frac{I_C}{\beta} = \frac{0.025}{90}\,\text{A} = 0.277\ \text{mA}$$

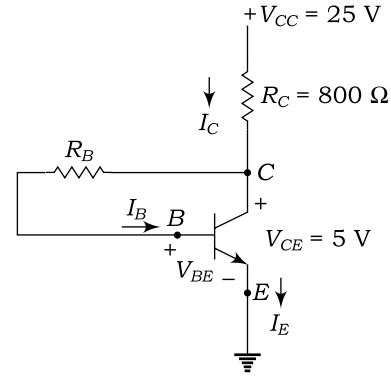


Fig. 2.38

Applying Kirchhoff's voltage law in the base-emitter junction, we get

$$V_{CC} = I_C R_C + I_B R_B + V_{BE}$$

or

$$25 = 0.025 \times 800 + 0.277 \times 10^{-3} \times R_B + 0.7$$

Then the base resistance is

$$R_B = \frac{25 - 0.025 \times 800 - 0.7}{0.277 \times 10^{-3}} = 15.52 \text{ k}\Omega$$

The stability factor is

$$S = \frac{1+\beta}{1+\beta\dfrac{R_C}{R_C + R_B}}$$

$$= \frac{1+90}{1+90\dfrac{800}{800+15.52\times10^3}} = 16.81$$

Example 2.16 Figure 2.39 shows the voltage-divider bias circuit. Determine the collector current and collector-to-emitter voltage. Assume $V_{BE} = 0.65$ V and $\beta = 60$.

Sol. Given: $V_{CC} = 15$ V, $R_1 = 10$ kΩ, $R_2 = 4.7$ kΩ, $R_C = 500$ Ω, $R_E = 350$ Ω, $V_{BE} = 0.65$ V and $\beta = 60$

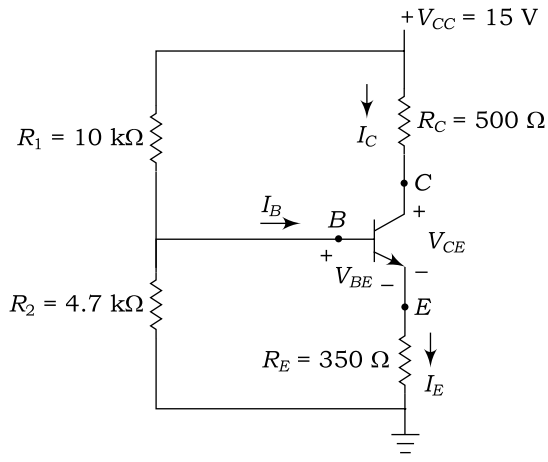


Fig. 2.39

The voltage at base of transistor is

$$V_B = V_{CC}\frac{R_2}{R_1+R_2} = 15 \times \frac{4.7}{10+4.7} \text{ V} = 4.79 \text{ V}$$

The voltage at emitter terminal is

$$V_E = V_B - V_{BE} = 4.79 - 0.65 \text{ V} = 4.14 \text{ V}$$

The emitter current is

$$I_E = \frac{V_E}{R_E} = \frac{4.14}{350} \text{ A} = 0.01182 \text{ A}$$

Assume the collector current is equal to the emitter current.

Hence, $I_C = I_E = 0.01182$ A

The collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C(R_C + R_E) = 15 - 0.01182(500 + 350) = 4.953 \text{ V}$$

Example 2.17 The voltage-divider bias circuit of an *NPN* transistor is shown in Fig. 2.40. Calculate the value of R_1 and R_C when collector current is 1 mA and collector to emitter voltage is 2.6 V. Assume $V_{BE} = 0.65$ V and $\beta = 100$.

Sol. Given: $V_{CC} = 6$ V, $R_2 = 10$ kΩ, $R_E = 350$ Ω, $V_{CE} = 2.6$ V, $V_{BE} = 0.65$ V and $\beta = 60$

The collector current is $I_C = 1$ mA

Assume the collector current is equal to the emitter current.

Then $I_C = I_E = 1$ mA

The collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

or $\quad 2.6 = 6 - 1 \times 10^{-3} \times (R_C + 350)$

Then $\quad R_C + 350 = \dfrac{6 - 2.6}{1 \times 10^{-3}} = 3400\ \Omega$

Therefore, the resistance R_C is equal to (3400 – 350) = 3050 Ω.

The voltage at emitter terminal is

$$V_E = I_E R_E = 1 \times 10^{-3} \times 350\ \text{V} = 0.35\ \text{V}$$

The voltage at base of transistor is

$$V_B = V_E + V_{BE} = (0.35 + 0.65)\ \text{V} = 1\ \text{V}$$

Actually, the voltage at the base of the transistor in terms of resistances R_1 and R_2 is

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2}$$

or

$$1 = 6 \times \frac{10}{R_1 + 10}$$

The value of the resistance R_1 is

$$R_1 = (60 - 10)\ \text{k}\Omega = 50\ \text{k}\Omega$$

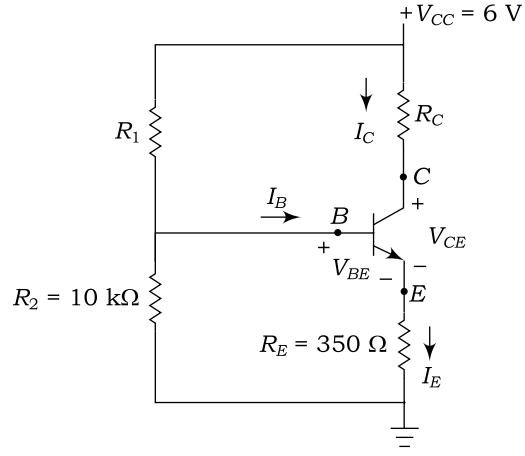


Fig. 2.40

Example 2.18 Figure 2.41 shows the voltage-divider bias circuit. Determine the emitter current and collector-to-emitter voltage. Calculate the collector potential V_C. Assume $V_{BE} = 0.65$ V and $\beta = 75$.

Sol. Given: $V_{CC} = 18$ V, $R_1 = 10$ kΩ, $R_2 = 9.5$ kΩ, $R_C = 1.5$ kΩ, $R_E = 4.5$ kΩ, $V_{BE} = 0.65$ V and $\beta = 75$

The voltage at base of transistor is

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2} = 18 \times \frac{9.5}{10 + 9.5}\ \text{V} = 8.769\ \text{V}$$

The voltage at emitter terminal is

$$V_E = V_B - V_{BE} = 8.769 - 0.65\ \text{V} = 8.119\ \text{V}$$

The emitter current is

$$I_E = \frac{V_E}{R_E} = \frac{8.119}{4.5 \times 10^3}\ \text{A} = 1.8042\ \text{mA}$$

Assume the collector current is equal to the emitter current.

Hence, $I_C = I_E = 1.8042$ mA

The collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 15 - 1.804 \times 10^{-3}(1.5 \times 10^3 + 4.5 \times 10^3) = 4.1746\ \text{V}$$

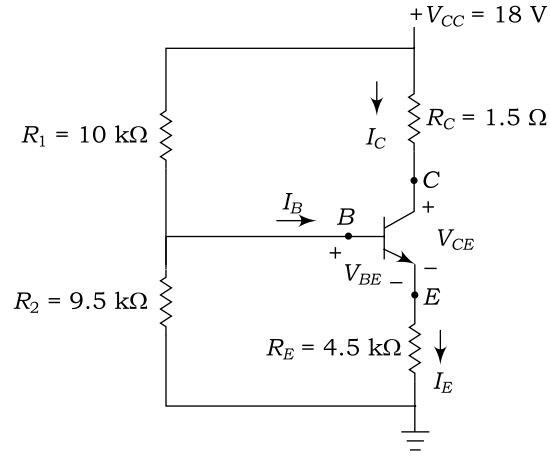


Fig. 2.41

The collector potential V_C is

$$V_C = V_{CC} - I_C R_C$$
$$= 15 - 1.804 \times 10^{-3} \times 1.5 \times 10^3 = 12.294 \text{ V}$$

Example 2.19 Figure 2.42 shows a transistor amplifier circuit. Determine the percentage change in collector current when the transistor with $\beta = 75$ is replaced by the transistor with $\beta = 100$. Assume $V_{BE} = 0.65$ V.

Sol. Given: $V_{CC} = 15$ V, $R_1 = 10$ kΩ, $R_2 = 10$ kΩ, $R_C = 1.2$ kΩ, $R_E = 500$ Ω, $V_{BE} = 0.65$ V and $\beta = 75$ and $\beta = 100$

Thevenin's voltage of transistor is

$$V_{th} = V_{CC} \frac{R_2}{R_1 + R_2} = 15 \times \frac{10}{10+10} \text{ V} = 7.5 \text{ V}$$

Thevenin's equivalent resistance is

$$R_{th} = R_1 \parallel R_2 = 10 \text{ k}\Omega \parallel 10 \text{ k}\Omega = 5 \text{ k}\Omega$$

At $\beta = 75$, the emitter current is

$$I_E = \frac{V_{th} - V_E}{\frac{R_{th}}{\beta} + R_E} = \frac{7.5 - 0.65}{\frac{5 \times 10^3}{75} + 500} \text{ A} = 12.088 \text{ mA}$$

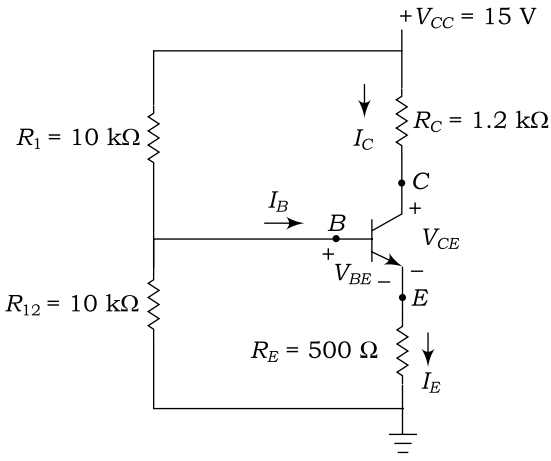


Fig. 2.42

At $\beta = 100$, the emitter current is

$$I_E = \frac{V_{th} - V_E}{\frac{R_{th}}{\beta} + R_E} = \frac{7.5 - 0.65}{\frac{5 \times 10^3}{100} + 500} \text{ A} = 12.45 \text{ mA}$$

The percentage change in emitter current when $\beta = 75$ is changed by the transistor with $\beta = 100$ is

$$\frac{12.45 - 12.088}{12.088} \times 100 = 2.99\%$$

Example 2.20 Figure 2.43 shows the voltage-divider bias circuit with $\beta = 60$. Determine the value of R_1, R_2 and R_E, if the stability factor is 5, $V_{CE} = 10.5$ V and $I_C = 1.2$ mA.

Sol. Given: $V_{CC} = 25$ V, $R_C = 2.2$ kΩ, $V_{BE} = 0.65$ V, $V_{CE} = 10.5$ V, $I_C = 1.2$ mA and $\beta = 60$

The collector to emitter voltage is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

or $$10.5 = 25 - 1.2 \times 10^{-3} (2.2 \times 10^3 + R_E)$$

The emitter resistance is equal to

$$R_E = \frac{25 - 10.5 - 1.2 \times 2.2}{1.2 \times 10^{-3}} = 9.88 \text{ k}\Omega$$

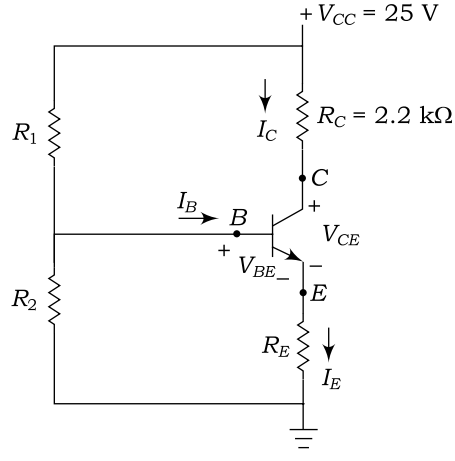


Fig. 2.43

The stability factor is

$$S = \frac{1+\beta}{1+\beta\dfrac{R_E}{R_{\text{th}}+R_E}}$$

or $$5 = \frac{1+60}{1+60\dfrac{9.88\times10^3}{R_{\text{th}}+9.88\times10^3}}$$

or $$5 = \frac{61\times(R_{\text{th}}+9.88\times10^3)}{R_{\text{th}}+9.88\times10^3+60\times9.88\times10^3}$$

$$R_{\text{th}} = \frac{5(9.88\times10^3+60\times9.88\times10^3)-61\times9.88\times10^3}{61-5} = 43.04\ \text{k}\Omega$$

For a very good voltage divider, the value of R_2 is

$$R_2 = 0.1\beta R_E = 0.1\times60\times9.88\ \text{k}\Omega = 59.28\ \text{k}\Omega$$

The value of Thevenin's resistance is

$$R_{\text{th}} = R_1 \| R_2 = \frac{R_1R_2}{R_1+R_2}$$

or $$43.04 = \frac{R_1\times59.28}{R_1+59.28}$$

The value of the resistance R_1 is

$$R_1 = \frac{43.04\times59.28}{59.28-43.04} = 157.05\ \text{k}\Omega$$

Example 2.21 Figure 2.44 shows the emitter bias circuit. Determine the emitter current, collector current, collector to emitter voltage and stability factor. Assume $V_{BE} = 0.7$ V and $\beta = 75$.

Sol. Given: $V_{CC} = 15$ V, $-V_{EE} = -15$ V, $R_B = 35$ kΩ, $R_C = 1.5$ kΩ, $R_E = 4.7$ kΩ, $V_{BE} = 0.7$ V

The emitter current is

$$I_E = \frac{V_{EE}-V_{BE}}{R_E} = \frac{15-0.7}{4.7\times10^3}\ \text{A} = 3.042\ \text{mA}$$

Assume the collector current is equal to the emitter current.

Hence, $I_C = I_E = 3.042$ mA

The collector potential V_C is

$$V_C = V_{CC} - I_CR_C$$
$$= 15 - 3.042\times10^{-3}\times1.5\times10^3 = 10.437\ \text{V}$$

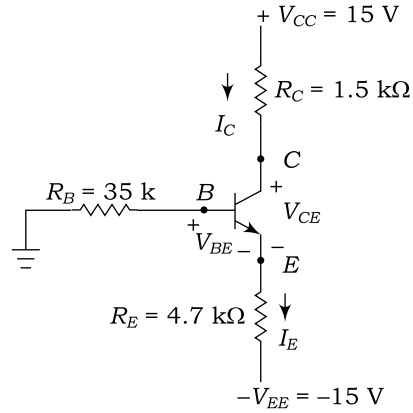


Fig. 2.44

The collector-to-emitter voltage is

$$V_{CE} = V_C - V_E$$
$$= 10.437 - (-0.7) = 11.137 \text{ V}$$

The stability factor is

$$S = \frac{1+\beta}{1+\beta\dfrac{R_E}{R_B+R_E}} = \frac{1+75}{1+75\dfrac{4.7}{35+4.7}} = 7.693$$

Example 2.22 The emitter-bias circuit of an *NPN* transistor is depicted in Fig. 2.45. Explain how the *Q*-point changes when the value of β changes from 60 to 100. Assume $V_{BE} = 0.7$ V.

Sol. Given: $V_{CC} = 10$ V, $-V_{EE} = -10$ V, $R_B = 25$ kΩ, $R_C = 4.7$ kΩ, $R_E = 4.7$ kΩ, $V_{BE} = 0.7$ V and $\beta = 60$ to 100

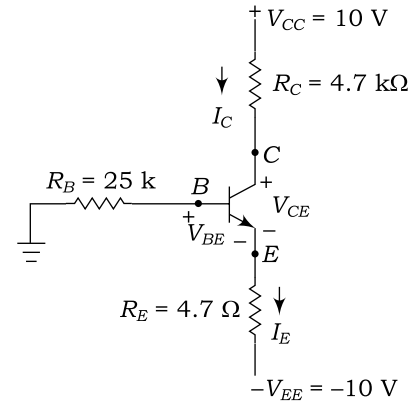


Fig. 2.45

The emitter current is

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + \dfrac{R_B}{\beta}} = \frac{15 - 0.7}{4.7\times10^3 + \dfrac{25\times10^3}{60}} \text{ A} = 2.795 \text{ mA}$$

Assume the collector current is equal to the emitter current.

Hence, $I_C = I_E = 2.795$ mA

The collector potential V_C is

$$V_C = V_{CC} - I_C R_C$$
$$= 15 - 2.795 \times 10^{-3} \times 4.7 \times 10^3 = 1.8635 \text{ V}$$

The collector-to-emitter voltage is

$$V_{CE} = V_C - V_E$$
$$= 1.8635 - (-0.7) = 2.5635 \text{ V}$$

The *Q*-point is 2.5635 V, 2.795 mA

Due to change in value of β from 60 to 100,

the emitter current is

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + \dfrac{R_B}{\beta}} = \frac{15 - 0.7}{4.7\times10^3 + \dfrac{25\times10^3}{100}} \text{ A} = 2.88 \text{ mA}$$

Assume the collector current is equal to the emitter current.

Hence, $I_C = I_E = 2.88$ mA

The collector potential V_C is

$$V_C = V_{CC} - I_C R_C$$
$$= 15 - 2.88 \times 10^{-3} \times 4.7 \times 10^3 = 1.464 \text{ V}$$

The collector-to-emitter voltage is

$$V_{CE} = V_C - V_E$$
$$= 1.464 - (-0.7) = 2.164 \text{ V}$$

The new *Q*-point is 2.164 V, 1.464 mA

Example 2.23 The divider biasing circuit of a *PNP* transistor is depicted in Fig. 2.46. Determine the *Q* point of the circuit when the value of β is 50. Assume $V_{BE} = 0.5$ V.

Sol. Given: $V_{CC} = 10$ V, $R_1 = 30$ kΩ, $R_2 = 1$ kΩ, $R_C = 1.2$ kΩ, $R_E = 300$ Ω, $V_{BE} = 0.5$ V and $\beta = 50$

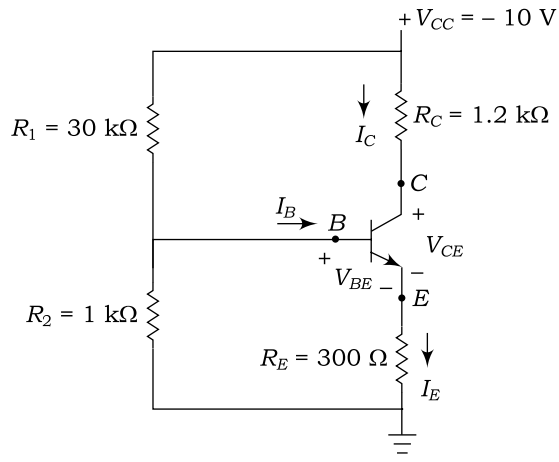


Fig. 2.46

The voltage *B* is

$$V_B = -V_{CC} \times \frac{R_2}{R_1 + R_2}$$

$$= -10 \times \frac{1}{10 + 30} = -0.25 \text{ V}$$

The voltage at emitter is

$$V_E = V_B - V_{BE}$$

$$= -0.25 \text{ V} - (+0.5) \text{ V} = -0.75 \text{ V}$$

The emitter current is

$$I_E = \frac{V_E}{R_E} = -\frac{0.75}{300} \text{A} = -0.0025 \text{ A}$$

Assume the collector current is equal to the emitter current.

Hence, $I_C = I_E = -0.0025$ A

The collector potential V_C is

$$V_C = (V_{CC} - I_C R_C)$$

$$= -10 - (-0.0025 \times 1.2 \times 10^3) = -7 \text{ V}$$

The collector-to-emitter voltage is

$$V_{CE} = -V_C - (-V_E)$$

$$= -7 - (-0.75) = -6.25 \text{ V}$$

The *Q* point is –6.25 V, 2.5 mA

2.18 BIAS COMPENSATION TECHNIQUES

The compensation techniques are used to stabilise the *Q*-point. Usually *PN*-junction diodes, thermistors (R_T) and transistors are temperature sensitive devices and can be used to compensate the change in collector current (I_C) and the operating point (*Q* point) will be stabilised. This method is called *bias compensation*.

2.18.1 Diode Compensation

Figure 2.47 shows that a *PN*-junction diode is connected across the base-emitter junction of the transistor for *bias compensation*. The diode is made by the same material as that of transistor to provide proper bias compensation. Since the diode is reverse biased by the base-emitter junction voltage, the reverse saturation current (I_{C0} or I_0) flows through diode. If the temperature increases, the amplitude of reverse saturation current (I_{C0}) increases in the transistor. Consequently, the leakage current I_0 through the diode also increases. The current flow through the resistance R_B is $I = I_B + I_0$ which remains constant. When the leakage current through the diode increases, the base current decreases and the current *I* is maintained at constant. As the current flow through R_B is maintained constant, the collector current will be constant.

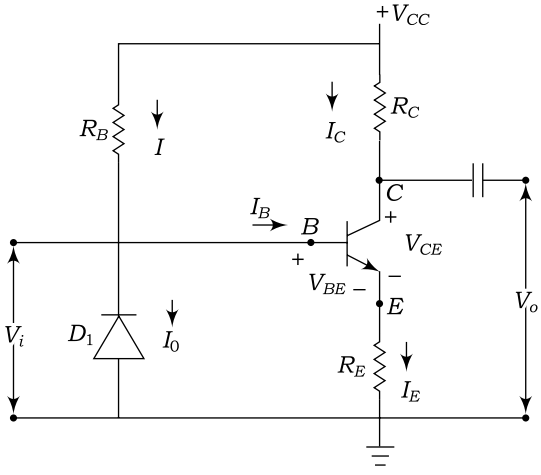


Fig. 2.47 Bias compensation using diode

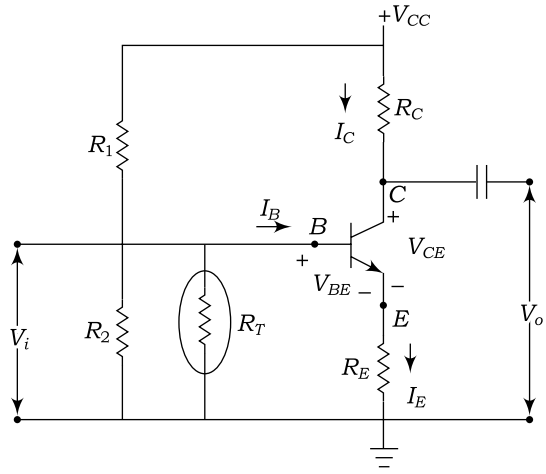


Fig. 2.48 Bias compensation using thermistor

2.18.2 Thermistor Compensation

Figure 2.48 shows the bias compensation using a *thermistor* (R_T) which is connected in parallel with resistance R_2. Thermistor (R_T) is a non-linear device and can be used for providing bias compensation. It has a negative temperature coefficient. The resistance of thermistor (R_T) decreases with increasing temperature. Similarly, the resistance of thermistor (R_T) increases when temperature decreases. As it is connected in parallel with resistance R_2, the value of equivalent resistance of $R_2 \| R_T$ decreases with increasing temperature and correspondingly the forward bias voltage of base-emitter junction decreases. Then, the base current decreases and consequently collector current will be constant.

2.18.3 Sensistor Compensation

Figure 2.49 shows the sensistor bias compensation where sensistor R_S is connected across R_1. R_S has positive temperature coefficient and its resistance value increases with increasing temperature. Consequently, the equivalent resistance of the parallel combination of R_1 and R_S increases and the base voltage decreases. Hence, the base current I_B and collector current I_C are reduced significantly. This reduced I_C compensates the increased I_C due to increase in I_{C0}, V_{BE} and β due to temperature increase.

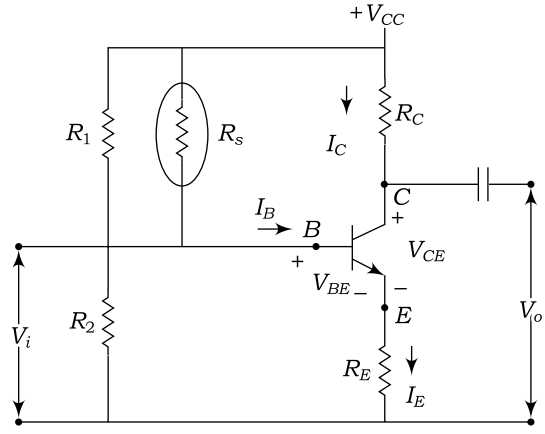


Fig. 2.49 Bias compensation using sensistor

2.19 *h*-PARAMETER EQUIVALENT CIRCUIT MODEL OF BJT

The *h*-parameter equivalent circuit model of a transistor can be represented by a two-port network. Figure 2.50 shows a two-port network, where V_1, I_1, V_2 and I_2 are the terminal voltages and current.

Assume I_1 and V_2 are independent variables, and V_1 and I_2 are dependent variables.

Then the values of V_1 and I_2 are expressed as

$$V_1 = f_1(I_1, V_2)$$

$$I_2 = f_2(I_1, V_2)$$

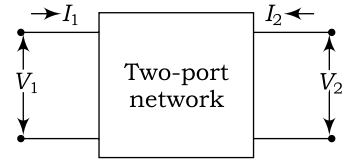


Fig.2.50 Two-port network

After taking total differential of the above equation, we obtain

$$dV_1 = \frac{\partial V_1}{\partial I_1} dI_1 + \frac{\partial V_1}{\partial V_2} dV_2 \tag{2.64}$$

$$dI_2 = \frac{\partial I_2}{\partial I_1} dI_1 + \frac{\partial I_2}{\partial V_2} dV_2 \tag{2.65}$$

When the two-port network operates at the linear region, the partial derivatives become constant. Equations (2.64) and (2.65) can be written as

$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$

where, V_1 = Input voltage ; I_1 = Input current,
V_2 = Output voltage ; I_2 = Output current, and
h_{11}, h_{12}, h_{21} and h_{22} are hybrid parameters.

When the output terminals are short circuited ($V_2 = 0$), hybrid parameters h_{11}, and h_{21} are determined.

h_{11} is the short-circuit input impedance and $h_{11} = \frac{V_1}{I_1}$ when $V_2 = 0$

h_{21} is the short-circuit forward current gain and $h_{21} = \frac{I_2}{I_1}$ when $V_2 = 0$

While the input terminals are open circuited ($I_1 = 0$), hybrid parameters h_{12} and h_{22} are determined.

h_{12} is the open-circuit reverse voltage gain and $h_{12} = \frac{V_1}{V_2}$ when $I_1 = 0$

h_{22} is the open-circuit output impedance and $h_{22} = \frac{I_2}{V_2}$ when $I_1 = 0$

Figure 2.51 shows the hybrid equivalent circuit of a linear circuit. In case of a transistor, $h_{11} = h_i$, $h_{12} = h_r$, $h_{21} = h_f$ and $h_{22} = h_o$. The hybrid equivalent circuit of a transistor is shown in Fig. 2.52.

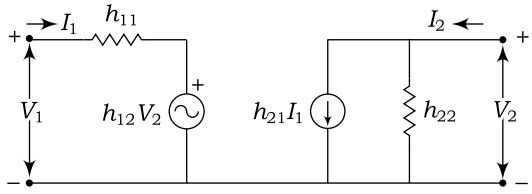


Fig. 2.51 Hybrid model of a linear circuit

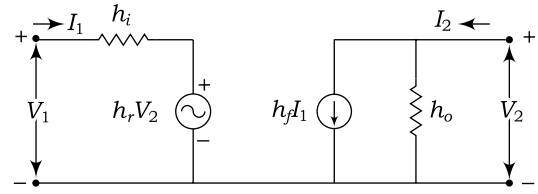


Fig. 2.52 Hybrid model of a bipolar junction

A bipolar junction transistor has three terminals, namely emitter, collector and base. A transistor has three different configurations known as common-emitter, common-base and common-collector configurations. In common-emitter configuration, the emitter is between input and output. Similarly, in common-base configuration, the base is common between input and output. In common-collector configuration, the collector is common between input and output. The corresponding *h*-parameters use a second subscript *e*, *b*, *c* to indicate the particular configuration. For example, the h_i parameter is represented by h_{ie}, h_{ib} and h_{ic} in common-emitter, common-base and common-collector configurations respectively. Table 2.2 shows the *h*-parameters of a transistor in different configurations.

Table 2.2 h-parameters of a transistor

General h-Parameters	*Common-Emitter (CE) Configuration*	*Common-Base (CB) Configuration*	*Common-Collector (CC) Configuration*
$h_{11} = h_i$	h_{ie}	h_{ib}	h_{ic}
$h_{12} = h_r$	h_{re}	h_{rb}	h_{rc}
$h_{21} = h_f$	h_{fe}	h_{fb}	h_{fc}
$h_{22} = h_o$	h_{oe}	h_{ob}	h_{oc}

2.19.1 Advantages of *h*-parameter

The advantages of *h*-parameter representation of a transistor are given below:

1. The *h*-parameters of a transistor are real numbers at audio-frequency range. Therefore, the reactive part of parameters are absent in *h*-parameter representation of transistor.
2. The *h*-parameters of a transistor can be measured and these parameters can be determined from static characteristics of a transistor.
3. The current gain, voltage gain, input resistance and output resistance can be derived in the simplest form.
4. The *h*-parameters can be used to analyse any transistor circuit.
5. In the data sheet of a transistor, the *h*-parameters are specified by the manufacturer.

2.19.2 Hybrid Equivalent Circuit of Common-Emitter Configuration

Figure 2.53(a) shows the common-emitter configuration of transistor and its hybrid equivalent circuit is depicted in Fig. 2.53(b). In this configuration, the input signal is applied between base and emitter terminals and the output is obtained from the collector and emitter terminals. The input voltage V_{BE} and output current I_C is expressed as

$$V_{BE} = h_{ie} I_B + h_{re} V_{CE}$$
$$I_C = h_{fe} I_B + h_{oe} V_{CE}$$

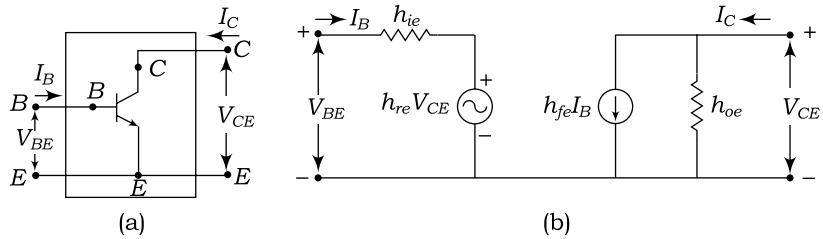


Fig. 2.53 (a) Common-emitter transistor (b) Hybrid equivalent circuit of a common-emitter transistor

2.19.3 Hybrid Equivalent Circuit of Common-Base Configuration

Figure 2.54(a) shows the common base configuration of a transistor and in Fig. 2.54(b), its hybrid equivalent circuit is depicted. In this configuration, the input signal is applied between emitter and base terminals and the output is obtained from the collector and base terminals. The input voltage V_{EB} and output current I_C are given by

$$V_{EB} = h_{ib} I_E + h_{re} V_{CB} \tag{2.66}$$

$$I_C = h_{fc} I_E + h_{ob} V_{CB} \tag{2.67}$$

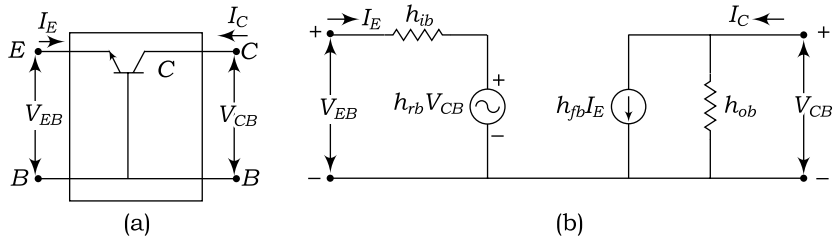


Fig. 2.54 (a) Common-base transistor (b) Hybrid equivalent circuit of a common-base transistor

2.19.4 Hybrid Equivalent Circuit of Common-Collector Configuration

Figure 2.55(a) shows the common-emitter configuration of a transistor and in Fig. 2.55(b) its hybrid equivalent circuit is depicted. In this configuration, the input signal is applied between base and collector terminals and the output is obtained from the emitter and collector terminals. The input voltage V_{BC} and output current I_E are expressed as

$$V_{BC} = h_{ic} I_B + h_{rc} V_{EC}$$

$$I_E = h_{fc} I_B + h_{oc} V_{EC}$$

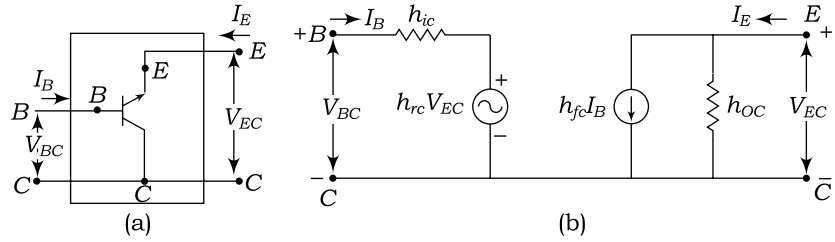


Fig. 2.55 (a) Common collector transistor (b) Hybrid equivalent circuit of a common-collector transistor

2.20 ANALYSIS OF A TRANSISTOR AMPLIFIER USING *h*-PARAMETERS

Figure 2.56 shows the generalised amplifier circuit and in Fig. 2.57, *h*-parameters equivalent circuit of a transistor as an amplifier is depicted. In this circuit, the transistor may be connected in either common-emitter or common-base or common-collector configurations. An ac voltage V_S having internal resistance R_S is connected to the input terminals. A load resistance R_L is connected to the output terminals. The input voltage V_1 and output current I_2 can be expressed as

$$V_1 = h_i I_1 + h_r V_2 \tag{2.68}$$

$$I_2 = h_f I_1 + h_o V_2 \tag{2.69}$$

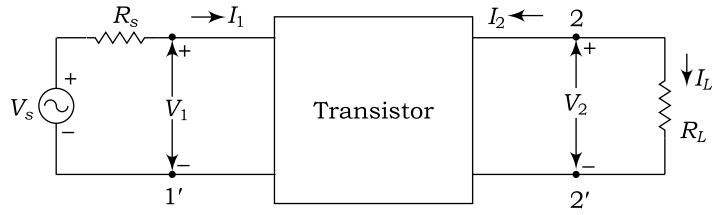


Fig. 2.56 Generalised transistor amplifier circuit

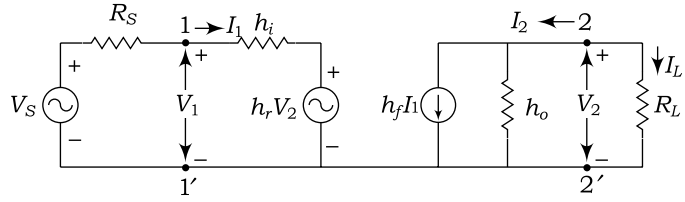


Fig. 2.57 Hybrid equivalent circuit of a generalised transistor amplifier

In this section, the determination of current gain, input resistance, voltage gain, output resistance and power gain are discussed in detail.

2.20.1 Current Gain

The current gain, or current amplification factor, of a transistor is defined by the ratio of the output current (I_L) to the input current (I_1). The current gain is represented by A_I and it can be represented by

$$A_I = \frac{I_L}{I_1} = -\frac{I_2}{I_1} \tag{2.70}$$

The output voltage is

$$V_2 = I_L R_L = -I_2 R_L \tag{2.71}$$

After substituting the value of V_2 in Eq. (2.69), we get

$$I_2 = h_f I_1 + h_o V_2 = h_f I_1 - h_o I_2 R_L$$

or $$(1 + h_o R_L) I_2 = h_f I_1$$

or $$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L} \tag{2.72}$$

Therefore, the current gain is equal to

$$A_I = \frac{I_L}{I_1} = -\frac{I_2}{I_1} = -\frac{h_f}{1 + h_o R_L} \tag{2.73}$$

Since $h_o R_L << 1$, the current gain is $A_I = -h_f$

2.20.2 Input Resistance

The input resistance of a transistor amplifier is defined by the resistance looking into the amplifier input terminals 1 and 1′. It is also defined by the ratio of the input voltage V_1 to the input current I_1 and it can be expressed as

$$R_i = \frac{V_1}{I_1}$$

After substituting the value of V_2 in Eq. (2.68), we get

$$V_1 = h_i I_1 + h_r V_2 = h_i I_1 - h_r I_2 R_L \qquad \text{as } V_2 = -I_2 R_L$$

After dividing the above equation by I_1, we obtain

$$\frac{V_1}{I_1} = \frac{h_i I_1 - h_r I_2 R_L}{I_1} = h_i - h_r R_L \frac{I_2}{I_1} \tag{2.74}$$

Then input resistance is equal to

$$R_i = \frac{V_1}{I_1} = h_i + h_r R_L A_I \qquad \text{as } A_I = -\frac{I_2}{I_1} \tag{2.75}$$

After substituting the value of A_I in the above equation, we find

$$R_i = h_i + h_r R_L A_I = h_i - \frac{h_r h_f R_L}{1 + h_o R_L} \qquad \text{as } A_I = -\frac{h_f}{1 + h_o R_L} \tag{2.76}$$

It is clear from the above expression that the input resistance (R_i) is a function the load resistance R_L.

2.20.3 Voltage Gain

The voltage gain, or voltage amplification factor, is defined as the ratio of output voltage (V_2) to the input voltage (V_1) and it can be expressed as

$$A_V = \frac{V_2}{V_1} = -\frac{I_2 R_L}{V_1}$$

After substituting the value of I_2 in the above equation, we get

$$A_V = -\frac{I_2 R_L}{V_1} = \frac{A_I I_1 R_L}{V_1} \qquad \text{as } I_2 = -A_I I_1$$

or

$$A_V = \frac{A_I I_1 R_L}{V_1} = A_I R_L \frac{I_1}{V_1} = \frac{A_I R_L}{R_i} \qquad \text{as } R_i = \frac{V_1}{I_1} \tag{2.77}$$

When the values of A_I and R_I are substituted in Eq. (2.77), we obtain

$$A_V = -\frac{h_f R_L}{h_i + (h_i h_o - h_r h_f) R_L} \tag{2.78}$$

As $\Delta h = h_i h_o - h_r h_f$, the voltage gain can be expressed as

$$A_V = -\frac{h_f R_L}{h_i + \Delta h R_L} \tag{2.79}$$

2.20.4 Output Resistance

The output resistance of transistor amplifier is the resistance looking into the output terminals 2 and 2′ when the source voltage is zero but its internal resistance is connected between input terminals as shown in Fig. 2.58. Actually, the output resistance is the ratio of output voltage (V_2) to the output current (I_2) and it is given by

$$R_o = \frac{V_2}{I_2}$$

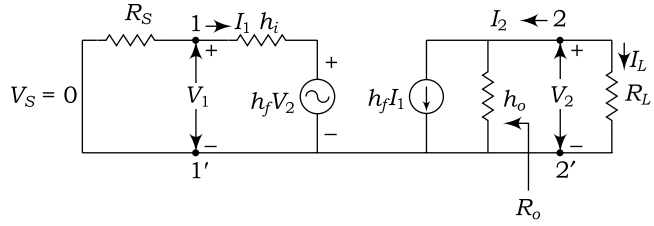


Fig. 2.58 Hybrid equivalent circuit of a transistor amplifier with $V_S = 0$

After substituting the value of $I_2 = h_f I_1 + h_o V_2$ in the above equation, we get

$$R_o = \frac{V_2}{h_f I_1 + h_o V_2} \tag{2.80}$$

Applying the Kirchhoff's voltage law (KVL) in the input side of the transistor amplifier circuit, we obtain

$$I_1(R_S + h_i) + h_r V_2 = 0$$

or
$$I_1 = -\frac{h_r V_2}{R_S + h_i} \tag{2.81}$$

After substituting value of I_1 in Eq. (2.80), we obtain

$$R_o = \frac{V_2}{h_f I_1 + h_o V_2} = \frac{V_2}{h_f \left(-\frac{h_r V_2}{R_S + h_i}\right)_1 + h_o V_2}$$

or
$$R_o = \frac{R_S + h_i}{(R_S + h_i)h_o - h_f h_r} = \frac{R_S + h_i}{R_S h_o + (h_i h_o - h_f h_r)}$$

or
$$R_o = \frac{R_S + h_i}{R_S h_o + \Delta h} \qquad \text{As } \Delta h = h_i h_o - h_r h_f \tag{2.82}$$

Since internal resistance is very small, $\Delta h >> R_S h_o$. Then the output resistance is equal to

$$R_o = \frac{R_S + h_i}{\Delta h}$$

2.20.5 Power Gain

The power gain of a transistor amplifier is the ratio of the output power to the input power and it can be written as

$$A_P = \frac{V_2 I_L}{V_1 I_1} = \left(\frac{V_2}{V_1}\right)\left(-\frac{I_2}{I_1}\right) = A_V A_I \tag{2.83}$$

Hence, the power gain is the product of voltage gain (A_V) and the current gain (A_I).

As $A_V = \frac{A_I R_L}{R_i}$, the power gain is equal to

$$A_P = A_V A_I = {A_I}^2 \frac{R_L}{R_i} \tag{2.84}$$

After substituting the value of A_I in the above equation, we get

$$A_P = \frac{h_f^2 R_L}{(1 + h_o R_L)(\Delta_h R_L + h_i)} \tag{2.85}$$

2.20.6 Effect of Source Resistance on Voltage and Current Gains

When the source resistance R_S is incorporated into account, the overall voltage gain becomes

$$A_{VO} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \times \frac{V_1}{V_S} = A_V \times \frac{V_1}{V_S} \tag{2.86}$$

The input voltage is equal to

$$V_1 = V_S \times \frac{R_i}{R_S + R_i}$$

or

$$\frac{V_1}{V_S} = \frac{R_i}{R_S + R_i} \tag{2.87}$$

Therefore, the voltage gain is given by

$$A_{VO} = \frac{V_2}{V_S} = A_V \times \frac{V_1}{V_S} = A_V \times \frac{R_i}{R_S + R_i} \quad \text{as } \frac{V_1}{V_S} = \frac{R_i}{R_S + R_i} \tag{2.88}$$

The overall current gain of the transistor is the ratio of the output current I_L to the source current I_S. Then overall current gain is

$$A_{IO} = \frac{I_L}{I_S} = -\frac{I_2}{I_S}$$

or

$$A_{IO} = -\frac{I_2}{I_S} = -\frac{I_2}{I_1} \times \frac{I_1}{I_S} = -A_I \times \frac{I_1}{I_S} \tag{2.89}$$

The input current is

$$I_1 = I_S \frac{R_S}{R_S + R_i}$$

or

$$\frac{I_1}{I_S} = \frac{R_S}{R_S + R_i} \tag{2.90}$$

Then overall current gain is equal to

$$A_{IO} = -A_I \times \frac{I_1}{I_S} = -A_I \times \frac{R_S}{R_S + R_i} \tag{2.91}$$

2.21 COMMON-EMITTER AMPLIFIER

Figure 2.59 shows the common-emitter amplifier circuit of a transistor and its *h*-parameter equivalent circuit is depicted in Fig. 2.60. The equations for V_{BE} and I_C of a common emitter amplifier are

$$V_{BE} = h_{ie} I_B + h_{re} V_{CE} \tag{2.92}$$

$$I_C = h_{fe} I_B + h_{oe} V_{CE} \tag{2.93}$$

The current gain, voltage gain, input resistance and output resistance of a common emitter amplifier can be determined using the same procedure which is used in a generalised transistor amplifier. Therefore, the equations of a generalised transistor amplifier can be used for common-emitter amplifier circuit by adding a second subscript *e* with the *h*-parameters.

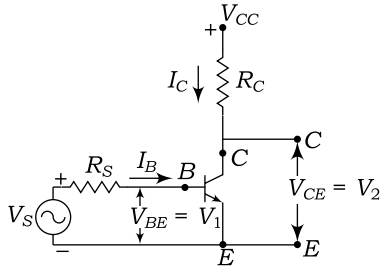


Fig. 2.59 Common-emitter amplifier circuit of a transistor

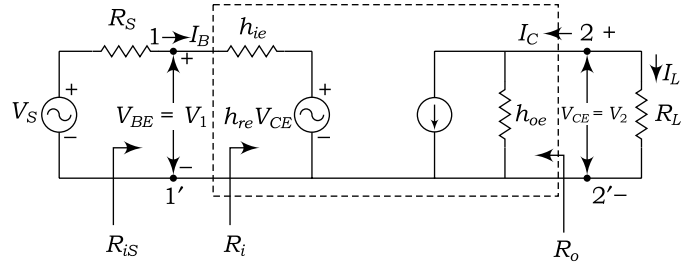


Fig. 2.60 *h*-parameter equivalent of a common-emitter transistor amplifier

2.21.1 Current Gain

The current gain of a common-emitter amplifier is given by

$$A_I = -\frac{h_{fe}}{1 + h_{oe}R_L} \tag{2.94}$$

where, R_L is the load resistance which is the equivalent resistance of a parallel combination of R_C and R_L. h_{fe} is the short-circuit forward current gain and h_{oe} is the open-circuit output impedance.

2.21.2 Input Resistance

The input resistance of a common-emitter transistor amplifier is

$$\begin{aligned} R_i &= \frac{V_1}{I_1} \\ &= h_{ie} + h_{re}R_L A_I \\ &= h_{ie} - \frac{h_{re}h_{fe}R_L}{1 + h_{oe}R_L} \quad \text{as } A_I = -\frac{h_{fe}}{1 + h_{oe}R_L} \end{aligned} \tag{2.95}$$

The input resistance of an amplifier depends on the biasing circuit configuration. In a fixed-bias circuit, the input resistance is equal to

$$R_{iS} = R_i \| R_B \tag{2.96}$$

2.21.3 Voltage Gain

The voltage gain of a common-emitter transistor amplifier is

$$A_V = \frac{V_2}{V_1} = \frac{A_I R_L}{R_i} \tag{2.97}$$

As the current gain of a common-emitter amplifier is negative, voltage gain is also negative. Hence, the output voltage has 180° phase shift from the input voltage. Therefore, in a common-emitter amplifier, the output signal is the inverse of the input signal.

After substituting the value of A_I in the above equation (2.97), we obtain

$$A_V = -\frac{h_{fe}R_L}{h_{ie} + (h_{ie}h_{oe} - h_{re}h_{fe})R_L}$$

As $\Delta h = h_{ie}h_{oe} - h_{re}h_{fe}$, the voltage gain can be expressed as

$$A_V = -\frac{h_{fe}R_L}{h_{ie} + \Delta h R_L} \tag{2.98}$$

2.21.4 Output Resistance

The output resistance of a common-emitter transistor amplifier is

$$R_o = \frac{V_2}{I_2}$$

or

$$R_o = \frac{R_S + h_{ie}}{(R_S + h_{ie})h_{oe} - h_{fe}h_{re}} = \frac{R_S + h_{ie}}{R_S h_{oe} + (h_{ie}h_{oe} - h_{fe}h_{re})}$$

or

$$R_o = \frac{R_S + h_{ie}}{R_S h_{oe} + \Delta h} \qquad \text{as } \Delta h = h_{ie}h_{oe} - h_{re}h_{fe} \tag{2.99}$$

2.21.5 Effect of Source Resistance on Voltage and Current Gains

The overall voltage gain is

$$A_{VO} = \frac{V_2}{V_S} = A_V \times \frac{V_1}{V_S} = A_V \times \frac{R_S}{R_S + R_{iS}} \tag{2.100}$$

The overall current is equal to

$$A_{IO} = -A_I \times \frac{I_1}{I_S} = -A_I \times \frac{R_S}{R_S + R_{iS}} \tag{2.101}$$

2.22 COMMON-EMITTER AMPLIFIER WITH COLLECTOR FEEDBACK

Figure 2.61 shows a common-emitter amplifier with collector feedback. By using Miller's theorem, this circuit will be analysed. As per Miller's theorem, the collector feedback bias resistance R_B will be removed after incorporating two equivalent resistances R_1 and R_2 as shown in Fig. 2.62.

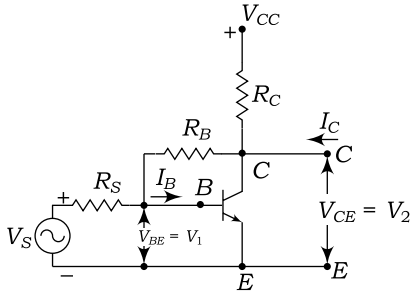


Fig. 2.61 Common-emitter amplifier with collector feedback

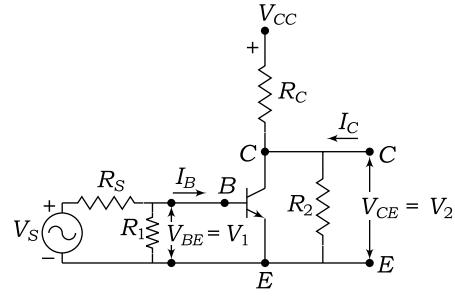


Fig. 2.62 The equivalent circuit of a common-emitter amplifier with collector feedback

The resistance R_1 is connected between the base and ground and its value is equal to

$$R_1 = \frac{R_B}{1 - A_V} \tag{2.102}$$

where, A_V is the voltage gain.

The resistance R_2 is connected between the collector and ground and its value is equal to

$$R_2 = \frac{R_B}{1 - \frac{1}{A_V}} = \frac{A_V}{A_V - 1} R_B \tag{2.103}$$

The ac equivalent load resistance is

$$R_L = R_C \parallel R_2 = \frac{R_C R_2}{R_C + R_2} \tag{2.104}$$

The current gain is equal to

$$A_I = -\frac{h_{fe}}{1 + h_{oe} R_L} \tag{2.105}$$

The voltage gain is given by

$$A_V = \frac{V_2}{V_1} = \frac{A_I R_L}{R_i} \tag{2.106}$$

The input resistance is

$$R_i = \frac{V_1}{I_1} = h_{ie} + h_{re} R_L A_I \tag{2.107}$$

The output resistance is equal to

$$R_o = \frac{R_s + h_{ie}}{R_s h_{oe} + \Delta h} \tag{2.108}$$

The overall voltage gain is given by

$$A_{VO} = A_V \frac{R_s}{R_s + R_i} \tag{2.109}$$

The overall current gain is

$$A_{IO} = A_I \frac{R_s}{R_s + R_i} \tag{2.110}$$

2.23 COMMON-BASE AMPLIFIER

Figure 2.63 shows the common-base amplifier and its *h*-parameter equivalent circuit is depicted in Fig. 2.64.

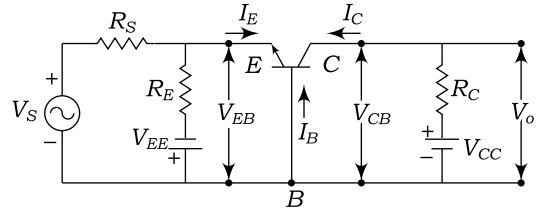


Fig. 2.63 Common-base amplifier

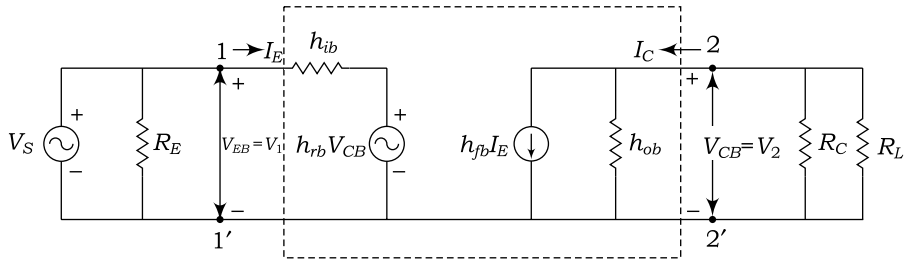


Fig. 2.64 h-parameter equivalent of a common-emitter transistor amplifier

The current gain of a common-base amplifier is

$$A_I = -\frac{h_{fb}}{1 + h_{ob}R_L} \tag{2.111}$$

The input resistance is

$$R_i = \frac{V_1}{I_1} = h_{ib} + h_{rb}R_L A_I \tag{2.112}$$

The voltage gain is given by

$$A_V = \frac{V_2}{V_1} = \frac{A_I R_L}{R_i} = -\frac{h_{fb}R_L}{h_{ib} + (h_{ib}h_{ob} - h_{rb}h_{fb})R_L} = -\frac{h_{fb}R_L}{h_{ib} + \Delta h R_L} \tag{2.113}$$

where, $\Delta h = h_{ib}h_{ob} - h_{rb}h_{fb}$

The output resistance is equal to

$$R_o = \frac{R_s + h_{ib}}{R_s h_{ob} + \Delta h} \tag{2.114}$$

The overall voltage gain is

$$A_{VO} = A_V \frac{R_s}{R_s + R_i} \tag{2.115}$$

The overall current gain is

$$A_{IO} = A_I \frac{R_s}{R_s + R_i} \tag{2.116}$$

2.24 COMMON-COLLECTOR AMPLIFIER

Figure 2.65 shows a common-collector amplifier and its *h*-parameter equivalent circuit is illustrated in Fig. 2.66.

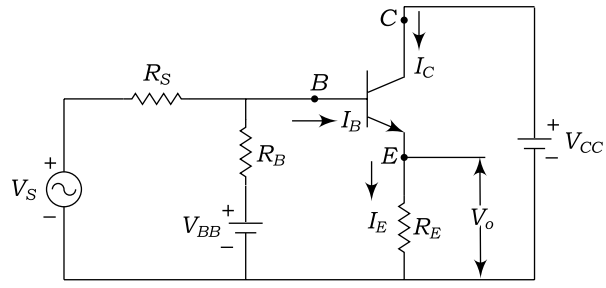


Fig. 2.65 Common-collector amplifier circuit

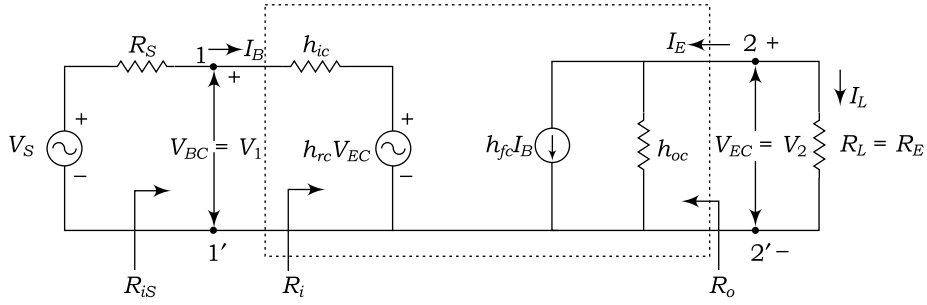


Fig. 2.66 *h*-parameter equivalent circuit of a common-collector amplifier

The current gain of a common-collector amplifier is

$$A_I = -\frac{h_{fc}}{1 + h_{oc}R_L} \tag{2.117}$$

where, R_L is the ac load resistance which is equal to resistance R_E and R_L.
As the value of h_{fc} is negative, the current gain is positive.
The input resistance is

$$R_i = \frac{V_1}{I_1} = h_{ic} + h_{rc}R_L A_I$$

$$= h_{ic} - \frac{h_{rc}h_{fc}R_L}{1 + h_{oc}R_L} \quad \text{as} \quad A_I = -\frac{h_{fc}}{1 + h_{oc}R_L} \tag{2.118}$$

The voltage gain is given by

$$A_V = \frac{V_2}{V_1} = \frac{A_I R_L}{R_i}$$

$$= -\frac{h_{fc}R_L}{h_{ic} + (h_{ic}h_{oc} - h_{rc}h_{fc})R_L} = -\frac{h_{fc}R_L}{h_{ic} + \Delta h R_L} \tag{2.119}$$

where, $\Delta h = h_{ic}h_{oc} - h_{rc}h_{fc}$
The output resistance is equal to

$$R_o = \frac{R_s + h_{ic}}{R_s h_{oc} + \Delta h} \tag{2.120}$$

where, R_s is the source resistance.
The overall voltage gain is

$$A_{VO} = A_V \frac{R_s}{R_s + R_i} \tag{2.121}$$

The overall current gain is

$$A_{IO} = A_I \frac{R_s}{R_s + R_i} \tag{2.122}$$

2.25 COMPARISON BETWEEN COMMON-EMITTER, COMMON-BASE AND COMMON-COLLECTOR AMPLIFIER

The current gain, voltage gain, input resistance and output resistance of common-emitter, common-base and common-collector amplifiers are derived in Sections 2.20 to 2.24. Table 2.3 shows the comparison between common-emitter, common-base and common-collector amplifiers.

Table 2.3 Comparison of CE, CB and CC amplifiers

Parameters	*Common-Emitter (CE) Amplifier*	*Common-Base (CB) Amplifier*	*Common-Collector (CC) Amplifier*
Current gain (A_I)	h_{fe}	$h_{fb} \approx 1$	h_{fc}
Voltage gain (A_V)	$\frac{h_{fe}R_L}{h_{ie}}$	$\frac{h_{fb}R_L}{h_{ib}}$	1
Input resistance (R_i)	h_{ie}	h_{ib}	$h_{ic} + h_{fc}R_L$
Output resistance (R_o)	$\frac{1}{h_{oe}}$	$\frac{1}{h_{ob}}$	$\frac{R_s + h_{ic}}{R_s h_{oc} + \Delta h}$

2.26 CONVERSION OF *h*-parameters

The transistor manufacturers do not provide the *h*-parameters for all three configurations. Only the common-emitter (CE) *h*-parameters are available in the manufacturer's data sheet. Therefore, whenever the transistor is used in some other configurations, it is required to convert the *h*-parameters from common emitter (CE) to either common base (CB) or common collector (CC) configuration. In this section, the conversion equations are discussed.

2.26.1 Conversion Equations from Common-Emitter to Common-Base Configuration

The conversion equations to determine the *h*-parameters of transistor in common-base configuration are given below:

$$h_{ib} = \frac{h_{ie}}{1 + h_{fe}} \quad (2.123) \qquad h_{rb} = \frac{h_{ie}h_{oe}}{1 + h_{fe}} \quad (2.124)$$

$$h_{fb} = \frac{h_{fe}}{1 + h_{fe}} \quad (2.125) \qquad h_{ob} = \frac{h_{oe}}{1 + h_{fe}} \quad (2.126)$$

2.26.2 Conversion Equations from Common-Emitter to Common-Collector Configuration

The conversion equations to determine the *h*-parameters of transistor in common-collector configuration are given below:

$$h_{ic} = h_{ie} \quad (2.127) \qquad h_{rc} = 1 - h_{re} \quad (2.128)$$

$$h_{fc} = -(1 + h_{fe}) \quad (2.129) \qquad h_{oc} = h_{oe} \quad (2.130)$$

2.27 DETERMINATION OF *h*-PARAMETERS

In a common-emitter configuration, input voltage is V_{BE} and output current is I_C. The base-emitter voltage V_{BE} and collector-current I_C are functions of base current I_B and collector to emitter voltage V_{CE} and the values of V_{BE} and I_C are expressed as

$$V_{BE} = f_1(I_B, V_{CE}) \tag{2.131}$$

$$I_C = f_2(I_B, V_{CE}) \tag{2.132}$$

After taking total differential of the above equation, we obtain

$$dV_{BE} = \frac{\partial V_{BE}}{\partial I_B} dI_B + \frac{\partial V_{BE}}{\partial V_{CE}} dV_{CE}$$

$$dI_C = \frac{\partial I_C}{\partial I_B} dI_B + \frac{\partial I_C}{\partial V_{CE}} dV_{CE}$$

The above equation can be written as

$$dV_{BE} = h_{ie} dI_B + h_{re} dV_{CE} \tag{2.133}$$

$$dI_C = h_{fe} dI_B + h_{oe} dV_{CE} \tag{2.134}$$

where, $h_{ie} = \frac{\partial V_{BE}}{\partial I_B}$, $h_{re} = \frac{\partial V_{BE}}{\partial V_{CE}}$, $h_{fe} = \frac{\partial I_C}{\partial I_B}$, and $h_{oe} = \frac{\partial I_C}{\partial V_{CE}}$

It is clear from the above equations that

- h_{ie} can be determined by the ratio of a small change in base-to-emitter voltage (ΔV_{BE}) to the change in the base current (ΔI_B) when the collector-to-emitter voltage V_{CE} is constant
- h_{re} can be determined by the ratio of a small change in base-to-emitter voltage (ΔV_{BE}) to the change in the collector-to-emitter voltage (ΔV_{CE}) when the base current (I_B) is constant
- h_{fe} can be determined by the ratio of a small change in collector current (ΔI_C) to the change in the base current (ΔI_B) when the collector-to-emitter voltage V_{CE} is constant
- h_{oe} can be determined by the ratio of a small change in collector current (ΔI_C) to the change in the collector to emitter voltage (ΔV_{CE}) when the base current (I_B) is constant.

The h_{ie} and h_{re} parameters can be determined from the input characteristics whereas h_{fe} and h_{oe} are determined from the output characteristics of a transistor.

Figure 2.67 shows the input characteristics of a transistor to determine h_{ie} and h_{re}. To compute the value of h_{ie}, draw a tangent on the point A. The small change in base-to-emitter voltage is ΔV_{BE} and the corresponding change in base current is ΔI_B. Then the value of h_{ie} is expressed as

$$h_{ie} = \frac{\partial V_{BE}}{\partial I_B} = \frac{\Delta V_{BE}}{\Delta I_B} \tag{2.135}$$

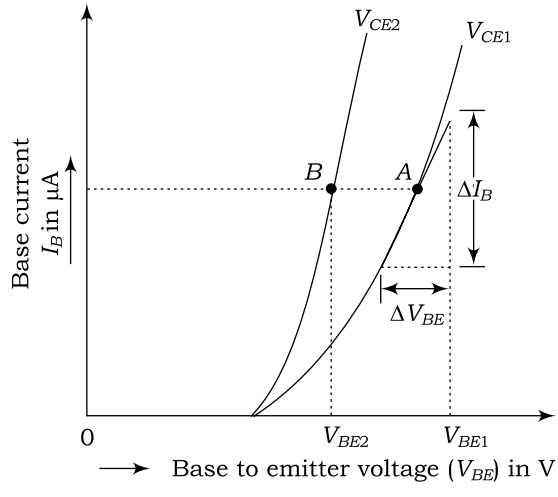


Fig. 2.67 Input characteristics of a transistor to determine h_{ie} and h_{re}

Another input characteristic is drawn at collector-to-emitter voltage V_{CE2} and draw a horizontal line through the point A which intersects at the point B on the input characteristic curve. Subsequently, measure the small change in base to emitter voltage ($\Delta V_{BE} = V_{BE1} - V_{BE2}$) and the change in the collector-to-emitter voltage $\Delta V_{CE} = V_{CE1} - V_{CE2}$. Then the value of h_{re} is computed from the equation

$$h_{re} = \frac{\partial V_{BE}}{\partial V_{CE}} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \tag{2.136}$$

Figure 2.68 shows the output characteristics a transistor to find h_{fe} and h_{oe}. To determine the value of h_{fe}, select two points C and D which are above and below the Q-point for constant collector-to-emitter voltage. The small change in base current is $\Delta I_B = I_{B1} - I_{B2}$ and the corresponding change in collector current is $\Delta I_C = I_{C1} - I_{C2}$. Then the value of h_{fe} is measured from the equation

$$h_{fe} = \frac{\partial I_C}{\partial I_B} = \frac{\Delta I_C}{\Delta I_B} \tag{2.137}$$

Draw a tangent to the curve at the point Q and find the change in the collector-to-emitter voltage $\Delta V_{CE} = V_{CE1} - V_{CE2}$ and the corresponding change in collector current $\Delta I_C = I_{C1} - I_{C2}$. Then the value of h_{oe} is measured using the equation

$$h_{oe} = \frac{\partial I_C}{\partial V_{CE}} = \frac{\Delta I_C}{\Delta V_{CE}} \tag{2.138}$$

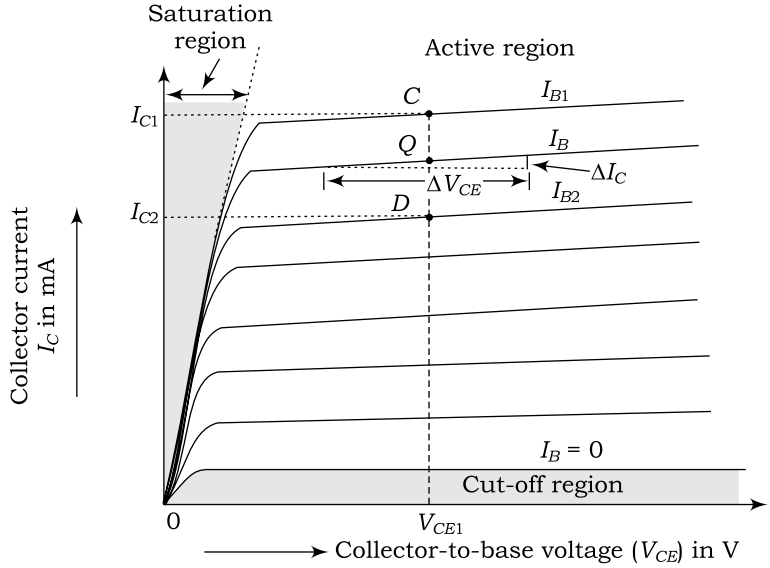


Fig. 2.68 Output characteristics a transistor to find h_{fe} and h_{oe}

Example 2.24 In common emitter configuration, a transistor has the following parameters $h_{ie} = 2.4$ kΩ, $h_{re} = 1.5 \times 10^{-4}$, $h_{fe} = 55$, $h_{oe} = 50 \times 10^{-6}$ μ siemens, $R_S = 1$ kΩ and $R_L = 2$ kΩ Determine the current gain, voltage gain, input impedance and output impedance.

Sol. Given: $h_{ie} = 2.4\ \text{k}\Omega$, $h_{re} = 1.5 \times 10^{-4}$, $h_{fe} = 55$, $h_{oe} = 50 \times 10^{-6}$ μ siemens, $R_S = 1\ \text{k}\Omega$ and $R_K = 2\ \text{k}\Omega$

The current gain of a common-emitter amplifier is given by

$$A_I = -\frac{h_{fe}}{1 + h_{oe}R_L} = -\frac{55}{1 + 50 \times 10^{-6} \times 2 \times 10^3} = 50$$

The input resistance of a common-emitter transistor amplifier is

$$R_i = \frac{V_1}{I_1} = h_{ie} + h_{re}R_L A_I = 2.4 \times 10^3 + 1.5 \times 10^{-4} \times 2 \times 10^3 \times 50 = 2415\ \Omega$$

The input resistance of an amplifier depends on the biasing circuit configuration. In a fixed-bias circuit, the input resistance is equal to

$$R_{iS} = R_i \| R_B = 2415 \| 1000\ \Omega = 707.17\ \Omega$$

The voltage gain of a common-emitter transistor amplifier is

$$A_V = \frac{V_2}{V_1} = \frac{A_I R_L}{R_i} = \frac{50 \times 2 \times 10^3}{2415} = 41.407$$

The output resistance of a common-emitter transistor amplifier is

$$R_o = \frac{V_2}{I_2} = \frac{R_S + h_{ie}}{R_S h_{oe} + (h_{ie}h_{oe} - h_{fe}h_{re})}$$

$$= \frac{1 \times 10^3 + 2.4 \times 10^3}{1 \times 10^3 \times 50 \times 10^{-6} + (2.4 \times 10^3 \times 50 \times 10^{-6} - 55 \times 1.5 \times 10^{-4})} = 21.63\ \text{k}\Omega$$

Example 2.25 Figure 2.69 shows a common-emitter transistor configuration with collector feedback, and it has the following parameters**:**

$h_{ie} = 1.4\ \text{k}\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 50 \times 10^{-6}$ μ siemens, $R_S = 1\ \text{k}\Omega$ and $R_L = 2\ \text{k}\Omega$

Determine the current gain, voltage gain, input impedance and output impedance.

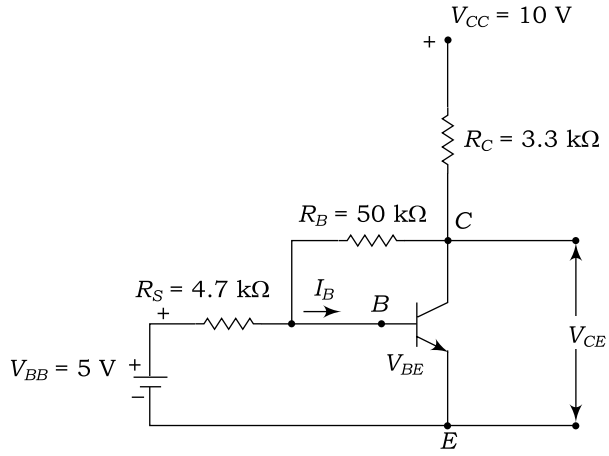


Fig. 2.69

Sol. Given: $h_{ie} = 1.4$ kΩ, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 50 \times 10^{-6}$ μ siemens, $R_S = 1$ kΩ and $R_L = 2$ kΩ

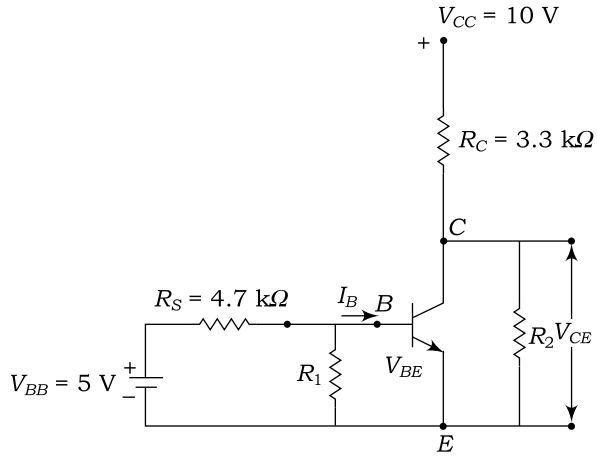


Fig. 2.70

The resistance R_1 is connected between the base and ground and its value is

$$R_1 = \frac{R_B}{1 - A_V}$$

The resistance R_2 is connected between the collector and ground and its value is

$$R_2 = \frac{R_B}{1 - \frac{1}{A_V}} = \frac{A_V}{A_V - 1} R_B$$ where, A_V is the voltage gain.

Since $A_V >> 1$, $R_2 = R_B = 50$ kΩ

The ac equivalent load resistance is

$$R_L = R_C \| R_2 = \frac{R_C R_2}{R_C + R_2} = \frac{3.3 \times 50}{3.3 + 50} = 3.095 \text{ kΩ}$$

The current gain is equal to

$$A_I = -\frac{h_{fe}}{1 + h_{oe} R_L} = -\frac{50}{1 + 50 \times 10^{-6} \times 3.095 \times 10^3} = -43.32$$

The input resistance is

$$R_i = \frac{V_1}{I_1} = h_{ie} + h_{re} R_L A_I = 1.4 \times 10^3 + 2.5 \times 10^{-4} \times 3.095 \times 10^3 \times 43.32 = 1433.51$$

The voltage gain is given by

$$A_V = \frac{V_2}{V_1} = \frac{A_I R_L}{R_i} = -\frac{43.32 \times 3.095 \times 10^3}{1433.51} = 93.52$$

Example 2.26 In common-base configuration, a transistor has the following parameters: $h_{ib} = 30\ \Omega$, $h_{rb} = 2.25 \times 10^{-4}$, $h_{fb} = -0.95$, $h_{ob} = 50 \times 10^{-6}$ siemens, $R_S = 1.5\ \text{k}\Omega$ and $R_L = 2.5\ \text{k}\Omega$
Determine the current gain, voltage gain, input impedance and output impedance.

Sol. Given: $h_{ib} = 30\ \Omega$, $h_{rb} = 2.25 \times 10^{-4}$, $h_{fb} = -0.95$, $h_{ob} = 50 \times 10^{-6}$ siemens, $R_S = 1.5\ \text{k}\Omega$ and $R_L = 2.5\ \text{k}\Omega$

The current gain of a common-base amplifier is

$$A_I = -\frac{h_{fb}}{1 + h_{ob}R_L} = -\frac{-0.95}{1 + 50 \times 10^{-6} \times 2.5 \times 10^3} = 0.844$$

The input resistance is

$$R_i = \frac{V_1}{I_1} = h_{ib} + h_{rb}R_L A_I$$

$$= 30 + 2.25 \times 10^{-4} \times 2.5 \times 10^3 \times 0.844 = 30.474$$

The voltage gain is given by

$$A_V = \frac{V_2}{V_1} = \frac{A_I R_L}{R_i} = \frac{0.844 \times 2.5 \times 10^3}{30.474} = 69.23$$

$$\Delta h = h_{ib}h_{ob} - h_{rb}h_{fb} = 30 \times 50 \times 10^{-6} - (2.25 \times 10^{-4} \times (-0.95)) = 17.1375 \times 10^{-4}$$

The output resistance is equal to

$$R_o = \frac{R_s + h_{ib}}{R_s h_{ob} + \Delta h} = \frac{1.5 \times 10^3 + 30}{1.5 \times 10^3 \times 50 \times 10^{-6} + 17.1375 \times 10^{-4}} = 19.94\ \text{k}\Omega$$

Example 2.27 In common-collector configuration, a transistor has the following parameters: $h_{ic} = 1.5\ \Omega$, $h_{rc} = 1$, $h_{fc} = -55$, $h_{oc} = 50 \times 10\ 10^{-6}$ siemens, $R_S = 1.5\ \text{k}\Omega$ and $R_L = 2.0\ \text{k}\Omega$
Determine the current gain, voltage gain, input impedance and output impedance.

Sol. Given: $h_{ic} = 1.5\ \text{k}\Omega$, $h_{rc} = 1$, $h_{fc} = -55$, $h_{oc} = 50 \times 10^{-6}$ siemens, $R_S = 1.5\ \text{k}\Omega$ and $R_L = 2.0\ \text{k}\Omega$

The current gain of a common collector amplifier is

$$A_I = -\frac{h_{fc}}{1 + h_{oc}R_L} = -\frac{-55}{1 + 50 \times 10^{-6} \times 2.0 \times 10^3} = 50$$

The input resistance is

$$R_i = \frac{V_1}{I_1} = h_{ic} + h_{rc}R_L A_I = 1.5 \times 10^3 + 1 \times 2.0 \times 10^3 \times 50 = 101.5\ \text{k}\Omega$$

The voltage gain is given by

$$A_V = \frac{V_2}{V_1} = \frac{A_I R_L}{R_i} = \frac{50 \times 2.0 \times 10^3}{101.5 \times 10^3} = 0.9852$$

$$\Delta h = h_{ic}h_{oc} - h_{rc}h_{fc} = 1.5 \times 10^3 \times 50 \times 10^{-6} - (1 \times (-55)) = 55.075$$

The output resistance is equal to

$$R_o = \frac{R_s + h_{ic}}{R_s h_{oc} + \Delta h} = \frac{1.5 \times 10^3 + 1.5 \times 10^3}{1.5 \times 10^3 \times 50 \times 10^{-6} + 55.075} = 54.39\ \Omega$$

2.28 EBERS–MOLL MODEL

A transistor consists of two interactive *PN*-junction diodes. Figure 2.71 shows the biasing arrangement of an *NPN* transistor which is commonly used to understand the Ebers–Moll model of a transistor. When the emitter-base junction is forward biased and the collector-base junction is reverse biased, the transistor can operate in the active region. If both the junctions of a transistor are forward biased, the transistor operates in saturation region. When both the junctions of a transistor are reverse biased, the transistor operates in cut-off region.

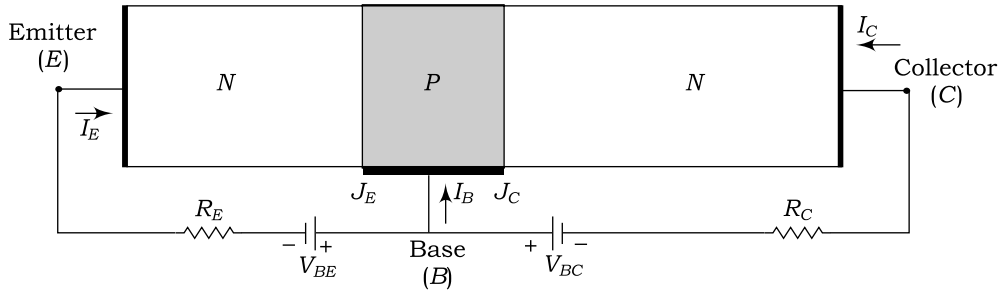


Fig. 2.71 Biasing of an NPN transistor

It is clear from Fig. 2.71 that the emitter current is

$$I_E = -(I_B + I_C)$$

The collector current I_C is equal to

$$I_C = \alpha_F I_E - I_R \tag{2.139}$$

where, α_F is the common-base current gain,
I_E is the emitter current, and
I_R is the base-collector current.

During the active mode, the base-collector junction is reverse biased, the above equation can be expressed as

$$I_C = \alpha_F I_E + I_{C0} \tag{2.140}$$

where, I_{C0} is the base-to-collector reverse saturation current.
The current I_E can be expressed as

$$I_E = I_{E0}\left(e^{\frac{eV_{BE}}{kT}} - 1\right) \tag{2.141}$$

In the saturation mode, the base-collector junction is forward biased, and the current I_R can be written as

$$I_R = I_{C0}\left(e^{\frac{eV_{BC}}{kT}} - 1\right) \tag{2.142}$$

After substituting the value I_E and I_R in Eq. (2.139), we get

$$I_C = \alpha_F I_{E0}\left(e^{\frac{eV_{BE}}{kT}} - 1\right) - I_{C0}\left(e^{\frac{eV_{BC}}{kT}} - 1\right) \tag{2.143}$$

The emitter current I_E is equal to

$$I_E = \alpha_R I_R - I_F$$

where, α_R is the common-base gain in the inverse mode, and

I_F is the emitter-base junction current.

After substituting the value of I_R and I_F in the above equation, we obtain

$$I_E = \alpha_R I_{C0}\left(e^{\frac{eV_{BC}}{kT}} - 1\right) - I_{E0}\left(e^{\frac{eV_{BE}}{kT}} - 1\right) \tag{2.144}$$

Equations (2.143) and (2.144) are the Ebers–Moll equations and the equivalent circuit of transistor is depicted in Fig. 2.72.

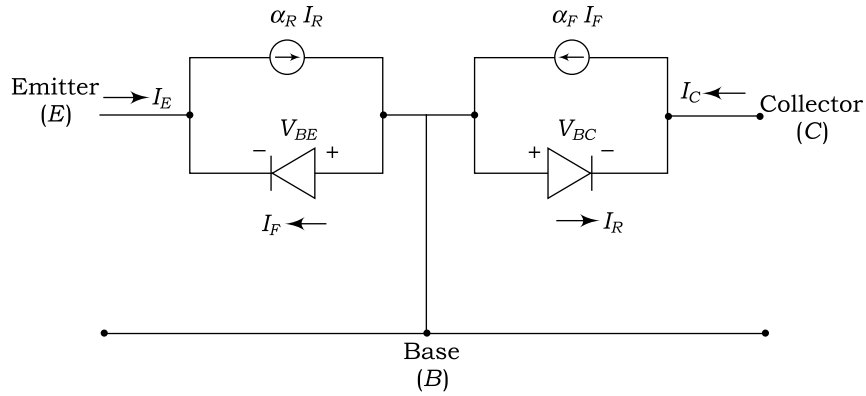


Fig. 2.72 Ebers–Moll equivalent circuit of an NPN transistor

The above equivalent circuit consists of two current sources and two ideal *PN*-junction diodes. Each current source depends on the voltage across the other junction. The parameters α_F α_R, I_{C0} and I_{E0} are dependent quantities and the relationship between them is

$$\alpha_R I_{C0} = \alpha_F I_{E0}$$

Usually, the values of parameters α_F, α_R, I_{C0} and I_{E0} are available in the manufacturer's data sheet. The Ebers–Moll model can be used to justify the three operating modes of a transistor. For example, in the saturation mode, the emitter-base and collector-base junctions are forward biased. The V_{BE} and V_{BC} are positive quantities in the above equations. The collector-emitter voltage at saturation, $V_{CE\text{sat}}$ is equal to

$$V_{CE.\text{sat}} = V_{BE} - V_{BC} \tag{2.145}$$

As $I_E = -(I_B + I_C)$, we can write

$$-(I_B + I_C) = \alpha_R I_{C0}\left(e^{\frac{eV_{BC}}{kT}} - 1\right) - I_{E0}\left(e^{\frac{eV_{BE}}{kT}} - 1\right) \tag{2.146}$$

By using the equations (2.145), (2.146), we can find the voltage V_{BE} and V_{BC} as follows:

$$V_{BE} = \frac{kT}{e}\ln\left[\frac{I_C(1-\alpha_R) + I_B + I_{E0}(1-\alpha_F\alpha_R)}{I_{E0}(1-\alpha_F\alpha_R)}\right] \tag{2.147}$$

$$V_{BC} = \frac{kT}{e}\ln\left[\frac{\alpha_F I_B - I_C(1-\alpha_F) + I_{C0}(1-\alpha_F\alpha_R)}{I_{C0}(1-\alpha_F\alpha_R)}\right] \tag{2.148}$$

After substituting the value of V_{BE} and V_{BC} in Eq. (2.145), we obtain

$$V_{CE}(sat) = \frac{kT}{e}\ln\left[\frac{I_C(1-\alpha_R)+I_B}{\alpha_F I_B - I_C(1-\alpha_F)} \times \frac{I_{C0}}{I_{E0}}\right]$$

or

$$V_{CE}(sat) = \frac{kT}{e}\ln\left[\frac{I_C(1-\alpha_R)+I_B}{\alpha_F I_B - I_C(1-\alpha_F)} \times \frac{\alpha_F}{\alpha_R}\right] \quad \text{as } \alpha_R I_{C0} = \alpha_F I_{E0} \tag{2.149}$$

Similarly, a *PNP* transistor consists of two interactive *PN*-junction diodes. The biasing arrangement of a *PNP* transistor is shown in Fig. 2.73(a) to understand the Ebers–Moll model of a *PNP* transistor. The Ebers–Moll model of a *PNP* transistor is depicted in Fig. 2.73(b). The different currents and voltages can also be derived for a *PNP* transistor just like an *NPN* transistor.

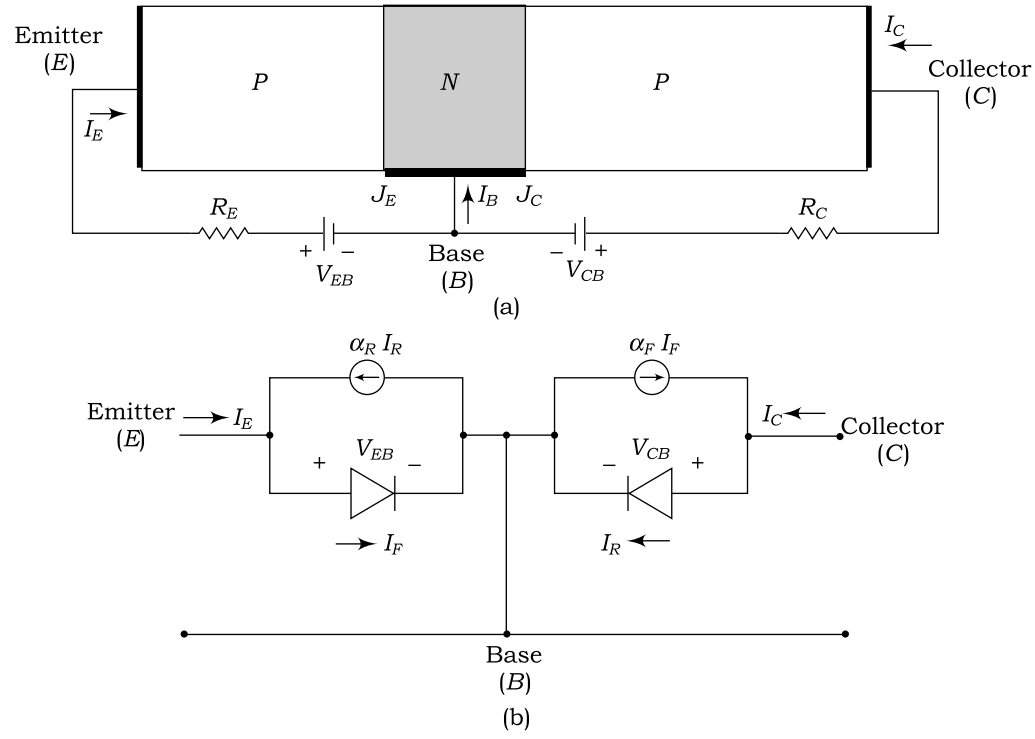


Fig. 2.73 (a) Biasing of a PNP transistor (b) Ebers–Moll equivalent circuit of a PNP transistor

2.29 HIGH-FREQUENCY MODEL OF TRANSISTOR

The Ebers–Moll model of a bipolar junction transistor does not include the junction capacitance. Therefore, this model cannot be used in analysis of transistors at high frequency. Figure 2.73 shows the hybrid-π model or Giacoletto model of a transistor in the common-emitter configuration. In this, Fig. 2.73 represents the external base terminal and B' is the virtual base terminal or the active internal terminal of the base region. The virtual base terminal is depicted in Fig. 2.74. The hybrid-π model of BJT is developed based on the following assumptions:

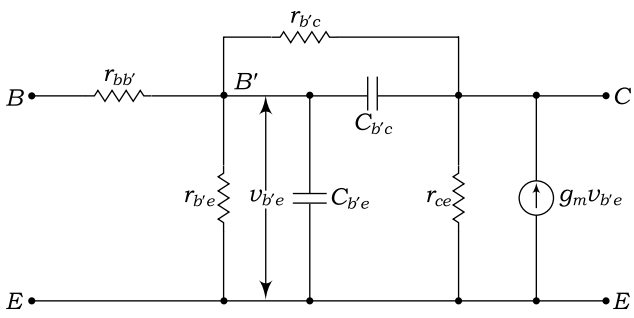


Fig. 2.73 Hybrid-π model of the bipolar junction transistor at high frequency

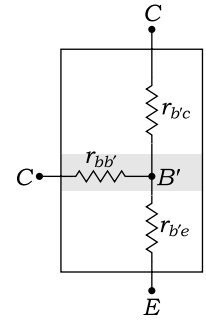


Fig. 2.74 BJT with *B*, *C*, *E* and *B′* terminals and $r_{bb'}$, $r_{b'e}$ and $r_{b'c}$ resistances

1. In this model, resistances and capacitances are frequency independent.
2. At a certain biasing condition, the values of resistances and capacitances do not change due to small signal variation.

- $r_{bb'}$—It is the base spreading resistance between the external base terminal B and the virtual base terminal B'. Its typical value is about 100 Ω.
- $r_{b'e}$—It is the resistance between the virtual base terminal B' and the emitter terminal E. Its typical value is about 1000 Ω.
- $r_{b'c}$—It is the resistance between the virtual base terminal B' and the collector terminal C. Its typical value is about 4 MΩ.
- $C_{b'e}$—It is the diffusion capacitance of the normally forward-biased base emitter junction. Actually, the excess minority carriers are stored in the base region and the diffusion capacitance exists between the base region B' and emitter E. Its typical value is about 100 pF.
- $C_{b'c}$—It is the transistor capacitance of the normally reverse-biased collector base junction. It is also known as the collector junction barrier capacitance. Its typical value is about 3 pF.
- r_{ce}—This is the resistance between the collector and emitter. Its typical value is about 80 kΩ.
- $g_m v_{b'e}$—The g_m is called the transconductance of the transistor. Any small change in $v_{b'e}$, the emitter-base junction generates a corresponding change in the small-signal collector current. This produces a current source and is represented by $g_m v_{b'e}$.

At low frequency, all capacitors ($C_{b'e}$ and $C_{b'c}$) are negligible. Then removing the $C_{b'e}$ and $C_{b'c}$, we obtain the hybrid-π model of the bipolar junction transistor at low frequency as shown in Fig. 2.75.

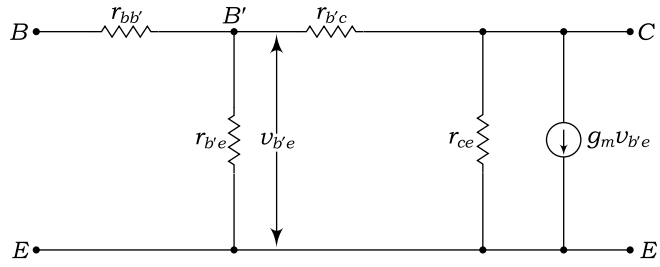


Fig. 2.75 Hybrid-π model of the bipolar junction transistor at low frequency

2.30 SPECIFICATION OF A TRANSISTOR

The most commonly used transistors are shown in Fig. 2.76. A transistor can always operate safely within certain limitations. These limitations are the maximum ratings of a transistor. During operation of a transistor, if the parameters are above the maximum ratings, the transistor will be damaged. Therefore, transistor manufacturers provide a datasheet for each transistor which contain all related specification of a transistor. As per the manufacturers data sheet, a transistor has the following ratings:

- Maximum collector current
- Maximum power dissipation
- Maximum output voltage

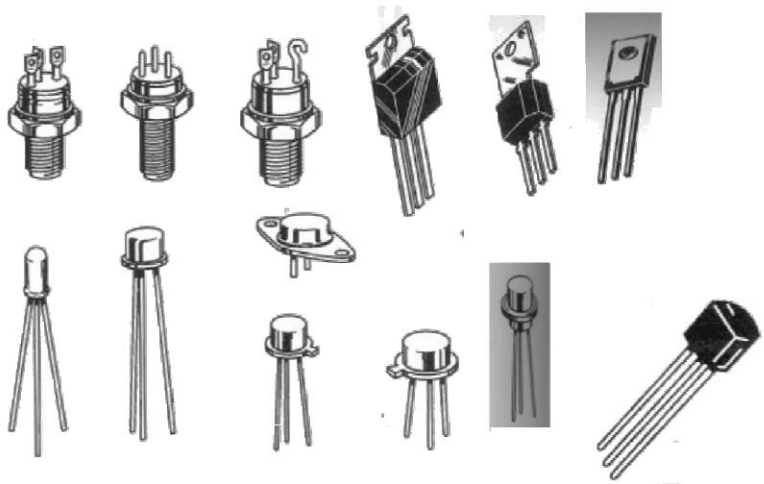


Fig. 2.76 Transistors

2.30.1 Maximum Collector Current

The transistor can operate at a maximum collector current $I_{C(\max)}$. When the collector current is greater than $I_{C(\max)}$, localised hot spots are developed within the transistor due to high current density at some unavoidable current path. For example, the maximum current rating of the transistor 2N3903 is about 200 mA.

2.30.2 Maximum Power Dissipation

The maximum power dissipation is used to indicate the limits of power-handling capacity of a transistor. Actually, power is dissipated in a transistor in its junctions. The power at the junction is the product of junction voltage and junction current. Usually, the J_E and J_C junctions have the same current, but the collector base junction voltage is higher than the emitter-base junction. Consequently, the power dissipation at collector-base junction is more than at emitter-base junction. The maximum power dissipation of a transistor can be expressed as

$$P_{D\max} = V_{CE} \times I_{C\max} = V_{CE\max} \times I_C \tag{2.150}$$

During proper operation of a transistor, the value of collector-to-emitter voltage (V_{CE}) and collector current (I_C) will not be maximum at the same time. Figure 2.77 shows the maximum power dissipation curve. In Fig. 2.77, $I_{C\max}$ is the maximum collector current limit which is *AB*. In the *CD* portion of the curve, the

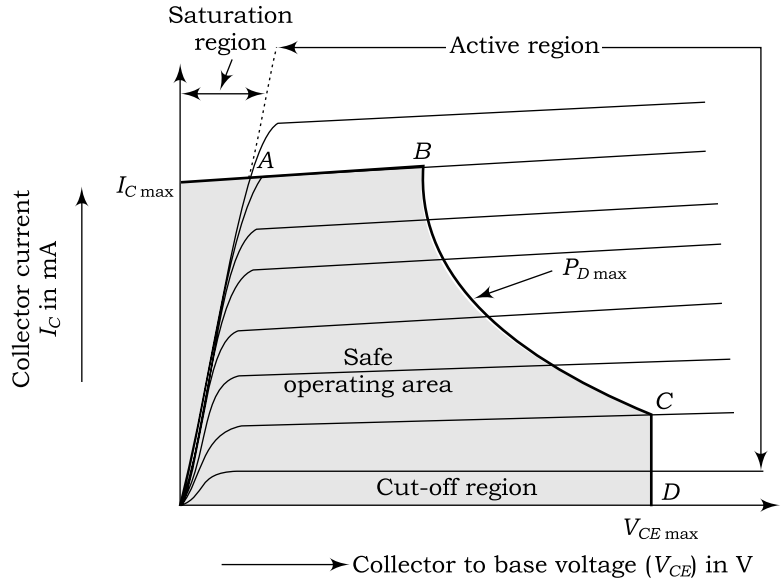


Fig. 2.77 Maximum power dissipation P_{Dmax} in a transistor

breakdown voltage of transistor is $V_{CE\,max}$. In the *BC* portion of the curve, the V_{CE} is less than $V_{CE\,max}$ and I_C is less than $I_{C\,max}$. As the power dissipation is $P_{Dmax} = V_{CE} \times I_C$, the transistor can operate safely. Hence, the safe operating area is *ABCD* as depicted in Fig. 2.75. For example, the maximum power dissipation of the transistor 2N3903 is about 350 mW.

2.30.3 Maximum Output Voltage

Usually, the collector-base junction of a transistor can withstand high voltage. However, there is some possibility of voltage breakdown of a bipolar junction transistor at high voltage. As a result, it is required to specify the maximum collector-base voltage or collector-emitter voltage or both. Generally, the voltage breakdown can happen in two different ways such as *avalanche breakdown* and *punch-through*.

1. Avalanche Breakdown

When a voltage is applied across a *PN*-junction, the electrons and holes in the semiconductors are energised and accelerated with the applied voltage. Then the accelerated electrons and holes collide with atoms and generate more free electrons. Again, these free electrons are accelerated and collide with atoms and generate more free electrons. As this process continues, the current increase rapidly and its value is

$$M \times I_{C0} \tag{2.151}$$

where, M is the multiplication factor and it is equal to

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CB0}} \right)^n} \tag{2.152}$$

where, V_{CB} is the voltage between the collector and base,
BV_{CB0} is the applied voltage between the collector and base terminals just before breakdown, and n is in the range of 3 to 10.

As the current rises abruptly, there is a large change in current with very small change in voltage and junction breakdown occurs.

When an emitter current I_E flows across the emitter junction and the avalanche effect is neglected, αI_E current can reach to the collector junction. After considering multiplication into account, the collector current becomes $M\alpha I_E$. Due to presence of avalanche multiplication, the transistor behaves as common-base and its current gain is $M\alpha$.

The avalanche breakdown for the common-emitter configuration represents that the collector to emitter breakdown voltage is BV_{CE0} when the base is an open circuit. The value of BV_{CE0} is

$$BV_{CE0} = BV_{CB0}\left(\frac{1}{h_{fe}}\right)^{\frac{1}{n}} \tag{2.153}$$

For example, if $n = 6$ and $h_{fe} = 50$ for a germanium transistor, the voltage BV_{CE0} is equal to

$$BV_{CE0} = 0.52 \times BV_{CB0}$$

If BV_{CB0} of a transistor is about 50 V, BV_{CE0} of a transistor is about 26 V which is half of the BV_{CB0}. Figure 2.78 shows the common-emitter characteristics extended into the breakdown region.

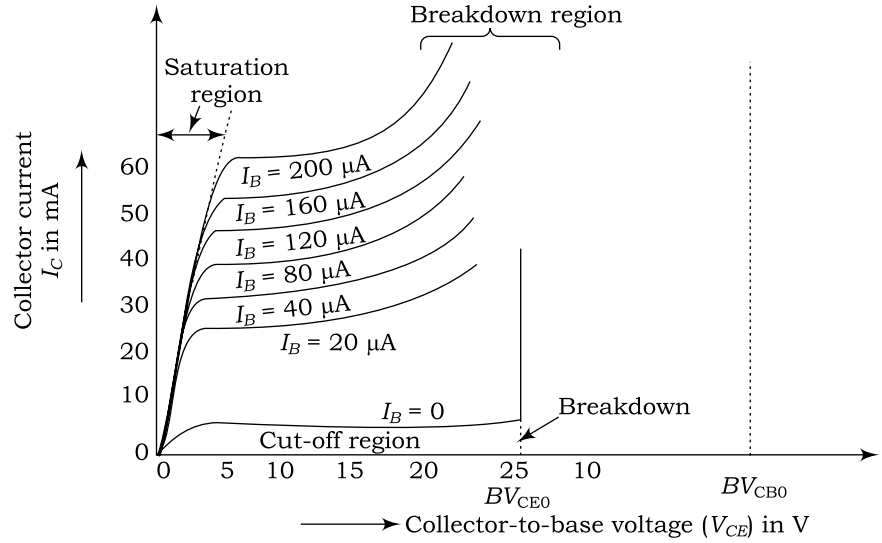


Fig. 2.78 Output characteristics of a collector-emitter configuration of a transistor extended into the breakdown region.

3. Punch-Through

When the reverse-bias voltage is applied across the collector-base junction, the width of the depletion layer in the collector-base junction is increased significantly. If the applied voltage across the junction increases, the depletion region can penetrate deeper into the base region. As the base is thin compared to the emitter and collector, the depletion region can spread completely across the base region and can reach the emitter-base junction. Therefore, the current increases very rapidly to a large value. Punch-through takes place at a fixed voltage across the collector and base and it does not dependent on the circuit configuration.

2.30.4 Thermal Runaway and Heat Sink

The reverse saturation current of a transistor changes with temperature. Actually, the reverse saturation current I_{C0} doubles for each 10°C increase in temperature. Due to this, it is a most practical difficulty to use a transistor as an amplifier. Whenever the temperature of the collector-base junction increases, the leakage current of the transistor also increases. Hence, the collector current I_C also increases. Due to increase in collector current, the power dissipation at the collector-base junction increases. Consequently, the temperature of the collector-base junction further increases and subsequently the collector current I_C also increases. If this cumulative process will continue, the ratings of the transistor may be exceeded. When the above process continues, the transistor may be burnt out and completely damaged. This process is known as *thermal runaway* of a transistor. Practically, thermal runaway should be avoided by using temperature-controlling circuits with transistor. Usually, heat sinks are used to control the temperature of a transistor.

Figure 2.79 shows the basic structure of heat sinks. Generally, a heat sink is a metallic heat-conducting device which is used in close contact with a transistor to increase the power-dissipation capacity of a transistor. For small-signal operation, there is no need of heat sink. For power applications, power transistors are used and heat sinks are very essential. For a low power transistor, fin-type heat sink is commonly used. For a high-power transistor, a rectangular heat sink is used.

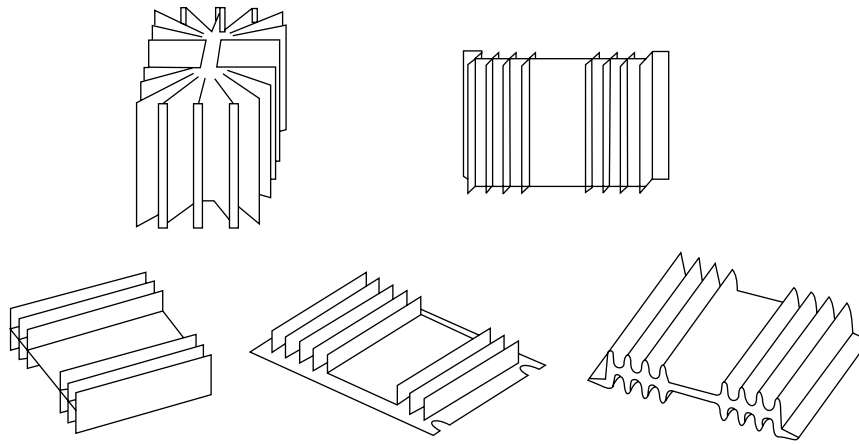


Fig. 2.79 Basic structures of heat sinks

Assume that a transistor is used in an electronic circuit where the ambient temperature of air around the transistor is T_A°C and the collector-base junction of the transistor is T_J°C. Since the transistor is operating in the circuit, heat is generated within the transistor and T_J is greater than T_A. The temperature difference $(T_J - T_A)$ is directly proportional to the power dissipation within transistor P_D and it is given by

$$(T_J - T_A) \propto P_D$$

or

$$(T_J - T_A) = R_\Theta P_D$$

where, R_Θ is the proportionality constant and it known as *thermal resistance*.

or

$$R_\Theta = \frac{(T_J - T_A)}{P_D} \tag{2.154}$$

Hence, R_Θ is measured in °C/W and its value is varies from 0.2 °C/W to 1000 °C/W.

In small-signal amplifier circuits, a transistor is used as low power device and no cooling is required. In large signal amplifier circuits, power transistors are used and heat sink is required for cooling. Figure 2.80(a) shows steady-state heat flow from junction to heat sink and the thermal resistance when a transistor mounted on a heat sink is depicted in Fig. 2.80(b).

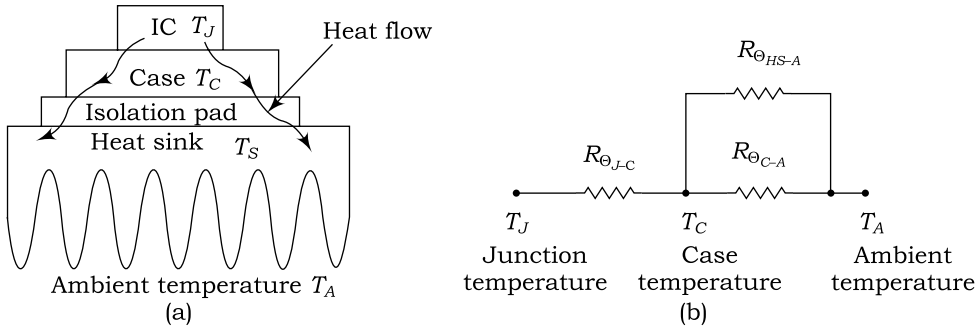


Fig. 2.80 (a) Steady-state heat flow from junction to heat sink (b) Thermal resistance when a transistor is mounted on a heat sink

The thermal resistance from junction to ambiance $R_{\Theta_{J-A}}$ is the sum of thermal resistance from junction to case $R_{\Theta_{J-C}}$ and thermal resistance from case to ambiance $R_{\Theta_{C-A}}$, i.e.,

$$R_{\Theta_{J-A}} = R_{\Theta_{J-C}} + R_{\Theta_{C-A}}$$

Then power dissipation is equal to

$$P_D = \frac{(T_J - T_A)}{R_{\Theta_{J-A}}} = \frac{(T_J - T_A)}{R_{\Theta_{J-C}} + R_{\Theta_{C-A}}} \tag{2.155}$$

$R_{\Theta_{J-C}}$ depends on the manufacture of a transistor and $R_{\Theta_{C-A}}$ depends on surface area of the case and its contact with air. When the effective surface area of a transistor is increased, the resistance to heat flow $R_{\Theta_{C-A}}$ decreases. This is possible by using a heat sink. Different types of heat sinks depending upon the shape and size are used for transistors. When heat sink size is large, thermal resistance $R_{\Theta_{HS-A}}$ is small. This thermal resistance $R_{\Theta_{HS-A}}$ is not added in with the thermal resistance from case to ambiance $R_{\Theta_{C-A}}$, but it is parallel with $R_{\Theta_{C-A}}$. Therefore, effective value of $R_{\Theta_{C-A}} || R_{\Theta_{HS-A}}$ is significantly small value, and thermal resistance from junction to ambiance is equal to $R_{\Theta_{J-A}} = R_{\Theta_{J-C}} + R_{\Theta_{C-A}} || R_{\Theta_{HS-A}}$ and the power dissipation capability of transistor increases.

Example 2.28 In a transistor amplifier circuit, the thermal resistance is 5°C/W and the ambient temperature T_A is 35°C. When the transistor dissipates 5 W of power, determine the junction temperature.

Sol. Given $T_A = 35°C$, $R_\Theta = 5°C/W$, $P_D = 5$ W

We know that $(T_J - T_A) = R_\Theta P_D$

Then junction temperature $T_J = T_A + R_\Theta P_D = 35 + 5 \times 5°C = 60°C$

Example 2.29 For a transistor, the thermal resistance is 50°C/W and the ambient temperature T_A is 25°C, junction temperature T_J is 150°C. Calculate the power that the transistor can dissipate.

Sol. Given $T_A = 25°C$, $T_J = 150°C$, $\Theta = 50°C/W$, $P_D = ?$

We know that $(T_J - T_A) = R_\Theta P_D$

Then, $P_D = \frac{(T_J - T_A)}{R_{\Theta_{J-A}}} = \frac{150 - 25}{50} = 2.5$ W

Example 2.30 Calculate the power-dissipation capability of a transistor, which is mounted on a heat sink. Assume $T_A = 35°C$, $T_J = 250°C$, $R_{\Theta_{J-C}} = 15°C/W$, $R_{\Theta_{C-A}} = 75°C/W$ and $R_{\Theta_{HS-A}} = 10°C/W$.

Sol. Given: $T_A = 35°C$, $T_J = 250°C$, $R_{\Theta_{J-C}} = 15°C/W$, $R_{\Theta_{C-A}} = 75°C/W$ and $R_{\Theta_{HS-A}} = 10°C/W$

$$R_{\Theta_{J-A}} = R_{\Theta_{J-C}} + R_{\Theta_{C-A}} \| R_{\Theta_{HS-A}} = 15 + 75 \| 10 = 15 + \frac{75 \times 10}{75 + 10} = 23.82\,°C/W$$

Then, $P_D = \dfrac{(T_J - T_A)}{R_{\Theta_{J-A}}} = \dfrac{250 - 35}{23.82} = 9.02$ W

Example 2.31 What is β_{dc} of BJT if $I_C = 20.5$ mA and $I_E = 20.8$ mA? What is α_{dc} if $I_C = 5.35$ mA and $I_B = 50$ μA?

Sol. When $I_C = 20.5$ mA and $I_E = 20.8$ mA, $\beta_{dc} = \dfrac{I_C}{I_B} = \dfrac{I_C}{I_E - I_C} = \dfrac{20.5\text{ mA}}{(20.8 - 20.5)\text{ mA}} = 68.333$

When $I_C = 5.35$ mA and $I_B = 50$ μA, $\beta_{dc} = \dfrac{I_C}{I_B} = \dfrac{5.35 \times 10^{-3}}{50 \times 10^{-6}} = 107$ and $\alpha_{dc} = \dfrac{\beta_{dc}}{1 + \beta_{dc}} = \dfrac{107}{1 + 107} = 0.99$

Example 2.32 Determine whether or not the transistor shown in Fig. 2.81 is in saturation. Assume $V_{CE(sat)} = 0.2$ V

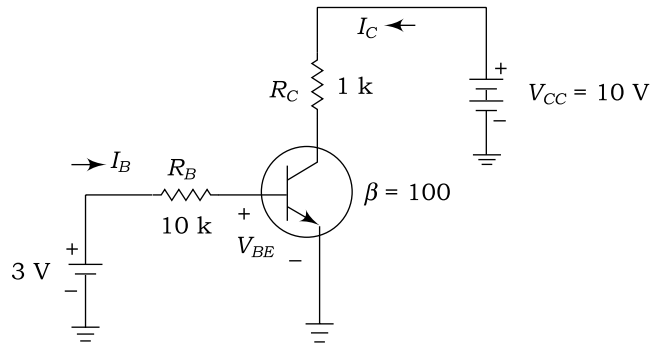


Fig. 2.81

Sol. Given: $V_{CC} = 10$ V, $V_{CE(sat)} = 0.2$ V, $\beta = 100$, $R_C = 1$ kΩ, $R_B = 10$ kΩ

Applying KVL in the collector loop, we get $V_{CC} = I_{C(sat)}R_C + V_{CE(sat)}$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10 - 0.2}{1 \times 10^3} = 9.8 \times 10^{-3}\,\text{A} = 9.8\text{ mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta} = \frac{9.8\text{ mA}}{100} = 98\,\mu\text{A}$$

Applying KVL to the base loop, we obtain $3 = I_BR_B + V_{BE(sat)}$

$$I_B = \frac{3 - V_{BE(sat)}}{R_B} = \frac{3 - 0.8}{10 \times 10^3} = 220\,\mu\text{A}.\ \text{Assume}\ V_{BE(sat)} = 0.8\text{ V}$$

Since base current I_B is greater than $I_{B(min)}$, the transistor operates in saturation.

Example 2.33 Determine I_B, I_C, I_E, V_{CE} in the circuit of Fig. 2.82, where the transistor has a $\beta = 150$. Assume $V_{BE} = 0.7$ V.

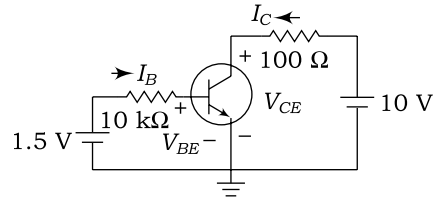


Fig. 2.82

Sol. Applying KVL in the base-emitter loop, we get $1.5 = 10\ \text{k}\Omega \times I_B + V_{BE}$

$$I_B = \frac{1.5 - V_{BE}}{10 \times 10^3} = \frac{1.5 - 0.7}{10 \times 10^3} = 80\ \mu\text{A}$$

$$I_C = \beta I_B = 150 \times 80 \times 10^{-6}\ \text{A} = 12\ \text{mA}$$

$$I_E = I_C + I_B = 12\ \text{mA} + 80\ \mu\text{A} = 12\ \text{mA} + 0.08\ \text{mA} = 12.08\ \text{mA}$$

Applying KVL in the collector loop, we obtain

$$10 = 100 I_C + V_{\text{CE}} \text{ or } V_{CE} = 10 - 100 I_C = 10 - 100 \times 12 \times 10^{-3} = 8.8\ \text{V}$$

Example 2.34 Calculate the values of I_C and I_E for a BJT with $\alpha_{\text{dc}} = 0.97$ and $I_B = 50\ \mu\text{A}$. Determine β_{dc} of the device.

Sol.
$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.97}{1 - 0.97} = 32.333$$

$$I_C = \beta I_B = 32.333 \times 50 \times 10^{-6}\ \text{A} = 1.6166\ \text{mA}$$

$$I_E = \frac{I_C}{\alpha} = \frac{1.6166}{0.97}\ \text{mA} = 1.6665\ \text{mA}$$

Example 2.35 Determine the coordinates of operating point for the circuit shown in Fig. 2.83.

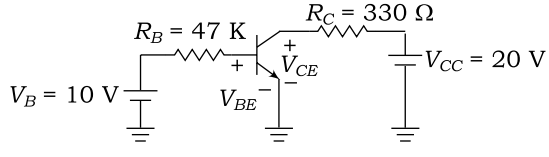


Fig. 2.83

Sol. Applying KVL to the base loop, we get

$$V_B = I_B R_B + V_{BE} \text{ or } I_B = \frac{V_B - V_{BE}}{R_B} = \frac{10 - 0.7}{47 \times 10^3} = 0.19787 \times 10^{-3}\ \text{A} = 197.87\ \mu\text{A}$$

$$I_{CQ} = \beta I_B = 100 \times 197.87 \times 10^{-6}\ \text{A} = 19.787\ \text{mA}$$

Applying KVL to the collector loop, we obtain

$$V_{CC} = I_C R_C + V_{CEQ} \text{ or } V_{CEQ} = V_{CC} - I_{CQ} R_C = 20 - 19.787 \times 10^{-3} \times 330 = 13.47$$

The coordinates of the operating Q-point = (13.47 V, 19.787 mA)

Example 2.36 For a transistor in common-emitter configuration, the reverse leakage current is 21μA, whereas when the same transistor is connected in common-base configuration, it reduces to 1.1 μA. Calculate values of α_{dc} and β_{dc} of the transistor.

Sol. Given: I_{CEO} = 21 μA, I_{CBO} = 1.1 μA

We know that $I_{CEO} = (1 + \beta_{dc})I_{CBO}$. Then $\beta_{dc} = \dfrac{I_{CEO}}{I_{CBO}} - 1 = \dfrac{21\,\mu A}{1.1\,\mu A} - 1 = 18.09$

Example 2.37 Calculate the α_{dc} and β_{dc} for the given transistor for which I_C = 5 mA, I_B = 50 μA and I_{CO} = 1 μA

Sol. Given: I_C = 5 mA, I_B = 50 μA and I_{CO} = 1 μA

We know that $I_C = \beta_{dc} I_B + (1 + \beta_{dc})I_{CO}$ or

$$\beta_{dc} = \frac{I_C - I_{CO}}{I_B + I_{CO}} = \frac{5\times10^{-3} - 1\times10^{-6}}{50\times10^{-6} + 1\times10^{-6}} = 98.01$$

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{98.01}{1+98.01} = 0.9899$$

Example 2.38 For the circuit shown in Fig. 2.84, calculate the minimum and maximum value of emitter current when β of the transistor varies from 75 to 150. Also, calculate the corresponding values of collector-to-emitter voltage. Take V_{BE} = 0.3 V, R_B = 10 kΩ, R_C = 50 Ω, R_B = 100 Ω, V_{CC} = +6 V

Sol. Apply KVL to the base loop, we obtain $V_{CC} = I_B R_B + V_{BE} + I_E R_E$

Since $I_E = (\beta + 1)I_B$, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$

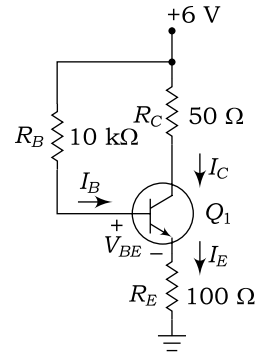


Fig. 2.84

At $\beta = 75$, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} = \dfrac{6 - 0.3}{10\times10^3 + (75+1)\times100} = 0.323$ mA

$I_C = \beta I_B = 75 \times 0.323$ mA = 24.225 mA

$I_E = (\beta + 1)I_B = (75 + 1) \times 0.323$ mA = 24.548 mA

Therefore, $I_{E(min)}$ = 24.548 mA

Applying KVL in the collector loop, we get $V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6 - 24.225\times10^{-3}\times50 - 24.548\times10^{-3}\times100 = 2.333 \text{ V}$$

At $\beta = 150$, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} = \dfrac{6 - 0.3}{10\times10^3 + (150+1)\times100} = 0.227$ mA

$I_C = \beta I_B = 150 \times 0.227$ mA = 34.05 mA

$I_E = (\beta + 1)I_B = (150 + 1) \times 0.227$ mA = 34.227 mA

Therefore, $I_{E(max)}$ = 34.227 mA

Applying KVL in the collector loop, we get $V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6 - 34.05\times10^{-3}\times50 - 34.227\times10^{-3}\times100 = 0.8698 \text{ V}$$

Example 2.39 A silicon transistor with $V_{BE(sat)} = 0.8$ V, $\beta = h_{FE} = 100$, $V_{CE(sat)} = 0.2$ V is used in the circuit shown in Fig. 2.85. Find the minimum value of R_C for which the transistor remains in saturation.

Sol. Given: $V_{BE(sat)} = 0.8$ V, $\beta = h_{FE} = 100$, $V_{CE(sat)} = 0.2$ V

Apply KVL to the base loop, we obtain $5 = I_B \times 200 \times 10^3 + V_{BE}$

$$I_B = \frac{5 - 0.8}{200 \times 10^3} = 0.021 \text{ mA}$$

$$I_{C(sat)} = \beta I_B = 100 \times 0.021 \text{ mA} = 2.1 \text{ mA}$$

Applying KVL in the collector loop, we get $V_{CC} = I_{C(sat)} R_C + V_{CE(sat)}$

$$R_C = \frac{V_{CC} - V_{CE(sat)}}{I_{C(sat)}} = \frac{10 - 0.2}{2.1 \times 10^{-3}} = 4.6667 \text{ k}\Omega$$

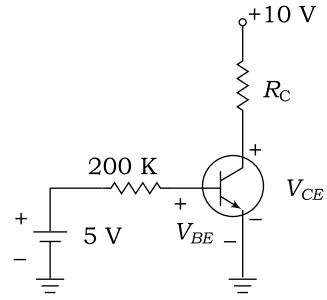


Fig. 2.85

Example 2.40 The fixed-bias circuit is given in Fig. 2.86 and it is subjected to an increase in temperature from 25°C to 75°C. If $\beta = 100$ at 25°C and $\beta = 125$ at 75°C, determine the percentage change in Q-point values (V_{CE}, I_C) over the temperature range. Neglect any change in V_{BE}. Take $V_{BE} = 0.7$ V.

Sol. At 25°C, $\beta_{25} = 100$. At 75°C, $\beta_{75} = 125$, $V_{BE} = 0.7$ V

Applying KVL to the base loop, we obtain $V_{CC} = I_B R_B + V_{BE}$

At 25°C, the base current $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{12 - 0.7}{100 \times 10^3} = 0.113 \text{ mA}$

The collector current $I_C = \beta_{25} I_B = 100 \times 0.113 = 11.3 \text{ mA}$

Applying KVL in the collector loop, we get $V_{CC} = I_C R_C + V_{CE}$

$$V_{CE} = V_{CC} - I_C R_C = 12 - 11.3 \times 10^{-3} \times 600 = 5.22 \text{ V}$$

The Q-point at 25°C is (5.22 V, 11.3 mA)

At 75°C, the base current $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{12 - 0.7}{100 \times 10^3} = 0.113 \text{ mA}$

The collector current $I_C = \beta_{75} I_B = 125 \times 0.113 = 14.125 \text{ mA}$

Applying KVL in the collector loop, we get $V_{CC} = I_C R_C + V_{CE}$

$$V_{CE} = V_{CC} - I_C R_C = 12 - 14.125 \times 10^{-3} \times 600 = 3.525 \text{ V}$$

The Q-point at 75°C is (3.525 V, 14.125 mA)

The percentage change in Q-point values (V_{CE}, I_C)

$$\text{The percentage change in } I_{CQ} = \frac{I_C(75°\text{C}) - I_C(25°\text{C})}{I_C(25°\text{C})} = \frac{14.125 - 11.3}{11.3} \times 100\% = 25\%$$

$$\text{The percentage change in } V_{CE} = \frac{V_{CE}(75°\text{C}) - V_{CE}(25°\text{C})}{V_{CE}(25°\text{C})} = \frac{3.525 - 5.22}{5.22} \times 100\% = -32.47\%$$

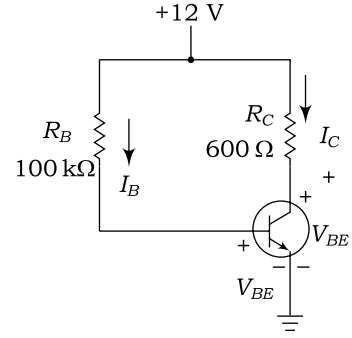


Fig. 2.86

Example 2.41 Determine whether or not the transistor as shown in Fig. 2.87 in circuit is in saturation. Assume $\beta = 50$ and $V_{CE(sat)} = 0.3$ V, $V_{BE} = 0.7$ V

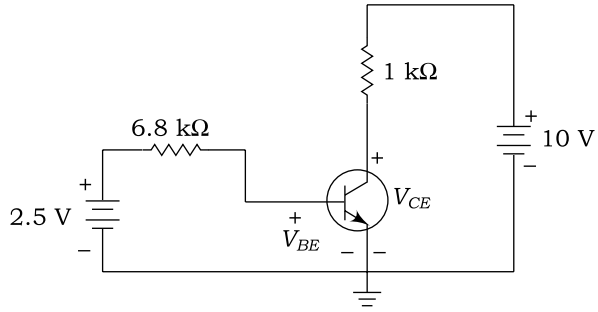


Fig. 2.87

Sol. Given: $\beta = 50$, $V_{CE(sat)} = 0.3$ V, and $V_{BE} = 0.7$ V

Applying KVL in the collector loop, we get $V_{CC} = I_{C(sat)}R_C + V_{CE(sat)}$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10 - 0.3}{1 \times 10^3} = 9.7 \text{ mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta} = \frac{9.7 \times 10^{-3}}{50} = 0.194 \text{ mA}$$

Applying KVL in the base loop, we obtain $V_B = I_B R_B + V_{BE}$

$$2.5 = I_B \times 6.8 \times 10^3 + 0.7 \text{ or, } I_B = \frac{2.5 - 0.7}{6.8 \times 10^3} = 0.2647 \text{ mA}$$

As the base current $I_B > I_{B(min)}$, the transistor operates in saturation.

Example 2.42 Design a fixed circuit using a silicon *NPN* transistor (Fig. 2.88) which has $\beta_{dc} = 150$. The dc biasing point is at $V_{CE} = 5$ V and $I_C = 5$ mA. Supply voltage is 10 volts.

Sol. Given: $V_{CC} = 10$ V, $\beta_{dc} = 150$, $V_{BE} = 0.7$ V, $V_{CEQ} = 5$ V and $I_C = 5$ mA. Supply voltage is 10 volts.

$$I_B = \frac{I_{CQ}}{\beta_{dc}} = \frac{5 \text{ mA}}{150} = 33.333 \text{ μA}$$

Applying KVL to the collector loop, we get

$$V_{CC} = I_{CQ}R_C + V_{CEQ}$$

Resistance $R_C = \dfrac{V_{CC} - V_{CEQ}}{I_{CQ}} = \dfrac{10 - 5}{5 \times 10^{-3}} = 1000 \text{ Ω}$

Applying KVL to the base loop, we get $V_{CC} = I_B R_B + V_{BE}$

Resistance $R_B = \dfrac{V_{CC} - V_{BE}}{I_B} = \dfrac{10 - 0.7}{33.3333 \times 10^{-6}} = 279 \text{ kΩ}$

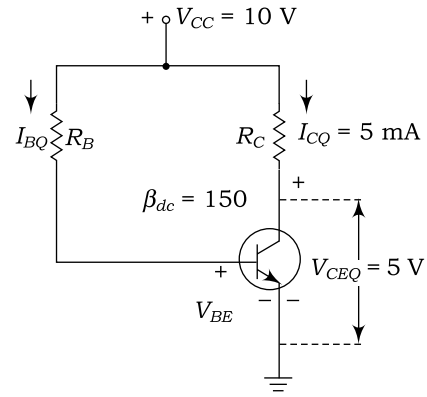


Fig. 2.88

Transistor will be selected for the following specification:

$$\beta_{dc} = 150, I_C = 5 \text{ mA}, I_{C(max)} = 2 \times I_{CQ} = 2 \times 5 = 10 \text{ mA}$$

$$V_{CE(max)} = 2 \times V_{CEQ} = 2 \times 5 = 10 \text{ V}, P_{D(max)} = 2 \times V_{CE(max)} \times I_{C(max)} = 2 \times 10 \times 10 \times 10^{-3} = 200 \text{ mW}$$

Example 2.43 For the circuit shown below, determine I_B, I_{CQ}, V_E, V_{CEQ} and V_B where symbols denote their usual meaning.

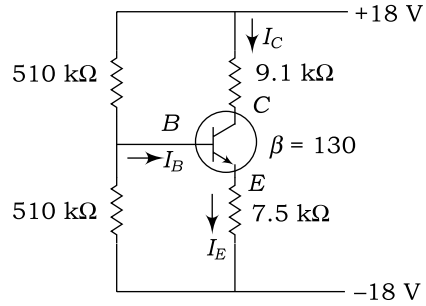


Fig. 2.89(a)

Sol. Given: $R_1 = R_2 = 510$ kΩ, $R_C = 9.1$ kΩ, $R_E = 7.5$ kΩ, $+V_{CC} = +18$ V, $-V_{CC} = -18$ V

$$R_{eq} = R_{th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{510 \times 510}{510 + 510}\text{k}\Omega = 255\ \text{k}\Omega$$

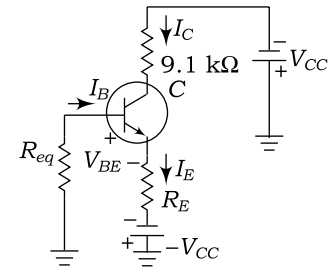


Fig. 2.89(b)

Figure 2.89(b) shows the equivalent circuit of Fig. 2.89(a).

Applying KVL loop to the base, we write

$$-R_{eq} I_B - V_{BE} - (\beta + 1) I_B R_E + V_{CC} = 0$$

or $$-255 \times 10^3 I_B - 0.7 - (130 + 1) I_B \times 7.5 \times 10^3 + 18 = 0$$

or $$I_B (255 \times 10^3 + 131 \times 7.5 \times 10^3) = 18 - 0.7$$

Therefore, $$I_B = \frac{18 - 0.7}{255 \times 10^3 + 131 \times 7.5 \times 10^3} = 0.013979 \times 10^{-3}\ \text{A} = 0.013979\ \text{mA}$$

$$I_C = \beta I_B = 130 \times 0.013979\ \text{mA} = 1.8173\ \text{mA}$$

$$V_E = -V_{CC} + I_C \times 7.5\ \text{k}\Omega = -18 + 1.8173 \times 10^{-3} \times 7.5 \times 10^3 = -4.37\ \text{V}$$

Applying KVL loop to the collector, we obtain

$$+18 - I_C R_C - V_{CE} - I_C \times 7.5 \times 10^3 + 18 = 0$$

or $$+18 - 1.8173 \times 10^{-3} \times 9.1 \times 10^3 - V_{CE} - 1.8173 \times 10^{-3} \times 7.5 \times 10^3 + 18 = 0$$

Therefore, $V_{CE} = 5.84$ V and $V_B = I_B R_{eq} = 0.013979 \times 10^{-3} \times 255 \times 10^3 = 3.57$ V

Example 2.44 Find Q-point of the fixed-bias circuit (Fig. 2.90) having Si transistor with dc bias $\beta = 50$. Assume $V_{BE} = 0.6$ V

Sol. Applying KVL in the base loop, we get $V_{CC} - I_B R_B - V_{BE} = 0$

Therefore, $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{9 - 0.6}{270 \times 10^3} = 31.11\ \mu\text{A}$$

$$I_C = \beta I_B = 50 \times 31.11\ \mu\text{A} = 1555.5\ \mu\text{A}$$

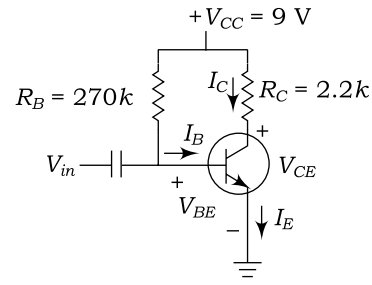


Fig. 2.90

Applying KVL at the collector loop, we obtain $V_{CC} - I_C R_C - V_{CE} = 0$

Therefore, $V_{CE} = V_{CC} - I_C R_C = 9 - 1555.5 \times 10^{-6} \times 2.2 \times 10^3 = 5.5779$ V

The Q-point is (5.5779 V,1.5555 mA)

Example 2.45 In the above circuit (Fig. 2.91), how does the Q-point vary when emitter resistance is increased from zero ohm to 1.5 kΩ?

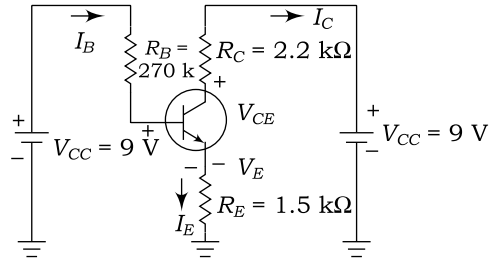


Fig. 2.91

Sol. Applying KVL in the base loop, we obtain

$$V_{CC} - I_B R_B - V_{BE} - V_E = 0 \text{ or } V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \text{ as } V_E = I_E R_E$$

or $$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0 \text{ as } I_E = (1 + \beta) I_B$$

Therefore, $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} = \frac{9 - 0.6}{270 \times 10^3 + (50 + 1) \times 1.5 \times 10^3} = \frac{8.4}{346.5 \times 10^3} = 0.02424 \text{ mA}$$

Then $$I_C = \beta I_B = 50 \times 0.02424 \text{ mA} = 1.212 \text{ mA}$$

Applying KVL in the collector loop, we get

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

Assume $I_E \approx I_C$,

or, $$V_{CE} = V_{CC} - I_C (R_B + R_E) = 9 - 1.212 \times 10^{-3} (2.2 \times 10^3 + 1.5 \times 10^3) \text{ V} = 4.5156 \text{ V}$$

The Q-point values are (V_{CEQ}, I_{CQ}) = (4.5156 V, 1.212 mA)

Example 2.46 Determine V_{CE} for the following voltage-divider bias configuration (Fig. 92). Take $\beta = 120$.

Sol. Given V_{BE} = 0.7 V, V_{CC} = –18 V, R_C = 2.4 kΩ, R_E = 1.1 kΩ,

Voltage across 10 kΩ is $$V_2 = \frac{10}{47 + 10} \times -18 \text{ V} = -3.1578 \text{ V}$$

Current $$I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{3.1578 - 0.7}{1.1 \times 10^3} = 2.234 \text{ mA}$$

At dc operating point $I_C = I_E$ = 2.234 mA

The collector-emitter voltage

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= -18 + 2.234 \times 10^{-3} (2.4 + 1.1) \times 10^3 = -10.181 \text{ V}$$

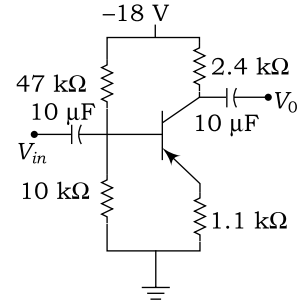


Fig. 2.92

Example 2.47 Determine the voltage gain of the following circuit (Fig. 2.93). Assume $\beta = 100$.

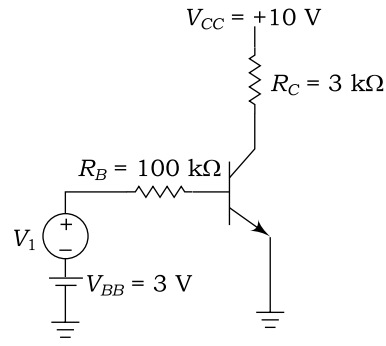


Fig. 2.93

Sol. Given: $V_{BB} = 3$ V, $V_{BE} = 0.7$ V, $R_B = 100$ kΩ, $R_C = 3$ kΩ

Base current $I_B = \dfrac{V_{BB} - V_{BE}}{R_B} = \dfrac{3 - 0.7}{100 \times 10^3} = 0.023$ mA

Current $I_C = \beta I_B = 100 \times 0.023$ mA $= 2.3$ mA

Voltage $V_{CE} = V_{CC} - I_C R_C = 10 - 2.3 \times 10^{-3} \times 3 \times 10^3 = 3.1$ V

Voltage gain = $A_v = \beta \dfrac{R_C}{R_B} = 100 \times \dfrac{3 \times 10^3}{100 \times 10^3} = 3$

Example 2.48 The following measurements were made in a transistor connected in a circuit: $I_C = 10.525$ mA, $I_B = 100$ μA and $I_{CB0} = 5$ μA. Find the values for α_{dc}, β_{dc}

Sol. Given: $I_C = 10.525$ mA, $I_B = 100$ μA

Current $I_E = I_C + I_B = 10.525 \text{ mA} + 100 \text{ μA} = 10.625 \text{ mA}$

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{10.525 \text{ mA}}{10.625 \text{ mA}} = 0.99$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.99}{1 - 0.99} = 99$$

Example 2.49 In a *CE* transistor, if the base current in a transistor is 0.01 mA and emitter current is 1 mA, calculate the values of α and β.

Sol. Given $I_B = 0.01$ mA, $I_E = 1$ mA, $I_C = I_E - I_B = 1$ mA $- 0.01$ mA $= 0.99$ mA

$$\beta = \frac{I_C}{I_B} = \frac{0.99}{0.01} = 99$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{0.99 \text{ mA}}{1 \text{ mA}} = 0.99 \text{ or } \alpha = \frac{\beta}{1 + \beta} = \frac{99}{1 + 99} = 0.99$$

Example 2.50 Calculate $A_i = \dfrac{I_o}{I_i}$, A_v, A_{vs} and R_i for an amplifier circuit shown in Fig. 2.94 for which the *h*-parameters are $h_{ie} = 1100\ \Omega$, $h_{re} = 0$, $h_{fe} = 50$ and $\dfrac{1}{h_{oe}} = 0$

Sol. The small-signal equivalent circuit of Fig. 2.94 is depicted in Fig. 2.95.

Current gain $A_i = h_{fe} = 50$

Input resistance $R_i = h_{ie} + (1 + h_{fe}) R_E = 1.1k + (1 + 50) \times 1k = 52.1k$

$$R_{th} = 100k \,||\, 10k = 9.09k$$

$$R_i' = R_i \,||\, R_{th} = 52.1 \,||\, 9.09k = 7.739k$$

The voltage gain is $A_v = A_i \dfrac{R_L}{R_i} = 50 \times \dfrac{5}{52.1} = 4.798$

$$A_{VS} = A_v \frac{R_i'}{R_i' + R_s} = 4.798 \times \frac{7.739}{7.739 + 10} = 2.093$$

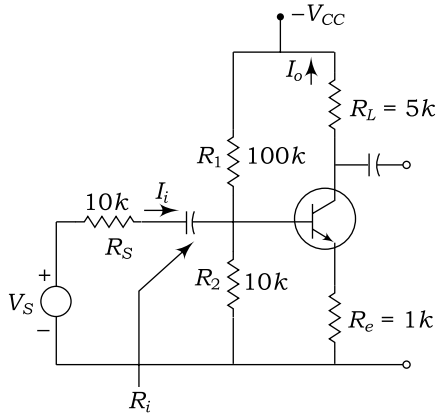


Fig. 2.94

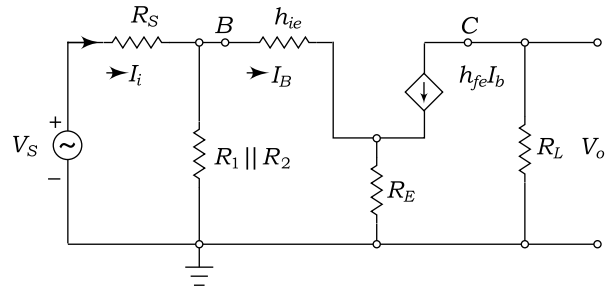


Fig. 2.95

Example 2.51 In the circuit diagram shown in Fig. 2.96, the transistor is made of silicon. Will the biasing circuit shown be placed in an active region? If no, explain the situation. If yes, compute the collector current I_{CQ} and V_{CEQ}. Assume $\beta = 100$.

Sol. The equivalent circuit of Fig. 2.96 is depicted in Fig. 2.97.

$$R_{\text{th}} = R_1 \| R_2 = 2.2k \| 2.2k = 1.1k$$

$$V_{\text{th}} = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{2.2}{2.2 + 2.2} \times 5 = 2.5 \text{ V}$$

$$V_{BE} = 0.8 \text{ V and } V_{CE} = 0.2$$

Applying KVL in the collector loop, $V_{CC} = I_E R_E + V_{CE}$ or $V_{CC} = (I_C + I_B)R_E + V_{CE}$

$$5 = I_C + I_B + 0.2 \text{ as } V_{CC} = 5V,\ R_E = 1k \text{ and } V_{CE} = 0.2$$

or $$I_C + I_B = 4.8 \text{ mA}$$

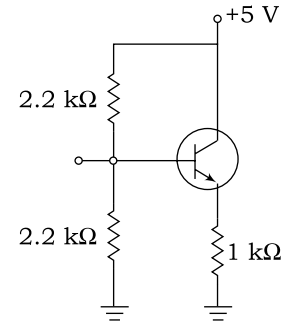


Fig. 2.96

Applying KVL in the base loop,

$$V_{\text{th}} = I_B R_B + V_{BE} + (I_C + I_B)R_E \text{ or } 2.5 = I_B \times 1.1 + 0.8 + 4.8 \times 1$$

Therefore, $I_B = (2.5 - 0.8 - 4.8)/1.1 = -2.818$ mA

Since $I_B = 2.818$ mA, the transistor cannot operate in saturation. Therefore, it operates in the active region.

$$V_{\text{th}} = I_B R_B + V_{BE(\text{active})} + I_E R_E$$

or $$V_{\text{th}} = I_B R_B + V_{BE(\text{active})} + (1 + \beta) I_B R_E \text{ as } I_E = (1 + \beta) I_B$$

$$I_B = \frac{V_{\text{th}} - V_{\text{BE(active)}}}{R_B + (1 + \beta)R_{\text{E}}} = \frac{2.5 - 0.7}{1.1 + (1 + 100)1} = 17.629 \text{ μA}$$

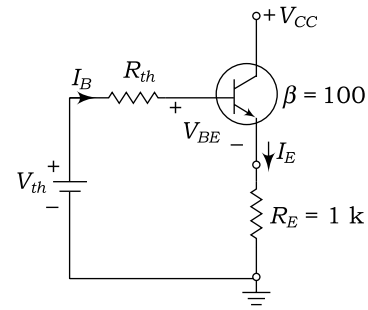


Fig. 2.97

The collector current $I_{\text{CQ}} = \beta I_B = 100 \times 17.629 \text{ μA} = 1.7629$ mA

The emitter current $I_E = (1 + \beta)I_B = (1 + 100) \times 17.629 \text{ μA} = 1.7805$ mA

$$V_{CEQ} = V_{CC} - I_E R_E = 5 - 1.7805 \times 10^{-3} \times 1 \times 10^3 = 3.2195 \text{ V}$$

Example 2.52 Determine I_C, V_E, V_B, V_C and I_B for the following circuit (Fig. 2.98).

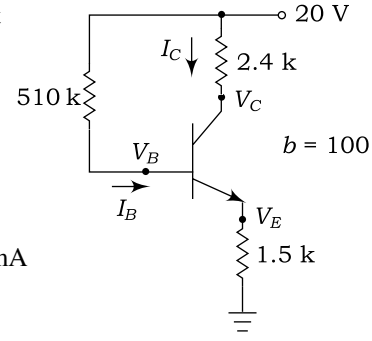


Fig. 2.98

Sol. The KVL equation in the base-emitter circuit is

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

or $V_{CC} = I_B R_B + V_{BE} + (1+\beta) I_B R_E$ as $I_E = (1+\beta) I_B$

Then

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E} = \frac{20 - 0.7}{[510 + (1+100) \times 1.5] \times 10^3} = 0.02917 \text{ mA}$$

$$I_C = \beta I_B = 100 \times 0.02917 \text{ mA} = 2.9176 \text{ mA}$$

$$I_E = (1+\beta) I_B = (1+100) \times 0.02917 \text{ mA} = 2.946 \text{ mA}$$

The KVL equation in the collector-emitter circuit is $V_{CC} = I_C R_C + V_{CE} + I_E R_E$

or $V_{CE} = V_{CC} - I_C R_C - I_E R_E = 20 - 2.9176 \times 2.4 - 2.946 \times 1.5 = 8.578 \text{ V}$

$$V_E = I_E R_E = 2.946 \times 1.5 = 4.419 \text{ V}$$

$$V_B = V_{BE} + V_E = 0.7 + 4.419 = 5.119 \text{ V}$$

$$V_C = V_{CE} + V_E = 8.578 + 4.419 = 12.997 \text{ V}$$

Example 2.53 For a *CE* amplifier, $h_{ie} = 2$ kΩ, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 20 \times 10^{-6}$ mho . If the load resistance is 4 kΩ and source resistance is 200 Ω, determine the input impedance, voltage and current gains.

Sol. Given: $h_{ie} = 2$ kΩ, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 20 \times 10^{-6}$ mho, $R_L = 4$ kΩ and $R_s = 200$ Ω

The current gain of the *CE* amplifier is

$$A_I = \frac{h_{fe}}{1 + h_{oe} R_L} = \frac{50}{1 + (20 \times 10^{-6} \times 4 \times 10^3)} = 46.296$$

Input resistance is

$$R_i = h_{ie} + h_{re} A_I R_L = 2000 + (2 \times 10^{-4} \times 46.296 \times 4000) = 2037.0368$$

The voltage gain is

$$A_V = A_I \frac{R_L}{R_i} = 46.296 \times \frac{4000}{200} = 925.92$$

Example 2.54 A transistor amplifier in *CE* configuration couples a source of 1 kΩ internal resistance to a 20 kΩ load. Find the input and the output resistance if $h_{ie} = 1$ kΩ, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 150$ and $1/h_{oe} = 40$ kΩ.

Sol. Given: $h_{ie} = 1$ kΩ, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 150$ and $1/h_{oe} = 40$ kΩ, $R_L = 20$ kΩ and $Rs = 1$ kΩ

The current gain of the *CE* amplifier is

$$A_I = \frac{h_{fe}}{1 + h_{oe} R_L} = \frac{150}{1 + [(1/40 \times 10^3) \times 20 \times 10^3]} = 100$$

Input resistance is

$$R_i = h_{ie} + h_{re} A_I R_L = 1000 + (2.5 \times 10^{-4} \times 100 \times 20{,}000) = 1500 \text{ Ω}$$

The voltage gain is

$$A_V = A_I \frac{R_L}{R_i} = 100 \times \frac{20,000}{1500} = 1333.33$$

At collector-emitter terminals, the output resistance is

$$R_o = \frac{1}{h_{oe}} \| R_L = 40\ \text{k}\Omega \| 20\ \text{k}\Omega = 13.33\ \text{k}\Omega$$

2.31 TRANSRESISTANCE AMPLIFIER

The equivalent circuit of a transresistance amplifier is shown in Fig. 2.99. This circuit is represented by a Norton's equivalent in the input circuit and a Thevenin's equivalent in its output circuit.

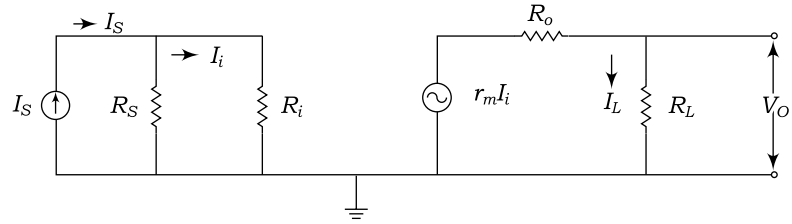


Fig. 2.99

The input current can be expressed by

$$I_i = I_s \frac{R_s}{R_s + R_i}$$

If the input resistance $R_{\text{in}} << R_s$, $I_i = I_s$

Therefore, source current is equal to input current as $R_s >> R_i$

The output voltage is equal to

$$V_o = r_m I_i + I_L R_o = I_L R_L$$

If $R_L >> R_o$,

$$V_o = r_m I_i = I_L R_L$$

or,

$$r_m I_i = I_L R_L = V_o = r_m I_s \quad \text{as} \quad I_i \approx I_s$$

The transresistive amplifier gain is $r_m = \dfrac{V_o}{I_s}$

Therefore, the output voltage V_o is directly proportional to the source current I_s and the proportionality factor r_m and it is independent of R_s and R_L. An ideal transresistive amplifier has zero input resistance $R_i = 0$ and zero output resistance $R_o = 0$.

Example 2.55 Figure 2.100 shows an amplifier circuit. Determine the voltage gain and power gain. Assume $A_i = 1000$.

Sol. $R_s = 10\ \text{k}\Omega$, $R_i = 10\ \Omega$, $R_o = 10\ \text{k}\Omega$, $R_L = 10\ \Omega$

Input voltage is equal to

$$V_i = I_i R_i = 10 I_i \text{ as } R_i = 10\ \Omega$$

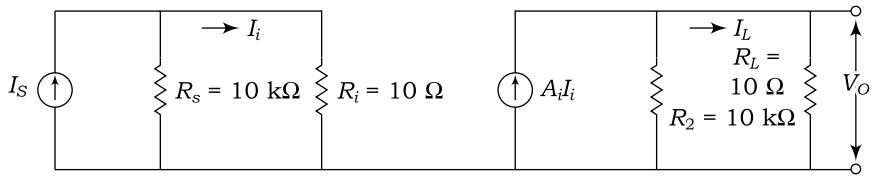


Fig. 2.100

Output voltage is

$$V_o = A_i I_i \frac{R_o R_L}{R_o + R_L}$$
$$= 1000 I_i \frac{10,000 \times 10}{10,000 + 10} = 9990 I_i$$

The voltage gain is

$$A_v = \frac{V_o}{V_i} = \frac{9990 I_i}{10 I_i} = 999$$

Current gain is

$$A_i = \frac{I_L}{I_s} = \frac{V_o / R_L}{I_i \frac{R_s + R_i}{R_s}} \quad \text{as} \quad I_L = V_o / R_L \text{ and } I_i = I_s \frac{R_s}{R_s + R_i}$$
$$= \frac{9990 I_i}{10 I_i \frac{10,000 + 10}{10,000}} = \frac{9.990 \times 1000}{10,010}$$
$$= 998$$

The power gain is equal to

$$A_P = A_V \quad A_i = 999 \times 998$$
$$= 997 \times 10^3$$

2.32 TRANSCONDUCTANCE AMPLIFIER

Figure 2.101 shows a equivalent circuit of a transconductance amplifier. This circuit is represented by a Thevenin's equivalent in input circuit and a Norton's equivalent in output circuit.

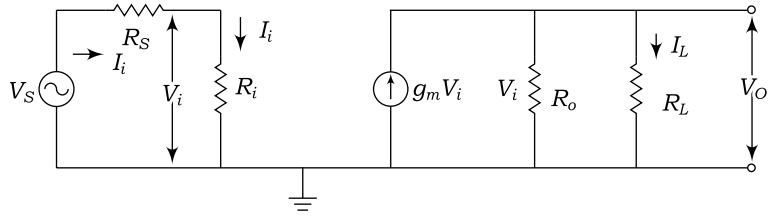


Fig. 2.101

The source voltage can be expressed as

$$V_s = I_i R_s + V_i$$

or $$V_s = I_i R_s + I_i R_i \quad \text{as} \quad V_i = I_i R_i$$

As $R_s << R_i$, $V_s = I_i R_i = V_i$

Therefore source voltage is equal to input voltage as $R_i >> R_s$

The output current I_L flows through load resistance R_L and I_t can be expressed by

$$I_L = g_m V_i \frac{R_o}{R_o + R_L}$$

If $R_o >> R_L$, $I_L = g_m V_i = g_m V_s$ as $V_i = V_s$

The transconductance amplifier gain is

$$g_m = \frac{I_L}{V_S}$$

Therefore, in an ideal transconductance amplifier, output current is proportional to the supply voltage and the proportionality factor g_m and it is independent R_i and R_o. An ideal transconductance amplifier has infinite resistance $R_i = \infty$ and infinite output resistance $R_o = \infty$.

2.33 EMITTER FOLLOWER CIRCUITS

Emitter follower circuit is a negative current feedback circuit. This circuit has large input impedance, small output impedance and a voltage gain of approximately unity. Since the output voltage tends to be in phase with the input voltage in this circuit, the term 'follower' is used. Due to unity voltage gain and high input impedance and small output impedance, an emitter follower circuit is used as input and output buffer stages in amplifier systems.

Figure 2.102 shows an emitter follower circuit. The difference between an emitter follower circuit and a conventional amplifier is the absence of collector load R_C and the emitter bypass capacitor C_E. Here the

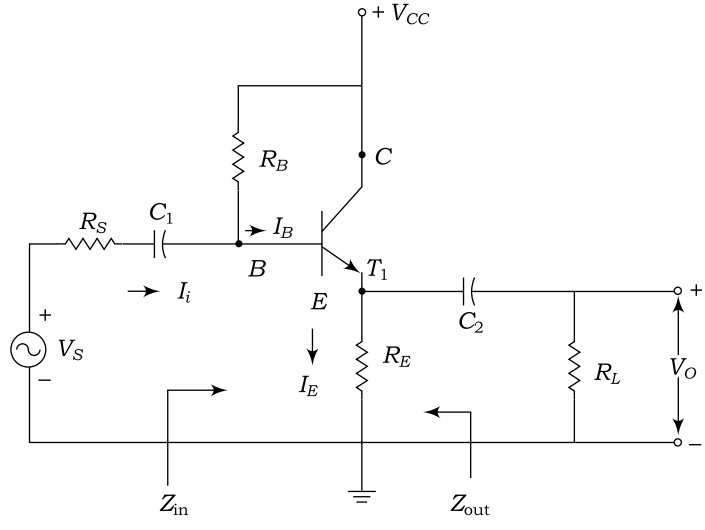


Fig. 2.102 Emitter follower circuit

emitter resistance R_E acts as a load and the ac output voltage V_o is obtained from emitter terminal. In this circuit, the biasing is provided either by base resistance R_B or potential divider method. This circuit has a resistance of the order of 10 kΩ in emitter itself and the collector terminal is directly connected to the dc supply V_{CC}. The stabilization of operating point is exceptionally good due to high value of emitter resistance R_E.

While input voltage V_s is applied to the base of transistor T_1, the resulting emitter current I_E flows through resistance R_E and an output voltage V_o is obtained from emitter terminal. The voltage V_o is equal to voltage drop across the emitter resistance R_E. Therefore, $V_o = I_E R_E$.

In this circuit, the output voltage V_o opposes the ac input signal voltage V_s as it is inphase opposition to V_s. Hence, this circuit provides negative current feedback. As the output voltage V_o feedback to the input and V_o is proportional to the emitter current, this circuit is called a negative current feedback circuit.

When the input signal voltage V_s passes through its positive half cycle, the output voltage V_o is also passed through its positive half cycle. Therefore, the output voltage is in phase with the input signal voltage V_s. As output voltage V_o just follows the input voltage V_s, this circuit is called *emitter follower*.

The small signal ac equivalent circuit of Fig. 2.102 is shown in Fig. 2.103. In Fig. 2.103, the value of R_B is neglected as it is very much larger than source resistance R_S. The Thevenin's equivalent circuit of Fig. 2.103 is depicted in Fig. 2.104

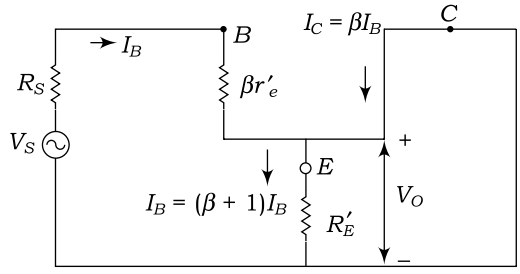


Fig. 2.103 Small signal equivalent circuit of emitter follower

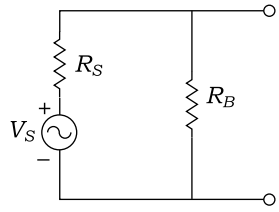


Fig. 2.104 Thevenin's equivalent circuit for the input circuit of emitter follower

Applying KVL in the input circuit of emitter follower, we get

$$V_s - I_B R_s - I_B \beta r'_e - (\beta + 1) I_B R'_E = 0$$

or $$V_s = I_B [R_s + \beta r'_e + (\beta + 1) R'_E]$$

or $$I_B = \frac{V_s}{R_s + \beta r_e' + (\beta + 1) R'_E}, \text{ where } R'_E = R_E \| R_L$$

The emitter current $I_E = (\beta + 1) I_B$

$$= \frac{(\beta + 1) V_s}{R_s + \beta r_e' + (\beta + 1) R'_E}$$

or $$I_E = \frac{V_s}{(R_s + \beta r_e')/(\beta + 1) + R_s'}$$

If we assume $(\beta + 1) \cong \beta$, the emitter current is equal to

$$I_E = \frac{V_s}{\frac{R_s}{\beta} + r_e' + R'_E}$$

The above equation can be represented by Fig. 2.105

when R_E' is represented by the parallel combination of R_E and R_L, Fig. 2.105 will be represented by Fig. 2.106.

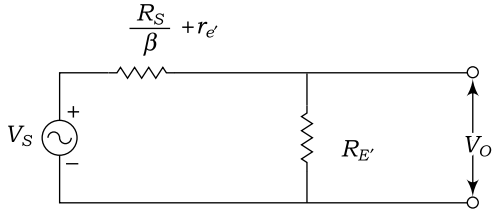


Fig. 2.105

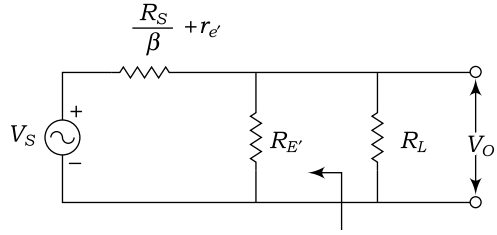


Fig. 2.106

The output voltage is equal to

$$V_o = V_s \cdot \frac{R_E'}{\frac{R_s}{\beta} + r_e' + R_E'}$$

The voltage gain is

$$A_v = \frac{V_o}{V_s} = \frac{R_E'}{R_E' + \frac{R_s}{\beta} + r_e'}$$

As $R_E' = R_E \| R_L$, $A_v = \dfrac{R_E \| R_L}{R_E \| R_L + \dfrac{R_s}{\beta} + r_e'}$

To find Z_{out}, assume $V_s = 0$. Then Z_{out} is equal to

$$Z_{out} = R_E \| \left(\frac{R_s}{\beta} + r_e' \right)$$

The input impedance

$$Z_{in\ (base)} = \beta(r_e' + R_E') = \beta(r_e' + R_E \| R_L)$$

The input impedance Z_{in} is equal to

$$\begin{aligned} Z_{in} &= R_B \| Z_{in\ (Base)} \\ &= R_B \| \beta(r_e' + R_E \| R_L) \end{aligned}$$

At no-load condition, the gain becomes

$$A_{V\text{no-load}} = \frac{R_E}{R_E + r_e'} \cong 1 \quad \text{as} \quad R_E >> r_e'$$

For loaded condition, the gain is

$$A_V = \frac{V_o}{V_{in}} = \frac{R_E \| R_L}{R_E \| R_L + r_e'} \cong 1$$

The current gain is equal to

$$A_I = \frac{I_E}{I_B} = (\beta + 1) \cong \beta$$

The input voltage to the amplifier is

$$V_{BE} = V_s - I_E R_E = V_s - V_o$$

when the voltage drop in source resistance R_s is neglected.

The feedback ratio of emitter follower circuit is β.

2.33.1 Advantages of Emitter Follower Circuit

The emitter follower circuit has the following advantages:

(i) This circuit has high input impedance and low output impedance. Therefore, this circuit can be used for impedance matching.

(ii) The feedback ratio of emitter follower is β, i.e., 100% feedback. Consequently, output is distortion-less and bandwidth is very large.

(iii) This circuit has relatively high current gain and power gain.

(iv) The output voltage is in phase with the input voltage and approximately equal in magnitude. The emitter voltage closely follows the input voltage, so it is called emitter follower circuit.

2.33.2 Applications of Emitter Follower Circuit

(i) Due to high input impedance and low output impedance, an emitter follower circuit is capable of transferring maximum power from the high impedance source to low impedance load. This circuit is called *buffer amplifier*.

(ii) Usually impedance matching can be achieved by employing a step down transformer, but emitter follower is preferred. Emitter follower is not only more convenient than a transformer but also provides better frequency response.

(iii) In digital electronics circuits, an increase in current is required but no increase in voltage is required. For these applications, emitter follower circuit is used due to high current gain.

Example 2.56 Find the input impedance for the emitter follower circuit as shown in Fig. 2.107.

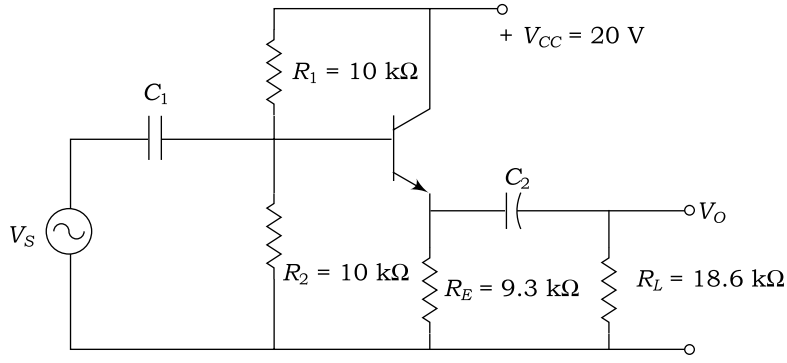


Fig. 2.107

Sol. The voltage across R_2 is

$$V_2 = V_{CC} \cdot \frac{R_2}{R_1 + R_2} = 20 \times \frac{10}{10 + 10} = 10 \text{ V}$$

The voltage across R_E is equal to

$$V_E = V_2 - V_{BE} = 10 - 0.7 = 9.3 \text{ V}$$

The emitter current is

$$I_E = \frac{V_E}{R_E} = \frac{9.3}{9.3 \times 10^3} = 1 \text{ mA}$$

AC emitter resistance

$$r'_e = \frac{25 \text{ mV}}{I_C} = \frac{25 \text{ mV}}{1 \text{ mA}} = 25 \ \Omega$$

The effective emitter resistance is equal to

$$R'_E = 9.3 \text{ k}\Omega \parallel 18.6 \text{ k}\Omega = \frac{9.3 \times 18.6}{9.3 + 18.6} = 6.2 \text{ k}\Omega$$

The input impedance to the base is

$$Z_{\text{in (base)}} = \beta(r'_e + R'_E)$$
$$= 100(25 + 6200) = 622.5 \text{ k}\Omega$$

The input impedance of emitter follower is

$$Z_{\text{in}} = R_1 \parallel R_2 \parallel Z_{\text{in (base)}}$$
$$= 10 \text{ k}\Omega \parallel 10 \text{ k}\Omega \parallel 622.5 \text{ k}\Omega$$
$$= 4.96 \text{ k}\Omega.$$

Review Exercises

Short-Answer Questions

1. Why is BJT a current-controlled device?

Ans. The output current, voltage and power of transistor are controlled by the input current of BJT. So it is called a current-controlled device.

2. Why is collector region of BJT larger than emitter and base regions?

Ans. Since the maximum power dissipates in the collector of a transistor, the collector region is larger than emitter and base regions.

3. Why is the width of the base region very small when compared to emitter and collector regions?

Ans. The width of the base region is very small and very lightly doped so that most of the injected charge carriers pass to the collector.

4. What is the need of biasing for a transistor?

Ans. Under normal operating condition, the base-emitter junction is forward biased and the collector-base junction is reverse biased. The biasing arrangement is required to establish a stable *Q*-point which indicates the desired mode of operation.

If the transistor is not biased adequately, a distorted output signal is obtained from transistor. Due to temperature variation, transistor parameters are changed and the operating point gets shifted and the amplifier output will be unstable.

5. Is it possible to make a transistor by connecting two semiconductor diodes back to back?

Ans. When two semiconductor diodes are connected back to back, a base region between collector and emitter will not be developed. Hence, we cannot make a transistor by connecting two semiconductor diodes back to back.

6. Why are silicon transistors extensively used in place of germanium transistors?

Ans. In a silicon transistor, the value of current I_{CB0} is small and its variation is small due to temperature variation. Hence, silicon transistors can operate at high temperature compared to germanium transistors.

7. Which of the transistor currents is always the largest? Which is always the smallest? Which two currents are relatively close in magnitude?

Ans. Always the emitter current I_E is the largest current and the base current I_B is smallest. The collector current I_C is approximately equal to the emitter current I_E, i.e. $I_C = I_E$.

8. Why is *CC* configuration called a voltage buffer? What is its other name?

Ans. Due to high input impedance and low output impedance, the common collector current is widely used as a voltage buffer. It is also called emitter follower.

9. Why is CE configuration of a transistor used in amplifier circuits?

Ans. Since voltage, current and power gains are high, the ratio of output impedance and input impedance is moderate, and so *CE* configuration of transistor is commonly used in amplifier circuits.

10. Which transistor configuration provides maximum input impedance and about unity voltage gain?

Ans. Common-collector configuration has the maximum input impedance and voltage gain is less than unity.

11. What is punch-through effect?

Ans. With the increase in collector voltage, effective base width is reduced to zero, and the emitter barrier voltage becomes smaller than $V_o - |V_{EB}|$ as the collector voltage reaches through the base region. Due to lowering of emitter junction voltage, an extensively large emitter current flows. Therefore, there is an upper limit on the magnitude of collector voltage. This phenomenon is called punch-through.

12. What is stability factor?

Ans. The stability factor S is defined as the rate of change of collector current with respect to leakage current I_{C0} when V_{BE} and β are constant.

13. What are the different devices used in biasing compensation?

Ans. It is achieved by temperature-sensitive devices such as diodes, thermistors and sensistors.

14. What is the significance of arrow in the transistor symbol?

Ans. The arrow in transistor symbol represents the direction of conventional emitter current flow and thereby defines the direction of other currents in the transistor.

Multiple-choice Questions

1. In a transistor,
   (a) the emitter is heavily doped than collector and base
   (b) the collector is heavily doped than emitter and base
   (c) the base is heavily doped than emitter and base collector
   (d) the base region must be very narrow
2. In a *PNP* transistor, holes are injected
   (a) into emitter and cross the emitter base junction and move towards collector
   (b) into base and cross the emitter-base junction and move towards collector
   (c) into collector and cross the collector-base junction and moves towards collector
   (d) only into the collector

3. The leakage current I_{CB0} flows through
   (a) the emitter, base and collector terminals (b) the base and collector terminals
   (c) the emitter and base terminals (d) the collector and emitter terminals
4. In an *NPN* transistor, electrons are injected
   (a) into base and cross the emitter-base junction and move towards collector
   (b) into emitter and cross the emitter base junction and move towards collector
   (c) into collector and cross the collector-base junction and moves towards collector
   (d) only into the collector
5. The relationship between α and current gain β is
   (a) $\alpha = \frac{\beta}{\beta+1}$ (b) $\alpha = \frac{\beta+1}{\beta}$ (c) $\alpha = \frac{\beta}{\beta-1}$ (d) $\alpha = \frac{\beta-1}{\beta}$
6. The collector current in a common-base circuit is
   (a) $I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{C0}}{1-\alpha}$ (b) $I_C = \frac{\alpha}{1+\alpha} I_B + \frac{I_{C0}}{1+\alpha}$
   (c) $I_C = \alpha I_E + I_{C0}$ (d) $I_C = \alpha I_E - I_{C0}$
7. If there is a small increase in collector-base reverse bias voltage,
   (a) the emitter current increase significantly
   (b) the collector current increase significantly
   (c) the collector current decrease significantly
   (d) the emitter current decrease significantly
8. The emitter region of a transistor is highly doped compared to base and collector region to
   (a) provide or supply charge carriers
   (b) collect the charge carriers
   (c) dissipate maximum power
   (d) provide minimum resistance
9. Early effect in a transistor is known as
   (a) zener breakdown (b) avalanche breakdown
   (c) thermal breakdown (d) reduction in width of base or base narrowing
10. The value of α in a bipolar junction transistor is
    (a) 0.95 to 0.998 (b) 0.45 to 0.498 (c) 1.95 to 1.998 (d) –0.95 to –0.998
11. Which of the following relationships is the correct one for a bipolar transistor
    (a) $I_E = I_C + I_B$ (b) $I_E = I_C - I_B$ (c) $I_C = I_E + I_B$ (d) $I_B = I_E - I_B$
12. If the collector-base junction is reverse biased and the emitter-base junction is forward biased, the transistor operates in
    (a) saturation region (b) active region (c) cut-off region (d) All of these
13. The transistor operates in saturation region if
    (a) collector junction is reverse biased and the emitter junction is forward biased
    (b) collector junction is forward biased and the emitter junction is reverse biased
    (c) both the collector junction and the emitter junction are forward biased
    (d) both the collector junction and the emitter junction are reverse biased

14. The transistor operates in cut-off region if
    (a) collector junction is reverse biased and the emitter junction is forward biased
    (b) collector junction is forward biased and the emitter junction is reverse biased
    (c) both the collector junction and the emitter junction are forward biased
    (d) both the collector junction and the emitter junction are reverse biased
15. If a *PNP* transistor operates in active region, the holes
    (a) diffuse and recombine in the *N*-type base region
    (b) drift in the *N*-type base region
    (c) injected from collector
    (d) provide avalanche multiplication
16. If an *NPN* transistor operates in active region, the electrons
    (a) drift in the *N*-type base region
    (b) diffuse and recombine in the *P*-type base region
    (c) injected from collector
    (d) provide avalanche multiplication
17. If the transistor operates in active region during common-emitter configuration,
    (a) $I_C = \beta I_B$ (b) $I_E = \beta I_B$ (c) $I_B = \beta I_C$ (d) $I_B = \beta I_E$
18. The emitter is heavily doped
    (a) to increase injection efficiency (b) to reduce injection efficiency
    (c) to drift charge carriers in the base region (d) All of these
19. A common-base configuration transistor has
    (a) high input impedance(resistance) and low output impedance(resistance)
    (b) high input impedance(resistance) and high output impedance(resistance)
    (c) low input impedance(resistance) and high output impedance(resistance)
    (d) low input impedance(resistance) and low output impedance(resistance)
20. When the transistor operates in saturation mode, it behaves as
    (a) a closed switch (b) an open switch (c) an amplifier (d) All of these
21. When the transistor operates in cut-off region, it behaves as
    (a) a closed switch (b) an open switch (c) an amplifier (d) All of these
22. When the transistor operates in active region mode, it behaves as
    (a) a closed switch (b) an open switch (c) an amplifier (d) All of these
23. The load line of a transistor amplifier circuit is
    (a) a graph between V_{CE} and I_C (b) a graph between V_{CE} and I_B
    (c) a graph between V_{BE} and I_B (d) a graph between V_{BE} and I_C
24. If the *Q*-point is _____, the positive part of input signal is clipped at output.
    (a) near saturation point (b) near cut-off point
    (c) middle of active region (d) any where of the load line
25. When the *Q*-point is _____, the negative part of input signal is clipped at output.
    (a) near saturation point (b) near cut-off point
    (c) middle of active region (d) any where of the load line

26. The undistorted output signal is available when the Q-point is
    (a) near saturation point (b) near cut-off point
    (c) in middle of active region (d) anywhere of the load line
27. The saturation point on the dc load line is
    (a) $V_{CE} = 0, I_{Csat} = \frac{V_{CC}}{R_C}$ (b) $V_{BE} = 0, I_{Csat} = \frac{V_{CC}}{R_C}$
    (c) $V_{CE} = 0, I_{Csat} = \frac{V_{BB}}{R_C}$ (d) $V_{BE} = 0, I_{Csat} = \frac{V_{BB}}{R_C}$
28. The cut-off point on the dc load line is
    (a) $V_{CE} = V_{CC}, I_C = 0$ (b) $V_{BE} = V_{CC}, I_C = 0$
    (c) $V_{CE} = 0, I_C = 0$ (d) $V_{BE} = 0, I_B = 0$
29. The stability factor of a common-base transistor circuit is
    (a) $S = 1$ (b) $S = \beta$ (c) $S = 1 + \beta$ (d) $S = 1 - \beta$
30. The stability factor of a common emitter transistor circuit is
    (a) $S = 1$ (b) $S = \beta$ (c) $S = 1 + \beta$ (d) $S = 1 - \beta$
31. The stability factor of a transistor can be expressed as
    (a) $S = \frac{1+\beta}{1+\beta\left(\frac{dI_B}{dI_C}\right)}$ (b) $S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$ (c) $S = \frac{1-\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$ (d) $S = \frac{1-\beta}{1+\beta\left(\frac{dI_B}{dI_C}\right)}$
32. The stability factor of a fixed bias with emitter feedback transistor circuit is
    (a) $S = \frac{1+\beta}{1+\beta\frac{R_E}{R_E+R_B}}$ (b) $S = \frac{1-\beta}{1-\beta\frac{R_E}{R_E+R_B}}$
    (c) $S = \frac{1+\beta}{1-\beta\frac{R_E}{R_E+R_B}}$ (d) $S = \frac{1-\beta}{1+\beta\frac{R_E}{R_E+R_B}}$
33. The stability factor of a fixed bias with collector feedback transistor circuit is
    (a) $S = \frac{1+\beta}{1-\beta\frac{R_C}{R_C+R_B}}$ (b) $S = \frac{1-\beta}{1+\beta\frac{R_C}{R_C+R_B}}$
    (c) $S = \frac{1+\beta}{1+\beta\frac{R_C}{R_C+R_B}}$ (d) $S = \frac{1-\beta}{1-\beta\frac{R_C}{R_C+R_B}}$
34. The stability factor of a voltage-divider common-emitter transistor circuit is
    (a) $S = \frac{1+\beta}{1+\beta\frac{R_E}{R_{th}+R_E}}$ (b) $S = \frac{1-\beta}{1-\beta\frac{R_E}{R_{th}+R_E}}$

(c) $S = \dfrac{1-\beta}{1+\beta\dfrac{R_E}{R_{th}+R_E}}$ (d) $S = \dfrac{1+\beta}{1-\beta\dfrac{R_E}{R_{th}+R_E}}$

35. The stability factor of an emitter-bias transistor circuit is

(a) $S = \dfrac{1+\beta}{1+\beta\dfrac{R_E}{R_B+R_E}}$ (b) $S = \dfrac{1-\beta}{1+\beta\dfrac{R_E}{R_B+R_E}}$

(c) $S = \dfrac{1+\beta}{1-\beta\dfrac{R_E}{R_B+R_E}}$ (d) $S = \dfrac{1-\beta}{1-\beta\dfrac{R_E}{R_B+R_E}}$

36. In bias compensation circuits, _____ devices are used.
    (a) diode (b) thermistor
    (c) diode and thermistor (d) None of these
37. The self-bias arrangement provides a better Q-point stability if
    (a) R_E is small (b) R_E is large
    (c) β is small and R_E is large (d) both β and R_E are large
38. Unity gain bandwidth means
    (a) Gain = 1 dB (b) Gain = 0 dB
    (c) Bandwidth = 1 (d) Gain × Bandwidth = 1
39. Difference between an amplifier and a transformer is that an amplifier has
    (a) current gain (b) voltage gain (c) power gain (d) None of these
40. To improve the efficiency of an amplifier, we have to
    (a) reduce the power dissipation rating (b) reduce supply voltage
    (c) reduce the load power (d) reduce unwanted power loss

Review Questions

1. What is a transistor? Why are transistors called bipolar devices?
2. Why is the emitter region of a transistor highly doped compared to collector and emitter region?
3. What do you mean by static characteristic of a transistor?
4. Draw the common-base transistor input characteristics and discuss briefly.
5. Explain saturation, active and cut-off regions of transistors. How is ac input resistance of transistor computed from characteristics curve?
6. Draw the common-base transistor circuit and output characteristics.
7. What is saturation of a transistor?
8. Draw the common-emitter transistor input characteristics.
9. What are the different types of biasing of a transistor? Which method of biasing is used to operate transistor as an amplifier?
10. Draw the common-emitter transistor circuit and output characteristics.

11. Define the current gain α and current gain β. Find the relationship between α and β.
12. What is reverse saturation current I_{CB0}? How does I_{CB0} vary with temperature? Define h_{fe}.
13. What is thermal runaway? How it can be prevented in power transistor?
14. Write about the minority carrier concentration in a *PNP* transistor.
15. Write short notes on the following:
    (a) Transistor as a switch
    (b) Transistor as an amplifier
    (c) Comparison between *CB*, *CE* and *CC* configuration of a transistor
16. Why does the common emitter (*CE*) configuration provide large current amplification while the common base (*CB*) configuration does not?
17. Compare the performance of a transistor in different configurations.
18. What do you mean by the *Q*-point of a transistor amplifier?
19. Draw a circuit diagram of a common-emitter amplifier and explain its output characteristics.
20. Define dc load line. How you can draw a dc load line of a transistor?
21. What do you mean by the distortion output in amplifiers? Explain how you can obtain an undistorted output of an amplifier.
22. What do you mean by biasing? What are the different types of biasing?
23. What are the factors that can affect the stability of a transistor?
24. Derive the stability factor in terms of I_{C0}, V_{BE} and β. Explain why the common-emitter amplifier requires a form of dc stabilization, whereas common base amplifiers does not require dc stabilisation circuit.
25. Is the operating *Q*-point of a transistor amplifier fixed? If not, write the names of different factors which can affect the *Q*-point.
26. What are the different types of biasing? Derive the stability factor of voltage-divider biasing circuit. Can the value of the stability factor is less than unity?
27. What is self-bias? Draw a self-bias circuit and derive the stability factor.
28. How is the temperature compensation provided in biasing circuit.
29. Figure 2.108 shows a common-emitter configuration of a *NPN* transistor. When $\beta = 75$ and $I_{C0} = 10$ μA, determine the transistor currents. What will happen if the R_C is indefinitely increased?

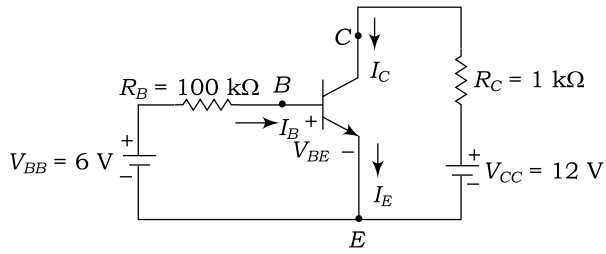


Fig. 2.108

30. Figure 2.109 shows an *NPN* transistor circuit. If the voltage across the base emitter is $V_{BE} = 0.6$ V and the voltage between collector emitter terminals is $V_{CE} = 0.35$ V and dc current gain $\beta = 80$. Find the operation mode of the transistor.

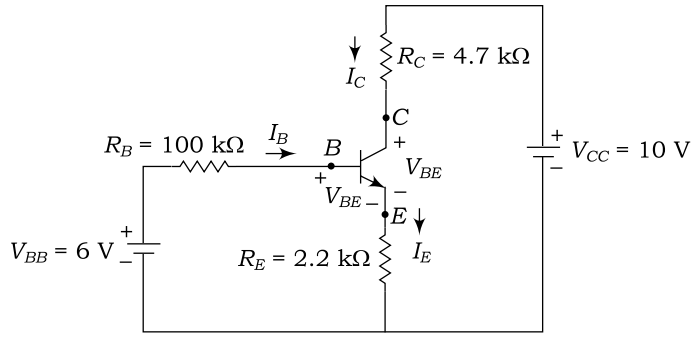


Fig. 2.109

31. When a transistor operates in common-emitter mode configuration, the base current is 25 μA. The collector current has been changed from 4.5 mA to 4.9 mA if the collector emitter voltage is changed from 7.2 V to 11.5 V. Determine the output resistance and dc current gains α and β.
32. Figure 2.110 shows an *NPN* transistor circuit. Determine the base current, collector current, emitter current, and collector-emitter voltage V_{CE} when $V_{BE} = 0.65$ V and $\beta = 90$.
33. The reverse saturation current of a transistor in common-base configuration is 0.15 μA and in common emitter configuration is 22 μA. Determine dc current gains α and β. Assume the base current $I_B = 11$ mA.
34. The reverse saturation current of a transistor in common-base configuration is 0.30 μA and the dc current gain α is 0.99. Calculate the collector current and emitter current of transistor. Assume the base current $I_B = 15.5$ mA.
35. In common-emitter configuration, a transistor has the following parameters:
$h_{ie} = 2.5$ kΩ, $h_{re} = 1.5 \times 10^{-4}$, $h_{fe} = 55$, $h_{oe} = 50 \times 10^{-6}$ μ siemens, $R_S = 1.5$ kΩ and $R_L = 2$ kΩ
Determine the current gain, voltage gain, input impedance and output impedance.

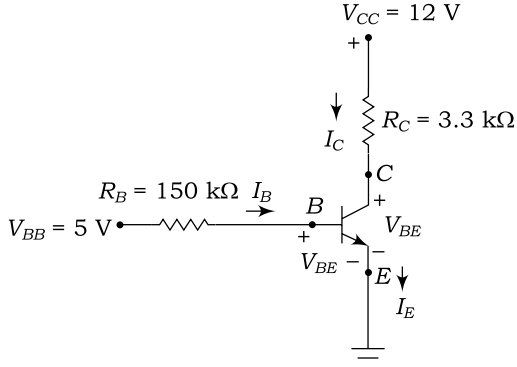


Fig. 2.110

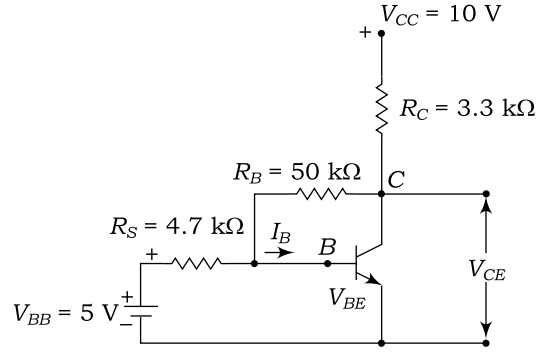


Fig. 2.111

36. Figure 2.111 shows a common-emitter transistor configuration with collector feedback, and it has the following parameters**:**
$h_{ie} = 1.6$ kΩ, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 55$, $h_{oe} = 50 \times 10^{-6}$ μ siemens, $R_S = 1$ kΩ and $R_L = 2.5$ kΩ
Determine the current gain, voltage gain, input impedance and output impedance.
37. In common-base configuration, a transistor has the following parameters:
$h_{ib} = 35$ Ω, $h_{rb} = 2.25 \times 10^{-4}$, $h_{fb} = -0.95$, $h_{ob} = 50 \times 10^{-6}$ siemens, $R_S = 1.25$ kΩ and $R_L = 2.25$ kΩ
Determine the current gain, voltage gain, input impedance and output impedance.

38. In common-collector configuration, a transistor has the following parameters:
$h_{ic} = 3.5\ \Omega$, $h_{rc} = 1$, $h_{fc} = -55$, $h_{oc} = 50 \times 10^{-6}$ siemens, $R_S = 1.5\ \text{k}\Omega$ and $R_L = 2.5\ \text{k}\Omega$
Determine the current gain, voltage gain, input impedance and output impedance.
39. Figure 2.112 shows a transistor amplifier circuit. Determine the value of saturation current and the collector emitter cut-off voltage. Draw the dc load line.

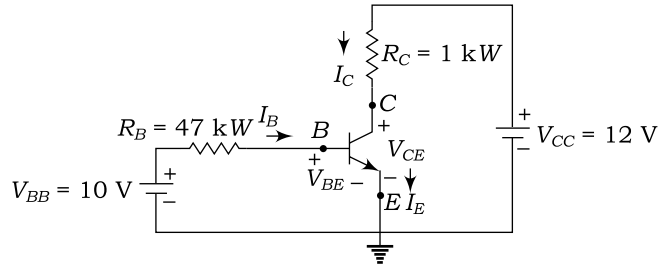


Fig. 2.112

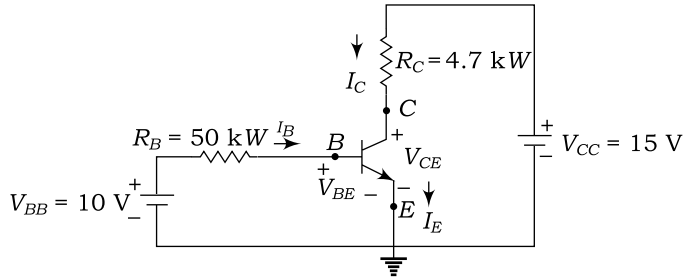


Fig. 2.113

40. A transistor amplifier circuit is shown in Fig. 2.113. Draw the dc load line and locate the *Q*-point on the dc load line. Assume $V_{BE} = 0.65$ V and $\beta = 55$.
41. Figure 2.114 shows a biasing circuit of an *NPN* transistor amplifier circuit. Calculate the base current, collector current, emitter current and collector-to-emitter voltage. Assume $V_{BE} = 0.6$ V and $\beta = 60$.

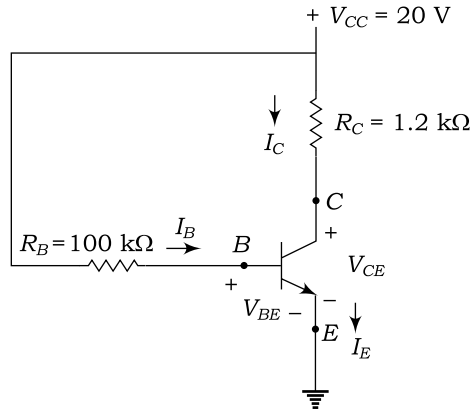


Fig. 2.114

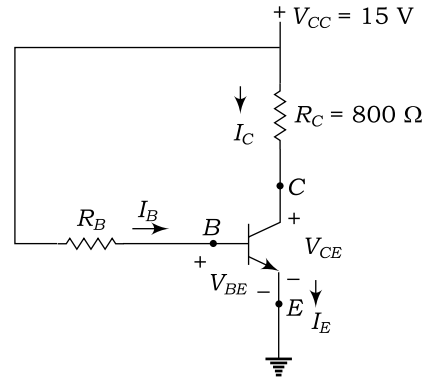


Fig. 2.115

42. Determine the biasing resistance R_B of a biasing circuit of an *NPN* transistor as depicted in Fig. 2.115 when the base current is 0.25 mA. Calculate the collector current, collector to emitter voltage and stability factor. Assume $V_{BE} = 0.65$ V and $\beta = 85$.

43. Determine the base current, collector current, and collector to emitter voltage of a biasing circuit as shown in Fig. 2.116. Assume $V_{BE} = 0.6$ V and $\beta = 95$.

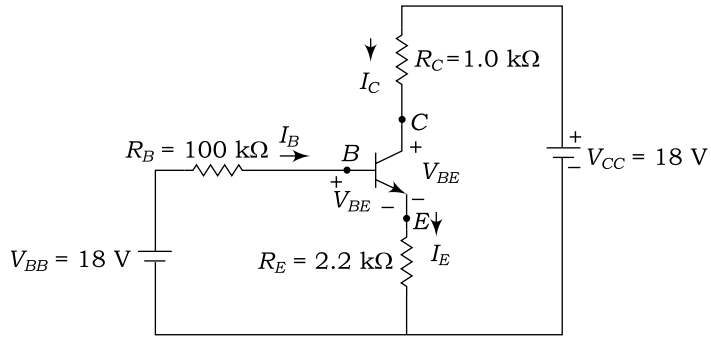


Fig. 2.116

44. Figure 2.117 shows the fixed bias with emitter feedback circuit. Determine the base current, collector current, collector to emitter voltage and stability factor of a biasing circuit. Assume $V_{BE} = 0.68$ V and $\beta = 55$.

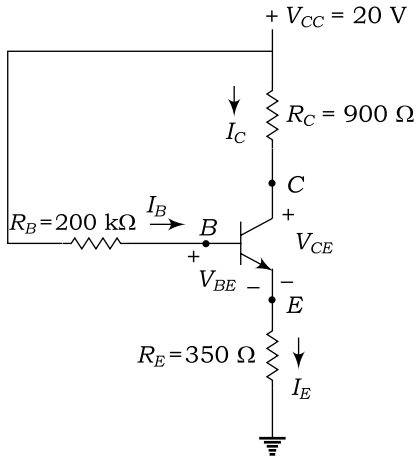


Fig. 2.117

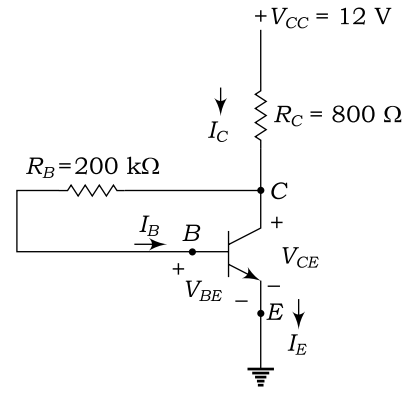


Fig. 2.118

45. Figure 2.118 shows the fixed bias with collector feedback circuit. Calculate the base current, collector current, collector to emitter voltage and stability factor. Assume $V_{BE} = 0.69$ V and $\beta = 45$.
46. Determine the biasing resistance R_B of a collector feedback biasing circuit of an *NPN* transistor as depicted in Fig. 2.119 when the base current is 0.22 mA. Calculate the collector current, collector to emitter voltage and stability factor. Assume $V_{BE} = 0.7$ V and $\beta = 85$.
47. Figure 2.120 shows the voltage-divider bias circuit. Determine the collector current and collector-to-emitter voltage. Assume $V_{BE} = 0.7$ V and $\beta = 55$.
48. The voltage-divider bias circuit of an *NPN* transistor is shown in Fig. 2.121. Calculate the value of R_1 and R_C when collector current is 1 mA and collector to emitter voltage is 2.45 V. Assume $V_{BE} = 0.7$ V and $\beta = 95$.

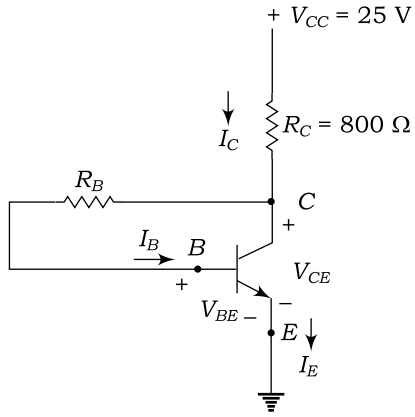


Fig. 2.119

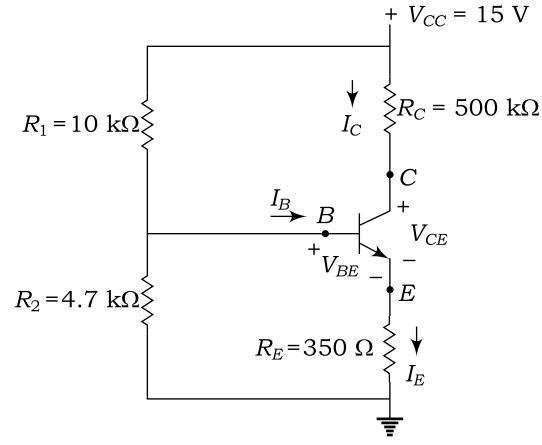


Fig. 2.120

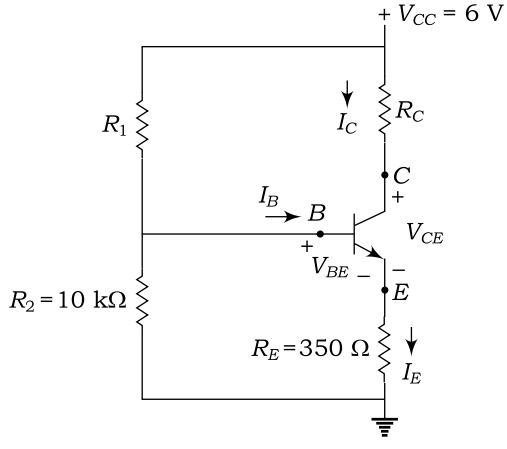


Fig. 2.121

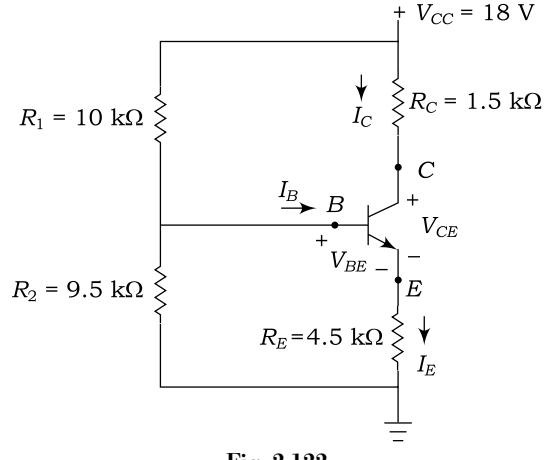


Fig. 2.122

49. Figure 2.122 shows the voltage-divider bias circuit. Determine the emitter current and collector to emitter voltage. Calculate the collector potential V_C. Assume $V_{BE} = 0.7$ V and $\beta = 70$.
50. Figure 2.123 shows a transistor amplifier circuit. Determine the percentage change in collector current when the transistor with $\beta = 60$ is replaced by the transistor with $\beta = 100$. Assume $V_{BE} = 0.7$ V.
51. Figure 2.124 shows the voltage-divider bias circuit with $\beta = 65$. Determine the value of R_1, R_2 and R_E if the stability factor is 5, $V_{CE} = 10.0$ V and $I_C = 1.25$ mA.
52. Figure 2.125 shows the emitter-bias circuit. Determine the emitter current, collector current, collector to emitter voltage and stability factor. Assume $V_{BE} = 0.75$ V and $\beta = 70$.
53. The emitter bias circuit of an *NPN* transistor is depicted in Fig. 2.126. Explain how the *Q*-point changes when the value of β changes from 50 to 100. Assume $V_{BE} = 0.65$ V.
54. The divider biasing circuit of a *PNP* transistor is depicted in Fig. 2.127. Determine the *Q*-point of the circuit when the value of β is 55. Assume $V_{BE} = 0.6$ V.

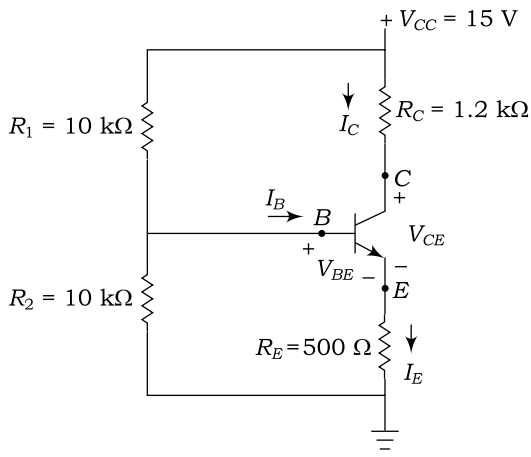


Fig. 2.123

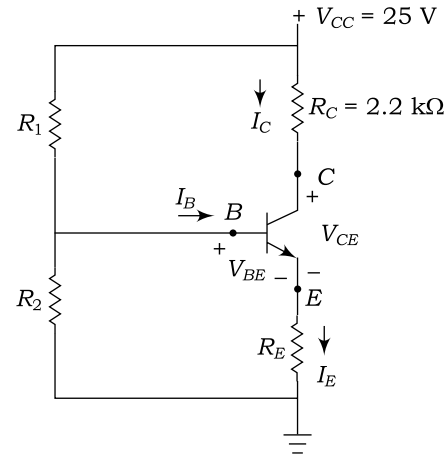


Fig. 2.124

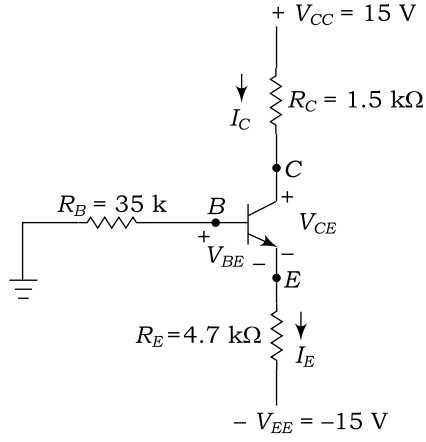


Fig. 2.125

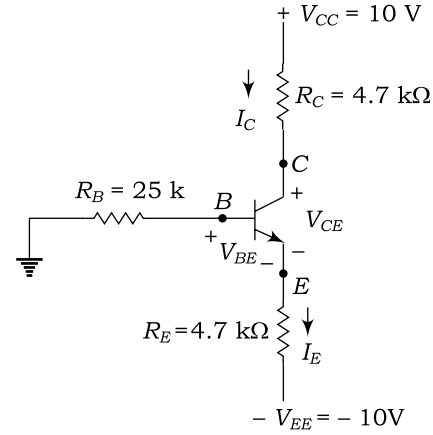


Fig. 2.126

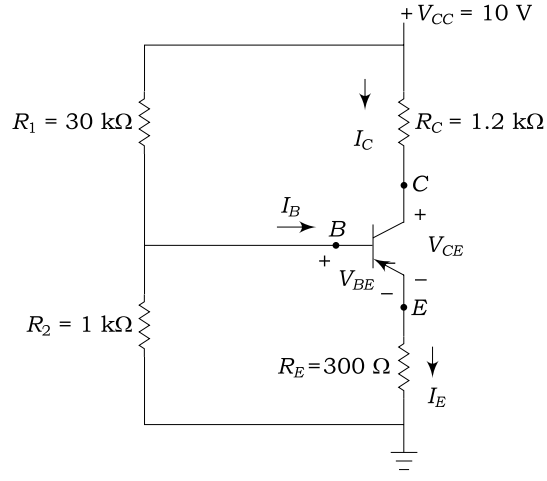


Fig. 2.127

55. With the help of load line and Q-point explain thermal instability of a *CE* amplifier.
56. Draw the circuit diagram of a self-bias circuit and explain physically how the stability is improved.
57. Explain 'thermal runway' of BJT.
58. List the three sources of instability of collector current in a transistor. Define the three stability factors.
59. Draw and explain a circuit which uses a diode to compensate for changes (i) in V_{BE} and (ii) I_{CO}.
60. Define the stability factor. Draw and explain the operation of transistor connected in *CB* mode.
61. Draw the Eber's–Moll model of the *pnp*-transistor and give the equations for the emitter current and collector current.
62. (a) Define transistor biasing and quiscent point. What are the factors that affect the bias stability of a transistor.
    (b) Write short note on the following:
        (i) Emitter follower circuit
        (ii) Bias compensation
        (iii) High frequency model of transistor
        (iv) Transconductance and transresistance amplifier

ANSWERS

Multiple-Choice Questions

1. (a)	2. (a)	3. (b)	4. (b)	5. (a)	6. (a,c)	7. (d)
8. (a)	9. (d)	10. (a)	11. (a)	12. (b)	13. (c)	14. (d)
15. (a)	16. (b)	17. (a)	18. (a)	19. (c)	20. (a)	21. (b)
22. (c)	23. (a)	24. (b)	25. (a)	26. (c)	27. (a)	28. (a)
29. (a)	30. (c)	31. (b)	32. (a)	33. (c)	34. (a)	35. (a)
36. (c)	37. (a)	38. (d)	39. (c)	40. (d)		

CHAPTER

3

Transistor Amplifier

3.1 INTRODUCTION

An amplifier is an electronic circuit that increases the amplitude of applied input signal. Usually, a small ac input signal is fed to the amplifier and a large ac output signal is obtained from the amplifier. The input signal will be either voltage or current, and correspondingly the output signal will be voltage or current. The input signal can be obtained from a transducer such as thermocouple and strain gauge, magnetic tape head, CD player, or microphone, etc. The output signal is applied to a loudspeaker in an audio amplifier, a motor drive in servo applications or an electromagnetic relay in control applications.

The basic block diagram of an audio amplifier system is shown in Fig. 3.1. The dc voltage source is connected to the amplifier and it is used as a source of energy for amplification. Generally, a battery or a dc rectifier with filter is a source of dc voltage. The amplifier contains transistors that must be biased in the forward-active region so that the transistors can act as amplifying devices. The microphone generates a very small signal in millivolt range and the amplifier produces a large voltage output signal which has sufficient power to drive the loudspeaker. The output of the speaker should be exactly same as the input signal of the microphone. Therefore, the output signal will be linearly proportional to the input signal.

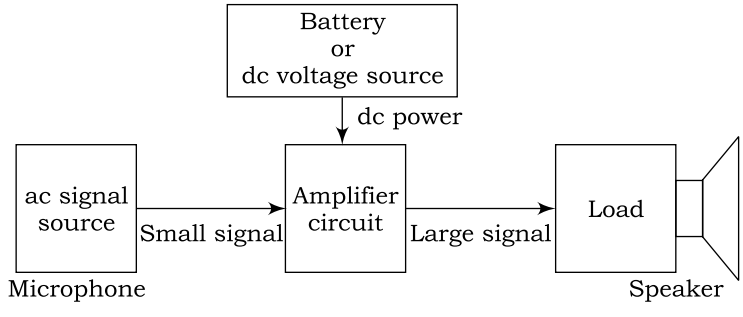


Fig. 3.1 Block diagram of an audio amplifier system

The ac input signal is an analog signal. The amplitude of an analog signal will be of any value within limits and can vary continuously with time. When an electronic circuit processes analog signals, it is called an *analog circuit*. An amplifier circuit is an example of an analog circuit and it is extensively used in radio, television, mobile phones and any communication equipments. Active devices such as bipolar junction transistor (BJT) and field effect transistors (FET) are commonly used in amplifier circuits. In this chapter, the operation of small-signal single-stage and multistage common-emitter (*CE*), common-collector (*CC*) and common-base amplifiers are discussed in detail. The frequency response of BJT amplifiers and large-signal amplifiers are also incorporated in this chapter.

3.2 LINEAR AND NONLINEAR AMPLIFIERS

A *linear amplifier* is an electronic circuit whose output signal is directly proportional to its input signal, but it has the capability to deliver more power into a load. The linear amplifier is usually used in radio-frequency (RF) power amplifier, and in amateur radio. Similarly, a *nonlinear amplifier* is one in which the output signal is not directly proportional to the input signal.

In a linear amplifier, the superposition principle can be applied. The principle of superposition states that the output of a linear circuit excited by multiple independent input signals is the sum of the outputs of the circuit corresponding to each of the input signals alone.

There are two types of analysis of the linear amplifier circuits such as *dc analysis* and *ac analysis*. In dc analysis, the applied voltage is the dc source, but in ac analysis, the time-varying ac input signal is used as a source.

1. dc Analysis

In dc analysis, the following steps are adopted:

(a) Initially, all ac sources are set to zero. Therefore, ac voltage source is replaced by a short circuit and current source is replaced by an open circuit.

(b) We assume that all capacitors are open circuit as they block dc current and analyse the transistor circuit using the simple large signal mode.

This analysis is also known as *large-signal analysis*, which establishes the *Q*-point of the transistors in the amplifier.

2. ac Analysis

The ac analysis is also known as *small-signal analysis* and it can be performed by the following steps:

(a) All dc sources are set to zero.

(b) All coupling capacitors are short circuit.

(c) Replace the BJT with its small-signal model.

(d) Solve KVL and KCL equations to determine voltage and current transfer functions, and input and output impedances.

(e) Determine the cut-off frequencies of the amplifier circuit.

The total response of the amplifier circuit is the sum of the responses of dc analysis and ac analysis. The above techniques are used in the analysis of small signal single stage and multistage common-emitter (*CE*), common-collector (*CC*) and common-base (*CB*) amplifiers.

3.3 CLASSIFICATION OF AMPLIFIERS

The linear amplifiers can be classified depending upon their mode of operation such as follows:

1. *Based on transistor configuration*
   - Common emitter (*CE*) amplifier
   - Common collector (*CC*) amplifier
   - Common base (*CB*) amplifier
2. *Based on input signals*
   - Small signal amplifier
   - Large signal amplifier
3. *Based on output*
   - Voltage amplifier
   - Power amplifier
4. *Based on active device*
   - BJT amplifier
   - FET amplifier
5. *Based on operating condition*
   - Class A amplifier
   - Class B amplifier
   - Class AB amplifier
   - Class C amplifier
   - Class D amplifier
6. *Based on frequency*
   - Audio-frequency (AF) amplifier
   - Intermediate frequency (IF) amplifier
   - Radio-frequency (AF) amplifier
7. *Based on number of stages*
   - Single-stage amplifier
   - Multistage amplifier
8. *Based on the method of coupling between two stages*
   - Direct coupling(dc) amplifier
   - RC coupled amplifier
   - Transformer coupled amplifier.

3.4 BIPOLAR JUNCTION TRANSISTOR (BJT) AS A LINEAR AMPLIFIER

Figure 3.2 shows a Bipolar Junction Transistor (BJT) which acts as a *linear amplifier*. In this circuit, the base-emitter junction is forward biased by V_{BB} and the collector-base junction is reverse biased by V_{CC}. Then the transistor operates in *active region*. v_i is the sinusoidal ac input voltage. The resistance R_B is the source resistance. The amplitude of input signal v_i is such that emitter-base junction is always forward biased regardless of the polarity of ac input voltage signal v_i. Figure 3.3 shows the dc bias and ac voltage signal in the base of bipolar junction transistor and it is an alternative representation of Fig. 3.2.

Initially, assume that there is no ac signal source. Then the dc base current I_B flows through resistance R_B and correspondingly dc collector current I_C flows through resistance R_C. This collector current is known as *quiescent operating current*.

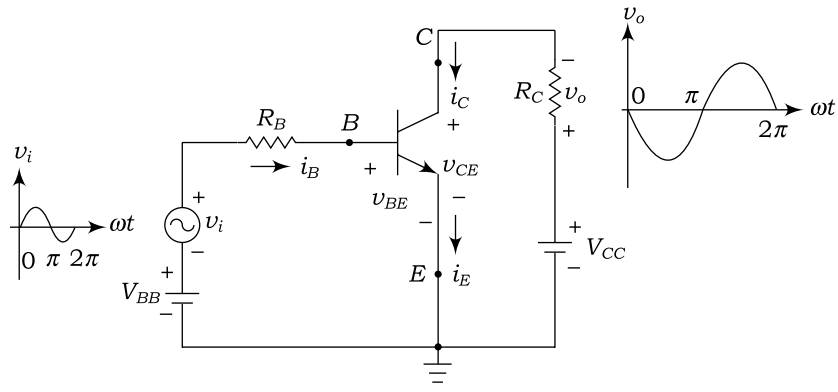


Fig. 3.2 Common-emitter amplifier

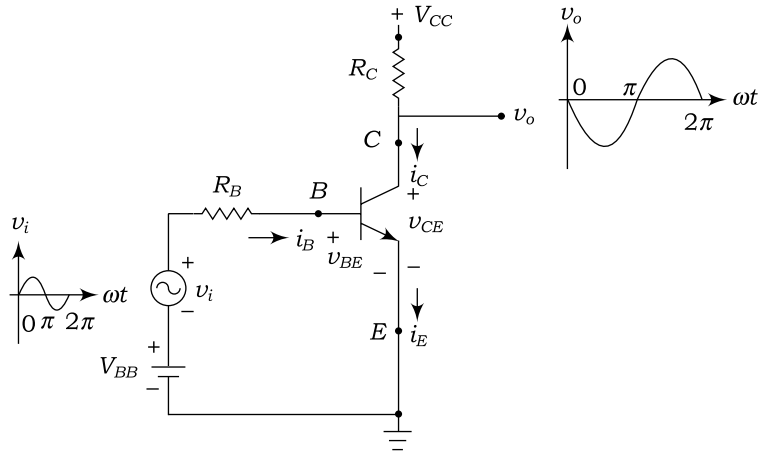


Fig. 3.3 dc bias and ac voltage signal in the base of bipolar junction transistor

When an ac signal is applied between the emitter-base junctions, the forward bias voltage across the emitter-base junction is increased during the positive half-cycle of input ac voltage signal v_i. Consequently, more electrons are injected into the base and they reach the collector. As a result, the collector current increases. Due to increase of the collector current I_C, the voltage drop across R_C is increased.

In the negative half-cycle of input ac voltage signal v_i, the forward bias voltage across the emitter-base junction decreases. Subsequently, the collector current decreases and the voltage drop across R_C decreases. The above relationship corresponds to the slope of the curve at the *quiescent (Q) operating* point.

Actually, a time-varying ac input voltage v_i across the base-emitter junction generates a time-varying base current i_B as shown in Fig. 3.4.

Assume

I_B is the dc value of base current,
V_{BE} is the dc value of base emitter voltage,
i_b is the ac value of base current, and
v_{be} is the ac value of base emitter voltage.

Then,

i_B is the total instantaneous value of base current, i.e., $i_B = I_B + i_b$,

v_B is the total instantaneous value of base emitter voltage, i.e., $v_{BE} = V_{BE} + v_{be}$

The relationship between the ac base emitter voltage and ac base current is

$$i_B = \frac{I_S}{\beta} e^{\frac{v_{BE}}{V_T}}$$

where, $v_{BE} = V_{BEQ} + v_{be}$, V_{BEQ} is the base emitter turn-on voltage at Q-point, and v_{be} is the ac input voltage across base and emitter.

Therefore,

$$i_B = \frac{I_S}{\beta} e^{\frac{V_{BEQ} + v_{be}}{V_T}}$$

$$= \frac{I_S}{\beta} e^{\frac{V_{BEQ}}{V_T}} e^{\frac{v_{be}}{V_T}} \quad (3.1)$$

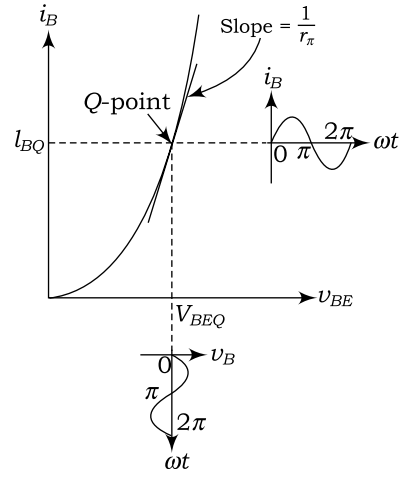


Fig. 3.4 The base current iB versus base-emitter voltage v_{BE} characteristics with superimposed sinusoidal ac input voltage v_{be}

Since $\frac{I_S}{\beta} e^{\frac{V_{BEQ}}{V_T}}$ is called the *quiescent base current* I_{BQ}, we can write, $i_B = I_{BQ} e^{\frac{v_{be}}{V_T}}$

Therefore, the base current i_B is nonlinear and cannot be represented by superposition of an ac current and a dc quiescent current.

Using Taylor series, the above equation can be expressed as

$$i_B = I_{BQ}\left[1 + \frac{v_{be}}{V_T} + \frac{1}{2}\left(\frac{v_{be}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{v_{be}}{V_T}\right)^3 + \ldots\ldots\right]$$

As $e^x = 1 + x + \frac{1}{2}x^2 + \frac{1}{6}x^3 + \ldots$ and $x = \frac{v_{be}}{V_T}$

Then $i_B = I_{BQ}\left[1 + \frac{v_{be}}{V_T}\right]$ as $V_T >> v_{be}$ and $\left(\frac{v_{be}}{V_T}\right)^2$ is negligible

or $i_B = I_{BQ} + \frac{I_{BQ}}{V_T} v_{be}$

or $i_B = I_{BQ} + i_b \quad (3.2)$

where, $i_b = \frac{I_{BQ}}{V_T} v_{be}$ is the sinusoidal base current as the v_{be} is sinusoidal base emitter voltage.

At the quiescent (Q) point, V_{BB} is a dc voltage which can forward bias the emitter-base junction of transistor and transistor operates in active region. When a time-varying ac signal is superimposed with dc voltage V_{BB}, the output voltage can be generated according to transfer characteristics of BJT. Then output voltage is also time varying and it has 180° phase shift from input voltage. Since the amplitude is time varying output voltage v_o is directly proportional to the ac input voltage v_i, this circuit is called *linear amplifier*.

At the Q-point, I_{BQ} is the base current, I_{CQ} is the collector current, V_{BEQ} is the base-emitter voltage, V_{CEQ} is the collector-emitter voltage. i_b is the ac component of base current, i_c is the ac component of collector current, v_{be} is the ac base-emitter voltage, and v_{ce} is the ac collector-emitter voltage. The dc equivalent circuit

of Fig. 3.3 is depicted in Fig. 3.5(a) and Fig. 3.5(b) shows the ac equivalent circuit of Fig. 3.3. The voltage transfer characteristics of bipolar junction transistor are illustrated in Fig. 3.6.

Applying the superposition theorem to a linear circuit, we obtain

$$i_B = I_{BQ} + i_b, \qquad i_C = I_{CQ} + i_c$$

$$v_{BE} = V_{BEQ} + v_{be}, \text{ and} \qquad v_{CE} = V_{CEQ} + v_{ce}$$

The KVL equation in the base-emitter loop is

$$V_{BB} = I_{BQ}R_B + V_{BEQ} \tag{3.3}$$

The KVL equation in the collector-emitter loop is

$$V_{CC} = I_{CQ}R_C + V_{CEQ} \tag{3.4}$$

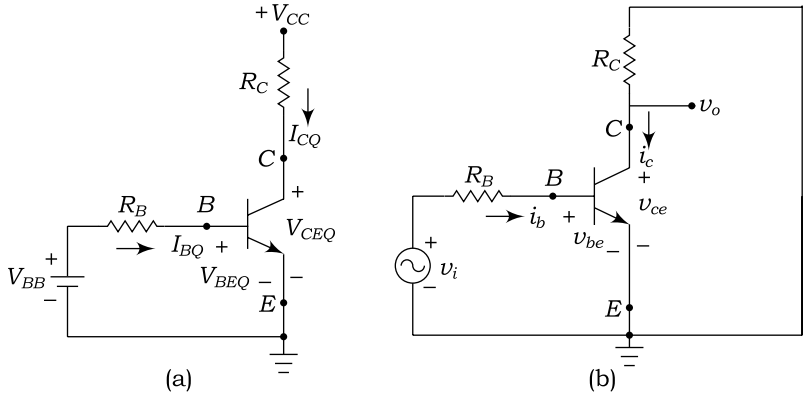


Fig. 3.5 (a) dc equivalent circuit of Fig. 3.3 (b) ac equivalent circuit of Fig. 3.3

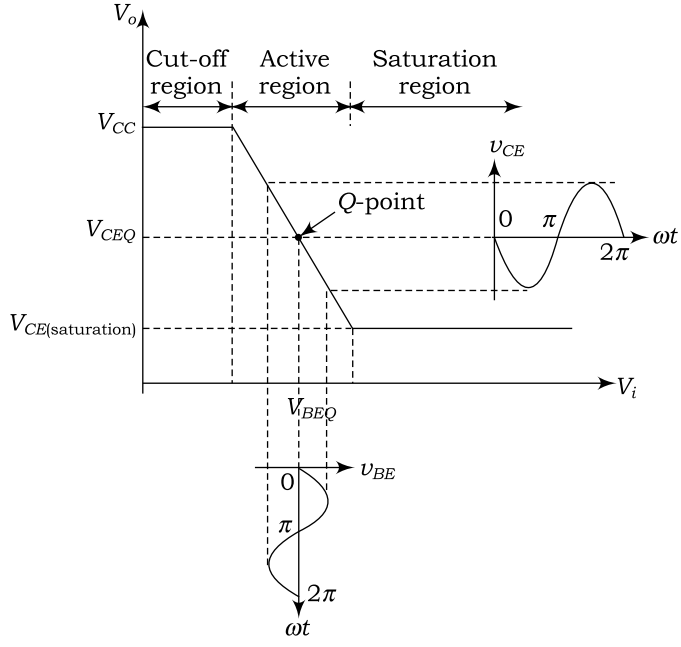


Fig. 3.6 Voltage transfer characteristics of bipolar junction transistor

When ac signal is incorporated in the base emitter loop equation, we get

$$\begin{aligned} V_{BB} + v_i &= i_B R_B + v_{BE} \\ &= (I_{BQ} + i_b)R_B + (V_{BEQ} + v_{be}) \quad \text{as } i_B = I_{BQ} + i_b \quad \text{and} \quad v_{BE} = V_{BEQ} + v_{be} \\ &= I_{BQ}R_B + i_b R_B + V_{BEQ} + v_{be} = I_{BQ}R_B + V_{BEQ} + i_b R_B + v_{be} \\ &= V_{BB} + i_b R_B + v_{be} \quad \text{as } V_{BB} = I_{BQ}R_B + V_{BEQ} \end{aligned}$$

Then $v_i = i_b R_B + v_{be}$

This base-emitter loop equation is justified only when an ac signal is present.

The collector-emitter loop equation can be written as

$$\begin{aligned} V_{CC} &= i_C R_C + v_{CE} \\ &= (I_{CQ} + i_c)R_C + (V_{CEQ} + v_{ce}) \quad \text{as } i_C = I_{CQ} + i_c \text{ and } v_{CE} = V_{CEQ} + v_{ce} \\ &= I_{CQ}R_C + i_c R_C + V_{CEQ} + v_{ce} = I_{CQ}R_C + V_{CEQ} + i_c R_C + v_{ce} \end{aligned}$$

Therefore, $i_c R_C + v_{ce} = 0$ as $V_{CC} = I_{CQ}R_C + V_{CEQ}$ (3.5)

This is the collector-emitter loop equation only when an ac signal is present and all the dc terms are set to zero.

The common-emitter characteristics of bipolar junction transistor, dc load line and quiescent (Q) operating point are depicted in Fig. 3.7. Due to sinusoidal input voltage v_i, a time-varying base current flows through base of BJT. Then time-varying base current generates an ac collector current which is superimposed on the quiescent collector current I_{CQ}. Subsequently, voltage across R_C is ac and collector emitter voltage is also ac. Figure 3.8 shows the base-emitter voltage v_{BE}, base current i_B, collector current i_C and collector-emitter voltage v_{CE}.

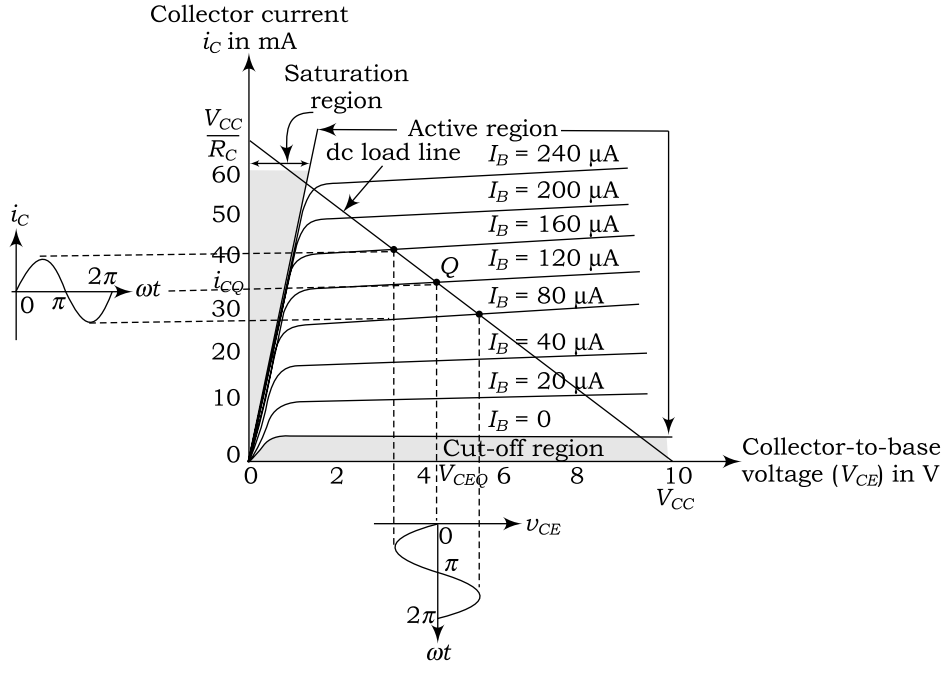


Fig. 3.7 Common-emitter characteristics, dc load line, collector current and collector-emitter voltage

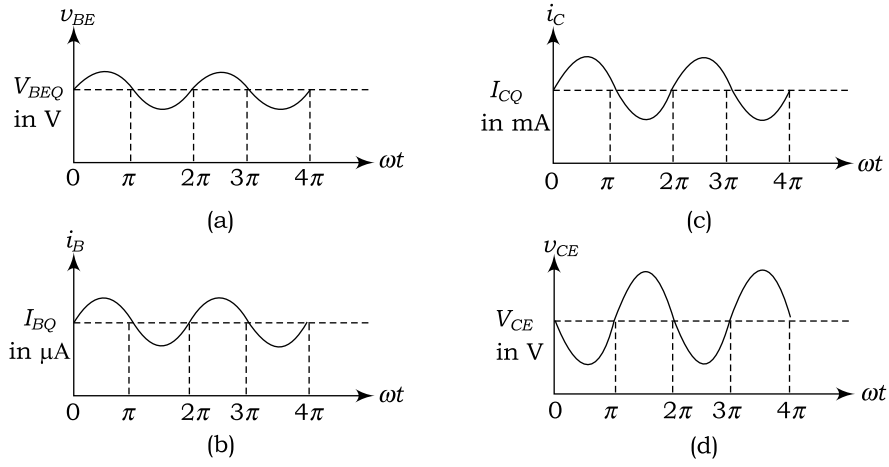


Fig. 3.8 (a) Base emitter voltage v_{BE} (b) Base current i_B (c) Collector current i_C (d) Collector-emitter voltage v_{CE}

It is clear from Fig. 3.8 that a small voltage change at the base generates a large voltage change at the collector and the circuit operates as amplifier. The amplitude of ac collector-emitter voltage, i.e., output voltage is larger than the sinusoidal input voltage. The voltage gain of amplifier can be expressed as

$$A_v = \frac{v_{ce}}{v_{be}}$$

When 8 mV peak change in v_{BE} provide 5 μA change in base current i_B and 0.5 mA change in i_C. The 0.5 mA change in i_C generates a 1.6 V change in v_{CE}. Then voltage gain is

$$A_v = \frac{v_{ce}}{v_{be}} = \frac{v_o}{v_i} = \frac{1.6\angle 180^\circ}{0.008\angle 0^\circ} = 200\angle 180^\circ = -200$$

The negative sign represents a 180° phase shift between input and output voltages.

3.5 SMALL-SIGNAL EQUIVALENT CIRCUIT OF BIPOLAR JUNCTION TRANSISTOR

Figure 3.9 shows bipolar junction transistor (BJT) as a small signal two-port network. For small-signal analysis of BJT, it is required to develop a small-signal equivalent circuit for the BJT. This circuit can be represented by hybrid-π model, *h*-parameter model and r_e model. In this section, Hybrid π model, *h*-parameter model and r_e model of BJT are discussed in detail.

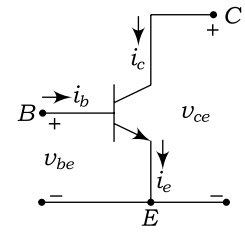


Fig. 3.9 BJT as a small-signal two-port network

3.5.1 Hybrid-π Model

The hybrid-π model of the circuit is closely related to the physics of the transistor. Figure 3.4 shows the base current versus base-emitter voltage characteristic, with small time-varying signals superimposed at the *Q*-point. As the sinusoidal signals are small, the slope at the *Q*-point is constant and its unit is conductance. The inverse of this conductance is the small-signal resistance defined as $r_\pi \cdot r_\pi$ is also known as *base-emitter input resistance* or *diffusion resistance*.

The relation between the small-signal input base current i_b to the small-signal input voltage is

$$v_{be} = i_b r_\pi$$

where, i_b is base current, v_{be} is base-emitter voltage, and $\frac{1}{r_\pi}$ is slope of the base current (i_B) versus base-emitter voltage (v_{BE}) characteristic at Q-point.

Then

$$\begin{aligned}\frac{1}{r_\pi} &= \frac{\partial i_B}{\partial v_{BE}}\Big|_{\text{at}-Q-\text{point}} \\ &= \frac{\partial}{\partial v_{BE}}\left[\frac{I_S}{\beta}e^{\frac{v_{BE}}{V_T}}\right]\Big|_{\text{at}-Q-\text{point}} \\ &= \frac{1}{V_T}\times\left[\frac{I_S}{\beta}e^{\frac{v_{BE}}{V_T}}\right]\Big|_{\text{at}-Q-\text{point}} = \frac{I_{BQ}}{V_T} \quad \text{as } I_{BQ} = \left[\frac{I_S}{\beta}e^{\frac{v_{BE}}{V_T}}\right]\Big|_{\text{at}-Q-\text{point}}\end{aligned} \tag{3.6}$$

Since $I_{CQ} = \beta I_{BQ}$, we can write $\frac{1}{r_\pi} = \frac{I_{BQ}}{V_T} = \frac{I_{CQ}}{\beta V_T}$

Then the base-emitter input resistance is equal to

$$r_\pi = \frac{v_{be}}{i_b} = \frac{V_T}{I_{BQ}} = \frac{\beta V_T}{I_{CQ}}$$

Assume that the output collector current is independent of collector-emitter voltage and the collector current is a function of base-emitter voltage only. Then we can write

$$\Delta i_C = \frac{\partial i_C}{\partial v_{BE}}\Big|_{\text{at}-Q-\text{point}} \times \Delta v_{BE}$$

The above equation can be written as

$$i_c = \frac{\partial i_C}{\partial v_{BE}}\Big|_{\text{at}-Q-\text{point}} \times \Delta v_{be} \quad \text{as } \Delta i_C = i_c \text{ and } \Delta v_{BE} = v_{be} \tag{3.7}$$

Since the collector current i_C is equal to $i_C = I_S e^{\frac{v_{BE}}{V_T}}$

$$\frac{\partial i_C}{\partial v_{BE}}\Big|_{\text{at}-Q-\text{point}} = \frac{\partial}{\partial v_{BE}}\left[I_S e^{\frac{v_{BE}}{V_T}}\right]\Big|_{\text{at}-Q-\text{point}} = \frac{1}{V_T}\times\left[I_S e^{\frac{v_{BE}}{V_T}}\right]\Big|_{\text{at}-Q-\text{point}} \tag{3.8}$$

The term $\left[I_S e^{\frac{v_{BE}}{V_T}}\right]\Big|_{\text{at}-Q-\text{point}}$ is equal to the quiescent collector current I_{CQ}, the above equation is equal to

$$\frac{\partial i_C}{\partial v_{BE}}\Big|_{\text{at}-Q-\text{point}} = \frac{I_{CQ}}{V_T} \tag{3.9}$$

Since the term $\frac{I_{CQ}}{V_T}$ is a conductance which relates the collector current and base-emitter voltage. This parameter is called *transconductance* and can be expressed as

$$g_m = \frac{I_{CQ}}{V_T}$$

The small-signal collector current can be expressed in terms of the small signal base current as follows:

$$\Delta i_C = \frac{\partial i_C}{\partial i_B}\Big|_{\text{at}-Q-\text{point}} \times \Delta i_B$$

or

$$i_c = \frac{\partial i_C}{\partial i_B}\Big|_{\text{at}-Q-\text{point}} \times i_b \quad \text{as } \Delta i_C = i_c \text{ and } \Delta i_B = i_b \tag{3.10}$$

Since $\frac{\partial i_C}{\partial i_B}\Big|_{\text{at}-Q-\text{point}} = \beta$ is an incremental or ac common-emitter current gain, the small signal collector current i_c can be expressed as

$$i_c = \beta i_b \tag{3.11}$$

The most simplified small-signal hybrid-π equivalent circuit of an *NPN* transistor with r_π and g_m is depicted in Fig. 3.10(a) and the small-signal hybrid-π equivalent circuit of *NPN* transistor using common-emitter current gain β is shown in Fig. 3.10(b).

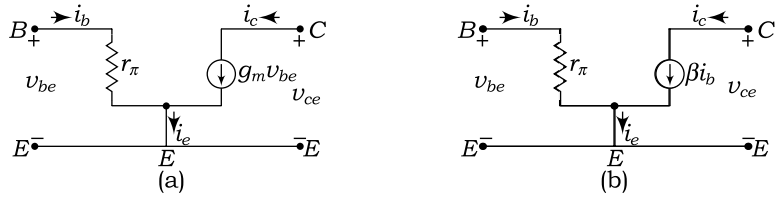


Fig. 3.10 (a) The most simplified small-signal hybrid-π equivalent circuit of an NPN transistor with r_π and g_m (b) The small-signal hybrid-π equivalent circuit of NPN transistor using common-emitter current gain β

1. ac Beta

The common-emitter current gain is actually defined as an ac *beta* and it is the ratio of ac collector current to an ac base current. It is represented by $\beta = \frac{i_c}{i_b}$.

2. dc Beta

β_{dc} is the ratio of a dc collector current (I_C) to the corresponding dc base current (I_B) and it is represented by $\beta_{dc} = \frac{I_C}{I_B}$. In this case, leakage currents are included. If we assume that leakage currents are negligible, the two definitions of beta are equivalent.

When the small-signal hybrid-π parameters r_π and g_m are multiplied, we obtain

$$r_\pi g_m = \frac{\beta V_T}{I_{CQ}} \times \frac{I_{CQ}}{V_T} = \beta \quad \text{as } r_\pi = \frac{\beta V_T}{I_{CQ}} \text{ and } g_m = \frac{I_{CQ}}{V_T} \tag{3.12}$$

Usually, the common-emitter current gain β is constant for a transistor. But the value of β varies from one transistor to another transistor and it also depends on the collector current. The variation of β with respect to collector current is specified on data sheets of specific transistors.

Figure 3.11 shows the small-signal equivalent circuit of common-emitter amplifier circuit as shown in Fig. 3.2. The small-signal voltage gain is the ratio of output voltage signal to input voltage signal and it can be expressed as

$$A_v = \frac{v_o}{v_i}$$

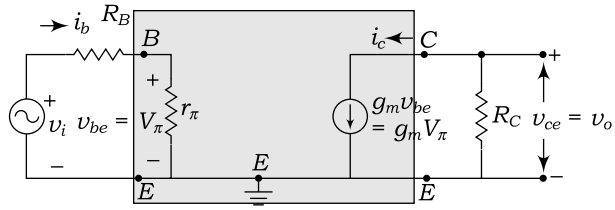


Fig. 3.11 The small-signal equivalent circuit of common-emitter amplifier circuit

The small-signal base emitter voltage is V_π which is called the *control voltage*. The voltage-dependent current source is represented by $g_m V_\pi$. As $g_m V_\pi$ current flows through resistance R_C, the output voltage is equal to the collector emitter voltage and it can be expressed as

$$v_o = v_{ce} = -g_m V_\pi R_C \tag{3.13}$$

The voltage across the resistance r_π is

$$V_\pi = \frac{r_\pi}{R_B + r_\pi} v_i$$

After substituting the value of V_π in Eq. (3.13), we get

$$v_o = -g_m \frac{r_\pi}{R_B + r_\pi} v_i R_C = -g_m \frac{r_\pi}{R_B + r_\pi} R_C v_i \tag{3.14}$$

Then small-signal voltage gain is

$$A_v = \frac{v_o}{v_i} = -g_m \frac{r_\pi}{R_B + r_\pi} R_C$$

Due to early effect, the collector current varies with collector-emitter voltage and it can be expressed as

$$i_C = I_S e^{\frac{v_{BE}}{V_T}} \times \left(1 + \frac{v_{CE}}{V_A}\right) \tag{3.15}$$

where, v_{CE} is the collector emitter voltage, and v_A is the early voltage.

The equivalent circuit can be expanded to consider the effect of early voltage and output resistance is incorporated with Fig. 3.12.

The output resistance r_o is equal to $r_o = \left.\frac{\partial v_{CE}}{\partial i_C}\right|_{\text{at}-Q-\text{point}}$

Then, $\frac{1}{r_o} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{\text{at}-Q-\text{point}}$

$$= \frac{\partial}{\partial v_{CE}} \left[I_S e^{\frac{v_{BE}}{V_T}} \left(1 + \frac{v_{CE}}{V_A}\right) \right] \Bigg|_{\text{at}-Q-\text{point}} \quad \text{as } i_C = I_S e^{\frac{v_{BE}}{V_T}} \times \left(1 + \frac{v_{CE}}{V_A}\right)$$

$$= \left[I_S e^{\frac{v_{BE}}{V_T}} \times \frac{1}{V_A} \right] \Bigg|_{\text{at}-Q-\text{point}} = \frac{1}{V_A} \times \left[I_S e^{\frac{v_{BE}}{V_T}} \right] \Bigg|_{\text{at}-Q-\text{point}}$$

$$= \frac{I_{CQ}}{V_A} \quad \text{as } I_{CQ} = \frac{1}{V_A} \times \left[I_S e^{\frac{v_{BE}}{V_T}} \right] \Big|_{\text{at}-Q-\text{point}} \tag{3.16}$$

Therefore, the small-signal output resistance r_o is $r_o = \dfrac{V_A}{I_{CQ}}$ (3.17)

The resistance r_o can be used as a Norton equivalent resistance and it is connected in parallel with the dependent current source. The modified equivalent circuit of BJT incorporating r_o is shown in Fig. 3.12.

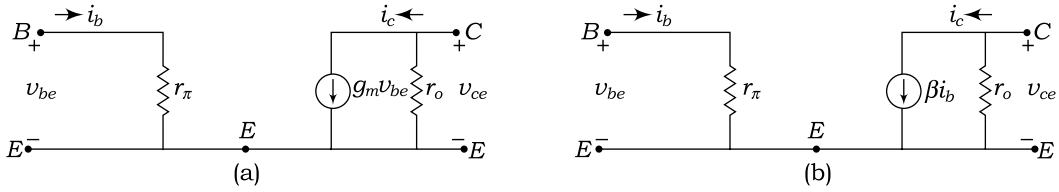


Fig. 3.12 (a) The most simplified small-signal hybrid-π equivalent circuit of NPN transistor with r_π, g_m and r_o (b) The small-signal hybrid-π equivalent circuit of NPN transistor using common-emitter current gain β

3.5.2 r_e Model of Bipolar Junction Transistor

Since the *h*-parameter values of transistors will vary with same type of different transistors, the accuracy of circuit analysis deepens upon the operating conditions. Therefore, an alternative r_e model of a bipolar junction transistor is used in circuit analysis. In this model, resistance values and β are required for proper circuit analysis. The advantages of r_e model of bipolar junction transistor are given below:

1. Required parameters are available very easily.
2. Analysis is very simple and easy.
3. Accuracy of circuit analysis is good.

In a common-emitter configuration, the base-emitter junction is forward biased and the collector current I_C is β times base current I_B and it can be expressed as $I_C = \beta I_B$. The dc equivalent circuit of an *NPN* transistor in common-emitter (CE) configuration is shown in Fig. 3.13. During ac condition, the *ac resistance of the base emitter junction* is equal to

$$r_{ac} = \frac{25\text{ mV}}{I_B}$$

As $I_B = \dfrac{I_C}{\beta} \cong \dfrac{I_E}{\beta}$, the ac resistance is

$$r_{ac} = \frac{25\text{ mV}}{I_B} = \frac{25\text{ mV}}{\frac{I_E}{\beta}} = \beta\frac{25\text{ mV}}{I_E} = \beta r_e \quad \text{as} \quad \frac{25\text{ mV}}{I_E} = r_e$$

where, r_e is the ac emitter resistance of the emitter diode and its value is determined from $r_e = \dfrac{25\text{ mV}}{I_E}$

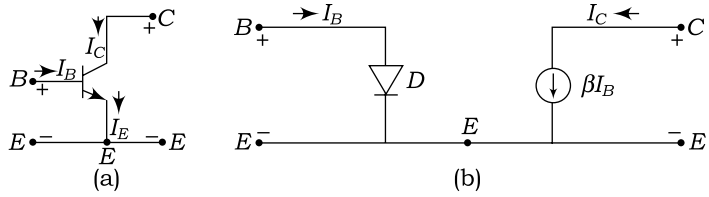


Fig. 3.13 (a) NPN bipolar junction transistor in CE configuration (b) dc equivalent circuit of Fig. 3.13(a)

When the ac resistance is placed in Fig. 3.13(b), we get r_e model of *NPN* transistor in common-emitter (*CE*) configuration as shown in Fig. 3.14(a). The approximate hybrid-equivalent circuit of an *NPN* transistor in common-emitter (*CE*) configuration is shown in Fig. 3.14(b). If we compare Fig. 3.14(a) and Fig. 3.14(b), we get

$$h_{ie} = \beta r_e \quad \text{and} \quad h_{fe} = \beta$$

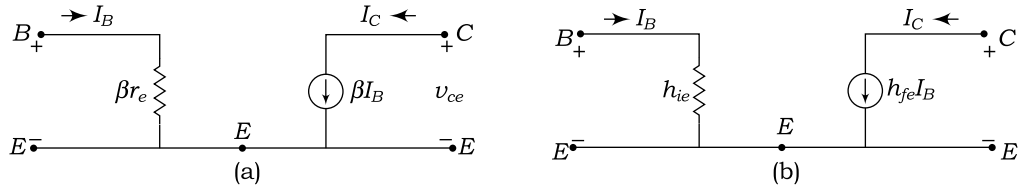


Fig. 3.14 (a) r_e model of npn transistor of NPN transistor in CE configuration (b) Approximate hybrid-π equivalent circuit of Fig. 3.14

In common-base configuration of *PNP* transistor, the emitter-base *PN*-junction diode is forward biased and collector current is equal to emitter current. The dc equivalent circuit of a *PNP* transistor is shown in Fig. 3.15(b). For an *NPN* transistor, the diode is reversed and the direction of current flow is also reversed as shown in Fig. 3.15(d).

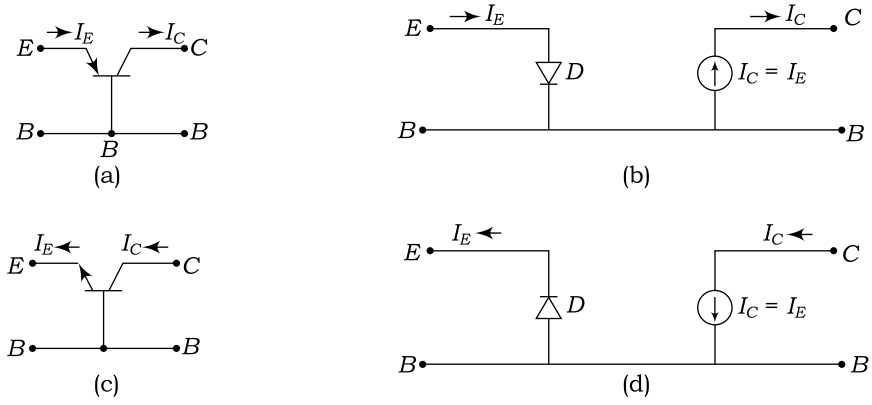


Fig. 3.15 (a) Common-base configuration of PNP transistor (b) dc equivalent circuit of PNP transistor (c) Common-base configuration of NPN transistor (d) dc equivalent circuit of NPN transistor

When small ac input voltage is applied, the emitter-base junction diode provides ac resistance. The current flow through the diode is equal to the emitter current and the ac resistance of the diode is represented by r_e. The value of r_e can determined from the equation

$$r_e = \frac{25 \text{ mV}}{I_E}$$

After substituting the ac resistance of diode r_e in Fig. 3.15(d), we get the r_e model equivalent circuit of an *NPN* transistor as shown in Fig. 3.16(a). The approximate *h*-parameter equivalent circuit of *NPN* transistor in common-base configuration is depicted in Fig. 3.16(b). When we compare Fig. 3.16(a) and Fig. 3.16(b), we find $h_{ib} = r_e$ and $h_{fb} = -1$.

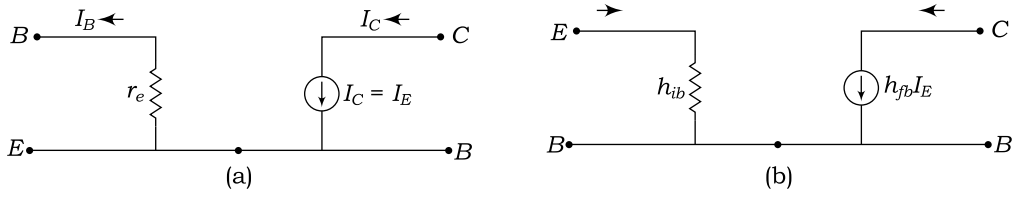


Fig. 3.16 (a) r_e model of NPN transistor of NPN transistor in CB configuration (b) Approximate hybrid-π equivalent circuit of Fig. 3.16(b)

Example 3.1 What is the ac resistance of the emitter diode if the dc emitter current is 1.25 mA?

Sol. The value of ac resistance of emitter diode is $r_e = \dfrac{25\text{ mV}}{I_E} = \dfrac{25\text{ mV}}{1.25\text{ mA}} = 20\ \Omega$

Example 3.2 What is the dc emitter current if the ac resistance of the emitter diode is 40 Ω?

Sol. The value of dc emitter current is $I_E = \dfrac{25\text{ mV}}{r_e}$ as $r_e = \dfrac{25\text{ mV}}{I_E}$

$$= \frac{25\text{ mV}}{40\ \Omega} = 0.625\text{ mA}$$

3.6 COMMON-EMITTER AMPLIFIER

Figure 3.17 shows a common-emitter amplifier circuit using *NPN* transistor. Its alternative representation is depicted in Fig. 3.18. The emitter-base junction of transistor is forward biased by the power supply V_{BB}. The collector-base junction of transistor is reverse biased by the power supply V_{CC}. Consequently, the transistor operates in the active region.

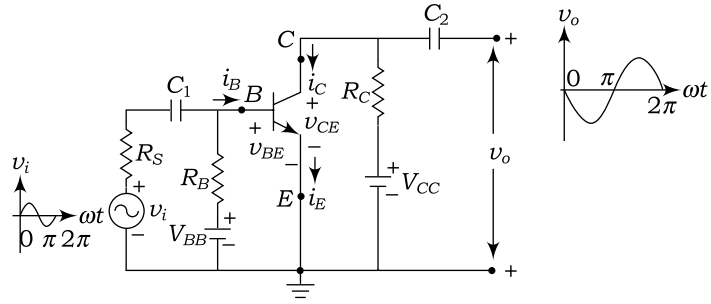


Fig. 3.17 Common-emitter amplifier circuit using NPN transistor

The quiescent (Q) operating can be determined by supply voltage V_{CC} and resistances R_B and R_C. The ac input voltage signal is applied to the base-emitter junction of transistor and the amplified output voltage signal is obtained from the collector and emitter terminals. Capacitors C_1 and C_2 are *coupling capacitors*. These capacitors are also known as *blocking capacitors*. Each capacitor acts as a switch. Capacitor behaves as open circuit to a direct current (dc), but behaves as short-circuit to alternating current (ac). In this way, coupling capacitors provide dc isolation at the input and output of the amplifier circuit. The function of C_1 is fed to ac input signal to base-emitter junction of transistor amplifier. Similarly, the function of C_2 is to connect the amplifier output to load resistance or the input of next stage amplifier.

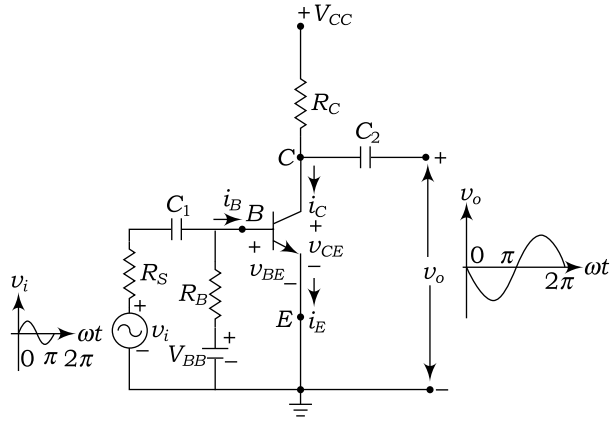


Fig. 3.18 Alternative common-emitter amplifier circuit using NPN transistor

Instead of two-power supply in Fig. 3.18, the common-emitter amplifier can be set up with a single power supply as shown in Fig. 3.19.

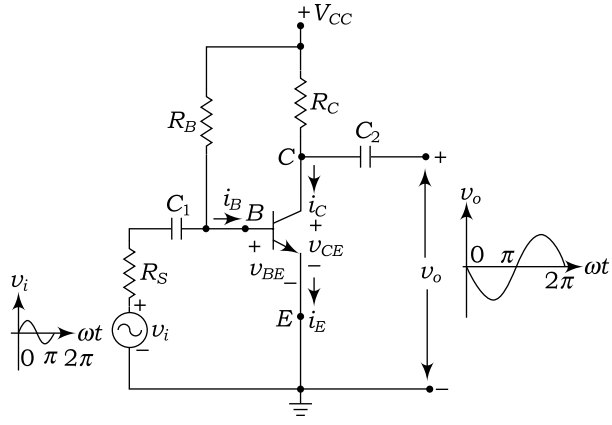


Fig. 3.19 Common-emitter amplifier with a single power supply

When there is no ac input signal, the base current of the transistor is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The collector current of transistor is $I_C = \beta I_B$ and the voltage across collector-emitter of transistor is equal to

$$V_{CE} = V_{CC} - I_C R_C$$

When a sinusoidal ac input voltage v_i is applied to the circuit during positive half-cycle of the input voltage, the forward bias voltage of base-emitter junction is increased. Subsequently, the base current i_B increases. Then the collector current is also increased by β times as $I_C = \beta I_B$ and V_{CE} is decreased as $V_{CE} = V_{CC} - I_C R_C$. Therefore, the output voltage is decreased.

During negative half-cycle of input voltage, the forward-bias voltage of base-emitter junction is decreased. As a result, the base current i_B decreases. After that the collector current is also decreased by β times as

$I_C = \beta I_B$ and V_{CE} is increased as $V_{CE} = V_{CC} - I_C R_C$. Consequently, the output voltage is increased. In this way 180° phase shift is introduced between the input and output signals, but the output signal is the amplified ac input signal with 180° phase shift as depicted in Fig. 3.20.

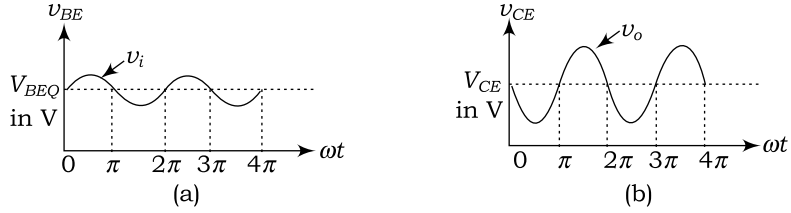


Fig. 3.20 (a) v_{BE} and input voltage v_i (b) v_{CE} and output voltage v_o

3.6.1 Characteristics of Common-Emitter Amplifier

A common-emitter amplifier has the following characteristics:

1. It has large voltage gain (A_v). The value of A_v is about 1500.
2. Its current gain (A_I) is very high. The value of A_I is in the range of 50 to 300.
3. It has very high power gain (A_P). The value of A_P is in the order of 10,000.
4. The output voltage has 180° phase shift with respect to input voltage.
5. Input impedance is moderately low and its value in the range of 1 kΩ to 2 kΩ.
6. Input impedance is moderately large and its value is about 50 kΩ.

3.6.2 Analysis of Common-Emitter Amplifier with Fixed Bias

Figure 3.21 shows a common-emitter amplifier circuit with fixed bias. The dc and ac analyses of Fig. 3.21 are explained below:

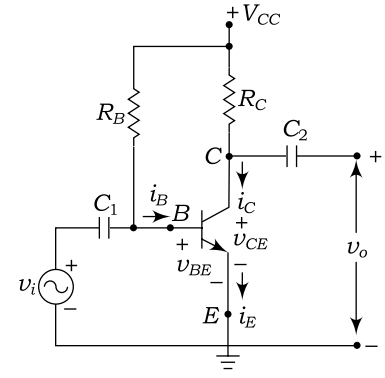


Fig. 3.21 Common-emitter amplifier with fixed bias

1. dc Analysis

With the capacitors open circuited, this circuit is same as good biasing circuit. The dc equivalent circuit of Fig. 3.21 is shown in Fig. 3.22(a).

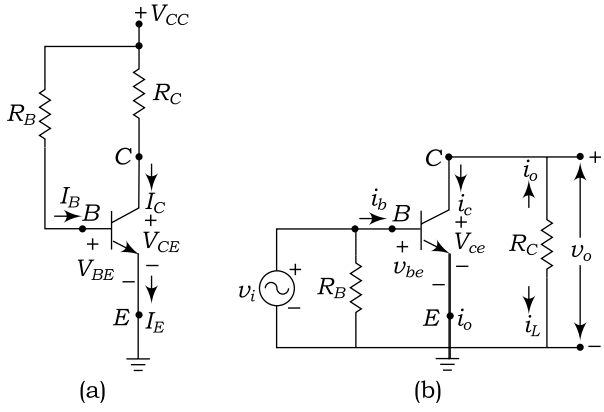


Fig. 3.22 (a) dc equivalent circuit of Fig. 3.21 (b) ac equivalent circuit of Fig. 3.22

The base current is $I_B = \dfrac{V_{CC}}{R_B}$

The collector current is equal to $I_C = \beta I_B$

The collector emitter voltage is $V_{CE} = V_{CC} - I_C R_C$

2. ac Analysis

The ac equivalent circuit of Fig. 3.21 can be drawn by the following steps:

(a) Remove all dc power supply by grounding them.

(b) Capacitors C_1 and C_2 are removed by short circuit.

Figure 3.22(b) shows the ac equivalent circuit of Fig. 3.21. This circuit can be analysed by using (i) hybrid-(h) model, (ii) hybrid-π equivalent circuit model, and (iii) r_e model of bipolar junction transistor.

(i) Analysis in *h*-parameter Model After substituting the approximate h-parameter model of the transistor, we get the ac equivalent circuit of common-emitter fixed-bias amplifier as depicted in Fig. 3.23. The input resistance, output resistance, voltage gain and current gain can be derived as shown below:

The input resistance is

$$R_i = R_B \| h_{ie} = \frac{R_B h_{ie}}{R_B + h_{ie}}$$

When $R_B >> h_{ie}$, input resistance

$$R_i = \frac{R_B h_{ie}}{R_B\left(1 + \dfrac{h_{ie}}{R_B}\right)} \approx h_{ie} \quad \text{as} \quad \frac{h_{ie}}{R_B} \to 0 \qquad (3.18)$$

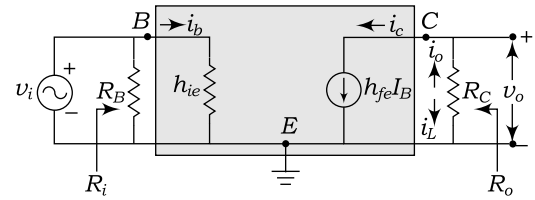


Fig. 3.23 ac equivalent circuit of Fig. 3.21 using approximate h-parameter model of transistor

The output resistance is determined when input voltage is equal to zero ($v_i = 0$). Since $v_i = 0$, current $i_b = 0$ and $h_{fe} i_b = 0$. Then the current behaves as open circuit. The output resistance is $R_o = R_C$.

The voltage is the ratio of output voltage v_o to the input voltage and it can be expressed as

$$A_v = \frac{v_o}{v_i}$$

The input voltage is equal to $v_i = h_{fe} i_b$ and the output voltage is $v_o = i_L R_C = -i_o R_C$

Since $i_o = h_{fe} i_b$, output voltage is $v_o = -i_o R_C = -h_{fe} i_b R_C$

Then voltage gain is

$$A_v = \frac{v_o}{v_i} = \frac{-h_{fe} i_b R_C}{h_{ie} i_b} = -\frac{h_{fe} R_C}{h_{ie}} \qquad (3.19)$$

Since h_{fe} and h_{ie} are positive, the voltage gain A_v is negative. The negative sign represents that output has 180° phase shift from input voltage.

Current gain is the ratio of load current to the input current (base current) and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-i_c}{i_b} = \frac{-h_{fe} i_b}{i_b} = -h_{fe} \qquad (3.20)$$

(ii) Analysis in Hybrid-π Equivalent Circuit Model After substituting the hybrid-π equivalent circuit model of a BJT, we get the circuit as shown in Fig. 3.24.

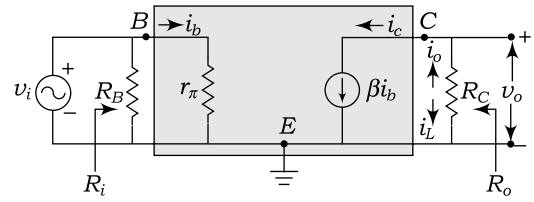


Fig. 3.24 The ac equivalent circuit of Fig. 3.21 using approximate hybrid-π model of transistor

The input resistance is

$$R_i = R_B \| r_\pi = \frac{R_B r_\pi}{R_B + r_\pi} \tag{3.21}$$

When input voltage is equal to zero ($v_i = 0$), the output resistance is determined and its value is

$R_o = R_C$

The input voltage is equal to $v_i = r_\pi i_b$ and the output voltage is $v_o = i_L R_C = -i_o R_C$

As $i_o = \beta i_b$, output voltage is $v_o = -i_o R_C = -\beta i_b R_C$

The voltage gain is

$$A_v = \frac{v_o}{v_i} = \frac{-\beta i_b R_C}{r_\pi i_b} = -\frac{\beta R_C}{r_\pi} \tag{3.22}$$

Current gain is the ratio of load current to the input current (base current) and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-i_c}{i_b} = \frac{-\beta i_b}{i_b} = -\beta \tag{3.23}$$

(iii) Analysis in r_e Model After substituting the r_e model of BJT in Fig. 3.21, we get the circuit as shown in Fig. 3.25.

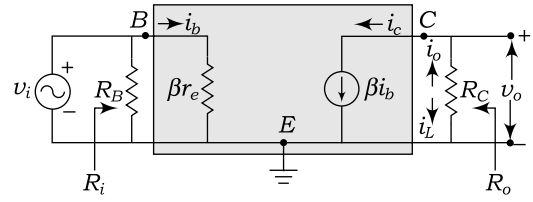


Fig. 3.25 ac equivalent circuit of Fig. 3.21 using r_e model of transistor

The input resistance is $R_i = R_B \| \beta r_e = \dfrac{R_B \beta r_e}{R_B + \beta r_e}$

When $R_B >> \beta r_e$, input resistance is

$$R_i = \frac{R_B \beta r_e}{R_B\left(1 + \dfrac{\beta r_e}{R_B}\right)} \approx \beta r_e \quad \text{as} \quad \frac{\beta r_e}{R_B} \to 0 \tag{3.24}$$

The output resistance is determined with input voltage equal to zero ($v_i = 0$), and its value is

$R_o = R_C$.

The input voltage is equal to $v_i = \beta r_e i_b$ and the output voltage is $v_o = i_L R_C = -i_o R_C$

As $i_o = \beta i_b$, output voltage is $v_o = -i_o R_C = -\beta i_b R_C$

The voltage gain is

$$A_v = \frac{v_o}{v_i} = \frac{-\beta i_b R_C}{\beta r_e i_b} = -\frac{R_C}{r_e} \tag{3.25}$$

Current gain is the ratio of load current to the input current (base current) and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-i_c}{i_b} = \frac{-\beta i_b}{i_b} = -\beta \tag{3.26}$$

3.6.3 The ac Load

A common-emitter amplifier with an external load resistance R_L is shown in Fig. 3.26(a). In this case, the effective load of the transistor is not equal to the resistance R_C and its value will be the parallel combination of R_L and R_C. The equivalent circuit of Fig. 3.26(a) is depicted in Fig. 3.26(b). It is clear from Fig. 3.26(b) that a capacitor C is collected across the dc supply V_{CC}. Due to presence of internal capacitor in dc power supply, the dc power source provides a very small resistance to the ac signal. Therefore, ac current flows through resistance R_C and capacitor. Hence, there is very small voltage drop within the dc power supply. Consequently, the complete voltage is dropped across the resistance R_C, which is connected to ground in ac signal. For an ac signal, the coupling capacitor acts as short circuit. Therefore, the resistances R_C and R_L may be connected in parallel as depicted in Fig. 3.26(c). Then the effective ac load resistance is

$$r_L = R_C \| R_L = \frac{R_C R_L}{R_C + R_L} \tag{3.27}$$

If $R_L >> R_C$, the effective ac load resistance is $r_L = R_C$

Example 3.3 Figure 3.27 shows a common-emitter amplifier. Determine (a) the input resistance looking from base, (b) output resistance, and (c) voltage gain. Assume $\beta = 100$.

Sol. Given: $V_{CC} = 12$ V, $R_C = 15$ kΩ , $R_B = 1000$ kΩ and $\beta = 100$

(a) The base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{1000 \times 10^3} = 11.3 \times 10^{-6} \text{ A}$$

The collector current $I_C = \beta I_B = 100 \times 11.3 \times 10^{-6}$ mA

Assume the emitter current is equal to collector current ($I_E = I_C$). Therefore, $I_E = 1.13$ mA.

The ac resistance of emitter diode,

$$r_e' = \frac{25 \text{ mV}}{I_E} = \frac{25}{1.13} = 22.123\ \Omega$$

The input resistance looking from base is

$$R_i = \beta r_e' = 100 \times 22.123\ \Omega = 2212.3\ \Omega$$

(b) The output resistance is $R_o = R_C = 15$ kΩ

(c) The voltage gain is

$$A_v = \frac{R_C}{r_e'} = \frac{15 \times 10^3}{22.123} = 678.02$$

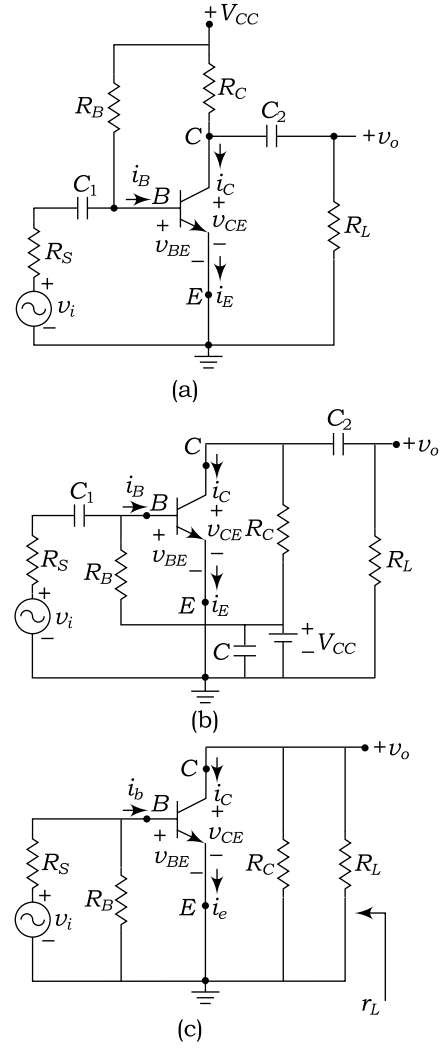


Fig. 3.26 **(a) Common-emitter amplifier (b) Equivalent circuit of Fig. 3.26(a) and (c) ac equivalent circuit of Fig. 3.26(a)**

(d) The power gain is $A_p = A_v A_i = 678.02 \times 100 = 67802$ and The power gain in decibel is

$$G_p = 10 \log_{10} A_p = 10 \log_{10} 67802 = 48.312 \text{ dB}$$

Example 3.4 A common-emitter amplifier has voltage gain of 500 and input resistance is 2 kΩ. When the ac input voltage is 10 mV, compute (a) the base current, (b) collector current, (c) current gain, and (d) power gain. Assume $\beta = 55$.

Sol. Given: $A_v = 500$, $R_i = 2$ kΩ, $v_i = 10$ mV and $\beta = 55$

(a) The input resistance is $R_i = \dfrac{v_i}{i_b}$ where ac input voltage is $v_i = 10$ mV and ac base current is i_b

Therefore, $2 \times 10^3 = \dfrac{10 \times 10^{-3}}{i_b}$ or $i_b = \dfrac{10 \times 10^{-3}}{2 \times 10^3}$

$= 5 \times 10^{-6}$ A $= 5$ μA

(b) The collector current $i_c = \beta i_b = 55 \times 5 \times 10^{-6} = 275$ μA

(c) The current gain is $A_i = \beta = 55$

(d) The power gain is $A_p = A_v A_i = 500 \times 55 = 27500$

The power gain in decibel is

$$G_p = 10 \log_{10} A_p = 10 \log_{10} 27500 = 44.393 \text{ dB}$$

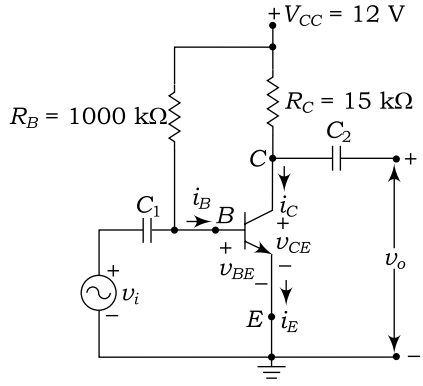


Fig. 3.27

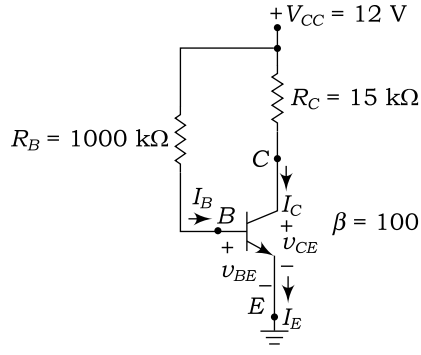


Fig. 3.28 dc equivalent circuit of Fig. 3.27

3.6.4 Analysis of Common-Emitter Amplifier with Emitter Feedback Resistor

A common-emitter amplifier circuit with emitter feedback resistance is shown in Fig. 3.29. The dc and ac analyses of Fig. 3.29 are explained below:

1. dc Analysis

The dc equivalent circuit of common-emitter amplifier circuit with emitter feedback resistance is depicted in Fig. 3.30(a), which is obtained by disconnecting the capacitors from the circuit. This circuit behaves as good biasing circuit.

The KVL equation in base-emitter circuit is

$$V_{CC} = I_B R_B + V_{BE} + I_B R_E$$

The base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E} \quad \text{as } \beta >> 1 \tag{3.28}$$

The collector current is

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B + \beta R_E} = \frac{V_{CC} - V_{BE}}{\dfrac{R_B}{\beta} + R_E} = \frac{V_{CC}}{\dfrac{R_B}{\beta} + R_E} \quad \text{as } V_{CC} >> V_{BE} \tag{3.29}$$

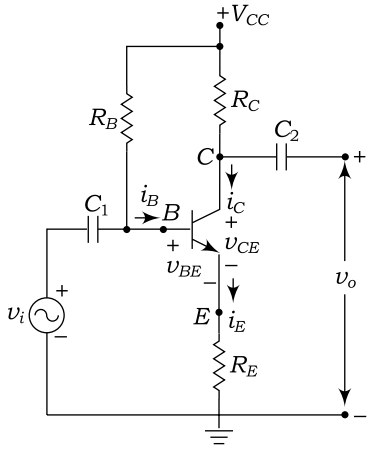


Fig. 3.29 Common-emitter amplifier circuit with emitter feedback

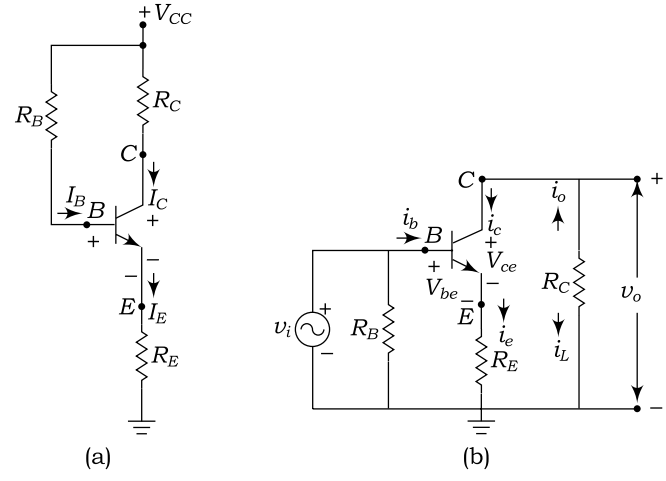


Fig. 3.30 (a) dc equivalent circuit of Fig. 3.29 (b) ac equivalent circuit of Fig. 3.29

2. ac Analysis

Figure 3.30(b) shows the ac equivalent circuit of Fig. 3.29. This circuit can be analysed by using (i) hybrid-(h) model, (ii) hybrid-π equivalent circuit model, and (iii) r_e model of bipolar junction transistor.

(i) Analysis in *h*-parameter Model After substituting the approximate h-parameter model of transistor, we get the ac equivalent circuit of common-emitter with emitter feedback amplifier as depicted in Fig. 3.31. The input resistance, output resistance, voltage gain and current gain can be derived as given below:

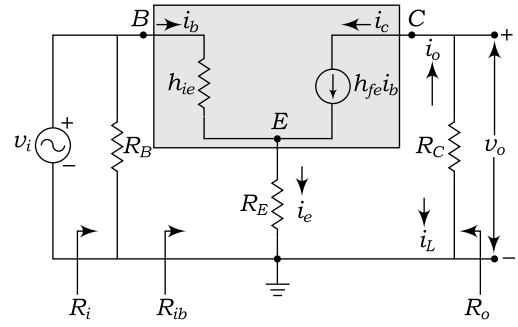


Fig. 3.31 ac equivalent circuit of Fig. 3.29 using approximate h-parameter model of transistor

The current flow through resistance R_E is

$$i_e = i_b + h_{fe}i_b = (1 + h_{fe})i_b$$

The input voltage v_i is equal to

$$v_i = i_b h_{ie} + i_e R_E = i_b h_{ie} + (1 + h_{fe})i_b R_E = i_b[h_{ie} + (1 + h_{fe})R_E]$$

Directly looking from base, the input resistance is

$$R_{ib} = \frac{v_i}{i_b} = \frac{i_b[h_{ie} + (1 + h_{fe})R_E]}{i_b}$$

$$= h_{ie} + (1 + h_{fe})R_E = h_{ie} + h_{fe}R_E \quad \text{as } h_{fe} >> 1$$

$$= h_{fe}R_E \quad \text{as } h_{fe}R_E >> h_{ie}$$

Then input resistance is $$R_i = R_{ib} \| R_B = \frac{R_{ib}R_B}{R_{ib} + R_B} = \frac{h_{fe}R_E R_B}{h_{fe}R_E + R_B} \tag{3.30}$$

The output resistance is determined when input voltage is equal to zero ($v_i = 0$). Since $v_i = 0$, current $i_b = 0$ and $h_{fe}i_b = 0$. Then the current behaves as open circuit. The output resistance is

$$R_o = R_C.$$

The voltage is the ratio of output voltage v_o to the input voltage v_i and it can be expressed as

$$A_v = \frac{v_o}{v_i}$$

The input voltage is equal to $v_i = R_{ib} i_b = h_{fe} R_E i_b$

The output voltage is $v_o = i_L R_C = -i_o R_C = -h_{fe} i_b R_C$ as $i_o = h_{fe} i_b$

Then voltage gain is

$$A_v = \frac{v_o}{v_i} = \frac{-h_{fe} i_b R_C}{h_{fe} R_E i_b} = -\frac{R_C}{R_E} \tag{3.31}$$

Since R_C and R_E are positive, the voltage gain A_v is negative. The negative sign represents that output has 180° phase shift from input voltage.

Current gain is the ratio of load current to the input current (base current) and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-h_{fe} i_b}{i_i} \quad \text{where } i_b = i_i \frac{R_B}{R_B + R_{ib}}$$

Then

$$A_i = \frac{-h_{fe} i_b}{i_i} = \frac{-h_{fe} i_i \dfrac{R_B}{R_B + R_{ib}}}{i_i} = -\frac{h_{fe} R_B}{R_B + R_{ib}} = -\frac{h_{fe} R_B}{R_B + h_{fe} R_E} \tag{3.32}$$

(ii) Analysis in Hybrid-π Equivalent Circuit Model After substituting the hybrid-π equivalent circuit model of BJT, we get circuit as shown in Fig. 3.32.

The current flow through resistance R_E is

$$i_e = i_b + \beta i_b = (1 + \beta) i_b \tag{3.33}$$

The input voltage v_i is equal to

$$\begin{aligned} v_i &= i_b r_\pi + i_e R_E = i_b r_\pi + (1 + \beta) i_b R_E \\ &= i_b [r_\pi + (1 + \beta) R_E] \end{aligned} \tag{3.34}$$

Directly looking from base, the input resistance is

$$\begin{aligned} R_{ib} &= \frac{v_i}{i_b} = \frac{i_b [r_\pi + (1 + \beta) R_E]}{i_b} \\ &= r_\pi + (1 + \beta) R_E \end{aligned} \tag{3.35}$$

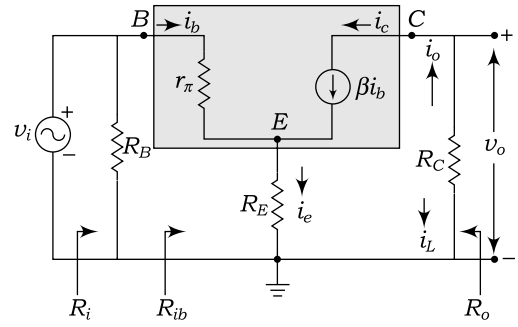


Fig. 3.32 ac equivalent circuit of Fig. 3.29 using approximate hybrid-π model of transistor

Then input resistance is equal to

$$R_i = R_{ib} \| R_B = \frac{R_{ib} R_B}{R_{ib} + R_B} = \frac{[r_\pi + (1 + \beta) R_E] R_B}{r_\pi + (1 + \beta) R_E + R_B} \tag{3.36}$$

The output resistance is determined when input voltage is equal to zero ($v_i = 0$). Since $v_i = 0$, current $i_b = 0$ and $h_{fe} i_b = 0$. Then the current behaves as open circuit. The output resistance is

$$R_o = R_C.$$

The voltage is the ratio of output voltage v_o to the input voltage and it is equal to $A_v = \dfrac{v_o}{v_i}$

The input voltage is equal to $v_i = R_{ib} i_b$

The output voltage is

$$v_o = i_L R_C = -i_o R_C = -\beta i_b R_C \quad \text{as } i_o = \beta i_b \tag{3.37}$$

Then voltage gain is

$$A_v = \frac{v_o}{v_i} = \frac{-\beta i_b R_C}{R_{ib} i_b} = -\frac{\beta R_C}{R_{ib}} \tag{3.38}$$

Current gain is the ratio of load current to the input current (base current) and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-\beta i_b}{i_i} \quad \text{where, } i_b = i_i \frac{R_B}{R_B + R_{ib}}$$

Then

$$A_i = \frac{-\beta i_b}{i_i} = \frac{-\beta i_i \dfrac{R_B}{R_B + R_{ib}}}{i_i} = -\frac{\beta R_B}{R_B + R_{ib}} = -\frac{\beta R_B}{R_B + r_\pi + (1+\beta) R_E} \tag{3.39}$$

(iii) Analysis in r_e Model After substituting the r_e model of BJT, we obtain the circuit as shown in Fig. 3.33.

The current flow through resistance R_E is

$$i_e = i_b + \beta i_b = (1+\beta) i_b \tag{3.40}$$

The input voltage v_i is equal to

$$\begin{aligned} v_i &= i_b \beta r_e + i_e R_E = i_b \beta r_e + (1+\beta) i_b R_E \\ &= i_b [\beta r_e + (1+\beta) R_E] \end{aligned} \tag{3.41}$$

Directly looking from base, the input resistance is

$$\begin{aligned} R_{ib} &= \frac{v_i}{i_b} = \frac{i_b [\beta r_e + (1+\beta) R_E]}{i_b} \\ &= \beta r_e + (1+\beta) R_E \end{aligned}$$

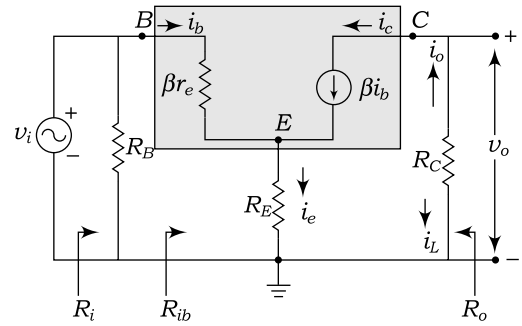


Fig. 3.33 ac equivalent circuit of Fig. 3.31 using r_e model of transistor

Then input resistance is

$$R_i = R_{ib} \| R_B = \frac{R_{ib} R_B}{R_{ib} + R_B} = \frac{[\beta r_e + (1+\beta) R_E] R_B}{\beta r_e + (1+\beta) R_E + R_B} \tag{3.42}$$

The output resistance is determined when input voltage is equal to zero ($v_i = 0$). Since $v_i = 0$, current $i_b = 0$ and $\beta i_b = 0$. Then the current behaves as open circuit. The output resistance is

$$R_o = R_C.$$

The voltage is the ratio of output voltage v_o to the input voltage v_i and it is equal to $A_v = \dfrac{v_o}{v_i}$.

The input voltage is equal to $v_i = R_{ib} i_b$

The output voltage is

$$v_o = i_L R_C = -i_o R_C = -\beta i_b R_C \quad \text{as } i_o = \beta i_b \tag{3.43}$$

Then voltage gain is

$$A_v = \frac{v_o}{v_i} = \frac{-\beta i_b R_C}{R_{ib} i_b} = -\frac{\beta R_C}{R_{ib}} = -\frac{\beta R_C}{\beta r_e + (1+\beta) R_E} \tag{3.44}$$

Current gain is the ratio of load current to the input current (base current) and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-\beta i_b}{i_i} \quad \text{where, } i_b = i_i \frac{R_B}{R_B + R_{ib}}$$

Then

$$A_i = \frac{-\beta i_b}{i_i} = \frac{-\beta i_i \dfrac{R_B}{R_B + R_{ib}}}{i_i} = -\frac{\beta R_B}{R_B + R_{ib}} = -\frac{\beta R_B}{R_B + \beta r_e + (1+\beta) R_E} \tag{3.45}$$

Example 3.5 Figure 3.34 shows a common-emitter amplifier with emitter feedback resistance R_E. Determine (a) the input resistance looking from base, (b) output resistance, and (c) voltage gain. Assume $\beta = 100$.

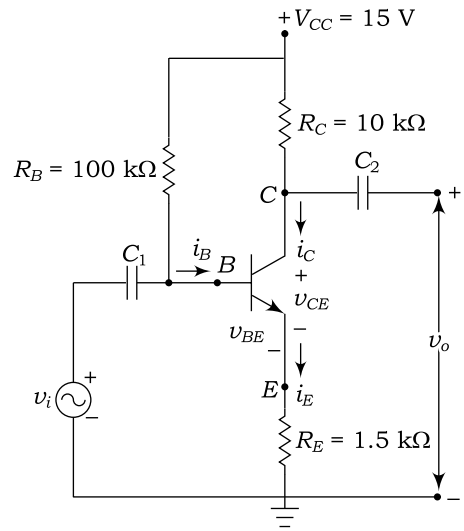


Fig. 3.34

Sol. Given: $V_{CC} = 15$ V, $R_C = 10$ kΩ, $R_B = 100$ kΩ, $R_E = 1.5$ kΩ and $\beta = 100$

(a) The collector current

$$I_C = \frac{V_{CC}}{R_E + \dfrac{R_B}{\beta}} = \frac{15}{1.5\times10^3 + \dfrac{100\times10^3}{100}}$$

$$= 6\times10^{-3}\text{ A} = 6\text{ mA}$$

Assume the emitter current is equal to collector current ($I_E = I_C$).

Therefore, $I_E = 6$ mA.

The ac resistance of emitter diode,

$$r_e' = \frac{25\text{ mV}}{I_E} = \frac{25}{6} = 4.166\ \Omega$$

The input resistance looking from base is

$$R_i = \beta(r_e' + R_E) = 100\times(4.166 + 1.5\times10^3)\Omega$$

$$= 150.416\text{ kΩ}$$

(b) The output resistance is $R_o = R_C = 10$ kΩ

(c) The voltage gain is

$$A_v = \frac{R_C}{r_e' + R_E} = \frac{10\times10^3}{4.166 + 1.5\times10^3} = 6.648$$

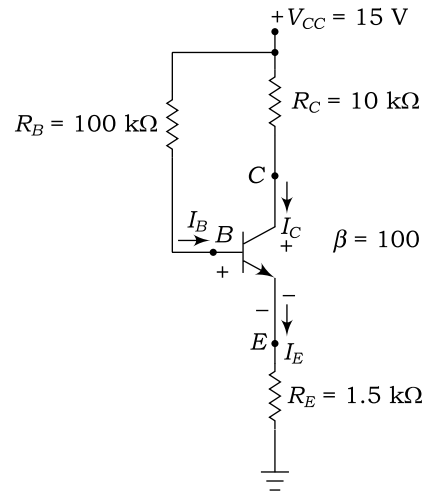


Fig. 3.35 dc equivalent circuit of Fig. 3.34

3.6.5 Effect of Bypass Capacitor on Common-Emitter Amplifier with Emitter Feedback Resistor

A common-emitter amplifier circuit with capacitor is connected across emitter feedback resistance R_E is shown in Fig. 3.35. Due to the presence of bypass capacitor, the emitter terminal is connected to ground for ac current. The bypass capacitor acts as an open circuit for dc current. The dc and ac analyses of Fig. 3.36 are explained as follows:

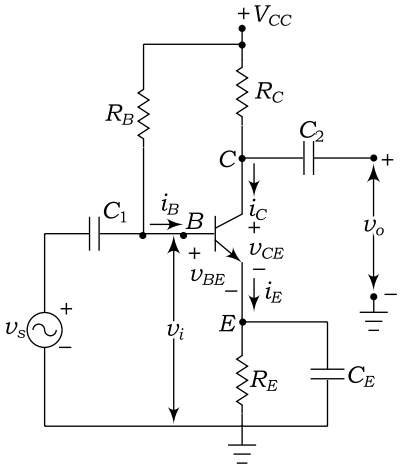


Fig. 3.36 Common emitter amplifier circuit with C_E connected across R_E

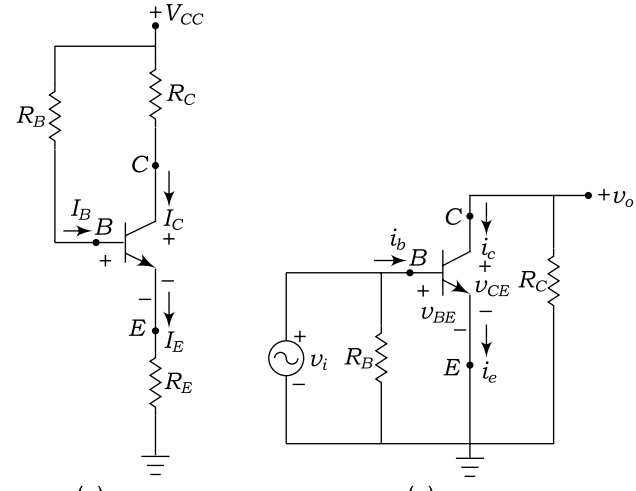


Fig. 3.37 (a) dc equivalent circuit of Fig. 3.36 (b) ac equivalent circuit of Fig. 3.36

1. dc Analysis

The dc equivalent circuit of Fig. 3.36 is depicted in Fig. 3.37(a) which is obtained by disconnecting the capacitors from the circuit. This circuit behaves as good biasing circuit.

The KVL equation in base-emitter circuit is $V_{CC} = I_B R_B + V_{BE} + I_B R_E$

The base current is $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E} \quad \text{as } \beta >> 1 \tag{3.46}$$

The collector current is $$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B + \beta R_E} = \frac{V_{CC} - V_{BE}}{\frac{R_B}{\beta} + R_E} = \frac{V_{CC}}{\frac{R_B}{\beta} + R_E} \text{ as } V_{CC} >> V_{BE} \tag{3.47}$$

2. ac Analysis

Figure 3.38(b) shows the ac equivalent circuit of Fig. 3.36. This circuit can be analysis by using r_e model of bipolar junction transistor.

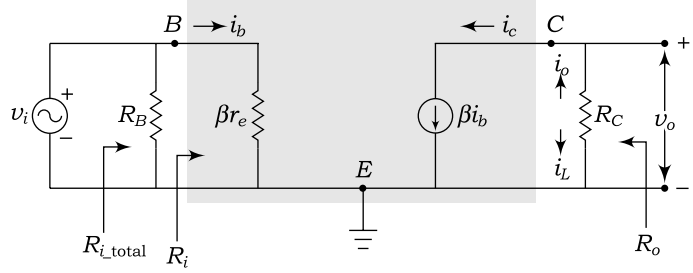


Fig. 3.38 r_e model of Fig. 3.36

Looking from the base, the internal resistance is $R_i = \beta r_e$ and the total input resistance is

$$R_i\_\text{total} = R_i \parallel \beta r_e \tag{3.48}$$

Hence, the presence of emitter bypass capacitor can reduce the input resistance of a common-emitter amplifier.

The input voltage v_i is equal to $v_i = i_b \beta r_e$ (3.49)

The output voltage is $v_o = i_c R_C = \beta i_b R_C$ as $i_c = \beta i_b$ (3.50)

Then voltage gain is $$A_v = \frac{v_o}{v_i} = \frac{\beta i_b R_C}{i_b \beta r_e} = \frac{R_C}{r_e} \quad (3.51)$$

Example 3.6 Figure 3.39 shows a common-emitter amplifier. Calculate (a) the input resistance looking from base, (b) output resistance, (c) voltage gain, and (d) voltage gain when bypass capacitor is connected across R_E.

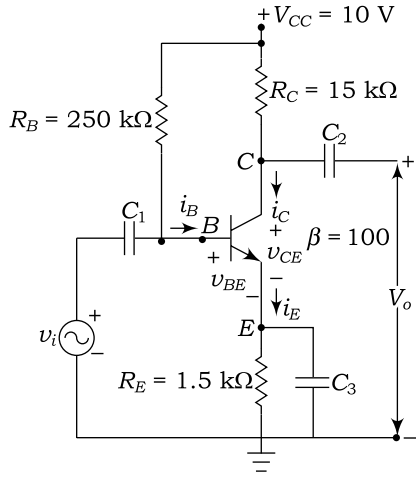


Fig. 3.39

Sol. Given: $V_{CC} = 10$ V, $R_C = 15$ kΩ , $R_B = 250$ kΩ, $R_E = 1.5$ kΩ and $\beta = 100$

(a) The collector current

$$I_C = \frac{V_{CC}}{R_E + \frac{R_B}{\beta}} = \frac{10}{1.5 \times 10^3 + \frac{250 \times 10^3}{100}}$$

$$= 2.5 \times 10^{-3} \text{ A} = 2.5 \text{ mA}$$

Assume the emitter current is equal to collector current ($I_E = I_C$).

Therefore, $I_E = 2.5$ mA.

The ac resistance of emitter diode,

$$r'_e = \frac{25 \text{ mV}}{I_E} = \frac{25}{2.5} = 10 \ \Omega$$

The input resistance looking from base is

$$R_i = \beta r'_e = 100 \times 10 \ \Omega = 1000 \ \Omega$$

The total input resistance is

$$R_{i-\text{total}} = R_i \| R_B = 1k \| 250k = 0.9960 \text{ kΩ}$$

(b) Output resistance is $R_o = R_C = 15$ kΩ

(c) Voltage gain $A_v = \frac{R_C}{r'_e} = \frac{15 \times 10^3}{10} = 1500$

(d) When the by pass capacitor is removed, the voltage gain is

$$A_v = \frac{R_C}{r'_e + R_E} = \frac{15 \times 10^3}{10 + 1.5 \times 10^3} = 9.933$$

3.6.6 Effect of ac Load on Common-Emitter Amplifier with Voltage-Divider Bias

A common-emitter amplifier circuit with voltage-divider bias is shown in Fig. 3.40. The dc and ac analyses of Fig. 3.40 are explained below:

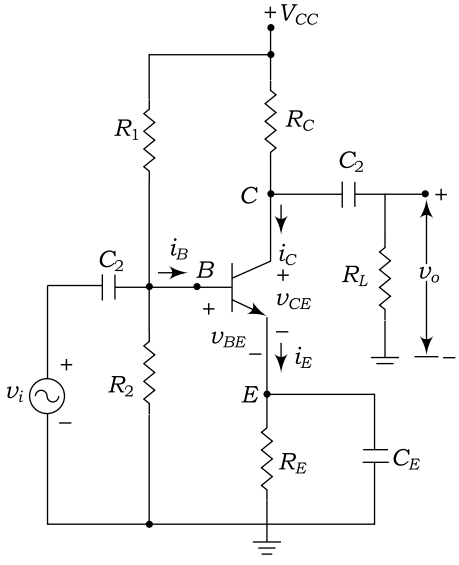


Fig. 3.40

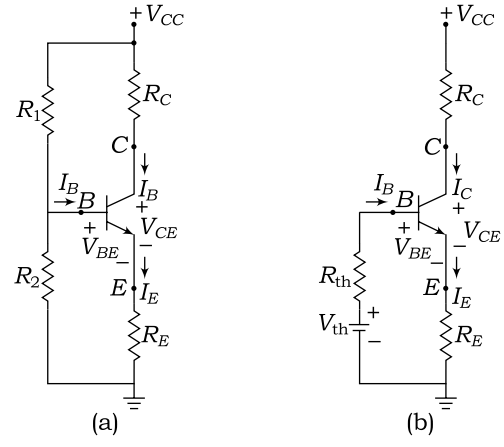


Fig. 3.41 (a) dc equivalent circuit
(b) Thevenin's equivalent circuit

1. dc Analysis

The dc equivalent circuit of common-emitter amplifier circuit with voltage-divider bias is depicted in Fig. 3.41, which is obtained by disconnecting the capacitors from the circuit. This circuit behaves as good biasing circuit.

The KVL equation in base-emitter circuit is

$$V_{\text{th}} = I_B R_{\text{th}} + V_{BE} + I_B R_E \quad \text{where, } V_{\text{th}} = V_{CC}\frac{R_2}{R_1 + R_2} \text{ and } R_{\text{th}} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

The base current is

$$I_B = \frac{V_{\text{th}} - V_{BE}}{R_{\text{th}} + (\beta + 1)R_E} = \frac{V_{\text{th}} - V_{BE}}{R_B + \beta R_E} \quad \text{as } \beta >> 1 \tag{3.52}$$

The collector current is

$$I_C = \beta I_B = \beta\frac{V_{\text{th}} - V_{BE}}{R_B + \beta R_E} = \frac{V_{\text{th}} - V_{BE}}{\frac{R_B}{\beta} + R_E} \tag{3.53}$$

2. ac Analysis

Figure 3.42 shows the ac equivalent circuit of Fig. 3.40. This circuit can be analysed by using (i) hybrid-(h) model, (ii) hybrid-π equivalent circuit model, and (iii) r_e model of bipolar junction transistor.

(i) Analysis in *h*-parameter Model After substituting the approximate h-parameter model of the transistor, we get the ac equivalent circuit of common-emitter with emitter feedback amplifier as shown in Fig. 3.43. The input resistance, output resistance, voltage gain and current gain can be derived as follows:

The input resistance is

$$R_i = R_1 \| R_2 \| h_{ie} = R_{\text{th}} \| h_{ie} = \frac{R_{\text{th}} h_{ie}}{R_{\text{th}} + h_{ie}} \tag{3.54}$$

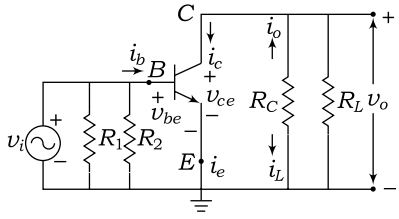


Fig. 3.42 ac equivalent circuit of Fig. 3.40

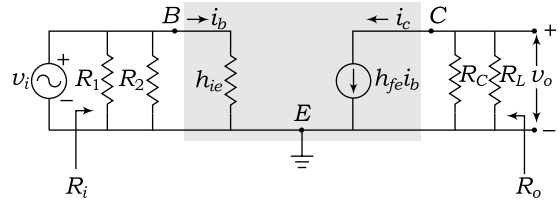


Fig. 3.43 ac equivalent circuit of Fig. 3.42 using approximate *h*-parameter model of transistor

The output resistance is determined when input voltage is equal to zero ($v_i = 0$). Since $v_i = 0$, current $i_b = 0$ and $h_{fe}i_b = 0$. Then the current behaves as open circuit. The output resistance is $R_o = R_C \parallel R_L$. The ac load resistance r_L is the parallel combination of R_C and R_L, i.e. $r_L = R_C \parallel R_L$.

The voltage gain is the ratio of output voltage v_o to the input voltage v_i. The input voltage is equal to $v_i = h_{ie}i_b$ and the output voltage is $v_o = -i_e r_L$.

Since $i_c = h_{fe}i_b$, output voltage is $$v_o = -i_c r_L = -h_{fe}i_b r_L \tag{3.55}$$

Then voltage gain is $$A_v = \frac{v_o}{v_i} = \frac{-h_{fe}i_b r_L}{h_{ie}i_b} = -\frac{h_{fe}r_L}{h_{ie}} \tag{3.56}$$

As h_{fe} and h_{ie} are positive, the voltage gain A_v is negative. The negative sign represents that output has 180° phase shift from input voltage.

Current gain is the ratio of load current to the input current (base current) and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-i_c}{i_i} = \frac{-h_{fe}i_b}{i_i} \quad \text{where, } i_b = i_i \frac{R_{th}}{R_{th} + h_{ie}}$$

Then current gain is $$A_i = \frac{-h_{fe}i_b}{i_i} = -\frac{h_{fe}i_i \dfrac{R_{th}}{R_{th} + h_{ie}}}{i_i} = -h_{fe}\frac{R_{th}}{R_{th} + h_{ie}} \tag{3.57}$$

(ii) Analysis in Hybrid-π Equivalent Circuit Model After substituting the hybrid-π model of BJT, we obtain the circuit as shown in Fig. 3.44.

The input resistance is

$$R_i = R_1 \parallel R_2 \parallel r_\pi = R_{th} \parallel r_\pi = \frac{R_{th}r_\pi}{R_{th} + r_\pi} \tag{3.58}$$

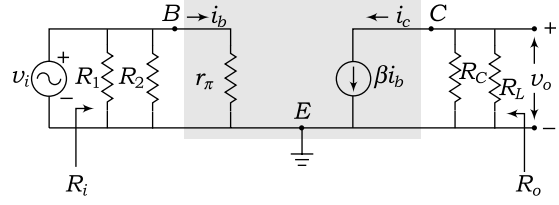


Fig. 3.44 ac equivalent circuit of Fig. 3.42 using hybrid-π model of transistor

With input voltage equal to zero ($v_i = 0$), the output resistance is determined. As $v_i = 0$, current $i_b = 0$ and $h_{fe}i_b = 0$. The current source behaves as open circuit. The output resistance is r_L. The ac load resistance r_L is the parallel combination of R_C and R_L, i.e., $r_L = R_C \parallel R_L$.

The input voltage is equal to $v_i = r_\pi i_b$ and the output voltage is $v_o = -i_c r_L$

As $i_c = \beta i_b$, output voltage is

$$v_o = -i_c r_L = -\beta i_b r_L \tag{3.59}$$

The voltage gain is $$A_v = \frac{v_o}{v_i} = \frac{-\beta i_b r_L}{r_\pi i_b} = -\frac{\beta r_L}{r_\pi} \quad (3.60)$$

The negative sign represents that output has 180° phase shift from input voltage.

Current gain is the ratio of load current to the input current (base current) and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-i_c}{i_i} = \frac{-\beta i_b}{i_i} \quad \text{where, } i_b = i_i \frac{R_{th}}{R_{th} + h_{ie}}$$

Then current gain is $$A_i = \frac{-\beta i_b}{i_i} = -\frac{\beta i_i \dfrac{R_{th}}{R_{th} + h_{ie}}}{i_i} = -\beta \frac{R_{th}}{R_{th} + h_{ie}} \quad (3.61)$$

(iii) Analysis in r_e Model After substituting the r_e model of BJT, we obtain the circuit as shown in Fig. 3.45.

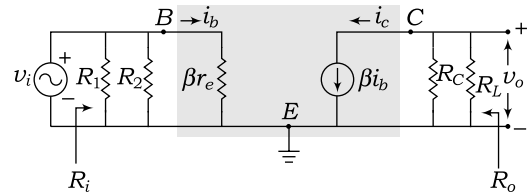


Fig. 3.45 ac equivalent circuit of Fig. 3.42 using r_e model of transistor

The input resistance is

$$R_i = R_1 \| R_2 \| \beta r_e = R_{th} \| \beta r_e = \frac{R_{th} \beta r_e}{R_{th} + \beta r_e}$$

When input voltage is equal to zero ($v_i = 0$), the output resistance is determined. Since $v_i = 0$, current $i_b = 0$ and $\beta i_b = 0$. Then the current source behaves as open circuit.

The output resistance is $R_o = R_C \| R_L$. The ac load resistance r_L is the parallel combination of R_C and R_L, i.e., $r_L = R_C \| R_L$.

The input voltage is $v_i = \beta r_e i_b$ and the output voltage is $v_o = -i_c r_L$

As $i_c = \beta i_b$, output voltage is $v_o = -i_c r_L = -\beta i_b r_L$ (3.62)

The voltage gain is $$A_v = \frac{v_o}{v_i} = \frac{-\beta i_b r_L}{\beta r_e i_b} = -\frac{r_L}{r_e} \quad (3.63)$$

The negative sign indicates that output voltage has 180° phase shift from input voltage.

Current gain is the ratio of load current to the input current and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-i_c}{i_i} = \frac{-\beta i_b}{i_i} \quad \text{where, } i_b = i_i \frac{R_{th}}{R_{th} + \beta r_e}$$

Then the current gain is

$$A_i = \frac{-\beta i_b}{i_i} = -\frac{\beta i_i \dfrac{R_{th}}{R_{th} + \beta r_e}}{i_i} = -\beta \frac{R_{th}}{R_{th} + \beta r_e} \quad (3.64)$$

Example 3.7 Figure 3.46 shows a common-emitter amplifier. Draw the ac equivalent circuit. Determine the input resistance, voltage gain and output voltage. Assume $\beta = 50$.

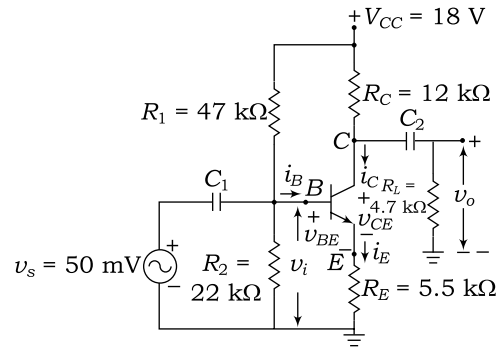


Fig. 3.46

Sol. Given: $V_{CC} = 18$ V, $R_C = 12$ kΩ, $R_1 = 47$ kΩ, $R_2 = 22$ kΩ, $R_E = 5.5$ kΩ, $R_L = 4.7$ kΩ, $v_s = 50$ mV and $\beta = 50$

The Thevenin's voltage is

$$V_{\text{th}} = V_{CC}\frac{R_2}{R_1+R_2} = 18\frac{22}{47+22}V = 5.739\text{ V}$$

The Thevenin's resistance is

$$R_{\text{th}} = R_1 \| R_2 = 47k \| 22k = \frac{47\times 22}{47+22}\text{ k}\Omega = 14.985\text{ k}\Omega$$

The emitter current $$I_E = \frac{V_{\text{th}} - V_{BE}}{R_E + \frac{R_{\text{th}}}{\beta}} = \frac{5.739-0.7}{5.5\times 10^3 + \frac{14.985\times 10^3}{50}} = 0.8688\times 10^{-3}\text{ A} = 0.8688\text{ mA}$$

The ac resistance of emitter diode, $r'_e = \frac{25\text{ mV}}{I_E} = \frac{25}{0.8688} = 28.775\ \Omega$

(a) The input resistance looking from base is

$$R_i = \beta r'_e = 50 \times 28.775\ \Omega = 1438.766\ \Omega = 1.438\text{ k}\Omega$$

The total input resistance is

$$R_t\_\text{total} = R_i \| R_{\text{th}} = 1.438k \| 14.985k = 1.311\text{ k}\Omega$$

(b) The ac load resistance is $r_L = R_C \| R_L = 12 \| 4.7\text{ k}\Omega = 3.377\text{ k}\Omega$

(c) Voltage gain $A_v = \frac{r_L}{r'_e + r_E} = \frac{3.377\times 10^3}{28.775} = 117.35$

The overall voltage gain is $A_v = \frac{v_o}{v_s}$ or $117.35 = \frac{v_o}{50}$

or $v_o = 50 \times 117.35\text{ mV} = 5867.5\text{ mV} = 5.8675\text{ V}$

3.6.7 Effect of Source Resistance on Common-Emitter Amplifier with Voltage Divider Bias

Figure 3.47 shows a common-emitter amplifier circuit with voltage-divider bias which is connected to a voltage source v_s with internal resistance R_S. This circuit is known as *swamped* amplifier. When $R_S = 0$, the input voltage is equal to voltage source ($v_i = v_s$). Actually, any ac source voltage has a nonzero internal resistance R_S. Then input voltage is always less than the voltage source ($v_i < v_s$).

The ac equivalent circuit of Fig. 3.47 is shown in Fig. 3.48. Looking from the signal source, the total input impedance of the amplifier is

$$R_i = R_1 \| R_2 \| \beta r_e.$$

The input voltage at the base of the transistor is equal to

$$v_i = \frac{R_i}{R_S + R_i} v_s$$

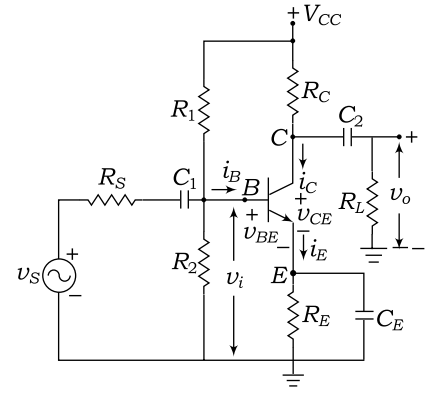


Fig. 3.47 Common-emitter amplifier circuit with source resistance and voltage divider bias

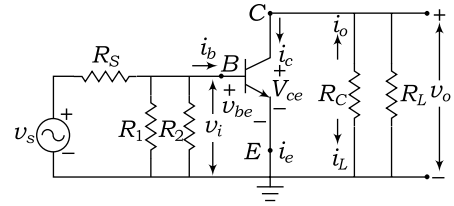


Fig. 3.48 ac equivalent circuit of Fig. 3.47

Then $$\frac{v_i}{v_s} = \frac{R_i}{R_S + R_i}$$

The input voltage is $v_i = \beta r_e i_b$ and the output voltage is $v_o = -i_c r_L$

$$\text{where, } r_L = R_C \| R_L = \frac{R_C R_L}{R_C + R_L}$$

As $i_c = \beta i_b$, output voltage is $v_o = -i_c r_L = -\beta i_b r_L$

The voltage gain is $$A_v = \frac{v_o}{v_i} = \frac{-\beta i_b r_L}{\beta r_e i_b} = -\frac{r_L}{r_e} \tag{3.65}$$

The overall voltage gain is $$A_{vs} = \frac{v_o}{v_s} = \frac{v_o}{v_i} \times \frac{v_i}{v_s} = A_v \times \frac{v_i}{v_s} = A_v \frac{R_i}{R_S + R_i} \tag{3.66}$$

It is clear from the above expression that the overall voltage gain A_{vs} is less than A_v.

In a common-emitter amplifier, voltage gains $A_v = \frac{v_o}{v_i} = -\frac{r_L}{r_e}$ where r_L is the ac load resistance and r_e is the ac resistance emitter diode. Then output voltage depends upon r_e. Since the ac resistance emitter diode depends upon the temperature, its value increases with increase in temperature. Then the output voltage and voltage gain decreases. The gain variation is acceptable only in radio receiver circuits, but other applications gain variation is not acceptable. The required stable voltage gain can be achieved by adding a resistance r_E in series with emitter as shown in Fig. 3.49. Due to resistance r_E, emitter is not at ac ground. As emitter current i_e flow through r_E, there will be a voltage at emitter terminal. If r_E is too much greater than r_e, approximately all ac input signal will be appear at the emitter and the emitter is said to be bootstrapped for ac as well as dc.

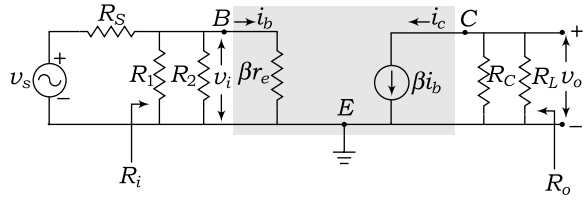


Fig. 3.49 ac equivalent circuit using r_e model of transistor

Figure 3.51 shows the ac equivalent circuit of Fig. 3.50. Looking from the base, the input resistance of amplifier is $R_{i\text{–base}} = (r_e + r_E)$ and total input resistance is equal to

$R_i = R_1 \| R_2 \| \beta(r_e + r_E)$.

It is clear from relationship $R_{i\_\text{base}} = (r_e + r_E)$ that the addition of resistance r_E increases the input resistance of the amplifier as compared to the input resistance of the unswamped amplifier.

The advantages of *swamped amplifier* are

1. it provides stable voltage gain
2. it provides high input resistance
3. it generates less distortion in the output signal

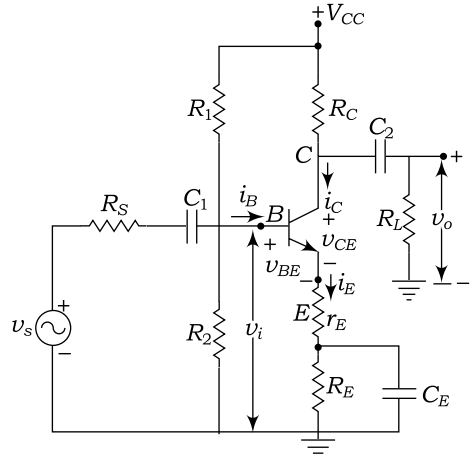


Fig. 3.50 Swamped common-emitter amplifier

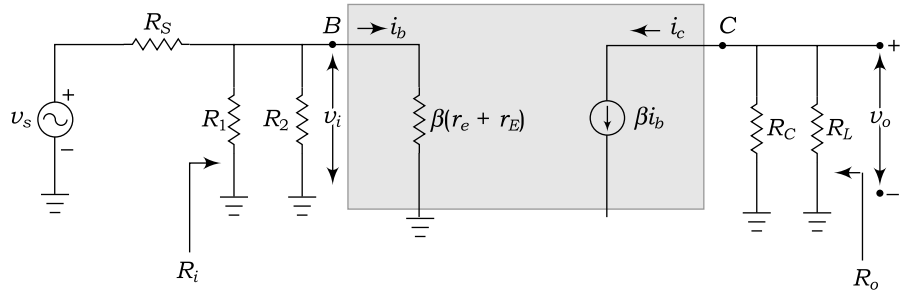


Fig. 3.51 ac equivalent circuit of Fig. 3.50 using r_e model

Example 3.8 Figure 3.52 shows a common-emitter amplifier. Draw the ac equivalent circuit. Determine the input resistance, ac load resistance, voltage gain and output voltage

Sol. Given: V_{CC} = 12 V, R_C = 10 kΩ, R_1 = 100 kΩ, R_2 = 50 kΩ, r_E = 1 kΩ, R_E = 2 kΩ, R_S = 100 Ω, v_s = 10 mV and $\beta = 60$

The Thevenin's voltage is

$$V_{th} = V_{CC}\frac{R_2}{R_1 + R_2} = 12\frac{50}{100 + 50}\text{V} = 4\text{V}$$

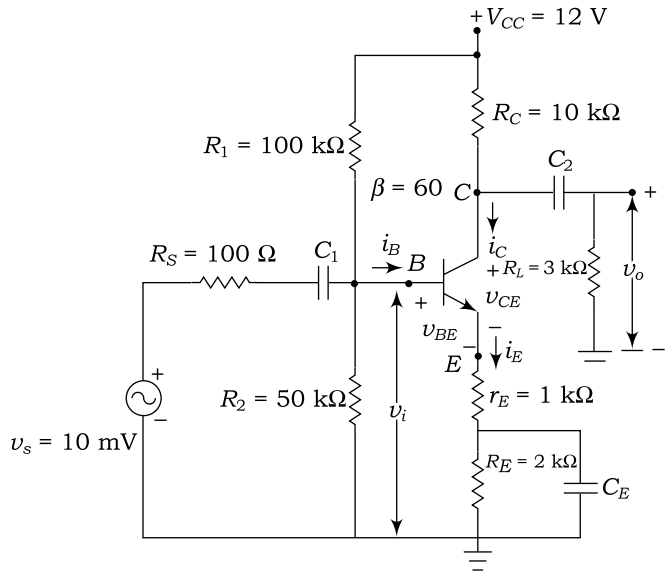


Fig. 3.52

The Thevenin's resistance is $R_{th} = R_1 \parallel R_2 = 100k \parallel 50k = \dfrac{100 \times 50}{150} = 33.333\ \text{k}\Omega$

The emitter resistance is $R_E' = R_E + r_E = 2k + 1k = 3\ \text{k}\Omega$

The emitter current $I_E = \dfrac{V_{th} - V_{BE}}{R'_E + \dfrac{R_{th}}{\beta}} = \dfrac{4 - 0.7}{3\times10^3 + \dfrac{33.333\times10^3}{60}} = 0.928\times10^{-3}\ \text{A} = 0.928\ \text{mA}$

The ac resistance of emitter diode, $r'_e = \dfrac{25\ \text{mV}}{I_E} = \dfrac{25}{0.928} = 26.939\ \Omega$

(a) The input resistance looking from base is

$$R_i = \beta(r'_e + r_E) = 60\times(26.939 + 1000)\ \Omega = 61.616\ \text{k}\Omega$$

The total input resistance is

$$R_{i\_\text{total}} = R_i \parallel R_{th} = 61.616k \parallel 33.333k = 21.631\ \text{k}\Omega$$

(b) The ac load resistance is $r_L = R_C \parallel R_L = 10 \parallel 3\ \text{k}\Omega = 2.30\ \text{k}\Omega$

(c) Voltage gain $A_v = \dfrac{r_L}{r'_e + r_E} = \dfrac{2.3\times10^3}{26.939 + 1000} = 2.239$

Overall voltage gain is $\dfrac{v_i}{v_s} = \dfrac{R_{i\_\text{total}}}{R_s + R_{i\_\text{total}}} = \dfrac{21.631k}{100 + 21.631k} = 0.995$

(d) The overall voltage gain is $A_{v\_\text{total}} = A_v \times \dfrac{v_i}{v_s} = 2.239\times0.995 = 2.227$

The output voltage is $v_o = A_{v\_\text{total}} \times v_s = 2.227\times10\ \text{mV} = 22.22\ \text{mV}$

Example 3.9 Figure 3.53 shows transistor amplifier. Determine the input resistance R_i and V_{CE}.

Sol. Given: $V_{CC} = 15$ V, $R_C = 35\ \text{k}\Omega$, $R_1 = 47\ \text{k}\Omega$, $R_2 = 22\ \text{k}\Omega$, $R_E = 2\ \text{k}\Omega$, $R_C = 35$ k, $R_L = 4.7\ \text{k}\Omega$, and $\beta = 120$

The Thevenin's voltage is

$$V_{th} = V_{CC}\frac{R_2}{R_1 + R_2} = -15\frac{22}{47 + 22}V = -4.782\ \text{V}$$

The Thevenin's resistance is

$$R_{th} = R_1 \parallel R_2 = 47k \parallel 22k = \frac{47\times22}{47 + 22} = 14.985\ \text{k}\Omega$$

The emitter current

$$I_E = \frac{V_{th} - V_{BE}}{R_E + \dfrac{R_{th}}{\beta}} = \frac{-4.782 - 0.7}{2\times10^3 + \dfrac{14.985\times10^3}{120}}$$

$$= 2.579\times10^{-3}\ \text{A} = 2.579\ \text{mA}$$

The ac resistance of emitter diode,

$$r'_e = \frac{25\ \text{mV}}{I_E} = \frac{25}{2.579} = 9.693\ \Omega$$

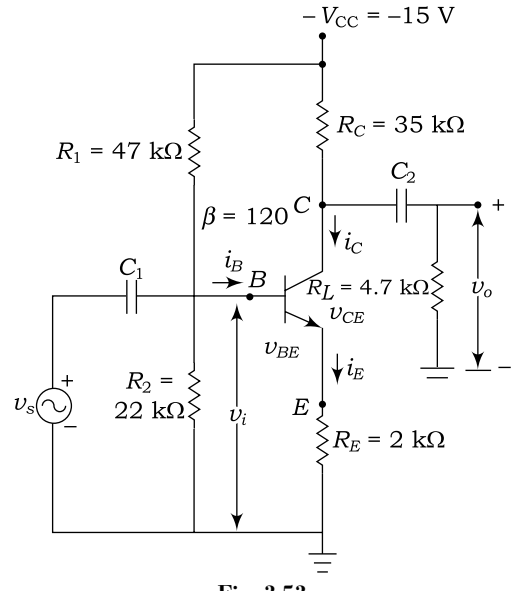


Fig. 3.53

(a) The input resistance looking from base is

$$R_i = \beta r_e' = 120 \times 9.693\ \Omega$$
$$= 1163.24\ \Omega = 1.16324\ \text{k}\Omega$$

The total input resistance is

$$R_{i-\text{total}} = R_i \,||\, R_{\text{th}} = 1.16324 \,||\, 14.985k = 1.079\ \text{k}\Omega$$

(b) The ac load resistance is $r_L = R_C || R_L = 35 || 4.7\ \text{k}\Omega = 4.143\ \text{k}\Omega$

(c) Voltage gain $A_v = \dfrac{r_L}{r_e'} = \dfrac{4.143 \times 10^3}{9.693} = 427.48$

3.7 COMMON-BASE AMPLIFIER

Figure 3.54 shows a common-base amplifier circuit using an *NPN* transistor. As the base of transistor is grounded, this circuit is also known as a *grounded-base amplifier*. The emitter-base junction is forward biased by the power supply voltage V_{EE} and the collector base junction is reverse biased by V_{CC}. Therefore, the transistor operates in the *active region*. The ac input signal is applied to the emitter-base terminals and the ac output signal is taken from the collector-base terminals. The capacitors C_1 and C_2 are called coupling capacitors. These capacitors are used to block the dc signal but pass the ac signal. Hence, these capacitors can isolate dc bias from ac signal.

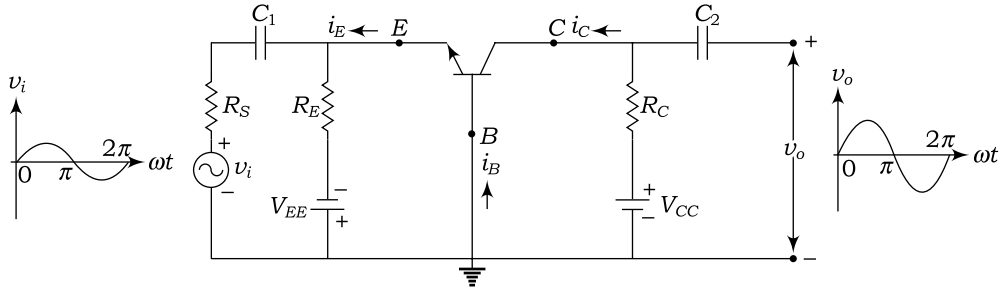


Fig. 3.54 Common-base amplifier circuit using NPN transistor

When the transistor operates at *Q*-point with dc power supply V_{EE} and V_{CC}, the output voltage V_o is equal to V_{CB} and it can be expressed as

$$V_o = V_{CB} = V_{CC} - I_C R_C \tag{3.67}$$

Whenever an ac voltage signal is applied across the emitter-base terminals, during the positive half-cycle of ac input voltage v_i, the forward bias voltage across emitter-base junction is decreased. As a result, the base current I_B decreases and the emitter current I_E decreases as $I_E \approx \beta I_B$. Subsequently, the collector current I_C also decreases. Then $I_C R_C$ voltage drop across resistance R_C decreases. Correspondingly, the output voltage V_o increases as $V_o = V_{CB} = V_{CC} - I_C R_C$. In this way, the positive half-cycle voltage will be available at the output without any phase shift.

During the negative half-cycle of ac input voltage v_i, the forward-bias voltage across emitter-base junction is increased. Consequently, the base current I_B increases and the emitter current I_E increases as $I_E \approx \beta I_B$. Then the collector current I_C also increases and $I_C R_C$ voltage drop across resistance R_C increases. Subsequently, the output voltage V_o decreases as $V_o = V_{CB} = V_{CC} - I_C R_C$. Thus, the negative half-cycle voltage will be available at the output without any phase shift as shown in Fig. 3.55.

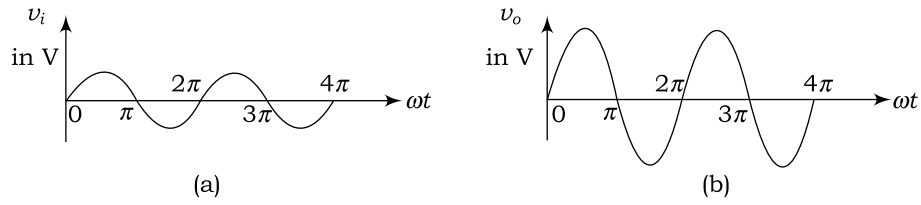


Fig. 3.55 (a) Input voltage v_i (b) Output voltage v_o

3.7.1 Characteristics of a Common-Base Amplifier

A common-base amplifier has the following characteristics:

1. It has large voltage gain (A_v). The value of A_v is about 1500.
2. Its current gain (A_I) is less than unity.
3. The power gain (A_P) is approximately equal to voltage gain.
4. The output signal has zero phase shift with respect to input signal.
5. Input impedance is very low and its value in the range of 30 Ω to 150 Ω.
6. Output impedance is very high and its value is about 500 kΩ.

3.7.2 Analysis of a Common-Base Amplifier

Figure 3.56 shows a common-base amplifier circuit where the battery symbol is not represented. It is always understood that '+' terminal is connected with positive terminal of battery and '–' terminal is connected with negative terminal of battery. The analysis of this amplifier can be done in two ways such as dc analysis and ac analysis. The dc and ac analyses of Fig. 3.56 are explained below:

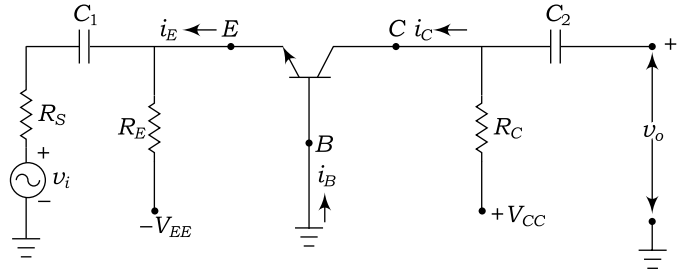


Fig. 3.56 Common-base amplifier

1. dc Analysis

With the capacitors open circuited, this circuit is same as good biasing circuit. The dc equivalent circuit of a common-base amplifier is shown in Fig. 3.57(a). The emitter current is $I_E = \dfrac{V_{EE} - V_{BE}}{R_E}$.

2. ac Analysis

The ac equivalent circuit of Fig. 3.56 can be drawn by the following steps:

(a) Remove all dc power supply by grounding them.

(b) Capacitors C_1 and C_2 are removed by short circuit.

Figure 3.57(b) shows the ac equivalent circuit of a common-base amplifier. This circuit can be analysed by using (i) hybrid-(h) model, and (ii) r_e model of a bipolar junction transistor.

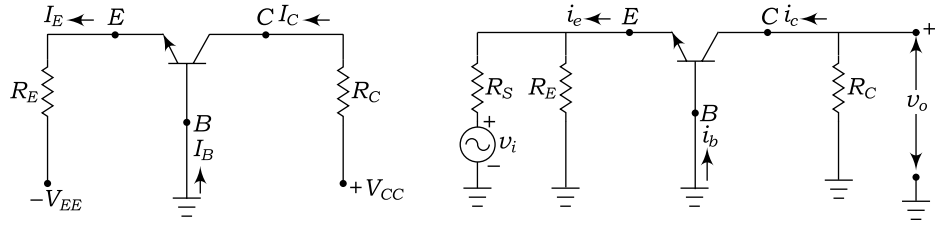


Fig. 3.57 (a) dc equivalent circuit of Fig. 3.56 (b) ac equivalent circuit of Fig. 3.56

(i) Analysis in h-parameter Model After substituting the approximate *h*-parameter model of the transistor, we get the ac equivalent circuit of common-base amplifier as depicted in Fig. 3.58. The input resistance, output resistance, voltage gain and current gain can be derived as follows:

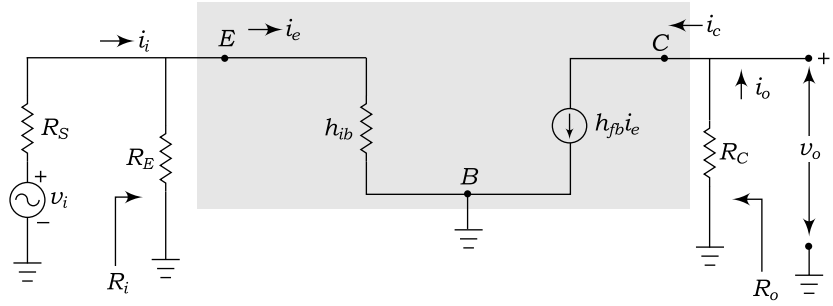


Fig. 3.58 ac equivalent circuit of Fig. 3.56 using approximate *h*-parameter model of transistor

The input resistance is equal to $R_i = R_E \| h_{ib} = \dfrac{R_E h_{ib}}{R_E + h_{ib}}$ (3.68)

When input voltage is equal to zero ($v_i = 0$), the output resistance is determined. Since $v_i = 0$, current $i_e = 0$ and $h_{fb} i_e = 0$. The current source behaves as open circuit. The output resistance is

$$R_o = R_C$$

When R_S is negligible, the input voltage is $v_i = h_{ib} i_e$ and the output voltage is

$$v_o = -i_o R_C = -h_{fb} i_e R_C \quad \text{as } i_o = h_{fb} i_e$$

The voltage gain is $$A_v = \frac{v_o}{v_i} = \frac{-h_{fb} i_e R_C}{h_{ib} i_e} = -\frac{h_{fb} R_C}{h_{ib}} \tag{3.69}$$

The current gain is the ratio of load current to the input current and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i} = \frac{-i_c}{i_i} = \frac{-h_{fb} i_e}{i_i} \quad \text{where, } i_e = i_i \frac{R_E}{R_E + h_{ib}} \tag{3.70}$$

Then the current gain is $$A_i = \frac{-h_{fb} i_e}{i_i} = -\frac{h_{fb} i_i \dfrac{R_E}{R_E + h_{ib}}}{i_i} = -h_{fb} \frac{R_E}{R_E + h_{ib}} \tag{3.71}$$

(ii) Analysis in r_e Parameter Model After substituting the approximate r_e parameter model of the transistor, we obtain the ac equivalent circuit of common-base amplifier as shown in Fig. 3.59. The input resistance, output resistance, voltage gain and current gain can be derived as follows:

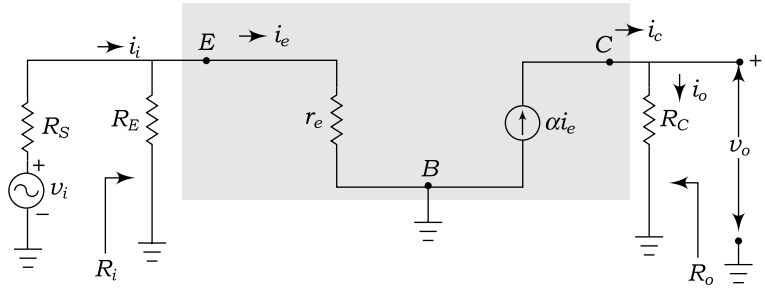


Fig. 3.59 ac equivalent circuit of Fig. 3.56 using approximate r_e parameter model of transistor

The input resistance is
$$R_i = R_E \| r_e = \frac{R_E r_e}{R_E + r_e} \tag{3.72}$$

The output resistance is
$$R_o = R_C \tag{3.73}$$

The current gain is the ratio of output current to the input current or the ratio of collector current to the emitter current. The current gain can be expressed as

$$A_i = \frac{i_o}{i_i} = \frac{i_c}{i_e} = \alpha \tag{3.74}$$

The voltage gain is the ratio of output voltage to the input voltage and it can be expressed as

$$A_v = \frac{v_o}{v_i}$$

When R_S is negligible, the input voltage is $v_i = i_e r_e$ and the output voltage is

$$v_o = i_o R_C = i_c R_L = \alpha i_e R_C \quad \text{as } i_c = \alpha i_e$$

The voltage gain is
$$A_v = \frac{v_o}{v_i} = \frac{\alpha i_e R_C}{i_e r_e} = \frac{\alpha R_C}{r_e} \tag{3.75}$$

Example 3.10 Figure 3.60 shows a common-base amplifier. Determine input resistance, current gain, voltage gain, power gain, and output voltage. Assume $\alpha = 0.99$.

Sol. Given: $V_{CC} = 12$ V, $-V_{EE} = -10$ V, $v_i = 20$ mV, $R_C = 10$ kΩ, $R_E = 22$ kΩ, $R_L = 4.7$ kΩ, and $\alpha = 0.99$

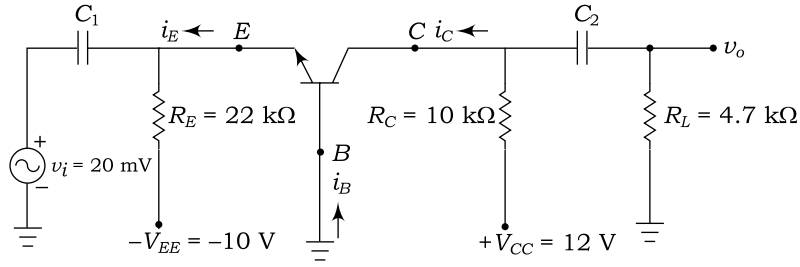


Fig. 3.60

The emitter current is $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{10 - 0.7}{22 \times 10^3} = 0.422 \times 10^{-3}$ A = 0.422 mA

The ac resistance of emitter diode is $r_e' = \dfrac{25 \text{ mV}}{I_E} = \dfrac{25}{0.422} = 59.24\ \Omega$

The input resistance looking from emitter is

$$R_i = r_e' = 59.24\ \Omega$$

The total input resistance is

$$R_{i-\text{total}} = R_i \| R_E = 59.24\ \Omega \| 22\ \text{k}\Omega = 59.08\ \Omega$$

The current gain is $A_i = \alpha = 0.99$

The ac load resistance is $r_L = R_C \| R_L = 10\ \text{k}\Omega \| 4.7\ \text{k}\Omega = 3.197\ \text{k}\Omega$

The voltage gain is $A_v = \dfrac{\alpha r_L}{r_e'} = \dfrac{0.99 \times 3.1972 \times 10^3}{59.24} = 53.43$

The power gain is $A_p = A_v A_i = 53.43 \times 0.99 = 52.895$

The power gain in decibel is $G_P = 10 \log_{10} A_p = 10 \log_{10} 52.895 = 17.23$ dB

The output voltage is $v_o = A_v v_i = 53.43 \times 20 \times 10^{-3}$ V = 1.068 V

Example 3.11 A common-base amplifier circuit is depicted in Fig. 3.61. Determine input resistance, current gain, voltage gain and power gain, output voltage Assume $\alpha = 0.95$.

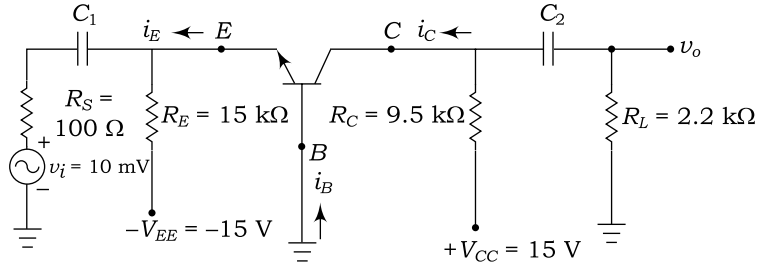


Fig. 3.61

Sol. Given: V_{CC} = 15 V, $-V_{EE}$ = –15 V, v_i = 10 mV, R_S = 100 Ω, R_C = 9.5 kΩ, R_E = 15 kΩ, R_L = 2.2 kΩ, and $\alpha = 0.95$

The emitter current is $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{15 - 0.7}{15 \times 10^3} = 0.953 \times 10^{-3}$ A = 0.953 mA

The ac resistance of emitter diode is $r_e' = \dfrac{25 \text{ mV}}{I_E} = \dfrac{25}{0.953} = 26.239\ \Omega$

The input resistance looking from emitter is

$$R_i = r_e' = 26.239\ \Omega$$

The total input resistance is

$$R_{i-\text{total}} = R_i \| R_E = 26.239\ \Omega \| 15\ \text{k}\Omega = 26.193\ \Omega$$

The current gain is $A_i = \alpha = 0.95$

The ac load resistance is $r_L = R_C \| R_L = 9.5 \| 2.2\ \text{k}\Omega = 1.786\ \text{k}\Omega$

When $r_e \| R_E \cong r_e$, the voltage gain from emitter to output is

$$A_v' = \frac{\alpha r_L}{r_e'} = \frac{0.95 \times 1.786 \times 10^3}{26.239} = 64.66$$

When $r_e \| R_E \cong r_e$, the voltage gain from source to output is

$$A_v = \frac{\alpha r_L}{r_e' + R_S} = \frac{0.95 \times 1.786 \times 10^3}{26.239 + 100} = 13.439$$

The output voltage is $v_o = A_v v_i = 13.439 \times 10 \times 10^{-3}\ \text{V} = 134.39\ \text{mV}$

3.8 COMMON-COLLECTOR AMPLIFIER

Figure 3.62 shows a common-collector amplifier circuit using *NPN* transistor. Its alternative representation is depicted in Fig. 3.63. Since R_C is zero, the collector terminal is at ac ground. For this reason, this circuit is also called *grounded collector amplifier*. The emitter-base junction of transistor is forward biased by the power supply V_{EE} and the collector-base junction of the transistor is reverse biased by the power supply V_{CC}. Therefore, this transistor operates in the active region.

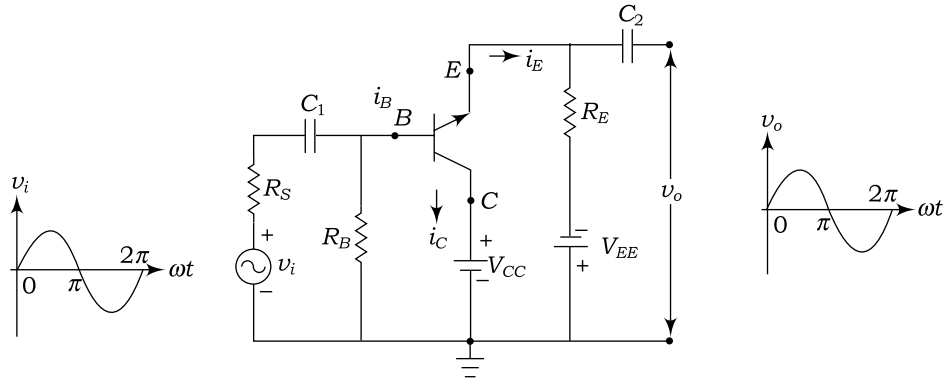


Fig. 3.62 Common-collector amplifier circuit using NPN transistor

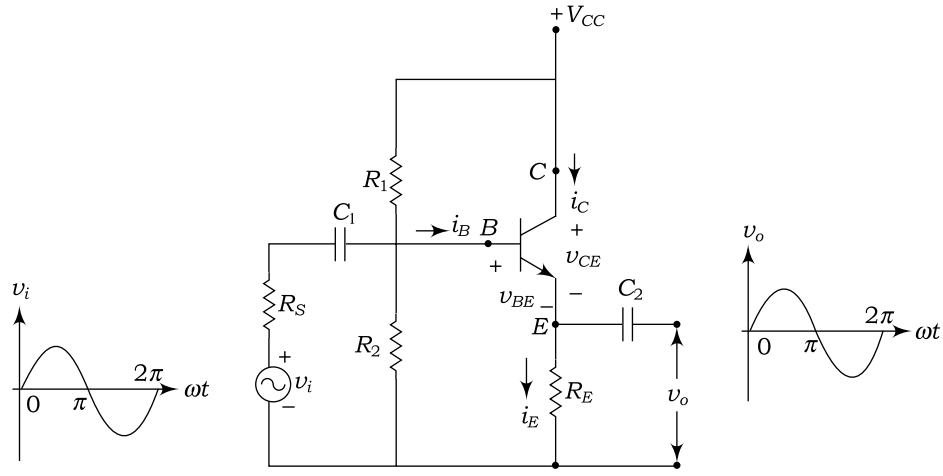


Fig. 3.63 Common-collector amplifier circuit using NPN transistor and single source

The quiescent (Q) operating can be determined by supply voltages V_{BB} and V_{CC} and resistances R_B and R_E. The ac input voltage signal is applied to the base collector junction of transistor and the output voltage signal is obtained from the emitter and collector terminals. Capacitors C_1 and C_2 are coupling capacitors. These capacitors are used to block the dc signal but pass the ac signal. Hence, these capacitors can isolate dc bias from ac signal. In this way, coupling capacitors provide dc isolation at the input and output of the amplifier circuit.

When the transistor operates at Q-point with dc power supply V_{EE} and V_{CC}, the output voltage V_o is equal to voltage drop across resistance R_E and it can be expressed as

$$V_o = I_E R_E = \beta I_B R_E \tag{3.76}$$

When an ac voltage signal is applied across the base-collector terminals, during the positive half-cycle of ac input voltage v_i, the forward-bias voltage across base-collector junction is increased. As a result, the base current I_B increases. Then emitter current I_E also increases since $I_E = I_C + I_B$. Subsequently, $I_E R_E$, the voltage drop across resistance R_E increases. Hence, the positive half-cycle voltage will be available at the output without any phase shift.

During the negative half-cycle of ac input voltage v_i, the forward-bias voltage across base-collector junction is decreased. Consequently, the base current (I_B) and the emitter current (I_E) are decreased. Since the emitter current I_E decreases, $I_E R_E$ voltage drop across resistance R_E decreases. Subsequently the output voltage V_o decreases. Thus, the negative half-cycle voltage will be available at the output without any phase shift as shown in Fig. 3.64.

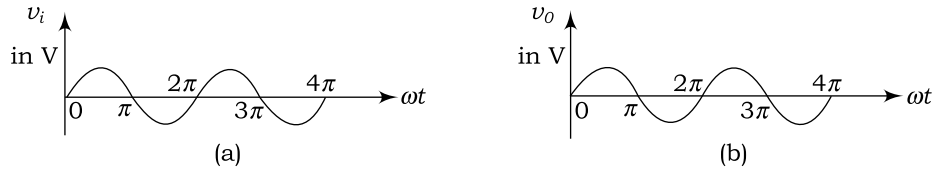


Fig. 3.64 (a) Input voltage v_i (b) Output voltage v_o

3.8.1 Characteristics of a Common-Collector Amplifier

A common-collector amplifier has the following characteristics:

1. Its voltage gain (A_V) is approximately unity and it has large voltage gain (A_v).
2. Its current gain (A_I) is high. The value of A_I is in the range of 50 to 500.
3. The power gain (A_P) is approximately equal to current gain.
4. The output signal has zero phase shifts with respect to input signal
5. Input impedance is very high and its value in the range of 20 kΩ to 500 kΩ
6. Output impedance is low and its value in the range of 50 Ω to 1000 Ω

3.8.2 Analysis of a Common-Collector Amplifier

The simplified representation of a common-collector amplifier circuit (Fig. 3.62) is shown in Fig. 3.65 where R_L is the load resistance and the battery symbol is not represented. It is always understood that '+' terminal is connected with positive terminal of battery and '–' terminal is connected with negative terminal of battery. The

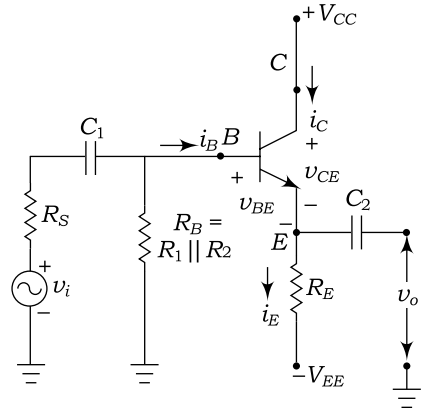


Fig. 3.65 Common collector amplifier

analysis of this amplifier can be done in two ways such as dc analysis and ac analysis. The dc and ac analyses of Fig. 3.65 are explained below:

1. dc Analysis

With the capacitors being open circuits, this circuit behaves as a biasing circuit. The dc equivalent circuit of common-collector amplifier is shown in Fig. 3.66(a). The emitter current is

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta}}$$

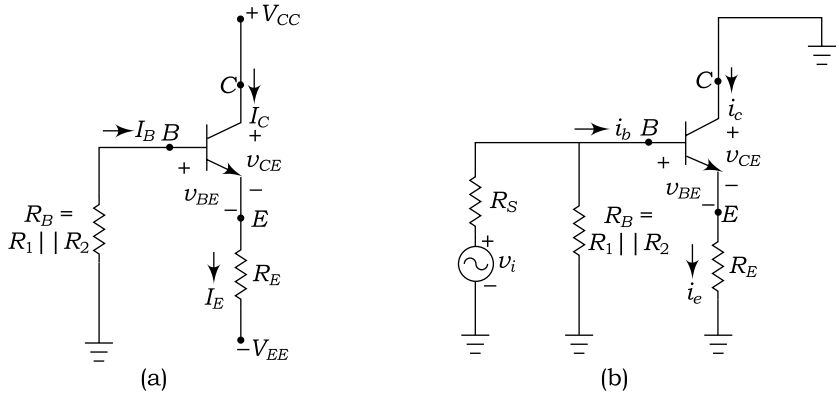


Fig. 3.66 (a) dc equivalent circuit of Fig. 3.65 (b) ac equivalent circuit of Fig. 3.65

2. ac Analysis

The ac equivalent circuit of a common-collector amplifier is depicted in Fig. 3.66(b). This circuit can be analysed by using (i) hybrid-(h) model, and (ii) r_e model of bipolar junction transistor.

(i) Analysis in *h*-parameter Model After substituting the approximate h-parameter model of the transistor, we obtain the small signal ac equivalent circuit of common-collector amplifier (emitter follower) as depicted in Fig. 3.67. The simplified representation of Fig. 3.67 is shown in Fig. 3.68. The input resistance, output resistance, voltage gain and current gain can be derived as follows:

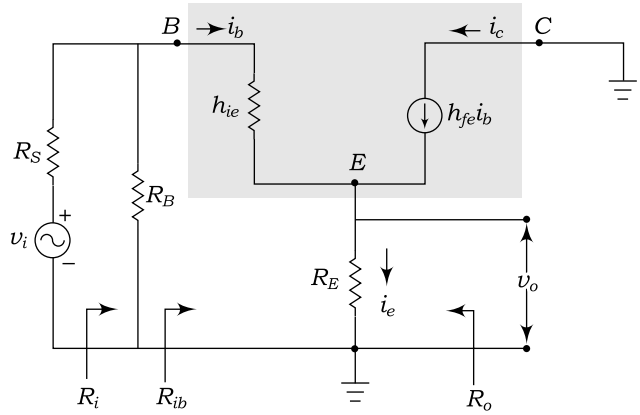


Fig. 3.67 Small-signal ac equivalent circuit of Fig. 3.65 using approximate *h*-parameter model of transistor

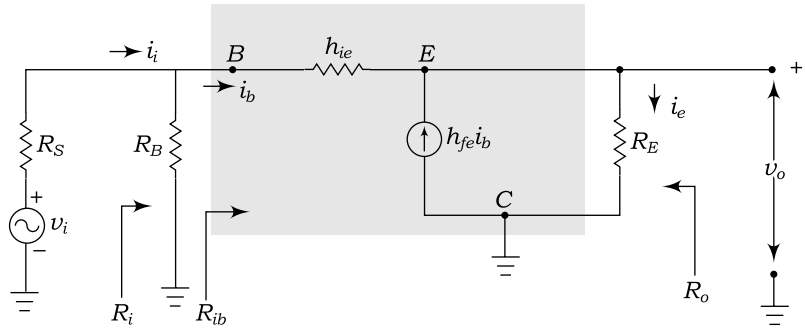


Fig. 3.68 Simplified small-signal ac equivalent circuit of Fig. 3.67

The current $$i_e = i_b + h_{fe}i_b = (1 + h_{fe})i_b \tag{3.77}$$

When R_S is neglected, the input voltage is equal to

$$v_i = i_b h_{ie} + i_e R_E = i_b h_{ie} + (1 + h_{fe})i_b R_E \tag{3.78}$$

The input resistance looking into the base is $$R_{ib} = \frac{v_i}{i_b} = h_{ie} + (1 + h_{fe})R_E \tag{3.79}$$

The input resistance is equal to $$R_i = R_B \| R_{ib} = \frac{R_B R_{ib}}{R_B + R_{ib}} \tag{3.80}$$

When R_S is negligible, the input voltage is $v_i = h_{ie}i_b + i_e R_E = h_{ie}i_b + (1 + h_{fe})i_b R_E$ and the output voltage is

$$v_o = i_e R_E = (1 + h_{fe})i_b R_E \quad \text{as } i_e = (1 + h_{fe})i_b \tag{3.81}$$

The voltage gain is $$A_v = \frac{v_o}{v_i} = \frac{(1 + h_{fe})i_b R_E}{h_{ie}i_b + (1 + h_{fe})i_b R_E} = \frac{(1 + h_{fe})R_E}{h_{ie} + (1 + h_{fe})R_E} \tag{3.82}$$

The current gain is the ratio of load current to the input current and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{i_o}{i_i} = \frac{(1 + h_{fe})i_b}{i_i} \quad \text{where, } i_b = i_i \frac{R_E}{R_E + R_{ib}}$$

Then the current gain is $$A_i = \frac{(1 + h_{fe})i_i \dfrac{R_B}{R_B + h_{ib}}}{i_i} = (1 + h_{fe})\frac{R_B}{R_B + R_{ib}} \tag{3.83}$$

When input voltage is equal to zero ($v_i = 0$), the output resistance can be determined.

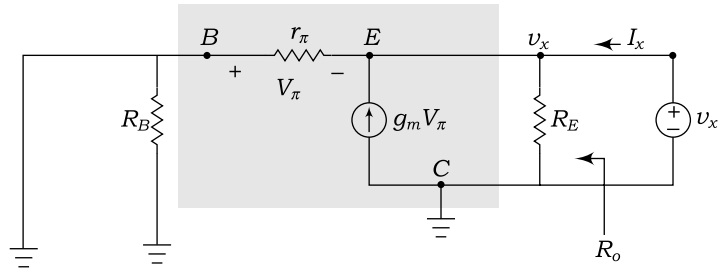


Fig. 3.69 Small-signal ac equivalent circuit to determine output resistance

The KCL equation at E is $$I_x + g_m V_\pi = \frac{V_x}{R_E} + \frac{V_x}{r_\pi}$$

Then $$I_x - g_m V_x = \frac{V_x}{R_E} + \frac{V_x}{r_\pi} \quad \text{as} \quad V_\pi = -V_x$$

or $$I_x = \left(g_m + \frac{1}{R_E} + \frac{1}{r_\pi} \right) V_x$$

Then $$\frac{I_x}{V_x} = \left(g_m + \frac{1}{R_E} + \frac{1}{r_\pi} \right)$$

or $$\frac{1}{R_o} = \left(g_m + \frac{1}{R_E} + \frac{1}{r_\pi} \right) = \left(g_m + \frac{1}{r_\pi} \right) + \frac{1}{R_E} = \left(\frac{g_m r_\pi + 1}{r_\pi} \right) + \frac{1}{R_E}$$

$$= \frac{1+\beta}{r_\pi} + \frac{1}{R_E} \quad \text{as } g_m r_\pi = \beta$$

The output resistance is $$R_o = \frac{V_x}{I_x} = \frac{r_\pi}{1+\beta} \| R_E = \frac{\beta r_e}{1+\beta} \| R_E \quad \text{as } r_\pi = \beta r_e \tag{3.84}$$

(ii) Analysis in r_e Parameter Model After substituting the approximate r_e parameter model of the transistor, we get the small signal ac equivalent circuit of common-collector amplifier as depicted in Fig. 3.70. The input resistance, output resistance, voltage gain and current gain can be derived as follows:

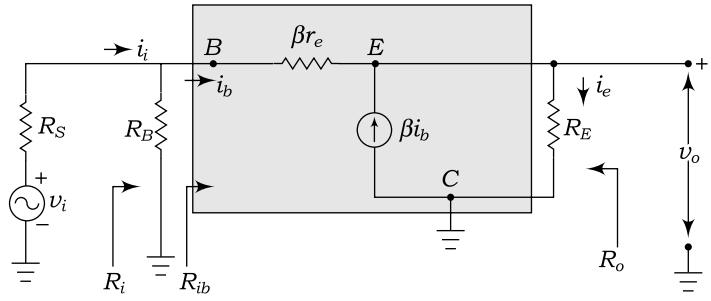


Fig. 3.70 ac equivalent circuit of Fig. 3.57 using approximate r_e parameter model of transistor

The current $i_e = i_b + \beta i_b = (1 + \beta) i_b$

Assume that R_S is neglected, then input voltage is equal to

$$v_i = i_b \beta r_e + i_e R_E = i_b \beta r_e + (1+\beta) i_b R_E \tag{3.85}$$

The input resistance looking into the base is

$$R_{ib} = \frac{v_i}{i_b} = \beta r_e + (1+\beta) R_E \approx \beta (r_e + R_E) \quad \text{as } \beta >> 1$$

The input resistance is equal to $$R_i = R_B \| R_{ib} = \frac{R_B R_{ib}}{R_B + R_{ib}} = \frac{R_B \beta (r_e + R_E)}{R_B + \beta (r_e + R_E)} \tag{3.86}$$

When R_S is negligible, the input voltage is $v_i = i_b \beta r_e + i_e R_E = i_b \beta r_e + (1 + \beta) i_b R_E$ and the output voltage is

$$v_o = i_e R_E = (1+\beta) i_b R_E \quad \text{as } i_e = (1+\beta) i_b \tag{3.87}$$

The voltage gain is $$A_v = \frac{v_o}{v_i} = \frac{(1+\beta) i_b R_E}{\beta r_e i_b + (1+\beta) i_b R_E} = \frac{\beta R_E}{\beta r_e + \beta R_E} = \frac{R_E}{r_e + R_E} \tag{3.88}$$

The current gain is the ratio of load current to the input current and it can be expressed as

$$A_i = \frac{i_L}{i_i} = \frac{i_o}{i_i} = \frac{(1+\beta)i_b}{i_i} \quad \text{where, } i_b = i_i \frac{R_B}{R_B + R_{ib}}$$

Then the current gain is

$$A_i = \frac{(1+\beta)i_i \dfrac{R_B}{R_B + R_{ib}}}{i_i} = (1+\beta)\frac{R_B}{R_B + R_{ib}} = \frac{\beta R_B}{R_B + R_{ib}} \approx \beta \quad \text{as } \beta >> 1 \tag{3.89}$$

The output resistance is $R_o = \dfrac{\beta r_e}{1+\beta} \| R_E$ as $r_\pi = \beta r_e$ (3.90)

Example 3.12 Figure 3.71 shows an emitter-follower circuit. Find the input resistance and voltage gain.

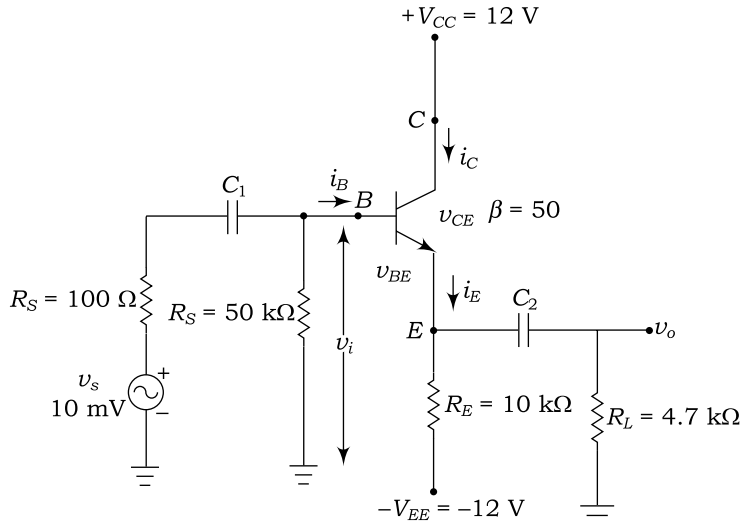


Fig. 3.71

Sol. Given: V_{CC} = 12 V, $-V_{EE}$ = –12 V, v_s = 10 mV, R_S = 100 Ω, R_B = 50 kΩ, R_E = 10 kΩ, R_L = 4.7 kΩ, and $\beta = 50$

The emitter current $I_E = \dfrac{V_{EE} - V_{BE}}{R_E + \dfrac{R_B}{\beta}} = \dfrac{12 - 0.7}{10 \times 10^3 + \dfrac{50 \times 10^3}{50}} = 1.027 \times 10^{-3}\ \text{A} = 1.027\ \text{mA}$

The ac resistance of emitter diode, $r_e' = \dfrac{25\ \text{mV}}{I_E} = \dfrac{25}{1.027} = 24.342\ \Omega$

The input resistance looking from base is

$$R_i = \beta(R_E + r_e') = 50(10 \times 10^3 + 24.342)\ \Omega = 501.21\ \text{k}\Omega$$

The total input resistance is

$$R_{i\_\text{total}} = R_i \| R_B = 501.21 \| 50\ \text{k}\Omega = 45.464\ \text{k}\Omega$$

The ac load resistance is $r_L = R_E \| R_L = 10 \| 4.7\ \text{k}\Omega = 3.1972\ \text{k}\Omega$

When R_S is negligible, the input voltage is

$$v_i = i_b\beta r_e + i_e r_L = i_b\beta r_e + (1+\beta) i_b r_L$$

The output voltage is

$$v_o = i_e r_L = (1+\beta) i_b r_L \text{ as } i_e = (1+\beta) i_b$$

The voltage gain is $A_v = \dfrac{v_o}{v_i} = \dfrac{(1+\beta) i_b r_L}{\beta r_e i_b + (1+\beta) i_b r_L}$ as $\beta >> 1$

$$= \frac{\beta r_L}{\beta r_e + \beta r_L} = \frac{r_L}{r_e + r_L} = \frac{3197.2}{24.39 + 3197.2} = 0.9924$$

Voltage gain from source to output is $A_v = \dfrac{r_L}{r_e' + R_S} = \dfrac{1.786 \times 10^3}{26.239 + 100} = 14.147$

The input voltage is $v_i = v_s \times \dfrac{R_{i\_\text{total}}}{R_S + R_{i\_\text{total}}} = 100 \times \dfrac{45.464\ \text{k}\Omega}{100\Omega + 45.464\ \text{k}\Omega}\ \text{mV} = 99.78\ \text{mV}$

The output voltage is $v_o = A_v v_i = 0.9924 \times 99.78\ \text{mV} = 99.02\ \text{mV}$

3.9 COMPARISON OF COMMON-EMITTER, COMMON-BASE AND COMMON-COLLECTOR AMPLIFIERS

The comparison between common-emitter (*CE*), common-base (*CB*) and common-collector (*CC*) amplifiers is given in Table 3.1.

Table 3.1 Comparison of CE, CB and CC amplifiers

Parameters	*Common-Emitter (CE) Amplifier*	*Common-Base (CB) Amplifier*	*Common-Collector (CC) Amplifier*
Input resistance	Moderate βr_e	Low r_e	High βR_E
Output resistance	High R_C	High R_C	Low r_e
Voltage gain	High $\dfrac{r_L}{r_e}$	High $\dfrac{r_L}{r_e}$	About 1
Current gain	High β	Low, about 1	High $(1 + \beta)$
Power gain	High	Moderate	Low
Phase shift	180°	0°	0°

3.10 DARLINGTON CONNECTION OF BJT

Figure 3.72(a) shows the Darlington connection of two bipolar junction transistors. The composite transistor works as a single unit with a current gain, which is the product of the current gain of individual transistors. When the current gain of a transistor is β_1 and the current gain of the other transistor is β_2, the current gain of composite transistor is $\beta_D = \beta_1\beta_2$.

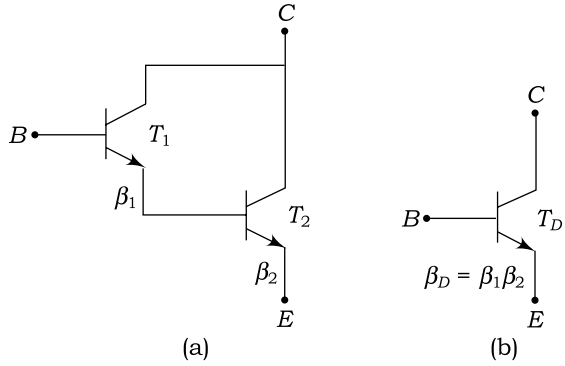


Fig. 3.72 (a) Darlington connection of T_1 and T_2 (b) Single Darlington transistor T_D

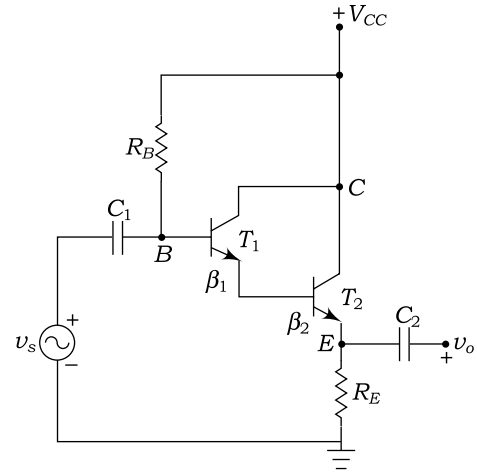


Fig. 3.73 Emitter-follower circuit using Darlington transistor

When two identical transistors are connected in Darlington form, the overall current will be

$$\beta_D = \beta_1\beta_2 = \beta^2 \quad \text{as} \quad \beta_1 = \beta_2 = \beta \tag{3.91}$$

If the current of the transistor is high and β is about 200, the overall gain of Darlington pair is $\beta_D = 200 \times 200 = 40000$. Usually, Darlington pairs are available in IC packages and each package has three terminals, namely emitter, base and collector. Figure 3.72(b) shows a single Darlington transistor which has very high current and this transistor is commonly used in an emitter-follower circuit . A emitter follower circuit using Darlington transistor is depicted in Fig. 3.73. The analysis of this amplifier can be done in two ways such as dc analysis and ac analysis. The dc and ac analyses of Fig. 3.73 are discussed in this section.

3.10.1 dc Analysis of a Darlington Transistor

Figure 3.74 shows the biasing of a Darlington transistor having β_D current gain. The base current is equal to $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}$ and the emitter current is $I_E = (1 + \beta_D)I_B \approx \beta_D I_B$

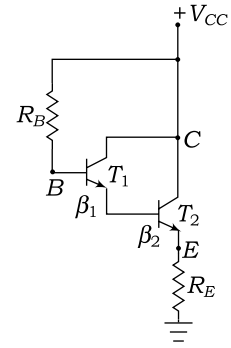


Fig. 3.74 Biasing circuit of Darlington transistor

The voltage at E is $V_E = I_E R_E = \beta_D I_B R_E$ (3.92)

The voltage at B is $V_B = V_{BE} + V_E = V_{BE} + I_E R_E = V_{BE} + \beta_D I_B R_E$ (3.93)

3.10.2 ac Analysis of a Darlington Transistor

The ac equivalent circuit of Darlington emitter follower is depicted in Fig. 3.75(a) where Darlington transistor is replaced by input resistance r_i and a current source $\beta_D i_b$. The simplified representation of Fig. 3.75(a) is given in Fig. 3.75(b).

The base current is equal to $i_b = \dfrac{v_i - v_o}{r_i}$ and

The emitter current is $i_e = i_b + i_c = i_b + \beta_D i_b = (1 + \beta_D)i_b$

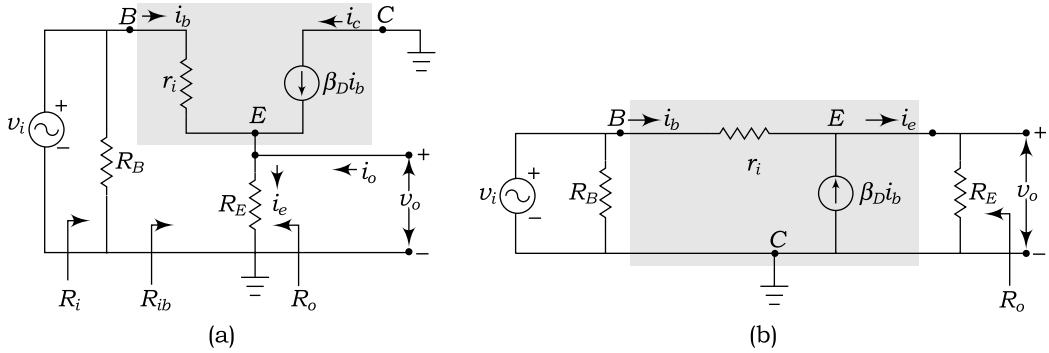


Fig. 3.75 (a) Small signal ac equivalent circuit of Fig. 3.74 (b) Alternative representation of Fig. 3.75(a)

The output voltage is $v_o = i_e R_E = (1 + \beta_D) i_b R_E$

The input voltage is $v_i = i_b r_i + i_e R_E = i_b r_i + (1 + \beta_D) i_b R_E$

The voltage is

$$A_v = \frac{v_o}{v_i} = \frac{(1 + \beta_D) i_b R_E}{i_b r_i + (1 + \beta_D) i_b R_E} = \frac{(1 + \beta_D) R_E}{r_i + (1 + \beta_D) R_E}$$

$$= \frac{\beta_D R_E}{r_i + \beta_D R_E} \quad \text{as } \beta_D >> 1$$

$$= \frac{\beta_D R_E}{\beta_D R_E} \approx 1 \quad \text{as } \beta_D R_E >> r_i \tag{3.94}$$

The ac input resistance looking from base is expressed by $R_{ib} = \frac{v_i}{i_b} = r_i + (1 + \beta_D) R_E$

The ac input resistance looking from base is expressed by $R_i = R_B \| R_{ib} = \frac{R_B R_{ib}}{R_B + R_{ib}}$

The ac output current is $i_o = i_e = i_b + i_c = i_b + \beta_D i_b = (1 + \beta_D) i_b$

The current ratio of a Darlington transistor is equal to $\frac{i_o}{i_b} = (1 + \beta_D) \approx \beta_D$ as $\beta_D >> 1$

The current ratio $\frac{i_b}{i_i} = \frac{R_B}{R_B + (r_i + \beta_D R_E)} = \frac{R_B}{R_B + \beta_D R_E}$ as $\beta_D R_E >> r_i$

The current gain of the circuit is $A_i = \frac{i_o}{i_i} = \frac{i_o}{i_b} \frac{i_b}{i_i} = \beta_D \frac{R_B}{R_B + \beta_D R_E}$ (3.95)

Figure 3.76 shows the small-signal ac equivalent circuit to determine the output resistance of the circuit when a voltage v_x is applied at output terminal and input voltage $v_s = 0$.

Applying the KCL at node x, we get $i_x + \beta_D i_b = \frac{v_x}{R_E} + \frac{v_x}{r_i}$ where, $i_b = -\frac{v_x}{r_i}$

or $$i_x = \frac{v_x}{R_E} + \frac{v_x}{r_i} - \beta_D i_b = \frac{v_x}{R_E} + \frac{v_x}{r_i} + \beta_D \frac{v_x}{r_i} = \left(\frac{1}{R_E} + \frac{1}{r_i} + \frac{\beta_D}{r_i} \right) v_x$$

The output impedance is equal to

$$z_o = \frac{1}{\frac{1}{R_E} + \frac{1}{r_i} + \frac{\beta_D}{r_i}} = R_E \| r_i \| \frac{r_i}{\beta_D} \approx \frac{r_i}{\beta_D} \quad \text{as } R_E >> \frac{r_i}{\beta_D} \text{ and } r_i >> \frac{r_i}{\beta_D} \tag{3.96}$$

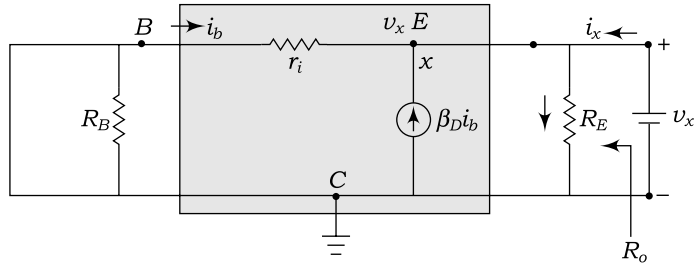


Fig. 3.76 Small-signal ac equivalent circuit of Fig. 3.74 to determine output resistance

3.11 MULTISTAGE AMPLIFIERS

Usually, the voltage gain or power gain of a single-stage small-signal amplifier is not sufficient for any practical applications. Therefore, we have to use more than one stage of amplification to get the desired voltage gain as well as power gain. Such an amplifier is known as *multistage amplifier*. The multistage amplifiers are most commonly used in radio and television receivers and communication equipments.

In a multistage amplifier, the output of first-stage is fed to the next stage as an input. This connection is called *cascade connection* of amplifiers. Figure 3.77 shows a two-stage *cascade amplifier*. In this circuit, v_{i_1} is the input voltage and v_{o_1} is the output voltage of first-stage amplifier and v_{i_2} is the input voltage and v_{o_2} the output voltage of second-stage amplifier. A two-stage common-emitter amplifier is depicted in Fig. 3.78.

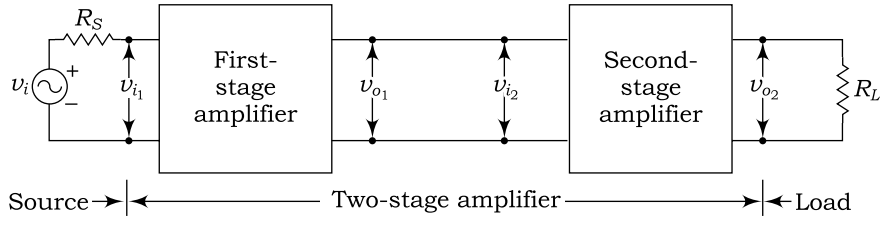


Fig. 3.77 Two-stage cascade amplifier

A multistage amplifier using two or more single-stage common-emitter amplifiers is known as *cascade amplifier*. The cascade term represents the type of connection used for coupling between two amplifier stages. When a common-emitter amplifier is used as first-stage amplifier, a common-base or common-collector is used as second-stage amplifier, this multistage amplifier is called a cascade amplifier. The cascade connection is not only used in a bipolar junction transistor (BJT) amplifier but also in Field Effect Transistor (FET) amplifiers. In this chapter, different coupling schemes used in amplifiers and operation of multistage amplifiers are discussed elaborately.

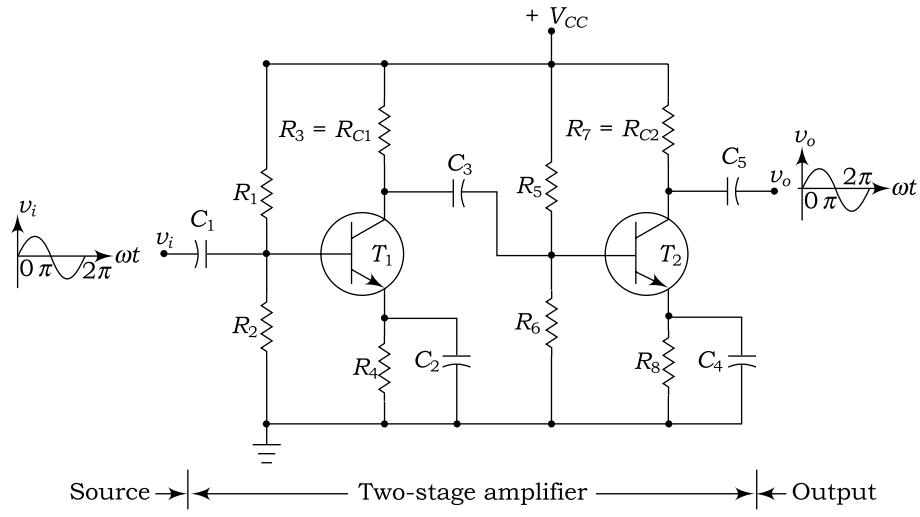


Fig. 3.78 Two-stage common-emitter amplifier

3.12 VOLTAGE GAIN, CURRENT GAIN AND POWER GAIN OF MULTISTAGE AMPLIFIERS

In a multistage amplifier, the output voltage of the first stage is used as input voltage of the second-stage amplifier. Again, the output of a second-stage amplifier acts as input to the third stage, and so on. Figure 3.79 shows the simplified representation of an *n*-stage common-emitter amplifier. The derivation of voltage gain, current gain and power gain for an *n*-stage amplifier is explained in this section.

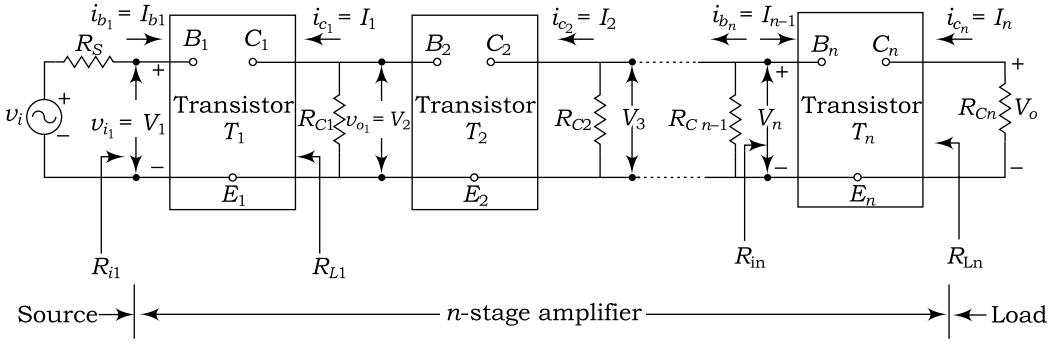


Fig. 3.79 *n*-stage common-emitter amplifier

3.12.1 Voltage Gain

The voltage gain of a multistage or cascade-connected amplifier is equal to the product of the voltage gains of the individual stages.

When $A_{v_1}, A_{v_2}, A_{v_3}$... and A_{v_n} are the individual stage gains of an *n*-stage amplifier, the overall voltage gain is

$$A_v = A_{v_1} A_{v_2} A_{v_3} \ldots A_{v_{n-1}} A_{v_n}$$

The voltage gain of a first-stage amplifier is

$$A_{v_1} = \frac{v_{o_1}}{v_{i_1}} = \frac{\text{Output voltage of first stage}}{\text{Input voltage of first stage}} = \frac{V_2}{V_1} \quad \text{as } v_{i_1} = V_1 \text{ and } v_{o_1} = V_2$$
$$= |A_{v_1}| \angle \theta_1 \tag{3.97}$$

where, $|A_{v_1}|$ is the amplitude of voltage gain, and

θ_1 is the phase angle of output voltage with respect to input voltage.

Similarly, the voltage gain of a second-stage amplifier is

$$A_{v_2} = \frac{v_{o_2}}{v_{i_2}} = \frac{\text{Output voltage of second stage}}{\text{Input voltage of second stage}} = \frac{V_3}{V_2} \quad \text{as } v_{i_2} = v_{o_1} = V_2 \text{ and } v_{o_2} = V_3$$
$$= |A_{v_2}| \angle \theta_2 \tag{3.98}$$

where, $|A_{v_2}|$ is the amplitude of voltage gain, and

θ_2 is the phase angle of output voltage with respect to input voltage.

In the same way, the voltage gain of n stages of the cascade amplifier is

$$A_v = \frac{v_{o_n}}{v_{i_1}} = \frac{\text{Output voltage of the } n^{\text{th}} \text{ stage}}{\text{Input voltage of first stage}} = \frac{V_o}{V_1} \quad \text{as } v_{i_1} = V_1 \text{ and } v_{o_n} = V_o$$
$$= |A_v| \angle \theta \tag{3.99}$$

where, $|A_v|$ is the amplitude of voltage gain n stages of the cascade amplifier, and

θ is the phase angle of output voltage, v_{o_n} or V_o with respect to input voltage, v_{i_1} or V_1.

Since $\frac{V_o}{V_1} = \frac{V_2}{V_1}\frac{V_3}{V_2}\frac{V_4}{V_3}\frac{V_5}{V_4}.....\frac{V_n}{V_{n-1}}\frac{V_o}{V_n}$, this equation can be represented by

$$A_v = A_{v_1} A_{v_2} A_{v_3} ... A_{v_{n-1}} A_{v_n}$$

Then
$$|A_v| \angle \theta = |A_{v_1}| \angle \theta_1 |A_{v_2}| \angle \theta_2 |A_{v_3}| \angle \theta_3 ... |A_{v_{n-1}}| \angle \theta_{n-1} |A_{v_n}| \angle \theta_n$$
$$= |A_{v_1}||A_{v_2}||A_{v_3}|...|A_{v_{n-1}}||A_{v_n}| \angle \theta_1 + \theta_2 + \theta_3 ... + \theta_{n-1} + \theta_n$$

Therefore, $|A_v| = |A_{v_1}||A_{v_2}||A_{v_3}|...|A_{v_{n-1}}||A_{v_n}|$ and $\angle\theta = \angle\theta_1 + \theta_2 + \theta_3 ... + \theta_{n-1} + \theta_n$

The magnitude of voltage gain is equal to the product of magnitude of the voltage gains of each stage and the total phase shift of a multistage amplifier is equal to the sum of the phase shifts by each stage.

Sometimes the amplifier voltage gain is expressed in decibels (dB). If $G_{v_1} G_{v_2} G_{v_3} ... G_{v_{n-1}} G_{v_n}$ are the gain of individual stage in decibels (dB), the overall voltage gain in decibels is

$$G_v = G_{v_1} + G_{v_2} + G_{v_3} ... + \cdot G_{v_{n-1}} + G_{v_n}$$
$$= 20 \log_{10} A_{v_1} + 20 \log_{10} A_{v_2} + 20 \log_{10} A_{v_3} ... + 20 \log_{10} A_{v_{n-1}} + 20 \log_{10} A_{v_n}$$
$$= 20 \log_{10} A_v \qquad \text{As } G_{v_1} = 20 \log_{10} A_{v_1}, G_{v_2} = 20 \log_{10} A_{v_2} ... G_{v_n} = 20 \log_{10} A_{v_n} \tag{3.100}$$

3.12.2 Current Gain

The current gain of a first-stage amplifier is the ratio of the output current i_{c_1} to the input base current i_{b_1} and it can be expressed as

$$A_{I_1} = \frac{i_{c_1}}{i_{b_1}} = \frac{I_1}{I_{b1}} \quad \text{as} \quad i_{c_1} = I_1 \text{ and } i_{b_1} = I_{b1} \tag{3.101}$$

Similarly, the current gain of a second-stage amplifier is

$$A_{I_2} = \frac{i_{c_2}}{i_{b_2}} = \frac{I_2}{I_1} \quad \text{as} \quad i_{c_2} = I_2 \text{ and } i_{b_2} = I_1 \tag{3.102}$$

Then the current gain of an n^{th} stage amplifier is

$$A_{I_n} = \frac{i_{c_n}}{i_{b_n}} = \frac{I_n}{I_{n-1}} \quad \text{as} \quad i_{c_n} = I_n \text{ and } i_{b_n} = I_{n-1} \tag{3.103}$$

In the same way, the current gain of an n-stage amplifier A_I is defined as the ratio of the output current the n^{th} stage (last stage) to the input (base) current of the first stage and it can be expressed as

$$A_I = \frac{i_{c_n}}{i_{b_1}} = \frac{I_n}{I_{b1}} \quad \text{as} \quad i_{c_n} = I_n \text{ and } i_{b_1} = I_{b1}$$

Since $\frac{I_n}{I_{b1}} = \frac{I_1}{I_{b1}}\frac{I_2}{I_1}\frac{I_3}{I_2}\frac{I_4}{I_3}.....\frac{I_{n-1}}{I_{n-2}}\frac{I_n}{I_{n-1}}$, the current gain is

$$A_I = A_{I_1} A_{I_2} A_{I_3} ... A_{I_{n-1}} A_{I_n}$$

3.12.3 Power Gain

The overall power gain of the n-stage amplifier is

$$\begin{aligned} A_P &= \frac{\text{Output power}}{\text{Input power}} = \frac{V_o I_n}{V_1 I_{b1}} = \frac{V_o}{V_1} \times \frac{I_n}{I_{b1}} = A_v A_I \\ &= (A_{v_1} A_{v_2} A_{v_3} ... A_{v_{n-1}} A_{v_n}) \times (A_{I_1} A_{I_2} A_{I_3} ... A_{I_{n-1}} A_{I_n}) \\ &\qquad \text{As } A_v = A_{v_1} A_{v_2} A_{v_3} ... A_{v_{n-1}} A_{v_n} \text{ and } A_I = A_{I_1} A_{I_2} A_{I_3} ... A_{I_{n-1}} A_{I_n} \\ &= A_{v_1} A_{I_1} \times A_{v_2} A_{I_2} \times A_{v_3} A_{I_3} \times ... A_{v_{n-1}} A_{I_{n-1}} \times A_{v_n} A_{I_n} \\ &= A_{P_1} A_{P_2} A_{P_3} ... A_{P_{n-1}} A_{P_n} \quad \text{as } A_{P_1} = A_{v_1} A_{I_1} ... \text{and } A_{P_n} = A_{v_n} A_{I_n} \end{aligned} \tag{3.104}$$

The overall power gain in decibel is

$$G_P = 10 \log_{10} A_P \tag{3.105}$$

Figure 3.80 shows the k^{th} stage common-emitter amplifier where V_k is input voltage, V_{k+1} is output voltage, R_{ik} is input resistance and R_{Lk} is the effective load resistance at the collector of the k^{th} transistor.

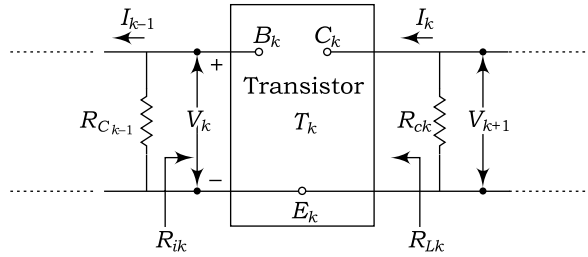


Fig. 3.80 k^{th} stage common-emitter amplifier

The voltage gain of the k^{th} stage amplifier is $A_{v_k} = A_{I_k} \dfrac{R_{Lk}}{R_{ik}}$ (3.106)

The current gain of the n^{th} stage amplifier is $A_{I_n} = -\dfrac{h_{fe}}{1 + h_{oe} R_{Ln}}$ (3.107)

The input impedance of the n^{th} stage amplifier is $R_{in} = h_{ie} + h_{re} A_{In} R_{Ln}$ where, $R_{Ln} = R_{Cn}$

The effective load resistance on the $(n-1)^{th}$ is equal to $R_{C \cdot n-1} \| R_{in}$.

Then $R_{L \cdot n-1} = \dfrac{R_{C \cdot n-1} R_{in}}{R_{Cn-1} + R_{in}}$ (3.108)

The voltage gain the $(n-1)^{th}$ stage amplifier is $A_{v_{n-1}} = A_{I_{n-1}} \dfrac{R_{Ln-1}}{R_{in-1}}$ (3.109)

The current gain of the $(n-1)^{th}$ stage amplifier is $A_{I_{n-1}} = -\dfrac{h_{fe}}{1 + h_{oe} R_{Ln-1}}$ (3.110)

Then input impedance of the $(n-1)^{th}$ stage amplifier is $R_{in-1} = h_{ie} + h_{re} A_{In-1} R_{Ln-1}$

In this way, we can compute the voltage, gain current and input resistance and effective load resistance in each stage.

Example 3.13 Two amplifiers are connected in cascade. When voltage gain of an amplifier is 10 and of the other is 20, determine the overall voltage gain in dB?

Sol. Given: $A_{v1} = 10$ and $A_{v2} = 20$

The overall voltage gain is $A_v = A_{v1} \times A_{v2} = 10 \times 20 = 200$

The gain dB is $G_v = 20 \log_{10} A_v = 20 \log_{10} 200 = 46.02$ dB

Example 3.14 When three amplifiers are connected in cascade with an input 0.025 peak to peak voltage, the output voltage is 15 V peak to peak. If the voltage gain of the first-stage amplifier is 5 and of the second-stage amplifier is 7.5, determine (a) the overall voltage gain, (b) gain of third stage amplifier and (c) input voltage of second-stage amplifier

Sol. Given: $V_{in_1} = 0.025$ V peak to peak, $V_{o_3} = 15$ V peak to peak, $A_{v1} = 5$ and $A_{v2} = 7.5$

(a) The overall voltage gain is $A_v = \dfrac{V_{o_3}}{V_{in_1}} = \dfrac{15}{0.025} = 600$

(b) The overall voltage gain is $A_v = A_{v1} \times A_{v2} \times A_{v3} = 5 \times 7.5 \times \times A_{v3} = 600$

The gain of third stage amplifier is $A_{v3} = \dfrac{600}{5 \times 7.5} = 16$

(c) The output voltage of first-stage amplifier is equal to the input voltage of second-stage amplifier. Then $V_{in_2} = V_{o_1} = A_{v1} \times V_{in_1} = 5 \times 0.025 \text{ V} = 0.125 \text{ V}$

3.13 COUPLING SCHEMES USED IN BJT AMPLIFIERS

Whenever amplifiers are connected in cascade, it is required to use a coupling network between the output of the amplifier and the input of the next-stage amplifier. This type of coupling is known as *inter-stage coupling*. And it is used for the following purposes:

1. It can transfer the ac output of one stage to the input of the next stage.
2. It can isolate the dc operation conditions of one stage to next stage
3. It is required to prevent the shifting of *Q* points

Usually, four different types of coupling schemes are commonly used in multistage or cascaded amplifiers as given below:

1. Resistance Capacitance (*RC*) coupling
2. Transformer coupling
3. Impedance coupling
4. Direct coupling

3.13.1 Resistance Capacitance (*RC*) Coupling

This coupling scheme is the most commonly used as it has satisfactory frequency response and is less expensive. In this method, the signal developed across the collector resistance of each stage is coupled through capacitor *C* into the base of the next stage. Figure 3.81 shows a two-stage *RC* coupled cascaded amplifier. This circuit consists of two single-stage common-emitter transistor amplifiers. The coupling network is formed through R_C, *C* and R_B as shown in Fig. 3.81. The cascaded amplifier stages can amplify the input signal and the overall gain of the amplifier is the product of individual stage gains.

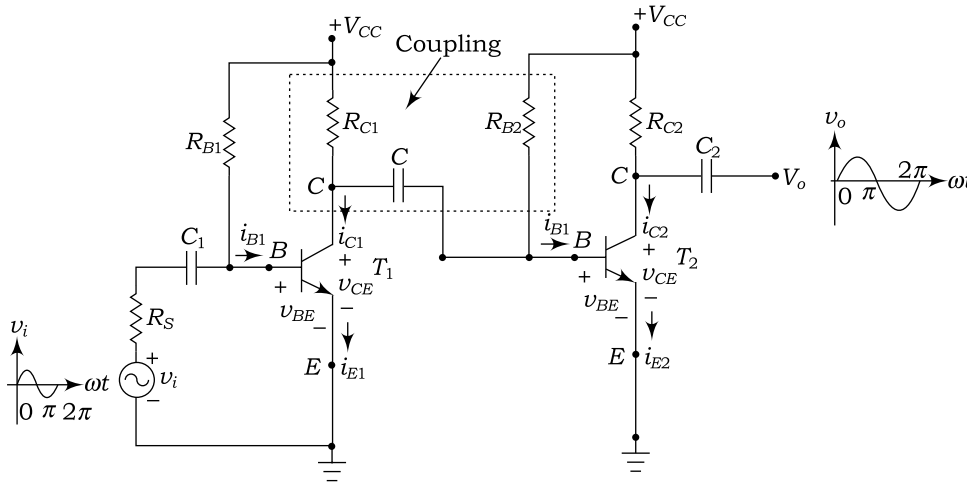


Fig. 3.81 Resistance capacitance coupling

3.13.2 Impedance Coupling

When the collector resistance R_C of Fig. 3.81 is replaced by an inductor (L), we obtain impedance coupling amplifier as depicted in Fig. 3.82. If the frequency increases, the value of inductive reactance moves towards infinity and each inductor appears as open circuit. Therefore, inductors can pass dc signals but block ac signals.

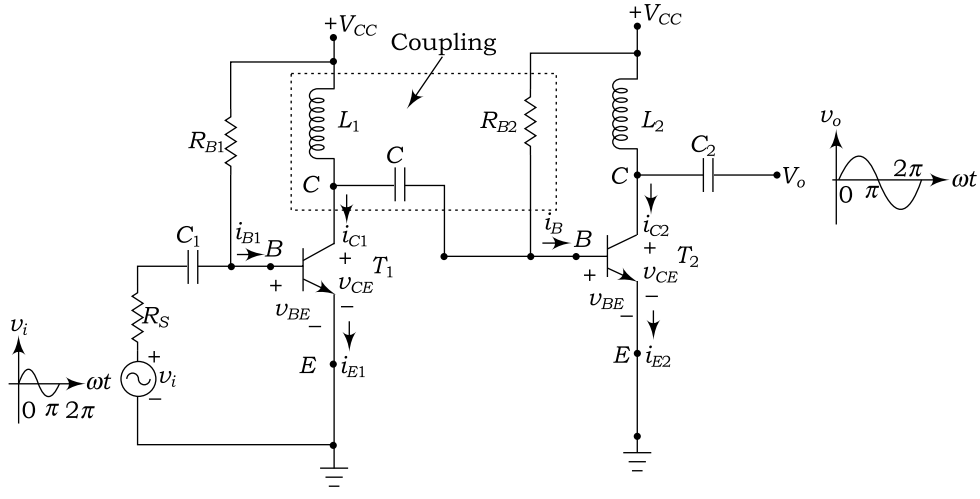


Fig. 3.82 Impedance coupling

3.13.3 Transformer Coupling

Figure 3.83 shows the transfer-coupling amplifier circuit. In this scheme, the primary winding of the transformer is used as a collector load and the secondary winding of transformer transmits the ac output voltage signal directly to the base of the next-stage amplifier. In this coupling, there is no requirement of coupling capacitors.

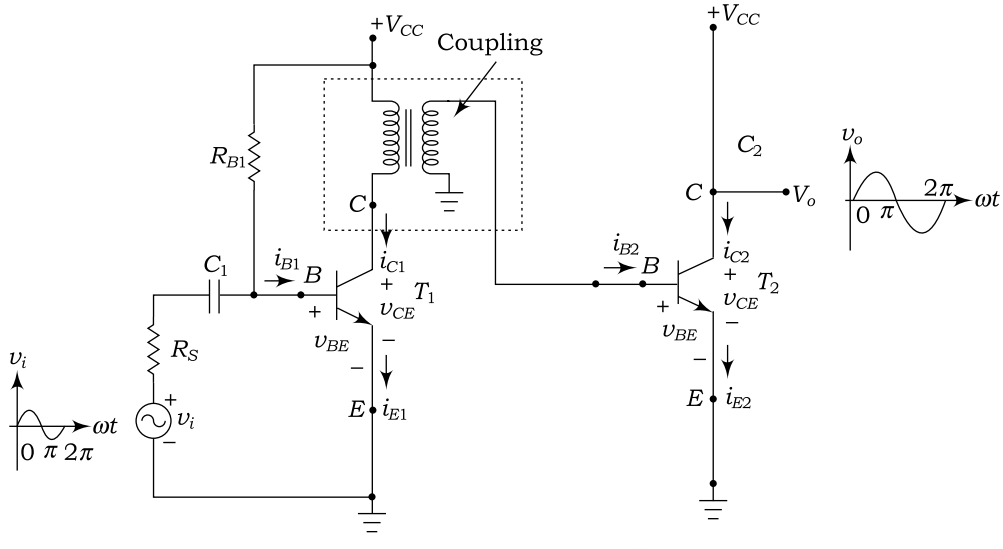


Fig. 3.83 Transformer coupling

3.13.4 Direct Coupling

The direct coupling scheme is given in Fig. 3.84. In this coupling, the ac output voltage signal can be fed directly to the next stage. This type of coupling amplifiers are used in low-frequency range. In this scheme, the coupling devices such as capacitors, inductors and transformers are not used due to low-frequency operation.

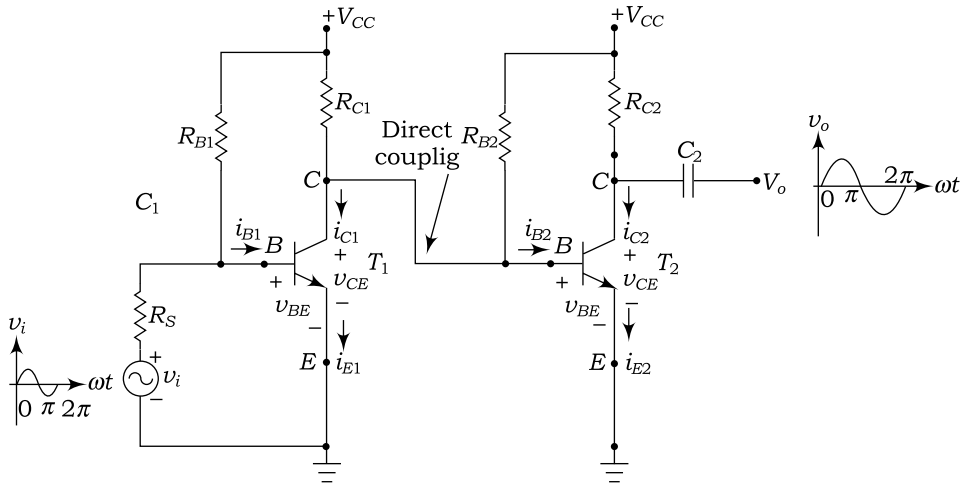


Fig. 3.84 Direct coupling

3.14 ANALYSIS OF RESISTANCE CAPACITANCE (*RC*) COUPLED AMPLIFIER

Figure 3.85 shows a two-stage *RC* coupled amplifier. This circuit consists of two single-stage common-emitter (*CE*) transistor amplifiers. The transistors T_1 and T_2 are identical and a common power supply is used. *R*esistances R_1, R_2, and R_E are used to provide proper bias. The capacitor C_1 is used to feed the ac input voltage signal to the base of the transistor T_1. The capacitor C_2 is used to couple the ac output voltage signal from transistor T_2 to load R_L. The capacitor C_E is connected across R_E of T_1 and T_2 to bypass the emitter to ground. The voltage gain of each stage will be lost without the above capacitors. The bypass capacitor is also used to prevent loss of amplification due to negative feedback.

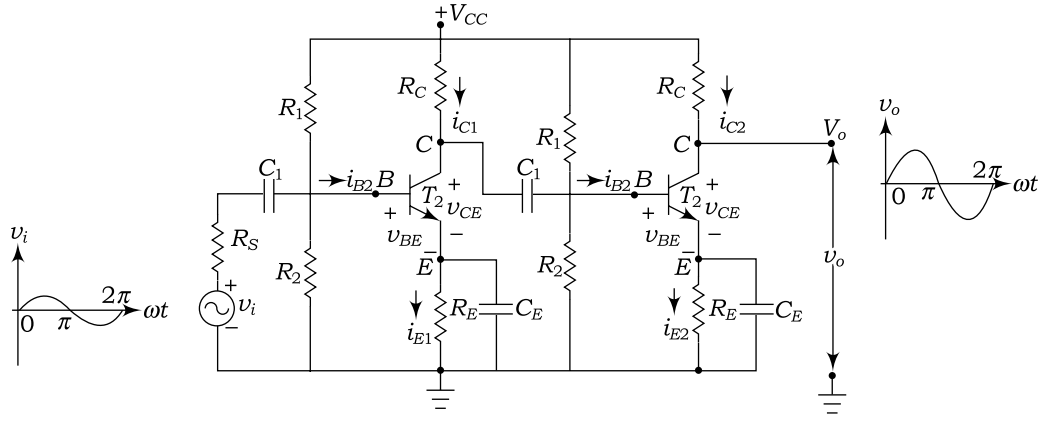


Fig. 3.85 Resistance capacitance coupled amplifier

When an ac input voltage is applied to the base of the first stage, it is amplified by transistor T_1 and ac output voltage will be obtained from the voltage across R_C. Then this output signal is fed to the input of second stage through a coupling capacitor C and the signal is further amplified by T_2. In this way, a multistage amplifier amplifies the ac input signal and the overall gain of amplifier is the product of each individual-stage amplifier. The capacitor C serves as the blocking capacitor and it blocks the dc components of the output voltage of first stage from reaching the input of the second stage and allows the passage of only ac components.

In the first stage of amplification, the amplified output voltage at collector terminal of T_1 has 180° phase shift from input voltage. Similarly, in the second stage of amplification, the amplified output voltage at collector terminal of T_2 has 180° phase shift from second stage input voltage. Hence, the output voltage signal is the twice amplified replica of the input voltage signal. Consequently, the output voltage of a two-stage amplifier has zero phase shifts from input signal and is always in phase with the input signal.

The high-frequency π-model representation of transistor T_1 is shown in Fig. 3.86 where the stray capacitance due to wiring and proximity components to chassis C_{S1} and C_{S2} are present in the circuit. $R_B = R_1 \parallel R_2$ is the biasing resistance of any specified stage.

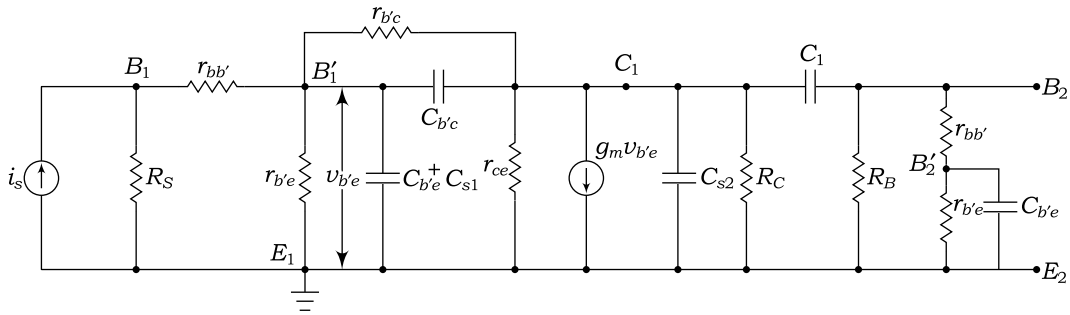


Fig. 3.86 Small-signal equivalent circuit of RC coupled amplifier

The circuit as shown in Fig. 3.87 can be modified by Miller's theorem. The resistance $r_{b'c}$ and capacitance $C_{b'c}$ are connected in parallel and can be represented by corresponding elements in the input circuit $\left[\frac{r_{b'c}}{1-A} \text{ and } C_{b'c}(1-A)\right]$ and output circuit $\left[r_{b'c}\left(\frac{A}{A-1}\right) \text{ and } \frac{C_{b'c}(A-1)}{A}\right]$. The modified equivalent circuit of Fig. 3.86 is shown in Fig. 3.87.

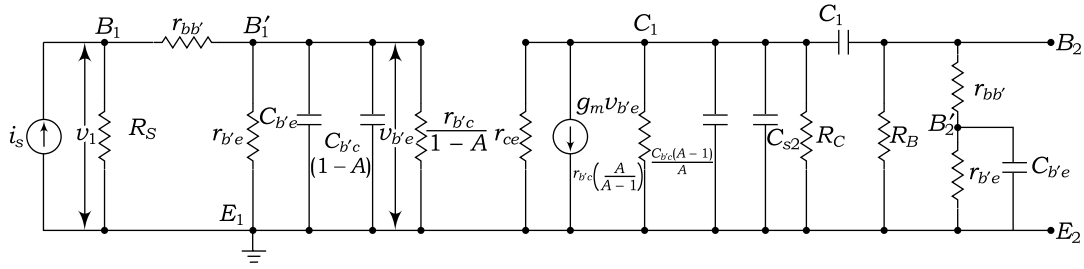


Fig. 3.87 Modified small-signal equivalent circuit of *RC* coupled amplifier using Miller's theorem

Usually, the time constant of the output shunt circuit is negligible compared to that of input circuit and the value of capacitances $\frac{C_{b'c}(A-1)}{A}$, $C_{b'c}$ and C_{S2} can be omitted from the output circuit.

As gain is $A = \frac{V_{ce}}{V_{b'e}}$ and $A >> 1$, $r_{b'c}\frac{A}{A-1} \approx r_{b'c}$.

Since $r_{b'c} >> r_{ce}, r_{b'c}\left(\frac{A}{A-1}\right) || r_{ce} \approx r_{ce}$.

Therefore, resistance $r_{b'c}\left(\frac{A}{A-1}\right)$ can be omitted from output circuit.

Assume that $r_{bb'}$ and $r_{b'e}$will be combined to $R_i = h_{ie} = r_{bb'} + r_{b'e}$. As r_{ce} is connected in parallel with much smaller resistance R_C, r_{ce} may be replaced by $\frac{1}{h_{oe}} = R_o$.

In the input circuit, C is the equivalent capacitance of $C_{b'e}$, C_{S1} and $C_{b'c}(1 - A)$.

As $\frac{r_{b'c}}{1-A} >> r_{b'e}, \frac{r_{b'c}}{1-A} || r_{b'e} = r_{b'e}$.

So $\frac{r_{b'c}}{1-A}$ can be omitted from the input circuit.

Based on the above assumptions, the simplified equivalent circuit of Fig. 3.87 is developed as depicted in Fig. 3.88.

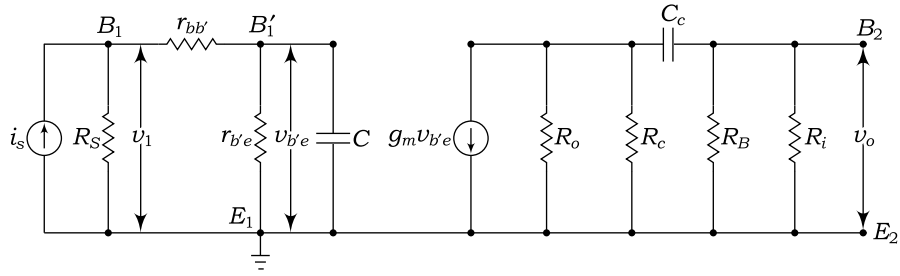


Fig. 3.88 Simplified small-signal equivalent circuit of *RC* coupled amplifier

Then in the output circuit, the parallel combination of R_o and R_C is represented by resistance $R_{C'}$.
Therefore, $R_{C'} = R_o || R_C$.
Since $R_o >> R_C$, $R_{C'} = R_o || R_C \approx R_C$
The resistance $R_{i'}$ is parallel combination of R_i and R_B.
Therefore, $R_{i'} = R_i || R_B$
As $R_i >> R_B$, $R_{i'} = R_i || R_B \approx R_i$.
Subsequently, the small-signal equivalent circuit of *RC* coupled amplifier can be represented by Fig. 3.89.

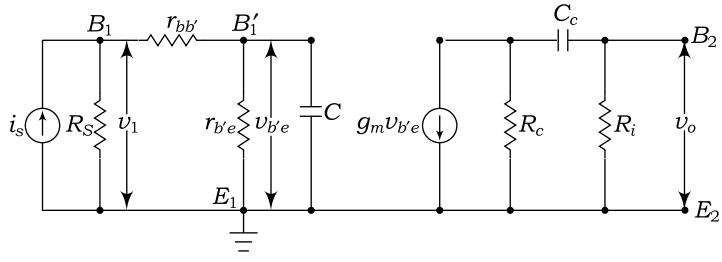


Fig. 3.89 Most simplified small-signal equivalent circuit of *RC* coupled amplifier

The analysis of *RC* coupled amplifier in three different frequency ranges such as mid-frequency range, high-frequency range and low-frequency range has been explained in this section.

3.14.1 Analysis in Mid-Frequency Range

In the mid-frequency range, the reactance of bypass capacitor (C_C) is $X_{C_C} = \frac{1}{\omega C_C} = \frac{1}{2\pi f C_C}$. Since X_{C_C} is very small in mid-frequency range, the bypass capacitor C_C can be omitted from output circuit. As the frequency is small enough to provide very large shunt capacitor reactance, $\left(X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C} \to \infty \right)$, the shunt capacitor C will be open circuit. After removing the C_C and C, we obtain the small signal equivalent circuit of *RC* coupled amplifier in mid-frequency range as shown in Fig. 3.90.

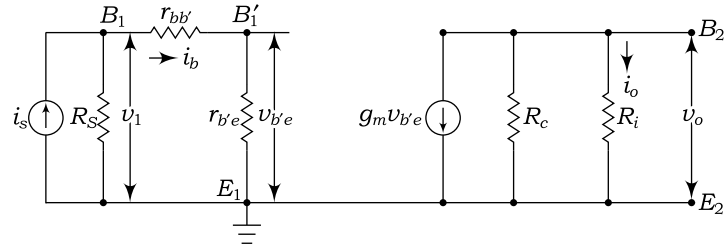


Fig. 3.90 Small-signal equivalent circuit of *RC* coupled amplifier in mid-frequency range

The voltage $v_{b'e} = i_b r_{b'e}$ (3.111)

The output current is $i_o = -g_m v_{b'e} \frac{R_C}{R_C + R_i}$ (3.112)

The mid-frequency current gain is

$$A_{\text{Im}} = \frac{i_o}{i_b} = -\frac{g_m v_{b'e}}{i_b} \frac{R_C}{R_C + R_i} \quad \text{as } v_{b'e} = i_b r_{b'e}$$

$$= -\frac{g_m i_b r_{b'e}}{i_b} \frac{R_C}{R_C + R_i} = -g_m r_{b'e} \frac{R_C}{R_C + R_i} \quad \text{as } v_{b'e} = i_b r_{b'e}$$

$$= -h_{fe} \frac{R_C}{R_C + R_i} \quad \text{as } h_{fe} = g_m r_{b'e} \tag{3.113}$$

It is clear from above equation that the mid-frequency current gain is independent of frequency.

The output voltage is equal to

$$v_o = i_o R_i = -g_m v_{b'e} \frac{R_C R_i}{R_C + R_i} = -g_m v_{b'e} R_{Ci} \quad \text{as } R_{Ci} = \frac{R_C R_i}{R_C + R_i} = R_C \| R_i \tag{3.114}$$

The input voltage is

$$v_i = i_b r_{bb'} + i_b r_{b'e} = i_b (r_{bb'} + r_{b'e}) = i_b h_{ie} \quad \text{as } h_{ie} = (r_{bb'} + r_{b'e}) \tag{3.115}$$

The mid-frequency voltage gain is

$$A_{Vm} = \frac{v_o}{v_i} = -\frac{g_m v_{b'e} R_{Ci}}{i_b h_{ie}}$$

$$= -\frac{g_m i_b r_{b'e} R_{Ci}}{i_b h_{ie}} = -\frac{g_m r_{b'e} R_{Ci}}{h_{ie}} \quad \text{as } v_{b'e} = i_b r_{b'e} \tag{3.116}$$

Since $g_m r_{b'e} = h_{fe}$, voltage gain is $A_{Vm} = -\dfrac{g_m r_{b'e} R_{Ci}}{h_{ie}} = -\dfrac{h_{fe} R_{Ci}}{h_{ie}}$ (3.117)

It is also clear from above equation that the mid-frequency voltage gain is independent of frequency.

3.14.2 Analysis in Low-frequency Range

In the low-frequency range, the shunt capacitor C provides extremely large reactance and $X_C = \dfrac{1}{\omega C} = \dfrac{1}{2\pi f} \to \infty$. Hence, the shunt capacitor C will be open circuit.

Then $X_C \parallel r_{b'e} \approx r_{b'e}$.

The reactance of bypass capacitor (C_C) is $X_{C_C} = \dfrac{1}{\omega C_C} = \dfrac{1}{2\pi f C_C}$ and it cannot be neglected. Therefore, capacitance C_C must be present in the output circuit. After removing C, we get the small signal equivalent circuit of RC coupled amplifier in low-frequency range as shown in Fig. 3.91.

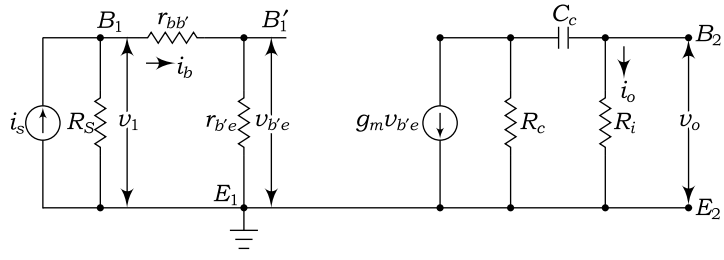


Fig. 3.91 Small-signal equivalent circuit of *RC* coupled amplifier in mid-frequency range

The voltage $v_{b'e} = i_b r_{b'e}$ (3.118)

The output current is

$$i_o = -g_m v_{b'e} \frac{R_C}{R_C + (R_i - jX_{C_C})} = -g_m v_{b'e} \frac{R_C}{R_C + R_i + \dfrac{1}{j\omega C_C}} \quad \text{as } X_{C_C} = \frac{1}{\omega C_C}$$

$$= -g_m i_b r_{b'e} \frac{R_C}{R_C + R_i + \dfrac{1}{j\omega C_C}} \quad \text{as } v_{b'e} = i_b r_{b'e} \tag{3.119}$$

The low-frequency current gain is

$$A_{Il} = \frac{i_o}{i_b} = -\frac{g_m i_b r_{b'e}}{i_b} \frac{R_C}{R_C + R_i + \dfrac{1}{j\omega C_C}} = -g_m r_{b'e} \frac{R_C}{R_C + R_i + \dfrac{1}{j\omega C_C}}$$

$$= -h_{fe} \frac{R_C}{R_C + R_i + \dfrac{1}{j\omega C_C}} \quad \text{as } h_{fe} = g_m r_{b'e} \tag{3.120}$$

The current gain can also be expressed as

$$A_{Il} = -\frac{h_{fe}R_C}{R_C + R_i}\frac{R_C + R_i}{R_C + R_i + \dfrac{1}{j\omega C_C}}$$

$$= A_{\text{Im}}\frac{R_C + R_i}{R_C + R_i + \dfrac{1}{j\omega C_C}} \quad \text{as } A_{\text{Im}} = -\frac{h_{fe}R_C}{R_C + R_i}$$

$$= A_{\text{Im}}\frac{R_C + R_i}{(R_C + R_i)\left[1 + \dfrac{1}{j\omega C_C(R_C + R_i)}\right]} = A_{\text{Im}}\frac{1}{\left[1 + \dfrac{1}{j\omega C_C(R_C + R_i)}\right]}$$

$$= \frac{A_{\text{Im}}}{\left[1 - j\dfrac{1}{2\pi f C_C(R_C + R_i)}\right]} = -\frac{A_{\text{Im}}}{\left[1 - j\dfrac{f_L}{f}\right]} \quad \text{as } f_L = \frac{1}{2\pi C_C(R_C + R_i)} \tag{3.121}$$

Then low-frequency current gain can be represented by

$$A_{Il} = |A_{Il}|\angle\phi_{Il} \quad \text{where, } |A_{Il}| = \frac{|A_{\text{Im}}|}{\left[1 + \left(\dfrac{f_L}{f}\right)^2\right]^{\frac{1}{2}}} \text{ and} \tag{3.122}$$

the phase angle is $\phi_{Il} = \text{Phase angle of } A_{\text{Im}} + \tan^{-1}\left(\dfrac{f_L}{f}\right)$

$$= 180° + \tan^{-1}\left(\frac{f_L}{f}\right) = 180° + \tan^{-1}\left(\frac{1}{2\pi f C_C(R_C + R_i)}\right) \tag{3.123}$$

When $f = f_L, |A_{Il}| = \dfrac{|A_{\text{Im}}|}{\sqrt{2}} = 0.707|A_{\text{Im}}|$

Therefore, at $f = f_L$, the low-frequency current gain is 3 dB lower from the current gain of mid-frequency gain.

The output voltage is equal to

$$v_o = i_o R_i = -g_m i_b r_{b'e}\frac{R_C R_i}{R_C + R_i + \dfrac{1}{j\omega C_C}} \tag{3.124}$$

The input voltage is

$$v_i = i_b r_{bb'} + i_b r_{b'e} = i_b(r_{bb'} + r_{b'e}) = i_b h_{ie} \quad \text{as } h_{ie} = (r_{bb'} + r_{b'e}) \tag{3.125}$$

The low-frequency voltage gain is

$$A_{Vl} = \frac{v_o}{v_i} = -\frac{g_m i_b r_{b'e}}{i_b h_{ie}}\frac{R_C R_i}{R_C + R_i + \dfrac{1}{j\omega C_C}} = -\frac{g_m r_{b'e}}{h_{ie}}\frac{R_C R_i}{R_C + R_i + \dfrac{1}{j\omega C_C}}$$

$$= -\frac{h_{fe}}{h_{ie}}\frac{R_C R_i}{R_C + R_i + \dfrac{1}{j\omega C_C}} \quad \text{as } g_m r_{b'e} = h_{fe} \tag{3.126}$$

The voltage gain can also be expressed as

$$A_{Vl} = -\frac{h_{fe}}{h_{ie}} \frac{R_C R_i}{R_C + R_i + \dfrac{1}{j\omega C_C}} = -\frac{h_{fe}}{h_{ie}} \frac{R_C R_i}{(R_C + R_i)\left[1 + \dfrac{1}{j\omega C_C (R_C + R_i)}\right]}$$

$$= -\frac{h_{fe}}{h_{ie}} \frac{R_{Ci}}{\left[1 + \dfrac{1}{j\omega C_C (R_C + R_i)}\right]} \quad \text{as } R_{Ci} = R_C \| R_i = \frac{R_C R_i}{R_C + R_i}$$

$$= -\frac{h_{fe}}{h_{ie}} R_{Ci} \frac{1}{\left[1 + \dfrac{1}{j\omega C_C (R_C + R_i)}\right]}$$

$$= \frac{A_{Vm}}{\left[1 + \dfrac{1}{j\omega C_C (R_C + R_i)}\right]} \quad \text{as } A_{Vm} = -\frac{h_{fe} R_{Ci}}{h_{ie}}$$

$$= \frac{A_{Vm}}{\left[1 - j\dfrac{1}{2\pi f C_C (R_C + R_i)}\right]} = \frac{A_{Vm}}{\left[1 - j\dfrac{f_L}{f}\right]} \quad \text{where, } f_L = \frac{1}{2\pi C_C (R_C + R_i)} \tag{3.127}$$

Then low-frequency voltage gain can be represented by

$$A_{Vl} = |A_{Vl}| \angle \phi_{Vl} \quad \text{where, } |A_{Vl}| = \frac{|A_{Vm}|}{\left[1 + \left(\dfrac{f_L}{f}\right)^2\right]^{\frac{1}{2}}} \text{ and} \tag{3.128}$$

the phase angle is $\phi_{Vl} = \text{Phase angle of } A_{Vm} + \tan^{-1}\left(\dfrac{f_L}{f}\right)$

$$= 180° + \tan^{-1}\left(\frac{f_L}{f}\right) = 180° + \tan^{-1}\left(\frac{1}{2\pi f C_C (R_C + R_i)}\right) \tag{3.129}$$

When $f = f_L, |A_{Vl}| = \dfrac{|A_{Vm}|}{\sqrt{2}} = 0.707 |A_{Vm}|$. Therefore at $f = f_L$, the low-frequency voltage gain is 3 dB lower from the voltage gain of mid-frequency gain.

It is also clear from the above discussion for current gain as well as voltage gain, the lower 3 dB frequencies are same and $f_L = \dfrac{1}{2\pi C_C (R_C + R_i)}$.

3.14.3 Analysis in High-frequency Range

In the high-frequency range, the reactance of coupling capacitor (C_C) is $X_{C_C} = \dfrac{1}{\omega C_C} = \dfrac{1}{2\pi f C_C}$. As X_{C_C} is very small, the coupling capacitor C_C can be omitted from the output circuit. At high frequency, the shunt

capacitor C provides a reactance, i.e., $X_C = \frac{1}{\omega C} = \frac{1}{2\pi f}$ and its value cannot be neglected. Hence, the shunt capacitor C must be present in the equivalent circuit. After removing the C_C, we get the small-signal equivalent circuit of an RC coupled amplifier in the high-frequency range as shown in Fig. 3.92.

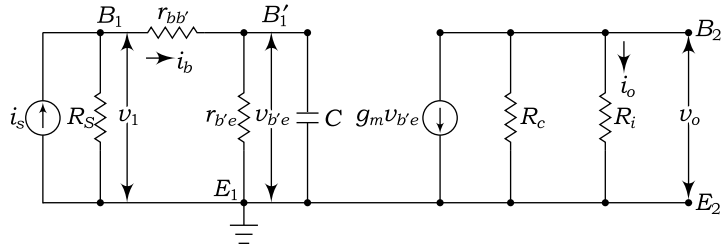


Fig. 3.92 Small signal equivalent circuit of *RC* coupled amplifier in high-frequency range

The base current
$$i_b = v_{b'e}\left(\frac{1}{r_{b'e}} + j\omega C\right) = v_{b'e}\frac{1 + j\omega C r_{b'e}}{r_{b'e}} \tag{3.130}$$

The voltage
$$v_{b'e} = \frac{i_b r_{b'e}}{1 + j\omega C r_{b'e}} \tag{3.131}$$

The output current is

$$\begin{aligned} i_o &= -g_m v_{b'e}\frac{R_C}{R_C + R_i} = -g_m \frac{i_b r_{b'e}}{1 + j\omega C r_{b'e}}\frac{R_C}{R_C + R_i} \\ &= -\frac{g_m r_{b'e} i_b}{1 + j\omega C r_{b'e}}\frac{R_C}{R_C + R_i} = -\frac{h_{fe} i_b}{1 + j\omega C r_{b'e}}\frac{R_C}{R_C + R_i} \quad \text{as } g_m r_{b'e} = h_{fe} \end{aligned} \tag{3.132}$$

The high-frequency current gain is

$$\begin{aligned} A_{Ih} &= \frac{i_o}{i_b} = -\frac{h_{fe} i_b}{i_b(1 + j\omega C r_{b'e})}\frac{R_C}{R_C + R_i} = -\frac{h_{fe}}{(1 + j\omega C r_{b'e})}\frac{R_C}{R_C + R_i} \\ &= -h_{fe}\frac{R_C}{R_C + R_i}\frac{1}{(1 + j\omega C r_{b'e})} \\ &= \frac{A_{\text{Im}}}{(1 + j\omega C r_{b'e})} \quad \text{as } A_{\text{Im}} = -h_{fe}\frac{R_C}{R_C + R_i} \\ &= \frac{A_{\text{Im}}}{(1 + j2\pi f C r_{b'e})} = \frac{A_{\text{Im}}}{\left[1 + j\frac{f}{f_H}\right]} \quad \text{as } f_H = \frac{1}{2\pi C_C r_{b'e}} \end{aligned} \tag{3.133}$$

Then high-frequency current gain can be represented by

$$A_{Ih} = |A_{Ih}| \angle \phi_{Ih} \quad \text{where, } |A_{Ih}| = \frac{|A_{\text{Im}}|}{\left[1 + \left(\frac{f}{f_H}\right)^2\right]^{\frac{1}{2}}} \text{ and} \tag{3.134}$$

the phase angle is ϕ_{Ih} = phase angle of $A_{\text{Im}} - \tan^{-1}\left(\frac{f}{f_H}\right)$

$$= 180° - \tan^{-1}\left(\frac{f}{f_H}\right) = 180° - \tan^{-1}(2\pi f C r_{b'e}) \tag{3.135}$$

At $f = f_H$, $|A_{Ih}| = \frac{|A_{\text{Im}}|}{\sqrt{2}} = 0.707\,|A_{\text{Im}}|$

Therefore, at $f = f_H$, the high-frequency current gain is 3 dB lower from the current gain of mid-frequency gain.

The output voltage is equal to

$$v_o = i_o R_i = -g_m v_{b'e} \frac{R_C R_i}{R_C + R_i} = -g_m v_{b'e} R_{Ci} \quad \text{as } R_{Ci} = \frac{R_C R_i}{R_C + R_i} = R_C \| R_i$$

$$= -g_m \frac{i_b r_{b'e}}{1 + j\omega C r_{b'e}} R_{Ci} \quad \text{as } v_{b'e} = \frac{i_b r_{b'e}}{1 + j\omega C r_{b'e}} \tag{3.136}$$

Assume that input voltage is $v_i = i_b r_{bb'} + i_b r_{b'e} = i_b(r_{bb'} + r_{b'e}) = i_b h_{ie}$ as $h_{ie} = (r_{bb'} + r_{b'e})$

The high-frequency voltage gain is

$$A_{Vh} = \frac{v_o}{v_i} = -\frac{g_m}{i_b h_{ie}} \frac{i_b r_{b'e}}{1 + j\omega C r_{b'e}} R_{Ci} = -\frac{g_m r_{b'e}}{h_{ie}} \frac{1}{1 + j\omega C r_{b'e}} R_{Ci}$$

$$= -\frac{h_{fe} R_{Ci}}{h_{ie}} \frac{1}{1 + j\omega C r_{b'e}} \quad \text{as } g_m r_{b'e} = h_{fe}$$

$$= \frac{A_{Vm}}{1 + j\omega C r_{b'e}} \quad \text{where, } A_{Vm} = -\frac{g_m r_{b'e} R_{Ci}}{h_{ie}} = -\frac{h_{fe} R_{Ci}}{h_{ie}}$$

$$= \frac{A_{Vm}}{1 + j2\pi f C r_{b'e}} = \frac{A_{Vm}}{\left[1 + j\frac{f}{f_H}\right]} \quad \text{as } f_H = \frac{1}{2\pi C_C r_{b'e}} \tag{3.137}$$

Then high-frequency voltage gain can be represented by

$$A_{Vh} = |A_{Vh}| \angle \phi_{Vh} \quad \text{where, } |A_{Vh}| = \frac{|A_{Vm}|}{\left[1 + \left(\frac{f}{f_H}\right)^2\right]^{\frac{1}{2}}} \text{ and} \tag{3.138}$$

the phase angle is ϕ_{Vh} = Phase angle of $A_{Vm} - \tan^{-1}\left(\frac{f}{f_H}\right)$

$$= 180° - \tan^{-1}\left(\frac{f}{f_H}\right) = 180° - \tan^{-1}(2\pi f C r_{b'e}) \tag{3.139}$$

At $$f = f_H,\ |A_{Vh}| = \frac{|A_{Vm}|}{\sqrt{2}} = 0.707 |A_{Vm}| \tag{3.140}$$

Therefore, at $f = f_H$, the high-frequency voltage gain is 3 dB lower from the voltage gain of mid-frequency gain.

3.14.4 Frequency Response of an *RC* Coupled Amplifier

The frequency response of an *RC* coupled amplifier is depicted in Fig. 3.93. it is clear from frequency response that the voltage gain drops at low frequency (below 50 Hz) and at high frequency (above 20 kHz) but, it is constant in the mid-frequency range. The bandwidth is $f_2 - f_1 = f_H - f_L$.

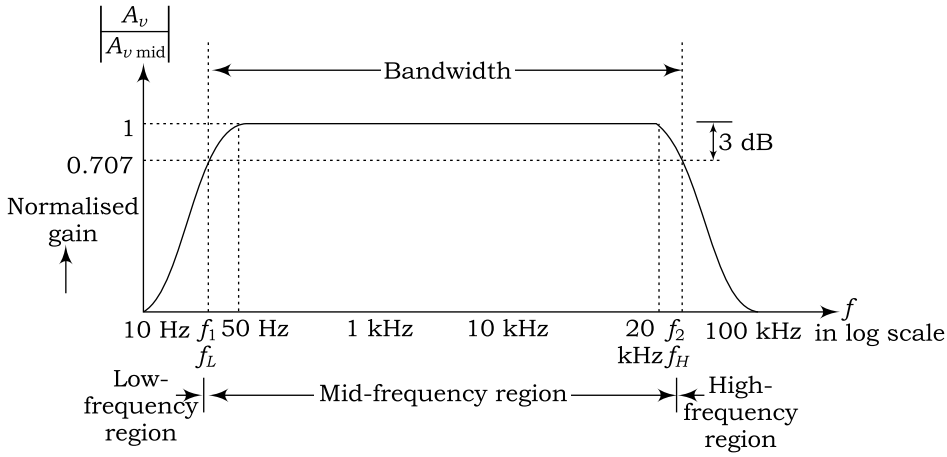


Fig. 3.93 Frequency response of a typical *RC* coupled amplifier

3.14.5 Advantages of an *RC* Coupled Amplifier

The *RC* coupled amplifier has the following advantages:

1. This amplifier requires components such as resistances and capacitors which are least expensive, easily available, and small in size.
2. This amplifier provides uniform voltage amplification over a wide frequency range from few Hz to few kHz as resistance values are independent of frequency.
3. This amplifier has minimum possible nonlinear distortion as no coil or transformer is used in this amplifier.
4. The overall amplification factor of an *RC* coupled amplifier is higher than that of other amplifiers.

3.14.6 Disadvantages of an *RC* Coupled Amplifier

The *RC* coupled amplifier has the following disadvantages:

1. This amplifier gets noisy with duration of usage especially in humid weather.
2. This amplifier provides poor impedance matching as the output impedance of the *RC* coupled amplifier is several hundred ohms but the impedance of the speaker is only few ohms. Therefore, less power is transferred to the speaker.

3.14.7 Applications of an *RC* an Coupled Amplifier

The *RC* coupled amplifier has the following applications:

1. Since an *RC* coupled amplifier has very good frequency response from few Hz to few kHz, it is extensively used as a voltage amplifier in initial stages of public address systems.
2. This amplifier cannot be used as a final amplifier as it has poor impedance-matching characteristics.

3.15 IMPEDANCE-COUPLED AMPLIFIER

Figure 3.94 shows a two-stage impedance-coupled amplifier. This circuit has two single-stage common-emitter amplifiers. If the collector resistance *RC* of Fig. 3.94 is replaced by an inductor (*L*), we get an impedance-coupling amplifier. The functions of C_1, C_2, and *C* are same as *RC* coupled amplifier.

The individual stage gain and the overall voltage gain can be derived in the same way as obtained for an *RC* coupled amplifier. The one change in the expression is that *RC* has to be replaced by inductive reactance ($X_L = \omega L$).

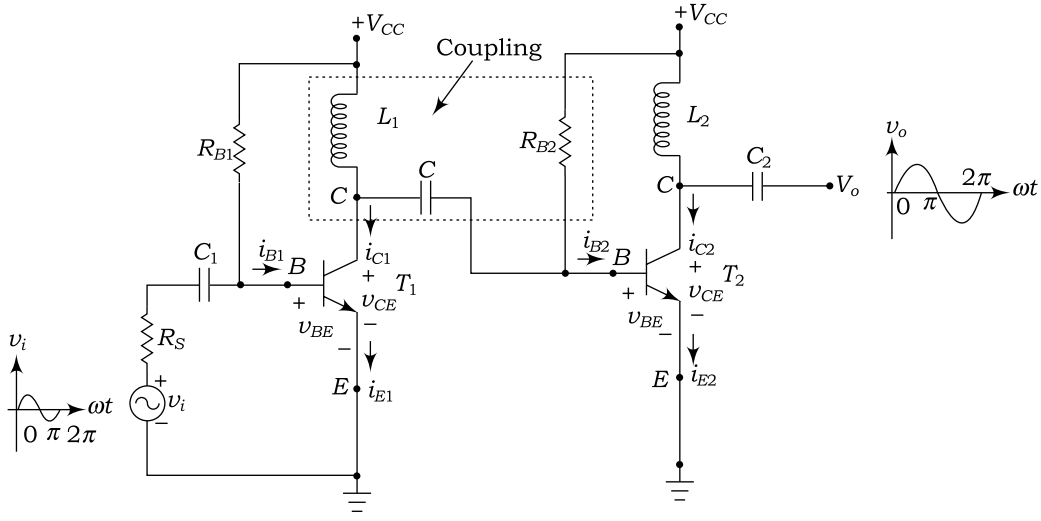


Fig. 3.94 Impedance coupling

The advantage of an impedance coupled amplifier is that it is able to operate at low collector supply voltage as the voltage drop across the inductor (*L*) is very small.

The disadvantage of an impedance coupled amplifier is that it is comparatively expensive due to use of inductors. At low frequency, voltage drop across inductance is very small. An impedance-coupled amplifier is used only at radio frequency which is above 20 kH.

3.16 TRANSFORMER-COUPLED AMPLIFIER

Figure 3.95 shows the two-stage transformer-coupled amplifier circuit. This circuit consists of two single-stage common-emitter transistor amplifiers. In this amplifier, the primary winding of the transformer TRA_1 is used as a collector load and the secondary winding is used to transmit the ac output voltage of the first-stage amplifier directly to the base of the second-stage amplifier. The transformer TRA_2 couples the output signal to the load *RL*. C_E is used as the emitter bypass capacitor.

When an ac input signal is applied to the base of the transistor T_1, the amplified output signal appears across the primary winding of the transformer TRA_1. Then, the primary winding voltage of TRA_1 is transferred to the input of the next stage by the secondary winding of the transformer TRA_1. The second-stage amplifier then continues the process in the same way.

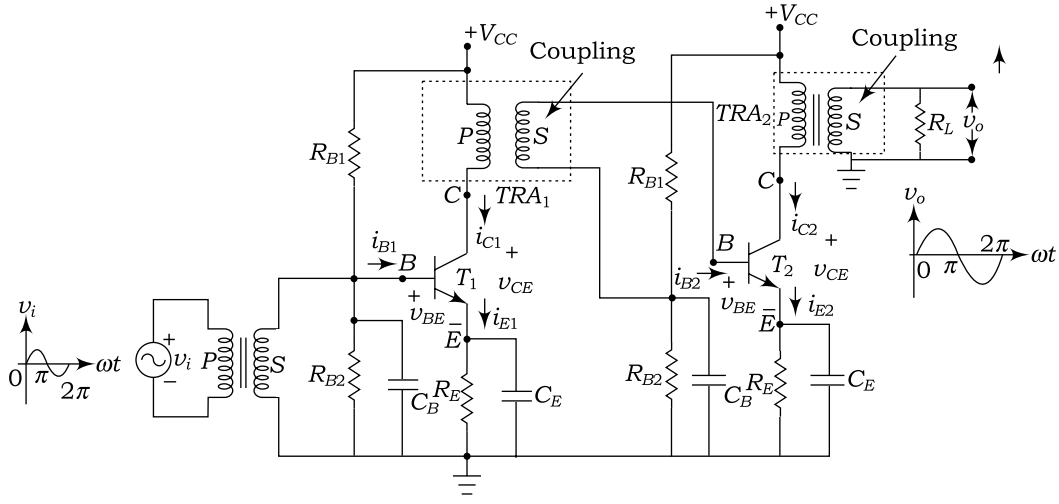


Fig. 3.95 Two-stage transformer-coupled common-emitter amplifier circuit

In practical circuits, a bypass capacitor is used at the bottom of each primary winding of transformers to provide ac ground. These keep away from the load inductance of the connecting line that returns to the dc supply ground. Similarly, a bypass capacitor is also used at the bottom of each secondary winding to provide ac ground and prevents the signal power loss in the biasing resistances. The small-signal equivalent circuit of cascaded transformer-coupled common-emitter amplifier circuit is shown in Fig. 3.96.

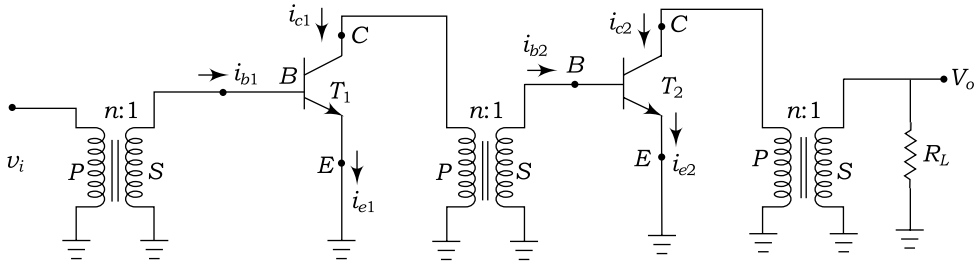


Fig. 3.96 Small-signal equivalent circuit of cascaded transformer-coupled common-emitter amplifier circuit

Assume R_L is the load resistance. For maximum power transfer, the load resistance of transistor T_2 should be equal to the output resistance of T_2 and its value is RL_2, which can be determined by taking into account the turn ratio of transformer TRA_2. The input resistance of transistor T_2 is R_{i_2} which is approximately h_{ie_2} and it can be used to determine the load across the inter-stage transformer TRA_1. When the turn ratio of TRA_1 is known, RL_1, the effective load of the transistor T_1, can be determined.

The analysis of a multistage transformer-coupled common-emitter amplifier can be done in three frequency regions such as mid-frequency range, high-frequency range and low-frequency range.

3.16.1 Analysis in Mid-frequency Range

Figure 3.97 shows the approximate equivalent circuit of transformer-coupled amplifier assuming that all capacitor reactances are negligible. The transformer turns ratio of TRA_1 reflects load impedance h_{ie_2} on the secondary.

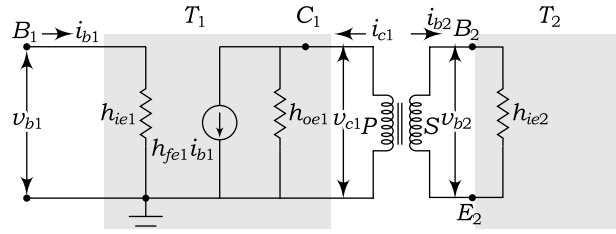


Fig. 3.97 Approximate equivalent circuit of transformer-coupled amplifier

The load impedance of the transistor T_1 is equal to $\left(\frac{N_1}{N_2}\right)^2 h_{ie_2} = n^2 h_{ie_2}$ as $\left(\frac{N_1}{N_2}\right) = n{:}1$. (3.141)

The output impedance of transistor T_1 is equal to $\frac{1}{h_{oe1}}$. According to maximum power transfer, two impedances (load impedance and output impedance) must be equal.

Therefore, $n^2 h_{ie_2} = \frac{1}{h_{oe1}}$, or $n = \frac{1}{\sqrt{h_{ie_2} h_{oe1}}}$, or $\frac{N_1}{N_2} = \frac{1}{\sqrt{h_{ie_2} h_{oe1}}}$ as $n = \frac{N_1}{N_2}$. (3.142)

Then the modified small-signal equivalent circuit of transformer-coupled amplifier (Fig. 3.97) is depicted in Fig. 3.98.

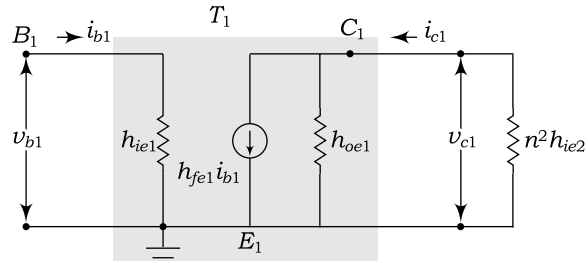


Fig. 3.98 Modified small-signal equivalent circuit of transformer-coupled amplifier

Due to impedance-matched condition, the current flows through the transformer's primary winding $i_{c_1} = \frac{h_{fe_1} i_{b_1}}{2}$.

The base current $i_{b2} = \frac{N_1}{N_2} i_{c1} = \frac{N_1}{N_2} \frac{h_{fe_1} i_{b_1}}{2} = n \frac{h_{fe_1} i_{b_1}}{2}$ as $i_{c_1} = \frac{h_{fe_1} i_{b_1}}{2}$ and $n = \frac{N_1}{N_2}$ (3.143)

The mid-frequency current gain of the transistor T_1 is $A_{\text{Im}} = \frac{i_{b2}}{i_{b1}} = \frac{n h_{fe_1} i_{b_1}}{2} \times \frac{1}{i_{b1}} = \frac{n h_{fe_1}}{2}$. (3.144)

The above expression for current gain can also be used for second-stage when load impedance R_L matches the output resistance of the transistor T_2.

The voltage $v_{c1} = -i_{c1} n^2 h_{ie_2} = -\frac{h_{fe_1} i_{b_1}}{2} n^2 h_{ie_2}$ as $i_{c_1} = \frac{h_{fe_1} i_{b_1}}{2}$.

Since $$i_{b_1} = \frac{v_{b_1}}{h_{ie_1}},\ v_{c1} = -\frac{h_{fe_1} v_{b_1}}{2h_{ie_1}} n^2 h_{ie_2} \tag{3.145}$$

Then the voltage ratio $\frac{v_{c1}}{v_{b_1}} = -\frac{h_{fe_1}}{2h_{ie_1}} n^2 h_{ie_2}$ and the voltage ratio $\frac{v_{c1}}{v_{b_2}} = -\frac{N_1}{N_2} = -n$.

The mid-frequency voltage gain is

$$A_{vm} = \frac{v_{b2}}{v_{b1}} = \frac{v_{b2}}{v_{c1}} \times \frac{v_{c1}}{v_{b1}} = \left(-\frac{1}{n}\right) \times \left(-\frac{h_{fe_1}}{2h_{ie_1}} n^2 h_{ie_2}\right)$$

$$= \frac{h_{fe_1}}{2h_{ie_1}} n h_{ie_2} = n\frac{h_{fe_1}}{2} \quad \text{as} \quad h_{ie_1} = h_{ie_2} \tag{3.146}$$

3.16.2 Analysis in Low-frequency Range

At low frequency, the primary inductance L_P will be incorporated in the small-signal equivalent circuit of a transformer-coupled amplifier. Figure 3.99 shows the equivalent circuit of a transformer-coupled amplifier in low frequency.

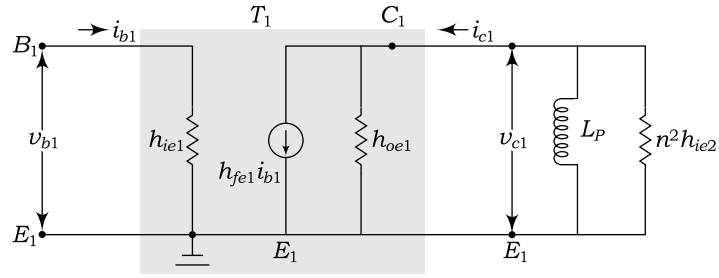


Fig. 3.99 Equivalent circuit of a transformer-coupled amplifier in low frequency

The reactance of L_P is $X_P = \omega L_P = 2\pi f L_P$.

Due to shunting effect of L_P, the effective load for the transistor T_1 will be reduced with reduction in v_{C1} and voltage gain.

R is the parallel combination of $\frac{1}{h_{oe_1}}$ and $n^2 h_{ie_2}$, and

the reactance value of L_P is equal to R at lower 3 dB frequency f_L.

Therefore, $X_P = \omega L_P = 2\pi f_L L_P = R$

where, $$R = \frac{1}{h_{oe_1}} \| n^2 h_{ie_2}$$

Then $$L_P = \frac{R}{2\pi f_L} \text{ and } f_L = \frac{R}{2\pi L_P} \tag{3.146}$$

3.16.3 Analysis in High-frequency Range

At high frequency, the shunting effect of a transformer's primary inductance L_P is negligible but the transformer leakage inductance and distribution capacitance become significant. Figure 3.100 shows the equivalent circuit of a transformer-coupled amplifier at high frequency and its simplified representation is depicted in Fig. 3.101(a).

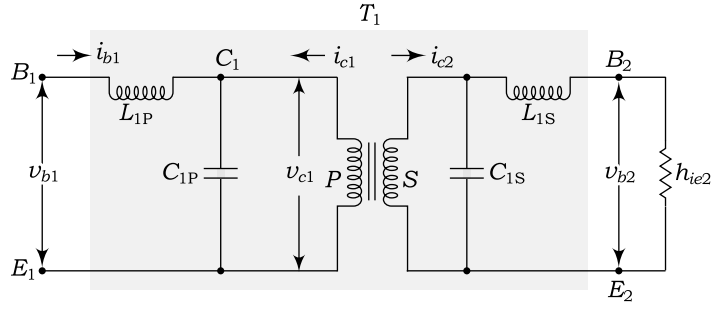


Fig. 3.100 High-frequency equivalent circuit of transformer-coupled amplifier

The equivalent inductance referred to primary is

$$L_1 = L_{1P} + L_{1S}\left(\frac{N_1}{N_2}\right)^2 = L_{1P} + n^2 L_{1S} \quad \text{as } n = \frac{N_1}{N_2}. \tag{3.147}$$

Similarly, the equivalent capacitance referred to primary is

$$C_1 = C_{1P} + C_{1S}\left(\frac{N_1}{N_2}\right)^2 = C_{1P} + n^2 C_{1S} \quad \text{as } n = \frac{N_1}{N_2}, \tag{3.148}$$

This circuit has a series resonant effect at high frequencies.

At resonant $X_{C_1} = X_{L_1}$, the resonant frequency is $f_o = \dfrac{1}{2\pi\sqrt{L_1 C_1}}$.

The upper 3 dB frequency f_H is much greater than f_o.

Figure 3.101(b) shows the frequency response of voltage gain with respect to frequency for a transformer-coupled amplifier. It is clear from this response that the voltage gain drops at low as well as high frequencies, but in mid-frequency range, the voltage gain remains constant. It is also noticeable that voltage gain increases at resonance frequency f_o, and after that voltage gain continuously decreases with increasing frequency.

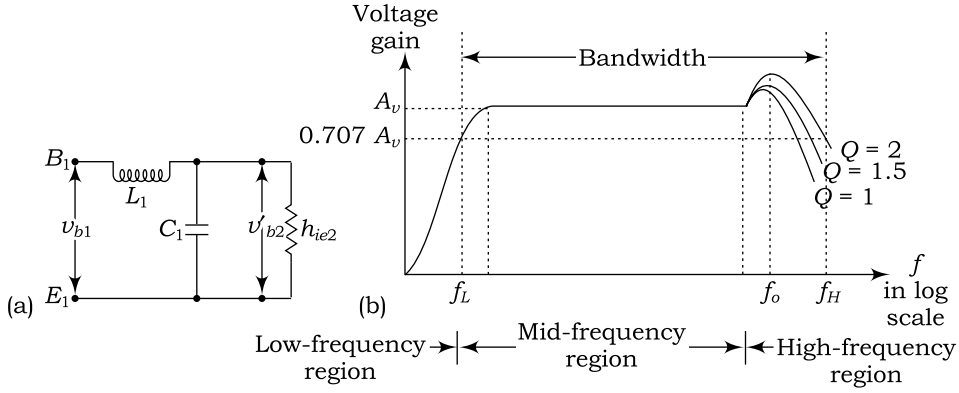


Fig. 3.101 (a) Simplified equivalent circuit of transformer-coupled amplifier (b) Frequency response of transformer-coupled amplifier

3.16.4 Advantages of a Transformer-Coupled Amplifier

The transformer-coupled amplifier has the following advantages:

1. There is no power loss of signal in the collector or base resistance due to low winding resistance of transformer.
2. This amplifier provides higher voltage gain compared to the *RC* coupled amplifier.
3. This amplifier provides very good impedance matching between two stages. This impedance matching is used for maximum power transfer in the amplifier.

3.16.5 Disadvantages of Transformer-Coupled Amplifier

The transformer-coupled amplifier has the following disadvantages:

1. When this amplifier operates in audio-frequency range, the coupling transformer is bulky in size and expensive.
2. In radio-frequency range, the winding inductance and distributed capacitance generates a reverse frequency distortion. It generates hum in the amplifier circuit.

3.16.6 Applications of a Transformer-Coupled Amplifier

The transformer-coupled amplifier has the following applications:

1. This amplifier is used as input stage.
2. It has excellent impedance matching between two intermediate stages.
3. This amplifier is commonly used to transfer power to the low impedance load like a speaker. The impedance of the speaker varies in between 4 ohms to 16 ohms, but the output resistance of the transistor amplifier is several hundred ohms. To develop proper match with the load impedance and amplifier output, a step-down transformer of required turn ratio is used. For this, the secondary winding resistance should be equal to the speaker impedance and primary winding resistance must be equal to the output resistance of the amplifier.

3.17 DIRECT-COUPLED AMPLIFIER

The two-stage direct-coupled common-emitter amplifier is shown in Fig. 3.102. In this coupling, the ac output signal of the first stage is directly fed to the base of the next-stage transistor. In this type of coupling amplifiers, there are no coupling devices such as capacitors, inductors and transformers. This amplifier is known as *dc amplifier* and it is used to amplify very low-frequency signals including dc.

During the design of dc amplifiers, the designer should ensure that dc levels of each individual stage are compatible with the next stage. For example, consider that two identical common-emitter amplifiers are connected directly, as shown in Fig. 3.102. When $V_{CC1} = 12$ V, $V_{B1} = V_{B2} = 2.2$ V, $V_{E1} = V_{E2} = 1.5$ V and $V_{C1} = V_{C2} = 5$ V, $V_{BE} = 0.7$ and $V_{CB} = 3$ V. Therefore, there is a difference of 3 V between the collector of T_1 and the base of T_2.

In ac operation, a capacitor C is connected between the collector of T_1 and base of T_2 as depicted in Fig. 3.103. The ac output signal of first stage is coupled to the second-stage amplifier and the capacitor C must be charged to 2.8 V. Subsequently, V_{C1} will remain at 5 V and V_{B2} will remain at 2.2 V.

In dc operation, the capacitor should be removed, but the collector of T_1 cannot be connected directly to the base of T_2 as the voltage V_{C1} is not equal to V_{B2}. To connect directly, no change is made in the first stage, but the voltage level of the second-stage is increased by 2.8 V with respect to ground so that, the value of V_{B2}, V_{E2} and V_{C2} becomes 2.8 V higher than their original value.

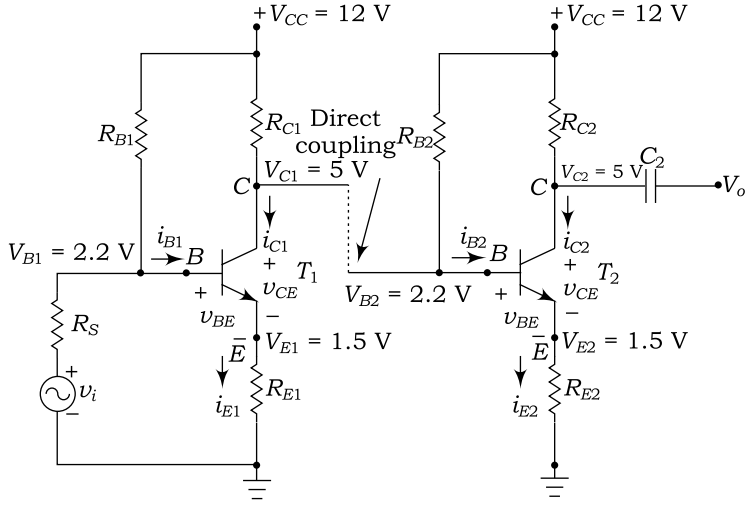


Fig. 3.102 Two-stage direct-coupled common-emitter amplifier

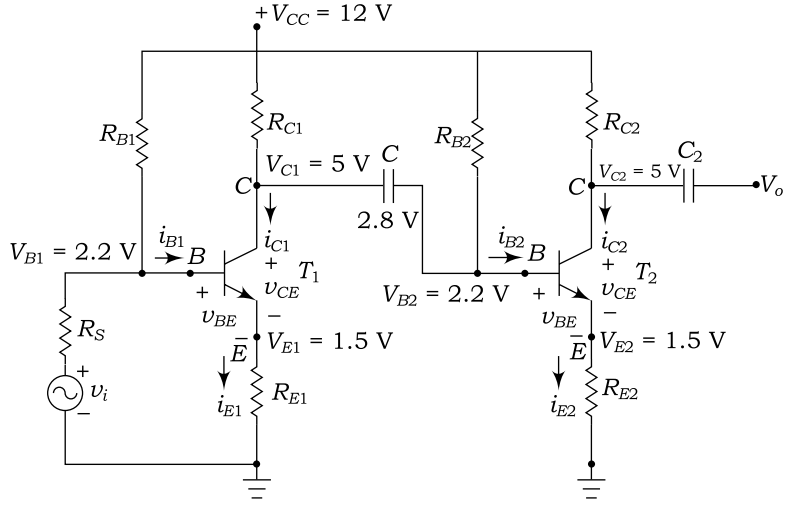


Fig. 3.103 Two-stage common-emitter amplifier coupled by the capacitor *C*

This is possible by collecting a 2.8 V battery in series with R_{E2} and 14.8 V supply in place of 12 V supply as shown in Fig. 3.104.

It is clear from Fig. 3.104 that $V_{B2} = 5$ V and $V_{C2} = 7.8$ V. Therefore, V_{C1} is equal to V_{B2} and the amplifiers can be connected directly. Due to increase of base, emitter and collector voltages by the same value, the $V_{BE} = 0.7$ V and $V_{CB2} = 2.8$ V. Therefore, the Q-point of the transistor will be same. This type of direct coupling has a lot of disadvantages. Since V_{CC1} (12 V) and V_{CC2} (14.8 V) are not same, a 2.8 V battery must be connected in series with R_{E2}. The 2.8 V battery can be replaced by a 2.8 V zener diode and it can be removed by increasing the R_{E2}. Then the input resistance increases to T_2 and gain is reduced due to increase of negative feedback. Since V_{CC2} is larger than V_{CC1}, in a three-stage amplifier V_{CC3} must be larger than $V_{CC2.}$ Consequently, the required dc voltage supplies are impractically high in a multistage amplifier.

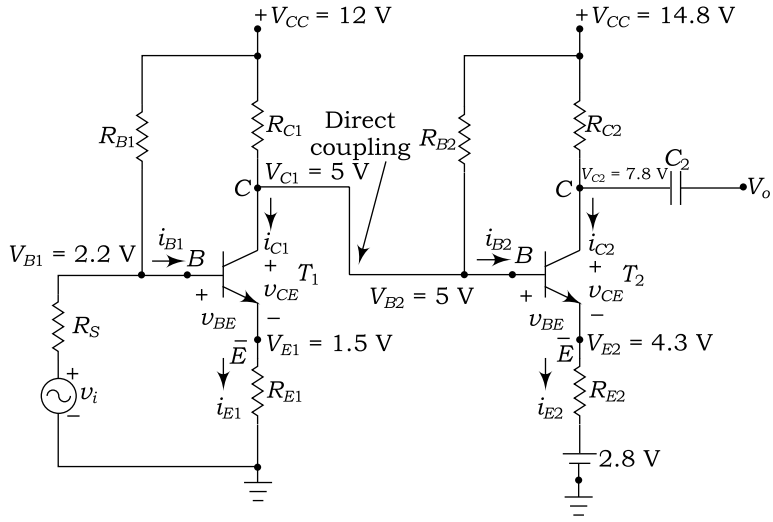


Fig. 3.104 Direct coupling

The alternative solution of the above problem is shown in Fig. 3.105 where alternative polarity transistors are connected in cascade and the dc voltages are adjusted in such a way that each transistor operates at the same *Q*-point.

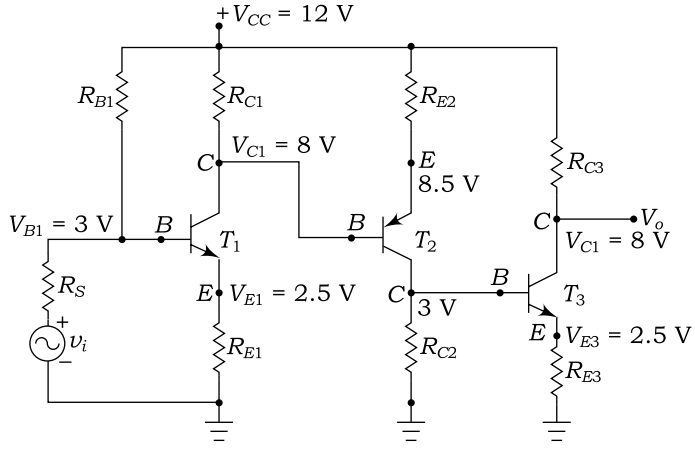


Fig. 3.105 Three-stage direct-coupled amplifier

3.17.1 Advantages of a Direct-Coupled Amplifier

The direct-coupled amplifier has the following advantages:

1. This circuit is very simple as very few resistances are present in an amplifier circuit.
2. The cost of this amplifier is low due to absence of coupling devices.
3. This amplifier operates in very low frequency including zero frequency.

3.17.2 Disadvantages of a Direct-Coupled Amplifier

The direct-coupled amplifier has the following disadvantages:

1. This amplifier cannot operate in high-frequency range. Hence, it cannot amplify the high-frequency signals.
2. This amplifier has poor temperature stability. Due to this, Q-point of transistors shifts. Therefore, in a multistage amplifier, the last-stage transistor is to be operated in either cut-off or saturation.
3. All integrated circuit (IC) amplifiers are direct-coupled due to the difficulty of fabrication of capacitors.

3.17.3 Applications of a Direct-Coupled Amplifier

The direct-coupled amplifier has the following applications:

1. This amplifier is used in analog computation.
2. It is used in linear integrated circuits.
3. It is used in regulated dc power supply.
4. It is used in bioelectric measurements.

3.18 FREQUENCY RESPONSE OF BJT AMPLIFIERS

The small-signal analysis of BJT amplifier is already discussed in this chapter. In this section, low-frequency and high-frequency response of BJT amplifiers are discussed in detail. The gain of an amplifier is a function of frequency. In this section amplifier gain versus frequency plot is given where gain factor is given in terms of decibels and frequency in terms of Hz on logarithmic scale. To obtain the frequency response of an amplifier, capacitors and transistor capacitors are incorporated in circuit analysis. Usually, we determine the bandwidth of the amplifier circuit from the frequency response. For this, initially transfer function of the circuit is derived in s-domain or in complex frequency domain. Using the Bode plots of the transfer function, the magnitude response, phase response, time constant and 3 dB cut-off frequencies are computed.

3.19 GENERAL FREQUENCY RESPONSE OF AMPLIFIERS

The frequency of the applied input signal has a significant effect on the frequency response of the single-stage and multistage amplifiers. At low frequency, the effect of coupling and bypass capacitors cannot be neglected due to the capacitive reactance value. At high-frequency response, frequency dependent parameters will be present in the circuit and stay capacitance will be associated with small-signal model of BJT and FET.

During plotting the frequency response of the amplifier circuit, the logarithmic scale along the x-axis permit a plot extending from low frequency to high-frequency regions. Usually, any frequency response can be divided into three regions such as

1. Low-frequency region
2. Mid-frequency region
3. High-frequency region

Actually, the frequency response curve of any amplifier is a plot between the magnitude of gain and logarithmic frequencies. Figure 3.106 shows a frequency response curve of an *RC* coupled amplifier. The drop in gain at low-frequency region is due to increase in capacitive reactance in this region. In the high-frequency region, the drop in gain is due to parasitic capacitance or the frequency-dependent gain on active device in those regions. The frequencies corresponding to f_L and f_H are called *cut-off frequency*, corner frequency or half-power frequency. f_L is called lower cut-off frequency and f_H represents the higher cut-off frequency.

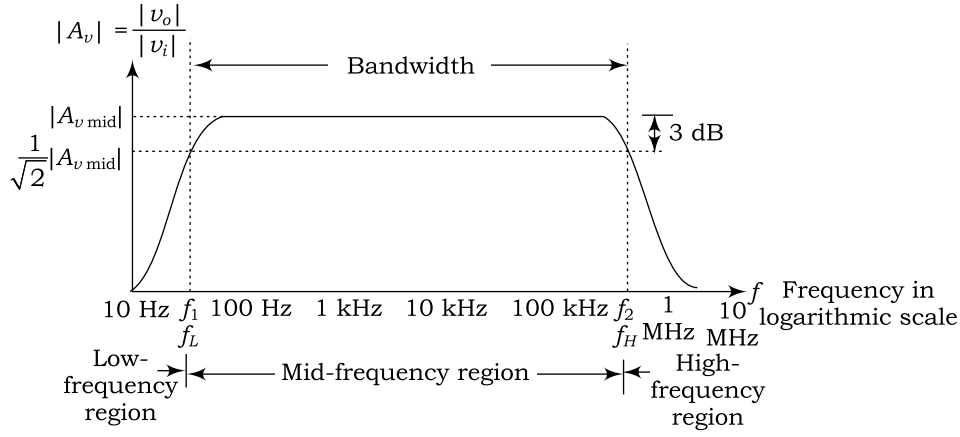


Fig. 3.106 Gain vs frequency plot of a *RC* coupled amplifier

At cut-off frequencies f_L and f_H, the output power is half of the mid-band power output. The power output at mid-frequency is equal to

$$P_{\text{output(mid)}} = \frac{|v_o^2|}{R} \tag{3.149}$$

As voltage gain at mid-frequency is $A_{v\text{mid}} = \frac{|v_o|}{|v_i|}$, $P_{\text{output(mid)}} = \frac{|v_o^2|}{R} = \frac{|A_{v\text{mid}} v_i|^2}{R}$ (3.150)

At half-power frequencies f_L and f_H, the power output is

$$P_{\text{output-HPF}} = \frac{|0.707 A_{v\text{mid}} v_i|^2}{R} = 0.5 \frac{|A_{v\text{mid}} v_i|^2}{R} \tag{3.151}$$

Then $$P_{\text{output–HPF}} = 0.5 P_{\text{output(mid)}} \tag{3.152}$$

The bandwidth of amplifier can be determined by f_L and f_H and it is expressed by

$$\text{Bandwidth} = f_H - f_L$$

This is also called *passband* of the amplifier. Usually, a decibel (dB) plot of voltage gain with respect to frequency is very useful in most applications. Before the logarithmic plot, the magnitude should be normalised. The gain at each frequency is divided by the mid-band gain. Figure 3.107 shows the normalised plot of gain vs frequency in log scale.

Assume the mid-band gain is 1. At half-power frequency, gain is equal to $0.707 = \frac{1}{\sqrt{2}}$. A decibel plot can be obtained by the following transformation.

$$\frac{A_v}{A_{v\text{mid}}}|_{\text{dB}} = 20 \log_{10} \frac{A_v}{A_{v\text{mid}}} \tag{3.153}$$

The gain at half-power point in decibel is

$$\frac{A_{v\text{HPF}}}{A_{v\text{mid}}}|_{\text{dB}} = 20 \log_{10} \frac{A_{v\text{HPF}}}{A_{v\text{mid}}} = 20 \log_{10} \frac{0.707\, A_{v\text{mid}}}{A_{v\text{mid}}} \quad \text{as } A_{v\text{HPF}} = 0.707\, A_{v\text{mid}}$$

$$= 20 \log_{10} 0.707 = -3 \text{ dB} \tag{3.154}$$

The decibel plot of the normalised gain vs frequency for an RC coupled amplifier is depicted in Fig. 3.108.

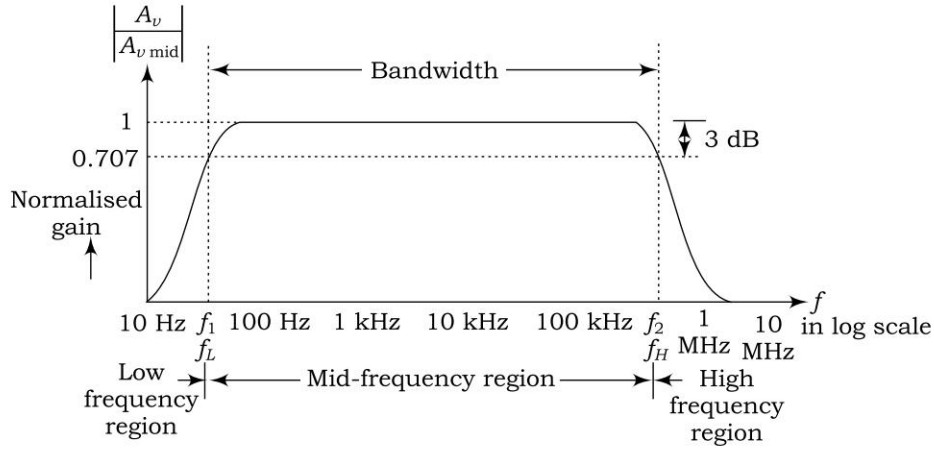


Fig. 3.107 Normalised plot of gain vs frequency for an RC coupled amplifier

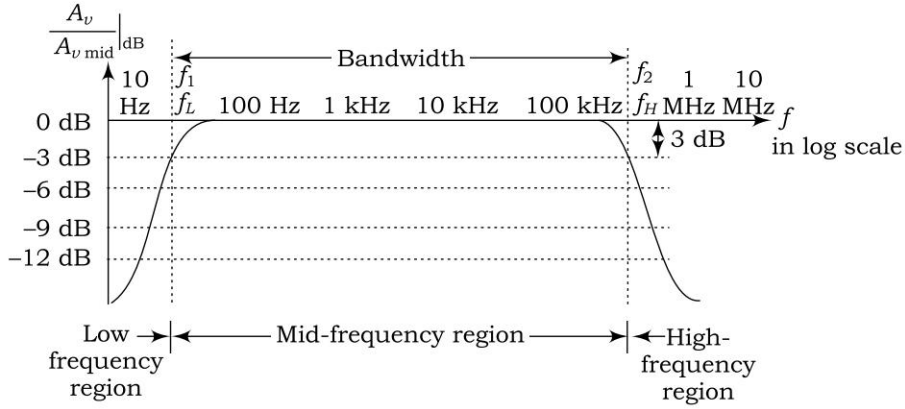


Fig. 3.108 Decibel plot of the normalised gain vs frequency for an RC coupled amplifier

3.20 BODE PLOT OF RC CIRCUIT

The cut-off frequencies of a single-stage BJT amplifier depends on the *RC* combinations formed by coupling and bypass capacitors C_1, C_2, C, C_E and resistive parameters. For circuit analysis, each capacitor can be modelled and its frequency response can be studied. If we know the cut-off frequency of each capacitor, we can determine the lower cut-off frequency of the amplifier circuit.

The method for determining the *lower cut-off frequency* f_L is presented in this section. The *upper cut-off frequency* f_H can be determined with some extension in the frequency response. f_L and f_H are also known as α *cut-off* and β *cut-off* frequency.

The capacitive reactance value is presented by $X_C = \dfrac{1}{\omega C} = \dfrac{1}{2\pi fC}$ as $\omega = 2\pi f$ (3.155)

At very low frequency, $f = 0$ and capacitive reactance value is $X_C = \dfrac{1}{2\pi fC} = \dfrac{1}{2\pi \times 0 \times C} = \infty$.

Hence, this is equivalent to open circuit as shown in Fig. 3.109(b).

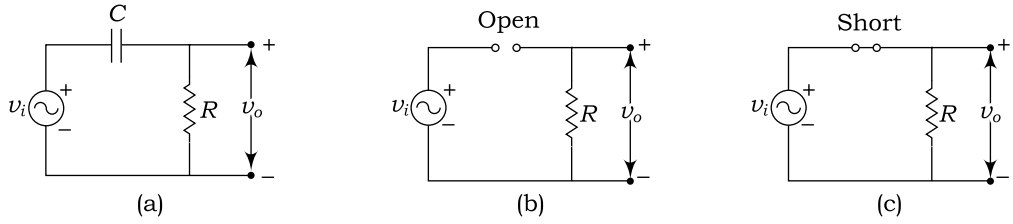


Fig. 3.109 (a) *RC* circuit (b) Equivalent circuit at low frequency (c) Equivalent circuit at high frequency

At very high frequency, $f = \infty$ and capacitive reactance value is $X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times \infty \times C} = 0$. Hence, this is equivalent to short circuit as shown in Fig. 3.109(c). Then output voltage is equal to input voltage, i.e., $v_o = v_i$.

The frequency response of voltage gain $\left(A_v = \frac{v_o}{v_i}\right)$ between two extremes (very low frequency $f = 0$ and very high frequency $f = \infty$) is shown in Fig. 3.110. It is clear from Fig. 3.110 that as the frequency increases, the capacitive reactance decreases and more input voltage appear at the output terminals.

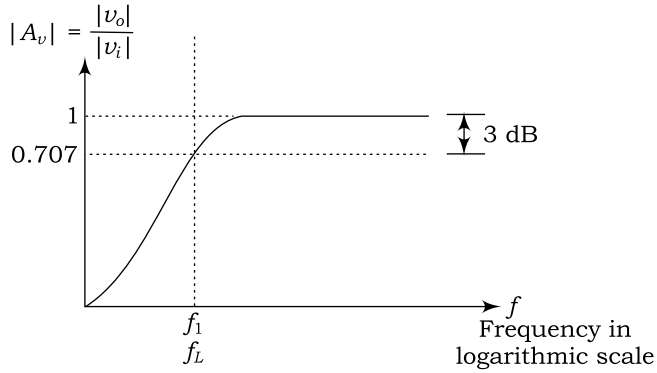


Fig. 3.110 A_v vs frequency for a *RC* circuit

Applying the voltage divider rule in Fig. 3.109(a), we find the output voltage and its value is equal to

$$v_o = \frac{R}{R - jX_C} v_i \tag{3.156}$$

Then the magnitude of v_o is given by $|v_o| = \frac{R}{\sqrt{R^2 + X_C^2}} |v_i|$ (3.157)

When $X_C = R$, the output voltage is

$$|v_o| = \frac{R}{\sqrt{R^2 + X_C^2}} |v_i| = \frac{R}{\sqrt{R^2 + R^2}} |v_i| = \frac{R}{\sqrt{2R^2}} |v_i| = \frac{R}{\sqrt{2}R} |v_i| = \frac{1}{\sqrt{2}} |v_i| \tag{3.158}$$

Then the magnitude of voltage gain is $|A_v| = \frac{|v_o|}{|v_i|} = \frac{1}{\sqrt{2}} = 0.707$ (3.159)

It is clear from Eq. (3.159) that the frequency corresponds to $X_C = R$, and the output voltage will be equal to 0.707 times of input voltage.

The frequency at which $X_C = R$ can be obtained as follows:

Assume at frequency f_1, $X_C = R$. Then $X_C = \dfrac{1}{2\pi f_1 C} = R$ and $f_1 = \dfrac{1}{2\pi RC}$

Then gain in dB is $G_v = 20 \log_{10} A_v = 20 \log_{10} 0.707 = 20 \log_{10} \dfrac{1}{\sqrt{2}} = -3dB$ (3.160)

At $f = f_1 = f_L$, there is –3 dB drop in gain from the mid-band frequency gain.

When voltage gain $\left(A_v = \dfrac{v_o}{v_i} \right)$ is equal to 1, the gain in decibel is

$$G_v = 20 \log_{10} A_v = 20 \log_{10} 1 = 0 \text{ dB}$$

The voltage gain can also be written as

$$A_v = \frac{v_o}{v_i} = \frac{R}{R - jX_C} = \frac{1}{1 - j\dfrac{X_C}{R}} = \frac{1}{1 - j\dfrac{1}{2\pi fCR}} \quad \text{as } X_C = \frac{1}{\omega C} = \frac{1}{2\pi fC}$$

Since $f_1 = f_L = \dfrac{1}{2\pi RC}$, we get $A_v = \dfrac{1}{1 - j\dfrac{f_1}{f}}$ (3.161)

The voltage gain is expressed by

$$A_v = |A_v| \angle\theta = \frac{v_o}{v_i} = \frac{1}{1 - j\dfrac{f_1}{f}} = \frac{1}{\sqrt{1 + \left(\dfrac{f_1}{f}\right)^2}} \angle \tan^{-1}\left(\frac{f_1}{f}\right) \tag{3.162}$$

At $f = f_1$, voltage gain $|A_v| = \dfrac{1}{\sqrt{1 + \left(\dfrac{f_1}{f_1}\right)^2}} = \dfrac{1}{\sqrt{1+1^2}} = \dfrac{1}{\sqrt{2}} = 0.707$ which corresponds to –3 dB.

In the logarithmic form, the gain is equal to

$$|A_v|_{\text{dB}} = 20 \log_{10} \frac{1}{\sqrt{1 + (f_1/f)^2}} = 20 \log_{10} [1 + (f_1/f)^2]^{-\frac{1}{2}}$$

$$= 20 \times \left(-\frac{1}{2}\right) \times \log_{10} [1 + (f_1/f)^2] = -10 \log_{10} [1 + (f_1/f)^2] \tag{3.163}$$

When $f_1 >> f$, the ratio $\dfrac{f_1}{f} >> 1$ and Eq. (3.163) can be written as

$$|A_v|_{\text{dB}} = -10 \log_{10} \left[1 + \left(\frac{f_1}{f}\right)^2 \right] = -10 \log_{10} \left(\frac{f_1}{f}\right)^2 = -20 \log_{10} \left(\frac{f_1}{f}\right)$$

At $f = f_1, \dfrac{f_1}{f} = 1$ and $|A_v|_{\text{dB}} = -20 \log_{10} \left(\dfrac{f_1}{f}\right) = -20 \log_{10} 1 = 0$ dB

At $f = \dfrac{1}{2} f_1, \dfrac{f_1}{f} = 2$ and $|A_v|_{\text{dB}} = -20 \log_{10} \left(\dfrac{f_1}{f}\right) = -20 \log_{10} 2 = -6$ dB

At $f = \frac{1}{4} f_1, \frac{f_1}{f} = 4$ and $|A_v|_{dB} = -20 \log_{10}\left(\frac{f_1}{f}\right) = -20 \log_{10} 4 = -12$ dB

At $f = \frac{1}{10} f_1, \frac{f_1}{f} = 10$ and $|A_v|_{dB} = -20 \log_{10}\left(\frac{f_1}{f}\right) = -20 \log_{10} 10 = -20$ dB

The plot of the above values is a straight line. For $f >> f_1$, a straight line is obtained only for 0 dB value. Hence the low-frequency response can be obtained only when $f << f_1$. At $f = f_1$ there is 3 dB drop in gain. From the Fig. 3.111 we can say that

1. A change in frequency by a factor of 2 (equivalent to 1 octave) results in 6 dB change in the ratio of the frequency from $\frac{f_1}{2}$ to f_1
2. For a 10:1 change in frequency (equivalent to 1 decade), there is a 20 dB change in the ratio. The frequency change from $\frac{f_1}{10}$ to f_1 is clear from Fig. 3.111.

We can generate the decibel plot of an amplifier circuit by the following steps:

1. Find f_1 of the amplifier circuit from the circuit parameters.
2. Sketch two asymptotes, one along 0 dB and the other at f_1 with 6 dB/octave or 20 dB/decade.
3. Find the –3 dB point corresponding to frequency f_1 and draw a smooth curve.

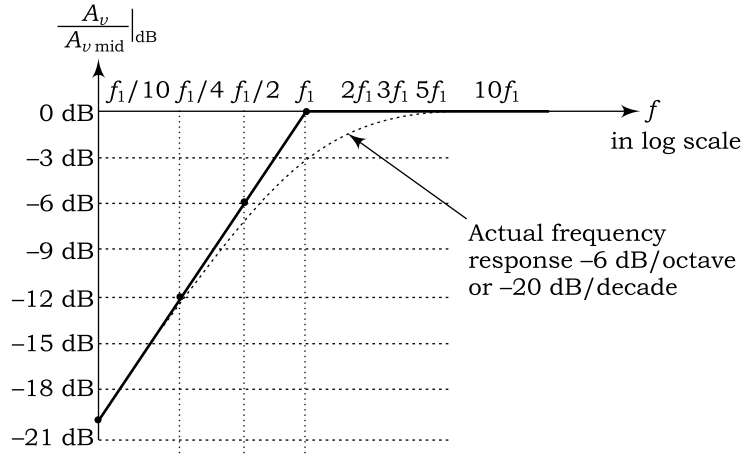


Fig. 3.111 Bode plot of *RC* circuit in low-frequency region

3.21 TRANSIENT RESPONSE

The transient response of an amplifier is the output waveform generated when there is a sudden change in input voltage or a step signal is applied to the amplifier. This response is represented by a plot of voltage with respect to time in contrast to frequency response.

The transient response of an amplifier depends on its frequency response. When two amplifiers have the same frequency response, their transient responses will be identical.

A pulse may consist of infinite number of frequency components. Then the transient output waveform represents the amplifier's ability to amplify all the frequency components equally. It is not possible for an

amplifier to have infinite bandwidth. Therefore, the transient output waveform will always be a distorted version of the input signal.

Figure 3.113(b) shows the transient response of an *RC* circuit. This circuit works as a low pass filter. The frequency response of an *RC* circuit is given in Fig. 3.113(a).

1. Time Constant τ

The time constant of the *RC* circuit is the time required for the transient output to reach 0.632 times of final value. It is represented by τ and it is expressed as $\tau = RC$.

The upper cut-off frequency is $f_2 = f_H = \dfrac{1}{2\pi RC} = \dfrac{1}{2\pi\tau}$

The bandwidth of the low-pass filter is

$$\text{Bandwidth} = f_2 - f_1 = f_H - f_L = f_H - 0 = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau}$$

It is clear from the above expression that the time required for the transient response to rise up to a certain voltage level is inversely proportional to bandwidth as $\tau = \dfrac{1}{2\pi \times \text{Bandwidth}}$.

2. Rise Time t_r

This is the time required for an output voltage waveform to change from 10% of its final value to 90% of its final value. It is represented by t_r. The relationship between rise time and bandwidth is $t_r = \dfrac{0.35}{\text{Bandwidth}}$ s

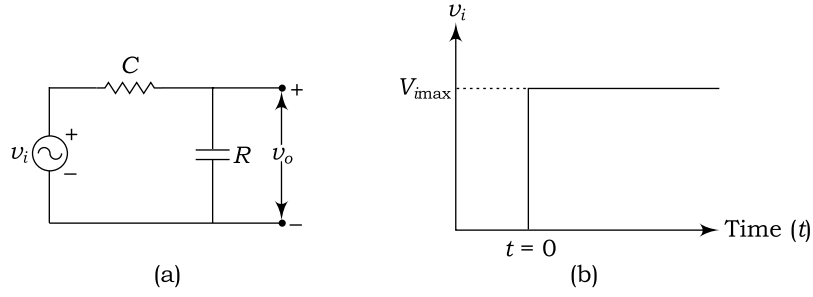


Fig. 3.112 (a) *RC* circuit (b) Input voltage

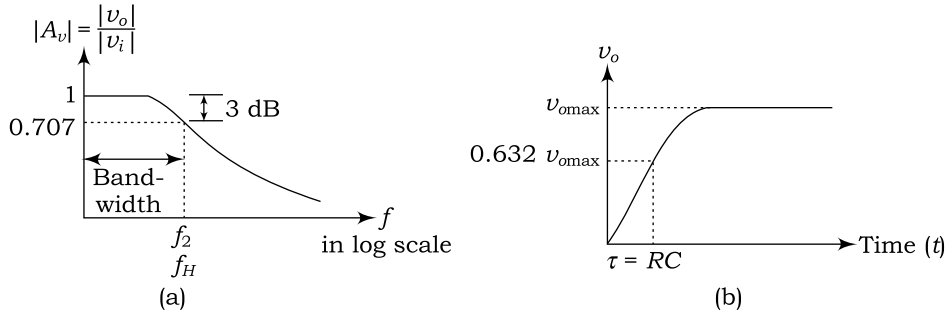


Fig. 3.113 (a) Frequency response of *RC* circuit (b) Transient response of output voltage

3.22 HIGH-FREQUENCY MODEL OF TRANSISTOR

The Ebers–Moll model of a bipolar junction transistor does not include the junction capacitance. Therefore, this model cannot be used in analysis of transistors at high frequency. Figure 3.114 shows the hybrid-π model or Giacoletto model of a transistor in the common-emitter configuration. In this, Fig. 3.114 represents the external base terminal and B' is the virtual base terminal or the active internal terminal of the base region. The virtual base terminal is depicted in Fig. 3.115. The hybrid-π model of BJT is developed based on the following assumptions:

1. In this model, resistances and capacitances are frequency independent.
2. At a certain biasing condition, the values of resistances and capacitances do not change due to small signal variation.

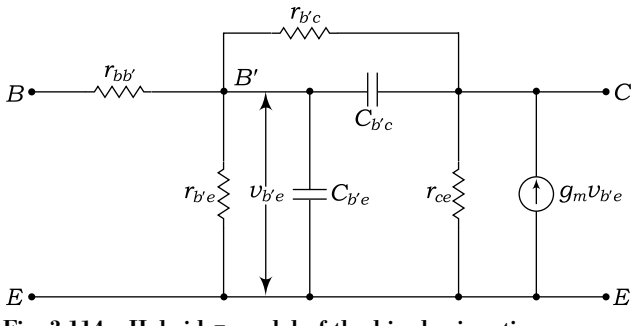


Fig. 3.114 Hybrid-π model of the bipolar junction transistor at high frequency

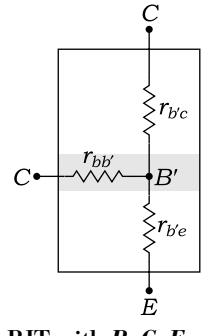


Fig. 3.115 BJT with *B*, *C*, *E* and *B′* terminals and $r_{bb'}$, $r_{b'e}$ and $r_{b'c}$ resistances

- $r_{bb'}$—It is the base spreading resistance between the external base terminal B and the virtual base terminal B'. Its typical value is about 100 Ω.
- $r_{b'e}$—It is the resistance between the virtual base terminal B' and the emitter terminal E. Its typical value is about 1000 Ω.
- $r_{b'c}$—It is the resistance between the virtual base terminal B' and the collector terminal C. Its typical value is about 4 MΩ.
- $C_{b'e}$—It is the diffusion capacitance of the normally forward-biased base emitter junction. Actually, the excess minority carriers are stored in the base region and the diffusion capacitance exists between the base region B' and emitter E. Its typical value is about 100 pF.
- $C_{b'c}$—It is the transistor capacitance of the normally reverse-biased collector base junction. It is also known as the collector junction barrier capacitance. Its typical value is about 3 pF.
- r_{ce}—This is the resistance between the collector and emitter. Its typical value is about 80 kΩ.
- $g_m v_{b'e}$—The g_m is called the transconductance of the transistor. Any small change in $v_{b'e}$, the emitter-base junction generates a corresponding change in the small-signal collector current. This produces a current source and is represented by $g_m v_{b'e}$.

At low frequency, all capacitors ($C_{b'e}$ and $C_{b'c}$) are negligible. Then removing the $C_{b'e}$ and $C_{b'c}$, we obtain the hybrid-π model of the bipolar junction transistor at low frequency as shown in Fig. 3.116.

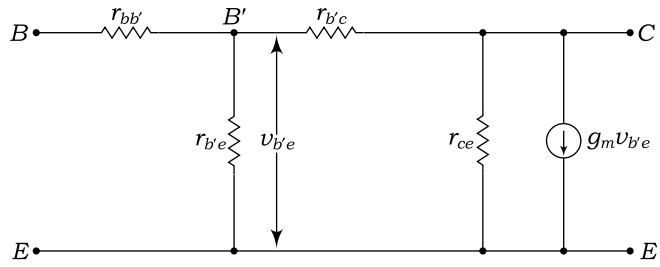


Fig. 3.116 Hybrid-π model of the bipolar junction transistor at low frequency

3.23 MILLER'S THEOREM

When an impedance Z is connected between the input (1) and output (2) terminals of a network which provides a voltage gain A_v as shown in Fig. 3.117(a), an equivalent circuit which gives the same effect can be drawn by removing Z and connecting an impedance $Z_1 = \dfrac{Z}{1 - A_v}$ across input terminals and another impedance $Z_2 = \dfrac{Z}{1 - \dfrac{1}{A_v}} = \dfrac{ZA_v}{A_v - 1}$ across output terminals as shown in Fig. 3.117(b). This theorem is called *Miller's theorem*.

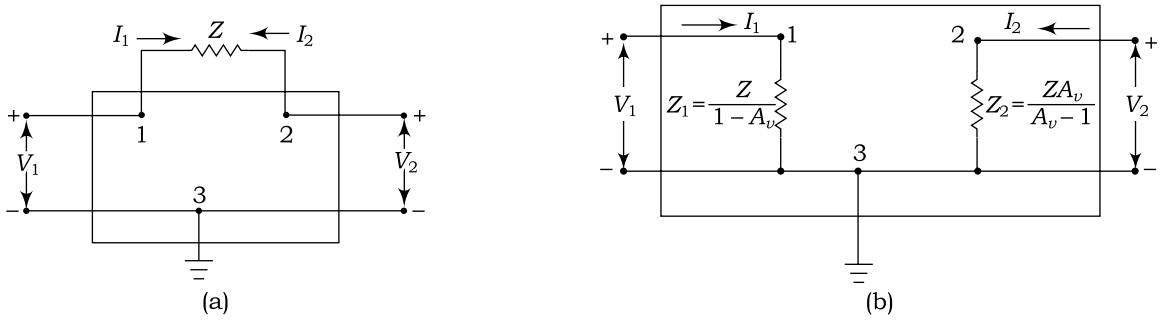


Fig. 3.117 (a) Miller's theorem (b) Miller's theorem: equivalent circuit of Fig. 3.117(a)

Proof: In the circuit 3.117(a), the current I_1 is equal to $I_1 = \dfrac{V_1 - V_2}{Z}$ (3.164)

The voltage gain of the circuit is A_v and it is given by $A_v = \dfrac{V_2}{V_1}$

Then $V_2 = A_v V_1$. After substituting the value of V_2 in Eq. (3.164) we get

$$I_1 = \frac{V_1 - A_v V_1}{Z} = \frac{(1 - A_v)V_1}{Z} = \frac{V_1}{\dfrac{Z}{1 - A_v}} \tag{3.165}$$

As per Fig. 3.117(b), the current I_1 is $I_1 = \dfrac{V_1}{Z_1}$

Then $Z_1 = \dfrac{Z}{1 - A_v}$

As current $I_2 = -I_1$,

$$I_2 = -\frac{V_1 - V_2}{Z} = \frac{V_2 - V_1}{Z}$$

$$= \frac{V_2 - \dfrac{V_2}{A_v}}{Z} = \frac{\dfrac{A_v - 1}{A_v}V_2}{Z} = \frac{V_2}{\dfrac{ZA_v}{A_v - 1}} \quad \text{As } V_2 = A_v V_1, V_1 = \frac{V_2}{A_v}$$

As per Fig. 3.117(b), the current I_2 is $I_2 = \dfrac{V_2}{Z_2}$

Then $Z_2 = \dfrac{ZA_v}{A_v - 1}$

3.24 DUAL OF MILLER'S THEOREM

When an impedance Z is connected as shunt between the input and output terminals of a network which provides a current gain A_I as shown in Fig. 3.118(a), an equivalent circuit which gives the same effect can be drawn by removing Z and connecting the impedance $Z_1 = Z(1 - A_I)$ at the input side and another impedance $Z_2 = Z\left(1 - \dfrac{1}{A_I}\right) = \dfrac{Z(A_I - 1)}{A_I}$ at the output side as shown in Fig. 3.118(b). This theorem is known as *dual of Miller's theorem*.

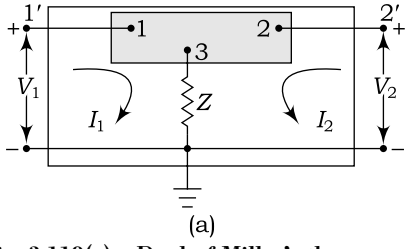


Fig. 3.118(a) Dual of Miller's theorem

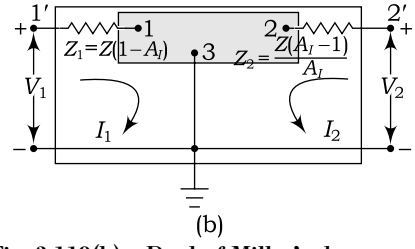


Fig. 3.118(b) Dual of Miller's theorem: equivalent circuit of Fig. 3.118(a)

Proof: In the circuit 3.118(a), the currents I_1 and I_2 flow through impedance Z. The voltage drop across Z is equal to $V_1 = (I_1 + I_2)Z$. (3.166)

The current gain of the circuit is A_I and it is expressed by $A_I = \dfrac{-I_2}{I_1}$

Then $I_2 = -A_I I_1$. After substituting the value of I_2 in Eq. (3.166) we obtain

$$V_1 = (I_1 + I_2)Z = (I_1 - A_I I_1)Z = (1 - A_I)I_1 Z = (1 - A_I)ZI_1 \tag{3.167}$$

As per Fig. 3.118(b), the voltage V_1 is equal to $V_1 = I_1 Z_1$

Then $Z_1 = (1 - A_I)Z$

The voltage $V_2 = (I_1 + I_2)Z$

As $A_I = \dfrac{-I_2}{I_1}, I_1 = -\dfrac{I_2}{A_I}$

After substituting the value of I_1 in Eq. (3.166), we get

$$V_2 = (I_1 + I_2)Z = \left(-\frac{I_2}{A_I} + I_2\right)Z = \left(1 - \frac{1}{A_I}\right)I_2 Z = \left(1 - \frac{1}{A_I}\right)ZI_2 = \left(\frac{A_I - 1}{A_I}\right)ZI_2$$

As per Fig. 3.118(b), the voltage V_2 is equal to $V_2 = I_2 Z_2$

Then $Z_2 = \dfrac{(A_I - 1)Z}{A_I} = \dfrac{Z(A_I - 1)}{A_I}$

3.25 EFFECT OF BYPASS CAPACITOR AT LOW-FREQUENCY RESPONSE

Figure 3.119(a) shows a single-stage common-emitter amplifier. The emitter resistance R_E provides biasing and thermal stability. The bypass capacitor C_E is connected across R_E to remove degenerative effect due to negative feedback.

The voltage gain in low-frequency region $A_{v(\text{LF})}$ is defined as the ratio of output voltage v_o to the input voltage v_i. Then $A_{v(\text{LF})}$ is expressed by

$$A_{v(\text{LF})} = \frac{v_o}{v_i}$$

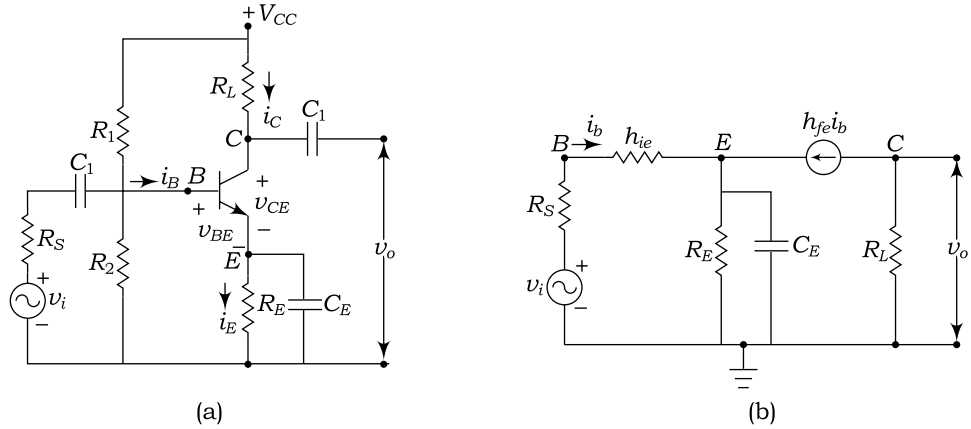


Fig. 3.119 (a) Single-stage *CE* amplifier (b) *h*-parameter equivalent circuit of Fig. 3.119(a)

In the low-frequency region, the coupling capacitance C is sufficiently large and its capacitive reactance is small. Then there is no effect of the coupling capacitance on the output response. The value of $R_1 \| R_2$ is larger than the input resistance R_i so that $R_1 \| R_2$ can be neglected in the h-parameter equivalent circuit.

The output voltage is $v_o = i_L R_L = -h_{fe} i_b R_L \ldots$ as $i_L = -h_{fe} i_b$ (3.168)

The base current is $i_b = \dfrac{v_S}{R_S + R_i}$

where, R_i is input resistance of *CE* amplifier and R_S is the internal resistance of source

The value of R_i is equal to $R_i = h_{ie} + (1 + h_{fe})Z_E$ (3.169)

where, $Z_E = R_E \| X_{C_E} = \dfrac{R_E \times X_{C_E}}{R_E + X_{C_E}} \dfrac{R_E \times \dfrac{1}{j\omega C_E}}{R_E + \dfrac{1}{j\omega C_E}} = \dfrac{R_E}{1 + j\omega R_E C_E}$ as $X_{C_E} = \dfrac{1}{j\omega C_E}$

Then $$R_i = h_{ie} + (1 + h_{fe})Z_E = h_{ie} + (1 + h_{fe})\frac{R_E}{1 + j\omega R_E C_E} \tag{3.170}$$

Therefore, base current $i_b = \dfrac{v_i}{R_S + R_i} = \dfrac{v_i}{R_S + h_{ie} + (1 + h_{fe})\dfrac{R_E}{1 + j\omega R_E C_E}}$ (3.171)

After substituting the value of i_b in Eq. (3.168), we obtain

$$v_o = -h_{fe} i_b R_L = -h_{fe} \frac{v_i}{R_S + h_{ie} + \dfrac{(1 + h_{fe})R_E}{1 + j\omega R_E C_E}} R_L \tag{3.172}$$

Then $$A_{v(\text{LF})} = \frac{v_o}{v_i} = \frac{-h_{fe} R_L}{R_S + h_{ie} + \dfrac{(1 + h_{fe})R_E}{1 + j\omega R_E C_E}} \tag{3.173}$$

In the mid-frequency range, ω is very large and the voltage gain in the mid-frequency region is

$$A_{v(\text{MF})} = \frac{v_o}{v_i} = \frac{-h_{fe} R_L}{R_S + h_{ie}} \quad \text{as } \frac{(1 + h_{fe})R_E}{1 + j\omega R_E C_E} \to 0 \tag{3.174}$$

Then the voltage gain at low-frequency region to the voltage gain in mid-frequency region is

$$\frac{A_{v(\text{LF})}}{A_{v(\text{MF})}} = \frac{\dfrac{-h_{fe} R_L}{R_S + h_{ie} + \dfrac{(1 + h_{fe})R_E}{1 + j\omega R_E C_E}}}{\dfrac{-h_{fe} R_L}{R_S + h_{ie}}} = \frac{R_S + h_{ie}}{R_S + h_{ie} + \dfrac{(1 + h_{fe})R_E}{1 + j\omega R_E C_E}}$$

$$= \frac{1}{1 + \dfrac{(1 + h_{fe})R_E}{R_S + h_{ie}}} \frac{1 + j\dfrac{f}{f_o}}{1 + j\dfrac{f}{f_p}} \text{ where, } f_o = \frac{1}{2\pi C_E R_E} \text{ and } f_p = \frac{1 + \dfrac{(1 + h_{fe})R_E}{R_S + h_{ie}}}{2\pi C_E R_E} \tag{3.175}$$

Since $\dfrac{(1 + h_{fe})R_E}{R_S + h_{ie}} >> 1, f_p = \dfrac{\dfrac{(1 + h_{fe})R_E}{R_S + h_{ie}}}{2\pi C_E R_E}$ and $f_p >> f_o$

At $$f = f_p, \text{ the } \frac{A_{v(\text{LF})}}{A_{v(\text{MF})}} = \frac{1}{1 + \dfrac{(1 + h_{fe})R_E}{R_S + h_{ie}}} \frac{1 + j\dfrac{f_p}{f_o}}{1 + j\dfrac{f_p}{f_p}} = \frac{R_S + h_{ie}}{(1 + h_{fe})R_E} \frac{j\dfrac{f_p}{f_o}}{1 + j1} \quad f_p >> f_o \tag{3.176}$$

Then $$\left|\frac{A_{v(\text{LF})}}{A_{v(\text{MF})}}\right| = \frac{R_S + h_{ie}}{(1+h_{fe})R_E}\frac{\frac{f_p}{f_o}}{\sqrt{2}} = \frac{1}{\sqrt{2}} \quad \text{as } \frac{f_p}{f_o} = \frac{(1+h_{fe})R_E}{R_S + h_{ie}} \tag{3.177}$$

Since the ratio of voltage gain at low frequency to mid-frequency has dropped by $\frac{1}{\sqrt{2}}$, the power gain at low frequency will be dropped by 3 dB from the gain at mid-frequency. Then the lower 3 dB frequency is equal to

$$f_1 = f_p = \frac{\frac{(1+h_{fe})R_E}{R_S + h_{ie}}}{2\pi C_E R_E} = \frac{(1+h_{fe})R_E}{(R_S + h_{ie})2\pi C_E R_E} = \frac{(1+h_{fe})}{(R_S + h_{ie})2\pi C_E} \tag{3.178}$$

Then the value of C_E is equal to $$C_E = \frac{(1+h_{fe})}{(R_S + h_{ie})2\pi f_1} \tag{3.179}$$

3.26 EFFECT OF COUPLING CAPACITANCE IN LOW-FREQUENCY RESPONSE

Figure 3.120 shows a *CE* amplifier in the low-frequency region. The effect of coupling capacitance C_1 on the low-frequency region is studied. Since C_E is large, there is no reduction in low-frequency gain. As R_E is effectively bypassed, the low-frequency model for a *CE* amplifier with the coupling capacitor C_1 is depicted in Fig. 3.120.

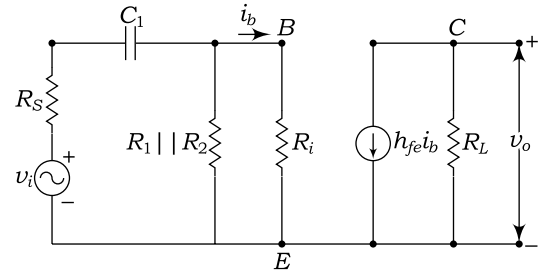


Fig. 3.120 Low-frequency model for *CE* amplifier with the coupling capacitor C_1

In the mid-frequency range, reactance of C_1 is negligible and the $$A_{v(\text{MF})} = \frac{v_o}{v_i} = \frac{-h_{fe}R_L}{R_S + h_{ie} + (1+h_{fe})R_{C_E}} \tag{3.180}$$

where, R_{C_E} represents the series resistance of C_E.

The lower 3 dB frequency $$f_1 = \frac{1}{2\pi(R_S + R_1')C_1} \tag{3.181}$$

where, $R_i' = R_1 || R_2 || R_i$, $R_i = h_{ie}$ for emitter bypass capacitor and $R_i = h_{ie} + (1 + h_{fe})\, R_{C_E}$ when capacitor series resistance R_{C_E} is considered.

For better low-frequency response, the capacitors C_1 and C_E must be very large.

3.27 SHORT-CIRCUIT CURRENT GAIN IN CE AMPLIFIER

The transistor's high-frequency capability can be determined if the common-emitter short-circuit current gain is a function of frequency. Figure 3.121 shows the high-frequency circuit when the load resistance R_L is short circuited. In Fig. 3.121, the capacitance $C_{b'e}$ is connected in parallel with $C_{b'c}$.

The short-circuit current gain is

$$A_I = \frac{I_L}{I_i}$$

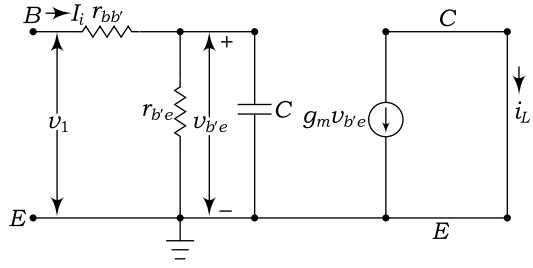


Fig. 3.121 High-frequency equivalent circuit of a *CE* amplifier to determine short-circuit current gain

The load current $I_L = -g_m v_{b'e}$ and the input current is $I_i = \dfrac{v_{b'e}}{r_{b'e} \| \dfrac{1}{j\omega C}}$

As $C = C_{b'e} + C_{b'c}, r_{b'e} \| \dfrac{1}{j\omega C} = r_{b'e} \| \dfrac{1}{j\omega(C_{b'e} + C_{b'c})}$

$$= \frac{r_{b'e} \dfrac{1}{j\omega(C_{b'e} + C_{b'c})}}{r_{b'e} + \dfrac{1}{j\omega(C_{b'e} + C_{b'c})}} = \frac{r_{b'e}}{1 + j\omega(C_{b'e} + C_{b'c}) r_{b'e}} = \frac{r_{b'e}}{1 + j2\pi f(C_{b'e} + C_{b'c}) r_{b'e}}$$

$$= \frac{r_{b'e}}{1 + j\dfrac{f}{f_\beta}} \text{ where, } f_\beta = \frac{1}{2\pi \cdot r_{b'e}(C_{b'e} + C_{b'c})} \text{ is the } \beta \textit{ cut-off frequency.}$$

Then $I_i = \dfrac{v_{b'e}}{\dfrac{r_{b'e}}{1 + j\dfrac{f}{f_\beta}}}$ (3.182)

Then current gain $A_I = \dfrac{I_L}{I_i} = \dfrac{-g_m v_{b'e}}{v_{b'e}} \dfrac{r_{b'e}}{1 + j\dfrac{f}{f_\beta}}$

$$= \frac{-g_m r_{b'e}}{1 + j\dfrac{f}{f_\beta}} = \frac{-h_{fe}}{1 + j\dfrac{f}{f_\beta}} \quad \text{as } h_{fe} = g_m r_{b'e} \tag{3.183}$$

The β *cut-off frequency* f_β is also represented by $f_{h_{fe}}$ the *CE* short-circuit small-signal forward current transfer ratio cut-off frequency. f_β is the frequency at which the short-circuit current gain of a *CE* transistor drops by 3 dB from its mid-frequency gain.

The short-circuit current gain of a common-base amplifier is

$$A_I = \frac{I_L}{I_i} = \frac{-h_{fb}}{1 + j\dfrac{f}{f_\alpha}} \tag{3.184}$$

where, f_α is α cut-off frequency, $f_\alpha = \dfrac{1}{2\pi \cdot r_{b'e}(1+h_{fb})C_{b'e}} = \dfrac{h_{fe}}{2\pi \cdot r_{b'e}C_{b'e}}$

The relationship between f_β and f_α is

$$f_\alpha = \frac{h_{fe} f_\beta (C_{b'e} + C_{b'c})}{C_{b'e}} \tag{3.185}$$

The f_α is α *cut-off frequency* at which the common-base short-circuit small signal forward-current transfer ratio A_I has dropped by 3 dB from its value at low frequency. The gain A_I vs frequency plot and the f_β for a common-emitter amplifier and f_α for a common-base amplifier are depicted in Fig. 3.122.

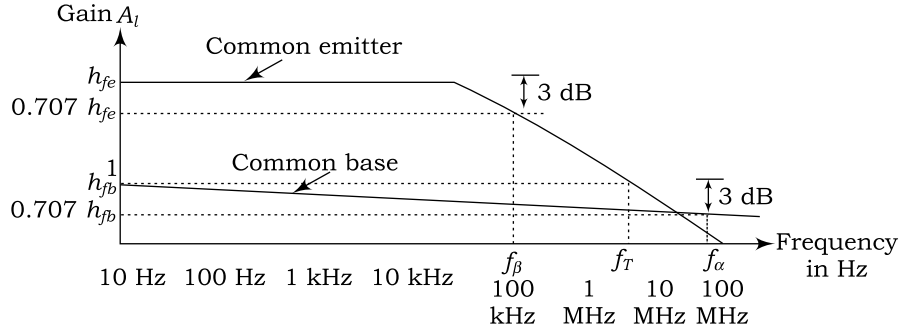


Fig. 3.122 Gain A_I vs frequency plot for common-emitter and common-base amplifiers

The short-circuit *CE* current gain is $|A_I| = \left|\dfrac{-h_{fe}}{1 + j\dfrac{f}{f_\beta}}\right|, = \dfrac{h_{fe}}{\sqrt{1 + \left(\dfrac{f}{f_\beta}\right)^2}}$ (3.186)

At $f = f_T, |A_I| = 1, f_T << f_\alpha$ and $f_T >> f_\beta$. As $\dfrac{f_T}{f_\beta} >> 1, 1 = \dfrac{h_{fe}}{\dfrac{f_T}{f_\beta}}$, and $f_T = h_{fe} f_\beta$

Hence, f_T is the product of low-frequency current gain h_{fe} and β cut-off frequency f_β.
In the same way, we can prove that $f_T = h_{fb} f_\alpha$.

3.28 HIGH-FREQUENCY CURRENT GAIN WITH RESISTIVE LOAD

Figure 3.123 shows the high-frequency equivalent circuit of *CE* amplifier with resistive load. By using Miller's theorem, Fig. 3.95 will be represented by Fig. 3.124.

The voltage gain $A = \dfrac{V_{CE}}{V_{b'e}} = \dfrac{-g_m V_{b'e} R_L}{V_{b'e}} = -g_m R_L$ (3.187)

Then $(1 - A) = 1 + g_m R_L$. When Miller's theorem is used, the impedance at input is decreased by a factor $(1 - A)$ and the capacitance is increased by a factor $(1 - A)$ or $1 + g_m R_L$.

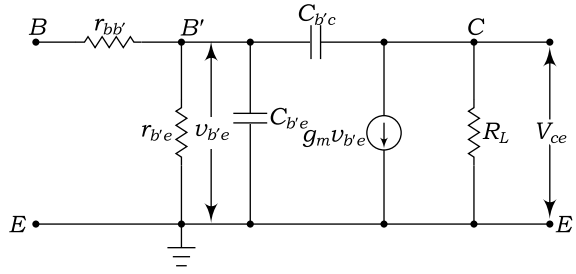


Fig. 3.123 High-frequency equivalent circuit of *CE* amplifier with R_L load

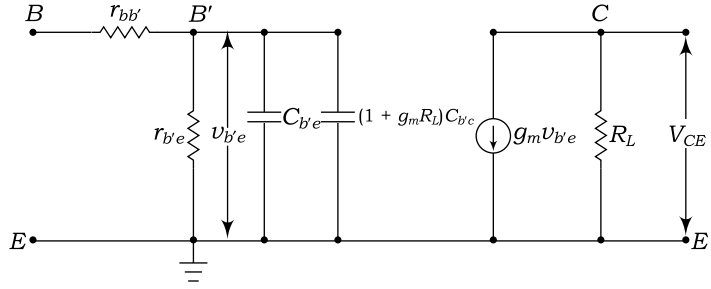


Fig. 3.124 Simplified equivalent circuit of Fig. 3.123 using Miller's theorem

Then total capacitance between B' and E is equal to $C = C_{b'c} + (1 + g_m R_L)C_{b'c}$

The upper 3 dB frequency is $f_2 = \dfrac{1}{2\pi r_{b'e} C}$

Due to increase the value of C, f_2 is lower than that determined for f_β. When the source resistance R_S is present in the circuit, the upper 3 dB frequency is given by

$$f_2 = \frac{1}{2\pi R' C} \text{ where, } R' = (R_S + r_{bb'}) \| r_{b'e} = \frac{(R_S + r_{bb'}) r_{b'e}}{R_S + r_{bb'} + r_{b'e}} = \frac{(R_S + r_{bb'}) r_{b'e}}{R_S + h_{ie}} \text{ as } h_{ie} = r_{bb'} + r_{b'e} \quad (3.188)$$

When the effect of biasing resistance R_1 and R_2 are incorporated, the $R' = \dfrac{(R'_S + r_{bb'}) r_{b'e}}{R'_S + h_{ie}}$ where, $R'_S = R_S \| R_B$ and $R_B = R_1 \| R_2$.

Hence, the source resistance R_S and biasing resistance R_1 and R_2 have an effect on the upper 3 dB frequency f_2.

Example 3.15 If the midband gain of an amplifier is 100 and if the half-power frequencies are $f_1 = 40$ Hz and $f_2 = 16$ kHz, calculate the amplifier gain at the frequencies of 20 Hz and 20 kHz.

Sol. Given: $A_{v(\text{mid})} = 100, f_1 = 40$ Hz, $f_2 = 16$ kHz

Amplifier gain at the frequency of 20 Hz $A_{V(\text{low})} = \dfrac{A_{V(\text{mid})}}{\sqrt{1 + \left(\dfrac{f_1}{f}\right)^2}} = \dfrac{100}{\sqrt{1 + \left(\dfrac{40}{20}\right)^2}} = 44.72$

Amplifier gain at the frequency of 20 kHz $A_{V(\text{high})} = \dfrac{A_{V(\text{mid})}}{\sqrt{1+\left(\dfrac{f}{f_2}\right)^2}} = \dfrac{100}{\sqrt{1+\left(\dfrac{20}{16}\right)^2}} = 62.46$

Example 3.16 If the voltage gain of an amplifier reduces from 200 to 141.4 at a frequency of 35 Hz and if upper half-power frequency is 18 kHz, what is the BW of the amplifier? Calculate the gain of the amplifier at 20 Hz and 20 kHz. What should be the minimum value of the input coupling capacitor if the total series resistance is 9 kΩ (reactance to be approximately 10% of the total series resistance)?

Sol. Given: $f_H = f_2 = 18$ kHz, $A_{v(\text{mid})} = 200$

The voltage gain reduces to 0.707 times of the midband gain at half-power frequency.

Since the voltage gain of an amplifier reduces from 200 to 141.4 at a frequency of 35 Hz, $f_L = f_1 = 35$ Hz

Bandwidth $BW = f_H - f_L = f_2 - f_1 = 18 \times 10^3 - 35 = 17965$ Hz

Gain at $f = 20$ Hz, $A_{V(\text{low})} = \dfrac{A_{V(\text{mid})}}{\sqrt{1+\left(\dfrac{f_1}{f}\right)^2}} = \dfrac{200}{\sqrt{1+\left(\dfrac{35}{20}\right)^2}} = 99.228$

Gain at $f = 20$ kHz, $A_{V(\text{low})} = \dfrac{A_{V(\text{mid})}}{\sqrt{1+\left(\dfrac{f}{f_2}\right)^2}} = \dfrac{200}{\sqrt{1+\left(\dfrac{20}{18}\right)^2}} = 133.79$

The value of capacitance reactance X_{C1} is one-tenth of the total series resistance.

$$X_{C1} = 0.1R = 0.1 \times 9 \times 10^3\,\Omega = 900\,\Omega$$

$$X_{C1} = \frac{1}{2\pi f C_1} = 900\,\Omega \text{ or, } C_1 = \frac{1}{2\pi \times 20 \times 900} = 8.846 \times 10^{-6}\,\text{F} = 8.846\,\mu\text{F}$$

Example 3.17 Two-stage amplifier circuits are shown in Fig. 1.125 Calculate overall voltage gain A_v. Take $h_{ie} = 2.2k$, $h_{fe} = 60$, $h_{re} = 2.5 \times 10^{-4}$, $h_{oe} = 2.5\,\mu$A/V, $R_C = 5$ kΩ, $R_E = 4.7$ kΩ, $R_S = 1$ kΩ, $V_{CC} = 12$ V

Sol. Analysis of common-collector amplifier:

$$R_{L2} = R_E = 4.7\,\text{k}\Omega,\ h_{oc} = h_{oe} = 2.5\,\mu\text{A/V},\ h_{oc}R_{L2} = 2.5 \times 10^{-6} \times 4.7 \times 10^3 = 0.01175$$

$$A_{i2} = -h_{fe} = -[-(1+h_{fe})] = (1+h_{fe}) = 1 + 60 = 61$$

Input resistance $R_{i2} = h_{ie} + A_{i2}h_{re}R_{L2} = 2.2k + 61 \times 1 \times 4.7k = 288.9k$

Voltage gain $A_{v2} = (1+h_{fe})\dfrac{R_{L2}}{R_{i2}} = (1+60)\dfrac{4.7}{288.9} = 0.9923$

$$R_{L1} = R_{C1} \parallel R_{i2} = 5k \parallel 288.9k = 4.914k$$

$$h_{oe}R_{L1} = 2.5 \times 10^{-6} \times 4.914 \times 10^3 = 12.285 \times 10^{-3}$$

As $h_{oe}R_{L1} < 0.1$, approximate analysis will be done for the stage I.

Current gain $A_{i1} = -h_{fe} = -60$, input resistance $R_{i1} = h_{ie} = 2.2k$

Voltage gain $A_{v1} = -h_{fe}\dfrac{R_{L1}}{R_{i1}} = -60 \times \dfrac{5k}{2.2k} = -136.36$

Output voltage gain

$A_v = A_{v1} \times A_{v2} = -136.36 \times 0.9923 = -135.31$

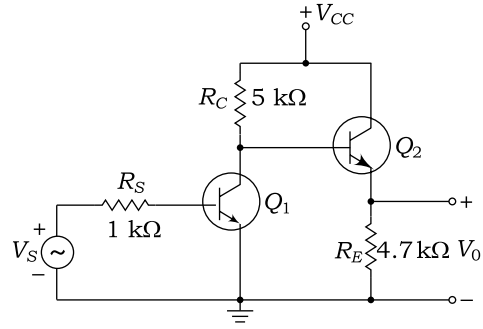


Fig. 1.125

Example 3.18 An *RC* coupled amplifier has a midband frequency gain of 400 and lower and upper 3 dB frequencies of 100 Hz and 10 kHz. A negative feedback with $\beta = 0.01$ is incorporated in the amplifier circuit. Find the gain with feedback and new bandwidth with feedback.

Sol. Given A = 400, f_1 = 100 Hz, f_2 = 10 kHz, $\beta = 0.01$

The gain with feedback $A_f = \dfrac{A}{1+\beta A} = \dfrac{400}{1+0.01\times 400} = 80$

Lower cut-off frequency with feedback is

$$f_{lf} = \frac{f_1}{1+\beta A} = \frac{100}{1+0.01\times 400} = \frac{100}{5}\text{Hz} = 20\text{ Hz}$$

The upper cut-off frequency with feedback is

$$f_{2f} = f_1(1+\beta A) = 10\times 10^3(1+0.01\times 400) = 50\text{ kHz}$$

Bandwidth $BW = f_{2f} - f_{1f} = 50\text{ kHz} - 20\text{ Hz} = 49.98\text{ kHz}$

3.29 WIDE BAND AMPLIFIER

The amplification factor of an amplifier is frequency dependent and decreases with frequency above some upper frequency limit. It is asymptotically to –20 dB/10*f* and its nature is just like a first order low pass system.

In communications, a system is wide band when the message bandwidth significantly exceeds the coherence bandwidth of the channel. The wide band amplifier is commonly used in high-speed measurement instrumentation and data acquisition, telecommunications and radio frequency engineering, and high-quality audio and video amplifier.

Figure 3.126 shows a circuit diagram of a common base amplifier. If the voltage gain is not too high, the base emitter capacitance C_π is the dominant and the frequency response is rolling off at high frequencies.

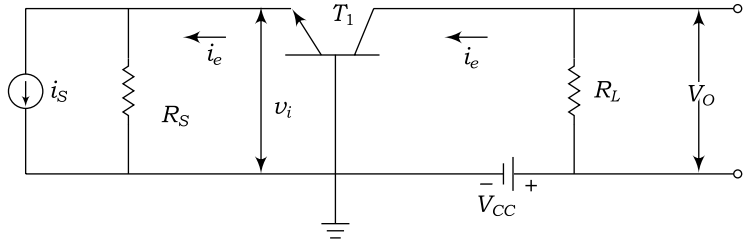


Fig. 3.126 Common base amplifier

The small signal high frequency model of common base amplifier is shown in Fig. 3.127. In this circuit, i_c, i_e and i_b are the collector current, emitter current and base current respectively. The dc current amplification factor is

$$\alpha_o = \frac{I_c}{I_e}$$

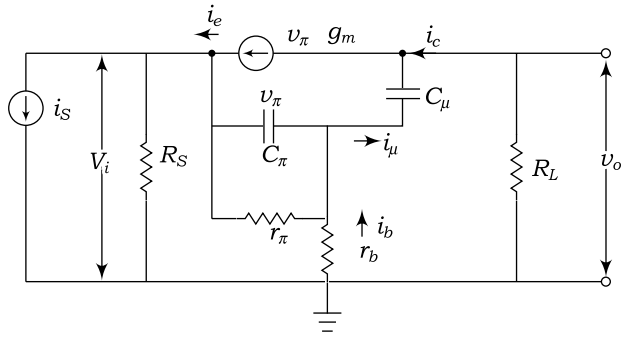


Fig. 3.127 High frequency small signal equivalent circuit of common base amplifier

The mutual conductance is

$$g_m = \frac{\alpha_o}{r_e} = \frac{\beta_o}{(1+\beta_o)r_e}$$

where β_o is the common emitter dc current amplification factor.

When $\beta_o >> 1$, $\alpha_o \cong 1$ and the collector current is almost equal to the emitter current I_e and $g_m \cong \frac{1}{r_e}$ as $\alpha_o = 1$

Assume $r_b = 0$. Then input resistance is equal to

$$r_\pi = \frac{v_\pi}{i_b}$$

where v_π is the base to emitter voltage

The emitter current is

$$i_e = i_b + i_c = i_b + \beta_o i_b = (1 + \beta_o) i_b$$

The base current is

$$i_b = \frac{i_e}{1+\beta_o}$$

Therefore, $r_\pi = \frac{v_\pi}{i_b} = \frac{v_\pi(1+\beta_o)}{i_e} = r_e\,(1 + \beta_o) \approx \beta_o r_e$ as $\beta_o >> 1$

To determine the input impedance at high frequencies the parallel connection of C_π must be used in computation, then

$$Z_b = \frac{(1+\beta_o)r_e}{1+(1+\beta_o)sC_\pi r_e}$$

The base current is equal to

$$i_b = \frac{v_\pi}{Z_b} = v_\pi \cdot \frac{1 + (1+\beta_o) s C_\pi r_e}{(1+\beta_0) r_e}$$

Therefore,

$$v_\pi = i_b \cdot \frac{(1+\beta_o) r_e}{1 + (1+\beta_o) s C_\pi r_e}$$

The collector current is

$$i_c = g_m v_\pi = \frac{\beta_o}{1+\beta_o} \cdot \frac{1}{r_e} v_\pi = \frac{\alpha_o}{r_e} v_\pi$$

After substituting the value of v_π in the above equation, we obtain

$$i_e = i_b \cdot \frac{\beta_o}{1+\beta_o} \cdot \frac{1}{r_e} \cdot \frac{(1+\beta_o) r_e}{1 + s(1+\beta_o) r_e C_\pi}$$

$$= i_b \cdot \frac{1}{\frac{1}{\beta_o} + s\left(\frac{\beta_o + 1}{\beta_o}\right) r_e C_\pi}$$

$$\cong i_b \cdot \frac{1}{\frac{1}{\beta_o} + s\tau_T} \text{ as } \beta_o >> 1$$

where $\tau_T = r_e C_\pi = \dfrac{1}{\omega_T}$ and $\omega_T = 2\pi f_T$

ω_T is the angular frequency at which current amplification factor β decreases to unity. Figure 3.128 shows the frequency dependence of β and the equivalent high frequency current generator is shown in Fig. 3.129.

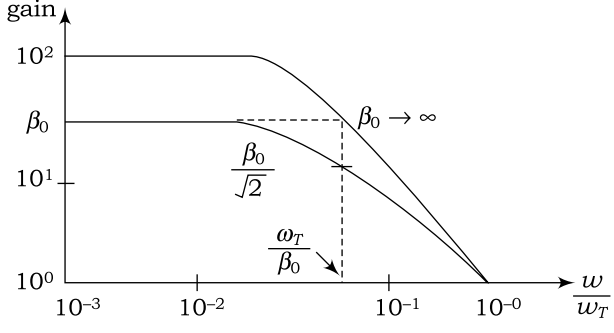


Fig. 3.128 Transistor gain is function of frequency

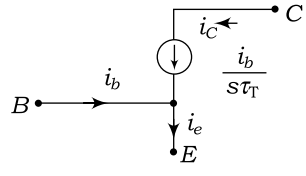


Fig. 3.129 Equivalent circuit of high frequency current generator

The collector current to base current ratio is equal to

$$\frac{i_c}{i_b} \approx \beta_o \cdot \frac{-\omega_T/\beta_o}{s - \left(\frac{-\omega_T}{\beta_o}\right)} = \beta_o \frac{-s_1}{s - s_1}$$

where, $s_1 = -\dfrac{\omega_T}{\beta_o}$

At very high frequencies, $\beta_o >> 1$ and the term $S\gamma_T$ prevails.

Then $$\frac{i_c}{i_b} = \beta(s) \approx \frac{1}{s\tau_T} = \frac{1}{j\omega\, r_e\, C_\pi}$$

It is clear from above equation that β is decreasing with frequency. At $\omega = \omega_T$, the current ratio $\frac{i_c}{i_b} = 1$ and the capacitance

$$C_\pi = \frac{1}{\omega_T r_e}$$

The simplified relation $\beta(s) = \frac{1}{j\omega r_e C_\pi}$ represents the –20 dB/10*f* asymptote as shown in Fig. 3.128.

Review Exercises

Short-Answer Questions

1. Define an amplifier.

Ans. An amplifier is an electronic circuit that increases the amplitude of applied input signal, i.e., current, voltage or power.

2. What is small-signal amplifier?

Ans. When the input signal of an amplifier is relatively weak and generates amplified output signal, i.e. small fluctuation in the output signal with respect to quiescent (*Q*) point value, the amplifier is called a small-signal amplifier or voltage amplifier.

3. What is ac emitter resistance?

Ans. The dynamic resistance of emitter-base junction diode of a BJT is called ac emitter resistance and it value is equal to $r_e = \frac{25\text{ mV}}{I_E}$ where, I_E is dc emitter current at *Q*-point.

4. What is the effect of emitter resistance and emitter bypass capacitor in a CE amplifier? What happenes when the emitter bypass capacitor is removed from a CE amplifier?

Ans. When an emitter resistance is added in a *CE* amplifier, its voltage gain is reduced but the input impedance increases. When a bypass capacitor is connected in parallel with an emitter resistance, voltage gain of *CE* amplifier increases.

If the bypass capacitor is removed, excessive degeneration produced in the amplifier circuit and voltage gain will be reduced.

5. Why is a common-collector amplifier circuit called an emitter follower?

Ans. In a common-collector amplifier circuit, the output voltage at the emitter terminal follows the applied input signal at the base terminal. Therefore, a common-collector amplifier circuit is called emitter follower.

6. What is distortion in an amplifier? Why is distortion in an amplifier not permissible?

Ans. The change in amplified output signal waveform with respect to input signal is called distortion. The distortion in amplifier is not permissible as distortion changes the actual information.

7. What is transconductance?

Ans. The term $\frac{I_{CQ}}{V_T}$ is conductance, which relates the collector current and base-emitter voltage. This parameter is called transconductance and can be expressed as $g_m = \frac{I_{CQ}}{V_T}$ where the quiescent collector current is I_{CQ}.

8. Define ac beta and dc beta.

Ans. The common-emitter current gain is actually defined as an ac beta and it is the ratio of ac collector current to ac base current. It is represented by $\beta = \frac{i_c}{i_b}$.

β_{dc} is the ratio of a dc collector current (I_C) to the corresponding dc base current (I_B) and it is represented by $\beta_{dc} = \frac{I_C}{I_B}$.

9. What is time constant (τ) of an RC circuit?

Ans. The time constant of the *RC* circuit is the time required for the transient output to reach 0.632 times of its final value. It is represented by τ and it is expressed as $\tau = RC$.

10. What is rise time t_r?

Ans. This is the time required for a output voltage waveform to change from 10% to 90% of its final value. It is represented by t_r. The relationship between rise time and bandwidth is $t_r = \frac{0.35}{\text{Bandwidth}}\text{s}$.

11. What is -3 dB frequency?

Ans. This is frequency at which the power is reduced to one-half of the maximum power.

12. What is bandwidth?

Ans. This is the difference between lower –3 dB frequency and upper –3 dB frequency. Bandwidth = $f_H - f_L$.

13. Define beta cut-off and alpha cut-off frequencies. Write the relationship between f_α and f_β.

Ans. The beta cut-off frequency f_β is defined as the frequency at which, common emitter current gain h_{fe} drops to 0.707 times of its low-frequency value. The alpha cut-off frequency f_α is defined as the frequency at which common-base current gain h_{fb} drops to 0.707 times of its low-frequency value.

The relation between f_α and f_β is $f_\alpha = \frac{h_{fe} f_\beta (C_{b'e} + C_{b'c})}{C_{b'e}}$ or $f_\beta = (1 - \alpha_0) f_\alpha$.

14. If h_{fe} = 50 and f_β = 20 MHz, what is f_T or gain bandwidth product?

Ans. $f_T = h_{fe} f_\beta = 50 \times 20$ MHz = 1000 MHz.

15. What is Miller's theorem?

Ans. Refer to Section 3.17.

16. What is the effect of coupling capacitor on voltage gain of an amplifier?

Ans. At mid-frequency and high frequency, capacitive reactance of coupling capacitor is very small and coupling capacitor behaves as short circuit. At low frequency, capacitive reactance of coupling capacitor has significant value and some voltage drops across them and voltage gain is reduced.

17. What is the effect of bypass capacitor on voltage gain of an amplifier?

Ans. The emitter bypass capacitor is connected across emitter resistance R_E. At mid-frequency and high frequency, bypass capacitor provides very small capacitive reactance and this capacitor behaves as short circuit. Hence, R_E is bypassed and bypass capacitor has no effect on voltage gain. At low frequency, capacitive reactance of a bypass capacitor has significant value and there is some voltage drops across R_E and C_E and voltage gain is reduced.

18. Why are amplifiers connected in cascade?

Ans. The voltage gain or power gain or frequency response of single-stage amplifier is not sufficient to meet the requirement of a load. Therefore, the cascade connection of amplifiers is needed to provide better voltage gain or power gain or frequency response or all of them.

19. Which transistor configuration is most commonly used for multistage or cascade amplifier?

Ans. Due to high voltage gain, common-emitter transistor configuration is most commonly used for multistage or cascade amplifier.

20. Why is coupling capacitor in a CE, RC coupled amplifier called blocking capacitor?

Ans. The coupling capacitor can only bypass ac signal but it blocks the dc voltage of the first stage from reaching the next stage, so that it is called the blocking capacitor.

21. Why is gain of RC coupled amplifier constant in mid-frequency range?

Ans. In mid-frequency range, the reactance of coupling capacitor decreases and the gain increases. On the other hand, due to low capacitive reactance, there will be higher loading effect and gain will be reduced. As the two different effects neutralise each other, gain of *RC* coupled amplifier is constant in mid-frequency range.

22. Why is a bypass capacitor used at the bottom of each secondary winding in a transformer-coupled amplifier?

Ans. A bypass capacitor is used at the bottom of each secondary winding in a transformer-coupled amplifier to provide ac ground and to prevent the loss of signal power in the biasing transistors.

23. What are the main features of cascade amplifier?

Ans. A cascade amplifier has high input impedance, same voltage gain as that of a *CE* amplifier, and very good performance at high frequency operation.

24. Why is direct coupling not suitable for high-frequency signal amplification?

Ans. At high frequency, the gain of direct-coupled amplifier drops significantly due to inter-electrode capacitances of BJT. Therefore, direct coupling is not suitable for high-frequency signal amplification.

Multiple-Choice Questions

1. In a common-emitter amplifier circuit with emitter feedback, the input impedance is equal to

   (a) h_{fe} (b) R_E (c) $\frac{h_{fe}}{R_E}$ (d) $h_{fe}R_E$

2. The current gain of a common-base amplifier is

   (a) less than unity (b) greater than unity
   (c) unity (d) zero

3. In a common-base amplifier, input impedance (R_i) is _____ and output impedance (R_o) is _____.

   (a) low, high (b) high, low (c) low, high (d) high, high

4. The current gain of an emitter follower is
   (a) less than unity (b) greater than unity
   (c) unity (d) zero
5. _____ amplifier circuit has highest voltage gain.
   (a) Common-emitter (b) Common base
   (c) Common-collector (d) None of these
6. The main application of a common-collector or emitter follower circuit is
   (a) impedance matching (b) low impedance circuit
   (c) power amplifier (d) None of these
7. The voltage gain of single-stage *CE* amplifier is
   (a) $A_v = -\frac{r_L}{r_e}$ (b) $A_v = -\frac{r_e}{r_L}$
   (c) $A_v = -r_e r_L$ (d) $A_v = -r_L$
8. The voltage gain of a single-stage *CE* amplifier increases with
   (a) increase in ac load resistance
   (b) decrease in ac load resistance
   (c) increase in source resistance
   (d) increase r_e
9. If the emitter bypass capacitor is removed from a *CE* amplifier circuit, _____ is decreased significantly.
   (a) current gain (b) voltage gain
   (c) input impedance (d) output impedance
10. The normalised gain of an amplifier is
    (a) $\frac{A_v}{A_{\text{mid}}}$ (b) A_v (c) $A_{v\text{mid}}$ (d) $20 \log \frac{A_v}{A_{v\text{mid}}}$
11. In a single-stage *RC* coupled *CE* amplifier, the phase-shift at the lower and upper 3 dB frequencies are
    (a) 45°, 135° (b) 45°, 225° (c) 90°, 180° (d) 45°, 180°
12. The gain of a BJT drops at high frequencies due to
    (a) coupling and bypass capacitor
    (b) inter-electrode transistor capacitances
    (c) coupling and bypass capacitor and inter-electrode transistor capacitances
    (d) early effect
13. The gain of a BJT drops at low frequencies due to
    (a) coupling and bypass capacitor
    (b) inter-electrode transistor capacitances
    (c) coupling and bypass capacitor and inter-electrode transistor capacitances
    (d) early effect

14. In the hybrid-π model for CE transistor configuration, $r_{b'b'}$ is
    (a) bias resistance
    (b) base spreading resistance
    (c) resistance due to increased recombination base current
    (d) base resistance
15. In a cascade amplifier, the intermediate stage is
    (a) *CE* (b) *CB* (c) *CC* (d) None of these
16. In an *RC* coupled common-emitter amplifier,
    (a) coupling capacitor affects high-frequency response and bypass capacitor affects low-frequency response
    (b) coupling capacitor and bypass capacitor affect low-frequency response
    (c) coupling capacitor affects low-frequency response and bypass capacitor affects high-frequency response
    (d) coupling capacitor and bypass capacitor affect high-frequency response
17. The overall bandwidth of two identical voltage amplifiers connected in cascade will be
    (a) same as single stage
    (b) better than single stage
    (c) worse than single stage
    (d) better if stage gain is low and worse if stage gain is high.
18. The major advantages of a direct-coupled amplifier is that it
    (a) uses less number of components
    (b) has very good temperature stability
    (c) can amplify direct current and low frequency signals
    (d) does not use frequency sensitive components
19. A transformer-coupled amplifier provide
    (a) impedance matching (b) maximum voltage gain
    (c) maximum current gain (d) large bandwidth
20. A Darlington amplifier has
    (a) a large current gain and high input resistance
    (b) a large voltage gain and low output resistance
    (c) a small voltage gain and low input resistance
    (d) a small current gain and high output resistance
21. A Darlington pair consists of two stages:
    (a) *CE* and *CB* (b) *CE* and *CC* (c) Both *CC* (d) Both *CE*
22. A Darlington pair is used for
    (a) wideband voltage amplification (b) impedance matching
    (c) reducing distortion (d) power amplification

23. Cascade amplifiers are used for
    (a) voltage amplification (b) video amplifiers
    (c) power amplifiers (d) tuned amplifier
24. Which BJT amplifier has highest input impedance and least voltage gain?
    (a) *CE* (b) *CB* (c) *CC* (d) None of these

Review Questions

1. Define amplifier. Write the difference between linear and nonlinear amplifier.
2. What are the types of amplifier based on configuration, coupling, input signal and operating condition?
3. Explain BJT as a linear amplifier.
4. Draw small-signal hybrid-π equivalent circuit of an *NPN* transistor. Derive the expression for small-signal voltage gain.
5. What is ac resistance of base emitter junction or ac emitter resistance?
6. Draw the circuit diagram of a *CE* amplifier and explain its working principle.
7. Draw the small-signal ac equivalent circuit of a *CE* amplifier with fixed bias using *h* model and r_e model. Derive the equations for voltage gain, current gain, input impedance and output impedance.
8. Draw the circuit diagram of *CB* amplifier and explain its working principle.
9. Draw the small-signal ac equivalent circuit of a *CB* amplifier using *h* model and r_e model. Derive the equations for voltage gain, current gain, input impedance and output impedance.
10. Draw the circuit diagram of *CB* amplifier and explain its working principle.
11. Draw the small-signal ac equivalent circuit of a *CC* amplifier using *h* model and r_e model. Derive the equations for voltage gain, current gain, input impedance and output impedance.
12. Compare the performance between *CE*, *CB* and *CC* amplifiers.
13. What is an emitter follower? Explain briefly.
14. Write a short note on cascode amplifier.
15. What is Darlington connector transistor? What are the important features of a Darlington transistor?
16. Draw the biasing circuit of a Darlington emitter-follower circuit. Derive the expressions for voltage gain, current gain, input impedance and output impedance.
17. Define half-power frequencies. Justify the statement "The cut-off frequencies of a single stage BJT amplifier are affected by *R* and *C*".
18. What is Bode plot? Derive the lower cut-off frequency for *RC* network and draw the Bode plot.
19. Explain the effect of a bypass capacitor at low-frequency response of a BJT amplifier.
20. Discuss the effect of a coupling capacitor at low-frequency response of a BJT amplifier.
21. Draw the high-frequency π model of a BJT and explain briefly. Derive the expression of α cut-off and β cut-off frequencies.
22. Explain Miller's theorem with a suitable example.
23. Discuss Dual of Miller's theorem with a suitable example.
24. Prove that the common-emitter short-circuit current gain is function of frequency.
25. Define f_β, f_α and f_T. Define gain-bandwidth product.

26. Draw gain A_I vs frequency plot for common-emitter and common-base amplifier indicating f_β, f_α and f_T.
27. What is a multistage amplifier? Derive the equation for voltage gain, current gain and power gain of multistage amplifier.
28. What are the different methods of cascading amplifiers? Explain any two methods.
29. Draw a circuit diagram of a two-stage *RC* coupled BJT amplifier. Draw the frequency response of an *RC* coupled amplifier.
30. Draw the equivalent circuit of an *RC* coupled amplifier in mid-frequency, low-frequency and high-frequency range. Derive the voltage gain, current gain, lower 3 dB frequency f_L and upper 3 dB frequency f_H.
31. Draw the equivalent circuit of a transformer-coupled amplifier in mid-frequency, low-frequency and high-frequency range. Draw the frequency response of a transformer-coupled amplifier.
32. What is a direct-coupled amplifier? Write applications of a direct-coupled amplifier.
33. What is the difference between *RC* coupled amplifier and direct-coupled amplifier?
34. Why is a large-signal amplifier called power amplifier? Write the difference between voltage amplifier and power amplifier.
35. Draw the small-signal high frequency CE model of a transistor. What are the physical origin of the two capacitors in the hybrid-π model?
36. What is Miller capacitor?
37. Obtain expressions for
    (i) short circuit current gain and
    (ii) f_T for a CE amplifier using high frequency hybrid-π model.
38. What is Miller Effect? When it is a factor to take into consideration? What effect does it have on high frequency gain?
39. The following low frequency parameters are known for a given transistor at room temperature and at $I_C = 10$ mA and $V_{CE} = 10$ V. Assume $h_{ie} = 500\ \Omega$, $h_{oe} = 4 \times 10^{-5}$ A/V, $h_{fe} = 100$ and $h_{re} = 10^{-4}$. At the same operating point $f_T = 50$ mHz and $C_b = 3$ pf. Compute the values of all the hybrid-π parameters.
40. Write short notes on the following:
    (i) Low frequency model of BJT
    (ii) High frequency model of BJT

ANSWERS

Multiple-Choice Questions

1. (d)	2. (a)	3. (a)	4. (b)	5. (a)	6. (a)	7. (a)
8. (a)	9. (b)	10. (a)	11. (b)	12. (b)	13. (a)	14. (b)
15. (a)	16. (b)	17. (c)	18. (c)	19. (a)	20. (a)	21. (c)
22. (d)	23 (c)	24. (c)				

CHAPTER

4
Feedback Amplifier

4.1 INTRODUCTION

Usually, amplifier circuits are used in signal-processing systems to provide good voltage gain. Therefore, amplifier circuits are known as voltage amplifiers. The example of an amplifier circuit is audio amplifiers. The simplified block diagram of an audio amplifier is shown in Fig. 4.1, which consists of microphone, small signal amplifiers, large-signal amplifiers and speaker. The microphone generates a very small-signal, in millivolt range, which is fed to *small-signal* voltage amplifiers. The first two stages (small signal stages) of an amplifier are used to amplify the small voltage audio signal, thus increasing the voltage level but decreasing the current level. The output of the small signal-stage amplifier is fed to the last-stage amplifier, which is known as *power amplifier*. The power amplifiers can handle large voltage and current swings as it has larger power gain and high efficiency.

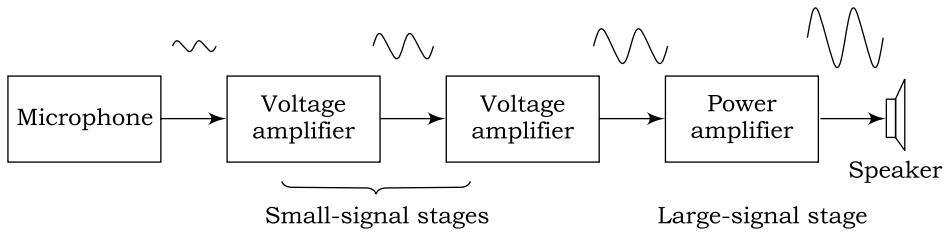


Fig. 4.1 Block diagram of audio amplifier

Due to changes in ambient temperature, device (BJT or FET) parameters are varied. Therefore, gain stability of practical amplifiers is not very high. In case of BJT amplifier circuits, this problem is very acute. The gain stability can be moderately improved by using feedback technique. The feedback in amplifiers gives better performance in different ways such as

1. Increased stability in the amplification. (the gain is less dependent on device parameters)
2. Higher input impedance
3. Lower output impedance
4. Feedback reduces distortion in the amplifier
5. Bandwidth of the amplifier is increased (improved frequency response)
6. Linear operation over a wide range

The above advantages are achieved at the expense of gain, which is much less than the amplifier gain without feedback. The other disadvantages of feedback amplifiers are the following:

1. The feedback amplifier may lead to instability if it is not designed properly.
2. Gain of the amplifier decreases.
3. Input and output impedances of feedback amplifier are sensitive with open-loop gain of amplifier and parameter variations.

In this chapter, basic concept of feedback amplifier, positive and negative feedback, topologies of feedback amplifier, effect of feedback on gain, input impedance, output impedance, sensitivities, bandwidth stability and applications of feedback amplifiers are discussed elaborately.

4.2 FEEDBACK AMPLIFIER

A feedback amplifier is an electronic circuit in which the output signal is sampled and feedbacked to the input to generate an error signal, which drives the amplifier. Generally, feedback amplifiers are of two types as given below:

- Negative feedback amplifier
- Positive feedback amplifier

4.2.1 Negative Feedback Amplifier

Figure 4.2 shows the basic block diagram of a negative feedback amplifier (non-inverting type amplifier).

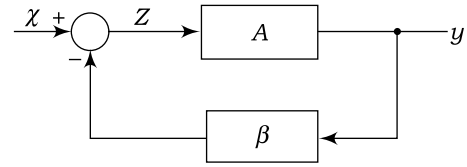


Fig. 4.2 Negative feedback amplifier (non-inverting type)

Here, x is the input signal,
y is the output signal,
z is the error signal,
A is amplifier gain, and
β is the gain of feedback path.

Depending on the type of feedback, the variables x, y and z are used for voltages or currents. The gain around the loop is negative and it is equal to $-\beta A$ where, both A and β are positive real constants. Due to the loop gain being negative, the feedback is called *negative feedback*.

The output of feedback is $-\beta \cdot y$.

The error signal can be computed as $z = x - \beta \cdot y$

Then output signal is $y = A \cdot z = A(x - \beta \cdot y)$

The overall gain is equal to $A_f = \dfrac{y}{x} = \dfrac{A}{1 + \beta \cdot A}$

where, A is the gain without feedback or open-loop gain, and
A_f is the gain of amplifier with feedback or closed-loop gain.

It is justified from the above expression that the effect of the feedback is to reduce the gain by the factor $(1 + \beta A)$. This factor is known as "*amount of feedback*". Commonly it is specified in decibel (dB) by the relation $20 \log |1 + \beta A|$.

The amount of feedback is expressed by the following relationship as given below:

$$\text{Amount of feedback in dB} = 20 \log_{10} \left| \frac{A_f}{A} \right| = 20 \log_{10} \left| \frac{1}{1 + \beta A} \right| \tag{4.1}$$

In negative feedback, the amount of feedback is negative as $|1 + \beta A| > 1$, but during positive feedback, the amount of feedback is positive as $|1 + \beta A| < 1$.

The basic block diagram of an inverting feedback amplifier is depicted in Fig. 4.3. In this figure, x is the input signal, y is the output signal, and z is the error signal. The gain around the loop is negative and it is equal to $-\beta A$ where both A and β are positive real constants. As the loop gain is negative, the feedback is said to negative.

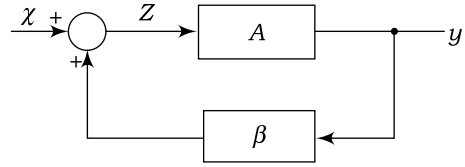


Fig. 4.3 Negative feedback amplifier (inverting type)

This amplifier has an inverting gain, and the feedback signal must be added to the input signal to determine error signal.

The output of feedback is $\beta \cdot y$.

In the inverting amplifier, the error signal is $z = x + \beta \cdot y$. If x is positive and y is negative, so that the error signal represents a difference signal.

Then output signal will be $y = -A \cdot z = -A(x + \beta \cdot y)$

Then overall gain will be $A_f = \dfrac{y}{x} = \dfrac{-A}{1 + \beta \cdot A}$

Hence, the amount of feedback for inverting amplifier is the same as for the non-inverting amplifier.

When A is very large, $\beta A >> 1$, the gain of the negative (non-inverting type) amplifier is about

$$A_f = \frac{y}{x} \cong \frac{A}{\beta \cdot A} = \frac{1}{\beta}$$

The gain of the inverting type amplifier is approximated by

$$A_f = \frac{y}{x} \cong \frac{-A}{\beta \cdot A} = -\frac{1}{\beta} \tag{4.2}$$

Therefore, the gain is set by the feedback network and not by the amplifier. The amplifier without feedback can be designed with high gain. However, when feedback is added, the gain can be reduced to any desired value by the feedback circuit.

4.2.2 Positive Feedback Amplifier

The basic block diagram of a positive feedback amplifier is depicted in Fig. 4.4. In this figure, x is the input signal, y is the output signal and z is the error signal. The gain around the loop is positive and it is equal to βA where, both A and β are positive real constants. The amplifier has positive feedback, which causes it to be unstable. This amplifier has a gain A, and the feedback signal must be added to the input signal to determine error signal.

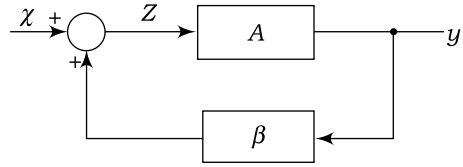


Fig. 4.4 Positive feedback amplifier

The output of feedback is $\beta \cdot y$.

The error signal can be computed as $z = x + \beta \cdot y$

Then output signal is $y = A \cdot z = A(x + \beta \cdot y)$

The overall gain is equal to $A_f = \dfrac{y}{x} = \dfrac{A}{1 - \beta \cdot A}$ (4.3)

In the positive feedback amplifier, the error signal is $z = x + \beta \cdot y$. If x is positive and y is negative, the error signal represents a difference signal.

When A is the voltage gain (Output Voltage/ Input Voltage) or A is the current gain (Output Current/ Input Current), the product βA is dimensionless and β is also dimensionless. If A is the transconductance

gain (Output Current/Input Voltage), β has the units of ohms (Ω). When A is the transresistance gain (Output Voltage/Input Current), the units of β will be siemens (Ω^{-1}). Actually, the gains are phasor functions of frequency. This creates a stability problem in a feedback amplifier. If frequency is increased, absolute value of $|A|$ must be decreased as each amplifier has a finite bandwidth. Therefore, the decrease in $|A|$ go along with a phase shift so that βA can be a negative real number at some frequency. If $\beta A = -1$ at some frequency, we can say from the expression $A_f = \frac{y}{x} = \frac{A}{1 + \beta \cdot A}$ that the overall gain becomes infinite at that frequency. Therefore, an amplifier with an infinite gain at any frequency can generate a output signal at that frequency without any input signal. Then the amplifier is known as *oscillator*. An amplifier will oscillate if $|\beta A| \geq 1$ at any frequency when βA is a negative real number and the phase of βA will be 180°.

Example 4.1 A power amplifier with a gain of 100 has an output voltage of 12 V. A negative feedback is provided to reduce the gain to 25%. What should be the gain of the feedback path?

Sol. Gain of amplifier $A = 100$

Due to negative feedback, the overall gain is reduced to 25% of actual gain.

$$A_f = 0.25\, A$$

The overall gain $$A_f = \frac{A}{1 + \beta A}$$

Or $$\frac{100}{1 + \beta \times 100} = 0.25 \times 100$$

Then the gain of the feedback path is $\beta = 0.03$.

Example 4.2 A feedback amplifier consists of two amplifying blocks and each amplifying block has a gain of 100.

(a) What should be the gain of the feedback block in order to maintain overall gain to 90?

(b) When the gain of each amplifier block has been reduced to 50% of actual value due to parameter variation, what is the percentage change in the overall gain of the feedback amplifier?

Sol. (a) Two amplifying blocks are connected in cascade and gain of each amplifying block is $A_1 = 100$

The gain of amplifier $A = A_1 \times A_1 = 100 \times 100 = 10^4$

The overall gain of feedback amplifier $A_f = \frac{A}{1 + \beta A} = \frac{10^4}{1 + \beta \times 10^4}$

When $A_f = 90$, $\quad 90 = \frac{10^4}{1 + \beta \times 10^4}$

The gain of the feedback block is $\beta = (10^4 - 90)/(90 \times 10^4) = 0.011011$

(b) When the gain of each amplifier block has been reduced to 50% of actual value, the gain of each amplifier block is $A_1' = 50\% \times A_1 = \frac{50}{100} \times 100 = 50$

New gain of amplifier $A' = A_1' \times A_1' = 50 \times 50 = 2500$

The new overall gain of feedback amplifier

$$A_f' = \frac{A'}{1 + \beta A'} = \frac{50^2}{1 + 0.011011 \times 50^2} = \frac{2500}{28.5275} = 87.634$$

Reduction in overall gain = $A_f - A'_f = 90 - 87.634 = 2.366$

The % change in the overall gain of feedback amplifier

$$= \frac{A_f - A'_f}{A_f} \times 100 = \frac{2.366}{90} \times 100 = 2.62\%$$

Example 4.3 An amplifier provides a gain of $A = 200$

(a) Determine the feedback path gain to provide overall gain of $A_f = 100$

(b) If A is increased by 1%, calculate the new A_f. What is the percentage change in A_f

Sol. (a) Given $A = 200$ and $A_f = 100$

The feedback path gain = β

Overall gain of the system $A_f = \frac{A}{1 + \beta A}$

After substituting the values of A and A_f, we get

$$\frac{200}{1 + \beta \times 200} = 100$$

Then the feedback path gain is $\beta = 100/(200 \times 100) = 0.005$

(b) As A is increased by 1%, the new value of A is $A' = 1.01 \times 200 = 202$

The new value of A_f is $A'_f = \frac{A'}{1 + \beta A'} = \frac{202}{1 + 0.005 \times 202} = 100.4975$

The percentage change in A_f is

$$\frac{A_f - A'_f}{A_f} \times 100$$

$$= \frac{100 - 100.4975}{100} \times 100 = \frac{-0.4975}{100} \times 100 = -0.4975\%$$

Example 4.4 An amplifier has gain of –1000 and feedback of $\beta = -0.1$. If it had a gain change of 10% due to temperature, what will be the change in gain of the feedback amplifier?

Sol. Assume amplifier gain $A = -1000$, feedback path gain $\beta = -0.1$, and change in amplifier gain is $\frac{\partial A}{A} = 10\% = 0.1$

The overall gain of the system is $A_f = \frac{A}{1 + \beta A}$

The rate of change in gain is $\frac{\partial A_f}{\partial A} = \frac{1 + \beta A - \beta A}{(1 + \beta A)^2}$

or $$\partial A_f = \partial A \times \frac{1}{(1 + \beta A)^2}$$

or $$\frac{\partial A_f}{A} = \frac{\frac{\partial A}{A}}{(1 + \beta A)}$$

or
$$\frac{\partial A_f}{A} \times 100 = \frac{\frac{\partial A}{A}}{(1+\beta A)} \times 100$$
$$= \frac{0.1}{1+(-1000)(-0.1)} \times 100 = 0.099\%$$

4.3 CLASSIFICATION OF AMPLIFIERS

To understand the basic concept of feedback, amplifiers are classified into four different categories such as

1. Voltage amplifiers
2. Current amplifiers
3. Transconductance amplifiers
4. Transresistive amplifiers

Usually, the type of amplifiers can be determined based on the magnitudes of the input and output impedances of an amplifier with respect to source and load impedances. In this section, voltage amplifiers, current amplifiers, transconductance amplifiers and transresistive amplifiers are explained in detail.

4.3.1 Voltage Amplifiers

Figure 4.5 shows the Thevenin's equivalent circuit of a voltage amplifier. In this circuit,

V_s = Supply voltage, V_i = Input voltage,
V_o = Output voltage, R_s = Source resistance,
R_L = Load resistance, R_i = Input resistance,
R_o = Output resistance, I_i = Input current, and
I_o = Output current.

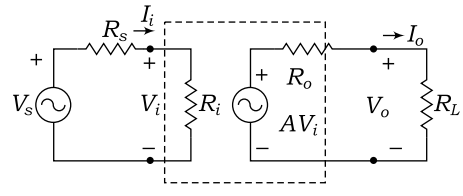


Fig. 4.5 Equivalent circuit of a voltage amplifier

The source voltage can be expressed as $V_s = I_i R_s + V_i$ and input voltage $V_i = I_i R_i$.

Therefore, $V_s = I_i R_s + I_i R_i$

When $R_i >> R_s$, $V_s \approx I_i R_i = V_i$

If input resistance R_i of voltage amplifier is very large compared to source resistance R_s, supply voltage is equal to input voltage $V_s = V_i$

The output voltage is $V_o = A_v V_i + I_o R_o = I_o R_L$

If $R_L >> R_o$, $A_v V_i = I_o R_L = V_o$

In this amplifier, load resistance R_L is very large compared to output resistance and output voltage $V_o = A_v V_i = A_v V_s$ as $V_s = V_i$.

Voltage amplifier gain $A_v = \frac{V_o}{V_s}$

Therefore, we can say that output voltage is proportional to input voltage and proportionality factor A_v is independent of the magnitude of the source and load resistance. This circuit is called *voltage amplifier*. An ideal voltage amplifier should have infinite input resistance $R_i = \infty$ and zero output resistance $R_o = 0$.

4.3.2 Current Amplifiers

Figure 4.6 shows the Norton's equivalent circuit of a current amplifier. In this circuit,

I_s = Source current, R_s = Source resistance,
I_i = Input current, R_i = Input resistance,
I_o = Output current, V_o = Output voltage,
R_o = Output resistance, and
R_L = Load resistance.

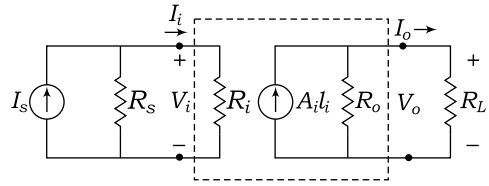


Fig. 4.6 Equivalent circuit of a current amplifier

The input current can be expressed as $I_i = I_s \dfrac{R_s}{R_s + R_i}$

If $R_s >> R_i \quad I_i \approx I_s$

In a current amplifier circuit, source resistance R_s is very large compared to R_i and source current is equal to input current.

The output current can be expressed as

$$I_o = A_i I_i \cdot \frac{R_o}{R_o + R_L} \tag{4.4}$$

If $R_o >> R_L, I_o = A_i I_i = A_i I_s \qquad$ as $I_i = I_s$

Hence, output current is proportional to the input current I_s and current amplifier gain A_i

Then current amplifier gain is $A_i = \dfrac{I_o}{I_s}$

Therefore, in an current amplifier, output current is proportional to the input current signal and the proportionality factor (A_i) is independent of R_s and R_o. An ideal current amplifier should have zero input resistance ($R_i = 0$) and infinite output resistance ($R_o = \infty$).

4.3.3 Transconductance Amplifiers

Figure 4.7 shows a transconductance amplifier, which is represented by a Thevenin's equivalent in input circuit and a Norton's equivalent in output circuit.

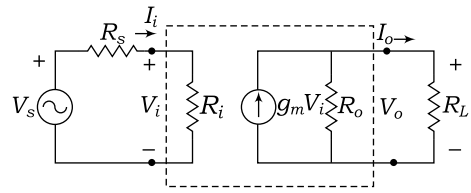


Fig. 4.7 Equivalent circuit of a transconductance amplifier

The source voltage can be expressed as

$$V_s = I_i R_s + V_i$$

or $V_s = I_i R_s + I_i R_i \quad$ as input voltage $V_i = I_i R_i$

If $R_i >> R_s, V_s \approx I_i R_i = V_i$

Therefore, source voltage is equal to input voltage as $R_i >> R_s$.

The output current can be expressed as

$$I_o = g_m V_i \cdot \frac{R_o}{R_o + R_L} \tag{4.5}$$

If $R_o >> R_L, I_o = g_m V_i = g_m V_s \quad$ as $V_i = V_s$

The transconductance amplifier gain is $g_m = \dfrac{I_o}{V_s}$

In an ideal transconductance amplifier, output current is proportional to the supply voltage and the proportionality factor (g_m) is independent of R_i and R_o. This amplifier should have infinite input resistance $R_i = \infty$ and infinite output resistance ($R_o = \infty$).

4.3.4 Transresistive Amplifiers

The equivalent circuit of a transresistive amplifier is depicted in Fig. 4.8. It is represented by Norton's equivalent in input circuit and a Thevenin's equivalent in its output circuit.

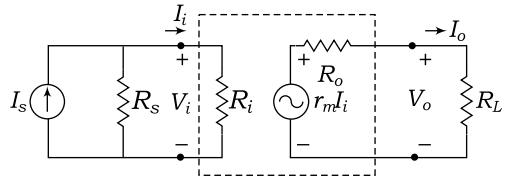


Fig. 4.8 Equivalent circuit of a transresistive amplifier

The input current can be expressed as

$$I_i = I_s \frac{R_s}{R_s + R_i} \tag{4.6}$$

If $R_s >> R_i, \quad I_i \approx I_s$

Hence, source current is equal to input current as $R_s >> R_i$

The output voltage is

$$V_o = r_m I_i + I_o R_o = I_o R_L$$

If $R_L >> R_o, V_o = r_m I_i = I_o R_L$

or $r_m I_s = I_o R_L \quad$ as $I_i \approx I_s$

The transresistive amplifier gain is $r_m = \dfrac{V_o}{I_s}$

Therefore, output voltage V_o is directly proportional to the source current I_S and proportionality factor r_m is independent of R_s and R_L. This type of amplifier is known as *transresistive amplifier*. This amplifier should have zero input resistance, $R_i = 0$ and zero output resistance, $R_o = 0$. Table 4.1 shows the ideal characteristics of Amplifiers.

Table 4.1 Amplifier characteristics

	Amplifier type			
Parameters	*Voltage Amplifier*	*Current Amplifier*	*Transconductance Amplifier*	*Transresistive Amplifier*
Input resistance R_i	∞	0	∞	0
Output resistance R_o	0	∞	∞	0
Input quantity	V_s	I_s	V_s	I_s
Output quantity	V_o	I_o	I_o	V_o
Transfer characteristics	$A_v = \dfrac{V_o}{V_s}$	$A_I = \dfrac{I_o}{I_s}$	$g_m = \dfrac{I_o}{V_s}$	$r_m = \dfrac{V_o}{I_s}$

4.4 GENERALISED CONCEPT OF FEEDBACK AMPLIFIERS

The schematic block diagram of feedback amplifier is shown in Fig. 4.9. This block diagram consists of sampling network, mixer network, feedback network, main amplifier, source signal and load. The output signal (voltage or current) is sampled by a sampling network and fed to the feedback network. The output of feedback network is combined with the input signal in the mixer network to obtain the difference signal V_i. Then output of the mixer network is fed to the main amplifier (basic practical amplifier). In this section, operation of sampling network, mixer network, feedback network, and main amplifier are explained briefly.

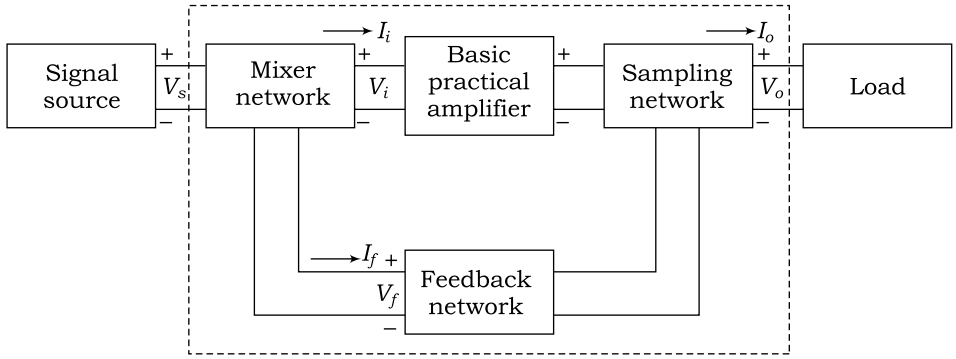


Fig. 4.9 Schematic diagram of a feedback amplifier

1. Sampling Network

Generally, two types of sampling networks such as voltage sampling and current sampling are used in a feedback system. In Fig. 4.10(a) the output voltage is sampled and in Fig. 4.10(b) the output current is sampled. The voltage sampling is called *node sampling* and the current sampling is known as *loop sampling*. Usually,

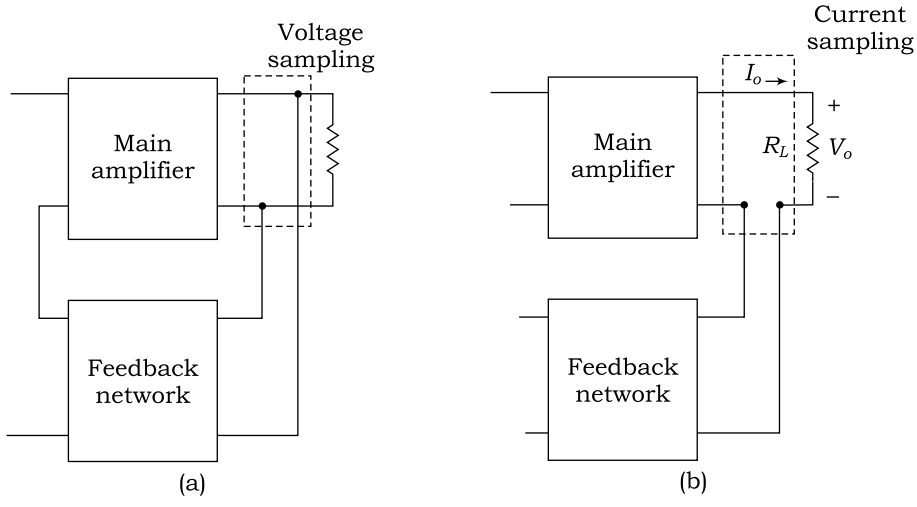


Fig. 4.10 (a) Voltage sampling (b) Current sampling

the output voltage is sampled by connecting the feedback network in shunt across the output and output current is sampled where feedback network is connected in series with the output as depicted in Fig. 4.10.

2. Mixer Network

This circuit is also known as comparator network. There are two mixer networks such as series mixing and shunt mixing. Figure 4.11(a) shows the series mixing and shunt mixing is depicted in Fig. 4.11(b). Sometimes, a differential amplifier is also used in mixer networks. The differential amplifier has two inputs and provides an output proportional to the difference between the two input signals.

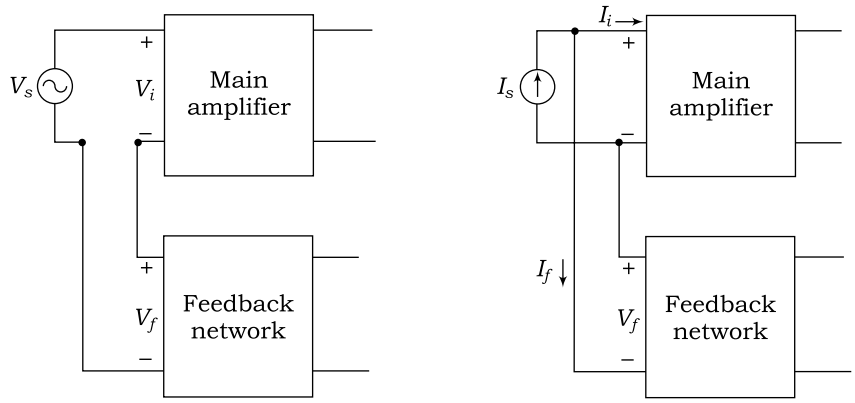


Fig. 4.11 (a) Series mixing (b) Shunt mixing

3. Main Amplifier

The main amplifier is also known as basic amplifier. Usually, four types of amplifiers such as voltage amplifier, current amplifier, transconductance amplifier and transresistance amplifiers are used in main amplifier circuit.

4. Feedback Network

This network is a passive two-port network which consists of resistances, capacitances and inductances, and its input side is connected to the sampling network and output side is connected with the mixer network.

5. Signal Source

The input signal will be either voltage source or current source. The voltage source (a voltage signal V_s in series with a resistor R_s) is known as Thevenin source and the current source (a current signal I_s in parallel with a resistor R_s) is called Norton source.

4.5 TOPOLOGIES OF FEEDBACK AMPLIFIERS

In a feedback amplifier, the input and output variables can be modeled as either a voltage or current. There are four combinations of inputs and outputs that represent the possible types of feedback amplifier. The four different types of feedback amplifiers are as follows:

1. Series-series feedback or current-series feedback
2. Series-parallel feedback or voltage-series feedback

3. Parallel-series feedback or current-shunt feedback
4. Parallel-parallel feedback or voltage-shunt feedback

Table 4.2 shows the different types of feedback amplifier with input variables, output variables, error signal, gain and feedback factor. The names of feedback amplifiers come from the way that the feedback network is connected between input and output. The four different types of feedback amplifier circuits are shown in Fig. 4.12(a) to Fig. 4.12(d). In this section, all types of feedback amplifiers are explained in detail.

Table 4.2 Types of feedback amplifiers

Feedback Amplifier	*Input Variable*	*Output Variable*	*Error Signal*	*Forward Gain*	*Feedback Factor*
Series-Series	Voltage	Current	Voltage	Transconductance	Ohms
Series-Parallel	Voltage	Voltage	Voltage	Voltage gain	Dimensionless
Parallel-Series	Current	Current	Current	Current gain	Dimensionless
Parallel-Parallel	Current	Voltage	Current	Transresistance	Siemens

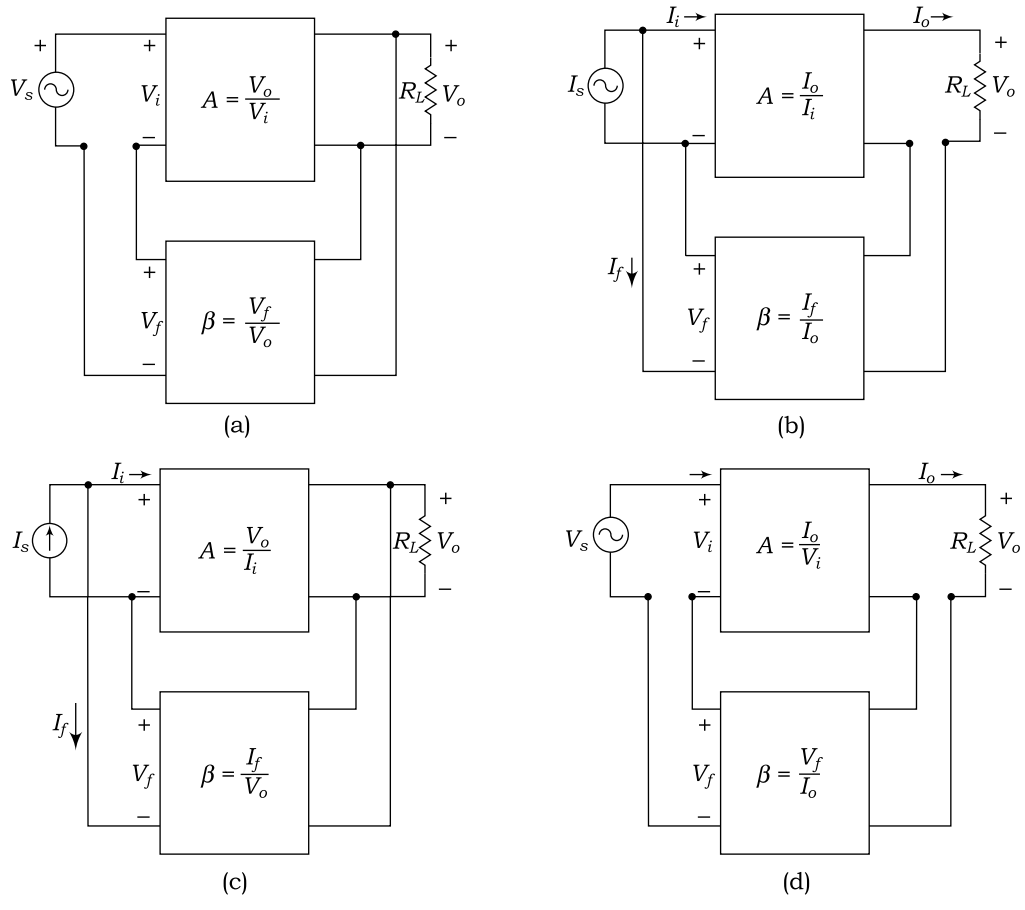


Fig. 4.12 (a) Voltage-series feedback (b) Current-shunt feedback (c) Voltage-shunt feedback (d) Current-series feedback

4.5.1 Voltage-Series Feedback Amplifier

Figure 4.13 shows the voltage-series feedback amplifier. In this circuit A is gain of main amplifier, β is the gain of feedback amplifier, V_s is supply voltage, V_f is feedback voltage, V_o is output voltage.

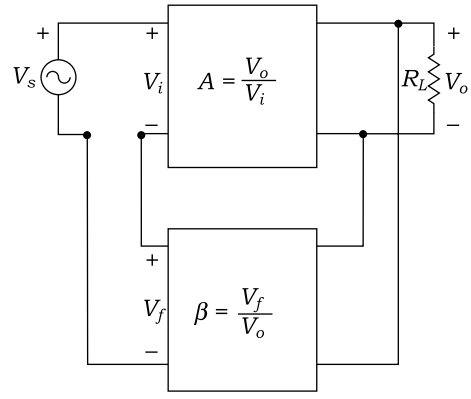


Fig. 4.13 The voltage-series feedback amplifier

The output voltage of a feedback amplifier is

$$V_f = \beta V_o \quad \text{as } \beta = \frac{V_f}{V_o}. \tag{4.7}$$

The feedback amplifier output voltage V_f is connected in series but in opposition to the input voltage.

Therefore, input voltage of the main amplifier is

$$V_i = V_s - V_f = V_s - \beta V_o$$

The main amplifier gain is

$$A = \frac{V_o}{V_i} \tag{4.8}$$

Then output voltage is equal to

$$V_o = AV_i = A(V_s - \beta V_o) \tag{4.9}$$

The overall amplifier gain with feedback is

$$A_f = \frac{V_o}{V_s} \tag{4.10}$$

Then $V_o = A(V_s - \beta V_o)$

or $V_o = AV_s - A\beta V_o$

or $V_o + \beta A V_o = AV_s$

or $(1 + \beta A)V_o = AV_s$

The overall amplifier gain is expressed as $A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}$ (4.11)

Hence, the negative feedback reduces the amplifier gain by a factor $(1 + \beta A)$.

4.5.2 Voltage-Shunt Feedback Amplifier

The block diagram of a voltage-shunt feedback amplifier is shown in Fig. 4.14.

where I_i is input current,

I_f is feedback current,

I_s is supply or source current, and

V_o is output voltage.

In this circuit, the feedback signal is proportional to output voltage V_o and is fed in parallel to the input signal. The main amplifier is transresistive amplifier as output signal is voltage V_o and input signal is current I_i.

The gain of main amplifier is

$$A = \frac{V_O}{I_i}$$ and units of A is ohms

Output voltage is

$$V_o = AI_i$$

The gain of feedback amplifier is

$$\beta = \frac{I_f}{V_o}$$

The feedback current is equal to

$$I_f = \beta V_o$$

The supply current is sum of input current and feedback current.

Therefore, $I_s = I_i + I_f = I_i + \beta V_o$

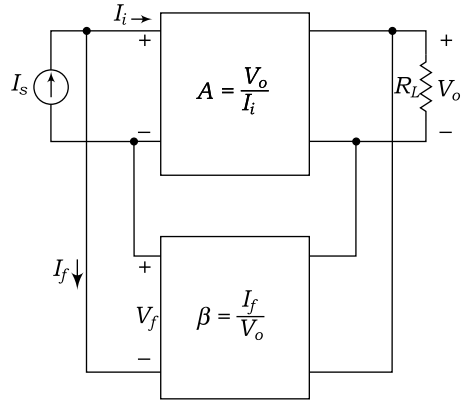


Fig. 4.14 The voltage-shunt feedback amplifier

The overall gain with feedback

$$A_f = \frac{V_o}{I_s} = \frac{V_o}{I_i + \beta V_o}$$

$$= \frac{AI_i}{I_i + \beta AI_i} = \frac{A}{1 + \beta A} \quad (4.12)$$

Again, we can say that the amplifier gain is reduced by a factor $(1 + \beta A)$ due to feedback.

4.5.3 Current-Shunt Feedback Amplifier

The block diagram of current-shunt feedback is shown in Fig. 4.15. The feedback signal is proportional to output current I_o and is fed in parallel with input. The main amplifier is a current amplifier.

The gain of main amplifier is

$$A = \frac{I_O}{I_i}$$ and A is dimensionless

The output current is

$$I_o = AI_i$$

The gain of feedback amplifier is $\beta = \frac{I_f}{I_o}$,

The feedback current is equal to $I_f = \beta I_o$

The source current is sum of input current and feedback current.

Therefore, $I_s = I_i + I_f = I_i + \beta I_o$

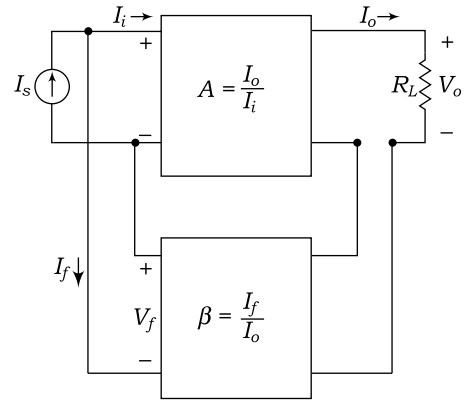


Fig. 4.15 The current-shunt feedback amplifier

The overall gain with feedback is

$$A_f = \frac{I_o}{I_s} = \frac{I_o}{I_i + I_f} = \frac{I_o}{I_i + \beta I_o}$$

$$= \frac{AI_i}{I_i + \beta AI_i} = \frac{A}{1 + \beta A} \quad (4.13)$$

It is clear from the above expression that the amplifier gain is to reduce by a factor $(1 + \beta A)$ when negative current feedback is provided.

4.5.4 Current-Series Feedback Amplifier

Figure 4.16 shows the block diagram of a current-series feedback. In this case, the feedback signal is proportional to output current I_o, which is fed back negatively to the input in series with the voltage source. The main amplifier is a transconductance amplifier as its output signal is current I_o and input signal is voltage V_i.

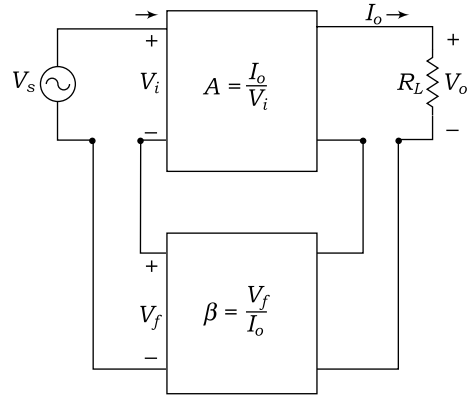


Fig. 4.16 The current-series feedback amplifier

The gain of main amplifier is

$$A = \frac{I_O}{V_i} \text{ and the units of } A \text{ is siemens}$$

The output current is

$$I_o = AV_i$$

The gain of feedback amplifier is

$$\beta = \frac{V_f}{I_o},$$

The feedback voltage is equal to $V_f = \beta I_o$

The supply voltage is sum of input voltage and feedback voltage.

Therefore,

$$\begin{aligned} V_s &= V_i + V_f \\ &= V_i + \beta I_o \\ &= V_i + \beta A V_i \\ &= (1 + \beta A) V_i \end{aligned}$$

The overall gain with feedback is

$$\begin{aligned} A_f &= \frac{I_o}{V_s} = \frac{I_o}{V_i + V_f} \\ &= \frac{AV_i}{V_i + \beta AV_i} = \frac{A}{1 + \beta A} \end{aligned} \tag{4.14}$$

Therefore, the amplifier gain is to reduce by a factor $(1 + \beta A)$ when feedback is provided.

4.6 EFFECT OF FEEDBACK ON IMPEDANCES

In this section, the effect of feedback on input and output impedances are explained for all four types feedback amplifiers such as voltage-series, current-series, voltage-shunt and current-shunt feedback amplifiers.

4.6.1 Effect of Voltage-Series Feedback Amplifier in Input Impedance

In a voltage-series feedback amplifier, the main amplifier is modelled as a voltage-dependent voltage source as depicted in Fig. 4.17.

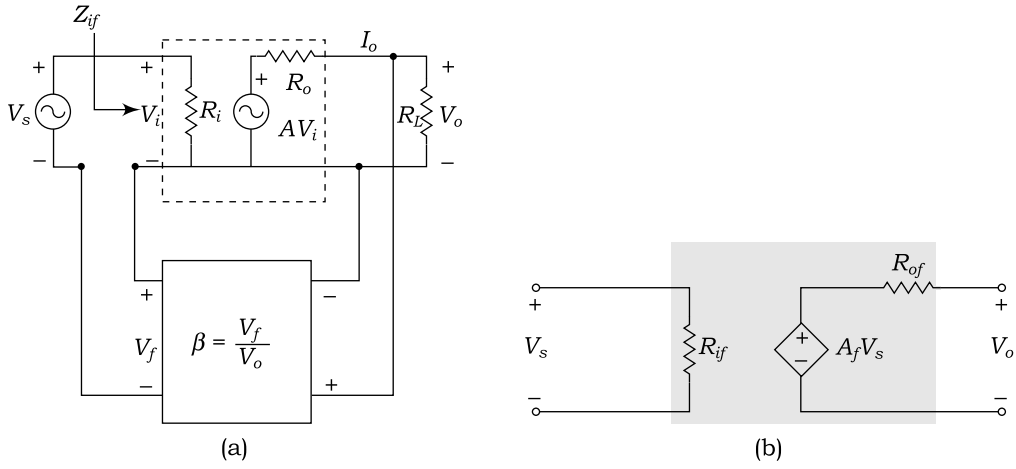


Fig. 4.17 (a) Ideal structure of voltage-series feedback amplifier (b) Equivalent structure of voltage-series feedback amplifier

Input impedance of the main amplifier is

$$Z_i = R_i$$

The input voltage is equal to

$$V_i = Z_i I_i = V_s - V_f$$

Assume R_o is negligible. Then output voltage is equal to $V_o = AV_i$

The feedback voltage is

$$V_f = \beta V_o$$

The source voltage is equal to

$$\begin{aligned} V_s &= V_i + V_f = Z_i I_i + \beta V_o \\ &= Z_i I_i + \beta A V_i \\ &= Z_i I_i + \beta A Z_i I_i \\ &= (1 + \beta A) Z_i I_i \end{aligned} \tag{4.15}$$

The input impedance of the feedback amplifier is

$$Z_{if} = \frac{V_s}{I_i} = \frac{(1 + \beta A) Z_i I_i}{I_i} = (1 + \beta A) Z_i \tag{4.16}$$

Hence, the value of input impedance without feedback is multiplied by a factor $(1 + \beta A)$.

4.6.2 Effect of Current-Series Feedback Amplifier in Input impedance

Figure 4.18 shows the current-series feedback amplifier. In this circuit, the main amplifier is modelled as a voltage-dependent current source.

Input impedance of main amplifier is $Z_i = R_i$

The input voltage is equal to

$$V_i = Z_i I_i = V_s - V_f$$

Assume R_o is very high. Then output current is equal to $I_o = AV_i$

The feedback voltage is

$$V_f = \beta I_o$$

The source voltage is equal to

$$\begin{aligned} V_s &= V_i + V_f = Z_i I_i + \beta I_o \\ &= Z_i I_i + \beta A V_i \\ &= Z_i I_i + \beta A Z_i I_i \\ &= (1 + \beta A) Z_i I_i \end{aligned} \tag{4.17}$$

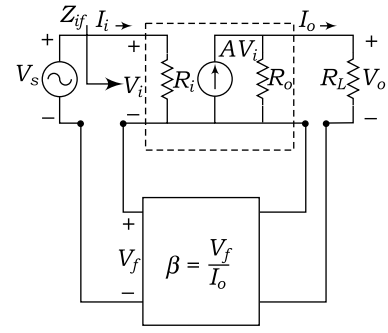


Fig. 4.18 Ideal structure of a voltage-series feedback amplifier

The input impedance of the feedback amplifier is

$$Z_{if} = \frac{V_s}{I_i} = \frac{(1 + \beta A) Z_i I_i}{I_i} = (1 + \beta A) Z_i \tag{4.18}$$

Therefore, the value of input impedance without feedback is multiplied by a factor $(1 + \beta A)$.

4.6.3 Effect of Voltage-Shunt Feedback Amplifier in Input impedance

Figure 4.19 shows a voltage-shunt feedback connection where the main amplifier is modeled as current dependence voltage source.

The input impedance of main amplifier is $Z_i = R_i$

Input voltage is

$$V_i = Z_i I_i$$

Assume R_o is negligible. The output voltage is equal to $V_o = AI_i$

Feedback gain is

$$\beta = \frac{I_f}{V_o}$$

The feedback current is equal to $I_f = \beta V_o$

The source current is

$$I_s = I_i + I_f$$

The input impedance $Z_{if} = \dfrac{V_i}{I_s} = \dfrac{V_i}{I_i + I_f}$

$$= \frac{V_i}{I_i + \beta V_o} = \frac{V_i / I_i}{1 + \beta \dfrac{V_o}{I_i}}$$

$$= \frac{Z_i}{1 + \beta A} \tag{4.19}$$

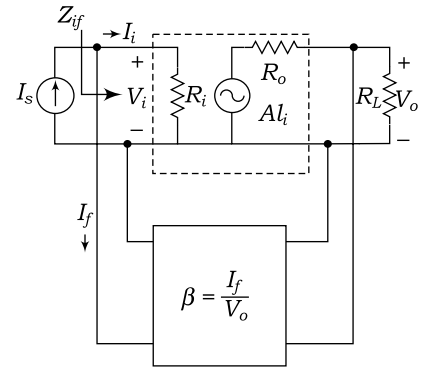


Fig. 4.19 Ideal structure of a voltage-shunt feedback amplifier

Hence, input impedance is reduced by a factor $(1 + \beta A)$

4.6.4 Effect of Current-Shunt Feedback Amplifier in Input Impedance

Figure 4.20 shows a current-shunt feedback connection where the main amplifier is modelled as a current-dependent current source.

The input impedance of main amplifier $Z_i = R_i$

Input voltage is

$$V_i = Z_i I_i$$

Assume R_o is very high. The output current is equal to $I_o = AI_i$

Feedback gain is

$$\beta = \frac{I_f}{I_o}$$

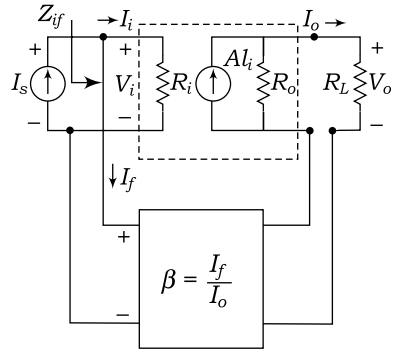


Fig. 4.20 **Ideal structure of current-shunt feedback amplifier**

The feedback current is equal to $I_f = \beta I_o$

The source current is $I_s = I_i + I_f$

The input impedance $Z_{if} = \dfrac{V_i}{I_s} = \dfrac{V_i}{I_i + I_f}$

$$= \frac{V_i}{I_i + \beta I_o} = \frac{V_i}{I_i + \beta A I_i}$$

$$= \frac{Z_i I_i}{I_i + \beta A I_i} = \frac{Z_i I_i}{(1 + \beta A) I_i}$$

$$= \frac{Z_i}{1 + \beta A} \qquad (4.20)$$

Hence, input impedance is reduced by a factor $(1 + \beta A)$.

4.6.5 Effect of Voltage-Series Feedback Amplifier in Output impedance

The output impedance can be obtained when a voltage V is applied at output terminals and V_s is shorted. Refer the ideal structure of voltage-series feedback amplifier as shown in Fig. 4.17 and V_s is shorted and a voltage V is applied at output terminals. Figure 4.21 shows the equivalent circuit to determine the output impedance of a voltage-series feedback amplifier where $V_s = 0$ and load resistance is disconnected.

Assume I current flows through the circuit.

The voltage is

$$V = IZ_o + AV_i \quad \text{where } Z_o = R_o$$

The input voltage is equal to feedback voltage but polarity is reversed.

Therefore, $V_i = -V_f$

Then voltage $V = IZ_o - AV_f = IZ_o - A\beta V$ As $V_f = \beta V_o$

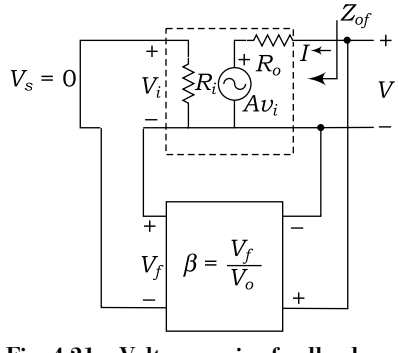


Fig. 4.21 **Voltage-series feedback amplifier with $V_s = 0$ and R_L disconnected**

Hence, $IZ_o = V + \beta AV$

$= (1 + \beta A)V$

The output impedance is equal to

$$Z_{of} = \frac{V}{I} = \frac{Z_o}{1 + \beta A} \tag{4.21}$$

Hence, in voltage-series feedback, the output impedance is reduced from the without feedback by the factor $(1 + \beta A)$.

In the same way, the output impedance of voltage-shunt feedback amplifier can also be computed and output impedance can be expressed as $Z_{of} = \frac{Z_o}{1 + \beta A}$.

4.6.6 Effect of Current-Series Feedback Amplifier in Output impedance

Figure 4.18 shows the current-series feedback amplifier circuit. In this case, the main amplifier is represented by current model. To calculate the output impedance, voltage V is applied at output terminals with V_s is shorted. Figure 4.22 shows the equivalent circuit to determine the output impedance of a current-series feedback amplifier where $V_s = 0$ and load resistance is disconnected.

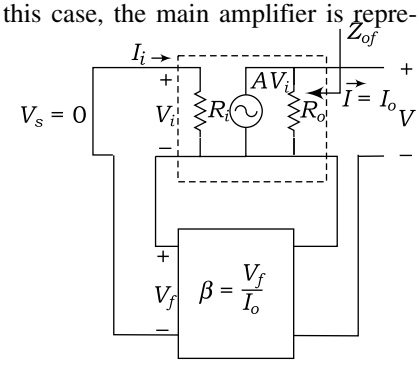


Fig. 4.22 Current-series feedback amplifier with $V_s = 0$ and R_L disconnected

Assume current I flows through the circuit.

As $V_s = 0$, $V_i = -V_f$

The output current is

$$I = \frac{V}{Z_o} + AV_i$$

$$= \frac{V}{Z_o} - AV_f \quad \text{as} \quad V_i = -V_f$$

$$= \frac{V}{Z_o} - A\beta I \quad \text{as} \quad V_f = \beta I$$

Then we can write $(1 + A\beta)I = \frac{V}{Z_o}$

or $(1 + A\beta)IZ_o = V$

The output impedance is equal to

$$Z_{of} = \frac{V}{I} = Z_o(1 + \beta A) \tag{4.22}$$

In the same way, the output impedance of current-shunt feedback amplifier can be computed and output impedance can be expressed as $Z_{of} = Z_o(1 + \beta A)$.

Table 4.3 shows the summary of input and output impedances of voltage-series, current-series, voltage-shunt and current-shunt feedback amplifiers.

Table 4.3 Input and output impedances of feedback amplifiers

Impedance	*Types of feedback amplifier*			
	Voltage Series	*Current Series*	*Voltage Shunt*	*Current Shunt*
Input impedance Z_{if}	Increased $Z_i(1+\beta A)$	Increased $Z_i(1+\beta A)$	Decreased $\frac{Z_i}{1+\beta A}$	Decreased $\frac{Z_i}{1+\beta A}$
Output impedance Z_{of}	Decreased $\frac{Z_o}{1+\beta A}$	Increased $Z_o(1+\beta A)$	Decreased $\frac{Z_o}{1+\beta A}$	Increased $Z_o(1+\beta A)$

Example 4.5 In a voltage-series feedback amplifier $A = 400$, $R_i = 2$ kΩ, $R_o = 100$ kΩ and $\beta = 0.1$, determine overall gain, input impedance and output impedance of feedback amplifier.

Solution

Sol. Assume $A = 400$, $R_i = 2$ kΩ, $R_o = 100$ kΩ and $\beta = 0.1$

In a voltage-series feedback amplifier,

Overall gain is
$$A_f = \frac{A}{1+\beta A}$$
$$= \frac{400}{1+0.1\times 400} = 9.756$$

Input impedance is
$$Z_{if} = Z_i(1+\beta A)$$
$$= R_i(1+\beta A) = 2\times 10^3(1+0.1\times 400) = 82 \text{ k}\Omega$$

Output impedance is
$$Z_{of} = \frac{Z_o}{1+\beta A}$$
$$= \frac{R_o}{1+\beta A} = \frac{100\times 10^3}{(1+0.1\times 400)} = 2.439 \text{ k}\Omega$$

Example 4.6 Calculate the overall loop gain, input and output impedances for an amplifier in a current-series feedback amplifier with $A = 100$, $R_i = 1$ kΩ, $R_o = 50$ kΩ and $\beta = 0.025$.

Sol. Given A = 100, R_i = 1 kΩ, R_o = 50 kΩ and $\beta = 0.025$

In a current-series feedback amplifier,

Overall gain is $A_f = \frac{A}{1+\beta A} = \frac{100}{1+0.025\times 100} = 28.571$

Input impedance is $Z_{if} = Z_i(1+\beta A)$ assume $Z_i = R_i$
$$= R_i(1+\beta A) = 1\times 10^3(1+0.025\times 100) = 3.5 \text{ k}\Omega$$

Output impedance is $Z_{of} = Z_o(1+\beta A)$ assume $Z_o = R_o$
$$= R_o(1+\beta A) = 50\times 10^3(1+0.025\times 100) = 175 \text{ k}\Omega$$

Example 4.7 A voltage-series feedback amplifier has $A = -100$, $R_i = 25$ kΩ, $R_o = 10$ kΩ and feedback factor $\beta = -0.1$.

(a) Determine overall gain, input impedance, and output impedance of feedback amplifier.

(b) If the gain has been reduced to –2.5, what will be the feedback factor?

Sol. Given $A = -100$, $R_i = 25$ kΩ, $R_o = 10$ kΩ and $\beta = -0.1$

(a) In a voltage-series feedback amplifier,

Overall gain is

$$A_f = \frac{A}{1+\beta A} = \frac{-100}{1+(-0.1)\times(-100)} = 9.0909$$

Input impedance is

$$Z_{if} = Z_i(1+\beta A) \quad \text{as } Z_i = R_i$$

$$= R_i(1+\beta A) = 25\times10^3(1+(-0.1)\times(-100)) = 275 \text{ kΩ}$$

Output impedance is

$$Z_{of} = \frac{Z_o}{1+\beta A} \quad \text{as } Z_o = R_o$$

$$= \frac{R_o}{1+\beta A} = \frac{-10 \text{ kΩ}}{(1+(-0.1)\times(-100))} = 0.909 \text{ kΩ} = 909 \text{ Ω}$$

(b) When the gain has been reduced to –2.5, the feedback factor will be computed from

$$A'_f = \frac{A}{1+\beta A} \quad \text{as } A'_f = -2.5$$

$$= \frac{-100}{1+\beta\times(-100)} = -2.5$$

Then the feedback factor is $\beta = -0.39$

Example 4.8 A feedback amplifier circuit is shown in Fig. 4.23 with the gain of amplifier $A = 100 \angle 180°$, $R_1 = 10$ kΩ and $R_2 = 150$ kΩ.

Calculate output voltage and source voltage when input voltage of amplifier $1\angle 0°$.

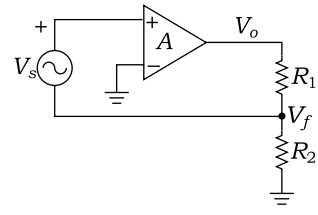


Fig. 4.23

Sol. The above circuit configuration is voltage-series feedback.

The feedback voltage is

$$V_f = \frac{R_2}{R_1+R_2}V_o = \frac{150}{150+10}V_o$$

$$= \frac{150}{160}V_o = \beta V_o$$

So, feedback path gain is $\beta = \frac{150}{160}$

The overall gain is $A_f = \frac{V_o}{V_s} = \frac{A}{1+\beta A}$

$$= \frac{100\angle 180°}{1 + \frac{150}{160} \times 100\angle 180°}$$

$$= \frac{-100}{1 + \frac{150}{160} \times (-100)} = 1.078$$

Hence, $V_o = 1.078 V_s$

The input voltage of main amplifier is

$$V_i = V_s - V_f = V_s - \beta V_o$$

$$= V_s - \frac{150}{160} \times 1.078 V_s = 0.010625 V_s$$

As $V_i = 1\angle 0°$, the source voltage is equal to

$$V_s = -\frac{1\angle 0°}{0.010625} = -94.11\angle 0°$$

The output voltage is equal to $V_o = 1.078 V_s$

Then output voltage $V_o = 1.078 V_s = 1.078 \times (-94.11\angle 0°) = -101.45\angle 0°$

Example 4.9 An amplifier has an open-loop gain of 200, an input impedance of 1 kΩ and an output impedance of 100 Ω. A feedback network with a feedback factor of 0.5 is connected in a voltage-series feedback mode. Determine the new input and output impedances.

Sol. Assume, input impedance Z_i = 1 kΩ, output impedance Z_o = 100 Ω, open-loop gain A = 200 and feedback factor $\beta = 0.5$.

After feedback, new input impedance is $Z_{if}(1 + \beta A)$ = 1 kΩ (1 + 0.5 × 200) = 101 kΩ

and new output impedance is $Z_{of} = \frac{Z_o}{1+\beta A}$

$$= \frac{100}{1 + 0.5 \times 200} = 0.99\ \Omega$$

Example 4.10 Determine overall gain, input impedance and output impedance of a voltage-shunt feedback amplifier. Assume the following parameters of feedback amplifier

Open-loop gain A = –1000, input resistance R_i = 10 kΩ, output resistance R_o = 20 kΩ and β = –0.1.

Sol. Given A = –1000, R_i = 10 kΩ, R_o = 20 kΩ and β = –0.1

In a voltage-shunt feedback amplifier,

Overall gain is $A_f = \frac{A}{1+\beta A}$

$$= \frac{-1000}{1 + (-0.1) \times -1000} = -9.90$$

Input impedance is

$$Z_{if} = \frac{Z_i}{1+\beta A}$$

$$= \frac{R_i}{1+\beta A} = \frac{10\ \text{K}\Omega}{1+(-0.1)(-1000)} = 99\ \Omega$$

Output impedance is $Z_{of} = \dfrac{Z_o}{1+\beta A}$

$$= \frac{R_o}{1+\beta A} = \frac{20\times 10^3}{(1+(-0.1)\times(-1000))} = 198\ \Omega$$

Example 4.11 Compute input and output impedances for an amplifier in a current-shunt feedback configuration with $A = 500$, $R_i = 1000\ \Omega$, $R_o = 5000\ \Omega$ and $\beta = 0.075$.

Sol. Given $A = 500$, $R_i = 1000\ \Omega$, $R_o = 5000\ \Omega$ and $\beta = 0.075$

In current-shunt feedback amplifier,

Input impedance is

$$Z_{if} = \frac{Z_i}{1+\beta A} \quad \text{assume } Z_i = R_i$$

$$= \frac{R_i}{1+\beta A} = \frac{1000\,\Omega}{1+(0.075\times 500)} = 25.97\ \Omega$$

Output impedance is $Z_{of} = Z_o(1+\beta A)$ assume $Z_o = R_o$

$$= R_o(1+\beta A) = 5000(1+0.075\times 500) = 192.5\ \text{k}\Omega$$

4.7 PROPERTIES OF FEEDBACK AMPLIFIERS

The properties of feedback amplifiers are

- Reduction in frequency distortion
- Reduction in noise and nonlinear distortion
- Effect of negative feedback on gain and bandwidth
- Gain stability with feedback
- Reduction in phase distortion

4.7.1 Reduction in Frequency Distortion

In a negative feedback amplifier with feedback gain β, the overall loop gain of the amplifier is reduced by a factor $(1 + \beta A)$. If we assume $\beta A >> 1$, the gain with feedback is $A_f \cong \dfrac{1}{\beta}$. It follows that the feedback network is purely resistive and the gain with feedback does not depend on frequency even though the main amplifier gain is frequency dependent. Therefore, the frequency distortion arising because of varying amplifier gain with frequency is considerably reduced in a negative voltage feedback amplifier circuit.

4.7.2 Reduction in Noise and Nonlinear Distortion

Feedback signal tends to hold down the amount of noise signal and nonlinear distortion at the output stage. Figure 4.24 shows the block diagram representation of negative feedback amplifier with noise signal V_N.

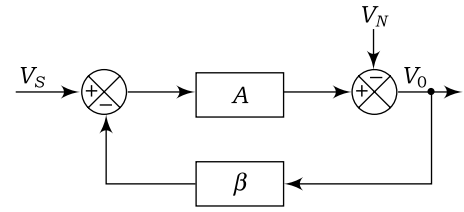


Fig. 4.24 Feedback amplifier with noise signal

When the noise signal V_N is present, the output voltage will be function of input signal V_S, open-loop gain A, gain of feedback path β and noise signal V_N. The output voltage can be expressed as

$$V_o = \frac{A}{1+\beta A} V_s + \frac{1}{1+\beta A} V_N \tag{4.23}$$

It is clear from the above expression that there is a reduction in overall gain, but noise is reduced by the factor $(1 + \beta A)$. Hence, nonlinear distortion is considerably improved.

An additional preamplifier of gain $(1 + \beta A)$ is used to bring the overall gain up to the level without feedback as depicted in Fig. 4.25.

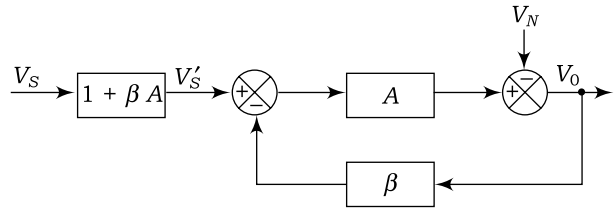


Fig. 4.25 Feedback amplifier with noise signal and a preamplifier

The output voltage can be expressed as

$$V_o = \frac{A}{1+\beta A} V_s' + \frac{1}{1+\beta A} V_N \tag{4.24}$$

As $V_s = (1+\beta A)V_s'$, output voltage is $V_o = AV_s + \frac{1}{1+\beta A} V_N$

The above equation states that the input signal V_s is amplified by A and the noise signal in the output is reduced by $(1 + \beta A)$.

Sometimes the extra stages might introduce as much noise back into the system as that reduced by the feedback amplifier. This problem can be solved to some extent by readjusting the gain of the feedback amplifier circuit to obtain higher gain while also providing reduced noise signal.

4.7.3 Effect of Negative Feedback on Gain and Bandwidth

In a negative feedback amplifier, the overall loop gain can be expressed as

$$A_f = \frac{A}{1+\beta \cdot A} \cong \frac{A}{\beta A} = \frac{1}{\beta} \quad \text{as} \quad \beta A >> 1 \tag{4.25}$$

As long as $\beta A >> 1$, the overall loop gain is $A_f = \frac{1}{\beta}$

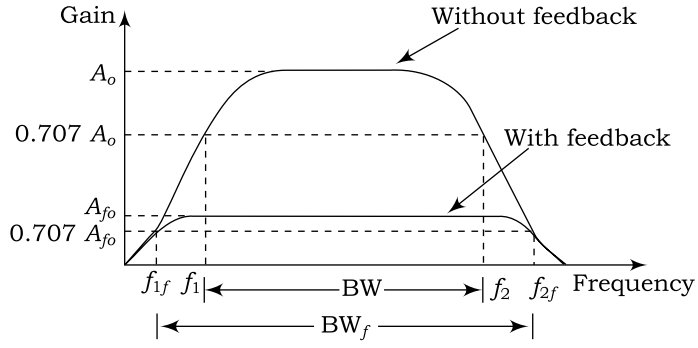


Fig. 4.26 Effect of negative feedback on gain and bandwidth

Figure 4.26 shows the effect of negative feedback on gain and bandwidth.
The low-frequency gain of the amplifier is A_l and it can be expressed as

$$A_l = \frac{Ao}{1 - j\left(\frac{f_1}{f}\right)} \tag{4.26}$$

where, A_o is the mid-frequency gain and f_1 is the lower half-power frequency
The high-frequency gain of amplifier is A_h and it can be expressed as

$$A_h = \frac{Ao}{1 + j\left(\frac{f}{f_2}\right)} \tag{4.27}$$

where, f_2 is the upper half-power frequency.

With feedback, the overall gain at low frequency is $A_{lf} = \frac{A_l}{1 + \beta A_l}$

With feedback, the overall gain at high frequency is $A_{hf} = \frac{A_h}{1 + \beta A_h}$

After substituting the value of $A_l = \frac{A_o}{1 - j\left(\frac{f_1}{f}\right)}$ in the equation $A_{lf} = \frac{A_l}{1 + \beta A_l}$, we get

$$A_{lf} = \frac{A_o}{1 + \beta A_o - j\left(\frac{f_1}{f}\right)} = \frac{A_{fo}}{1 - j\left(\frac{f_{1f}}{f}\right)} \tag{4.28}$$

where A_{fo} is the mid-frequency gain with negative feedback and $A_{fo} = \frac{Ao}{1 + \beta A_o}$

f_{1f} is known as lower half-power frequency with negative feedback and $f_{1f} = \frac{f_1}{1 + \beta A_o}$

After substituting the value of $A_h = \dfrac{A_o}{1 + j\left(\dfrac{f}{f_2}\right)}$ in the equation $A_{hf} = \dfrac{A_h}{1 + \beta A_h}$, we obtain

$$A_{hf} = \frac{A_{fo}}{1 + j\left(\dfrac{f}{f_{2f}}\right)} \tag{4.29}$$

where, f_{2f} is known as upper half-power frequency with negative feedback and $f_{2f} = f_2(1 + \beta A_o)$
In an amplifier without feedback, bandwidth is equal to the difference between f_2 and f_1

$$BW = f_2 - f_1$$

When feedback is used, there is some reduction in gain in low-frequency and high-frequency regions. The feedback amplifier has a higher upper 3 dB frequency and smaller 3 dB frequency.
The bandwidth with feedback is $BW_f = f_{2f} - f_{1f}$

where, upper cut-off frequency $f_{2f} = f_2(1 + \beta A_o)$

lower cut-off frequency $f_{1f} = \dfrac{f_1}{1 + \beta A_o}$

Therefore, an amplifier with negative feedback has larger bandwidth with respect to bandwidth without feedback.

4.7.4 Gain Stability with Feedback

The overall loop gain of a feedback amplifier is $A_f = \dfrac{A}{1 + \beta \cdot A}$

Differentiation of the above equation gives

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1 + \beta A|}\left|\frac{dA}{A}\right|$$

or

$$\left|\frac{dA_f}{A_f}\right| = \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \quad \text{for } \beta A >> 1 \tag{4.30}$$

This shows that the magnitude of relative change in overall gain $\left|\dfrac{dA_f}{A_f}\right|$ is reduced by the factor $|\beta A|$ compared to relative change $\left|\dfrac{dA}{A}\right|$ in basic amplifier gain.

The fractional change in amplification with feedback divided by the fractional change without feedback is called sensitivity of the transfer gain. The sensitivity S can be expressed as

Sensitivity = $S = \dfrac{dA_f/A_f}{dA/A} = \dfrac{1}{1 + \beta A} = \dfrac{1}{\beta A}$ for $\beta A >> 1$.

The desensitivity D is equal to $\dfrac{1}{\text{Sensitivity}} = \dfrac{1}{S}$.

Therefore, $D = \frac{1}{S} = 1 + \beta A$ and $\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1+\beta A|}\left|\frac{dA}{A}\right| = \frac{1}{|D|}\left|\frac{dA}{A}\right|$

Since $|D|$ is greater than 1 for negative feedback amplifier, the percentage change in amplification with feedback is less than the percentage change in A. Therefore, $\left|\frac{dA_f}{A_f}\right| < \left|\frac{dA}{A}\right|$.

4.7.5 Phase Distortion with Feedback

The gain of an amplifier is a complex quantity and it has a magnitude and a phase angle. As a result, the gain A of an amplifier without feedback can be expressed as

$$A = |A| \angle \theta$$

With feedback, the gain of the amplifier is $A_f = \frac{A}{1 + \beta \cdot A}$.

The gain of feedback path β is either a real or a complex quantity. To simplify the mathematical analysis, we assume β is a real number.

After substituting the value of $A = |A| \angle \theta$ in overall gain, we get

$$\begin{aligned} A_f &= \frac{A}{1 + \beta \cdot A} = \frac{|A| \angle \theta}{1 + \beta |A| \angle \theta} \\ &= \frac{|A| \angle \theta}{1 + \beta |A| (\cos \theta + j \sin \theta)} \\ &= \frac{|A| \angle \theta}{(1 + \beta |A| \cos \theta) + j \beta |A| \sin \theta} \\ &= \frac{A \angle \theta}{B \angle \phi} \end{aligned}$$

where, $|B| = \sqrt{(1 + \beta |A| \cos \theta)^2 + (\beta |A| \sin \theta)^2}$ and $\phi = \tan^{-1}\left(\frac{\beta |A| \sin \theta}{1 + \beta |A| \cos \theta}\right)$

$$A_f = \frac{|A|}{|B|} \angle \theta - \phi = |A_f| \angle \psi \tag{4.31}$$

where, $$|A_f| = \frac{|A|}{|B|} \text{ and } \angle \psi = \angle \theta - \phi$$

It is clear from $A_f = \frac{|A|}{|B|} \angle \theta - \phi = |A_f| \angle \psi$ that the phase angle of the overall gain decreases by ϕ in negative feedback amplifier. Therefore, the phase distortion is reduced.

Example 4.12 An operational amplifier has an open-loop gain of 10^6 and open-loop upper cut-off frequency of 10 Hz. If this operational amplifier is connected as an amplifier with a closed-loop gain of 100, what will be the new upper cut-off frequency?

Sol. The closed-loop gain is $A_f = \frac{A}{1 + \beta \cdot A}$

Here, $A = 10^6$ and $A_f = 100$ and open-loop upper cut-off frequency $f_2 = 10$ Hz

$$(1 + \beta A) = \frac{A}{A_f} = \frac{10^6}{100} = 10^4$$

The upper cut-off frequency $f_{2f} = f_2(1 + \beta A) = 10 \times 10^4 = 100$ kHz

Example 4.13 An amplifier circuit has a gain of –100 and feedback path gain is $\beta = -0.01$. When the amplifier gain is changed by 25% due to temperature, determine the change in gain of feedback amplifier.

Sol. Given A = –100, $\beta = -0.01$ and $\left|\frac{dA}{A}\right| = 25\% = 0.25$

The change in gain of feedback amplifier

$$\left|\frac{dA_f}{A_f}\right| = \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| = \frac{1}{(-0.01) \times (-100)} \times 0.25 = 0.25 = 25\%$$

Example 4.14 An amplifier circuit has a gain of –100 and feedback ratio is $\beta = -0.05$. Determine (a) the amplifier gain with feedback, (b) the amount of feedback in dB, (c) the feedback factor, and (d) feedback voltage.

Assume input voltage $V_s = 50$ mV

Sol. Given $A = -100$, $\beta = -0.05$

(a) The amplifier gain with feedback is $A_f = \frac{A}{1 + \beta \cdot A} = \frac{-100}{1 + (-0.05)(-100)} = -16.67$

(b) The amount of feedback in dB = $20 \log_{10}\left|\frac{A_f}{A}\right| = 20 \log_{10}\left|\frac{-16.67}{-100}\right| = -15.56$ dB

(c) The feedback factor is $\beta A = (-100) \times (-0.05) = 5$

(d) The feedback voltage is

$$V_f = \beta V_o \quad \text{as } V_o = A_f V_s$$

$$= \beta A_f V_s = (-0.05) \times (-16.67) \times 50 \text{ mV} = 41.675 \text{ mV}$$

4.8 METHOD OF ANALYSIS OF A FEEDBACK AMPLIFIER

The complete analysis of feedback amplifier is done by the following steps given below:

Step-1

Identify the topology of the feedback amplifier.

(a) Find the sampled signal, either voltage or current. It can be determined by the fact that whether the sampled signal is taken from the output voltage node or from the output current loop.

(b) Find the feedback signal, either voltage or current. If the feedback signal is a voltage, it is mixed with external input signal in shunt connection. When the feedback signal is a current, it is mixed with external input signal in series connection.

Depending upon the sampled signal as well as feedback signal, there are four different topologies of feedback amplifiers as given in Table 4.4.

Table 4.4 Feedback amplifier

Topology	*Sampled Signal*	*Feedback Signal*
Voltage series	Voltage	Series
Voltage shunt	Voltage	Shunt
Current series	Current	Series
Current shunt	Current	Shunt

Step-2

Draw the basic amplifier circuit without feedback by using the following method:

(a) For the input circuit, modify the output side as follows:
- In case of voltage-series or voltage-shunt topology, short the output node to ground.
- In case of current-series or current-shunt topology, open the output loop.

(b) For the output circuit, modify the input side as follows:
- In case of voltage-shunt or current-shunt topology, short the input node.
- In case of voltage-series or current-series topology, open the input loop.

Step-3

Input signal source must be converted into following ways:

(a) Use Thevenin's source for voltage series or current-series topology.

(b) Use Norton source voltage-shunt or current-shunt topology.

Step-4

Mention the output signal (V_o or I_o) on the circuit.

Mention the feedback signal (V_f or I_f) on the circuit.

Step-5

Determine the gain of feedback path $\beta = \dfrac{\text{Feedback signal}}{\text{Output signal}}$.

Step-6

Draw the equivalent circuit of the main amplifier by replacing each active device by its proper *h*-parameter model. From the equivalent circuit, determine A_V for voltage amplifier, A_I for current amplifier, g_m for transconductance amplifier or r_m for transresistance amplifier.

Step-7

Determine overall loop gain, $A_f = \dfrac{A}{1 + \beta A}$.

Step-8

In the same way, determine input impedance, R_{if} and output impedance, R_{of}.

4.9 PRACTICAL FEEDBACK CIRCUITS

This section provides some examples of practical feedback circuits to demonstrate the effect of feedback.

4.9.1 FET Amplifier With Voltage-Series Feedback

Figure 4.27 shows an FET amplifier circuit with voltage-series feedback. A part of output voltage can be feedbacked using a voltage divider circuit, which consists of resistors R_1 and R_2. The feedback voltage is connected in series with source signal V_S. The mid-frequency small-signal model of Fig. 4.27 is depicted in Fig. 4.28.

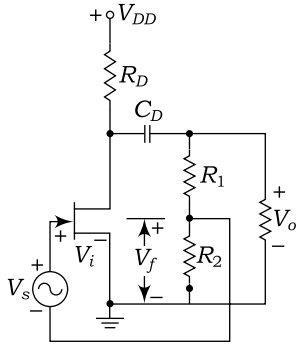


Fig. 4.27 FET amplifier

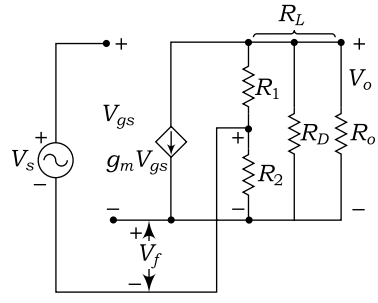


Fig. 4.28 Equivalent circuit of FET amplifier

Amplifier gain is $A = \dfrac{V_o}{V_i} = -g_m R_L$ where, R_L is parallel combination of resistances, R_o, R_D and R_1 and R_2.

R_L can be expressed as $R_L = R_D \| (R_1 + R_2) \| R_o$

Feedback factor $\beta = \dfrac{V_f}{V_o} = -\dfrac{R_2}{R_1 + R_2}$

Figure 4.29 shows the block-diagram representation of the feedback amplifier. The gain of the negative feedback amplifier is

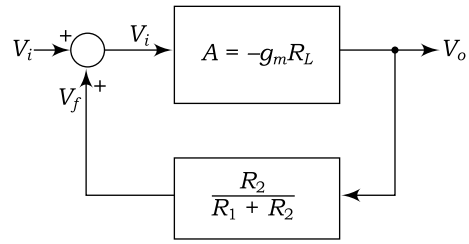


Fig. 4.29 Block-diagram representation of feedback amplifier

$$A_f = \frac{A}{1 + \beta \cdot A} = \frac{-g_m R_L}{1 + \left(-\dfrac{R_2}{R_1 + R_2}\right)(-g_m R_L)}$$

$$= \frac{-g_m R_L}{1 + g_m \left(\dfrac{R_2 R_L}{R_1 + R_2}\right)} \tag{4.32}$$

For $\beta A >> 1$, $A_f = \dfrac{1}{\beta} = \dfrac{-g_m R_L}{g_m \left(\dfrac{R_2 R_L}{R_1 + R_2}\right)} = -\dfrac{R_1 + R_2}{R_2}$

Example 4.15 Determine the overall loop gain of FET amplifier circuit as depicted in Fig. 4.27 with the following parameters g_m = 1000 μs, R_1 = 20 kΩ, R_2 = 10 kΩ, R_o = 15 kΩ and R_D = 10 kΩ.

Sol. Given g_m = 1000 μs, R_1 = 20 kΩ, R_2 = 10 kΩ, R_o = 15 kΩ and R_D = 10 kΩ.

$$R_L = R_D \| (R_1 + R_2) \| R_o$$

or $$\frac{1}{R_L}=\frac{1}{R_D}+\frac{1}{R_1+R_2}+\frac{1}{R_o}=\frac{1}{10}+\frac{1}{30}+\frac{1}{15}$$

or $$R_L = 5\ \text{k}\Omega$$

Amplifier gain is $A=\frac{V_o}{V_i}=-g_mR_L=-1000\times10^{-6}\times5\times10^{3}=-5$

Feedback factor is $\beta=\frac{V_f}{V_o}=-\frac{R_2}{R_1+R_2}=-\frac{10}{20+10}=-\frac{1}{3}$

Overall loop gain is $A_f=\frac{A}{1+\beta\cdot A}=\frac{-5}{1+\left(-\frac{1}{3}\right)\times(-5)}=-1.87$

4.9.2 BJT Emitter-Follower Circuit

Figure 4.30 shows the emitter-follower circuit with voltage-series feedback. In this circuit V_s is supply voltage, V_i is input voltage, V_o is output voltage and V_f is feedback voltage.
The output voltage is $V_o = V_f$

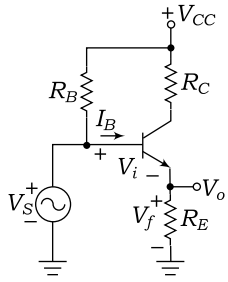


Fig. 4.30 BJT amplifier with voltage-series feedback

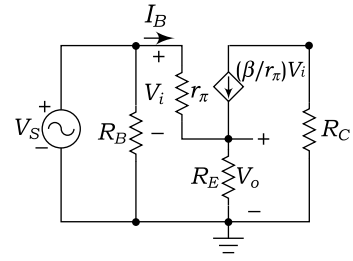


Fig. 4.31 Equivalent circuit of a BJT amplifier

In this circuit, feedback voltage is in series with the input voltage.
The mid-frequency small-signal model of Fig. 4.30 is depicted in Fig. 4.31.

Amplifier gain is $A=\frac{V_o}{V_s}=\frac{(1+\beta)}{r_\pi}R_E=\frac{\beta}{r_\pi}R_E \quad \text{as } \beta >> 1$

Feedback factor is $B=\frac{V_f}{V_o}=1$

The block-diagram representation of Fig. 4.30 is depicted in Fig. 4.32.
The overall loop gain is

$$A_f=\frac{A}{1+B\cdot A}$$

$$=\frac{\beta R_E}{r_\pi+\beta R_E}\approx 1 \quad \text{as } \beta R_E >> r_\pi$$

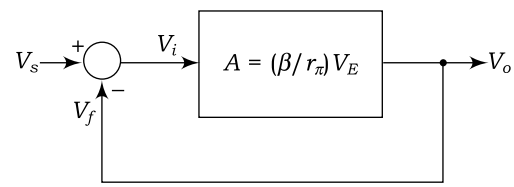


Fig. 4.32 Block-diagram representation of feedback amplifier

4.9.3 Emitter-Current Feedback Amplifier

The emitter-current feedback amplifier is shown in Fig. 4.33 and its small-signal model is depicted in Fig. 4.34. It is clear from Fig. 4.33 that the feedback voltage is proportional to the emitter current which is being fed negatively. The R_B resistance across base and V_{CC} does not affect voltage gain of the amplifier. The block-diagram representation of BJT amplifier with current-series feedback is illustrated in Fig. 4.35.

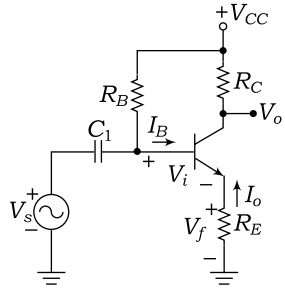


Fig. 4.33 BJT amplifier with current-series feedback

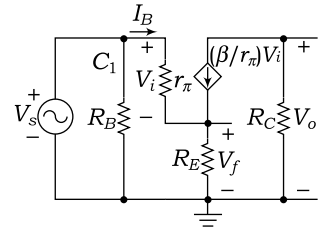


Fig. 4.34 Equivalent circuit of BJT amplifier

The gain $A = -\dfrac{\beta}{r_\pi}$ and the feedback voltage $V_f = -I_o R_E$

As $V_f = BI_o$, $B = -R_E$

Amplifier gain is

$$A_f = \frac{I_o}{V_s} = \frac{A}{(1+BA)} = \frac{-\dfrac{\beta}{r_\pi}}{1+(-R_E)\left(-\dfrac{\beta}{r_\pi}\right)} = -\frac{\beta}{r_\pi + \beta R_E} \tag{4.33}$$

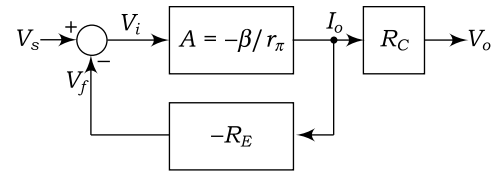


Fig. 4.35 Block-diagram representation of a BJT amplifier with current-series feedback

Voltage gain with feedback is

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_C}{V_s} = \frac{I_o}{V_s} R_C = \left(-\frac{\beta}{r_\pi + \beta R_E}\right) R_C = -\frac{\beta R_C}{r_\pi + \beta R_E} \tag{4.34}$$

Input and output impedances without feedback

$$Z_i = R_B \| r_\pi, \text{ assuming } R_E = 0$$

$$Z_o = R_C$$

Input and output impedances with feedback

$$Z_{if} = Z_i(1+BA) = r_\pi + \beta R_E \tag{4.35}$$

$$Z_{of} = Z_o(1+BA) = R_C\left(1 + \frac{\beta R_E}{r_\pi}\right) \tag{4.36}$$

It is clear from the above expressions that input and output impedances are increased in current-series feedback amplifier.

Example 4.16 Determine the voltage gain of a BJT amplifier with current-series feedback as depicted in Fig. 4.33 with the following parameters: $\beta = 100$, $r_m = 800\ \Omega$, $R_C = 2.47\ \text{k}\Omega$, $R_E = 470\ \Omega$, and $R_B = 470\ \Omega$.

Sol. Amplifier gain is

$$A = \frac{I_o}{V_s} = -\frac{\beta}{r_\pi + \beta R_E} = -\frac{100}{800 + 100 \times 470} = -0.00209$$

Voltage gain with feedback is

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_C}{V_s} = \frac{I_o}{V_s} R_C = \left(-\frac{\beta}{r_\pi + \beta R_E}\right) R_C = -\frac{\beta R_C}{r_\pi + \beta R_E}$$

$$= -\frac{100 \times 2.47 \times 10^3}{800 + 100 \times 470} = -5.167$$

4.9.4 Voltage-Shunt Feedback

Figure 4.36 shows the voltage-shunt feedback. Its equivalent circuit is illustrated in Fig. 4.37.

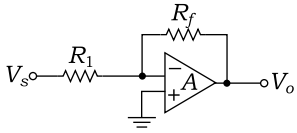


Fig. 4.36 Voltage-shunt negative feedback amplifier

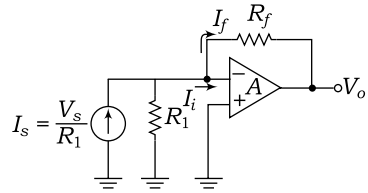


Fig. 4.37 Equivalent circuit of voltage-shunt negative feedback amplifier

The gain of the amplifier

$$A = \frac{V_o}{I_i}, \quad A \to \infty \text{ as } I_i = 0 \tag{4.37}$$

The feedback gain is $\beta = \dfrac{I_f}{V_o} = -\dfrac{1}{R_f}$

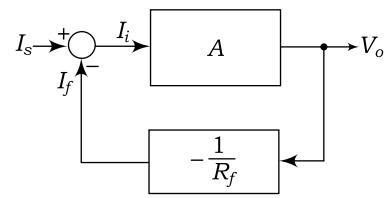


Fig. 4.38 Block-diagram representation of voltage-shunt negative feedback amplifier

The block-diagram representation of Fig. 4.37 is depicted in Fig. 4.38.

The overall loop gain is

$$A_f = \frac{V_o}{I_s} = \frac{A}{1 + \beta A} = \frac{A}{1 - \dfrac{A}{R_f}} = -R_f \quad \text{as } A \to \infty \text{ and } I_i = 0 \tag{4.38}$$

The voltage gain is

$$A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s}\frac{I_s}{V_s} = -\frac{R_f}{R_1} \quad \text{as } \frac{V_o}{I_s} = -R_f \text{ and } \frac{I_s}{V_s} = \frac{1}{R_1} \tag{4.39}$$

Example 4.17 Figure 4.39 shows the transistor feedback amplifier circuit and it has the following parameters:

$$h_{ie} = 1K, \text{ and } h_{fe} = 50,\ R_C = 10K,\ R_B = 1K,\ R_F = 100K$$

Determine the topology of the feedback and compute $\frac{V_o}{V_S}$, R_{if} and R_{of}.

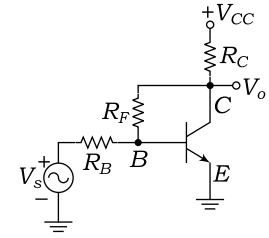


Fig. 4.39

Sol. The feedback signal is proportional to output voltage and is connected in shunt with input signal. Therefore, this circuit is a voltage-shunt topology.

The resistance R_F is connected between the collector terminal of the transistor (output) and the base terminal of the transistor (input). Applying Miller's theorem, the R_F can be replaced by the two resistances R_1 and R_2 as shown in Fig. 4.40. The values of R_1 and R_2 are given below:

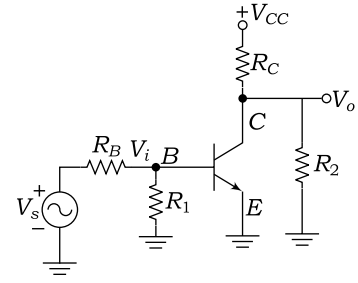


Fig. 4.40

$$R_1 = \frac{R_F}{1-K} \text{ and } R_2 = R_F \frac{K}{K-1}$$

where, $K = \dfrac{\text{Collector voltage}}{\text{Base voltage}} = \dfrac{\text{Output voltage}}{\text{Input voltage}}$

= Voltage gain of amplifier = A_V

The effective load resistance $R_L = R_C \parallel R_2$

where $R_2 = \dfrac{100K \times A_V}{A_V - 1}$ and $R_C = 10K$

$$R_L = \frac{10K \times \dfrac{100K \times A_V}{A_V - 1}}{10K + \dfrac{100K \times A_V}{A_V - 1}} = \frac{1000 \times A_V}{110A_V - 10} \text{ k-ohms}$$

The voltage gain of the transistor

$$A_V = -\frac{h_{fe}}{h_{ie}} R_L = -\frac{50}{1000} R_L = -\frac{50}{1000} \times \frac{1000 \times A_V}{110A_V - 10} \times 1000$$

or $$A_V = -\frac{50A_V}{110A_V - 10} \times 1000$$

or $$110A_V - 10 = -50 \times 1000$$

or $$A_V = \frac{-50 \times 1000 + 10}{110} = -454.45$$

The value of $$R_1 = \frac{R_F}{1-K} = \frac{R_F}{1-A_V} = \frac{100K}{1-(-454.45)} = 219.56 \text{ ohms}$$

The value of $$R_2 = R_F \frac{K}{K-1} = R_F \frac{A_V}{A_V - 1} = 100K \frac{(-454.45)}{-454.45 - 1} \approx 100K$$

$$R_i = h_{ie} = 1K$$

$$R_{ieff} = R_1 \| R_i = 219.56\ \Omega \| 1K = 180 \text{ ohms}$$

The voltage gain $\frac{V_o}{V_S} = \frac{V_o}{V_i} \times \frac{V_i}{V_S} = A_V \times \frac{V_i}{V_S}$

The $\frac{V_i}{V_S} = \frac{R_{ieff}}{R_{ieff} + R_s} = \frac{180}{180 + 1000} = 0.1525$

The voltage gain is $\frac{V_o}{V_S} = A_V \times 0.1525 = (-454.45) \times 0.1525 = -69.30$

The output impedance $R_{of} = R_C \| R_2 = 10K \| 100K = 9.09K$

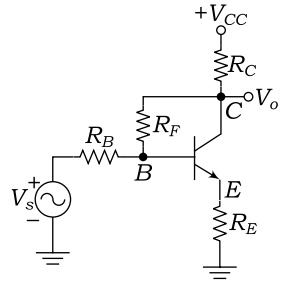


Fig. 4.41

Example 4.18 Figure 4.41 shows the transistor feedback amplifier circuit and it has the following parameters:

$h_{ie} = 2K$, and $h_{fe} = 100$, $R_C = 10K$, $R_E = 1K$, $R_B = 1K$, $R_F = 100K$

Determine the topology of the feedback and compute $\frac{V_o}{V_S}$, R_{if} and R_{of}.

Sol. The feedback signal is proportional to output voltage and is connected in shunt with input signal. Therefore, this circuit is a voltage-shunt topology.

The resistance R_F is connected between the collector terminal of the transistor (output) and the base terminal of the transistor (input). Applying Miller's theorem, the R_F can be replaced by the two resistances R_1 and R_2 as depicted in Fig. 4.42. The resistances R_1 and R_2 can be expressed as

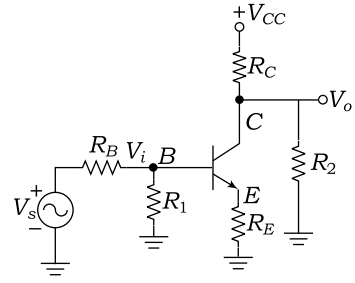


Fig. 4.42

$$R_1 = \frac{R_F}{1 - K} \text{ and } R_2 = R_F \frac{K}{K - 1} \quad \text{where } K = A_V$$

The effective load resistance $R_L = R_C \| R_2$

where, $R_2 = \frac{100K \times A_V}{A_V - 1}$ and $R_C = 10K$

$$R_L = \frac{10K \times \frac{100K \times A_V}{A_V - 1}}{10K + \frac{100K \times A_V}{A_V - 1}} = \frac{1000 \times A_V}{110A_V - 10} \text{ k-ohms}$$

The input resistance is

$$R_i = h_{ie} + (1 + h_{fe})R_E = 2K + (1 + 100)1K = 103 \text{ k-ohms}$$

The voltage gain of the transistor is

$$A_V = -\frac{h_{fe}}{h_{ie}} R_L = -\frac{100}{2000} R_L = -\frac{100}{2000} \times \frac{1000 \times A_V}{110A_V - 10} \text{ k-ohms}$$

$$= -\frac{50A_V}{110A_V - 10} \times 1000$$

or $$110A_V - 10 = -50 \times 1000$$

or $$A_V = \frac{-50 \times 1000 + 10}{110} = -454.45$$

The value of $$R_1 = \frac{R_F}{1-K} = \frac{R_F}{1-A_V} = \frac{100K}{1-(-454.45)} = 219.56 \text{ ohms}$$

The value of $$R_2 = R_F \frac{K}{K-1} = R_F \frac{A_V}{A_V - 1} = 100K \frac{(-454.45)}{-454.45 - 1} \approx 100 \text{ k-ohms}$$

$$R_{ieff} = R_1 \| R_i = 219.56 \text{ ohms} \| 103 \text{ k-ohms} = 219.09 \text{ ohms}$$

The voltage gain $$\frac{V_o}{V_S} = \frac{V_o}{V_i} \times \frac{V_i}{V_S} = A_V \times \frac{V_i}{V_S}$$

The $$\frac{V_i}{V_S} = \frac{R_{ieff}}{R_{ieff} + R_s} = \frac{219.09}{219.09 + 1000} = 0.179$$

The voltage gain $$\frac{V_o}{V_S} = A_V \times 0.179 = (-454.45) \times 0.179 = -81.34$$

The output impedance $R_{of} = R_C \| R_2 = 10K \| 100K = 9.09K$

Example 4.19 Figure 4.43 shows the transistor feedback amplifier circuit and it has the following parameters:

$h_{ie} = 2K$, and $h_{fe} = 100$, $R_{C1} = 10K$, $R_{C2} = 1K$, $R_E = 0.1K$, $R_S = 2K$, $R_f = 1K$

Determine the topology of the feedback, gain A_V and R_{if}.

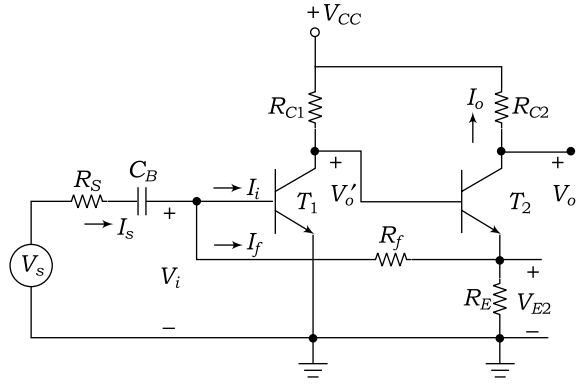


Fig. 4.43 Emitter-to-base feedback amplifier circuit

Sol. In Fig. 4.43, the transistors T_1 and T_2 are connected in cascade. The feedback resistance R_f is connected between the emitter of T_2 and base of T_1 to provide feedback path. The output voltage of the transistor T_1 is the output voltage of first stage amplifier, V_O and it is 180° out of phase from the input voltage V_i. The voltage across R_E is V_{E2}. The output voltage V_o is connected in series with the voltage V_{E2}. The topology of the feedback is current-shunt or series shunt feedback.

The source current is the sum of input current and feedback current i.e. $I_S = I_i + I_f$.

The feedback current is equal to

$$I_f = \frac{V_i - V_{E2}}{R_f}$$

Since, $$V_{E2} >> V_i, I_f = -\frac{V_{E2}}{R_f}$$

After neglecting the base current of the transistor T_2, we obtain the emitter voltage

$$V_{E2} = (I_f - I_o)R_{E2}$$

Then $$I_f = -\frac{V_{E2}}{R_f} = -\frac{(I_f - I_o)R_{E2}}{R_f}$$

or $$I_f = \frac{R_{E2}}{R_f + R_{E2}} I_o$$

As feedback current is directly proportional to the output current I_o, the feedback configuration is current-shunt or series shunt feedback.

This feedback amplifier circuit can be analysed by using Miller's theorem. It is possible to replace the feedback resistance R_f with two equivalent resistances R_1 and R_2 as shown in Fig. 4.44.

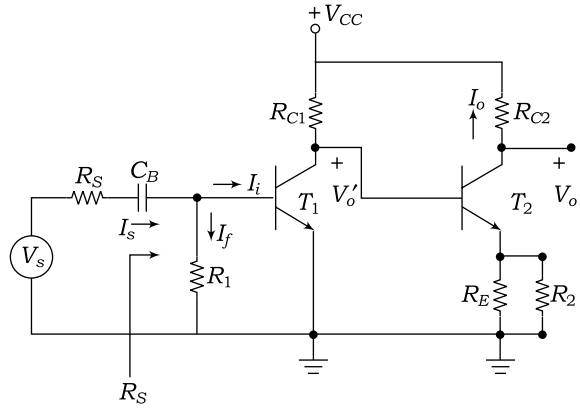


Fig. 4.44 Miller's theorem applied to emitter-to-base feedback amplifier circuit of Fig. 4.43

The values of R_1 and R_2 are

$$R_1 = \frac{R_f}{1 - A'_V} \text{ and } R_2 = \frac{R_f}{1 - 1/A'_V}$$

where, $A_V' = \frac{V_{E2}}{V_i} =$ voltage gain from base of the transistor T_1 to the emitter of the transistor T_2.

As $A_V' >> 1$, the effective emitter resistance is

$$R_E' = R_E \| R_f = 100 \| 1000\ \Omega = 90.909\ \Omega$$

The input resistance of T_2 is

$$R_{i2} = h_{ie} + (1 + h_{fe}) R_E' = 2000 + (1 + 100)90.909\ \Omega = 11181.809\ \Omega$$

The voltage gain from base to collector of the transistor T_2 is

$$A_{V2} = 1 - \frac{h_{ie}}{R_{i2}} = 1 - \frac{2000}{11181.809} = 0.821$$

The effective load resistance of T_1 is

$$R_L' = R_{C1} \| R_{i2} = 10{,}000 \| 11181.809\ \Omega = 5278.96\ \Omega$$

The voltage gain of the transistor T_1 from base to collector is

$$A_{V1} = -\frac{h_{fe}}{h_{ie}} R_L' = -\frac{100}{2000} \times 5278.96 = -263.94$$

The voltage gain $A_V' = A_{V1} \times A_{V2} = (-263.94) \times 0.821 = -216.70$

The value of R_1 is

$$R_1 = \frac{R_f}{1 - A_V'} = \frac{1000}{1 + 216.70} = 4.59\ \Omega$$

The input impedance $R_{if} = R_1 \| R_{i1} = R_1 \| h_{ie} = 4.59 \| 2000 = 4.579\ \Omega$

The resistance of signal source is

$$R_S + R_{if} = (2000 + 4.579)\ \Omega = 2004.579\ \Omega$$

4.10 STABILITY OF FEEDBACK AMPLIFIER

In this chapter, negative feedback amplifier has been discussed so far. The gain A and phase shift of a feedback amplifier are function of frequency. For negative feedback operation, $|1 + \beta A| > 1$. If $|1 + \beta A| < 1$, the feedback becomes positive or regenerative. During positive feedback, the overall gain A_f is greater than A. Therefore, regeneration means increasing the amplification of amplifier.

If an amplifier is designed to operate as negative feedback at a specified frequency and it oscillates at some other frequency then the amplifier is not very useful for that specified applications. As a result, feedback amplifiers must be designed in such a way that the circuit must be stable over a wide range of frequency or all frequencies. Otherwise, transient response makes the amplifier unstable. Any feedback amplifier will be stable, when transient disturbance produces a response, but the amplitude of response must be decay with time. The feedback system will be unstable if any transient disturbance persists indefinitely and output response increases with time, but amplitude of output response is limited by nonlinearity of the circuit parameters. For any stable system, all poles of the transfer function, or the zeros of $(1 + \beta A)$ must be in the left half of the complex frequency plane. The stability of amplifier can be investigated using the Nyquist Criterion.

4.10.1 Nyquist Criterion

The gain A and phase shift of a feedback amplifier are function of frequency. As βA is also a complex quantity and function of frequency, different points on the complex plane can be obtained corresponding to different values of frequency. When frequency is varied from $+\infty$ to $-\infty$, βA is plotted on a complex plane with the real component along the X-axis and the imaginary component along the Y-axis and a closed curve is formed by the locus of $(1 + \beta A)$. The locus of $|1 + \beta A|$ is a circle of unit radius with the center at point $(-1 + j0)$. This plot is known as Nyquist plot as shown in Fig. 4.45.

The Nyquist criterion states that the amplifier is unstable if the Nyquist plot encloses the point $(-1 + j0)$, and the amplifier is stable if the curve does not enclose the point $(-1 + j0)$. The Nyquist criterion for positive and negative feedback is represented in the complex plane as depicted in Fig. 4.45. Figure 4.46 shows the frequency response of a feedback amplifier in the complex plane. When frequency is varied from 0 to f_1, the feedback is negative. During the frequency range from f_1 to ∞, the feedback is positive as shown in Fig. 4.46.

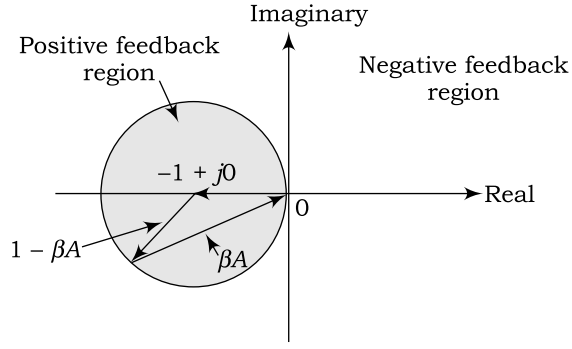


Fig. 4.45 Locus of $|1 + \beta A|$

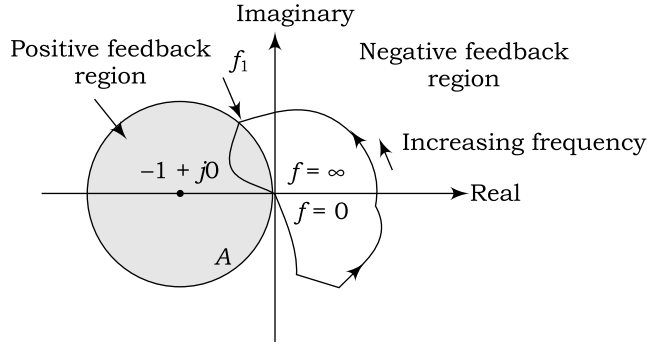


Fig. 4.46 Locus of βA in the complex plane for a feedback circuit which acts as negative feedback from $f = 0$ to $f = f_1$ and acts as positive feedback form $f = f_1$ to $f = \infty$

At any frequency range, if the locus of βA does not enclose the point $(-1 + j0)$, the feedback is negative and amplifier is stable. When the locus of βA enclose the point $(-1 + j0)$, the feedback is positive and amplifier is unstable as illustrated in Fig. 4.47. In this case, positive feedback amplifier acts as an oscillator whenever the Nyquist criterion is satisfied.

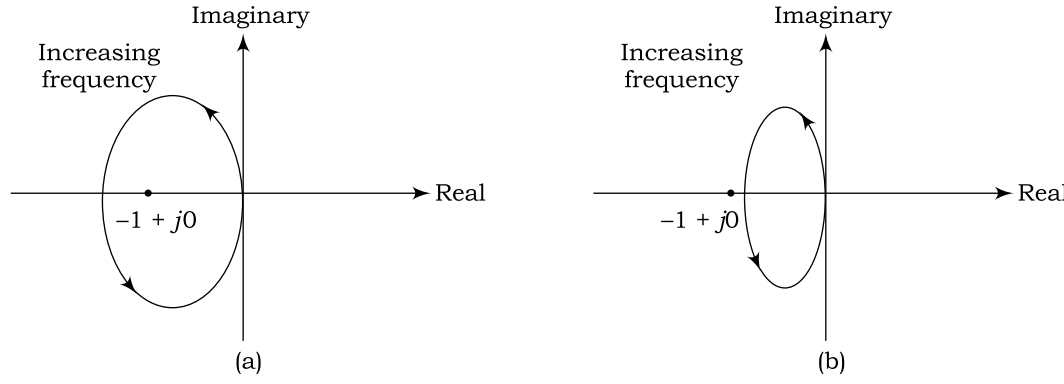


Fig. 4.47 Nyquist plot of feedback amplifier: (a) Unstable (b) Stable

Example 4.20 A negative feedback amplifier has open-loop gain of 10^5 and closed-loop gain of 100. (i) Determine feedback factor. (ii) If a manufacturing error results in a reduction of open-loop gain to 10^3, what will be the resulting closed-loop gain? (iii) What is the percentage change in closed-loop gain corresponding to this change in open-loop gain?

Sol. (i) $A_f = \dfrac{A}{1+\beta A}$ or, $100 = \dfrac{10^5}{1+10^5\beta}$ or, $10^5\beta = \dfrac{10^5}{100} - 1 = 999$

Feedback factor $\beta = \dfrac{999}{10^5} = 0.00999$

(ii) $A_f = \dfrac{10^3}{1+0.00999\times 103} = \dfrac{10^3}{2.02897} = 50.7646$

(iii) Percentage change in closed-loop gain = $\dfrac{100-50.7646}{100}\times 100\% = 49.2354\%$

Example 4.21 If the gain of an amplifier is 90 dB and 60 dB without and with feedback respectively, find the feedback factor of the amplifier.

Sol. Voltage gain with feedback is A_{vf}

Then $20\log_{10}(A_{vf}) = 60$ dB or, $A_{vf} = \text{Antilog}_{10}\left(\dfrac{60}{20}\right) = \text{Antilog}_{10}(3) = 1000$

Voltage gain with feedback is A_v.

Then $20\log_{10}(A_v) = 90$ dB or, $A_v = \text{Antilog}_{10}\left(\dfrac{90}{20}\right) = \text{Antilog}_{10}(4.5) = 31622$

Feedback factor of the amplifier = $\dfrac{A_v - A_{vf}}{A_v A_{vf}} = \dfrac{31622-1000}{31622\times 1000} = 9.68\times 10^{-4}$

Example 4.22 An amplifier has a midband gain of 1500 and a bandwidth of 4 MHz. The midband gain reduces to 150 when negative feedback is applied. Determine the value of feedback factor and the bandwidth.

Sol. $A_{vm} = 1500, A_{vmf} = 150$

We know that $A_{vmf} = \dfrac{A_{vm}}{1+\beta A_{vm}}$. Then $1+\beta A_{vm} = \dfrac{A_{vm}}{A_{vmf}} = \dfrac{1500}{150} = 10$

Bandwidth with feedback $BW_f = (1+\beta A_{vm}) \times BW = 10 \times 4 \text{ MHz} = 40 \text{ MHz}$

Example 4.23 An amplifier has a voltage gain of 10,000. Its input impedance is $1k$ and output impedance is $40k$. Determine the voltage gain, input and output impedance of the circuit if 5% of the amplifier is fed in the form of series negative voltage feedback.

Sol. $A = 10{,}000, Z_i = 1k, Z_o = 40k$

$$\beta = 5\% = \frac{5}{100} = 0.05$$

Gain with feedback $A_f = \dfrac{A}{1+\beta A} = \dfrac{10{,}000}{1+0.05\times 10{,}000} = 19.96$

Input impedance with feedback $Z_{if} = Z_i(1+\beta A) = 1k \times (1+0.05\times 10000) = 501 \text{ k}\Omega$

Output impedance with feedback $Z_{of} = \dfrac{Z_o}{1+\beta A} = \dfrac{40k}{1+0.05\times 10000} = 79.84\ \Omega$

Example 4.24

(i) The open-loop gain of an amplifier changes by 20% due to changes in the parameters of the active amplifying device. If a change of gain by 2% is allowable, what type of feedback has to be applied?

(ii) If the amplifier gain with feedback is 10, find the value of feedback ratio for an open-loop gain of 100.

Sol. (i) In a feedback amplifier $\left|\dfrac{dA_f}{A_f}\right| = \dfrac{1}{|1+\beta A|}\left|\dfrac{dA}{A}\right|$

where A_f = Closed-loop gain, A = Open-loop gain and β = Feedback ratio

Here, $\dfrac{dA_f}{A_f} = 2\% = \dfrac{2}{100}$ and $\dfrac{dA}{A} = 20\% = \dfrac{20}{100}$

Therefore, $\dfrac{2}{100} = \dfrac{20}{100}\dfrac{1}{1+\beta A}$

Then $\beta A = 9$

As $\beta A > 1$, negative feedback has to be applied.

(ii) The overall loop gain of a feedback amplifier is

$$A_f = \frac{A}{1+\beta \cdot A}$$

If $A_f = 10$, $A = 100$, we can write $10 = \dfrac{100}{1+100\beta}$

Then $\beta = \dfrac{9}{100} = 0.09$

Example 4.25 An FET amplifier in the common-source configuration uses a load resistance of 150 kW. The ac drain resistance of the device is 100 kW and the transconductance is 0.5 mA/V. What is the voltage gain of the amplifier?

Sol. Amplification factor $\mu = r_d \times g_m$ where r_d = Drain resistance, and g_m = Transconductance

Given $g_m = 0.5$ mA/V, $r_d = 100$ kΩ and $R_L = 150$ kΩ

The voltage gain

$$A_V = \frac{V_O}{V_i} = \frac{g_m r_d . R_L}{R_L + r_d}$$

$$= \frac{0.5 \times 10^{-3} \times 100 \times 10^3 \times 150 \times 10^3}{(150 + 100) \times 10^3} = 30$$

Example 4.26 An amplifier has a voltage gain of 200. The gain is reduced to 50 when negative feedback is applied. Determine feedback factor and express the amount of feedback in dB.

Sol. Given: A = 200, A_f = 50

The closed-loop gain of a feedback amplifier is

$$A_f = \frac{A}{1 + \beta \cdot A}$$

or $$50 = \frac{200}{1 + 200\beta}$$

Therefore, $\beta = \frac{3}{200} = 0.015$

The amount of feedback = $\frac{A_f}{A} = \frac{50}{200} = \frac{1}{4}$

The amount of feedback in dB = $20 \log_{10} \frac{A_f}{A} = 20 \log_{10} \left(\frac{1}{4}\right)$

$= -20\log_{10} 4$ dB = –12.0411 dB

Example 4.27 The variation of open-loop gain of an amplifier having internal gain 1000 is 10% , but for a specific use, only 1% gain variation is allowed. Design a feedback amplifier for this purpose and find the corresponding feedback fraction and overall gain.

Sol. In a feedback amplifier

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1 + \beta A|} \left|\frac{dA}{A}\right|$$

where A_f = Closed-loop gain, A = Open-loop gain, and β = Feedback ratio

Given: $\frac{dA_f}{A_f} = 1\% = \frac{1}{100}$ and $\frac{dA}{A} = 10\% = \frac{10}{100}$

Therefore, $\frac{1}{100} = \frac{10}{100} \frac{1}{1 + \beta A}$

or $\beta A = 9$

As $\beta A > 1$, negative feedback has to be applied.

The feedback fraction is $\beta = \frac{9}{A} = \frac{9}{1000} = 0.009$ as $A = 1000$

The overall gain is

$$A_f = \frac{A}{1 + \beta \cdot A} = \frac{1000}{1 + (0.009 \times 1000)} = 100$$

Example 4.28 An amplifier with negative (–ve) feedback provides an output voltage of 5 V with an input voltage of 0.2. On removal of feedback, it needs only 0.1 V input voltage to give the same output. Find out the (i) gain without feedback, (ii) gain with feedback, and (iii) feedback ratio.

Sol. Output voltage $V_o = 5$ V and input voltage $V_i = 0.2$ V with feedback.

Without feedback, input voltage $V_i = 0.1$ V

(i) The gain without feedback is $A_f = \frac{V_o}{V_i} = \frac{5}{0.1} = 50$

(ii) The gain with feedback is $A_f = \frac{V_o}{V_i} = \frac{5}{0.2} = 25$

(iii) The overall gain is $A_f = \frac{A}{1 + \beta \cdot A}$

where A_f = Closed-loop gain, A = Open-loop gain, and β = Feedback ratio

Therefore, $25 = \frac{50}{1 + \beta \times 50}$ and $\beta = \frac{1}{50}$

Example 4.29 An *RC* coupled amplifier has $A_v = 50{,}000$, $f_H = 20$ kHz, $f_L = 30$ Hz. A resistive voltage negative feedback is added such that, $\beta = 5 \times 10^{-6}$. Determine A_{vf}, f_{Hf} and f_{Lf}.

Sol. $$A_{vf} = \frac{A_v}{1 + \beta A_v} = \frac{50{,}000}{1 + 5 \times 10^{-6} \times 50{,}000} = 40000$$

$$f_{Hf} = f_H(1 + \beta A_v) = 20 \times (1 + 5 \times 10^{-6} \times 50{,}000) \text{ kHz} = 25 \text{ kHz}$$

$$f_{Lf} = \frac{f_L}{1 + \beta A_v} = \frac{30}{1 + 5 \times 10^{-6} \times 50{,}000} \text{Hz} = 24 \text{ Hz}$$

Review Exercises

Short-Answer Questions

1. What is a feedback amplifier?

Ans. A feedback amplifier is an electronic circuit in which the output signal is sampled and fed back to the input to generate an error signal which drives the amplifier.

2. What is the difference between series feedback and shunt feedback?

Ans. In series feedback, the feedback signal is connected in series with the input voltage signal. In shunt feedback, the feedback signal is connected in parallel with an input current source.

3. What is the difference between current and voltage feedback?

Ans. In voltage feedback, a fraction of output voltage is used as input to the feedback network. In current feedback, the trapping off a fraction of output current is through the feedback network.

4. What is the effect of negative feedback on the gain of an amplifier?

Ans. Due to negative feedback, the amplifier gain decreases by a factor $(1 + \beta A)$.

5. What is the effect of negative feedback on the bandwidth and gain of an amplifier?

Ans. When negative feedback is incorporated in an amplifier, the bandwidth will be increased by a factor $(1 + \beta A)$ but gain is reduced.

6. What is the effect of negative feedback on the input impedance and output impedance of voltage shunt feedback amplifier?

Ans. Due to negative feedback, both the input impedance and output impedance of a voltage-shunt feedback amplifier decreases by a factor $(1 + \beta A)$.

7. What is the effect of negative feedback on the input impedance and output impedance of a voltage-series feedback amplifier?

Ans. Due to negative feedback, the input impedance of a voltage-series feedback amplifier increases by a factor $(1 + \beta A)$ whereas the output impedance of voltage-series feedback amplifier decreases by a factor $(1 + \beta A)$.

8. Why is voltage-series feedback extensively used in cascade amplifier?

Ans. The cascade amplifier should have high input impedance and low output impedance. As a voltage-series feedback circuit has high input impedance and low output impedance, voltage-series feedbacks are extensively used in cascade amplifiers.

9. What is an emitter follower?

Ans. In an emitter follower, output and input voltages are approximately equal in magnitude and phase. Therefore, emitter output voltage follows the input signal in an emitter follower.

Multiple-Choice Questions

1. A negative feedback amplifier has a gain A and feedback path gain is β. What will be the overall gain of the amplifier?

   (a) $\frac{A}{1+\beta A}$ (b) $\frac{1+A}{1+\beta A}$ (c) $\frac{A}{1-\beta A}$ (d) $\frac{1-\beta A}{A}$

2. A positive feedback amplifier has a gain A and feedback path gain is β. What will be the overall gain of the amplifier?

   (a) $\frac{A}{1-\beta A}$ (b) $\frac{1+A}{1+\beta A}$ (c) $\frac{A}{1+\beta A}$ (d) $\frac{1-\beta A}{A}$

3. The transfer characteristics of a voltage amplifier is

   (a) $A_v = \frac{V_o}{V_s}$ (b) $A_I = \frac{I_o}{I_s}$ (c) $g_m = \frac{I_o}{V_s}$ (d) $r_m = \frac{V_o}{I_s}$

4. An amplifier has gain of –1000 and feedback of $\beta = -0.1$. If it had a gain change of 20% due to temperature, what will be the change in gain of the feedback amplifier?
   (a) 1% (b) 2% (c) 0.5% (d) 0.2%
5. An amplifier has an open-loop gain of 100, an input impedance of 1 kΩ and an output impedance of 100 Ω. A feedback network with a feedback factor of 0.5 is connected in a voltage-series feedback mode. The new input and output impedance are
   (a) 51 kΩ and 2 Ω (b) 510 kΩ and 20 Ω
   (c) 5.1 kΩ and 200 Ω (d) 5 kΩ and 100 Ω
6. An operational amplifier has an open-loop gain of 10^4 and open-loop upper cut-off frequency of 10 Hz. If this operational amplifier is connected as an amplifier with a closed-loop gain of 100, what will be the new upper cut-off frequency?
   (a) 1000 Hz (b) 100 Hz
   (c) 10 Hz (d) 1 Hz
7. Figure 4.48 shows the feedback amplifier circuit. What is the type of feedback used in this circuit?
   (a) Voltage-series feedback
   (b) Voltage-shunt feedback
   (c) Current-series feedback
   (d) Current-shunt feedback

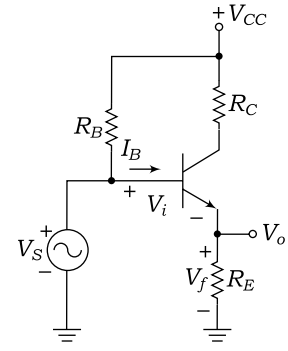


Fig. 4.48

8. Which topology of feedback amplifier has very high input and output impedances?
   (a) Voltage-series feedback (b) Voltage-shunt feedback
   (c) Current-series feedback (d) Current-shunt feedback
9. An amplifier with midband gain $A = 500$ has a negative feedback $\beta = \frac{1}{100}$. If the upper cut-off without feedback is 600 Hz then with feedback, it would become
   (a) 3000 Hz (b) 300 kHz (c) 30 Hz (d) 3 Hz
10. The feedback factor of the circuit shown in Fig. 4.49 is
    (a) $\frac{10}{15}$ (b) $\frac{5}{15}$
    (c) $\frac{1}{10}$ (d) $\frac{1}{5}$

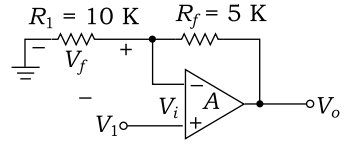


Fig. 4.49

11. Figure 4.50 shows an OP–AMP feedback amplifier circuit. What is the type of feedback shown there?
    (a) Voltage-series feedback
    (b) Voltage-shunt feedback
    (c) Current-series feedback
    (d) Current-shunt feedback

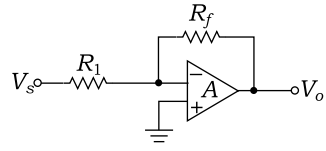


Fig. 4.50

12. In a common-emitter amplifier, the unbiased emitter resistance provides
    (a) voltage-series feedback (b) voltage-shunt feedback
    (c) current-series feedback (d) current-shunt feedback
13. The amount of feedback in a negative feedback amplifier is expressed as
    (a) $20 \log_{10} \left| \frac{1}{1+\beta A} \right|$ (b) $20 \log_{10} \left| \frac{1}{1-\beta A} \right|$
    (c) $40 \log_{10} \left| \frac{1}{1+\beta A} \right|$ (d) $40 \log_{10} \left| \frac{1}{1-\beta A} \right|$
14. The input and output impedances of a current-shunt feedback amplifier is
    (a) $\frac{Z_i}{1+\beta A}$ and $Z_o(1+\beta A)$ (b) $Z_i(1+\beta A)$ and $\frac{Z_o}{1+\beta A}$
    (c) $\frac{Z_i}{1+\beta A}$ and $\frac{Z_o}{1+\beta A}$ (d) $Z_i(1+\beta A)$ and $Z_o(1+\beta A)$
15. The advantages of a negative feedback amplifier are
    (a) high input impedance (b) increase in gain stability
    (c) low output impedance (d) all of these
16. A transconductance amplifier has
    (a) high input impedance and high output impedance
    (b) high input impedance and low output impedance
    (c) low input impedance and low output impedance
    (d) low input impedance and high output impedance
17. Voltage-shunt feedback amplifier is a
    (a) transconductance amplifier (b) transreistive amplifier
    (c) voltage amplifier (d) current amplifier
18. A transresistive amplifier has
    (a) low input impedance and high output impedance
    (b) high input impedance and low output impedance
    (c) low input impedance and low output impedance
    (d) high input impedance and high output impedance
19. Negative feedback increases the performance parameters except
    (a) gain (b) input impedance (c) noise distortion (d) 3 dB frequency
20. The transfer characteristic of a transconductance amplifier is
    (a) $g_m = \frac{I_o}{V_s}$ (b) $A_i = \frac{I_o}{I_s}$ (c) $A_v = \frac{V_o}{V_s}$ (d) $r_m = \frac{V_o}{I_s}$
21. Negative feedback in amplifier
    (a) increases bandwidth and increases gain (b) increases bandwidth and decreases gain
    (c) decreases bandwidth and decreases gain (d) decreases bandwidth and increases gain

Review Questions

1. Define feedback amplifier. What are the types of feedback amplifiers? Write advantages of feedback amplifiers.
2. What do you mean by negative feedback and positive feedback? Derive the overall gain of negative feedback and positive feedback amplifiers. What is the amount of feedback of a negative feedback amplifier?
3. Explain the following amplifiers:
   (a) Voltage amplifier
   (b) Current amplifier
   (c) Transconductance amplifier
   (d) Transresistive amplifier
4. Draw a schematic block diagram of a feedback amplifier and the working principle of a feedback amplifier in detail.
5. Justify the statement "*Negative feedback can reduce the gain of an amplifier*".
6. What are the different topologies of feedback amplifiers? Explain any one feedback topology with an example.
7. Draw a voltage-series feedback amplifier circuit and derive the following parameters:
   (a) Overall amplifier gain
   (b) Input impedance
   (c) Output impedance
8. Draw the circuit diagram of an emitter-follower circuit. What type of feedback topology is used in this circuit? Derive the overall loop gain of the amplifier.
9. Give a list of properties of a feedback amplifier
10. Explain the following terms:
    (a) Gain stability of a negative feedback amplifier
    (b) Effect of negative feedback on bandwidth
    (c) Effect on input impedance of a series-series feedback amplifier
    (d) Effect on output impedance of a voltage-series feedback amplifier
11. Define the following terminologies:
    (a) Feedback ratio
    (b) Feedback factor
    (c) Amount of feedback in dB
    (d) Phase distortion of negative feedback amplifier
12. Calculate the gain of a negative feedback amplifier if $A = -1000$ and $\beta = -1/10$.
13. When the gain of an amplifier changes from a value of –1000 by 10%, determine the gain change if the amplifier is used in a negative feedback circuit and $\beta = -1/50$.
14. Determine the gain, input and output impedances of a voltage-series feedback amplifier having $A = -200$, $R_i = 1.5$ k-ohms, $R_o = 100$ k-ohms and $\beta = -1/50$.
15. Compute the gain with and without feedback for an FET amplifier as shown in Fig. 4.51 for $R_1 = 500$ k-ohms, $R_2 = 250$ k-ohms, $R_o = 40$ k-ohms, $R_D = 8$ k-ohms and $g_m = 1000$ µs.

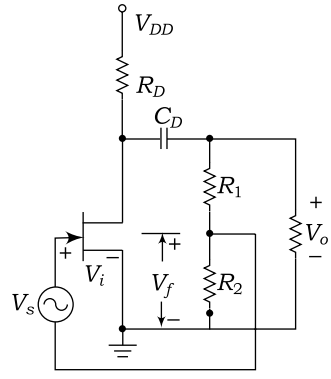


Fig. 4.51

16. Figure 4.52 shows a BJT amplifier circuit. What type of feedback topology is used in this circuit? Calculate the gain, input and output impedance with feedback R_B = 100 k-ohms, R_E = 1.2 k-ohms, R_C = 4.7 k-ohms, h_{fe} = 100 and h_{ie} = 1000.

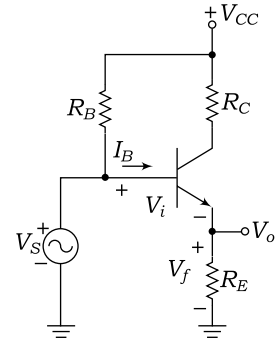


Fig. 4.52

17. An amplifier with a gain of 2500 has an output voltage of 10 V. A negative feedback is provided to reduce the gain to 10%. What should be the gain of the feedback path?
18. A feedback amplifier consists of four amplifying blocks and each amplifying block has a gain of 10.
    (a) What should be the gain of the feedback path in order to maintain an overall gain of 75?
    (b) If the gain of each amplifier block has been reduced to 80% of actual value due to parameter variation, what is the percentage change in the overall gain of the feedback amplifier?
19. An amplifier has an open-loop gain of A = 250.
    (a) Calculate the feedback path gain to provide overall gain of A_f = 100.
    (b) When A is increased by 10%, calculate the new A_f. What is the percentage change in A_f?
20. An amplifier has gain of –20000 and feedback of β = –0.1. Due to temperature rise, gain change is about 10%. What will be the change in gain of the feedback amplifier?
21. In a voltage-series feedback amplifier A = 5000, R_i = 100 Ω, R_o = 100 kΩ and β = 0.1, compute input impedance, and output impedance of feedback amplifier.
22. Determine the overall loop gain, and input and output impedances for an amplifier in a current-series feedback amplifier with A = 1000, R_i = 2 kΩ, R_o = 50 kΩ and β = 0.01.

23. A voltage series feedback amplifier has $A = -1000$, $R_i = 20$ kΩ, $R_o = 100$ kΩ and feedback factor $\beta = -0.2$. (a) Find overall gain, input impedance and output impedance of the feedback amplifier. (b) If the gain has been reduced to –200, what will be the feedback factor?
24. The transistor feedback amplifier circuit is depicted in Fig. 4.53 and it has the following parameters:
$h_{ie} = 2K$, $h_{fe} = 120$, $R_C = 5K$, $R_E = 1K$,
$R_B = 1K$, and $R_F = 100K$.
Determine the topology of the feedback and compute $\frac{V_o}{V_S}$, R_{if} and R_{of}.

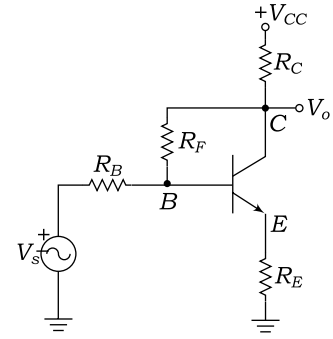


Fig. 4.53

25. Figure 4.54 shows the transistor feedback amplifier circuit and it has the following parameters:
$h_{ie} = 1K$, $h_{fe} = 50$, $R_{C1} = 5K$, $R_{C2} = 1K$,
$R_E = 50$, $R_S = 1K$, $R_f = 1K$.
Explain the topology of this feedback amplifier and determine A_{V1}, A_{V2}, $A_{V,}$ and $R_{if.}$ Assume any missing parameters.

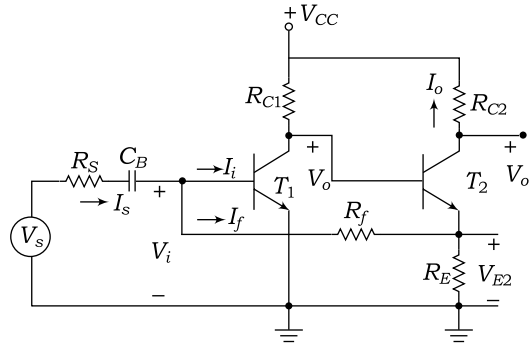


Fig. 4.54

26. Define desensitivity D. What is relation between D and A_f?
27. State the Nyquist criterion of stability of a feedback amplifier.
28. Explain sensitivity of a feedback amplifier.
29. Draw and explain briefly, the circuit of a single stage current series feed-back amplifier. Mention effect of negative feedback on gain and bandwidth.
30. (a) What do you mean by feedback in amplifiers?
    (b) Derive an expression for the closed loop gain of the amplifier with feedback
    (c) Write the effect of negative feedback in an amplifier in terms of gain, bandwidth, input resistance and output resistance with respect to voltage series configuration.
31. (a) Write short notes on the following:
    (a) Four basic feedback topologies
    (b) Classification of feedback amplifier
    (c) Concept of feedback amplifiers

32. What are the advantages and disadvantages of feedback amplifier? What are the types of feedback required for (i) voltage amplifier (ii) current amplifier.

ANSWERS

Multiple-Choice Questions

1. (a)	2. (a)	3. (a)	4. (d)	5. (a)	6. (a)	7. (a)
8. (c)	9. (a)	10. (a)	11. (a)	12. (c)	13. (a)	14. (a)
15. (d)	16. (a)	17. (b)	18. (a)	19. (a)	20. (a)	21. (b)

CHAPTER

5

Oscillators

5.1 INTRODUCTION

An oscillator is an electronic circuit that generates a repetitive electronic signal or periodic waveforms from a few hertz (Hz) to several gigahertz (GHz). In the field of electronics, oscillators are known as *wave generators*. Wave generators use many different circuits and produce output signals such as sinusoidal, square, rectangular, sawtooth and trapezoidal wave shapes. These wave shapes serve different useful purposes in the electronic circuits.

Usually, oscillators use some form of active devices like crystal surrounded by passive devices such as resistors, capacitors and inductors to generate the output signals. For example, oscillators are extensively used in television receivers to reproduce both sound and picture. Another example is that of clock signals generated by oscillators, which regulate computers and quartz-clocks. A low-frequency oscillator generates an ac waveform at a frequency below 20 Hz. These low-frequency oscillators are typically used in audio synthesisers.

In this chapter, classification of oscillators, oscillator operation, Barkhausen criteria, sinusoidal oscillators and relaxation oscillators are discussed elaborately.

5.2 CLASSIFICATION OF OSCILLATORS

Oscillators can be classified depending upon the following parameters as given below:

1. The wave shapes generated by the oscillators
2. The fundamental mechanisms used in oscillators
3. Range of frequency of output signal
4. Type of circuit (based on passive devices used in oscillators)

5.2.1 According to the Wave Shapes Generated by the Oscillators

Generally, oscillators are classified into two broad categories according to wave shapes such as

- Sinusoidal oscillators
- Nonsinusoidal or relaxation oscillators

1. Sinusoidal Oscillators

A sinusoidal oscillator generates a sine-wave output signal. Ideally, the output signal has constant amplitude with fixed frequency. However, in reality, the outcome is always less. The accuracy of oscillators depends on the class of amplifier used, amplifier characteristics, frequency stability and amplitude stability.

A sine-wave generator produces sine-wave signals from audio frequency to ultra-high radio frequency as well as microwave frequency. Low frequency sine-wave oscillators use resistors (R) and capacitors (C) to form a frequency-determining network. These oscillators are known as *RC* oscillators and are widely used in the audio-frequency range.

Some sine-wave oscillators use inductors (L) and capacitors (C) for their frequency-determining network. These types of oscillators are called *LC* oscillators. This oscillator is also known as tank circuit. *LC* oscillators are commonly used in high audio-frequency range.

The third type of sine-wave generators is the crystal oscillators. This oscillator provides excellent frequency stability and are used in mid-audio-frequency range.

2. Nonsinusoidal Oscillators

The nonsinusoidal oscillator generates nonsinusoidal or complex waveforms such as square, rectangular, sawtooth and trapezoidal. As oscillators outputs are generally characterised by a sudden change or relaxation, these oscillators are called *relaxation oscillators*. Usually, the signal frequency of the oscillators is governed by the charge or discharge time of a capacitor in series with a resistor. Sometimes inductors are also used in an oscillator's circuit. Hence, both *RC* and *LC* networks are used for determining the frequency of oscillation. The examples of nonsinusoidal oscillators are multivibrators, sawtooth generators and trapezoidal waveform generators.

5.2.2 According to the Fundamental Mechanisms used in Oscillators

Oscillators can also be classified according to the fundamental mechanisms used in oscillators. Types of oscillators are

1. Feedback oscillators
2. Negative resistance oscillators

1. Feedback Oscillators

In these oscillators, positive feedback is used in feedback amplifier and Barkhausen criteria must be satisfied.

2. Negative Resistance Oscillators

In negative resistance oscillators, the amplifying device has negative resistance to neutralise the positive resistance of oscillators.

5.2.3 According to the Range of Frequency of Output Signal

Oscillators can be classified according to the frequency of output signal generated by oscillators. Usually, oscillators produce signals in the audio-frequency (AF) range and radio-frequency range, and they are known as Audio-Frequency Oscillators (AFO) and Radio-Frequency Oscillators (RFO) respectively. Table 5.1 shows the different types of oscillators according to range of frequency.

Table 5.1 Types of oscillators according to range of frequency

Types of Oscillators	*Frequency Range*	*Example*
Audio frequency oscillators (AFO)	400 Hz to 20 kHz	*RC* oscillators such as Phase-shift and Wien-bridge oscillators
Radio frequency oscillators (RFO)	20 kHz to 30 MHz	*LC* feedback oscillators such as tuned collector, Hartley and Colpitt oscillators
Very high frequency (VHF) oscillators	30 MHz to 300 MHz	Crystal oscillators used in microprocessors, microcontrollers, ASICs, DSP processors and computer mother board
Ultra high frequency (UHF) oscillators	300 MHz to 3 GHz	Bulk Acoustic Wave (BAW) AT cut quartz crystal oscillators
Microwave frequency oscillators	Above 3 GHz	YIG tuned oscillators, oven controlled crystal oscillators

5.2.4 According to the Types of Circuit (Based on passive devices used in Oscillators)

Oscillators can also be classified according to type of circuit as given below:

1. *LC* tuned oscillators
2. *RC* phase-shift oscillators

5.3 THE BASIC OSCILLATOR

Figure 5.1 shows the basic oscillator block diagram. An oscillator can be regarded as an amplifier, which provides its own input signal. It is clear from the block diagram that amplification of signal power occurs from input to output. In any oscillator circuit, a portion of the output is fed back to the input. Enough power must be fedback to the input for the oscillator to drive itself as a signal generator. Therefore, the oscillator must be self driven and the feedback signal must be positive or regenerative.

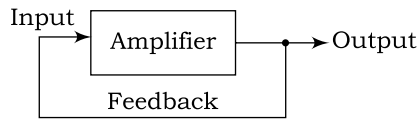


Fig. 5.1 Block diagram of basic oscillator

As practical oscillator generates signals at a predetermined frequency, a Frequency-Determining Network (FDN) is required. The FDN acts as a filter, which allows only the desired frequency to pass. The basic oscillator requirements, in addition to the application, determine the type of oscillator to be used. For any oscillator circuit, the following requirements must be fulfilled:

(i) Amplification is required to give necessary gain for the output signal.

(ii) There should be sufficient regenerative feedback to sustain oscillations.

(iii) A frequency-determining network (FDN) is required to maintain the desired output frequency.

(iv) Any oscillator has two types of stability such as amplitude stability and frequency stability. The *amplitude stability* refers to the ability of the oscillator to maintain constant amplitude of the output signal. Similarly, *frequency stability* refers to the ability of the oscillator to maintain constant frequency.

(v) Due to change in temperature and humidity, the value of capacitors, resistors and transistors can change. The changes in these components cause changes in amplitude and frequency. However, minimum change in amplitude and frequency has to be maintained.

(vi) For proper use of oscillators, output power is also another consideration. Sometimes high power is obtained with some compromise in stability. Generally, stable oscillators will be followed by a higher power buffer amplifier. The buffer is used to provide isolation between the oscillator and load so that changes in the load do not affect the oscillators.

(vii) Usually, oscillators use Class C amplifier to increase efficiency. Some oscillators use Class A amplifiers where high efficiency is not required but distortion must be minimum.

5.4 OSCILLATOR OPERATION

Figure 5.2 shows the negative feedback circuit. Assume the input voltage and output voltage are vector quantity and gains are also complex number. In this circuit,

$\overline{V_o}$ = Output voltage

$\overline{V_s}$ = Supply voltage

$\overline{A}$ = Gain of main amplifier

$\overline{\beta}$ = Feedback gain

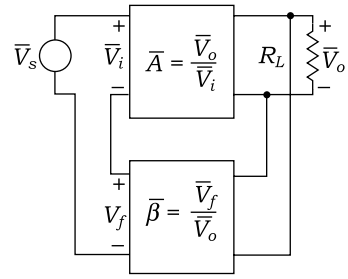


Fig. 5.2 Block diagram of negative feedback amplifier

The overall gain of an amplifier circuit is

$$\overline{A_f} = \frac{\overline{V_o}}{\overline{V_s}} = \frac{\overline{A}}{1 + \overline{\beta}\overline{A}} \tag{5.1}$$

At a particular frequency, the phase shift of $\overline{\beta}\overline{A}$ is 180° and polarity of the feedback voltage $\overline{V_f}$ is reversed. Therefore, the feedback is positive and overall gain becomes

$$\overline{A_f} = \frac{\overline{V_o}}{\overline{V_s}} = \frac{\overline{A}}{1 - \overline{\beta}\overline{A}} \tag{5.2}$$

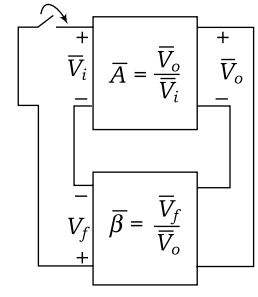


Fig. 5.3 Feedback circuit used as oscillator

When $|\overline{\beta}\overline{A}| < 2$, the gain of the amplifier must be larger than $|\overline{A}|$. If $|\overline{\beta}\overline{A}| = 1$ and $\angle\overline{\beta}\overline{A} = 180°$, the overall gain becomes infinite. It means that the input $\overline{V_s}$ is to be zero to produce any output voltage $\overline{V_o}$. Therefore, when the signal $\overline{V_s}$ is removed from Fig. 5.2, the circuit as shown in Fig. 5.3 oscillates at a particular frequency determined by frequency- determining network (FDN). Consequently, the condition for oscillation is $|\overline{\beta}\overline{A}| = 1$ and $\angle\overline{\beta}\overline{A} = 180°$ or $\overline{\beta}\overline{A} = -1$. This condition is called the *Barkhausen criteria for oscillation*.

To satisfy the Barkhausen criteria, the magnitude of the loop gain is unity with a corresponding phase shift of 180°. An equivalent expression using complex algebra is $\overline{\beta}\overline{A} = 1\angle -180°$ for a negative feedback system. In reality, there is no requirement of input signal to start oscillator. However, the condition $|\overline{\beta}\overline{A}| = 1$ will be satisfied only for self-sustained oscillators. Practically, $|\overline{\beta}\overline{A}|$ is made greater than 1 and the feedback circuit starts oscillating by amplifying noise voltage which is always present in the system. The saturation factors of the feedback circuit provide an average $|\overline{\beta}\overline{A}|$, which is about 1. Hence, the output waveforms of oscillators are not exactly sinusoidal; and it will be nonsinusoidal in nature.

As the phase shift approaches 180° and $|\overline{\beta}\overline{A}| = 1$ in a negative feedback circuit, the output voltage of the system tends to infinity, but it is limited to finite value due to an energy limited power supply. When the

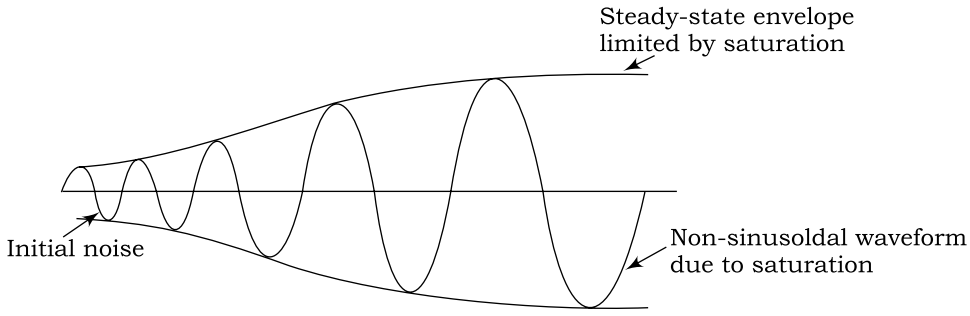


Fig. 5.4 The build up of oscillations

output voltage approaches power rail $+V_{CC}$ or $-V_{CC}$, the gains of active devices in the amplifiers are changed. The value of A changes and forces βA away from the singularity. Figure 5.4 shows the build up of oscillations starting from initial noise. Ideally, the trajectory of output voltage will be toward an infinite voltage, but practically, the following things can occur:

(i) Nonlinearity in saturation causes the system to become stable.

(ii) The initial change causes the system to saturate and stay that way for a long time before it becomes linear. This produce highly distorted oscillations called as relaxation oscillators.

(iii) The feedback amplifier circuit stays linear and in reverse direction, heading for the opposite power rail. This condition provides a sine-wave oscillator.

Barkhausen Criterion

In a positive feedback amplifier, the overall voltage gain of positive feedback amplifier is given by

$$A_f = \frac{A}{1 - \beta A}$$

where A is the gain of an amplifier without feedback or open-loop gain

βA is the product of feedback amplifier and open loop gain.

When βA is equal to one, the denominator becomes zero and the A_f will increase to infinity. But practically, the output of feedback amplifier cannot be infinite. Consequently, $1 - \beta A = 0$ represents that the frequency of output voltage is completely different from input voltage. Therefore, the positive feedback amplifier circuit stop functioning as an amplifier but it starts to oscillate. So that the condition of oscillation is that $\beta A = 1$.

An amplifier circuit reverses the phase of input voltage at its output. Hence, there is 180° phase shift between input voltage and output voltage. In positive feedback circuit, the feedback networks provide a phase shift of 180° and generate a signal with 0° or multiple of 360° at the amplifier input.

When the positive feedback circuit has the following conditions:

(i) $\beta A = 1$ and

(ii) the total phase shift around the loop is 0° or multiple of 360°,

it behaves as an oscillator. The above conditions for oscillation are called *Barkhausen Criterion for oscillation*. As βA is a complex quantity, mathematically the Barkhausen Criterion is represented by

$$\beta A = 1 + j0$$

or, $\beta A = 1$ and $\angle \beta A = 0°$ or multiple of 360°

In an oscillator, the value of βA must be exactly unity but it is not practicable for implementation. Therefore, for all practical oscillator, value of βA is slightly greater than unity.

Generally, amplifier gain A and feedback path gain β are complex quantity and function of frequency. Consequently, βA is also a complex quantity and function of frequency. When $|1 - \beta A| < 1$ in a positive feedback amplifier, the amplifier acts as an oscillator. Any feedback amplifier will be stable, when transient disturbance produces a response, but the amplitude of response must decay with time. The feedback system becomes unstable if any transient disturbance persists indefinitely and output response increases with time, but amplitude of output response is limited by nonlinearity of the circuit parameters. The stability of the amplifier can be investigated using the Nyquist criterion.

The gain and phase shift of a feedback amplifier are plotted on a complex plane. As βA is also a complex quantity and function of frequency, different points on the complex plane is obtained corresponding to different values of frequency. When frequency is varied from $+\infty$ to $-\infty$, a closed curve is formed by the locus of $(1 - \beta A)$. This plot is known as *Nyquist plot*.

The locus of $|1 - \beta A|$ is a circle of unit radius with the centre at point $(1 + j0)$. The locus of βA on the complex plane is $A_1 - A_2$, while frequency is varied. At a specified frequency f_o, the point on the locus $A_1 - A_2$ is P. If P is inside the circle of unit radius with its center at point $(1 + j0)$, then $|1 - \beta A| < 1$ and feedback is positive as shown in Fig. 5.6. If P is outside the circle then $|1 - \beta A| > 1$ and feedback is negative as depicted in Fig. 5.5. When P is located at the point $(1 + j0)$, the overall gain A_f is infinite and amplifier works as an oscillator. Consequently, the *Nyquist criterion* states that when the locus of βA passes through or encloses the circle of unit radius with the centre at the point $(1 + j0)$, the amplifier is unstable and will oscillate. When the locus of βA does not pass through or does not enclose the circle of unit radius with the centre at the point $(1 + j0)$, the amplifier is stable. Therefore, positive feedback amplifier acts as an oscillator only when the Nyquist criterion is satisfied.

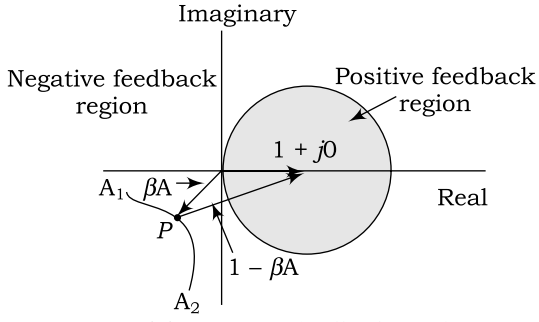


Fig. 5.5 Negative feedback amplifier

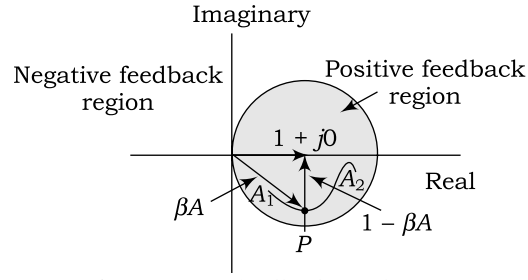


Fig. 5.6 Positive feedback amplifier

5.5 PHASE SHIFT IN OSCILLATION

The phase shift of $\beta A = 1\angle -180°$ is introduced by active and passive components. In any well-designed feedback circuit, oscillators are made dependent on only passive component phase shift, as it is most accurate. The phase shift contributed by active components is minimised as it changes with temperature and is device dependent. So the amplifiers are selected in such a way that they contribute very little or no-phase shift at the oscillator.

A single-pole *RC* circuit contributes up to 90° phase shift per pole. To get 180° phase shift in any oscillator, at least two poles must be used in oscillator design. Figure 5.7 shows that two cascaded *RC* circuits provide 180° phase shift. The value of $\frac{d\phi}{d\omega}$ at the oscillator frequency is unacceptably small. Therefore, oscillators made with two cascaded *RC* circuits, have poor frequency stability.

When three equal *RC* circuits are cascaded, the circuit has much higher $\frac{d\phi}{d\omega}$. As a result, the oscillator has improved frequency stability. The three section oscillators yield three sine waves of 60° phase shift relative to each other. If another *RC* circuit is added, i.e., four equally cascaded *RC* circuits, they produce an oscillator with an excellent $\frac{d\phi}{d\omega}$. Hence, this circuit is the most stable oscillator and yields four sine waves of 45° phase shift relative to each other.

An *LC* circuit has two poles and it can contribute up to 180° phase shift per pole pair. However, *LC* oscillators are not very useful at low-frequency operation as low-frequency inductors are very expensive, heavy, and bulky. Usually, *LC* oscillators are designed in high-frequency application, beyond the frequency range of voltage feedback OP-AMPs. Multiple *RC* circuits are used in low frequency oscillators.

5.6 PHASE SHIFT OSCILLATOR

Figure 5.8 shows a phase-shift oscillator circuit. The phase shift in feedback path of an amplifier can be provided by an *RC* network. The *RC* sections are cascaded to get the steep slope $\frac{d\phi}{d\omega}$ required for a stable oscillator frequency. The phase shifts of *RC* sections are independent of each other and βA will be equal to

$$\beta A = A\left(\frac{1}{1+sRC}\right)^3$$

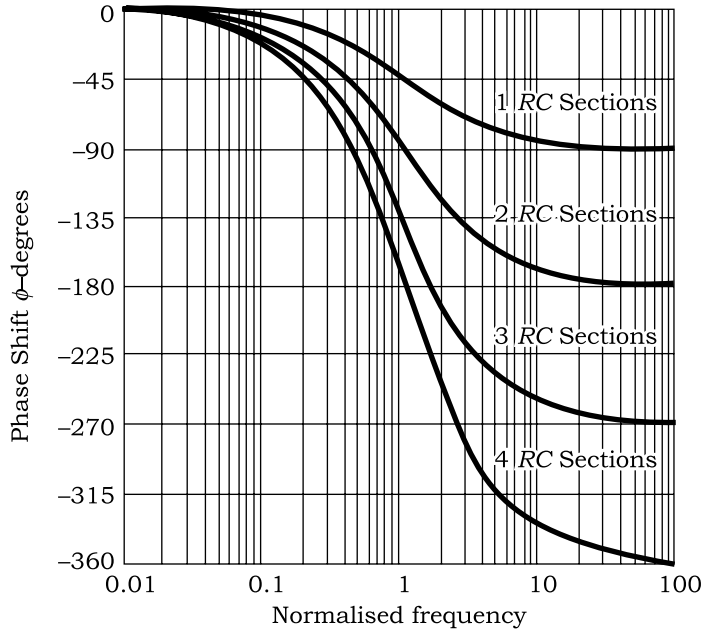


Fig. 5.7 Phase plot of RC sections

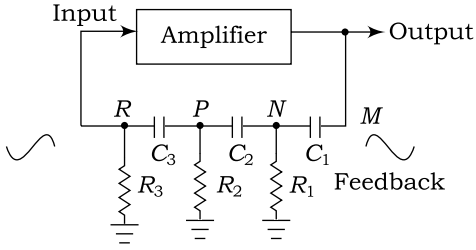


Fig. 5.8 Amplifier with an RC feedback network

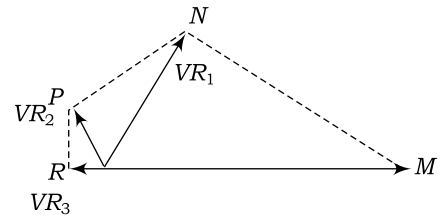


Fig. 5.9 Vector diagram of RC feedback network

Figure 5.9 shows the vector diagram of an *RC* feedback network. The signal at *M* is 180 degrees out of phase with the signal input at *R*. To produce regenerative feedback, the *RC* network must provide a 180° phase shift of the signal. When power is applied to the circuit, a noise voltage will appear at *M*. This noise signal couples through C_1 and a phase shift occurs across R_1. The voltage across R_1 is VR_1, which has been shifted in phase about 60° and reduced in amplitude. The signal at the point *N* is coupled to the next *RC* section (R_2 and C_2). As resistance and capacitor size are same as before, there will be another 60° phase shift. The signal at the point *P* is the voltage across R_2 represented by VR_2, which has been shifted about 120° and its magnitude is reduced further. The same type of operation takes place in the last *RC* section (R_3 and C_3). There will be another 60° phase shift and further amplitude reduction. Hence, the signal at the point *R*, VR_3 has been shifted 180°. The loop phase shift is –180° when phase shift of each section is –60°. The 60° phase shift occurs when $\omega = 2\pi f = \dfrac{1.732}{RC}$ as tan 60° = 1.732.

Assume the current *I* flows through *C* and *R*. The voltage across the capacitor *C* is V_C, which will be 90° lagging from the current *I*. The voltages across the resistance *R* is *VR*, which will be in phase with the current *I*. As a result, voltage *V* has a phase shift of θ angle with respect to current.

Figure 5.10(b) shows the vector diagram of an *RC* section.

From Fig. 5.10(b), we can write

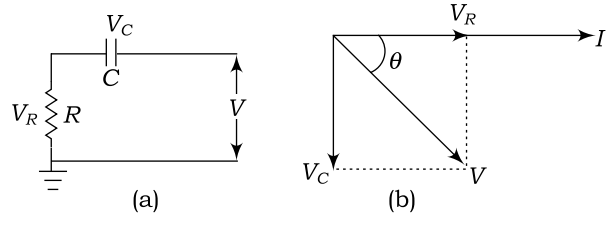


Fig. 5.10 (a) *RC* section (b) Its vector diagram

$$\tan\theta = \frac{V_C}{V_R} = \frac{IX_C}{IR} = \frac{1}{2\pi fRC}$$

The frequency is equal to

$$f = \frac{1}{2\pi RC\tan\theta}$$

As $\theta = 60°$, $\tan\theta = \tan 60° = \sqrt{3}$

Then $$f = \frac{1}{2\pi RC\sqrt{3}}$$

The transfer function of the three *RC* networks is

$$\beta = \frac{V_f}{V_o} = \frac{1}{1 + \frac{6}{sRC} + \frac{5}{s^2R^2C^2} + \frac{1}{s^3R^3C^3}} \tag{5.3}$$

After substituting $s = j\omega = j2\pi f$ and $f_1 = \frac{1}{2\pi RC}$, we get

$$\beta = \frac{1}{1 - 5\left(\frac{f_1}{f}\right)^2 - j\left[6\left(\frac{f_1}{f}\right) - \left(\frac{f_1}{f}\right)^3\right]} \tag{5.4}$$

As $|\beta A| = 1$, β must be real. The imaginary term in the above equation must be zero.

$$6\left(\frac{f_1}{f}\right) - \left(\frac{f_1}{f}\right)^3 = 0$$

or $$\frac{f_1}{f} = \sqrt{6}$$

The frequency of the oscillator is

$$f = \frac{1}{2\pi RC\sqrt{6}} \tag{5.5}$$

and the corresponding feedback gain is $\beta = \frac{1}{29}$

The above relation is only justified when each section of the *RC* network does not affect other sections. However, practically, it is not possible due to device parameter variations.

As $|\beta A| = 1$, $|A| = \frac{1}{\beta} = 29$ (5.6)

So the circuit will oscillate if $A = 29$.

Example 5.1 In an *RC* phase shift oscillator, if the value of resistors are $R_1 = R_2 = R_3 = 100$ kΩ and the value of capacitors are $C_1 = C_2 = C_3 = 0.20$ nF. Determine the frequency of the oscillation.

Sol. Given $R_1 = R_2 = R_3 = 100$ kΩ and $C_1 = C_2 = C_3 = 0.20$ nF

The frequency of *RC* phase-shift oscillator is

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$= \frac{1}{2\pi \times 100 \times 10^3 \times 0.20 \times 10^{-9}\sqrt{6}}$$

$$= 3.247 \text{ kHz}$$

5.7 BJT PHASE-SHIFT OSCILLATOR

Figure 5.11 shows the BJT phase-shift oscillator. The quiescent operating point of the transistor is determined by the resistances R_1, R_2, R_C, and R_E and supply voltage V_{CC}. The bypass capacitor C_E is connected in parallel with R_E and provides very small reactance at low-frequency signal. In this circuit, the transistor operates in common emitter configuration and it provides a 180° phase shift between input and output voltages. There are three *RC* sections in the circuit and these provide another 180° phase shift. Hence, the net phase shift around the loop is 0° or 360°. In this section, the detail circuit analysis is explained.

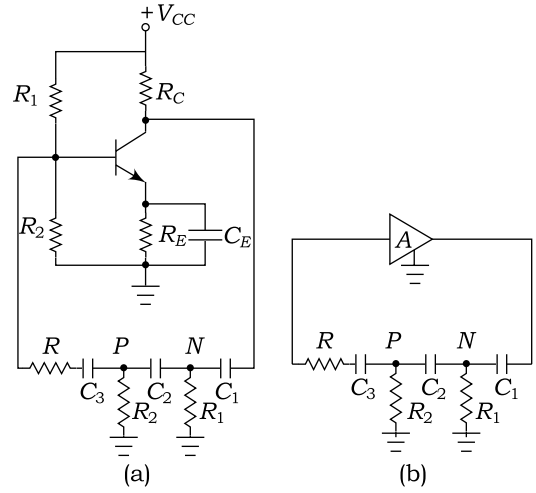


Fig. 5.11 ***RC*** **phase-shift oscillator using BJT**

5.7.1 Circuit Analysis of BJT Phase Shift Oscillator

Assume each *RC* section is identical. For this, $C_1 = C_2 = C_3 = C$, $R_1 = R_2 = R$. As input impedance of the transistor h_{ie} is connected in series with R', the effective resistance of last section is $R' = R - h_{ie}$. As R_1 and R_2 are very high, the effect on ac operation of the circuit is negligible. The parallel combination of R_E and C_E will be absent in the ac equivalent circuit of BJT oscillator. The equivalent circuit of Fig. 5.11 is shown in Fig. 5.12. As h_{re} is very small, the value of $h_{re}V_2$ may be neglected. As $\frac{1}{h_{oe}} >> R_C$, we can also neglect $\frac{1}{h_{oe}}$. Then the equivalent circuit is modified as represented by Fig. 5.13. This circuit can be represented in the most simplified form as shown in Fig. 5.14. There are three loops and loop currents are I_1, I_2 and I_3.

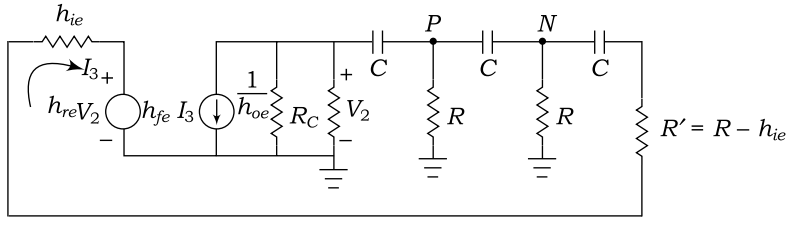


Fig. 5.12 **The ac equivalent circuit of Fig. 5.11**

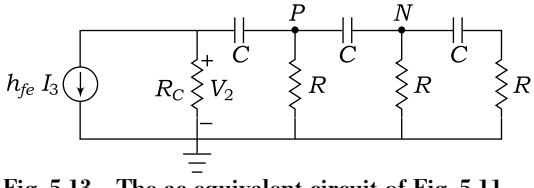


Fig. 5.13 **The ac equivalent circuit of Fig. 5.11 when $h_{re}V_2$ and $\frac{1}{h_{oe}}$ are neglected**

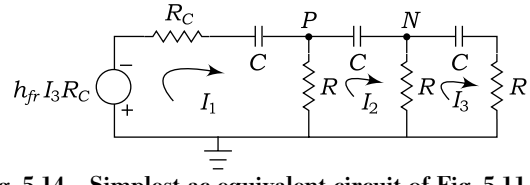


Fig. 5.14 **Simplest ac equivalent circuit of Fig. 5.11**

KVL equation of Loop I is

$$\left(R_C + R - j\frac{1}{\omega C}\right)I_1 - RI_2 + h_{fe}R_C I_3 = 0$$

KVL equation of Loop II is

$$-RI_1 + \left(2R - j\frac{1}{\omega C}\right)I_2 - RI_3 = 0$$

KVL equation of Loop III is

$$-RI_2 + \left(2R - j\frac{1}{\omega C}\right)I_3 = 0$$

We can write the KVL equations in matrix form as given below:

$$\begin{bmatrix} R_C + R - j\frac{1}{\omega C} & -R & h_{fe}R_C \\ -R & 2R - j\frac{1}{\omega C} & -R \\ 0 & -R & 2R - j\frac{1}{\omega C} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = 0 \tag{5.7}$$

As I_1, I_2, I_3 are nonzero quantities, the determinant of the coefficient of I_1, I_2 and I_3 must be zero.

Therefore, we can write the determinant of the matrix

$$\left(R_C + R - j\frac{1}{\omega C}\right)\left(3R^2 - j\frac{4R}{\omega C} - \frac{1}{\omega^2 C^2}\right) - R^2\left(2R - j\frac{1}{\omega C}\right) + h_{fe}R_C R^2 = 0 \tag{5.8}$$

The above equation has real and imaginary parts. For oscillation, imaginary part as well as real part will be zero.

The imaginary part is equal to

$$-4R\frac{R + R_C}{\omega C} - \frac{1}{\omega C}\left(3R^2 - \frac{1}{\omega^2 C^2}\right) + \frac{R^2}{\omega C} = 0 \tag{5.9}$$

Then we can find that

$$\omega^2 = \frac{1}{C^2(6R^2 + 4RR_C)}$$

or

$$\omega = \frac{1}{RC\sqrt{6 + 4\frac{R_C}{R}}} \tag{5.10}$$

Therefore, the circuit analysis of the small-signal model yielding the frequency of oscillation is

$$f = \frac{\omega}{2\pi} = \frac{1}{2\pi RC\sqrt{6 + 4\frac{R_C}{R}}} \tag{5.11}$$

If we assume $\frac{R_C}{R} = K$, the frequency of oscillation is

$$f = \frac{1}{2\pi RC\sqrt{6+4K}} \tag{5.12}$$

The real part of Eq. (5.8) is equal to

$$(R + R_C)\left(3R^2 - \frac{1}{\omega^2 C^2}\right) - 2R^3 - \frac{4R}{\omega^2 C^2} + h_{fe} R_C R^2 = 0 \tag{5.13}$$

After substituting the value of ω^2 in the above equation, we obtain

$$h_{fe} = 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R} \tag{5.14}$$

When the loop gain is greater than unity, the current gain of BJT must be equal to h_{fe} which follows the condition

$$h_{fe} \geq 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R} \tag{5.15}$$

The 'greater than' sign (>) in the above equation compensates for parameter changes in the amplifier. The optimum value of k is about 5.7. For this, the minimum value of h_{fe} is required for transistor to work as a *RC* oscillator. h_{fe} must be greater than 44.5 for oscillation.

RC phase-shift oscillators are widely used as signal sources in the audio-frequency and the ultrasonic range. If any one of the three capacitors or three resistors is changed in value, the phase shift provided by the section of the network becomes different and oscillator frequency will be changed. Due to change in single capacitor or resistor, the amplitude of the output signal also changes in some extent. While a large range of frequency is required, all capacitors must be varied simultaneously. Generally, the range of capacitance is 50 pF to 500 pF and the frequency of oscillation can be changed in the ratio 10:1. For higher range of frequency variation, the resistance value of different resistors will be changed by a factor of 10.

5.8 FET PHASE-SHIFT OSCILLATOR

Figure 5.15 shows the circuit diagram of a FET phase shift oscillator. The load resistance is $R_L = R_D \| r_d$ and the amplifier gain is $A = -g_m R_L$. As amplifier gain is negative, the feedback must be negative.

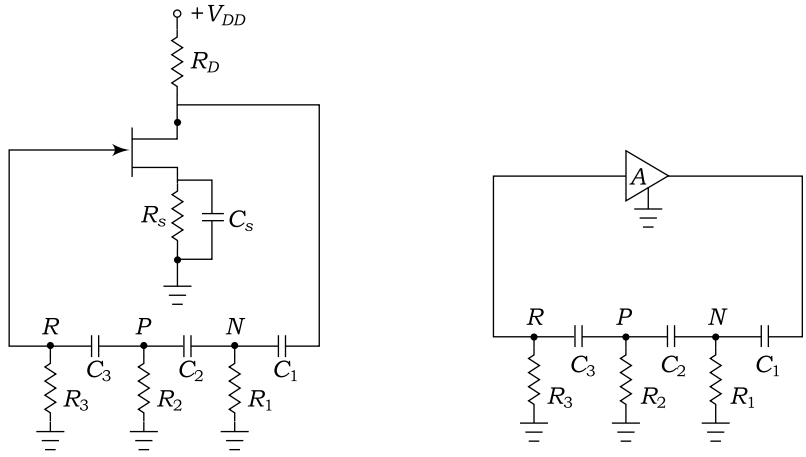


Fig. 5.15 ***RC*** **phase-shift oscillator using FET**

The frequency of the oscillator is $f = \frac{1}{2\pi RC\sqrt{6}}$ and magnitude of phase shift network gain $\beta = \frac{1}{29}$. The phase shift of 180° causes this feedback to behave as positive. At very high frequency, the input capacitance of FET contributes loading effect and FET should have high gain at low frequency for oscillation.

Example 5.2 Find the frequency of oscillation in an *RC* phase shift oscillator as shown in Fig. 5.11. Assume R = 20 kΩ, C = 0.047 μF, R_C = 4.7 kΩ. Determine the minimum value of current gain for the oscillation.

Sol. Given R = 20 kΩ, C = 0.047 μF and R_C = 4.7 kΩ

The frequency of *RC* phase-shift oscillator is

$$f = \frac{1}{2\pi RC\sqrt{6+4K}} \quad \text{where } \frac{R_C}{R} = K,$$

$$K = \frac{R_C}{R} = \frac{4.7}{20} = 0.235$$

The frequency of the oscillation is

$$= \frac{1}{2\pi \times 20 \times 10^3 \times 0.047 \times 10^{-6}\sqrt{6+4\times 0.235}}$$

$$= 64.26 \text{ Hz}$$

The minimum value of current gain for the oscillation is

$$h_{fe} = 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

$$= 23 + 29 \times \frac{20}{4.7} + 4 \times \frac{4.7}{20} = 147.34$$

Example 5.3 Determine the value of capacitors and current gain of the transistor when the frequency of oscillation in an *RC* phase-shift oscillator is 20 kHz. Assume $R_1 = R_2 = R_3 = R$ = 100 kΩ, R_C = 5.6 kΩ.

Sol. Given f = 20 kHz, $R_1 = R_2 = R_3 = R$ = 100 kΩ, and R_C = 5.6 kΩ

The frequency of *RC* phase-shift oscillator is

$$f = \frac{1}{2\pi RC\sqrt{6+4K}} \quad \text{where, } \frac{R_C}{R} = K,$$

$$K = \frac{R_C}{R} = \frac{5.6}{100} = 0.056$$

The frequency of the oscillation is

$$20 \times 10^3 = \frac{1}{2\pi \times 100 \times 10^3 \times C \times \sqrt{6+4\times 0.056}}$$

or

$$C = \frac{1}{2\pi \times 100 \times 10^3 \times 20 \times 10^3 \times \sqrt{6+4\times 0.056}}$$

$$= 0.03189 \text{ nF}$$

The minimum value of current gain for the oscillation is

$$h_{fe} = 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

$$= 23 + 29\frac{100}{5.6} + 4\frac{5.6}{100} = 541$$

5.9 WEIN-BRIDGE OSCILLATOR

Figure 5.16 shows a Wein-bridge oscillator using OP-AMP and *RC* bridge circuit. The output voltage of the operational amplifier (OP-AMP), V_o is used as the input voltage of the bridge. The output voltage of the bridge V_i can be used as the input voltage of the amplifier. When the bridge is in balanced condition, $V_i = 0$. However, to sustain oscillation, V_i will not be zero ($V_i \neq 0$). Therefore, the bridge is kept in slightly unbalanced condition by varying the ratio between the resistances R_3 and R_4. A Wein-bridge does not provide any phase shift between input and output voltages of a bridge circuit. As a result, the operational amplifier must not introduce any phase shift between input and output voltages of the amplifier and the overall phase shift around the loop is zero.

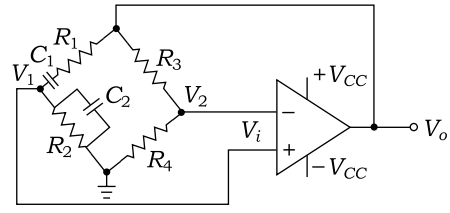


Fig. 5.16 Wien-bridge oscillator

Analysis of Wien-Bridge Oscillator

The oscillator frequency is determined by *R* and *C*. *R*esistors R_1 and R_2 and capacitors C_1 and C_2 are used as frequency adjustment elements of Wein-bridge oscillator. R_3 and R_4 are used as part of the feedback path of the amplifier circuit. The transfer function of the circuit has been derived using the following method as given below:

The impedances of four arms of the Wein-bridge are Z_1, Z_2, Z_3 and Z_4.

Impedance Z_1 is the series connection of R_1 and C_1 and it is equal to

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{sR_1C_1 + 1}{sC_1} = \frac{1 + j\omega R_1C_1}{j\omega C_1} \quad \text{as } s = j\omega \tag{5.16}$$

Impedance Z_2 is the parallel combination of R_2 and C_2 and $Z_2 = R_2 \| \frac{1}{sC_2}$.

Therefore,

$$\frac{1}{Z_2} = \frac{1}{R_2} + sC_2$$

$$= \frac{1 + sR_2C_2}{R_2}$$

Then

$$Z_2 = \frac{R_2}{1 + sR_2C_2} = \frac{R_2}{1 + j\omega R_2C_2} \quad \text{as } s = j\omega \tag{5.17}$$

The other two impedances are

$$Z_3 = R_3 \text{ and } Z_4 = R_4$$

The frequency of oscillation can be determined from the bridge-balance condition. For the bridge-balance condition, the phase angle of Z_1 and Z_2 will be same, and oscillation frequency f_o can be obtained at this condition.

The bridge will be balanced when $Z_1R_4 = Z_2R_3$ or $\frac{Z_1}{Z_2} = \frac{R_3}{R_4}$

Therefore, $$\frac{\frac{1 + j\omega R_1C_1}{j\omega C_1}}{\frac{R_2}{1 + j\omega R_2C_2}} = \frac{R_3}{R_4}$$

or $$\frac{(1 + j\omega R_1C_1)(1 + j\omega R_2C_2)}{j\omega R_2C_1} = \frac{R_3}{R_4} \tag{5.18}$$

When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the above equation can be written as

or $$\frac{(1 + j\omega RC)(1 + j\omega RC)}{j\omega RC} = \frac{R_3}{R_4}$$

or $$2 - j\frac{(1 - \omega^2R^2C^2)}{\omega RC} = \frac{R_3}{R_4} \tag{5.19}$$

The condition for oscillation is that the real and imaginary parts on both the sides must be equal.

Therefore, $\frac{R_3}{R_4} = 2$ and $1 - \omega^2R^2C^2 = 0$

Hence, we can also write the condition for oscillation as

$$\frac{Z_1}{Z_2} = \frac{R_3}{R_4} = 2$$

For oscillation, $Z_1 = 2Z_2$

or $$\frac{1 + j\omega R_1C_1}{j\omega C_1} = 2\frac{R_2}{1 + j\omega R_2C_2}$$

or $$(1 - \omega^2R_1C_1R_2C_2) = 0$$

Assume $R_1 = R_2 = R$ and $C_1 = C_2 = C$

Then $(1 - \omega^2R^2C^2) = 0$

or $$\omega = \frac{1}{RC}$$

or $$2\pi f = \frac{1}{RC}$$

The frequency of oscillation is $f = \frac{1}{2\pi RC}$

At the balanced condition of Wein-bridge, the voltage across the two arms of the bridge must be equal.

Therefore, $V_1 = V_2 = \frac{R_4}{R_3 + R_4}V_o$

As $\frac{R_3}{R_4} = 2, \frac{R_4}{R_3 + R_4} = \frac{1}{3}$ and $V_1 = V_2 = \frac{1}{3}V_o$

At balanced condition, we get

$$\frac{V_1}{V_o} = \frac{V_2}{V_o} = \frac{1}{3} \tag{5.20}$$

At oscillation, the input voltage of amplifier is not equal to zero ($V_i \neq 0$) and the ratio $\frac{R_4}{R_3 + R_4}$ will be less than $\frac{1}{3}$. Then we can write

$$\frac{R_4}{R_3 + R_4} = \frac{1}{3} - \frac{1}{\delta}$$

where, δ is real number which is greater than 3. The bridge is slightly unbalanced and provides a feedback voltage, V_i.

The ratio $\frac{V_1}{V_o}$ remains at $\frac{1}{3}$ and the ratio $\frac{V_2}{V_o}$ is

$$\frac{V_2}{V_o} = \frac{1}{3} - \frac{1}{\delta}$$

Then input voltage of feedback amplifier is

$$V_i = V_1 - V_2 = \frac{1}{3}V_o - \left(\frac{1}{3} - \frac{1}{\delta}\right)V_o = \frac{V_o}{\delta} \tag{5.21}$$

The feedback factor is $\beta = \frac{V_i}{V_o} = \frac{1}{\delta}$

The condition of oscillation is $\beta A = 1$. Then, $\frac{A}{\delta} = 1$. For oscillation, $A = \delta > 3$.

1. Advantages of Wein-Bridge Oscillator

The advantages of a Wein-bridge oscillator are as follows:

(a) As two stage amplifiers are used, the overall gain is very high.

(b) The output waveforms will be pure sine wave.

(c) The frequency stability is very good. Actually, oscillation frequency depends on R and C. Since the values of R and C are fixed against temperature variations, frequency stability can be achieved.

(d) The frequency of oscillation can be changed easily by varying R and C.

(e) When the resistance R_4 is replaced by a thermistor with negative temperature coefficient, the amplitude of oscillation will be stabilised with parameter variations of transistors aging effect of transistor, and other circuit parameters. Due to negative temperature coefficient, R_4 decreases with increasing temperature. Therefore, feedback factor β decreases. As a result, the Wein-bridge adjusts itself in such a way that $\beta A = 1$.

2. Disadvantages of a Wein-Bridge Oscillator

The disadvantages of a Wein-bridge oscillator are as follows:

(a) Large numbers of components are required for a two-stage amplifier.

(b) Wein bridge oscillators can generate only audio frequency (AF) range sine wave.

Example 5.4 In a Wein-bridge oscillator when the value of resistor $R = 200\ \text{k}\Omega$ and the frequency of the oscillation is 20 kHz, determine the value of capacitor C.

Sol. Given $R = 200\ \text{k}\Omega$ and $f = 20$ kHz

The frequency of the oscillation is

$$f = \frac{1}{2\pi RC}$$

The value of the capacitor C at the frequency of oscillation is

$$C = \frac{1}{2\pi Rf} = \frac{1}{2\pi \times 200 \times 10^3 \times 20 \times 10^3} = 0.0397\ \text{nF}$$

Example 5.5 In a Wein-bridge oscillator, the value of capacitors can be changed from 10 pF to 100 pF to generate sine-wave output signals from 20 Hz to 20 kHz.

(a) Determine the resistances required to generate the output signals from 20 Hz to 20 kHz.

(b) If the gain of the amplifier is 5, what will be the ratio of the resistances in the other arms of the bridge?

Sol. Given Capacitor range is 10 pF to 100 pF and frequency range is 20 Hz to 20 kHz.

(a) The frequency of the oscillation is

$$f = \frac{1}{2\pi RC}$$

When $f = 20$ Hz, $C = 100$ pF, the value of required resistance is

$$R = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 20 \times 100 \times 10^{-9}} = 79.54\ \text{k}\Omega$$

The capacitance varies in the ratio 10 pF : 100 pF = 1:10. Then the oscillator frequency range will be 20 Hz to 200 Hz with $R = 79.54\ \text{k}\Omega$.

Therefore, to generate output signal in the frequency range from 200 Hz to 2 kHz, the value of R will be $\frac{1}{10}$ th of $79.54\ \text{k}\Omega = 7.954\ \text{k}\Omega$.

In the same way, for the frequency range from 200 Hz to 2 kHz, the value of R will be $\frac{1}{10}$ th of $7.954\ \text{k}\Omega = 0.7954\ \text{k}\Omega$.

(b) Since the gain of amplifier $A = 5$, for oscillation $\delta = A = 5$

$$\frac{R_4}{R_3 + R_4} = \frac{1}{3} - \frac{1}{\delta} = \frac{1}{3} - \frac{1}{5} = \frac{2}{15}$$

or $$1 + \frac{R_3}{R_4} = 7.5$$

Therefore, the ratio of the resistances in the other arms of the bridge is

$$\frac{R_3}{R_4} = 6.5$$

5.10 TUNED COLLECTOR-OSCILLATOR

Figure 5.17 shows a tuned collector-oscillator circuit. The quiescent operating point can be determined by the supply voltage V_{CC} and the resistances R_1, R_2, R_E and R_B. The resistance R_B is in parallel with R_2. As R_B is very large, the effect on the quiescent operating point is very small. In this circuit, R_B is used to

1. Control the amount of feedback to the value which is just required to sustain oscillations
2. Reduce the loading effect of the collector by the transistor for low input impedance
3. Decrease distortion

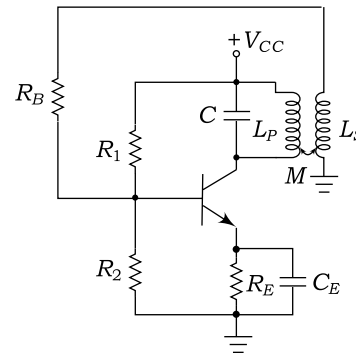


Fig. 5.17 A tuned collector-oscillator

The emitter-bypass capacitor C_E is connected in parallel with resistance R_E and it will not appear in the ac equivalent circuit. Here transistor operates in common-emitter configurations. The common-emitter amplifier provides 180° phase shift between input and output voltages. The additional 180° phase shift is required to sustain oscillation. Actually, phase shift of a tank circuit provides 180° phase shift.

The frequency-determining network (FDN) can be made up by the capacitor and transformer primary inductance L_P. As an *LC* tuned circuit is connected with the collector of transistor, this circuit is called as tuned collector-oscillator. This *LC* tuned circuit is also known as *tank circuit* as this circuit is used as frequency-determining network.

5.10.1 Analysis of Tuned Collector-Oscillator

Figure 5.18 shows the *h*-parameter ac equivalent circuit of Fig. 5.17. *R* is the resistance of the transformer primary winding and its value is very small and so the tank circuit's quality factor *Q* is very high.

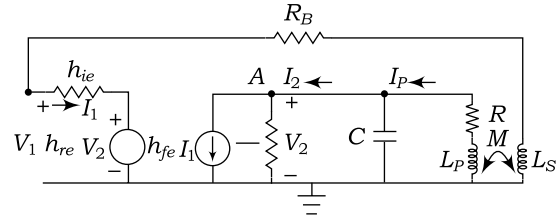


Fig. 5.18 The ac equivalent circuit of tuned collector-oscillator

The effective resistance offered by this circuit is

$$R_{eff} = \frac{L_P}{CR}$$

The current flowing through the secondary of the transformer I_1 is very small so that it induces a negligible voltage in the transformer primary. Due to large value of R_B, the *LC* tuned circuit is not considerably loaded. The frequency of oscillation is

$$f = \frac{\omega}{2\pi} = \frac{1}{2\pi\sqrt{L_P C}} \quad \text{as } \omega^2 = \frac{1}{L_P C}$$

Hence, the frequency of oscillation can be varied by changing either L_P or C or both. Usually, tuned collector oscillators generate oscillation signals in the radio frequency (RF) range.

The voltage V_2 is

$$V_2 = -I_2 R_{eff} = -I_2 \frac{L_P}{CR}$$

Applying KCL at the point *A*, we get

$$I_2 = h_{fe} I_1 + h_{oe} V_2$$

After substituting the value of V_2 in the above equation, we obtain

$$I_2 = h_{fe} I_1 + h_{oe}\left(-I_2 \frac{L_P}{CR}\right)$$

or
$$\left(1 + h_{oe}\frac{L_P}{CR}\right) I_2 = h_{fe} I_1 \tag{5.22}$$

The induced voltage across the transformer secondary winding is $j\omega M I_P$
where, M is the mutual inductance between primary and secondary, and I_P is the primary current.
The transformer primary current is equal to

$$I_P = \frac{\frac{1}{j\omega C}}{R + j\omega L_P + \frac{1}{j\omega C}} I_2 = \frac{1}{j\omega CR - \omega^2 L_P C + 1} I_2$$

$$= \frac{1}{j\omega CR} I_2 \quad \text{as } \omega^2 = \frac{1}{L_P C}$$

$$= -j\omega \frac{L_P}{R} I_2 \quad \text{as } C = \frac{1}{\omega^2 L_P} \tag{5.23}$$

As $R_B >> |\omega L_S|$, the effective impedance in the secondary circuit is $R_B + h_{ie}$
Applying KVL in the secondary circuit, we get

$$I_1 h_{ie} + h_{re} V_2 = j\omega M I_P - I_1 R_B$$

or
$$(R_B + h_{ie}) I_1 = j\omega M I_P - h_{re} V_2$$

or
$$I_1 = \frac{j\omega M I_P - h_{re} V_2}{R_B + h_{ie}} \tag{5.23a}$$

After substituting the values of I_P and V_2 in the equation (5.23a), we get

$$I_1 = \left(\frac{\omega^2 M L_P}{R} + h_{re}\frac{L_P}{CR}\right) I_2 / (R_B + h_{ie}) \tag{5.24}$$

*A*fter substituting the value of I_1 in Eq. (5.22), we obtain

$$\left(1 + h_{oe}\frac{L_P}{CR}\right) = \frac{h_{fe}}{R_B + h_{ie}}\left(\omega^2 M + h_{re}\frac{1}{C}\right)\frac{L_P}{R} \tag{5.25}$$

As $\omega^2 = \frac{1}{L_P C}$, we can find the mutual inductance is

$$M = \frac{R_B}{h_{fe}}(CR + h_{oe} L_P) + CR\frac{h_{ie}}{h_{fe}} + L_P \frac{\Delta_{he}}{h_{fe}} \tag{5.26}$$

where, $\Delta_{he} = (h_{ie} h_{oe} - h_{fe} h_{re})$

Example 5.6 A tuned collector-oscillator is used in a radio receiver and it has inductance $L_P = 0.5$ mH and its tuning frequency range from 400 Hz to 1600 kHz. Determine the range of capacitors.

Sol. Given $L_P = 0.5$ mH and frequency range is 400 Hz to 1600 kHz.

The frequency of oscillation of a tuned collector oscillator is

$$f = \frac{1}{2\pi\sqrt{L_P C}}$$

Therefore, $$C = \frac{1}{4\pi^2 f^2 L_P}$$

When $f = 400$ Hz, $C = \dfrac{1}{4\pi^2 \times 400^2 \times 0.5 \times 10^{-3}} = 316.66\ \mu\text{F}$

When $f = 1600$ kHz, $C = \dfrac{1}{4\pi^2 \times (1600 \times 1000)^2 \times 0.5 \times 10^{-3}} = 0.0198$ nF

Example 5.7 A tank circuit has an inductance $L_P = 0.25$ mH. Calculate the range of capacitors when the tuning frequency range is 400 kHz to 1200 kHz.

Sol. Given $L_P = 0.25$ mH and the tuning frequency range is 400 kHz to 1200 kHz

At any resonance frequency, the value of the capacitor is $C = \dfrac{1}{4\pi^2 f^2 L_P}$

If $f = 400$ kHz, $C = \dfrac{1}{4\pi^2 \times (400 \times 1000)^2 \times 0.5 \times 10^{-3}} = 0.31695$ nF

When $f = 1200$ kHz, $C = \dfrac{1}{4\pi^2 \times (1200 \times 1000)^2 \times 0.5 \times 10^{-3}} = 35.216$ pF

5.11 TUNED *LC* OSCILLATORS

The basic block diagram of a tuned oscillator is shown in Fig. 5.19. Any one of the active devices such as transistor, FET and operational amplifiers can be used in amplifier. The open-loop gain of the amplifier is A. Z_1, Z_2 and Z_3 are impedances, which provide the feedback tank circuit and are used to determine the frequency of oscillation. In this circuit, Z_1 and Z_2 act as a voltage-divider circuit between the output voltage and feedback signal. The feedback voltage is the voltage across Z_1.

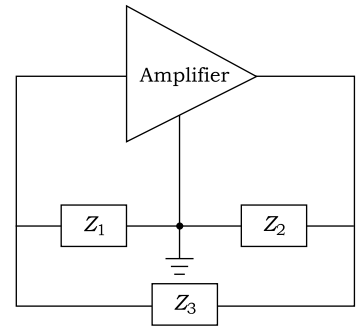


Fig. 5.19 Block diagram of tuned oscillator

The gain with load but without feedback is

$$\overline{A_L} = \frac{\overline{Z_L} A}{\overline{Z_L} + R_o} \tag{5.27}$$

where, R_o is the output resistance of the amplifier, and

$\overline{Z_L}$ is the load impedance.

The load impedance is

$$\overline{Z_L} = \overline{Z_2} \,||\, (\overline{Z_1} + \overline{Z_3}) = \frac{Z_2(Z_1 + Z_3)}{(Z_1 + Z_2 + Z_2)} \tag{5.28}$$

The feedback factor is

$$\overline{\beta} = \frac{\overline{Z_1}}{\overline{Z_1} + \overline{Z_3}} \tag{5.29}$$

The loop gain will be

$$-\overline{\beta}\,\overline{A_L} = -\frac{\overline{Z_1}}{\overline{Z_1} + \overline{Z_3}} \cdot \frac{\overline{Z_L} A}{\overline{Z_L} + R_o} = -\frac{A\overline{Z_1}\,\overline{Z_2}}{R_o(\overline{Z_1} + \overline{Z_2} + \overline{Z_3}) + \overline{Z_2}(\overline{Z_1} + \overline{Z_3})} \tag{5.30}$$

The condition of the oscillator is $|\overline{\beta}\overline{A}| = 1$

Assume $\overline{Z_1} = jX_1$, $\overline{Z_2} = jX_2$ and $\overline{Z_3} = jX_3$

Therefore, $$-\overline{\beta}\,\overline{A_L} = \frac{AX_1X_2}{jR_o(X_1 + X_2 + X_3) - X_2(X_1 + X_3)}$$

For oscillation, the loop gain must be real. As a result, $X_1 + X_2 + X_3 = 0$

Then, $$-\overline{\beta}\,\overline{A_L} = -\frac{AX_1X_2}{X_2(X_1 + X_3)}$$

or $$-\overline{\beta}\,\overline{A_L} = -\frac{AX_1}{(X_1 + X_3)}$$

or $$-\overline{\beta}\,\overline{A_L} = \frac{AX_1}{X_2} \quad \text{as } X_1 + X_3 = -X_2 \tag{5.31}$$

Both X_1 and X_2 must be either inductive or capacitive. The choice of X_1, X_2 and X_3 gives the three different oscillators such as Colpitts, Hartley, and tuned-input–tuned-output oscillators. Table 5.2 shows the reactive elements of different types of oscillators.

Table 5.2 Reactive elements of oscillators

Oscillator type	*Reactive Elements*		
	X_1	X_2	X_3
Colpitts oscillator	C	C	L
Hartley oscillator	L	L	C
Tuned input, and Tuned output	LC	LC	

5.11.1 Transistor Colpitts Oscillators

Figure 5.20 shows the transistor Colpitts oscillator. The quiescent operating point of the transistor can be determined by the supply voltage V_{CC} and the resistances R_1, R_2, R_C and R_E. The capacitor C_B is used to block the dc current flow from the collector to the base of the transistor and the inductance L. The reactance of capacitor C_B is negligible at the frequency of oscillation. The emitter bypass capacitor C_E is connected in parallel with resistance R_E and it will not appear in the ac equivalent circuit. In this circuit, the transistor operates in common-emitter configurations and introduces 180° phase shift between input and output voltages. The voltage across C_1 is a fraction of the output voltage. As the feedback voltage is equal to the voltage

across C_1 and it is 180° out of phase with respect to output voltage, the net phase shift around the loop is 0° or 360°. The frequency-determining network (FDN) is formed by the inductance L and capacitors C_1 and C_2.

In this circuit, X_1, X_2 and X_3 are reactance of capacitors C_1 and C_2, and inductance L respectively. The reactance values are $X_1 = -\frac{1}{\omega C_1}$, $X_2 = -\frac{1}{\omega C_2}$, $X_3 = \omega L$

The condition for oscillation is

$$(X_1 + X_2 + X_3) = 0$$

Assume at resonance frequency ω_o, we can write

$$\frac{1}{\omega_o C_1} + \frac{1}{\omega_o C_2} = \omega_o L$$

or $$\frac{\omega_o (C_1 + C_2)}{\omega_0^2 C_1 C_2} = \omega_o L$$

or $$\frac{1}{\omega_o C_{eq}} = \omega_o L \quad \text{where, } C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

or $$\omega_o^2 = \frac{1}{LC_{eq}}$$

or $$\omega_o = \frac{1}{\sqrt{LC_{eq}}}$$

or $$2\pi f_o = \frac{1}{\sqrt{LC_{eq}}}$$

The frequency of oscillation is

$$f_o = \frac{1}{2\pi\sqrt{LC_{eq}}} \tag{5.32}$$

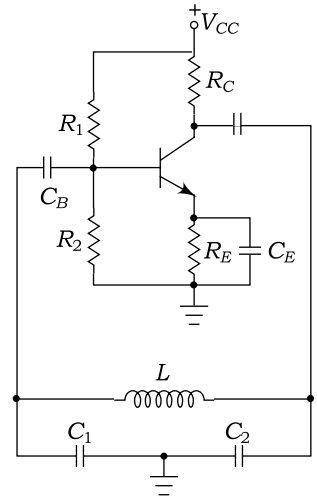


Fig. 5.20 Transistor Colpitts oscillators

Analysis of Colpitts Oscillator

Figure 5.21 shows the ac equivalent circuit of transistor Colpitts oscillator. In this circuit, actually, the current source $h_{fe}I_1$ is connected in parallel (shunt) with the resistance $\frac{1}{h_{oe}}$. After applying the Thevenin's theorem looking from AB terminals, we obtain a most simplified h-parameter ac equivalent circuit as depicted in Fig. 5.22. The Thevenin's t equivalent voltage is $\frac{h_{fe}}{h_{oe}} I_1$ and the internal resistance is $\frac{1}{h_{oe}}$.

The voltage difference between A and B is V_2.

$$V_2 = \frac{1}{h_{oe}} I_2 - \frac{h_{fe}}{h_{oe}} I_1$$

KVL loop equations are as follows:

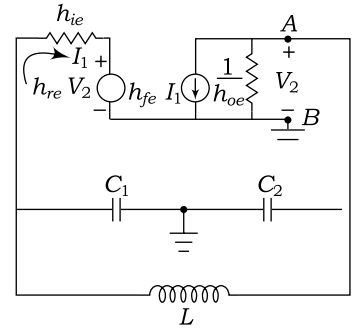


Fig. 5.21 Ac equivalent circuit of a Colpitts oscillator

Loop I equation is

$$\left(h_{ie}-\frac{h_{fe}h_{re}}{h_{oe}}-j\frac{1}{\omega C_1}\right)I_1+\frac{h_{re}}{h_{oe}}I_2+j\frac{1}{\omega C_1}I_3=0$$

Loop II equation is

$$-\frac{h_{fe}}{h_{oe}}I_1+\left(\frac{1}{h_{oe}}-j\frac{1}{\omega C_2}\right)I_2-j\frac{1}{\omega C_2}I_3=0$$

Loop III equation is

$$j\frac{1}{\omega C_1}I_1-j\frac{1}{\omega C_2}I_2+j\left(\omega L-\frac{1}{\omega C_1}-\frac{1}{\omega C_2}\right)I_3=0$$

The loop equations can be represented in combined form as

$$\begin{bmatrix} h_{ie}-\frac{h_{fe}h_{re}}{h_{oe}}-j\frac{1}{\omega C_1} & \frac{h_{re}}{h_{oe}} & j\frac{1}{\omega C_1} \\ -\frac{h_{fe}}{h_{oe}} & \frac{1}{h_{oe}}-j\frac{1}{\omega C_2} & -j\frac{1}{\omega C_2} \\ j\frac{1}{\omega C_1} & -j\frac{1}{\omega C_2} & j\omega L-j\frac{1}{\omega C_1}-j\frac{1}{\omega C_2} \end{bmatrix}\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}=0 \quad (5.33)$$

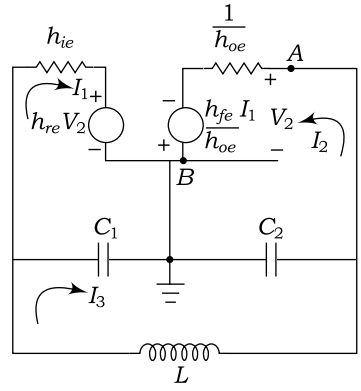


Fig. 5.22 Simplified ac equivalent circuit of a Colpitts oscillator

As I_1, I_2 and I_3 are not equal to zero, the determinant of the coefficients of I_1, I_2 and I_3 must be zero.
The real part of the determinant of the coefficients of I_1, I_2 and I_3 must be zero and we can derive

$$\frac{C_1}{C_2}=\frac{h_{fe}}{\Delta_{he}} \quad \text{where, } \Delta_{he}=(h_{ie}h_{oe}-h_{fe}h_{re})$$

Therefore, the condition of oscillation is $\frac{C_1}{C_2}=\frac{h_{fe}}{\Delta_{he}}$. For example, if $h_{fe}=100$ and $\Delta_{he}=0.5$, the condition for sustained oscillations is $\frac{C_1}{C_2}=\frac{h_{fe}}{\Delta_{he}}=\frac{100}{0.5}=200$.

The imaginary part of the determinant of the coefficients of I_1, I_2 and I_3 must be zero and we can derive

$$\omega^2=\frac{h_{oe}}{h_{ie}}\frac{1}{C_1C_2}+\frac{1}{LC_1}+\frac{1}{LC_2}$$

Then the frequency of oscillation is

$$\omega=2\pi f=\left(\frac{h_{oe}}{h_{ie}}\frac{1}{C_1C_2}+\frac{1}{LC_1}+\frac{1}{LC_2}\right)^{\frac{1}{2}}$$

or

$$f=\frac{1}{2\pi}\left(\frac{h_{oe}}{h_{ie}}\frac{1}{C_1C_2}+\frac{1}{LC_1}+\frac{1}{LC_2}\right)^{\frac{1}{2}} \quad (5.34)$$

Since $\frac{1}{LC_1}+\frac{1}{LC_2}>>\frac{h_{oe}}{h_{ie}}\frac{1}{C_1C_2}$, we get

$$f = \frac{1}{2\pi}\left(\frac{1}{LC_1} + \frac{1}{LC_2}\right)^{\frac{1}{2}} = \frac{1}{2\pi\sqrt{LC_{eq}}} \tag{5.35}$$

where, $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$ or $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$ which is the equivalent capacitance of C_1 and C_2 connected in series.

Example 5.8 In a Colpitts oscillator, the value of capacitors are $C_1 = 0.25$ pF and $C_2 = 0.020$ pF the inductance of coils are $L_1 = 0.5$ mH. Calculate the frequency of oscillations and the required gain for oscillation.

Sol. Given $C_1 = 0.25$ pF, $C_2 = 0.020$ pF and $L_1 = 0.5$ mH

The equivalent capacitance of $C_1$and C_2,

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.25 \times 0.020}{0.25 + 0.020}\text{pF} = 0.0185 \text{ pF}$$

The frequency of the Colpitts oscillator is

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.5 \times 10^{-3} \times 0.0185 \times 10^{-12}}} = 0.523565 \text{ MHz}$$

Example 5.9 In a Colpitts oscillator, the value of capacitors are $C_1 = 0.125$ μF and $C_2 = 0.020$ μF the inductance of coil is $L_1 = 0.5$ mH.

(a) Find the frequency of oscillation.

(b) If the frequency of the oscillation is 20 kHz, find the value of inductance of coil. Determine the voltage gain of oscillator.

Sol. Given $C_1 = 0.125$ μF , $C_2 = 0.020$ μF and $L_1 = 0.5$ mH

(a) The equivalent capacitance of C_1 and C_2,

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.125 \times 0.020}{0.125 + 0.020}\mu\text{F} = 0.01724\ \mu\text{F}$$

The frequency of the Colpitts oscillator is

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.5 \times 10^{-3} \times 0.01724 \times 10^{-6}}} = 54.236 \text{ kHz}$$

(b) When frequency of the oscillation is 20 kHz, the value of inductance of coil is

$$L = \frac{1}{4\pi^2 f^2 C_{eq}} = \frac{1}{4\pi^2 (20 \times 10^3)^2 \times 0.01724 \times 10^{-6}} = 3.677 \text{ mH}$$

The voltage gain is $\frac{C_1}{C_2} = \frac{0.125}{0.020} = 6.25$

Example 5.10 In a Colpitts oscillator, the values of capacitors and coil inductance are $C_1 = 0.5$ μF and $C_2 = 2.5$ μF and $L_1 = 0.5$ mH.

(a) When the output voltage is 10 V, calculate the feedback voltage.

(b) What is the frequency of oscillation

Sol. Given $C_1 = 0.5\ \mu F$, $C_2 = 8.5\ \mu F$ and $L_1 = 0.5$ mH

(a) The feedback voltage is the voltage across C_2 and it is directly proportional to XC_2.
Therefore, $V_f \propto XC_2$
The output voltage is the voltage across C_1 and it is directly proportional to XC_1.
so that $V_o \propto XC_1$

$$\frac{V_f}{Vo} = \frac{XC_2}{XC_1} = \frac{\frac{1}{\omega C_2}}{\frac{1}{\omega C_1}} = \frac{C_1}{C_2}$$

$$V_f = \frac{C_1}{C_2} V_o = \frac{0.5}{2.5} \times 10 = 2 \text{ V}$$

(b) The equivalent capacitance of C_1 and C_2,

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.5 \times 2.5}{0.5 + 2.5} \mu\text{F} = 0.417\ \mu\text{F}$$

The frequency of the Colpitts oscillator is

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.5 \times 10^{-3} \times 0.417 \times 10^{-6}}} = 11.02779 \text{ kHz}$$

5.11.2 Hartley Oscillator

Figure 5.23 shows the Hartley oscillator. The quiescent operating point of the transistor can be established by the supply voltage V_{CC} and the resistances R_1, R_2, R_C and R_E. The capacitor C_B is the blocking capacitor and is used to block the dc current flow. The reactance of capacitor C_B is negligible at the frequency of oscillation. C_E is the emitter-bypass capacitor. C_E is connected in parallel with resistance R_E and it will not appear in the ac equivalent circuit. As the transistor operates in common-emitter configuration, it introduces 180° phase shift between input and output voltages. In this circuit, the voltage across the tank circuit is connected to the collector. The feedback voltage is a fraction of the output voltage. As the feedback voltage is equal to the voltage across L_1 and it is 180° out of phase with respect to output voltage, the total phase shift around the loop is 0° or 360°. The frequency determining network is formed by the inductors L_1 and L_2 and capacitor C.

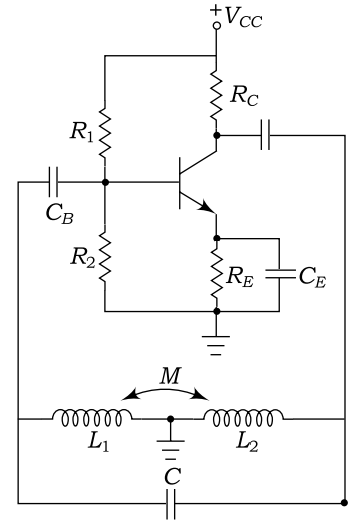


Fig. 5.23 Transistor Hartley Oscillator

In this circuit, X_1, X_2 and X_3 are reactance of inductors L_1 and L_2 and capacitor C respectively. The reactance values are

$$X_1 = \omega(L_1 + M), \quad X_2 = \omega(L_2 + M), \text{ and } X_3 = -\frac{1}{\omega C} \tag{5.36}$$

where, M is the mutual inductance.

The condition for oscillation is

$$(X_1 + X_2 + X_3) = 0$$

so that $$\omega(L_1 + M)) + \omega(L_2 + M) = \frac{1}{\omega C}$$

or $$\omega(L_1 + L_2 + 2M) = \frac{1}{\omega C}$$

or $$\omega^2 = \frac{1}{(L_1 + L_2 + 2M)C}$$

or $$\omega^2 = \frac{1}{L_{eq}C} \quad \text{as } L_{eq} = (L_1 + L_2 + 2M)$$

or $$\omega = \frac{1}{\sqrt{L_{eq}C}}$$

or $$2\pi f = \frac{1}{\sqrt{L_{eq}C}}$$

The frequency of oscillation is

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}} \text{ and} \qquad (5.37)$$

The condition for sustained oscillation is

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M} \qquad (5.38)$$

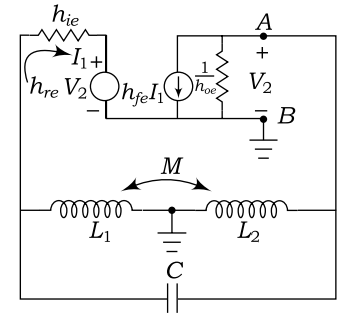


Fig. 5.24 The ac equivalent circuit of a Hartley oscilllator

Analysis of Hartley Oscillator

Figure 5.24 shows the *h*-parameter model ac equivalent circuit of Hartley oscillator. In this circuit, actually, the current source $h_{fe}I_1$ is connected in parallel (shunt) with the resistance $\frac{1}{h_{oe}}$. After applying the Thevenin's theorem looking from *AB* terminals, we obtain a most simplified circuit as shown in Fig. 5.25. The Thevenin's equivalent voltage is $\frac{h_{fe}}{h_{oe}}I_1$ and the internal resistance is $\frac{1}{h_{oe}}$. For simplifying the analysis of oscillator circuit, the mutual inductance between L_1 and L_2 is neglected.

The voltage across *A* and *B* is V_2

$$V_2 = \frac{1}{h_{oe}}I_2 - \frac{h_{fe}}{h_{oe}}I_1$$

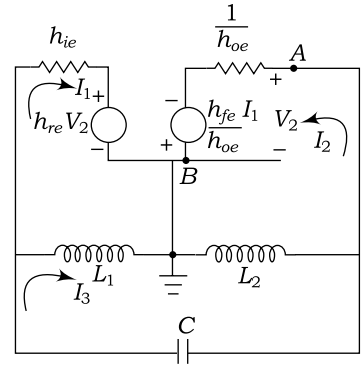


Fig. 5.25 Simplified ac equivalent circuit of a Hartley oscilllator

KVL equation for LOOP I is

$$\left(h_{ie} + j\omega L_1 - \frac{h_{fe}h_{re}}{h_{oe}}\right)I_1 + \frac{h_{re}}{h_{oe}}I_2 - j\omega L_1 I_3 = 0$$

KVL equation for LOOP II is

$$-\frac{h_{fe}}{h_{oe}}I_1 + \left(\frac{1}{h_{oe}} + j\omega L_2\right)I_2 + j\omega L_2 I_3 = 0$$

KVL equation for LOOP III is

$$-j\omega L_1 I_1 + j\omega L_2 I_2 + \left(j\omega L_1 + j\omega L_2 - j\frac{1}{\omega C}\right)I_3 = 0$$

The loop equation can be represented in combined form as

$$\begin{bmatrix} h_{ie} + j\omega L_1 - \frac{h_{fe}h_{re}}{h_{oe}} & \frac{h_{re}}{h_{oe}} & -j\omega L_1 \\ -\frac{h_{fe}}{h_{oe}} & \frac{1}{h_{oe}} + j\omega L_2 & j\omega L_2 \\ -j\omega L_1 & j\omega L_2 & j\omega L_1 + j\omega L_2 - j\frac{1}{\omega C} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = 0 \tag{5.39}$$

As I_1, I_2 and I_3 are not equal to zero, the determinant of the coefficients of I_1, I_2 and I_3 must be zero. The determinant of the coefficients of I_1, I_2 and I_3 is equal to zero, then we get

$$\left(h_{ie} + j\omega L_1 - \frac{h_{fe}h_{re}}{h_{oe}}\right)L_2^2 + \frac{h_{re}}{h_{oe}}L_1L_2 - \frac{h_{fe}}{h_{oe}}L_1L_2 + \left(\frac{1}{h_{oe}} + j\omega L_2\right)L_1^2 = 0 \tag{5.40}$$

as $\omega L_1 + \omega L_2 - \frac{1}{\omega C} = 0$ during oscillation.

The real part of the above equation is

$$\Delta_{he}L_2^2 - (h_{fe} - h_{re})L_1L_2 + L_1^2 = 0 \quad \text{where, } \Delta_{he} = (h_{ie}h_{oe} - h_{fe}h_{re})$$

or

$$\Delta_{he}L_2^2 - h_{fe}L_1L_2 + L_1^2 = 0 \quad \text{as } h_{re} << 1 \tag{5.41}$$

The value of inductance L_2 is

$$L_2 = \frac{h_{fe}L_1 \pm \sqrt{h_{fe}L_1^2 - 4\Delta_{he}L_1^2}}{2\Delta_{he}}$$

or

$$L_2 = \frac{h_{fe}L_1}{2\Delta_{he}} \quad \text{as } h_{fe}^2 >> 4\Delta_{he} \tag{5.42}$$

The imaginary part of Eq. (5.40) is equal to zero and we can write

$$\frac{\omega}{C}L_1L_2 + \frac{h_{ie}}{h_{oe}}\left(\omega L_1 + \omega L_2 - \frac{1}{\omega C}\right) = 0$$

or $$\omega^2 = \frac{1}{\left(\frac{h_{oe}L_1L_2}{h_{ie}}\right) + C(L_1 + L_2)} \tag{5.43}$$

The frequency of oscillation is

$$f = \frac{1}{2\pi}\frac{1}{\sqrt{\frac{h_{oe}L_1L_2}{h_{ie}} + C(L_1 + L_2)}}$$

As $C(L_1 + L_2) >> \frac{h_{oe}L_1L_2}{h_{ie}}$, the $f = \frac{1}{2\pi}\frac{1}{\sqrt{C(L_1 + L_2)}}$

Then, oscillator frequency is $f = \frac{1}{2\pi}\frac{1}{\sqrt{L_{eq}C}}$ where $L_{eq} = L_1 + L_2$ (5.44)

In the above analysis, the mutual inductance M between L_1 and L_2 is neglected. When M is incorporated in the analysis, L_1 will be replaced by $L_1 + M$ and L_2 will be replaced by $L_2 + M$.

Example 5.11 In a Hartley oscillator $L_1 = 0.02$ mH and $C = 0.047$ μF. When the frequency of the oscillator is 100 kHz, determine the value of L_2. Assume mutual inductance is negligible.

Sol. Given $L_1 = 0.02$ mH, $C = 0.047$ μF and $f = 100$ kHz

The frequency of the Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

The value of $L_2 = \frac{1}{4\pi^2 f^2 C} - L_1$

$$= \frac{1}{4\pi^2 \times (100 \times 10^3)^2 \times 0.047 \times 10^{-6}} - 0.02 \times 10^{-3}$$

$$= (0.05396 - 0.02) \text{ mH} = 0.03396 \text{ mH}$$

Example 5.12 The frequency of a transistorised Hartley oscillator can be varied from 50 kHz to 100 kHz. The tuning capacitor can be changed from 100 pF to 400 pF. Determine the values of inductances. Assume $h_{fe} = 100$ and $\Delta_{he} = 0.1$

Sol. Given $h_{fe} = 100$ and $\Delta_{he} = 0.1$, range of frequency = 50 kHz to 100 kHz and capacitor range 100 pF to 400 pF

The frequency of a transistorised Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

The effective inductance $L_1 + L_2 = \frac{1}{4\pi^2 f^2 C}$ mH

The ratio of inductances is $\frac{L_2}{L_1} = \frac{h_{fe}}{\Delta_{he}} = \frac{100}{0.1} = 1000$

So that $L_2 = 1000\ L_1$

The frequency variation ratio is 50 kHz : 100 kHz = 1:2. This frequency variation can be achieved by the capacitance ratio 100 pF : 400 pF = 1:4. Therefore, if frequency is 50 kHz, the capacitance value will be 400 pF.

When $f = 50$ kHz, $L_1 + L_2 = \frac{1}{4\pi^2 f^2 C}$

$$= \frac{1}{4\pi^2 (50 \times 10^3)^2 \times 400 \times 10^{-12}} \text{H}$$

$$= 25.35 \text{ mH}$$

$L_1 + L_2 = 1001 L_1 = 25.35$ mH (as $L_2 = 1000 L_1$)

Therefore, $L_1 = 0.02532$ mH and $L_2 = 25.32468$ mH

Example 5.13 A Hartley oscillator uses a tank circuit with $L_1 = 0.4$ mH, $L_2 = 0.3$ mH and $C = 0.047$ μF. What is the frequency of oscillator? Assume mutual inductance is negligible.

Sol. Given $L_1 = 0.4$ mH, $L_2 = 0.3$ mH and $C = 0.047$ μF

The frequency of the Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

$$= \frac{1}{2\pi\sqrt{(0.4 \times 10^{-3} + 0.3 \times 10^{-3}) \times 0.047 \times 10^{-6}}}$$

$$= \frac{1}{2\pi \times 0.5735 \times 10^{-5}} = 27.765 \text{ kHz}$$

Example 5.14 In a Hartley oscillator, $L_2 = 0.2$ mH and $C = 0.47$ nF. When the frequency of the oscillator is 150 kHz, determine the value of L_1. Assume mutual inductance is negligible.

Sol. Given $L_2 = 0.2$ mH, $C = 0.47$ nF and frequency of the oscillator $f = 150$ kHz

The frequency of the Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

The value of inductance L_1 is

$$L_1 = \frac{1}{4\pi^2 f^2 C} - L_2$$

$$= \frac{1}{4\pi^2 (150 \times 10^3)^2 \times 0.47 \times 10^{-9}} - 0.2 \times 10^{-3}$$

$$= 2.397 \text{ mH} - 0.2 \text{ mH} = 2.197 \text{ mH}$$

Example 5.15 In a transistorised Hartley oscillator L_1 = 0.5 mH, L_2 = 0.5 μH while the frequency has been changed from 100 kHz to 2000 kHz. Determine the range of capacitor. Assume mutual inductance is negligible.

Sol. Given L_1 = 0.5 mH, L_2 = 0.5 μH and range of frequency = 100 kHz to 2000 kHz

The frequency of the Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

The value of the capacitor is

$$C = \frac{1}{4\pi^2 f^2 (L_1 + L_2)}$$

When f_1 = 100 kHz, the capacitor value is

$$C = \frac{1}{4\pi^2 f_1^2 (L_1 + L_2)} = \frac{1}{4\pi^2 (100 \times 10^3)^2 (0.5 \times 10^{-3} + 0.5 \times 10^{-6})}$$
$$= 5.066 \text{ nF}$$

When f_2 = 2000 kHz,

$$C = \frac{1}{4\pi^2 f_2^2 (L_1 + L_2)} = \frac{1}{4\pi^2 (2000 \times 10^3)^2 (0.5 \times 10^{-3} + 0.5 \times 10^{-6})}$$
$$= 12.665 \text{ pF}$$

Therefore, the range of capacitance is 5.066 nF to 12.665 pF.

Example 5.16 In a Hartley oscillator, the value of capacitor is 250 pF and the inductance of coils are L_1 = 0.5 mH, L_2 = 0.025 mH. Calculate the frequency of oscillations and the feedback factor. Assume mutual inductance is negligible.

Sol. Given C = 250 pF, L_1 = 0.5 mH, L_2 = 0.025 mH

The frequency of the Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}} = \frac{1}{2\pi\sqrt{(0.5 + 0.025) \times 10^{-3} \times 250 \times 10^{-12}}}$$
$$= 439.53 \text{ kHz}$$

The feedback factor is $\beta = \frac{L_1}{L_2} = \frac{0.5}{0.025} = 20$

5.12 CRYSTAL OSCILLATORS

To get high frequency stability in an oscillator circuit, crystal is used as the frequency-determining element. This type of oscillator is known as crystal oscillator. Usually, cut-quartz crystals are used in crystal oscillators. There are two different methods of cutting of quartz crystals. Actually, the methods of cutting help to find out the resonant frequency of oscillation and temperature coefficient of the crystal. The cross section of a crystal is hexagonal. When the crystal is cut in such a way that its flat surfaces are perpendicular to the *X*-axis (electrical axis), this cut is called *X-cut crystal*. If the crystal is cut in such a way that its flat surfaces are perpendicular to *Y*-axis (mechanical axis), this cut is called *Y-cut crystal*. Figure 5.26(a) shows the quartz crystal, and *X*-cut and *Y*-cut of quartz crystal are shown in Fig. 5.26(b) and (c) respectively.

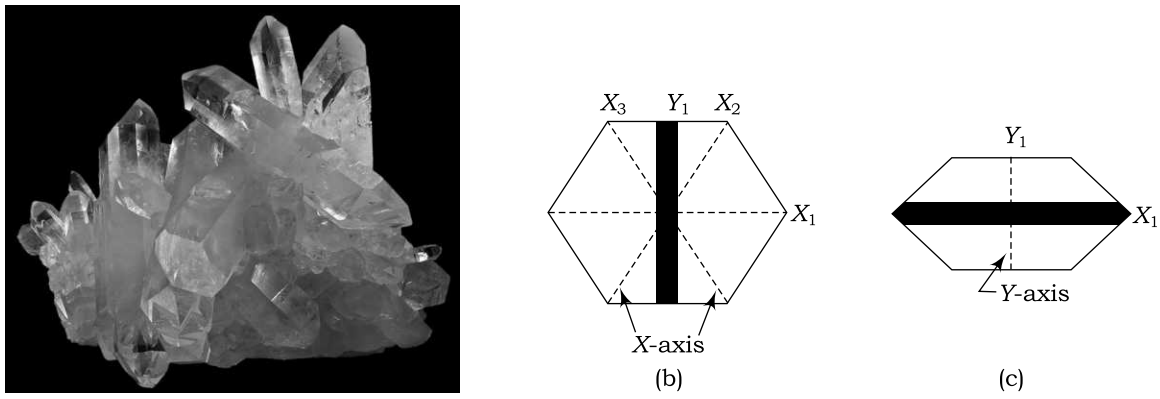


Fig. 5.26 (a) Quartz crystal (b) X-cut Quartz crystal (c) Y-cut Quartz crystal

When the edges of an *X*-cut crystal are subjected to mechanical stress, an electrical potential will be developed across its faces. The polarity of electrical potential will be reversed when stress changes from tension to compression. If electrodes are placed on opposite faces of the crystal or quartz (*X*-cut or *Y*-cut crystal) and a voltage is applied across the electrodes, a mechanical stress is developed along the edges. Actually, the set up electric field exerts forces on bound charges within the crystal. Then the crystal vibrates electromechanically. This property of a crystal is known as *piezoelectric effect*. The crystal oscillators are available within a wide range of frequencies from a few kHz to 100 MHz and *Q*-factors will be a few thousand to several hundred thousands. The crystal oscillator frequency is very stable with respect to temperature variation and aging. Figure 5.27(a) shows the crystal oscillator, and its reactance variation with respect to frequency is depicted in Fig. 5.27(c).

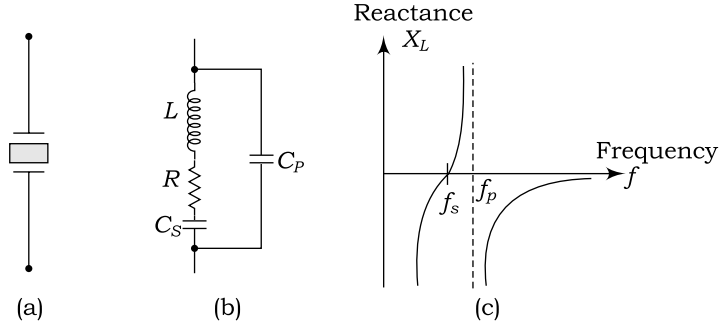


Fig. 5.27 (a) Symbol of crystal oscillator (b) Its circuit model (c) Reactance variation with respect to frequency

Figure 5.27(b) shows an *L R* C_S series resonant circuit which is used to represent a piezoelectric crystal. The inductance *L*, capacitance C_S and resistance *R* are electrical equivalent of the mass, compliance and friction of the vibrating crystal respectively. The capacitance C_S is the electrostatic capacitance between the electrodes and crystal as the dielectric. The values of *L*, C_S, *R* and C_P depends on crystal cut and its size and on the nature of vibration of the crystal oscillator.

This circuit has two resonant frequencies such as series resonant frequency and parallel resonant frequency. At series resonant frequency f_S, the reactance of the series arm is zero so that $\omega_S L - \dfrac{1}{\omega_S C_S} = 0$

Then series resonant frequency is $f_S = \frac{1}{2\pi\sqrt{LC_S}}$. At the frequency f_S, the impedance of the series arm is equal to R.

At parallel resonant frequency f_P, the reactance of the circuit will be zero. Then we can write

$$\omega_P L - \frac{1}{\omega_P C_s} - \frac{1}{\omega C_P} = 0$$

Subsequently, parallel resonant frequency is $f_P = \frac{1}{2\pi\sqrt{LC_{eq}}}$ where, $C_{eq} = \frac{C_S C_P}{C_S + C_P}$. (5.45)

The variation of reactance with frequency is depicted in Fig. 5.27(c). For the frequency range $0 < f < f_S$, X is negative, i.e., capacitive. At series resonant frequency $f = f_S$, $X = 0$. In the frequency range $f_S < f < f_P$, X is positive, i.e., inductive. When $f > f_P$, X is capacitive and asymptotically approaches zero.

Figure 5.28 shows a crystal oscillator circuit. If we compare this circuit with a Colpitts oscillator circuit, we find that both the circuits are identical except inductor of the Colpitts oscillator is replaced by crystal. The frequency of oscillation of the crystal oscillator is the parallel resonant frequency $f_P = \frac{1}{2\pi\sqrt{LC_{eq}}}$ where, $C_{eq} = \frac{C_S C_P}{C_S + C_P}$. Since R is very small, the quality factor Q of the circuit is very high. The typical value of Q will be several hundred thousands. The crystal oscillators are available within a wide range of frequencies from some kHz to several MHz and Q factors will be of few thousand to several hundred thousands. The stability of crystal oscillator frequency is very stable with respect to temperature and aging.

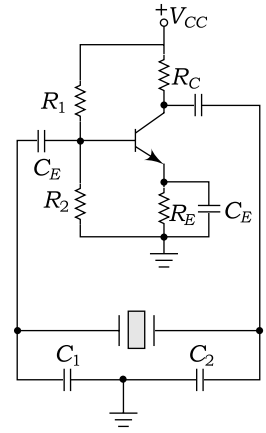


Fig. 5.28 Circuit of a crystal oscillator

Example 5.17 In a crystal oscillator, the value of inductance $L = 0.25$ mH, capacitor $C_S = 0.047$ pF capacitor $C_P = 4.77$ pF and $R = 10$ k. Determine the series resonant frequency, parallel resonant frequency and Q-factor of the crystal.

Sol. Given $L = 0.25$ mH, $C_S = 0.047$ pF, $C_P = 4.77$ pF and $R = 10$ kΩ

The series resonant frequency is $f_S = \frac{1}{2\pi\sqrt{LC_S}}$

$$= \frac{1}{2\pi\sqrt{0.25\times10^{-3}\times0.047\times10^{-12}}} = 46.45 \text{ MHz}$$

The parallel resonant frequency is $f_P = \frac{1}{2\pi\sqrt{LC_{eq}}}$

where, $C_{eq} = \frac{C_S C_P}{C_S + C_P} = \frac{0.047\times4.77}{0.047 + 4.77} = 0.0465$ pF

or $$f_p = \frac{1}{2\pi\sqrt{0.25\times10^{-3}\times0.0465\times10^{-12}}} = 46.70 \text{ MHz}$$

Q-factor of the crystal at series resonant frequency is

$$Q_S = \frac{\omega_S L}{R} = \frac{2\pi \times 46.45 \times 10^6 \times 0.25}{10 \times 10^3} = 7292.65$$

Q-factor of the crystal at parallel resonant frequency is

$$Q_P = \frac{\omega_P L}{R} = \frac{2\pi \times 46.70 \times 10^6 \times 0.25}{10 \times 10^3} = 7331.9$$

Example 5.18 Determine the value of R_f and frequency of RC phase shift oscillators if R = 10 kΩ and C = 0.001 μF

Sol. Frequency of oscillation is

$$f_o = \frac{1}{2\pi\sqrt{6}RC} = \frac{1}{2\pi\sqrt{6} \times 10 \times 10^3 \times 0.001 \times 10^{-6}} = 6.501 \text{ kHz}$$

For oscillation, the gain of an amplifier should be at least 29. Therefore, |A| ≥ 29

Since $|A| = \frac{R_f}{R_1}, \frac{R_f}{R_1} \geq 29$ or $R_f = 29R_1$. As $R_1 = 1k$, $R_f = 29k$

Example 5.19 Design a UJT relaxation oscillator to generate a 500 Hz sawtooth waveform. Assume V_{BB} = 18 V, V_P = 3.5 V, V_V = 1.5 V, I_P = 1.6 mA and I_V = 3.5 mA. Assume η = 0.55

Sol. $$R_E < \frac{V_{BB} - V_P}{I_P} \text{ or } R_E < \frac{18 - 3.5}{1.6 \times 10^{-3}} = 9.0625 \text{ kΩ}$$

$$R_E > \frac{V_{BB} - V_V}{I_V} > \frac{18 - 1.5}{3.5 \times 10^{-3}} = 4.7142 \text{ kΩ}$$

Therefore, R_E = 9.0265 kΩ

We know that

$$f = \frac{1}{T} = \frac{1}{2.3R_E C_E \log_{10} \frac{1}{1-\eta}} \text{ or } 500 = \frac{1}{2.3 \times 9026.5 C_E \log_{10} \frac{1}{1-0.55}}$$

Therefore, $C_E = \frac{1}{500 \times 2.3 \times 9026.5 \times 0.346} = 0.278 \text{ μF}$

Example 5.20 Design a phase-shift oscillator to operate at a frequency of 5 kHz. Use a JFET with μ = 55 and r_d = 5.5 kΩ. The phase-shift network is not to load down the amplifier. (i) Find the minimum value of the drain-current resistance (R_D) for which the circuit will oscillate. (ii) Find the product RC. (iii) Choose a reasonable value of R and find C.

Sol. For oscillation, |A| = 29

We know that $A = \frac{\mu R_D}{r_d + R_D}$.

Therefore, $29 = \frac{55R_D}{5.5 \times 10^3 + R_D}$ or, $R_D = \frac{29 \times 5.5 \times 10^3}{55 - 29} = 6.134 \text{ kΩ}$

We know that $\alpha = \sqrt{6} = \dfrac{1}{2\pi fRC}$.

Therefore, $RC = \dfrac{1}{2\pi\sqrt{6}f} = \dfrac{1}{2\pi\sqrt{6}\times 5\times 10^3} = 0.013001\times 10^{-3}$

$$R_L = r_d \| R_D = \frac{5.5\times 6.134}{5.5+6.134} = 2.899\ \text{k}\Omega$$

Assume R is ten times of R_L then $R = 28.99\ \text{k}\Omega$

Therefore, $C = \dfrac{0.013001\times 10^{-3}}{28.99\times 10^3} = 0.448\ \text{nF}$

Review Exercises

Short-Answer Questions

1. What is an oscillator?

Ans. An oscillator is an electronic circuit that generates a repetitive electronic signal or periodic waveforms from a few hertz (Hz) to several gigahertz (GHz). Oscillators are known as wave generators which generate sinusoidal, square, rectangular, sawtooth and trapezoidal wave signals.

2. What is the Barkhausen criterion for an oscillator?

Ans. The Barkhausen criterion for oscillator is that the loop gain must be slightly greater than unity ($\beta A \geq 1$) and the phase shift around the loop must be 360°.

3. What are the conditions for the successful operation of a phase-shift oscillator?

Ans. For the successful operation of a phase-shift oscillator, the gain must be ≥ 29 and the total phase shift of the circuit must be 360°.

4. Explain why positive feedback and not negative feedback is necessary to produce oscillations?

Ans. In negative feedback, the feedback factor βA is less than unity. Therefore, βAV_{in} is less than V_{in} and so the output signal will die out. In positive feedback, the feedback factor βA is greater than unity. As βAV_{in} is greater than V_{in}, an oscillation output signal will be generated.

5. Why are LC oscillator circuits impractical in audio-frequency range?

Ans. In audio-frequency range, the required *LC* components are too bulky, heavyweight and very expensive. Therefore, *LC* oscillator circuits are impractical in audio frequency range.

6. What is the difference between Hartley and Colpitts oscillators in construction?

Ans. A Hartley oscillator is similar to a Colpitts oscillator in construction except for the phase-shift network. A Hartley oscillator consists of two inductors and one capacitor, whereas a Colpitts oscillator consists of two inductors and one capacitor.

7. Why are Colpitts oscillators used to generate fixed radio-frequency signals?

Ans. Colpitts oscillators can be tuned by changing the inductance or capacitance of the tank circuit. The smooth variation of L is very difficult and for capacitive tuning, C_1 and C_2 must be changed simultaneously in the ratio of about 100:1, which is a difficult task. Therefore, Colpitts oscillators are used to generate fixed radio-frequency signals.

8. Why are crystal oscillators used in communication equipments?

Ans. As crystal oscillators have very high frequency stability, these oscillators are used in communication equipments.

9. What is the range of frequencies of crystal oscillators? Why?

Ans. Crystal oscillators are generally used in the frequency range from 15 kHz to 10 MHz. At low frequency, the size of the quartz crystal is large and at very high frequency, the thickness of the crystal is so small that it becomes fragile.

10. What is frequency stability of an oscillator?

Ans. In an oscillator, the tank circuit parameters determine the frequency of oscillator's output signal. As the tank circuit parameters change with temperature and climate conditions, the frequency of oscillation does not remain constant. The frequency stability of an oscillator states that frequency variation must be about zero. The quartz-crystal oscillator has very high frequency stability.

Multiple-choice Questions

1. A positive feedback amplifier with gain A and feedback path gain β works as an oscillator if
   (a) $|\overline{\beta}\overline{A}| = 1$ and $\angle\overline{\beta}\overline{A} = 180°$ (b) $|\overline{\beta}\overline{A}| = 2$ and $\angle\overline{\beta}\overline{A} = 180°$
   (c) $|\overline{\beta}\overline{A}| = 1$ and $\angle\overline{\beta}\overline{A} = 360°$ (d) $|\overline{\beta}\overline{A}| = 2$ and $\angle\overline{\beta}\overline{A} = 360°$
2. The maximum phase shift of the *RC* network as shown in Fig. 5.29 is
   (a) 90° (b) 180 (c) 270° (d) 360°

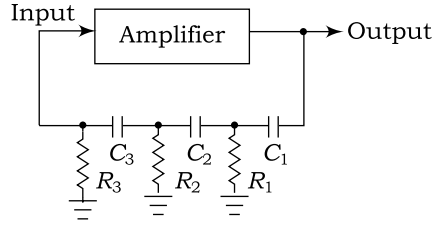


Fig. 5.29

3. Which of the following oscillators is used for generating low frequencies?
   (a) *RC* phase shift oscillator (b) *LC* oscillator
   (c) Wein-bridge oscillator (d) Blocking oscillator
4. An oscillator is an amplifier that uses
   (a) positive feedback (b) negative feedback
   (c) degenerative feedback (d) differentiators and integrators
5. Wein-bridge oscillators are
   (a) sinusoidal oscillators (b) multivibrators
   (c) nonsinusoidal oscillators (d) relaxation oscillators
6. The resonant frequency of a Wein-bridge oscillator is about
   (a) 10 Hz (b) 10 kHz (c) 100 kHz (d) 10 MHz

7. Which of the following statements is true of phase-shift type and Wein-bridge-type *RC* oscillator?
   (a) Both use positive feedback.
   (b) The phase-shift type oscillator uses positive feedback only whereas Wein-bridge oscillator uses both positive and negative feedback.
   (c) The phase-shift-type oscillator uses both positive and negative feedback whereas the Wein-bridge oscillator uses positive feedback only.
   (d) Both use negative feedback.
8. The Barkhausen criterion for oscillations in a feedback amplifier at a particular frequency is
   (a) the magnitude of the loop gain must be equal to 1 and the phase shift must be 360°
   (b) the magnitude of the loop gain must be greater than 1 when the phase shift is less than 360°
   (c) the magnitude of the loop gain must be greater than 1 when the phase shift is 180°
   (d) the magnitude of the loop gain must be less than 1 when the phase shift is 180°
9. In a practical sinusoidal oscillator,
   (a) the magnitude of the loop gain is slightly greater than 1, and the amplitude of the oscillation is limited by circuit parameters.
   (b) the phase shift of the loop gain is less than 360° and the oscillation frequency is variable with temperature
   (c) the magnitude of the loop gain is 1 and the phase shift is 180°
   (d) the magnitude of the loop gain is slightly greater than 1 and the phase shift is 180°
10. The frequency of oscillation of an *RC* phase shift oscillator is

    (a) $f = \frac{1}{2\pi RC\sqrt{6}}$ (b) $f = \frac{1}{2\pi RC\sqrt{3}}$ (c) $f = \frac{1}{2\pi RC\sqrt{16}}$ (d) $f = \frac{1}{2\pi RC\sqrt{4}}$

11. In a phase-shift oscillator, the *RC* sections in the feedback path provide a phase shift of 180° and it is very difficult to design with bipolar transistors as
    (a) the base current loads the phase shift *RC* network
    (b) bipolar transistors have a current gain greater than 1
    (c) the base-emitter voltage is about 0.7 V
    (d) bipolar transistors provide a phase- shift of 180° but not 360°
12. The frequency of oscillation of a BJT *RC* phase-shift oscillator is

    (a) $f = \frac{1}{2\pi RC\sqrt{6}}$ (b) $f = \frac{1}{2\pi RC\sqrt{6+4K}}$

    (c) $f = \frac{1}{2\pi RC\sqrt{6K+4}}$ (d) $f = \frac{1}{2\pi RC\sqrt{6-4K}}$

13. Colpitts and Hartley oscillators use the _____ feedback.
    (a) voltage-series (b) current-series (c) voltage-shunt (d) current-shunt
14. In a Wein-bridge oscillator, the feedback factor β is

    (a) $\beta = \frac{V_i}{V_o} = \frac{1}{\delta}$ (b) $\beta = \frac{V_i}{V_o} = \delta$ (c) $\beta = \frac{V_i}{V_o} = \frac{1}{\delta^2}$ (d) $\beta = \frac{V_i}{V_o} = \delta^2$

15. A quartz crystal is widely used in the design of sinusoidal oscillators as
    (a) the crystal is corresponding to a very high-*Q LC*-tuned circuit and its characteristics are stable with respect to temperature and time
    (b) when pressure is applied to the crystal, it generates electrical oscillations
    (c) the crystal provides accurate positive feedback
    (d) piezoelectric properties of quartz crystal provide very low-*Q LC*-tuned circuit
16. The frequency of oscillation of a Hartley oscillator is
    (a) $f = \frac{1}{2\pi\sqrt{L_{eq}C}}$ (b) $f_o = \frac{1}{2\pi\sqrt{LC_{eq}}}$ (c) $f = \frac{1}{2\pi RC\sqrt{6}}$ (d) $f = \frac{1}{2\pi RC}$
17. If gain is A and feedback factor is β, then condition to sustain oscillation of Wein-bridge oscillator is
    (a) $A = \frac{1}{3}, \beta = 3$ (b) $A = 3, \beta = \frac{1}{3}$
    (c) $A = 6, \beta = \frac{1}{6}$ (d) $A = \frac{1}{6}, \beta = 6$
18. A Wien-bridge oscillator uses Wien-bridge for
    (a) tuning phase shift
    (b) tuning
    (c) phase shift
    (d) either tuning or phase shift

Review Questions

1. Define an oscillator. What are the types of oscillators? What are the basic requirements of an oscillator circuit?
2. Write the basic principle of an oscillator. Explain the Barkhausen criteria for oscillation.
3. State the different conditions for oscillations in a feedback amplifier.
4. Explain Nyquist criterion to check the stability of an amplifier.
5. Explain the following:
   (a) Phase shift in oscillation
   (b) Phase-shift oscillator
   (c) BJT phase-shift oscillator
   (d) FET phase-shift oscillator
6. Draw a transistor phase-shift oscillator circuit. Derive an expression for the frequency of oscillation and the condition for sustained oscillations.
7. Justify the statement "Positive feedback amplifier works as an oscillator".
8. Draw a Wein-bridge oscillator using OP-AMP and *RC* bridge circuit and derive an expression for the frequency of oscillation.
9. (a) State the amplitude stability of Wein-bridge oscillator.
   (b) Justify the statement "The amplifier gain in a Wein-bridge oscillator must be greater than 3 for sustained oscillations".
   (c) Write the advantages and disadvantages of a Wein-bridge oscillator.
   (d) Write the difference between *RC* phase-shift oscillator and Wein-bridge oscillator.

10. Explain the operating principle of a tuned collector oscillator. Derive an expression for the frequency of oscillation. Write the condition for sustained oscillations.
11. Give the basic principle of operation of tuned *LC* oscillator.
12. Draw the circuit of transistor Colpitts oscillator and explain its operation. Analyse transistor Colpitts oscillator and derive an expression for the frequency of oscillation and the condition for sustained oscillations.
13. (a) Explain the Hartley oscillator and explain its operation.
    (b) Analyse transistor Hartley oscillator and derive an expression for the frequency of oscillation and the condition for sustained oscillations.
    (c) What is the difference between Colpitts oscillator and Hartley oscillator?
14. (a) State the principle of operation of a crystal oscillator and derive the frequency of oscillation.
    (b) What are the advantages of crystal oscillators?
15. In an *RC* phase-shift oscillator, if the value of resistors are $R_1 = R_2 = R_3 = 150$ kΩ and the value of capacitors are $C_1 = C_2 = C_3 = 0.25$ nF. Determine the frequency of the oscillation.
16. Find the frequency of oscillation in an *RC* phase-shift oscillator as shown in Fig. 5.11. Assume $R = 25$ kΩ, $C = 0.011$ μF, and $R_C = 5.2$ kΩ. Determine the minimum value of current gain for the oscillation.
17. Determine the value of capacitors and current gain of the transistor when the frequency of oscillation in a *RC* phase shift oscillator is 20 kHz. Assume $R_1 = R_2 = R_3 = R = 150$ kΩ, $R_C = 4.7$ kΩ.
18. In a Wein-bridge oscillator when the value of resistor $R = 250$ kΩ and the frequency of the oscillation is 30 kHz, determine the value of the capacitor *C*.
19. In a Wein-bridge oscillator, the value of capacitors can be changed from 10 pF to 100 pF to generate sine wave output signals from 50 Hz to 50 kHz.
    (a) Determine the resistances required to generate the output signals from 50 Hz to 50 kHz.
    (b) If the gain of the amplifier is 5, what will be the ratio of the resistances in the other arms of the bridge?
20. A tuned collector oscillator is used in a radio receiver and it has inductance $L_P = 0.5$ mH and its tuning frequency range from 200 Hz to 800 kHz. Determine the range of capacitors.
21. A tank circuit has an inductance $L_P = 0.25$ mH. calculate the range of capacitors when the tuning frequency range is 400 kHz to 1200 kHz.
22. In a Colpitts oscillator, the value of capacitors are $C_1 = 0.20$ pF and $C_2 = 0.020$ pF the inductance of coils are $L_1 = 0.5$ mH. Calculate the frequency of oscillations and the required gain for oscillation.
23. In a Colpitts oscillator, the value of capacitors are $C_1 = 0.125$ μF and $C_2 = 0.020$ μF the inductance of coil is $L_1 = 0.5$ mH.
    (a) Find the frequency of oscillation.
    (b) If the frequency of the oscillation is 15 Hz, find the value of inductance of coil and also determine the voltage gain of oscillator.
24. In a Colpitts oscillator, the values of capacitors and coil inductance are $C_1 = 0.5$ μF and $C_2 = 3.0$ μF and $L_1 = 0.5$ mH.
    (a) When the output voltage is 12 V, calculate the feedback voltage.
    (b) What is the frequency of oscillation?
25. In a Hartley oscillator, $L_1 = 0.025$ mH and $C = 0.047$ μF. When the frequency of the oscillator is 150 kHz, determine the value of L_2. Assume mutual inductance is negligible.

26. The frequency of a transistorised Hartley oscillator can be varied from 50 kHz to 100 kHz. The tuning capacitor can changed from 100 pF to 200 pF. Determine the values of inductances. Assume $h_{fe} = 50$ and $\Delta_{he} = 0.1$.
27. A Hartley oscillator uses a tank *C*ircuit with $L_1 = 0.5$ mH, $L_2 = 0.3$ mH and $C = 0.01$ μF. What is the frequency of oscillator? Assume mutual inductance is negligible.
28. In a Hartley oscillator, $L_2 = 0.25$ mH and $C = 0.047$ μF. When the frequency of the oscillator is 125 kHz, determine the value of L_1. Assume mutual inductance is negligible.
29. In a transistorised Hartley oscillator $L_1 = 0.5$ mH, $L_2 = 0.5$ μH while the frequency has been changed from 50 kHz to 500 kHz. Determine the range of capacitor. Assume mutual inductance is negligible.
30. In a Hartley oscillator, the value of the capacitor is 200 pF and the inductance of coils are $L_1 = 0.5$ mH, $L_2 = 0.025$ mH. calculate the frequency of oscillations and the feedback factor. Assume mutual inductance is negligible.
31. In a crystal oscillator, the value of inductance $L = 0.20$ H, capacitor $C_S = 0.047$ pF, capacitor $C_P = 4.77$ pF, and $R = 5.7$k. Determine the series resonant frequency, parallel resonant frequency and *Q*-factor of the crystal.
32. Draw the circuit diagram of a crystal oscillator and explain its operating principle. Derive the frequency of oscillation of a crystal oscillator. What are the advantages of crystal oscillators?
33. (a) What is the basic principle of oscillators?
    (b) Is an external input signal necessary for the output of an oscillator? If not, how are oscillations initiated.
    (c) Explain with a circuit diagram the action of a Wien-Bridge oscillator. Find an expression for the frequency of oscillator.
34. Write the short notes on the following:
    (a) Crystal oscillator
    (b) Tuned LC oscillator
    (c) Wein-bridge oscillator
    (d) Barkhausen criterion
35. Draw and explain the operation of Hartley oscillator.
36. Write down the Barkhausen criterion for sinusoidal oscillation. Obtain expression for output frequency and condition to sustain oscillation of a *R–C* phase shift oscillator.

ANSWERS

Multiple-Choice Questions

1. (c)	2. (b)	3. (a)	4. (a)	5. (a)	6. (a)	7. (a)
8. (a)	9. (a)	10. (a)	11. (a)	12. (b)	13. (a)	14. (a)
15. (a)	16. (a)	17. (b)	18. (a)			

CHAPTER

6

Operational Amplifier

6.1 INTRODUCTION

Commonly used semiconductor (solid state) devices are transistors (BJTs), diodes and FETs. Any electronic circuit is formed when solid-state devices or components are interconnected. This circuit is known as *discrete circuit*. In this circuit, components are separable. An *integrated circuit* (IC), is a semiconductor wafer on which thousands or millions of tiny resistors, capacitors, diodes and transistors are fabricated. Sometimes, an IC is called a *chip* or microchip. The first integrated circuit was developed in the 1950s by Jack Kilby of Texas Instruments and Robert Noyce of Fairchild Semiconductor. An IC can function as an amplifier, oscillator, gate, flip-flop, timer, counter, computer memory, or microprocessor etc. Depending on applications and type of signal process, ICs are categorised as

1. *Linear* (analog) ICs
2. *Digital* ICs

Based on application requirements, two distinctly different IC technologies such as monolithic technology and hybrid technology have been developed.

In *Monolithic ICs*, all active and passive elements of any electronic circuit such as resistors, capacitors, diodes and transistors, and their interconnections, are manufactured into a single chip of silicon. When identical circuits are required in very large quantities, monolithic ICs are manufactured at very low cost and high reliability.

In *hybrid ICs*, separate components are attached to a ceramic substrate and interconnected by wire or metallisation pattern. Depending upon the active devices used in ICs, they can be classified as bipolar ICs using BJT and unipolar ICs using FET. Figure 6.1 shows the classification of ICs.

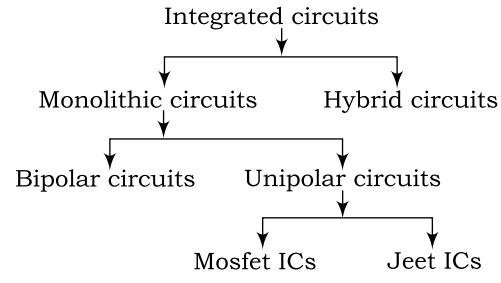


Fig. 6.1 Classification of ICs

The integrated circuits have a number of distinct advantages over discrete circuits. The advantages of ICs are as follows:

1. Its size is small. Due to miniaturisation, the density of components is increased. It is possible to incorporate about 20,000 components per square inch in it.

2. Improved performance as complex circuits are fabricated for better performance.
3. Low cost due to batch processing.
4. Reliability is high.
5. Less power consumption.
6. Higher operating speed due to absence of parasitic capacitance effect.
7. Matched devices.
8. Less weight.
9. Easy replacement.

Limitations of ICs

The integrated circuits has the following limitations

1. Due to small size, ICs are unable to dissipate a large amount of power. If the current flow in the IC is increased, more heat will be generated in it and the device may get damaged.
2. Inductance and transformers cannot be incorporated in IC.

The integration of solid-state technology has been progressed day by day. Based on level of integration, integrated circuits are often classified by the number of transistors and other electronic components they contain. The ICs are classified as SSI (small-scale integration), MSI (medium-scale integration), LSI (large-scale integration), VLSI (very large-scale integration) and ULSI (ultra large-scale integration). SSI chips have up to 100 transistors per chip, MSI chips have 100 to 1000, LSI chips have 1000 to 20,000, VLSI chips have 20,000 to 1000,000, and ULSI chips have up to 10^6 to 10^7 transistors per chip. Table 6.1 shows the different types of ICs with their applications.

Table 6.1 Types of Integrated circuits

Type of ICs	*SSI*	*MSI*	*LSI*	*VLSI*	*ULSI*
No. of transistors	Up to 100 transistors per chip	100 to 1000 transistors per chip	1000 to 20,000 transistors per chip	20,000 to 1000,000 transistors per chip	10^6 to 10^7 transistors per chip
No. of gates	Up to 30 gates per chip	30 to 300 gates per chip	300 to 3000 gates per chip	More than 3000 gates per chip	
Applications	Logic gates, flip-flops	Adders, Multiplexers, Counters	RAM, ROM, 8-bit microprocessor	16-bit and 32-bit microprocessor	Special processors, Smart sensors
Year of Development	1960–65	1965–70	1970–80	1980–90	1990–2000

ICs are also classified as linear ICs and digital ICs based on the type of signals. *Linear (analog) ICs* operate on continuous or analog signals and output signal is also continuous depending on the input signal level. Therefore, the output signal level is a linear function of the input signal level in linear ICs. Linear ICs are most commonly used as audio-frequency (AF) and radio-frequency (RF) amplifiers. The examples of linear ICs are OP-AMP, voltage regulators, comparators, and timers.

Digital ICs operate on discrete signals. The fundamental building blocks of digital ICs are logic gates, which work with binary data, either 0 V (logic 0) or +5 V (logic 1). Digital, or *discrete ICs*, are used in logic gates, flip-flops, counters, memory, microprocessors, computers, computer networks and modems.

The *operational amplifier* (OP-AMP) is a common device in audio-frequency (AF) and radio-frequency (RF) amplifiers applications. In this chapter, operation of OP-AMPs, symbol, equivalent circuit, voltage transfer curve, internal circuit diagram, and specification of OP-AMPs, differential amplifier, constant

current source, current mirror, level shifters, CMRR, open and closed loop circuits, importance of feedback loop (positive and negative), inverting and non-inverting amplifiers and voltage follower/Buffer circuits are explained in detail.

6.2 THE IDEAL OP-AMP

An ideal OP-AMP would exhibit the following characteristics:

1. Infinite open-loop voltage gain $A = \infty$
2. Infinite input resistance, $R_i = \infty$. Therefore, any input signal can drive it and there is no-loading on the preceding stage.
3. Zero output resistance $R_o = 0$. Therefore, the output can drive an infinite number of the devices.
4. Infinite bandwidth, $BW = \infty$. Therefore, any frequency signal from 0 to ∞ Hz can be amplified without attenuation.
5. Infinite common-mode rejection ratio, $CMRR = \infty$. Therefore, output common-mode noise voltage is zero.
6. Infinite slew rate, $SR = \infty$. Therefore, output voltage changes occurs simultaneously with input voltage changes.

In practice, the above characteristics of OP-AMPs can never be realised. An ideal OP-AMP simplifies the mathematical representation of any OP-AMP circuit. The practical OP-AMP can be made close to ideal values as given in Table 6.2.

Table 6.2 Characteristics of OP-AMPs

Property	*Ideal*	*Practical*	*Typical Value*
Open-loop gain	Infinite	Very high	2×10^5
Input resistance	Infinite	High	2 MΩ
Output resistance	Zero	Low	75 Ω
CMMR	Infinite	High	90 dB
Bandwidth	Infinite	Very high	Dominant pole 10 Hz

6.3 EQUIVALENT CIRCUIT OF AN OP-AMP

An equivalent circuit of an OP-AMP with finite input and out resistances is shown in Fig. 6.2. This circuit incorporates important values such as A, R_i, and R_o from manufacturer's data sheet.

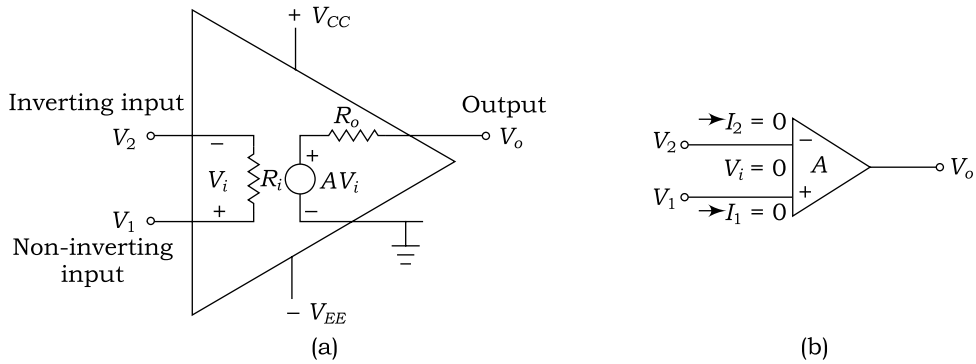


Fig. 6.2 Equivalent circuit of an OP-AMP

In this figure,

AV_i is the Thevenin's equivalent voltage source,

R_o is the Thevenin's equivalent resistance looking from the output terminal of an OP-AMP,

V_i is difference input voltage, R_i is input resistance, V_O is output voltage,

V_1 is voltage at non-inverting terminal with respect to ground, and

V_2 is voltage at inverting terminal with respect to ground.

Assuming OP-AMP characteristics are close to the ideal characteristics, the following conditions prevail at the input side of the OP-AMP.

- As $R_i = \infty$, current input into inverting and non-inverting terminals is approximately zero as shown in Fig. 6.2(a)
- As $A = \infty$, for any finite output voltage V_o, $V_i = V_- - V_+ = 0$. Hence, the inverting and non-inverting terminals should have the same potential.

The output voltage V_o can be expressed as

$$V_o = AV_i = A\left(V_1 - V_2\right)$$

Therefore, the output voltage V_o is directly proportional to the difference between two input voltages V_1 and V_2 or the operational amplifier amplifies the difference between two input voltages. The polarity of output voltage depends on the polarity of the difference voltage, $V_1 - V_2$.

6.4 IDEAL VOLTAGE TRANSFER CURVE

The basic OP-AMP equation $V_o = AV_i$ is justified when the output off-set voltage is assumed to be zero. This equation is very useful to study the OP-AMP characteristics and to analyse different circuit configurations that employ feedback. Figure 6.3 shows the graphical representation of the equation, where x-axis represents input difference voltage V_i and y-axis represents output voltage V_o and gain A is constant.

It is clear from Fig. 6.3 that the output voltage cannot exceed the positive saturation voltage $+V_{sat}$ and negative saturation voltage $-V_{sat}$. The $+V_{sat}$ and $-V_{sat}$ voltages are specified by an output voltage swing rating of the OP-AMP for given values of supply voltages. Therefore, the output voltage is directly proportional to V_i only when it reaches the saturation voltage, and thereafter output voltage is constant (either $+V_{sat}$ or $-V_{sat}$), depending upon the magnitude of V_i.

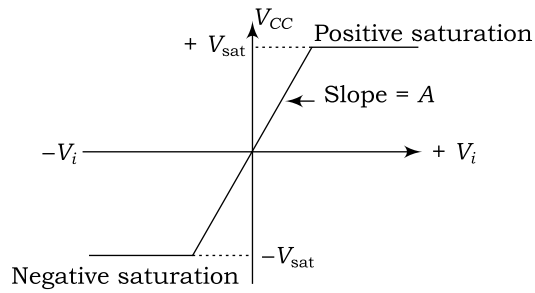


Fig. 6.3 Voltage transfer curve

Figure 6.3 is called an *ideal voltage transfer curve* as output offset voltage V_o is assumed to be zero. In a negative feedback OP-AMP circuit, this voltage is approximately zero. This figure is not drawn according to scale. If it is drawn as per scale, considering the very high value of A, the curve would be almost vertical.

6.5 OP-AMP SYMBOL AND TERMINALS

Figure 6.4 shows the symbol of an operational amplifier. The pin diagram of an OP-AMP is depicted in Fig. 6.5(a). It is available in dual in-line plastic package as shown in Fig. 6.5(b). Usually, it is indicated by a triangle with basic five terminals as follows:

- Positive supply voltage terminal, $+V_{CC}$ (7)

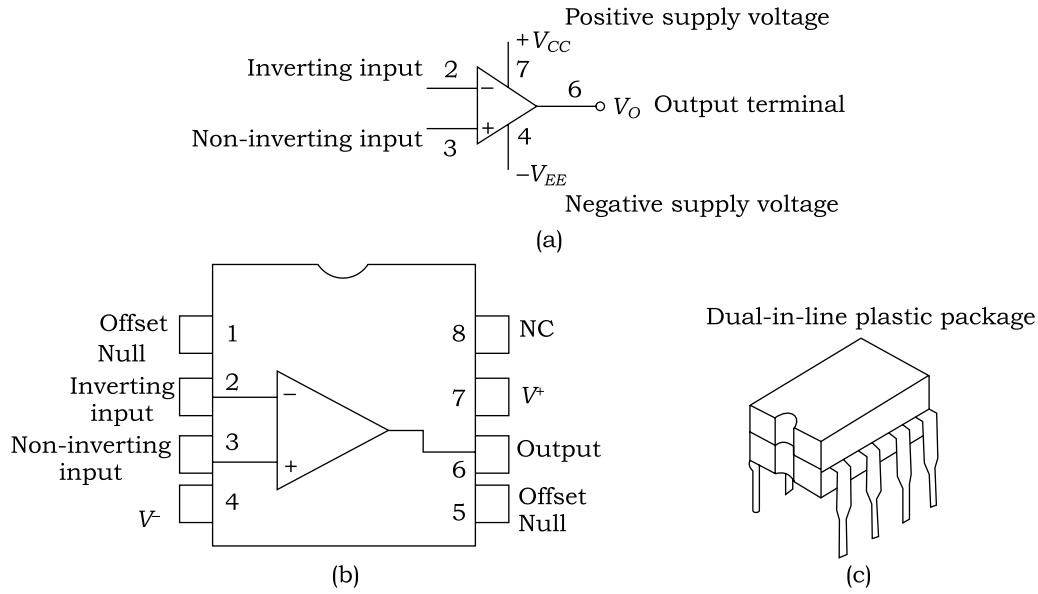


Fig. 6.4 (a) Symbol of OP-AMP (b) Pin diagram of OP-AMP in mini DIP (c) Dual in-line plastic package of OP-AMP

- Negative supply voltage terminal, $+V_{EE}$ (4)
- Output terminal voltage, V_O (6)
- Inverting input terminal (2)
- Non-inverting input terminal (3).

and other terminals are terminal (1) and terminal (5) which are used as null offset. The terminal (8) is used as NC (no connection).

6.6 THE PACKAGE STYLE AND PIN-OUTS

IC741 is commercially available in three types of packages such as metal package, dual-in-line package (DIP) and flat package. The OP-AMP packages contain single or dual (two) or quad (four) OP-AMP in a single IC. Usually, DIP and metal can packages have 8 terminals. Flat pack and DIP packages have 10 or 14 terminals. The most commonly used single OP-AMP IC741 is 8-pin metal can package, 8-pin DIP and 14-pin DIP. IC μA 747 is dual 741, which is available either in 10-pin metal can package or 14 pin DIP. OP-11 is a quad 741, which is available in 14-pin DIP package. Figure 6.5 shows different 741 package style and pin-outs.

6.7 DIFFERENCE AMPLIFIER

Figure 6.6 shows a *difference amplifier* where V_1 and V_2 are voltage inputs and V_o is the output voltage. Assuming that it is formed by a linear active device,it is an ideal one for the analysis of a difference amplifier. A difference amplifier can be defined as an ideal one if any signal, which is common to both inputs, has no effect on the output voltage.

The output voltage of a difference amplifier is

$$V_O = A_d\left(V_1 - V_2\right)$$

where, A_d is the gain of the difference amplifier.

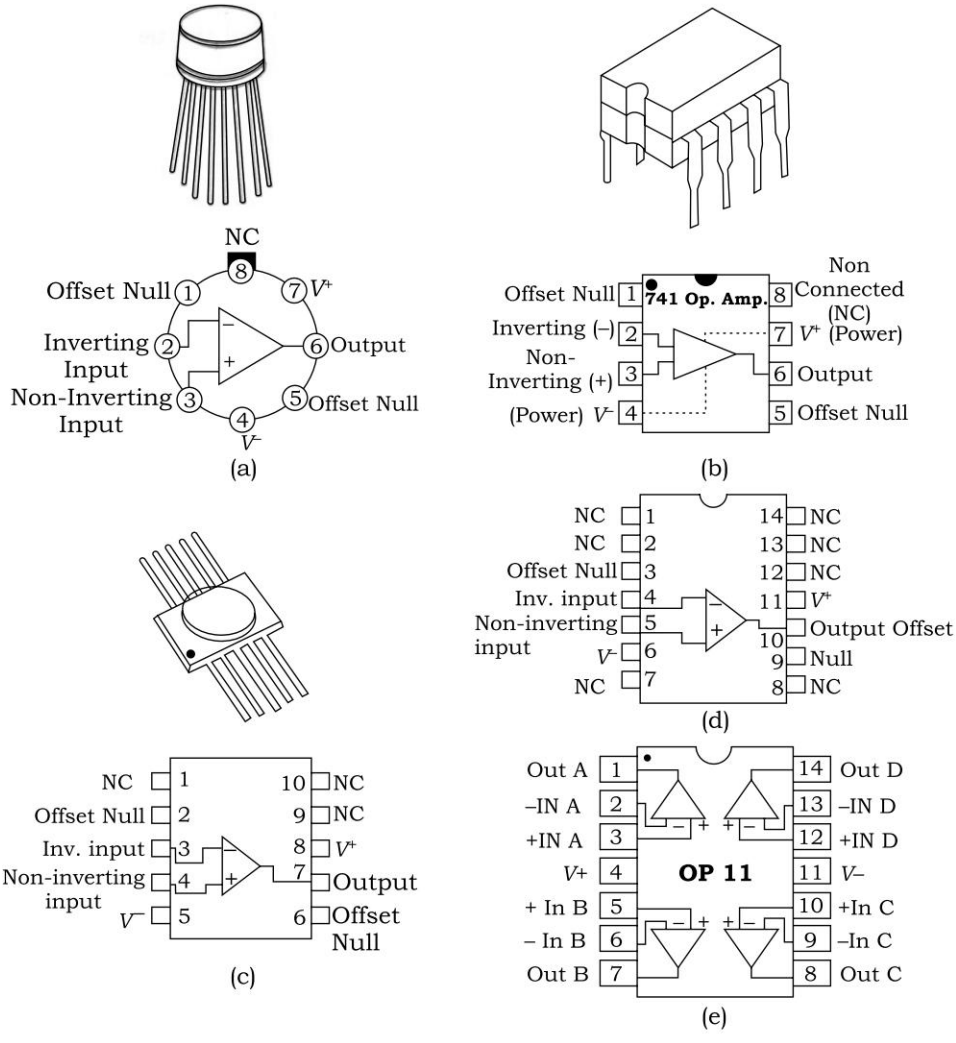


Fig. 6.5 (a) 8-pin metal can package (b) 8-pin dual-in-line package (c) 10-pin flat pack of a single OP-AMP (d)14-pin DIP of a single OP-AMP (e) quad OP-AMP.

If input voltage V_1 = input voltage V_2, then output voltage $V_o = 0$. Actually, the signal common to both inputs gets cancelled and generates zero output voltage. This is only possible for an ideal operational amplifier. But the practical difference amplifier does not follow the above equation as the output voltage depends not only upon the difference signal V_d but also depends upon the average voltage of the input signals V_c, which is called the common-mode signal. For example, the output voltage V_o with input voltages $V_1 = 200\ \mu V$ and $V_2 = 100\ \mu V$ will be different from the output voltage V_o with input voltages $V_1 = 1000\ \mu V$ and $V_2 = 900\ \mu V$, even though the difference signal $(V_1 - V_2) = 100\ \mu V$.

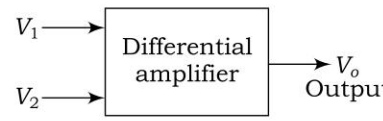


Fig. 6.6 Difference amplifier

The common-mode signal is $V_C = \dfrac{V_1 + V_2}{2}$

In any differential amplifier, the circuit is symmetric, but due to parameter mismatch, the gain at the output with respect to the positive terminal is different in magnitude to that of the negative terminal. Therefore, if the same voltage is applied to both terminals, the output is not zero.

Then output voltage can be expressed as

$$V_O = A_1 V_1 + A_2 V_2 \tag{6.1}$$

where, V_1 is amplified by A_1 and V_2 is amplified by A_2

At that moment, $2V_C = V_1 + V_2$, and $V_d = V_1 - V_2$

Then $2V_C + V_d = 2V_1$

or $$V_1 = V_C + \frac{1}{2}V_d \tag{6.2}$$

The input voltage is $V_2 = V_1 - V_d$

$$= V_C + \frac{1}{2}V_d - V_d = V_C - \frac{1}{2}V_d \tag{6.3}$$

The output voltage is $V_O = A_1 V_1 + A_2 V_2$

$$= A_1\left(V_C + \frac{V_d}{2}\right) + A_2\left(V_C - \frac{V_d}{2}\right)$$

$$= (A_1 + A_2)V_C + \frac{A_1 - A_2}{2}V_d$$

$$= A_C V_C + A_d V_d \tag{6.4}$$

where, common-mode gain $A_C = A_1 + A_2$, and

differential mode gain $A_d = \dfrac{A_1 - A_2}{2}$

6.7.1 Common-mode Rejection Ratio

The relative sensitivity of an operational amplifier to a difference signal as compared to a common-mode signal is known as Common-Mode Rejection Ratio (CMRR). CMRR can be defined as the ratio of the differential voltage gain A_d to common-mode voltage gain A_c. It can be expressed as

$$CMRR = \rho = \left|\frac{A_d}{A_C}\right|$$

Usually, *CMRR* is expressed in decibels (dB) as $CMRR = 20\log\left|\dfrac{A_d}{A_C}\right|$ dB

The output voltage can be expressed in terms of *CMRR* is

$$V_O = A_d V_d + A_C V_C$$

$$= A_d V_d\left(1 + \frac{A_C V_C}{A_d V_d}\right)$$

$$= A_d V_d\left(1 + \frac{1}{\dfrac{A_d}{A_c}}\frac{V_C}{V_d}\right) \qquad \text{as } CMRR = \frac{A_d}{A_c} = \rho$$

$$= A_d V_d \left(1 + \frac{1}{CMRR}\frac{V_C}{V_d}\right)$$

$$= A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right) \tag{6.5}$$

It is clear from the above equation that ρ must be large compared to the ratio of the common-mode signal to the difference-mode signal, as there is always some noise signals on the signal lines. In addition, it is undesirable that the amplification of noise signal will be present in the output signal. The differential amplifier can virtually eliminate the noise signal.

Example 6.1 Calculate the common-mode gain of an operational amplifier for the following parameters: the differential voltage gain $A_d = 10^4$, and common-mode rejection ratio $CMRR = 2000$.

Sol. Given $A_d = 10^4$ and $CMRR = 2000$.

The common-mode rejection ratio ($CMRR$) can be expressed as

$$CMRR = \rho = \left|\frac{A_d}{A_C}\right|$$

Then common-mode gain $A_C = \dfrac{A_d}{CMRR} = \dfrac{10^4}{2000} = 5.$

Example 6.2 Calculate the output voltage of a differential amplifier for the following parameters: $V_1 = 1000\ \mu V$, $V_2 = 500\ \mu V$, $A_d = 1000$ and $\rho = CMRR = 2000$

Sol. Given: $V_1 = 1000\ \mu V$, $V_2 = 500\ \mu V$, $A_d = 1000$, $\rho = CMRR = 2000$

The common-mode signal is

$$V_C = \frac{V_1 + V_2}{2} = \frac{1000 + 500}{2}\ \mu V = 750\ \mu V$$

The difference signal V_d is

$$V_d = V_1 - V_2 = (1000 - 500)\ \mu V = 500\ \mu V$$

The output voltage is

$$V_O = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$$

$$= 1000 \times 500 \times 10^{-6}\left(1 + \frac{1}{2000}\frac{750}{500}\right) = 500.375\ \text{mV}$$

Example 6.3 The common-mode rejection ratio $CMRR$ of an operational amplifier is about 120 dB and difference-mode voltage gain is 10,000. Determine common-mode gain.

Sol. Given $A_d = 10{,}000$, $CMRR = 120$ dB

The common-mode rejection ratio ($CMRR$) in dB can be expressed as

$$CMRR = 20\log\frac{A_d}{A_C} = 20(\log A_d - \log A_C)$$

$$= 20\log 10000 - 20\log A_C$$

$$= 80 - 20\log A_C = 120$$

Therefore, 20 log A_C = 120 – 80 = 40 dB

The common-mode gain is

$$A_C = \text{Antilog}\left(\frac{40}{20}\right) = 100$$

Example 6.4 The input signals of a differential amplifier are V_1 = 50 μV and V_2 = –25 μV.

(a) When the common-mode rejection ratio is 50, determine the output voltage of differential amplifier.

(b) If ρ = 10,000, find the output voltage.

Assume difference-mode gain A_d = 20,000

Sol. Given V_1 = 50 μV, V_2 = –25 μV and common-mode rejection ratio *CMRR* = 50

(a) The common-mode signal is

$$V_C = \frac{V_1 + V_2}{2} = \frac{50 - 25}{2}\,\mu\text{V} = 12.5\,\mu\text{V}$$

The difference signal is

$$V_d = V_1 - V_2 = 50 - (-25)\,\mu\text{V} = 75\,\mu\text{V}$$

The output voltage is

$$V_O = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$$

$$= 20000 \times 75 \times 10^{-6}\left(1 + \frac{1}{50}\frac{12.5}{75}\right) = 1505\ \text{mV}$$

(b) If ρ = 10,000, the output voltage is

$$V_O = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$$

$$= 20000 \times 75 \times 10^{-6}\left(1 + \frac{1}{10000}\frac{12.5}{75}\right) = 1500.025\ \text{mV}$$

Example 6.5 In a differential amplifier, the input voltages are

$$V_1 = 10\sin(2\pi \times 25t) + 5\sin(2\pi \times 1000t)\ \text{mV},\ \text{and}$$

$$V_2 = 10\sin(2\pi \times 25t) - 5\sin(2\pi \times 1000t)\ \text{mV}$$

The common-mode gain A_C = 0.5 and difference-mode gain A_d = 100. Determine (a) V_{O1}, (b) V_{O2}, and (c)V_O. Assume 25 Hz signal is a noise signal and 1000 Hz frequency signal will be processed.

Sol.

(a) The common-mode signal is

$$V_C = \frac{V_1 + V_2}{2} = 10\sin(2\pi \times 25t)\ \text{mV}$$

The difference signal is

$$V_d = V_1 - V_2 = 10\sin(2\pi \times 1000t)\ \text{mV}$$

The output voltage is

$$V_{O1} = A_d V_d + A_C V_C$$
$$= 100 \times 10\sin(2\pi \times 1000t) + 0.5 \times 10\sin(2\pi \times 25t)\ \text{mV}$$

(b) The output voltage is

$$V_{O2} = -A_d V_d + A_C V_C$$
$$= -100 \times 10\sin(2\pi \times 1000t) + 0.5 \times 10\sin(2\pi \times 25t)\ \text{mV}$$

(c) The output voltage is

$$V_O = V_{O1} - V_{O2}$$
$$= 2 \times 100 \times 10\sin(2\pi \times 1000t)\ \text{mV}$$
$$= 2\sin(2\pi \times 1000t)\ \text{V}$$

6.8 OPERATIONAL AMPLIFIER INTERNAL CIRCUIT

The block diagram of a typical operational amplifier is shown in Fig. 6.7. Usually, operational amplifier consists of four cascaded blocks. The first two stages are cascaded differential amplifiers, which are used to provide high gain and high input resistance. The third stage works as a buffer as well as a level shifter. Actually, the buffer is an emitter-follower. Its input impedance is very high. Hence, it prevents loading of the high gain stage. The level shifter adjusts the dc voltages and the output voltage is zero for zero inputs. As the gain stages are direct-coupled, the adjustment of dc level is required.

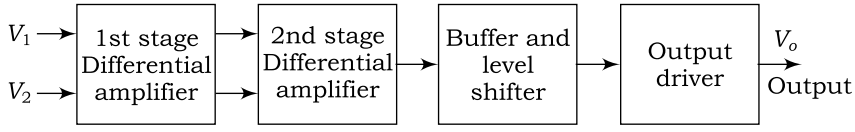


Fig. 6.7 Block-diagram representation of OP-AMP internal circuit

The output is used to provide low output impedance as demanded by the ideal characteristics of OP-AMP. The output voltage should swing symmetrically, in between $+V_{sat}$ and $-V_{sat}$. For this swing, the amplifier is provided with positive and negative supply voltages (±15 V).

In the first stage differential amplifier, there are two inputs and balanced differential output. In this stage, maximum voltage gain is provided and very high input impedance of operational amplifier is also established. This stage should have the following characteristics:

- Very high input impedance, about 10 MΩ
- High CMRR, about 120 dB
- Very high open-loop gain, about 10^5
- Low input bias current, about 0.5 μA
- Small input offset current, about 0.2 mA
- Small input offset voltage, about 10 mV

In the second-stage differential amplifier, there are two inputs and unbalanced output differential amplifier. In this stage, the overall gain of operational amplifier increases. Due to direct coupling between first-stage

and second-stage differential amplifiers, the dc level at the output of the second-stage differential amplifier is much higher than the ground potential. Consequently, a level translator must be used in the next stage in order to bring the dc level back to the ground potential.

Generally, the third-stage OP-AMP internal circuit is buffer and level shifter. This stage is used to shift the dc level to zero volts with respect to ground. Usually, the emitter-follower circuit is in this stage to provide low output resistance, and Class B and Class AB amplifiers are used to provide large output power. The last stage is output driver circuit. In this stage, a complementary symmetry push-pull amplifier is used. The output stage should have the following characteristics:

- Low output impedance
- Large output voltage swing capability
- Large output current swing capability
- Short-circuit protection

Figure 6.8 shows the schematic circuit diagram of a 741 OP-AMP, which consists of a differential amplifier, current mirrors, Class A gain stage, voltage level shifter and output stage.

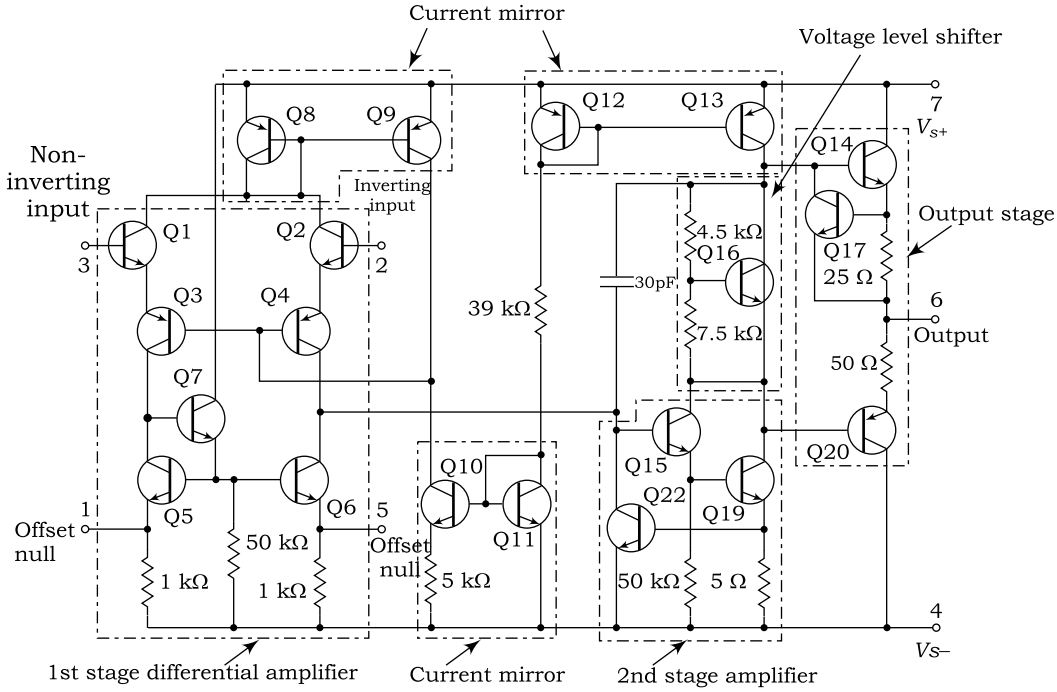


Fig. 6.8 Internal circuit diagram of 741 OP-AMP

1. Differential Amplifier

The input stage is a composed differential amplifier with a complex biasing circuit and a current mirror active load. The input stage differential amplifier contains transistors $Q1$-$Q3$ and $Q2$-$Q4$. Transistors $Q1$-$Q3$ and $Q2$-$Q4$ are connected in *CE-CB* (cascode) configuration. $Q1$ feeds $Q3$ and Transistors $Q1$-$Q3$ are connected in series to provide high voltage gain. Transistors $Q5$, $Q6$, $Q7$ are used as active load for $Q3$ and $Q4$. $Q5$ and $Q6$ operate as a differential amplifier for external offset null signal and the emitter current is controlled by external potentiometer.

2. Class A Gain Stage

Input-stage bias currents are provided by current mirror pairs. $Q12$ generates a current in $Q11$ and this current is reflected in $Q10$. The current in $Q10$ generates a series current in $Q9$ and it is reflected in the mirror pair $Q8$. Hence, the bias current of $Q3$ and $Q4$ is driven by the mirror pair $Q10$ and $Q11$. The output of the first differential amplifier is taken from the junction of $Q4$ (Point A) and $Q6$ (Point B). The output is directly proportional to the differential input signal. After that, this output signal is now amplified by the second stage, where transistors $Q15$ and $Q19$ are connected as Darlington amplifiers. This is known as Class A gain stage.

The top-right current mirror $Q12/Q13$ supplies this stage by a constant current load through the collector of $Q13$, which is independent of the output voltage. The Class A gain stage uses the output side of a current mirror as its collector load to achieve high gain. Transistor $Q22$ is used to prevent this stage from saturating by diverting the excessive $Q15$ base current.

3. Voltage-Level Shifter

Transistor $Q16$ is used as a voltage-level shifter. In the circuit, $Q16$ provides a constant voltage drop across its collector-emitter junction regardless of the current through it and it acts as a voltage stabiliser. This is achieved by introducing a negative feedback between $Q16$ collector and its base.

4. Output Stage

The output stage is a Class AB push-pull emitter-follower amplifier which is formed by $Q14$ and $Q20$. This stage is effectively driven by the collectors of $Q13$ and $Q19$.

6.8.1 Differential Amplifier

The differential amplifier stages are used to provide high gain in the difference mode signal and cancel the common-mode signal. The *CMRR* common-mode rejection ratio is the relative sensitivity of an OP-AMP to a difference signal as compared to common-mode signal. The *CMRR* is the advantage of the differential amplifier. If the *CMRR* value is very high, it is better for OP-AMP. An OP-AMP should have high input impedance.

A cascade dc amplifier can provide high gain down to zero frequency due to absence of coupling capacitor. However, this amplifier suffers from the drift of the operating point due to temperature dependency of I_{CBO}, V_{BE} and $\underline{h_{fe}}$ of transistors. This problem can be reduced by using differential amplifiers as depicted in Fig. 6.9. This is an emitter-coupled differential amplifier. Its circuit has low drift due to symmetrical construction and can be designed in such a way that it provides high input resistance.

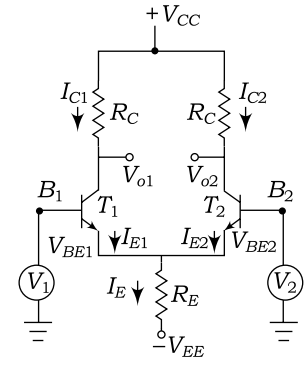


Fig. 6.9 Basic differential amplifier

It has two input terminals, B_1 and B_2. B_2 is the inverting terminal and B_1 is non-inverting terminal. This amplifier can be used in four different configurations depending upon the input and output signals. These four different configurations are

1. Differential input and differential output
2. Differential input and single ended output
3. Single input and differential output
4. Single input and single-ended output

When a signal is applied to both the inputs, it is differential input and differences of signals applied to the two inputs are amplified.

Assume transistor bases B_1 and B_2 are joined together and connected to a voltage V_C called the common-mode voltage. It is clear from Fig. 6.10, $V_1 = V_2 = V_C$. Transistors T_1 and T_2 are well matched and due to symmetry of the circuit, the current I_E divides equally through transistors T_1 and T_2. Therefore, the emitter current of T_1 is equal to emitter current of T_2.

Hence, $I_{E1} = I_{E2} = \frac{I_E}{2}$

The collector currents I_{C1} and I_{C2} that flow through the resistor R_C is $\alpha\frac{I_E}{2}$.

The voltage at each of the collectors will be

$$V_{CC} - \alpha\frac{I_E}{2}R_C$$

and the difference of the voltage between the two collectors $V_{o1} - V_{o2}$ will be zero.

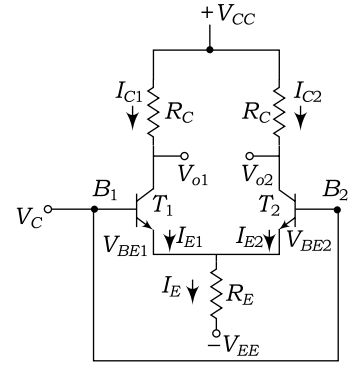


Fig. 6.10 Differential pair with a common-mode input signal V_C

If the value of V_C is changed, the output voltage across the two collectors will not be changed. Consequently, the differential pair will not respond to the common-mode input signals.

When the input voltage $V_2 = 0$ and input voltage $V_1 = 1$ V, Transistor T_1 will be ON and Transistor T_2 will be OFF as depicted in Fig. 6.11. Then, the total current I_E will flow through T_1. As T_1 is ON, the voltage at emitter will be 0.3 V. As a result, the emitter-base junction of T_2 will be reversed biased and T_2 becomes OFF. The collector voltage of T_1 is V_{O1} will be $V_{o1} = V_{CC} - \alpha I_E R_C$ and collector voltage of T_2 is $V_{O2} = V_{CC}$. Therefore, it is clear from the above discussion that the differential pair only responds to difference-mode signals and rejects common-mode signals.

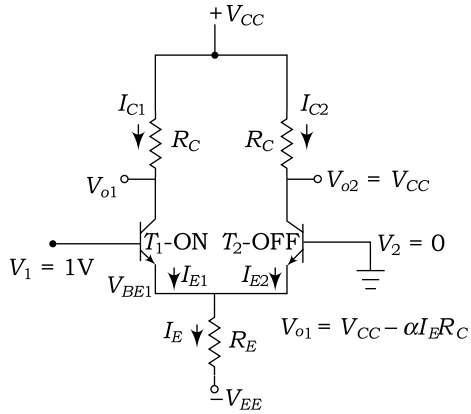


Fig. 6.11 Differential pair with large differential input signal V_C

Transfer Characteristics of Differential Amplifier

The collector currents for transistors T_1 and T_2 are I_{C1} and I_{C2} respectively. After neglecting the reverse saturation currents of the collector base junction, we obtain

The collector current for transistor T_1 is $I_{C1} = \alpha I_{ES} e^{\frac{V_{BE1}}{V_T}}$

The collector current for transistor T_2 is $I_{C2} = \alpha I_{ES} e^{\frac{V_{BE2}}{V_T}}$

where, I_{ES} is the reverse saturation current of emitter-base junction.

The ratio of two collector currents is

$$\frac{I_{C1}}{I_{C2}} = \frac{\alpha I_{ES} e^{\frac{V_{BE1}}{V_T}}}{\alpha I_{ES} e^{\frac{V_{BE2}}{V_T}}} = e^{\frac{V_{BE1} - V_{BE2}}{V_T}} \quad (6.6)$$

KVL for loop equation for two emitter-base junctions is

$$V_1 - V_{BE1} + V_{BE2} - V_2 = 0$$

or $$V_{BE1} - V_{BE2} = V_1 - V_2 = V_d$$

where, V_d is the difference of two input voltages.

The emitter current I_E is

$$\begin{aligned} I_E &= I_{E1} + I_{E2} \\ &= \frac{I_{C1}}{\alpha} + \frac{I_{C2}}{\alpha} \\ &= \frac{I_{C1}}{\alpha}\left(1 + \frac{I_{C2}}{I_{C1}}\right) \\ &= \frac{I_{C1}}{\alpha}\left(1 + e^{-\frac{V_d}{V_T}}\right) \end{aligned} \tag{6.7}$$

Therefore, $$I_{C1} = \frac{\alpha I_E}{1 + e^{-\frac{V_d}{V_T}}} \quad \text{and} \quad I_{C2} = \frac{\alpha I_E}{1 + e^{\frac{V_d}{V_T}}} \tag{6.8}$$

The transfer characteristics for a difference amplifier (I_C vs V_d plot) is illustrated in Fig. 6.12. The following is clear from the transfer characteristics as depicted Fig. 6.12:

1. If $V_d > 4V_T$ about 100 mV, $I_{C1} = \alpha I_E$ and $I_{C2} = 0$. Then output voltages are $V_{O1} = V_{CC} - \alpha I_E R_C$ and $V_{O2} = V_{CC}$
2. If $V_d < -4V_T$ about –100 mV, $I_{C1} = 0$ and $I_{C2} = \alpha I_E$. The output voltage $V_{O1} = V_{CC}$ and V_{O2} is very small or negligible. Therefore, during $-4V_T < V_d < 4V_T$ the differential amplifier can acts as switch.
3. When $V_d > \pm 4V_T$, the differential amplifier can acts as a very good limiter.
4. $-2V_T < V_d < 2V_T$, difference amplifier can function as linear amplifier.

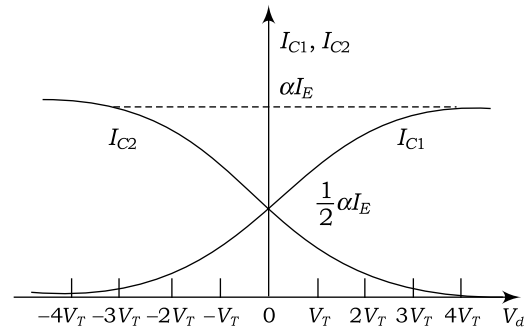


Fig. 6.12 Transfer characteristics for difference amplifier

Example 6.6 The difference amplifier as shown in Fig. 6.13 has the following parameters:

$$R_C = 10\ \text{k}\Omega,\ R_E = 100\ \text{k}\Omega,\ R_S = 10\ \text{k}\Omega$$

The transistor parameters are as follows:

$$h_{ie} = 10\ \text{k}\Omega,\ h_{fe} = 100,\ h_{re} = 0,\ h_{oe} = 0$$

When an amplifier is operated with common-mode signal of 50 mV and difference signal of 25 mV, determine output voltage and *CMRR*.

Sol. The difference gain is

$$\begin{aligned} A_d &= -\frac{h_{fe} R_C}{2(R_S + h_{ie})} \\ &= -\frac{100 \times 100\text{k-ohm}}{2(10\text{k-ohm} + 10\text{k-ohm})} = -250 \end{aligned}$$

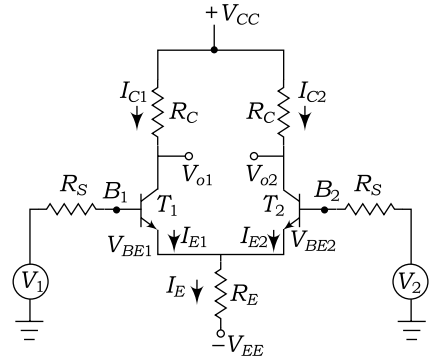


Fig. 6.13 Difference amplifier

The common-mode gain is

$$A_C = -\frac{h_{fe}R_C}{R_S + h_{ie} + (1 + h_{fe})\,2R_E}$$

$$= -\frac{100 \times 10\text{k-ohm}}{10\text{k-ohm} + 10\text{k-ohm} + (1+100) \times 2 \times 100\text{k-ohm}} = -0.049$$

The output voltage is

$$V_O = A_d V_d + A_C V_C$$

$$= (-250) \times 25\text{ mV} + (-0.049) \times 50\text{ mV} = 6252.45\text{ mV}$$

The common-mode rejection ratio in dB is

$$CMRR = 20\log\frac{A_d}{A_C} = 20\log\frac{250}{0.049} = 74.15\text{ dB}$$

6.8.2 Low Frequency Small Signal Analysis of Differential Amplifiers

Figure 6.14 shows a dual input differential amplifier which is used to amplify only differential signal at the two input signals and can reject the common signal of the two input signals. Since transistor T_1 and T_2 are similar rating, their parameters are matched, only unwanted signal like noise to both inputs should be rejected. But practically transistor T_1 and T_2 are not equally matched and there is an output even though same voltage is applied to the input terminals. Then we can find the small signal differential mode gain A_{DM} and common mode gain A_{CM}. The ac small signal analysis of differential amplifier can be performed by using hybrid-π model and h-parameter. Both the methods are explained in detail.

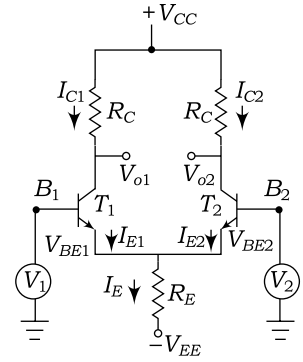


Fig. 6.14

Differential Mode Gain A_{DM} of Differential Amplifier

When input voltage V_1 is equal input voltage V_2 ($V_1 = V_2$), the current I_E flows through R_E divides equally into two transistors T_1 and T_2 due to symmetry. When V_1 is increased by small voltage $\Delta V_1 = \dfrac{\Delta V_d}{2}$ and V_2 is decreased by small signal $\Delta V_2 = \dfrac{\Delta V_d}{2}$, the differential amplifier is fed by differential small signal V_d. The common mode small signal is about zero. The collector current i_{C1} will be increased by small incremental current Δi_C and the collector current i_{C2} will be decreased by small increment current Δi_C. The total current in the transistors T_1 and T_2 is

$$I_E = i_{C1} + \Delta i_{C1} + i_{C2} - \Delta i_{C2}$$

$$= i_{C1} + \Delta i_C + i_{C2} - \Delta i_C = i_{C1} + i_{C2} \quad \text{as } \Delta i_{C_1} = \Delta i_{C_2} = \Delta i_C$$

Therefore, the current flows through resistance R_E is constant.

Since there is no change of current through resistance R_E, the voltage V_E at the common emitter terminal E is constant. During small signal analysis, the voltage at point E is 0 V. The small signal equivalent circuit of the differential input signal has differential mode gain A_{DM} and common mode gain A_{CM}. The ac small signal analysis of differential amplifier can be performed by using hybrid-π model and h-parameter. Both the methods are explained in detail.

Differential Mode Gain A_{DM} of Differential Amplifier

When input voltage V_1 is equal input voltage V_2 ($V_1 = V_2$), the current I_E flows through R_E divides equally into two transistors T_1 and T_2 due to symmetry. When V_1 is increased by small voltage $\Delta V_1 = \frac{\Delta V_d}{2}$ and V_2 is decreased by small signal $\Delta V_2 = \frac{\Delta V_d}{2}$, the differential amplifier is fed by differential small signal V_d. The common mode small signal is about zero. The collector current i_{C1} will be increased by small incremental current Δi_C and the collector current i_{C2} will be decreased by small increment current Δi_C. The total current in the transistors T_1 and T_2 is

$$I_E = i_{C1} + \Delta i_{C1} + i_{C2} - \Delta i_{C2}$$
$$= i_{C1} + \Delta i_C + i_{C2} - \Delta i_C = i_{C1} + i_{C2}$$

Therefore, the current flows through resistance R_E is constant.

Since there is no change of current through resistance R_E, the voltage V_E at the common emitter terminal E is constant. During small signal analysis, the voltage at point E is 0V. The small signal equivalent circuit with the differential input signal is shown in Fig. 6.15. The differential amplifier acts as a *linear amplifier*. When differential signal $V_d \le 2V_T$, the transfer characteristics is depicted in Fig. 6.12.

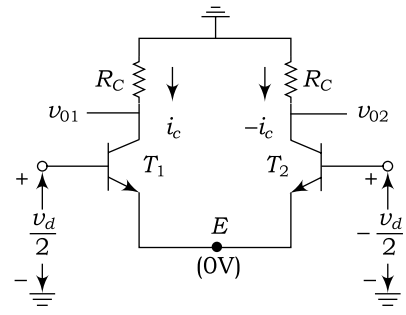


Fig. 6.15 Differential Amplifier with differential input voltage

Small Signal Analysis Using Hybrid π Model

As the performance of one side is identical to the performance of other side, we have to analyze only one side of the differential amplifier called differential-half circuit. Figure 6.16 shows a single stage CE transistor amplifier with a input voltage of $\frac{\Delta V_d}{2}$. The ac equivalent circuit in hybrid π-model of Fig. 6.16 is depicted in Fig. 6.17.

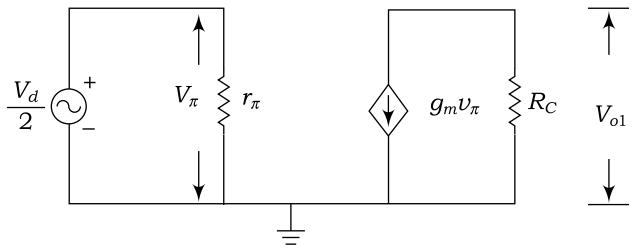


Fig. 6.17 ac equivalent circuit in hybrid π-model of Fig. 6.16

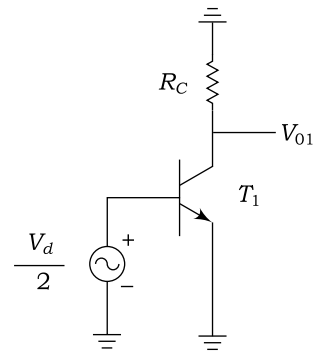


Fig. 6.16 Half circuit of differential amplifier

The output voltage $V_{o1} = -g_m V_\pi R_C$

As $V_\pi = \frac{V_d}{2}$, output voltage $V_{o1} = -g_m \frac{V_d}{2} R_C$

Therefore, $$\frac{V_{o1}}{V_d} = -\frac{1}{2} g_m R_C$$

Similarly, the output voltage $V_{o2} = g_m V_\pi R_C$

Since $$V_\pi = \frac{V_d}{2},\ V_{o2} = g_m \frac{V_d}{2} R_C$$

Then, $$\frac{V_{o2}}{V_d} = \frac{1}{2} g_m R_C$$

The output voltage of a differential amplifier

$$V_{o1} - V_{o2} = -\frac{1}{2} g_m R_C V_d - \frac{1}{2} g_m R_C V_d = -g_m R_C V_d$$

The differential mode gain A_{DM} is equal to

$$A_{\text{DM}} = \frac{V_{o1} - V_{o2}}{V_d} = -g_m R_C$$

When the output voltage is single ended (between collector of Transistor T_1 and ground), the differential mode gain A_{DM} is given by

$$A_{\text{DM}} = \frac{V_{o1}}{V_d} = -\frac{1}{2} g_m R_C \quad \text{and} \quad A_{\text{DM}} = \frac{V_{o2}}{V_d} = \frac{1}{2} g_m R_C$$

When r_o included in the transistor model, the differential mode gain A_{DM} is

$$A_{\text{DM}} = -g_m R_C \| r_o$$

Analysis using h parameters

The h parameter equivalent circuit of Fig. 6.16 is depicted in Fig. 6.18.

The output voltage is equal to

$$V_{o1} = -i_C R_C = -h_{fe} i_b R_C \quad \text{as} \quad i_C = h_{fe} i_b$$

The input voltage is $\frac{V_d}{2} = h_{ie} i_b$

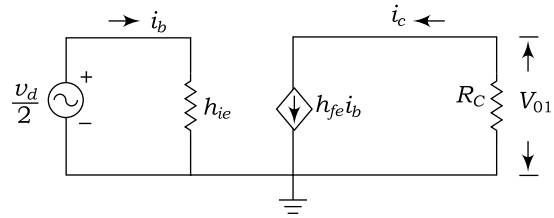


Fig. 6.18 h parameter equivalent circuit of Fig. 6.16

The differential mode gain A_{DM} is expressed by

$$A_{\text{DM}} = \frac{V_{o1}}{V_d} = -\frac{1}{2} \frac{h_{fe} i_b R_C}{h_{ie} i_b} = -\frac{1}{2} \frac{h_{fe}}{h_{ie}} R_C \quad \text{for single ended output}$$

In the same way, $A_{\text{DM}} = \frac{V_{o2}}{V_d} = \frac{1}{2} \frac{h_{fe} i_b R_C}{h_{ie} i_b} = \frac{1}{2} \frac{h_{fe}}{h_{ie}} R_C$ for single ended output

When the output is taken differentially between two collectors of transistors T_1 and T_2, the differential mode gain is $A_{\text{DM}} = \frac{V_{o1} - V_{o2}}{V_d} = -\frac{h_{fe}}{h_{ie}} R_C$

Common Mode Gain A_{CM} of Differential Amplifier

When both input signals V_1 and V_2 are increased by voltage V_C, the differential signal V_d is zero and the common mode signal is V_C. Subsequently i_{C1} and i_{C2} are increased by the incremental current i_C. The current through R_E can be increased by $2i_C$. The voltage at emitter terminal is V_E and its value is $2i_C R_E$.

To draw the common mode half circuit, R_E is replaced by $2R_E$. The common mode gain A_{CM} is computed from the small-signal hybrid π-equivalent model as shown in Fig. 6.20.

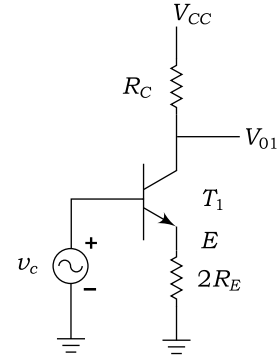


Fig. 6.19 Common mode half circuit

The common mode gain is equal to

$$A_{\text{CM}} = \frac{V_{o1}}{V_C} = \frac{V_{o2}}{V_C} = \frac{-\beta_o R_C}{r_\pi + 2(1+\beta_0)R_E}$$

Since $\beta_0 >> 1$,

$$A_{\text{CM}} = \frac{-g_m R_C}{1 + 2g_m R_E} = -\frac{1}{2}\frac{R_C}{R_E}$$

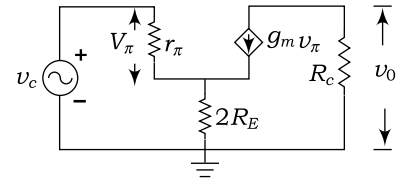


Fig. 6.20 The small-signal hybrid p-equivalent model of Fig. 6.19

When the output is taken differentially, the output voltage $V_{o1} - V_{o2}$ will be equal to zero and the common mode gain is zero.

Then

$$A_{\text{CM}} = \frac{V_{o1} - V_{o2}}{V_C} = 0$$

Using *h* parameter model, the common mode gain can be determined easily and it's value is

$$A_{\text{CM}} = \frac{V_{o1}}{V_C} = \frac{-h_{fe} R_C}{h_{ie} + 2(1+h_{fe})R_E}$$

The common mode rejection ratio (CMRR) is equal to ratio of differential mode gain A_{DM} to common mode gain A_{CM} and it is expressed by

$$CMRR = \left|\frac{A_{\text{DM}}}{A_{\text{CM}}}\right|$$

After substitutes the value of A_{DM} and $A_{\text{CM,}}$ we obtain

$$CMRR = \left|\frac{A_{\text{DM}}}{A_{\text{CM}}}\right| = \frac{g_m R_C (1 + 2g_m R_E)}{g_m R_C} \quad \text{as} \quad A_{\text{DM}} = -g_m R_C \quad \text{and} \quad A_{\text{CM}} = \frac{-g_m R_C}{1 + 2g_m R_E}$$

$$= (1 + 2g_m R_E) = 2g_m R_E$$

6.8.3 Improvement of CMRR of Differential Amplifier

If CMRR is very large, A_{CM} will be as small as possible. When A_{CM} is zero ($A_{\text{CM}} \to 0$), $R_E \to \infty$. There is a practical limitation on the magnitude of R_E due to quiescent dc voltage across it. When R_E is very large, the emitter voltage V_{EE} will be increased to maintain quiescent current. If the operating currents of the transistors are allowed to decrease, h_{ie} decreases and h_{fe} also decreases. Consequently, the common mode rejection ratio will decrease.

Therefore, a constant current bias can be used in place of R_E. It is shown in Fig. 6.21 that R_E can be replaced by a constant transistor circuit where R_1, R_2 and R_3 can be adjusted to provide the same quiescent conditions for the transistors T_1 and T_2. This circuit provides a very high effective emitter resistance R_E even for very small value of R_3. Usually, R_E is in the order of hundreds of kΩ even though the value of R_3 is small and its value is about 1 kΩ ($R_3 \cong 1$ kΩ). The emitter circuit behaves as a constant current source I_E.

KVL in transistor T_3 is

$$V_{BE3} + I_3 R_3 = V_D + (V_{EE} - V_D)\frac{R_2}{R_1 + R_2}$$

Where, the V_D is the voltage drop across diode *D*.

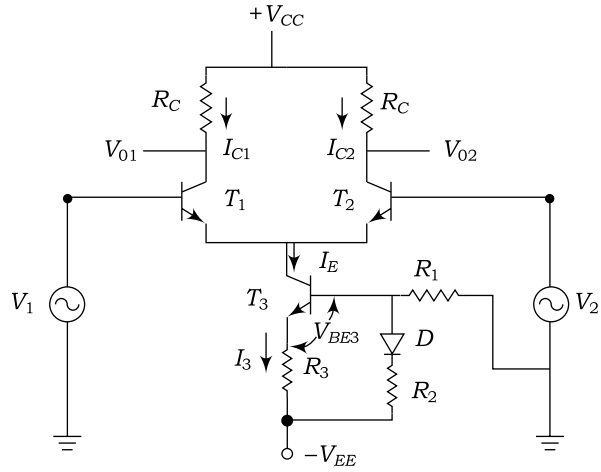


Fig. 6.21 Constant current bias differential amplifier

When the base current is neglected,

$$I_3 = I_E = \frac{1}{R_3}\left(V_{EE}\frac{R_2}{R_1+R_2} + V_D\frac{R_1}{R_1+R_2} - V_{BE3}\right)$$

If $$V_D\frac{R_1}{R_1+R_2} = V_{BE3},\ I_E = \frac{1}{R_3}\left(V_{EE}\frac{R_2}{R_1+R_2}\right)$$

The current I_E is constant and it does not depends on input voltage signals V_1 and V_2. The diode D makes I_E independent of temperature. The V_{BE3} decrease by 2.5mV/°C and the diode D has also same temperature dependence. Therefore, two variation of V_{BE3} and V_D can cancel each other and I_E independent of temperature. Generally, it is very difficult to satisfy the equation $V_D\frac{R_1}{R_1+R_2} = V_{BE3}$ using a single diode as V_D is approximately equal to V_{BE3}. Therefore, two diodes are used for V_D.

If I_E is constant, the common mode gain is zero and the current provides very high CMRR. At quiescent conditions, i.e., ac signal is not present, the current I_E is equally divided in transistors T_1 and T_2.

Then $$I_{C1} = I_{C2} = \frac{1}{2}I_E$$

When the same signal $V_1 = V_2$ is applied to both the inputs, there will be no change in collector currents I_{C1} and I_{C2} as the current I_E is constant. Consequently, the small signal current I_C flows through R_C is almost zero. Hence, the output voltage is zero.

If a differential amplifier is supplied by a constant current bias, this amplifier provides very high CMRR. IC 741 Op-amp uses different types of constant current source which are very simple circuit using less number of components. These circuits are called *current mirror* and provides extremely large resistance under ac conditions and subsequently provides a high value of CMRR.

6.9 CURRENT MIRROR (CONSTANT CURRENT SOURCE)

When a transistor operates in the active mode of operation, the collector current is independent of the collector voltage. This concept is used as a *constant current source*. In Fig. 6.22, transistor T_1 and T_2 having approximately same parameter are fabricated using IC technology. The bases and emitters of T_1 and T_2 are connected together and have the same V_{BE} as depicted in Fig. 6.22. Transistor T_1 is connected as a diode by shorting its collector to base. The input current I_{ref} flows through the diode connected transistor T_1. Hence there is a voltage across T_1. Accordingly, this voltage is also appears across the base and emitter of T_2.

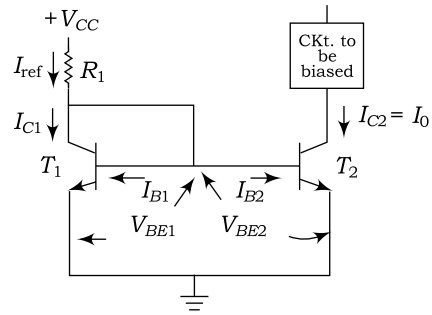


Fig. 6.22 Current mirror

As T_2 is identical to T_1, the emitter current of T_2 will be equal to the emitter current of T_1 which is equal to I_{ref}. If transistor T_2 operates in the active region, its collector current $I_{C2} = I_o$ which will be approximately equal to I_{ref}. Here, the output current I_o is a reflection or mirror of the reference current I_{ref}. Therefore this circuit can be referred as *current mirror*. The mirror effect of the circuit can be valid only for large value of β.

The collector current of transistor T_1 is I_{C1}

The collector current of transistor T_2 is I_{C2}

$$I_{C1} = \alpha_F I_{ES} e^{\frac{V_{BE1}}{V_T}} \quad \text{and} \quad I_{C2} = \alpha_F I_{ES} e^{\frac{V_{BE2}}{V_T}}$$

Then
$$\frac{I_{C2}}{I_{C1}} = \frac{\alpha_F I_{ES} e^{\frac{V_{BE2}}{V_T}}}{\alpha_F I_{ES} e^{\frac{V_{BE1}}{V_T}}} = e^{\frac{V_{BE2} - V_{BE1}}{V_T}}$$

Since
$$V_{BE1} = V_{BE2}, \; e^{\frac{V_{BE2} - V_{BE1}}{V_T}} = e^0 = 1$$

Therefore,
$$I_{C1} = I_{C2} = I_C = I_o$$

As transistor T_1 and T_2 are identical, $\beta_1 = \beta_2 = \beta$

KCL at the collector of transistor T_1 is

$$I_{\text{ref}} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

As
$$I_{C1} = I_{C2} = I_C \quad \text{and} \quad \beta_1 = \beta_2 = \beta, \; I_{\text{ref}} = \left(1 + \frac{2}{\beta}\right) I_C$$

I_C can be expressed as $I_C = \dfrac{\beta}{\beta + 2} I_{\text{ref}}$

Where,
$$I_{\text{ref}} = \frac{V_{CC} - V_{BE}}{R_1} = \frac{V_{CC}}{R_1} \text{ as } V_{CC} >> V_{BE} = 0.7V$$

Since $\beta >> 1$, $\frac{\beta}{\beta + 2} \to 1$ or unity. The output current I_o is equal to the reference I_{ref}, if R_1 is constant. When β varies between 50 and 200, I_o varies 3%. This circuit operates as a constant current source when transistor T_2 operates in active region, volt-ampere characteristics of transistor T_2 is depicted in Fig. 6.23 When $V_{CE2} < 0.3V$, transistor T_2 operates in saturation.

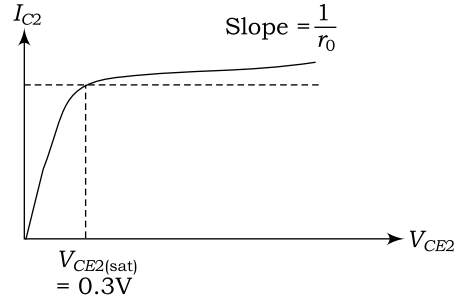


Fig. 6.23 V-I characteristics of a current mirror

For $V_{CE2} > 0.3V$, transistor operates in the active region and I_{C2} is about constant. Due to early effect, I_{C2} is increased slightly the slope of the curve in this region gives the output resistance r_o of the current source. The consequence of early effect is to deviate $\frac{I_{C1}}{I_{C2}}$ from unity. For practical cases, the early voltage may be assumed to be infinite, $r_o \to \infty$ and I_{C2} is constant.

6.10 OPEN-LOOP CONFIGURATIONS OF OP-AMP

The open-loop configuration of operational amplifier means that there is no connection between the output and input terminals either direct or via another network. Therefore, the output signal is not fed back in any form as a part of the input signal, and due to that, the loop is open.

During open-loop configuration, the operational amplifier simply works as a high-gain amplifier. Usually, the open-loop configurations of OP-AMPs are classified based on the number of inputs used and the terminal to which the input signal is applied. There are three different open-loop configurations of an OP-AMP as given below:

1. Differential amplifier
2. Inverting amplifier
3. Non-inverting amplifier

In this section, the above three configurations are explained elaborately.

6.10.1 Differential Amplifier

The circuit diagram of the open-loop differential amplifier is shown in Fig. 6.24. In this circuit diagram,

V_1 input signal is applied to the non-inverting terminal, and

V_2 input signal is applied to the inverting terminal.

As the OP-AMP amplifies the difference between the two input signals $(V_1 - V_2)$, this circuit configuration is known as a *differential amplifier*.

As OP-AMP amplifies both ac and dc input signals, this device is called a versatile device. Therefore, input signals V_1 and V_2 will be either ac or dc voltages. R_1 and R_2 are the source resistances of supply voltage V_1 and V_2 respectively. The magnitude of R_1 and R_2 are very less in value compared to the input resistance R_i. Consequently, the voltage drops across R_1 and R_2 can be assumed to be zero. Therefore, inverting terminal voltage $V_- = V_2$ and non-inverting terminal voltagee $V_+ = V_1$.

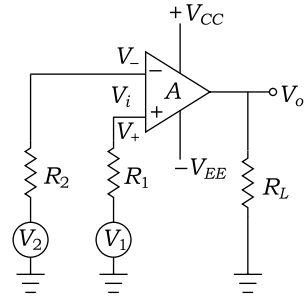


Fig. 6.24 Open-loop difference amplifier

The output voltage of OP-AMP is $V_o = A(V_+ - V_-)$

where, A is the open-loop gain of OP-AMP.

After substituting the values of $V_+ = V_1$ and $V_- = V_2$, we get

$$V_o = A(V_1 - V_2)$$

From the expression $V_o = A(V_1 - V_2)$, we can state that the output voltage is equal to the voltage gain A times the difference between two input voltages $(V_1 - V_2)$. It is also clear that the polarity of the output voltage is dependent on the polarity of the input difference voltage.

6.10.2 Inverting Amplifier

Figure 6.25 shows the open-loop configuration of the inverting amplifier. In this amplifier, only one input signal is applied to the inverting input terminal. The non-inverting input terminal is grounded.

Therefore, $V_+ = 0$ and $V_- = V_2$

Then output voltage is

$$V_o = A(V_+ - V_-) = A(0 - V_2) = -AV_2 \quad (6.9)$$

The negative sign indicates that output voltage is 180° out of phase with respect to input or output voltage having opposite polarity. In this way, the input signal is amplified by the open-loop gain A and is also inverted at the output in the inverting amplifier.

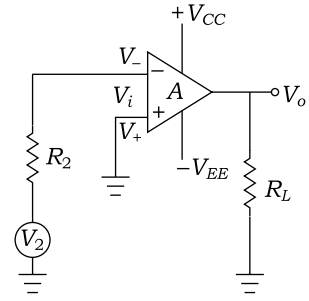


Fig. 6.25 Inverting amplifier

6.10.3 Non-Inverting Amplifier

The open-loop configuration of a non-inverting amplifier is depicted in Fig. 6.26. In this configuration, the input signal is applied to the non-inverting input terminal and inverting terminal is grounded.

Since $V_+ = V_1$ and $V_- = 0$, the output voltage is

$$V_o = A(V_+ - V_-) = A(V_1 - 0) = AV_1 \quad (6.10)$$

Therefore, the input voltage V_1 is amplified by a gain A. The output voltage is greater than A and it is in phase with the input voltage.

In each open-loop configuration of an operational amplifier, if any input signal is slightly greater than zero, the output voltage of an operational amplifier will be at saturation level. These results are obtained from the very high gain A of operational amplifier. Hence, when OP-AMP operates in open-loop configuration, the output of OP-AMP is either positive saturation voltage $+V_{sat}$ or negative saturation $-V_{sat}$. Consequently, open-loop OP-AMPs are not used in linear applications.

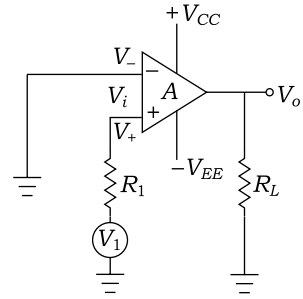


Fig. 6.26 Non-inverting amplifier

6.11 FEEDBACK IN IDEAL OP-AMP

The utility of OP-AMPs can be increased by using negative feedback. In this case, the output voltage is not saturation voltage and the OP-AMPs behave as a linear device as the output voltage is directly proportional to input voltages. There are two negative feedback circuits such as

1. Inverting amplifier
2. Non-inverting amplifier

In this section, inverting as well as non-inverting amplifiers are discussed assuming the following assumptions:

1. The current drawn by either inverting or non-inverting terminals is negligible.
2. The differential input voltage V_i between non-inverting and inverting terminals is approximately zero.

6.11.1 Inverting Amplifier

Figure 6.27 shows an inverting amplifier. The output voltage V_o is fed back to the inverting terminal through feedback resistance R_f and resistance R_1. The input voltage is applied to the inverting input terminal through resistance R_1. The non-inverting terminal is grounded.

In an ideal amplifier, $V_i = 0$, $i = 0$ for simplifying the output voltage equation. But in practical OP-AMP, $V_i \neq 0$. The equivalent circuit of a practical inverting amplifier is shown in Fig. 6.28. This circuit can be simplified by Thevenin's equivalent as depicted in Fig. 6.29 where, V_{eq} is Thevenin's equivalent voltage.

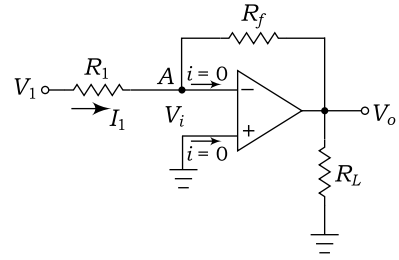


Fig. 6.27 Inverting amplifier

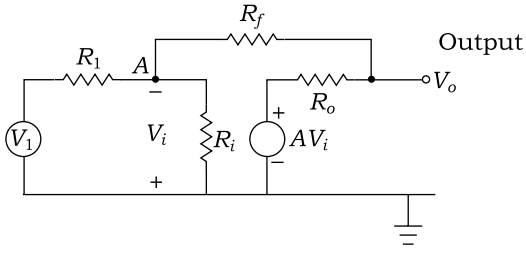


Fig. 6.28 Equivalent circuit of inverting amplifier

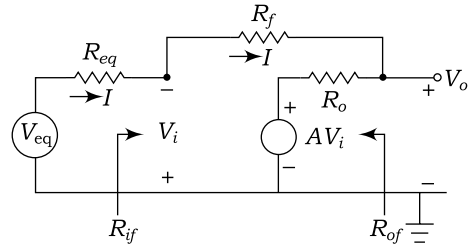


Fig. 6.29 Thevenin's equivalent circuit of inverting amplifier

The Thevenin's equivalent voltage is $V_{eq} = V_1 \dfrac{R_i}{R_1 + R_i}$

R_{eq} is Thevenin's equivalent resistance and $R_{eq} = R_i \| R_1 = \dfrac{R_1 R_i}{R_i + R_1}$

As $R_i >> R_1$, $R_{eq} = R_1$

$$V_{eq} = V_1 \frac{R_i}{R_1 + R_i} = V_1 \quad \text{as} \quad R_i >> R_1$$

The loop equations are

$$V_o = IR_o + AV_i \quad \text{and} \tag{6.11}$$

$$V_i + IR_f + V_o = 0$$

After substituting V_i in Eq. (6.11), we get

$$V_o = IR_o - A(IR_f + V_o)$$

or

$$(1 + A)V_o = I(R_o - AR_f) \tag{6.12}$$

The KVL equation is

$$V_{eq} = I(R_{eq} + R_f) + V_o = I(R_1 + R_f) + V_o \quad \text{as} \quad R_{eq} = R_1$$

or
$$V_{eq} = V_1 = \frac{(1+A)V_o}{R_o - AR_f}(R_1 + R_f) + V_o \quad \text{as} \quad I = \frac{(1+A)V_o}{R_o - AR_f}$$
$$= \frac{(1+A)(R_1 + R_f) + R_o - AR_f}{R_o - AR_f} V_o$$
$$= \frac{(1+A)R_1 + R_f + R_o}{R_o - AR_f} V_o \tag{6.13}$$

Closed-loop Gain

The closed-loop gain is
$$A_f = \frac{V_o}{V_1} = \frac{R_o - AR_f}{R_o + R_f + (1+A)R_1} \tag{6.14}$$

As $A >> 1$ and $AR_1 >> (R_o + R_f)$, $AR_f >> R_o$

Therefore, $A_f = \frac{V_o}{V_1} = -\frac{R_f}{R_1}$ (6.15)

Then the output voltage is $V_o = -\frac{R_f}{R_1} V_1$

The negative sign indicates that there is 180° phase shift between V_1 and V_o.

When R_f is replaced by Z_f and R_1 is replaced by Z_1, we get $V_o = -\frac{Z_f}{Z_1} V_1$

This expression can be used in different OP-AMPs applications such as integrator and differentiator which are explained in Chapter 7.

Input Resistance

Input resistance of OP-AMP is $R_{if} = \frac{V_i}{I}$

The KVL loop equation is
$$V_i + I(R_f + R_o) + AV_i = 0$$
or
$$(1+A)V_i + I(R_f + R_o) = 0$$
or
$$R_{if} = \frac{R_f + R_o}{1+A} \tag{6.16}$$

Output Resistance

Output resistance is calculated from the open-circuit output voltage V_{oc} and short-circuit output current I_{SC}

Output resistance is $R_{of} = \frac{V_{OC}}{I_{SC}}$

Figure 6.29 shows the equivalent circuit for calculating output resistance R_{of} when output is shorted.

Current $I_1 = \frac{V_{eq} - 0}{R_1 + R_f} = \frac{V_1}{R_1 + R_f}$, flow through R_{eq} and R_f

Current $I_2 = \dfrac{AV_i}{R_o}$, flow through R_o

As $$V_i = -I_1 R_f, I_2 = -\frac{AR_f}{R_o} I_1$$

The short-circuit output current is

$$I_{SC} = I_1 + I_2$$

After substituting I_1 and I_2, we get

$$= \frac{V_1}{R_1 + R_f} - \frac{AR_f}{R_o} \frac{V_1}{R_1 + R_f}$$

$$= \frac{V_1}{R_o(R_1 + R_f)}(R_o - AR_f) \tag{6.17}$$

The open-circuit output voltage is

$$V_{OC} = V_O = \frac{R_o - AR_f}{R_o + R_f + R_1(1 + A)} \tag{6.18}$$

The output impedance is

$$R_{of} = \frac{V_{OC}}{I_{SC}} = \frac{\dfrac{R_o - AR_f}{R_o + R_f + R_1(1 + A)} V_1}{\dfrac{(R_o - AR_f)V_1}{R_o(R_1 + R_f)}}$$

$$= \frac{R_o - AR_f}{R_o + R_f + R_1(1 + A)} \frac{R_o(R_1 + R_f)}{R_o - AR_f}$$

$$= \frac{R_o(R_1 + R_f)}{R_o + R_f + R_1(1 + A)}$$

$$= \frac{R_o(R_1 + R_f)}{(R_o + R_1 + R_f) + AR_1}$$

$$= \frac{\dfrac{R_o(R_1 + R_f)}{(R_o + R_1 + R_f)}}{1 + A\dfrac{R_1}{(R_o + R_1 + R_f)}} \tag{6.19}$$

The numerator is $R_o \| (R_1 + R_f)$ and its value is less than R_o. Hence, output resistance R_{of} is always less than R_o. If $A \to \infty$ and $R_{of} \to 0$.

6.11.2 Non-inverting Amplifier

Figure 6.30 shows a non-inverting amplifier. The input voltage is applied to the non-inverting input terminal. The feedback resistance R_f and R_1 are connected between the output terminal, inverting input terminal and ground. This circuit amplifies input voltage without

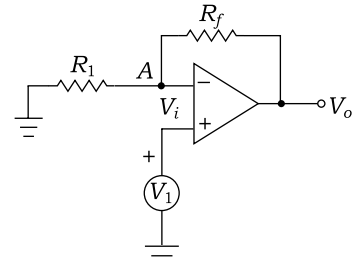


Fig. 6.30 Non-inverting amplifier

inverting. Therefore, there is no phase shift between input and output signals. This circuit is a negative feedback system as output is fed back to the inverting input terminal. The equivalent circuit of a practical non-inverting amplifier is depicted in Fig. 6.31.

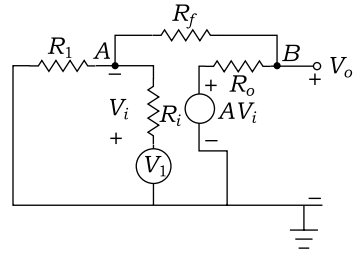


Fig. 6.31 Equivalent circuit of a practical non-inverting amplifier

The potential at the node A is $V_A = V_1 - V_i$

KCL law at the node A is

$$\frac{V_1 - V_i}{R_1} + \frac{V_i}{R_i} + \frac{V_1 - V_i - V_o}{R_f} = 0$$

Assume, $\frac{1}{R_1} = Y_1, \frac{1}{R_i} = Y_i$ and $\frac{1}{R_f} = Y_f$

Then we can write

$$(V_1 - V_i)Y_1 + V_iY_i + (V_1 - V_i - V_o)Y_f = 0$$

or
$$-(Y_1 + Y_i + Y_f)V_i + (Y_1 + Y_f)V_1 = Y_fV_o \tag{6.20}$$

Applying KCL at the node B, we get

$$\frac{(V_1 - V_i - V_o)}{R_f} + \frac{(AV_i - V_o)}{R_o} = 0$$

Assume $\frac{1}{R_o} = Y_o$

We can write $(V_1 - V_i - V_o)Y_f + (AV_i - V_o)R_o = 0$

or
$$-(Y_f - AY_o)V_i + Y_fV_1 = (Y_f + Y_o)V_o \tag{6.21}$$

After solving equations 6.20 and 6.21, we get

$$A_f = \frac{V_o}{V_i} = \frac{AY_o(Y_1 + Y_f) + Y_fY_i}{(A+1)Y_oY_f + (Y_1 + Y_i)(Y_f + Y_o)} \tag{6.22}$$

If $A \to \infty$

$$A_f = \frac{AY_o(Y_1 + Y_f)}{AY_oY_f}$$

or
$$A_f = \frac{(Y_1 + Y_f)}{Y_f} = 1 + \frac{Y_1}{Y_f}$$

$$A_f = 1 + \frac{R_f}{R_1} \quad \text{As} \quad \frac{1}{R_1} = Y_1, \text{and } \frac{1}{R_f} = Y_f \tag{6.23}$$

The gain of the amplifier can be adjusted by proper selection of resistances R_f and R_1.

6.12 OP-AMP CHARACTERISTICS

The manufacturers' data sheet of IC741 series operational amplifiers provide information regarding pin diagram, electrical characteristics and equivalent circuit of devices, etc. IC741 series OP-AMPs are available in

different models such as IC741, IC741A, IC741C and IC741E. The schematic diagram and electrical parameters for all models are same, but the value of parameters will differ from model to model. After studying the data sheet, we can state the following points:

1. IC741 is an internally frequency compensated OP-AMP.
2. IC741 is a monolithic IC.
3. Short-circuit protection is provided in this IC.
4. This IC has offset voltage null capacity.
5. It has large common-mode and differential voltage ranges.
6. Its power consumption is low.
7. Absence of latch-up makes the IC741 ideal for use as a voltage follower.
8. This IC is very useful for adder, subtractor, integrator, differentiation, voltage follower, multiplier and divider and other feedback applications.
9. Absolute maximum ratings for the following parameters such as supply voltage, input voltage, differential input voltage, internal power dissipation, operating temperature range and output short circuit duration, etc., are specified in the data sheet. Table 6.3 shows maximum rating of supply voltage, internal power dissipation, and operating temperature, etc.
10. The electrical specifications of the OP-AMP are input offset voltage, input offset current, input bias current, input capacitance, offset voltage adjustment range, etc. Table 6.4 shows the electrical characteristics of OP-AMP IC741C.

In this section, the electrical characteristics of typical operational amplifiers IC741C have been discussed.

Table 6.3 Maximum rating of IC

Parameters		*Absolute Maximum Rating*
Supply voltage	IC741, IC741A and IC741 E	±22 V
	IC741C	±18 V
Internal power dissipation	Metal can	500 mW
	Molded and hermetic DIP	670 mW
	Mini DIP	310 mW
	Flatpack	570 mW
Differential input voltage		±30 V
Input voltage		±15 V
Operating temperature range	Military IC741 and IC741A	–55°C to 125°C
	Commercial IC741E and IC741C	0°C to 70°C

Table 6.4 Electrical characteristics of IC741 at VS = ±15 V and operating temperature TA = 25°C

Electrical Characteristics	*Conditions*	*Minimum Value*	*Maximum Value*
Input offset voltage	$R_s \leq 10$ kΩ		20 mV
Input offset current		20 nA	200 nA
Input bias current		80 nA	500 nA
Input resistance		2.0 MΩ	
Input capacitance		1.4 pF	
Offset voltage adjustment range		±15 mV	

Contd.

Contd.

Input voltage range	±12 V	±13 V	
Common-mode rejection ratio	$R_s \le 10$ kΩ	70 dB	120 dB
Supply voltage rejection ratio		30 μV/V	150 μV/V
Large signal voltage gain	$R_L \ge 2$ kΩ $V_{out} = \pm 10$ V	20,000	200,000
Output voltage swing	$R_L \ge 2$ kΩ	±10 V	±14 V
Output resistance		75Ω	
Output short-circuit current		25 mA	
Supply current		1.7 mA	2.8 mA
Power consumption		50 mW	85 mW
Transient response	Rise time		0.3 μs
	overshoot		6%
Slew rate	$R_L \ge 2$ kΩ		0.5 μs

6.12.1 Input Offset Voltage

The input offset voltage (V_{IOS}) is the voltage that must be applied between inverting and non-inverting terminals of an operational amplifier to null the output voltage. Figure 6.32 shows the input offset voltage of an OP-AMP. In this circuit, V_{DC1} and V_{DC2} are dc voltages and R_S represents source resistance.

The input offset voltage is $V_{IOS} = (V_{DC1} - V_{DC2})$

The magnitude of input offset voltage can be positive or negative, but its absolute value is given on the manufacturer's data sheet. For example, the maximum value of V_{IOS} of IC 741C is about 20 mV. The smaller value of V_{IOS} is advantage for better input terminals matching.

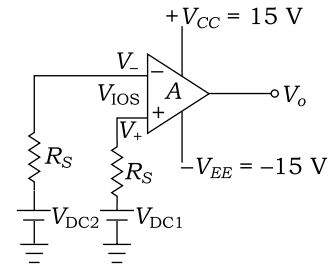


Fig. 6.32 Input offset voltage

6.12.2 Input Offset Current

The input offset current (I_{IOS}) is defined as the difference between the currents into the inverting and non-inverting terminals. Figure 6.33 shows the input offset current I_{IOS}.

The input offset current is

$$I_{IOS} = |I_{B1} - I_{B2}| \tag{6.24}$$

where, I_{B1} is the current input into the non-inverting terminal, and
I_{B2} is the current input into the inverting terminal.

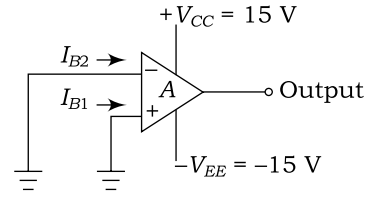


Fig. 6.33 Input offset current

The maximum value of input offset current for IC741C is about 200 nA. The difference between I_{B1} and I_{B2} will be small when the matching between two input terminals is improved.

6.12.3 Input Bias Current

The input bias current I_B is the average of the two input currents I_{B1} and I_{B2}. In the form of equation,

$$I_B = \frac{I_{B1} + I_{B2}}{2} \tag{6.25}$$

where, I_{B1} is the current input into the non-inverting terminal, and
I_{B2} is the current input into the inverting terminal.

For IC741C, the maximum value of input bias current, I_B is 500 nA. Actually I_{B1} and I_{B2} are base currents of the first-stage differential amplifier.

6.12.4 Offset Voltage Adjustment

One of the most important features of IC741 is an offset voltage null capability. Pins 1 and 5 are used as offset null. Figure 6.34 shows the offset voltage adjustment of the OP-AMP. A 10 kΩ potentiometer is connected between offset null pins 1 and 5. The wiper of the 10 kΩ potentiometer can be connected with the negative supply voltage $-V_{EE}$ = –15 V.

The output offset voltage can be reduced to zero by changing the wiper position of the potentiometer. The offset voltage adjustment range is the range through which the input offset voltage can be adjusted and it is about ±15 mV for IC741.

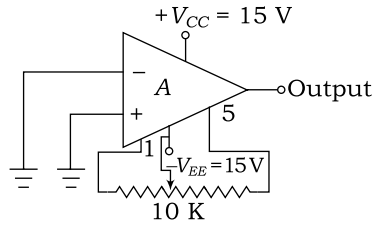


Fig. 6.34 Offset voltage adjustment

6.12.5 Thermal Drift

The operational amplifier parameters such as bias current, input offset current, input offset voltage change with temperature.

The average rate of change of input offset voltage permit change in temperature is called thermal voltage drift and it is represented by $\frac{\Delta V_{IOS}}{\Delta T}$ and its unit value is μV/°C.

In the same way, we can define the thermal drift in the input offset current and input bias current. Thermal drift of input offset current = $\frac{\Delta I_{IOS}}{\Delta T}$ nA/°C.

Thermal drift of input bias current = $\frac{\Delta I_B}{\Delta T}$ nA/°C.

Example 6.7 Assume input offset current (I_{IOS}) = 20 nA and input offset voltage (V_{IOS}) = 0 and $A = 10^5$. (a) What is the differential input voltage? (b) What is the output offset voltage?

Assume R_S = 1.5 kΩ

Sol.

(a) The differential input voltage = $I_{IOS} \times R_S$
$= 20 \times 10^{-9} \times 1.5 \times 10^3$
$= 30$ μV

(b) The output offset voltage is

$$V_{out} = AV_d = 10^5 \times 30 \times 10^{-6} \text{ V} = 3 \text{ V}$$

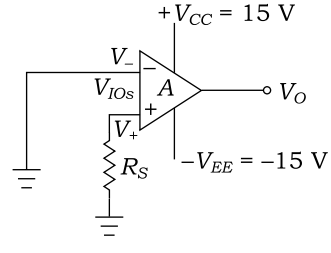


Fig. 6.35

Example 6.8 The base currents of a differential amplifier are I_{B1} = 15 μA and I_{B2} = 20 μA.

(a) What is the input bias current?

(b) Calculate the input offset current.

Sol. Given I_{B1} = 15 μA and I_{B2} = 20 μA

Input bias current is

$$I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{15 + 20}{2}\mu A = 17.5\,\mu A$$

The input offset current

$$I_{IOS} = |I_{B1} - I_{B2}| = |15 - 20|\,\mu A = 5\,\mu A$$

Example 6.9 The input base currents of differential amplifiers are I_{B1} = 100 nA and I_{B2} = 80 nA.

(a) Determine the input bias current and the input offset current.

(b) When $A = 10^5$, calculate the output offset voltage.

Assume R_S = 1 kΩ

Sol. Given I_{B1} = 100 nA and I_{B2} = 80 nA

(a) Input bias current is

$$I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{100 + 80}{2}\text{nA} = 90\text{ nA}$$

The input offset current

$$I_{IOS} = |I_{B1} - I_{B2}| = |100 - 80|\text{ nA} = 20\text{ nA}$$

(b) The differential input voltage $= I_{IOS} \times R_1$

$$= 20 \times 10^{-9} \times 1 \times 10^3 = 20\,\mu V$$

The output offset voltage is

$$V_{out} = AV_d = 10^5 \times 20 \times 10^{-6}\text{ V} = 2\text{ V}$$

6.12.6 Common-mode Rejection Ratio

Figure 6.36 shows the common-mode circuit of OP-AMP. The *common-mode rejection ratio* (*CMRR*) can be defined as the ratio of the differential voltage gain A_d to the common-mode voltage gain A_{cm}. It is expressed as $CMRR = \frac{A_d}{A_{cm}}$

The differential voltage gain A_d is same as the open-loop voltage gain A.

The common-mode voltage gain can be computed by using the equation

$$A_{cm} = \frac{V_{ocm}}{V_{cm}} \qquad (6.26)$$

where, A_{cm} is common-mode voltage gain,

V_{cm} is input common-mode voltage, and

V_{ocm} is output common-mode voltage.

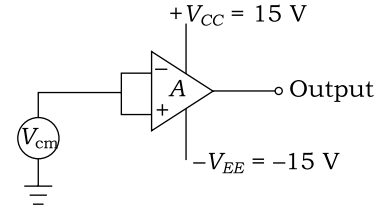


Fig. 6.36 Common-mode circuit of OP-AMP

Normally, A_{cm} is very small and A_d is very large. Therefore, the *CMRR* is very large and it is very frequently expressed in decibels (dB). The *CMRR* value of IC741 is about 90 dB.

Figure 6.36 shows the common-mode configuration of an operational amplifier. For this circuit, R_S is assumed to be zero as source resistances of practical voltage sources are very small.

6.12.7 Supply-Voltage Rejection Ratio

The change in an operational amplifier's input offset voltage due to variations in supply voltage is known as the *supply voltage rejection ratio* (*SVRR*). Some manufacturers represent the *SVRR* as power supply rejection (*PSRR*) or power supply sensitivity (*PSS*). Usually, it is expressed in μV/V or in decibels (dB).

In the form of an equation,

$$SVRR = \frac{\Delta V_{IOS}}{\Delta V} \tag{6.27}$$

where, ΔV is the change in supply voltage, and

ΔV_{IOS} is change in the input offset voltage.

For IC741, SVRR is about 6.3 μV/V.

6.12.8 Slew Rate

The Slew Rate (*SR*) is defined as the maximum rate of change of output voltage per unit time. It can be expressed as

$$SR = \left.\frac{dV_o}{dt}\right|_{\max} \text{ V/μs.} \tag{6.28}$$

This is an important parameter for high-frequency applications such as oscillators, comparators and filters. The typical values of slew rate for IC741 is about 0.5 V/μs.

The *SR* indicates how rapidly operational amplifier can vary in response to variation in the input frequency. These changes with change in voltage gain. Normally, the slew rate of an operational amplifier is fixed. If the slope requirements of the output signal are greater than the slew rate, output will be distorted. Therefore, slew rate is an important factor to select OP-AMPs in high frequency applications.

In a voltage-follower circuit, the input voltage is large amplitude and high frequency sine wave.

Assume supply voltage is $V_S = V_m \sin \omega t$

Then output is $V_o = V_m \sin \omega t$

The rate of change of output is

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t \tag{6.29}$$

The maximum rate of change of output at $\cos \omega t = 1$

$$SR = \left.\frac{dV_o}{dt}\right|_{\max} = \omega V_m = 2\pi f V_m \text{ V/s} \quad \text{as } \omega = 2\pi f$$

$$= \frac{2\pi f V_m}{10^6} \text{ V/μs} \tag{6.30}$$

The slew rate can also be expressed as

$$SR = \frac{dV_o}{dt} = \frac{\Delta V_O}{\Delta t} = \frac{I_{\max}}{C} \text{ V/μs.} \tag{6.31}$$

where, $I_{\max}$ is the maximum current which flows through the capacitor C and

C is the value of the capacitance.

The slew rate can be improved by increasing the current and decreasing the capacitor value. For high value of slew rate, operational amplifiers should have small value of capacitor with high current. The slew rate can also be improved with higher closed-loop gain.

Example 6.10 The output voltage of operational amplifier changes by 10 V within 5 μs. Calculate the slew rate.

Sol. Given: Change in output voltage $\Delta V_o = 10$ V and $\Delta t = 5$ μs

The slew rate is

$$SR = \frac{\Delta V_O}{\Delta t} \text{V/μs} = \frac{10}{5} \text{V/μs} = 2\text{V/μs}$$

Example 6.11 The output voltage of an operational amplifier is shown in Fig. 6.37. When input voltage is triangular 8 V wave peak-to-peak amplitude with frequency 2 MHz, what is the slew rate of the operational amplifier?

Sol. The slew rate is defined as the maximum rate of change of the output voltage and it is expressed as

$$SR = \frac{\Delta V_O}{\Delta t} \text{ V/μs}$$

Here, $\Delta V_o = 8$ V and $\Delta t = \frac{0.5}{2} = 0.25$ μs

Then slew rate $SR = \frac{\Delta V_O}{\Delta t} \text{V/μs} = \frac{8}{0.25} \text{V/μs} = 32$ V/μs

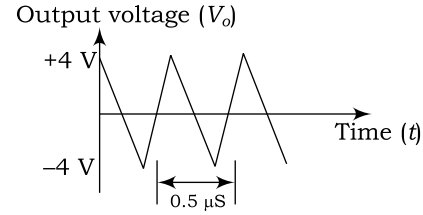


Fig. 6.37

Example 6.12 An IC741C OP-AMP is used as an inverting amplifier with a gain of 50. The input voltage is sinusoidal with maximum amplitude of 25 mV. What is the maximum frequency of the input voltage?

Sol. The typical slew rate of IC741C OP-AMP is 0.5 V/μs and $A = 50$

The maximum output voltage is

$$V_m = AV_{id} = 50 \times 25 \times 10^{-3} \text{ V} = 1.25 \text{ V}$$

As $V_{id} = 25$ mV

The slew rate is $SR = \frac{2\pi f V_m}{10^6} = 0.5$ V/μs

The maximum frequency is $f_{\max} = \frac{SR}{2\pi V_m} \times 10^6$

$$= \frac{0.5}{2\pi \times 1.25} \times 10^6 \text{ Hz}$$

$$= 63.694 \text{ kHz}$$

Example 6.13 An IC741C OP-AMP is used as an inverting amplifier with a gain of 40. The voltage gain vs frequency response is flat up to 30 kHz. What is the maximum peak to peak input signal that can be applied without distorting the output voltage?

Sol. The typical slew rate of IC741C OP-AMP is 0.5 V/μs

Therefore $SR = 0.5$ V/μs

Frequency $f = 30$ kHz

The maximum output voltage is

$$V_m = \frac{SR}{2\pi f} \times 10^6 = \frac{0.5}{2\pi \times 30 \times 10^3} \times 10^6 \text{ V}$$

$$= 2.653 \text{ V (peak)} = 5.306 \text{ V (peak to peak)}$$

The maximum peak-to-peak input voltage without distorting the output is

$$V_{\text{id}} = \frac{V_m}{A} = \frac{5.306}{40} V = 132.65 \text{ mV (peak-to-peak)}$$

Example 6.14 An operational amplifier has a slew rate of 0.5 V/μs. If the peak output voltage is 10 V, what is the maximum frequency at which operational amplifier operates properly?

Sol. The slew rate of the operational amplifier is 0.5 V/μs

The slew rate is $SR = \frac{2\pi f V_m}{10^6} = 0.5 \text{ V/μs}$

The maximum frequency of operation is

$$f_{\max} = \frac{SR}{2\pi V_m} \times 10^6 = \frac{0.5}{2\pi \times 10} \times 10^6 \text{ Hz} = 7.96 \text{ kHz}$$

Example 6.15 An operational amplifier has a slew rate of 0.45 V/μs. How much time will it take to change the output voltage from 0 V to 10 V?

Sol. The slew rate of operational amplifier is 0.45 V/μs

The change in output voltage, ΔV_o is 10 V

The slew rate is

$$SR = \frac{\Delta V_O}{\Delta t} \text{ V/μs}$$

or $$\Delta t = \frac{\Delta V_O}{SR} = \frac{10}{0.45} \text{ μs} = 22.23 \text{ μs}$$

Therefore the required time to change output voltage from 0 to 10 V is 22.23 μs

Example 6.16 The charging current of a 150 pF capacitor is 100 μA. What is the slew rate of operational amplifier?

Sol. Given: Capacitor $C = 150 \text{ pF} = 150 \times 10^{-12}$ F

Charging current $I_O = 100 \text{ μA} = 100 \times 10^{-6}$ s

The slew rate of the operational amplifier is

$$SR = \frac{dV_O}{dt} = \frac{I_O}{C}$$

$$= \frac{100 \times 10^{-6}}{150 \times 10^{-12}} \text{ V/s} = \frac{100 \times 10^{-6}}{150 \times 10^{-12} \times 10^6} \text{ V/μs} = 0.667 \text{ V/μs}$$

Example 6.17 An operational amplifier has slew rate about 0.45 V/μs and used as an inverting amplifier with a gain 100. The voltage gain vs frequency curve of an operational amplifier up to 20 kHz is flat. What is the maximum peak–to-peak input signal that can be applied to the operational amplifier without distorting the output voltage?

Sol. Given $SR = 0.45$ V/μs, $A = 100$ and $f_{max} = 20$ kHz

The slew rate is $SR = \dfrac{2\pi f V_m}{10^6} = 0.45$ V/μs

The maximum output voltage is

$$V_m = \frac{SR}{2\pi f} \times 10^6 = \frac{0.45}{2\pi \times 20 \times 10^3} \times 10^6 = 3.58 \text{ V}$$

The maximum output voltage is

$$V_m = AV_{id} \text{ V}$$

The maximum peak-to-peak input voltage to the OP-AMP without distorting the output voltage is

$$V_{id} = \frac{V_m}{A} = \frac{3.58}{100} \text{V} = 35.8 \text{ mV}$$

Example 6.18 Figure 6.38 shows an operational amplifier circuit. The operational amplifier has a slew rate of about 0. 5 V/μs, gain is 10 and output saturation voltage levels are ±10 V, maximum frequency is 100 kHz.

(a) Determine the maximum peak amplitude of the output sinusoidal signal at 100 kHz for the undistorted output voltage.

(b) Calculate the values of R_1 and R_2.

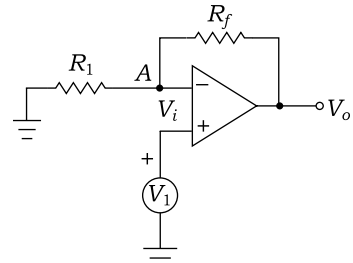


Fig. 6.38

Sol. Given $SR = 0.5$ V/μs, $A = 10$ and $f_{max} = 100$ kHz

(a) The slew rate is $SR = \dfrac{2\pi f V_m}{10^6} = 0.5$ V/μs

The maximum peak amplitude of the output sinusoidal signal is

$$V_m = \frac{SR}{2\pi f} \times 10^6 = \frac{0.5}{2\pi \times 100 \times 10^3} \times 10^6 \text{ V} = 0.796 \text{ V (peak)}$$

(b) The closed-loop gain of the operational amplifier is = 10

As gain $= 1 + \dfrac{R_f}{R_1} = 10$

Therefore, $\dfrac{R_f}{R_1} = 9$ or $R_f = 9R_1$

If $R_1 = 2.2$ k and $R_f = 2.2 \times 9$ kΩ = 19.8 kΩ

6.12.9 Input Resistance

It is the differential resistance found in any of the input terminals when the other terminal is grounded. The input resistance of 741 C is about 2 MΩ.

6.12.10 Input Capacitance

This is the equivalent capacitance which can be measured from any of the input terminals when the other terminal is grounded. The input capacitance of 741C is about 1.4 pF.

6.12.11 Large Signal Voltage Gain

An operational amplifier amplifies the difference in voltage between two input terminals. The voltage gain is defined as

$$\text{Voltage gain} = \frac{\text{Output voltage}}{\text{Differential input voltage}}$$

As the amplitude of output signal is larger than the input signal, the voltage gain is commonly known as large signal voltage gain. The typical value of voltage gain of IC741 is 2,00,000 when $R_L \geq 2\ \text{k}\Omega$ and $V_{out} = \pm 10$ V.

6.12.12 Output Resistance

The output resistance R_o is the resistance measured between the output terminal and ground. The typical value of output resistance for IC741C is about 75 Ω.

6.12.13 Output Short-Circuit Current

This current can flow when the operational amplifier gets shorted and its value is very high. The operational amplifier must be provided with short-circuit protection. The short-circuit current of IC741 is about 25 mA.

6.12.14 Supply Current

When the operational amplifier is working properly, the supply current I_S must be drawn by the device from the power supply. The typical value of supply current is 2.8 mA for IC741.

6.12.15 Power Consumption

If the operational amplifier is working properly, a certain amount of power must be consumed by this device. The typical value of power consumption is about 85 mW for IC741.

6.12.16 Transient Response

The rise time and overshoot are the two important characteristics of the transient response of an operational amplifier circuit. The typical values of rise time and overshoot are 0.3 μs and 6% respectively.

6.13 VIRTUAL GROUND

In an ideal operational amplifier, the input impedance is infinite ($Z_i = \infty$) and no current flows through inverting and non-inverting terminals ($I_i = 0$). As no current flows through the input terminals, the current I flows through resistance R_1 and the same current also passes through resistance R_f as shown in Fig. 6.39 . Since gain of ideal operational $A = \infty$, $\frac{V_O}{V_i} = A$, and $V_i = 0$. This states that the input terminals of the operational amplifier are effectively shorted and *virtual ground* exists in the circuit. The normal ground of a circuit means that it has zero potential (voltage) and it can sink infinite current.

In case of virtual ground, at any point of the circuit, the terminal voltage is zero with respect to ground and the said terminal draws zero current. Therefore, as far as voltage is concerned, there is no difference between the normal ground and virtual ground, but when current

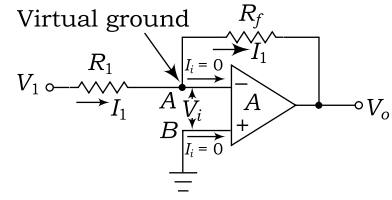


Fig. 6.39

is concerned, ordinary (normal) ground terminal can sink infinite current whereas virtual ground terminal draws no current. For any operational amplifier circuit, the input part appears as a short as $V_i = 0$, but it appears as open due to current $I_i = 0$.

Figure 6.40 shows the simplified equivalent circuit of Fig. 6.39. Assume B is connected with ground and its potential is ground potential (zero volt). The non-inverting terminal has ground potential. The inverting terminal A is connected with non-inverting terminal B by dotted line. The current flow $I_i = 0$, and voltage across A and B is $V_i = 0$. Therefore, the inverting terminal is also at ground potential though there is no physical connection between inverting terminal and ground. For that reason, the inverting terminal A is called *virtual ground*.

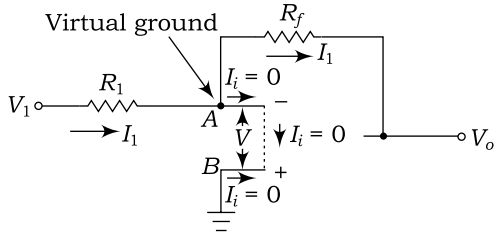


Fig. 6.40

6.14 FREQUENCY RESPONSE OF OPERATIONAL AMPLIFIER

The open-loop voltage gain of an operational amplifier is very high and it is about 10^5. When negative feedback is applied to an OP-AMP, the overall gain of feedback amplifier is reduced to any required value by the amount of feedback used in the circuit. At high frequency, a negative feedback operational amplifier becomes unstable as the *RC* coupling network introduces a phase shift in the output voltage with respect to input voltage. When phase shift is equal to 180°, feedback will be positive and oscillations occur in the OP-AMP feedback circuit. To avoid this problem, IC741 has internal *RC* network, which can reduce gain at high frequency.

The voltage gain of an operational amplifier should be uniform at all frequencies in the bandwidth. For a practical OP-AMP circuit, an ideal performance will not be available as transistor circuit has frequency-sensitive parameters, such as inductance and capacitance, both in lumped and distributed form. Capacitance effects come in the OP-AMP equivalent circuit due to transistors and FET devices as these are charge devices, and due to substrate on which OP-AMPs are fabricated. Figure 6.41 shows the equivalent circuit incorporating capacitance. The frequency response of an amplifier has been divided into three regions such as low frequency, mid frequency and high frequency. Actually, an operational amplifier is a dc amplifier and frequency response in the low-frequency and mid-frequency regions will be flat. A single capacitor at the output represents a single pole and each pole is an energy-storing element.

The output voltage is

$$V_O = AV_i \frac{\dfrac{1}{sC}}{R_O + \dfrac{1}{sC}} = \frac{1}{1 + sCR_O} AV_i \qquad (6.32)$$

The open-loop gain is

$$A_{\text{OL}} = \frac{V_O}{V_i} = \frac{A}{1 + sCR_O} \qquad (6.33)$$

where, A is the gain of the amplifier, and
CR_O is the time constant.

After substituting $s = j\omega$ for a sinusoidal frequency response, The A_{OL} becomes

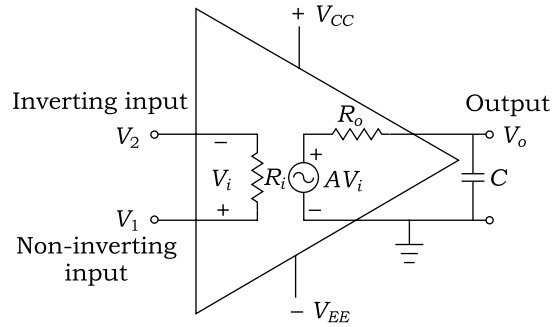


Fig. 6.41 Equivalent circuit of OP-AMP including capacitance

$$A_{\text{OL}} = \frac{A}{1 + j\omega CR_O} = \frac{A}{1 + j\dfrac{\omega}{\omega_C}} \quad \text{as} \quad \omega_C = \frac{1}{CR_O}$$

$$= \frac{A}{1 + j\dfrac{2\pi f}{2\pi f_C}} = \frac{A}{1 + j\dfrac{f}{f_C}} \tag{6.34}$$

The absolute magnitude is $|A_{\text{OL}}| = \dfrac{A}{\left[1 + \left(\dfrac{f}{f_C}\right)^2\right]^{1/2}}$ and phase angle $\phi = -\tan^{-1}\left(\dfrac{f}{f_C}\right)$

- At $f = 0$, $A_{\text{OL}} = A$
  In dB, $A_{\text{OL}} = 20 \log A$
- At $f = 0.1 f_C, |A_{OL}| = \dfrac{A}{\left[1 + \left(\dfrac{0.1 f_C}{f_C}\right)^2\right]^{1/2}} = \dfrac{A}{1.005}$
  In dB, $A_{\text{OL}} = 20 \log A - 20 \log 1.005 = 20 \log A - 0.0433$ dB
- At $f = f_C, |A_{OL}| = \dfrac{A}{\sqrt{2}}$
  In dB, $A_{OL} = 20 \log A - 20 \log 1.414 = 20 \log A - 3.0089$ dB
- At $f = 10 f_C, |A_{OL}| = \dfrac{A}{\sqrt{101}}$
  In dB, $A_{OL} = 20 \log A - 20 \log 10.049 = 20 \log A - 20.043$ dB

Figure 6.42 shows the frequency response of an operational amplifier. When the open-loop gain of an operational amplifier is 10^5, the gain at very low frequency is 20 log(10^5) = 100 dB. At frequency f_c, magnitude is reduced by $\dfrac{1}{\sqrt{2}}$ times or the gain drops by 3 dB. The f_c is called the *half-power frequency*. At frequency $f = 10 f_c$, the gain drops by 20 dB. The gain can be reduced to 0 dB (unity) at the frequency f_T. Then, f_T is called *frequency of unity gain*. After applying the negative feedback, if the overall gain A_f is 10, it will be 20 dB in dB as shown in Fig. 6.42 and the half-power frequency increases to f_H.

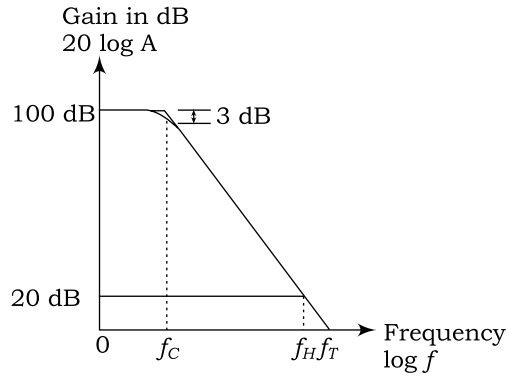


Fig. 6.42 Gain vs frequency plot of OP-AMP including capacitance

6.15 STABILITY OF OPERATIONAL AMPLIFIER

Assume the open-loop gain of the operational amplifier is frequency dependent and it can be represented as $A(f)$. Figure 6.43 shows a non-inverting feedback amplifier circuit and its block-diagram representation is depicted in Fig. 6.44.

The error signal is

$$V_i = V_1 - \beta V_o$$

where, feedback voltage is βV_o and input voltage is V_1.

The output voltage is $V_O = A_{OL} V_i$ and $V_i = \dfrac{V_O}{A_{OL}}$

Therefore, $$V_i = \frac{V_O}{A_{OL}} = V_1 - \beta V_O$$

or $$\frac{V_O}{A_{OL}} + \beta V_O = V_1$$

or $$\frac{1 + \beta A_{OL}}{A_{OL}} V_O = V_1$$

Then, $$\frac{V_O}{V_1} = \frac{A_{OL}}{1 + \beta A_{OL}} \qquad (6.35)$$

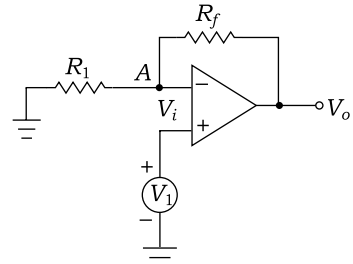


Fig. 6.43 Non-inverting amplifier

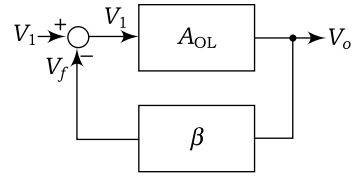


Fig. 6.44 Block-diagram representation of non-inverting amplifier

This is called *closed-loop gain* of the amplifier and βA_{oL} is called closed-loop gain which is used to determine the stability of the operational amplifier.

The condition for stability is $1 + \beta A_{OL}$ or $\beta A_{OL} = -1$.

In the complex plane, $\beta A_{OL} = -1$ and can be expressed as $\beta A_{OL} = -1 + j0$

Therefore, absolute value of $|\beta A_{OL}| = 1$ and $\angle \beta A_{OL} = 0°$ or $360°$.

When the conditions $|\beta A_{OL}| = 1$ and $\angle \beta A_{OL} = 0°$ or $360°$ are satisfied at a particular frequency, the system starts to oscillate and becomes unstable. The system will be stable if its output reaches a final value with infinite time. If output increases with time in the system or the system has output signal without input, the system is said to be unstable. To check the stability of system, the conditions $|\beta A_{OL}| = 1$ and $\angle \beta A_{OL} = 0°$ or $360°$ are verified. If these conditions are not satisfied, the system is stable and otherwise it is unstable.

6.16 IMPORTANCE OF FEEDBACK LOOP (POSITIVE AND NEGATIVE)

When an OP-AMP uses feedback, it is called feedback amplifier. Sometimes it is also known as a closed-loop-amplifier because the feedback forms a closed loop between input and output. There are two types of feedback such as negative feedback and positive feedback. Again negative feedback is of four types, namely voltage series feedback, voltage shunt feedback, current series feedback and current shunt feedback. Among the four types of negative feedback, voltage-series feedback and voltage shunt feedback are most important and are widely used in amplifiers but current-series and current-shunt feedbacks are seldom used.

The advantages of negative feedback loop are given below:

(i) The overall gain is reduced with negative feedback and the operation of feedback amplifier is stabilised.

(ii) Phase distortion is reduced with negative feedback.

(iii) Noise is reduced by the factor $(1 + \beta A)$ where β is feedback gain and A is open loop gain.

(iv) The frequency distortion arising because of varying amplifier gain with frequency is considerably reduced in a negative voltage feedback amplifier.

(v) With negative feedback, the bandwidth of the amplifier increases.

The importance of positive feedback in amplifier is given below:

(i) With positive feedback in the feedback amplifier, the circuit operates as an oscillator. Hence positive feedback circuit also operates in unstable mode.

(ii) The phase distortion as well as noise level are increased due to positive feedback.

(iii) With positive feedback, the bandwidth decreases.

6.17 VOLTAGE FOLLOWER (BUFFER CIRCUITS)

When the resistance R_f is set equal to zero or the inverting terminal of OPAMP is directly connected to the output terminal and the resistance R_1 is made ∞ by keeping it open-circuited in a non-inverting amplifier as shown in Fig. 6.45, the output voltage follows the input voltage.

The voltage follower is a circuit in which the output voltage follows the input voltage. Figure 6.45 shows a typical voltage-follower circuit. As the output voltage follows the input voltage, V_o will be equal to V_{in}.

Therefore, $$V_o = V_{\text{in}}$$

Actually the output voltage of the OPAMP circuit as shown in Fig. 6.45 exactly tracks the input voltage both in sign and magnitude. For this reason, this circuit is called a voltage follower.

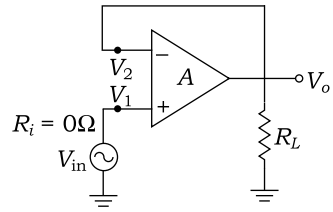


Fig. 6.45 Voltage follower

If we assume that v_1 is the voltage at non-inverting terminal and v_2 is the voltage at inverting terminal, the differential voltage is equal to $v_d = (v_1 - v_2)$

Then the output voltage is

$$V_o = A\ v_d = A(v_1 - v_2)$$
$$= A(V_{\text{in}} - V_o) \text{ as } v_1 = V_{\text{in}} \text{ and } v_2 = V_o$$

where A is open loop gain

Therefore, $$\frac{V_o}{V_{\text{in}}} = \frac{A}{1+A} \cong 1 \qquad \text{as } A >> 1$$

Hence, the gain of voltage follower $A_f = 1$

It is clear from Fig. 6.45 that the output voltage is directly connected to the inverting terminal of the OP-AMP and it represents the case of 100% negative feedback of the output to the input. Subsequently, the output voltage is always related to the input quantity. When the open-loop is very high value of the order of 10^5, the closed loop gain of voltage follower becomes unity.

The detailed analysis of the equivalent circuit of OPAMP reveals that the resistance looking into the input terminals is equal to the value of AR_{in}.

where, A is open-loop gain and it's value is about 10^5.

The value of R_{in} is high and it is about 1 MΩ.

Therefore, the input resistance of the voltage follower is

$$AR_{\text{in}} = 1 \times 10^6 \times 10^5 = 10^5 \text{ MΩ}$$

Consequently, the OPAMP produces virtually no effect on the input signal source.

The detailed analysis of the equivalent circuit of OPAMP reveals that the output resistance R_o looking into the output terminals is about $\frac{R_o}{A}$ when 100% feedback is used. The normal value of R_o is 75 Ω.

Therefore the output resistance of the OPAMP becomes $\frac{R_o}{A} = \frac{75}{10^5} = 0.75$ mΩ. This states that on the output side, the OPAMP behaves just like a voltage source with negligible internal resistance.

In this way, the voltage follower circuit has three unique characteristics such as

- Extremely high input resistance about 10^5 MΩ
- Extremely low output resistance about few mΩ
- Unity transmission gain $\left(\frac{V_o}{V_{\text{in}}} = 1\right)$

For the above features, the voltage follower circuit is an ideal circuit device to serve as a buffer.

6.18 LEVER SHIFTER

A level shifter should be used in an IC 741 OP-AMP as an OPAM should operate with dc supply and no coupling capacitor is used. Due to direct coupling, the dc level rises from one state to next stage. Therefore, the increase in dc level tends to shift the operating point of the next stage transistors. For this reason, the output voltage swing and the nature of output voltage signal may be distorted. Therefore, it is essential that the quiescent voltage of one stage is shifted before it is applied to the next stage. For proper operation of OPAMP, the output should have quiescent voltage level of 0V for zero input signal.

Figure 6.46 shows the most simplest type of a level shifter. This circuit is basically an emitter follower. Therefore, the level shifter can also act as a buffer to isolate the high gain stages from the output stage. The amount of shift obtained is equal to

$$V_o - V_{\text{in}} = - V_{BE} \cong -0.7 \text{ V}$$

When the voltage shift $V_o - V_{\text{in}} = -0.7$ V is not sufficient, the output can be taken from the junction of two resistors R_1 and R_2 as depicted in Fig. 6.47. Accordingly the voltage shift is now increased by the voltage drop across R_1. But this circuit has the disadvantage that signal voltage will be attenuated by the factor $\frac{R_2}{R_1 + R_2}$. This problem can be easily solved if R_2 is replaced by a current mirror I as shown in Fig. 6.48. Subsequently the voltage shift in level is

$$V_o - V_{\text{in}} = -(V_{BE} + IR_1)$$

and there is no attenuation of voltage signal due to high resistance of the current source.

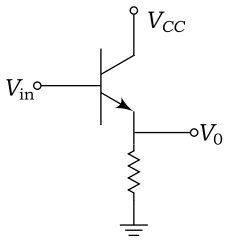


Fig. 6.46 Level Shifter

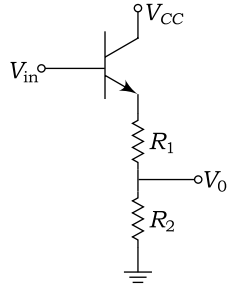


Fig. 6.47 Level shifter

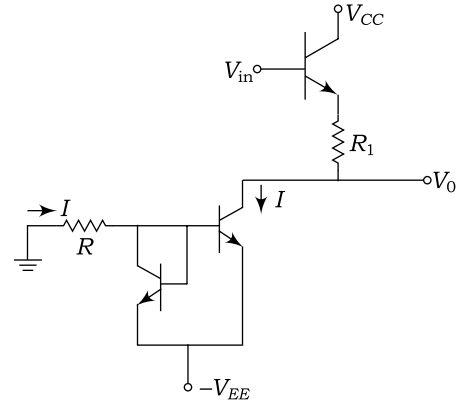


Fig. 6.48 Level shifter with current mirror

Review Exercises

Short-Answer Questions

1. What is an inverting amplifier?

Ans. In an inverting amplifier, only one input signal is applied to the inverting (–) input terminal and the non-inverting (+) input terminal is grounded.

2. What is a non-inverting amplifier?

Ans. In a non-inverting amplifier, only one input signal is applied to the non-inverting (+) input terminal and the inverting (–) input terminal is grounded.

3. Give a list of applications of an inverting amplifier.

Ans. Inverting amplifiers are used in adder, integrator, differentiator, phase shifter and analog computation.

4. What is a differential amplifier?

Ans. The differential amplifier is a combination of inverting and non-inverting amplifiers. This amplifier is used to amplify the voltage difference between two input lines where neither of them is grounded.

5. What is the differential gain of a differential amplifier? What is common-mode gain of a differential amplifier?

Ans. When the two input signals are applied to the two terminals of a differential amplifier, the difference between the two input signals is amplified and the gain of amplifier is known as the differential gain of the differential amplifier.

When two terminals of a differential amplifier are connected to the same input signal, the gain of a differential amplifier is called common-mode gain.

6. What is CMRR?

Ans. *CMRR* is the ratio of differential voltage gain to common-mode voltage gain and it is expressed by

$$CMRR = \frac{A_d}{A_{\text{cm}}}.$$

7. Why is an CMRR of OP-AMP high?

Ans. For an OP-AMP circuit, the output signal should be noise free. Due to high *CMRR*, the common-mode signal, such as noise, can be reduced significantly and the output voltage is directly proportional to the differential input voltage.

8. What is voltage-transfer curve of an OP-AMP?

Ans. The graphical plot between output voltage and input differential voltage when the voltage gain is constant is called voltage-transfer curve of an OP-AMP.

9. Why are open-loop OP-AMP configurations used in non-linear applications?

Ans. If an OP-AMP operates in open-loop configuration, the output signal will be either positive saturation voltage ($+V_{CC}$) or negative saturation voltage ($-V_{CC}$). Therefore, open-loop OP-AMP configurations are used in non-linear applications.

10. Why is input offset voltage applied to an OP-AMP?

Ans. The input offset voltage (V_{IOS}) is applied between inverting and non-inverting terminals of an operational amplifier to balance the amplifier and null the output voltage.

11. What is slew rate?

Ans. Slew rate is defined as the maximum rate of change of output voltage per unit time and it is measured in V/μs.

12. What is the type of negative feedback in a non-inverting OP-AMP circuit?

Ans. Voltage-series feedback is present in a non-inverting OP-AMP circuit.

Multiple-Choice Questions

1. The two input terminals of an operational amplifier are called
   (a) differential and non-differential (b) inverting and non inverting
   (c) positive and negative (d) high and low
2. A differential amplifier has
   (a) four inputs (b) three inputs (c) two inputs (d) one input
3. n OP-AMP circuit uses a feedback, which is called
   (a) open loop (b) inverting feedback
   (c) closed loop (d) non- inverting feedback
4. A differential amplifier has
   (a) common-collector transistor (b) an emitter follower
   (c) common-base transistor (d) an OP-AMP
5. A differential amplifier is used in OP-AMP circuits due to
   (a) high input impedance (b) low input impedance
   (c) high output impedance (d) low output impedance
6. Differential amplifiers are commonly used in
   (a) instrumentation amplifiers (b) buffers
   (c) summing amplifier (d) zero-crossing-detectors
7. The common-mode signal V_C is applied to
   (a) the inverting input terminal (b) the non-inverting input terminal
   (c) both the input terminals (d) all of the above
8. When the two input terminals of a difference amplifier are grounded
   (a) the dc output voltage is zero (b) the ac output voltage is zero
   (c) the output offset voltage exist (d) none of these
9. The *CMRR* of a difference amplifier is
   (a) $CMRR = 20 \log \left| \frac{A_d}{A_C} \right|$ (b) $CMRR = 20 \log \left| \frac{A_C}{A_d} \right| \text{dB}$
   (c) $CMRR = 40 \log \left| \frac{A_C}{A_d} \right| \text{dB}$ (d) $CMRR = 40 \log \left| \frac{A_C}{A_d} \right| \text{dB}$
10. The input offset current of a difference amplifier is
    (a) the difference of the two base currents (b) average of the two collector currents
    (c) the average of the two base currents (d) difference of the two collector currents
11. The input stage and second stage of an OP-AMP are
    (a) differential amplifiers (b) *CE* amplifier
    (c) common collector amplifier (d) power amplifier
12. An operational amplifier IC is an
    (a) analog IC (b) digital IC
    (c) hybrid IC (d) digital as well as analog IC

13. The output voltage can be expressed in terms of *CMRR* is

(a) $A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$ (b) $A_d V_d \left(1 - \frac{1}{\rho}\frac{V_C}{V_d}\right)$

(c) $A_d V_d \left(1 + \frac{1}{\rho}\frac{V_d}{V_C}\right)$ (d) $A_d V_d \left(1 - \frac{1}{\rho}\frac{V_d}{V_C}\right)$

14. In an ideal operational amplifier IC, the transistors are
(a) matched (b) different characters
(c) unmatched (d) none of these

15. The last stage of an operational amplifier is the
(a) output driver (b) differential amplifier
(c) buffer (d) level shifter

16. The rise time and overshoot of an operational amplifier are
(a) 0.3 ns and 6% (b) 0.3 μs and 6% (c) 0.3 ps and 2% (d) 0.3 ps and 6%

17. An ideal OP-AMP has
(a) infinite input impedance (b) zero output impedance
(c) infinite voltage gain (d) All of these

18. The number of pins of the IC741 OP-AMP is
(a) 8 (b) 10 (c) 12 (d) 14

19. The short-circuit output current of IC741 is
(a) 25 A (b) 25 mA (c) 25 pA (d) 25 nA

20. The maximum rate of change of output voltage per unit time is
(a) slew rate (b) *CMRR*
(c) offset voltage (d) supply-voltage rejection ratio

21. The input offset voltage in an OPAMP is due to
(a) mismatch in transistor parameters (b) voltage irregularity
(c) imperfect ground (d) None of these

22. Commercially available OPAMP is
(a) IC 742 (b) IC 723 (c) IC 741 (d) IC 555

23. Assume that the operational amplifier in the circuit shown is ideal. The current *I* flows through 2 kΩ resistance is

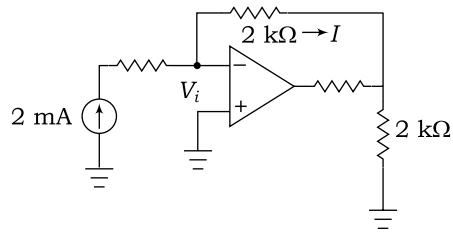


Fig. 6.49

(a) 2 mA (b) –3 mA (c) 1 mA (d) –4 mA

24. The CMRR of an OPAMP is
    (a) much larger than unity (b) zero
    (c) much smaller than unity (d) unity
25. The CMRR of an OPAMP is
    (a) Impedance dependent (b) Voltage dependent
    (c) Frequency dependent (d) Independent of these
26. A differential amplifier has the differential gain of 100. If its CMRR = 240, then the common mode gain is
    (a) 0.24 (b) 0.417 (c) 24000 (d) 1
27. The value of V_o is given for the following circuit by

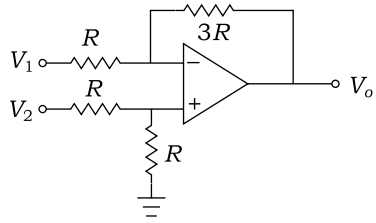


Fig. 6.50

    (a) $-3V_1 + 2V_2$ (b) $-3V_2$ (c) $1.5V_2 - 2.55V_1$ (d) $2V_2 - 3V_1$
28. An ideal OP-AMP has
    (a) infinite common mode gain and zero differential gain
    (b) infinite common mode gain as well as differential gain
    (c) infinite differential gain and zero common mode gain
    (d) None of these
29. Closed loop gain of the amplifier using OPAMP is shown in Fig. 6.51 is

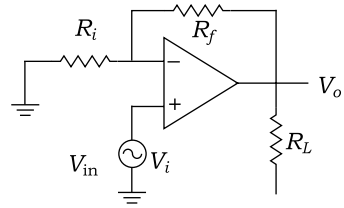


Fig. 6.51

    (a) $1 + \frac{R_f}{R_i}$ (b) $-\frac{R_f}{R_i}$ (c) $\frac{R_f}{R_i}$ (d) $1 - \frac{R_f}{R_i}$
30. Differential amplifier can be used to amplify
    (a) only AC signal (b) only DC signal
    (c) both AC and DC signals (d) None of these

Review Questions

1. Define integrated circuit. What are the types of ICs? Write some applications of ICs.
2. Give a list of advantages and disadvantages of ICs.
3. Explain the operation of difference amplifier with suitable diagram.
4. Define *CMRR*. Derive an expression for *CMRR*.
5. What are the characteristics of an ideal OP-AMP?
6. Draw the schematic block diagram of an OP-AMP and explain briefly.
7. Prove that $V_O = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$.
8. Explain the following:
   (a) Frequency response of an OP-AMP (b) Stability of OP-AMP
   (c) Integrated circuits (d) Virtual ground
9. Define slew rate. How is it calculated for sinusoidal input voltage? What are the different methods to improve slew rate?
10. State specifications of an IC 741.
11. What is virtual ground? Write the difference between ground and virtual ground.
12. Define (a) input offset voltage, (b) input bias current, (c) input offset current, and (d) thermal drift.
13. Draw the frequency response of an operational amplifier and explain its significance.
14. State the characteristics of an ideal operational amplifier. How are the characteristics of a practical operational amplifier different from ideal operational amplifier?
15. Calculate the common-mode gain of a operational amplifier for the following parameters: the differential voltage gain $A_d = 10^5$ and common-mode rejection ratio $CMRR = 2000$.
16. Calculate the output voltage of a differential amplifier for the following parameters:
    $V_1 = 500\ \mu V$, $V_2 = 100\ \mu V$, $A_d = 1000$ and $\rho = CMRR = 20000$
17. The common-mode rejection ratio *CMRR* of an operational amplifier is about 100 dB and difference-mode voltage gain is 10,000. Determine common-mode gain.
18. The input signals of a differential amplifier are $V_1 = 150\ \mu V$ and $V_2 = -50\ \mu V$.
    (a) When the common-mode rejection ratio is 50, determine the output voltage of a differential amplifier.
    (b) If $\rho = 20{,}000$, find the output voltage.
    Assume difference-mode gain $A_d = 20{,}000$.
19. The difference amplifier as shown in Fig. 6.52 has the following parameters:
    $R_C = 5\ k\Omega$, $R_E = 200\ k\Omega$, $R_S = 5\ k\Omega$
    The transistor parameters are as follows:
    $h_{ie} = 5\ k\Omega$, $h_{fe} = 100$, $h_{re} = 0$, $h_{oe} = 0$
    When the amplifier is operated with common-mode signal of 250 mV and difference signal of 250 mV, determine output voltage and *CMRR*.

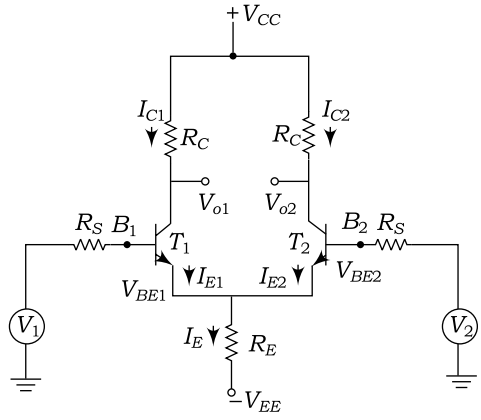


Fig. 6.52

20. Assume input offset current (I_{IOS}) = 100 nA and input offset voltage (V_{IOS}) = 0 and $A = 10^5$.
    (a) What is the differential input voltage?
    (b) What is the output offset voltage? Assume R_S = 1 kΩ

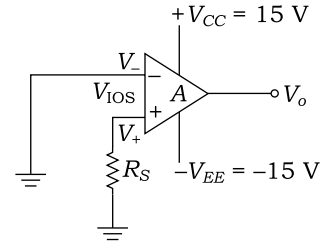


Fig. 6.53

21. The base currents of a differential amplifier are I_{B1} = 50 μA and I_{B2} = 30 μA.
    (a) What is the input bias current?
    (b) Calculate the input offset current.
22. The input base currents of a differential amplifier are I_{B1} = 200 nA and I_{B2} = 10 nA.
    (a) Determine the input bias current and the input offset current.
    (b) When $A = 10^5$, calculate the output offset voltage.
    Assume R_S = 1.5 kΩ.
23. The output voltage of an operational amplifier changes by 12 V within 4 μs. Calculate the slew rate.
24. The output voltage of an operational amplifier is shown in Fig. 6.54 When input voltage is a square wave 8 V peak-to-peak amplitude with 1 MHz frequency. What is the slew rate of the operational amplifier?

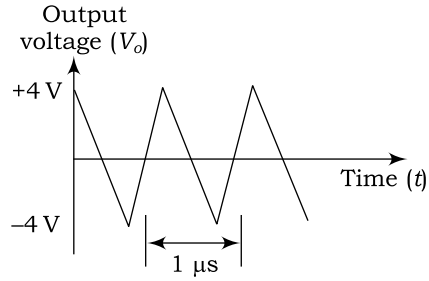


Fig. 6.54

25. An IC741C OP-AMP is used as an inverting amplifier with a gain of 60. The input voltage is sinusoidal with a maximum amplitude of 20 mV. What is the maximum frequency of the input voltage?

26. An IC741C OP-AMP is used as an inverting amplifier with a gain of 50. The voltage gain vs frequency response is flat up to 20 kHz. What is the maximum peak-to-peak input signal that can be applied without distorting the output voltage?
27. An operational amplifier has a slew rate of 0.5 V/μs. If the peak output voltage is 12 V, what is the maximum frequency at which the operational amplifier operates properly?
28. An operational amplifier has a slew rate of 0.55 V/ μs. How much time will it take to change the output voltage from 0 V to 12 V?
29. The charging current of a 200 pF capacitor is 100 μA. What is the slew rate of the operational amplifier?
30. An operational amplifier has a slew rate of about 0. 5 V/μs and used as an inverting amplifier with a gain of 50. The voltage gain vs frequency curve of an operational amplifier up to 30 kHz is flat. What is the maximum peak to peak input signal that can be applied to the operational amplifier without distorting the output voltage?
31. Figure 6.55 shows an operational amplifier circuit. The operational amplifier has slew rate about 0. 5 V/μs, gain is 9, output saturation voltage levels are ±10 V, and maximum frequency is 50 kHz.
    (a) Determine the maximum peak amplitude of the output sinusoidal signal at 50 kHz for the undistorted output voltage.
    (b) Calculate the values of R_1 and R_2.

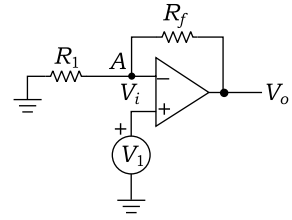


Fig. 6.55

32. (a) Draw the circuit diagram of a differential amplifier using BJT and obtain an expression for its differential voltage gain
    (b) What is the significance of CMRR in differential amplifiers?
33. Enlist the characteristics of an ideal OPAMP
34. Draw a block diagram showing different stages of an OPAMP.
35. Explain the concept of virtual ground.
36. Write short notes on the following:
    (a) Constant Current Source (b) Current Mirror
37. Explain the operation of a basic differential amplifier.
38. Describe the steps for building an Instrumentation Amplifier starting from the basic differential amplifier.
39. What are the advantages of differential amplifier?
40. What is voltage follower?
41. Establish the relationship between slew rate and full power bandwidth.

ANSWERS

Multiple-Choice Questions

1. (b)	2. (c)	3. (b)	4. (b)	5. (a)	6. (a)	7. (c)
8. (c)	9. (a)	10. (c)	11. (a)	12. (a)	13. (a)	14. (a)
15. (a)	16. (b)	17. (d)	18. (a)	19. (b)	20. (a)	21. (a)
22. (c)	23. (a)	24. (a)	25. (d)	26. (b)	27. (a)	28. (c)
29. (a)	30. (c)					

CHAPTER

7

Applications of Operational Amplifiers

7.1 INTRODUCTION

The basic operation of an operational amplifier, its dc and ac characteristics, limitations and different configuration have been explained in Chapter 6. Generally, an operational amplifier is a linear device and its output is directly proportional to the input. As per transfer characteristics, the practical operational amplifier operates as a linear device over a certain range of input signal and it also behaves as a nonlinear device over some other region. Hence, applications of operational amplifiers can be divided as linear applications and nonlinear applications.

1. Linear Applications

In linear applications of operational amplifiers, the output signal is related with the input signal linearly. Some of the linear applications of operational amplifiers are as follows:

- Adder or summing
- Subtractor or difference
- Voltage to current converter
- Current to voltage converter
- Instrumentation amplifiers
- Analog computation
- Power amplifier

2. Nonlinear Applications

In nonlinear applications, the relationship between input and output signals of operational amplifiers is nonlinear. Some of the nonlinear applications of operational amplifiers are as follows:

- Comparator
- Logarithmic and Antilogarithmic amplifiers
- Multiplier
- Divider
- Integrator
- Differentiator

- Rectifier
- Pear detector
- Clipper
- Clamper
- Sample-and-hold circuits

In this chapter, adder or summing, subtractor or difference, voltage to current converter, current to voltage converter, instrumentation amplifiers, analog computation, integrator, differentiator, comparator, Schmitt trigger, precision rectifier logarithmic and antilogarithmic amplifiers, multipliers and dividers are discussed elaborately with examples.

7.2 INVERTING AMPLIFIER

Figure 7.1 shows the circuit diagram of an inverting amplifier using operational amplifier. In this circuit

- Input voltage V_1 is applied to the inverting terminal through a series resistance R_1
- Output voltage V_o is fed back to the inverting terminal through the feedback resistance R_f
- The non-inverting terminal of the operational amplifier is grounded

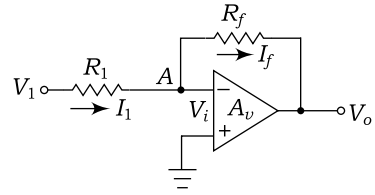


Fig. 7.1 Inverting amplifier

For circuit analysis, assume $A_v = \infty$, $R_i = \infty$ and $R_o = 0$. The input differential voltage V_i is approximately zero and the operational amplifier does not draw any current. Therefore, current flowing through R_1 is same as current flowing through R_f. As $V_i = 0$, the inverting terminal A is virtually grounded.

The current flow through R_1 is

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1} \quad \text{as } V_A = 0 \tag{7.1}$$

The current flow through R_f is

$$I_f = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f} = -\frac{V_o}{R_f} \quad \text{as } V_A = 0 \tag{7.2}$$

Since $I_1 = I_f$, we can write

$$\frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

or

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

or

$$V_o = -\frac{R_f}{R_1} V_1 = -A_{vf} V_1 \quad \text{Assume } A_{vf} = \frac{R_f}{R_1} \tag{7.3}$$

A_{vf} is the overall loop gain of the amplifier and its negative value indicates the phase inversion of output signal. Hence, the circuit acts as an inverting amplifier. If a sine wave signal is applied at V_1 then we get a amplified sine wave with a gain of A_{vf} and 180° phase shift from input signal.

This circuit can be used as *sign changer* when the gain is one ($A_{vf} = 1$). If the ratio $\left|\frac{V_o}{V_1}\right|$ is greater than unity (one), the circuit is called *scale changer*.

Example 7.1 Design an operational amplifier circuit with a gain of –20. Assume input resistance is equal to 5 kΩ.

Sol. As gain of operational amplifier is negative, an inverting amplifier has to be designed.

The gain of inverting amplifier is

$$-\frac{R_f}{R_1} = -20$$

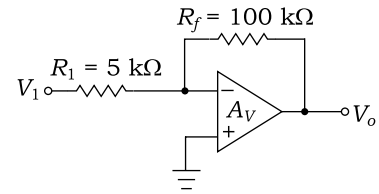


Fig. 7.2

Since R_1 = 5 kΩ, R_f = 20 × 5 kΩ = 100 kΩ. Figure 7.2 shows the operational amplifier with a gain –20.

Example 7.2 An inverting amplifier is shown in Fig. 7.3. Determine (a) I_1, (b) V_O, (c) I_L, (d) I_O. Assume input voltage V_1 is equal to 1 V.

Sol. The current I_1 is

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1} = \frac{1}{5 \times 10^3} \text{A} = 0.2 \text{ mA}$$

The output voltage is equal to

$$V_O = -\frac{R_f}{R_1} V_1 = -\frac{20}{5} \times 1 \text{ V} = -4 \text{ V}$$

The load current I_L is

$$I_L = \frac{V_O}{R_L} = \frac{4}{10 \times 10^3} = 0.4 \text{ mA}$$

The current I_O is equal to

$$I_O = I_1 + I_L = (0.2 + 0.4) \text{ mA} = 0.6 \text{ mA}$$

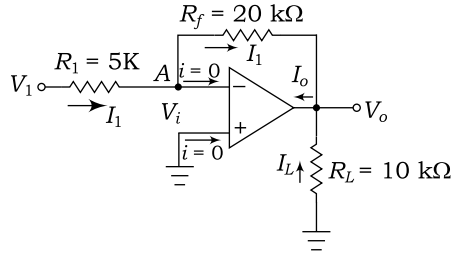


Fig. 7.3

7.3 NON-INVERTING AMPLIFIER

The circuit diagram of the non-inverting amplifier using operational amplifier is illustrated in Fig. 7.4. In this circuit,

- Input voltage V_1 is applied to the non-inverting terminal of the amplifier.
- The feedback resistance R_f is connected between the output voltage terminal and inverting input terminal and resistance R_1 is connected between inverting terminal and ground.

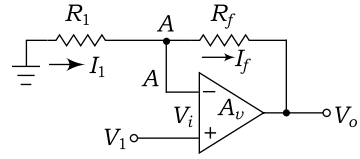


Fig. 7.4 Non-inverting amplifier

Assume $V_i = 0$

The potential at A is $V_A = V_1$

The current flow through R_1 is

$$I_1 = \frac{0 - V_A}{R_1} = -\frac{V_A}{R_1} = -\frac{V_A}{R_1} \tag{7.4}$$

The current flow through R_f is

$$I_f = \frac{V_A - V_o}{R_f} = \frac{V_1 - V_o}{R_f} \tag{7.5}$$

As $I_1 = I_f$, we can write

$$-\frac{V_1}{R_1} = \frac{V_1 - V_o}{R_f}$$

or
$$\frac{V_o}{R_f} = \frac{V_1}{R_f} + \frac{V_1}{R_1} = \left(\frac{1}{R_f} + \frac{1}{R_1}\right) V_1$$

or
$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$$

or
$$\frac{V_o}{V_1} = \left(1 + \frac{R_f}{R_1}\right) \tag{7.6}$$

It is clear from the above expression that the output signal has same sign as input signal and there is no phase shift between input voltage and output voltage. Therefore, output is not inverted. The required amplifier gain can be achieved by selecting proper value of R_f and R_1.

Example 7.3 Design an non-inverting operational amplifier circuit with a gain of 10. Assume input resistance is equal to 10 kΩ.

Sol. As gain of operational amplifier is positive, a non-inverting amplifier has to be designed.

The gain of non-inverting amplifier is

$$1 + \frac{R_f}{R_1} = 10$$

As R_1 = 10 kΩ, $R_f = 9R_1 = 9 \times 10\text{k}\Omega = 90$ kΩ. Figure 7.5 shows the operational amplifier with a gain 10.

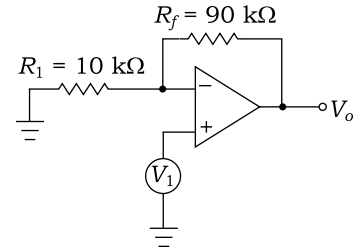


Fig. 7.5

Example 7.4 Figure 7.6 shows the non-inverting amplifier, where R_1 = 10 kΩ, R_f = 100 kΩ and V_1 = 1 V.

Determine (a) V_O, (b) gain, (c) I_1, (d) load current I_L, and (d) output current I_O.

Sol. Since V_1 = 1 V, the potential at A will be V_A = 1 V (as V_i = 0)

The output voltage is equal to

$$V_O = \left(1 + \frac{R_f}{R_1}\right) V_1 = \left(1 + \frac{100}{10}\right) \times 1\text{V} = 11\text{V}$$

The gain is $\frac{V_O}{V_1} = \frac{11}{1} = 11$

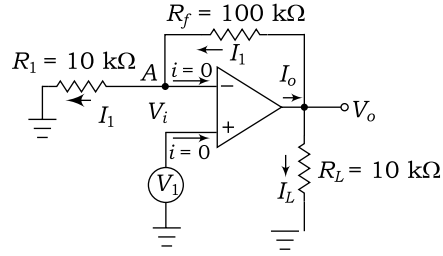


Fig. 7.6

The current I_1 is

$$I_1 = \frac{V_A}{R_1} = \frac{1}{10 \times 10^3} \text{ A} = 0.1 \text{ mA}$$

The load current I_L is

$$I_L = \frac{V_O}{R_L} = \frac{11}{10 \times 10^3} = 1.1 \text{ mA}$$

The current I_O is equal to

$$I_O = I_1 + I_L = (0.1 + 1.1) \text{ mA} = 1.2 \text{ mA}$$

7.4 VOLTAGE FOLLOWER

The voltage follower is a circuit in which the output voltage follows the input voltage. Figure 7.7 shows a typical voltage-follower circuit. As output voltage follows the input voltage, V_O will be equal to V_{in}.

The potential at the node A is V_{in}. As $V_i = 0$, $V_A = V_B = V_{in}$. It is clear from Fig. 7.7 that the output terminal is directly connected with the node B. The potential at node B is $V_B = V_O$.

Therefore, we can write, $V_O = V_{in}$.

As output voltage is equal to input voltage, the voltage gain of the voltage follower circuit is unity. This circuit is also known as *buffer circuit* with high input impedance and zero output impedance.

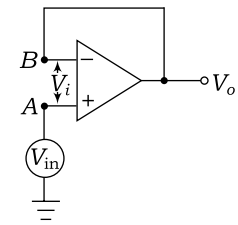


Fig. 7.7 Voltage follower

7.5 ADDER OR SUMMING AMPLIFIER

Operation amplifiers can be used as an adder circuit whose output is the sum of two or more input signals. Such a circuit is called *summing amplifier*. There are two types of summing amplifiers such as inverting summing amplifier and non-inverting summing amplifier. In this section, both inverting and non-inverting summing amplifiers are explained.

7.5.1 Inverting Summing Amplifier

Figure 7.8 shows an inverting summing amplifier with two inputs V_1 and V_2, two input resistors R_1 and R_2, and a feedback resistor R_f. Assume the operational amplifier is an ideal one. Therefore, $A_v = \infty$, $R_i = \infty$ and $V_i = 0$.

Hence, the inverting input terminal has ground potential as a virtual ground ($V_A = 0$)

The current flow through R_1 is

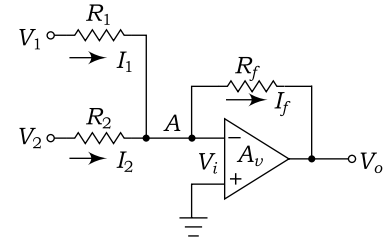


Fig. 7.8 Inverting summing amplifier

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1} \tag{7.7}$$

The current flow through R_2 is

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2 - 0}{R_2} = \frac{V_2}{R_2} \tag{7.8}$$

The current flow through R_f is

$$I_f = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f} = -\frac{V_o}{R_f} \tag{7.9}$$

Applying KCL law at the node A, we can write

$$I_1 + I_2 = I_f$$

or
$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = -\frac{V_o}{R_f}$$

or
$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right) \tag{7.10}$$

Therefore, the output voltage is an inverted weighted sum of two inputs. If $R_1 = R_2 = R_f = R$, the output voltage can be expressed as

$$V_o = -(V_1 + V_2)$$

Hence, the circuit acts as an inverting adder circuit.

When $R_1 = R_2 = 2R_f$, output voltage will be $V_o = -\left(\frac{V_1 + V_2}{2}\right)$

Thus the output voltage is the *average* of the two input voltages V_1 and V_2.

7.5.2 Non-inverting Summing Amplifier

A non-inverting summing amplifier with two inputs V_1 and V_2, two input resistors R_1 and R_2, and a feedback resistor R_f is shown in Fig. 7.9. Assume the voltage at inverting (–) input terminal is V_A and the voltage at non-inverting (+) input terminal is also V_A.

Apply KCL law at the node A, we can write

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} = 0$$

or
$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{V_A}{R_1} + \frac{V_A}{R_2} = \left(\frac{1}{R_1} + \frac{1}{R_2}\right)V_A$$

or
$$V_A = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}} \tag{7.11}$$

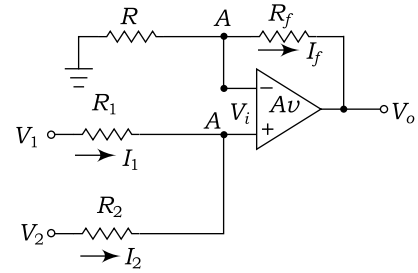


Fig. 7.9 Non-inverting summing amplifier

The non-inverting operational amplifier with resistors R_f and R has output voltage

$$V_o = \left(1 + \frac{R_f}{R}\right)V_A$$

Then, the output voltage can be expressed as

$$V_o = \left(1 + \frac{R_f}{R}\right) \times \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}} \tag{7.12}$$

The above expression is a non-inverted weighted sum of inputs.

If $R_1 = R_2 = R = R_f$, the output voltage is equal to $V_o = V_1 + V_2$.

Example 7.5 Figure 7.10 shows an adder circuit with $V_1 = 1$ V, $V_2 = 2$ V and $V_3 = -2$ V. Determine the output voltage V_O. Assume $R_1 = 2$ kΩ, $R_2 = 1$ kΩ, $R_3 = 2$ kΩ and $R_f = 4.7$ kΩ.

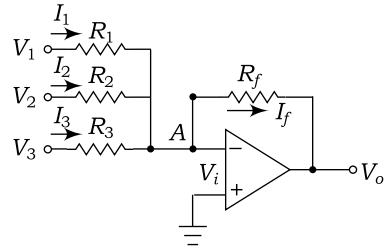


Fig. 7.10

Sol. The output voltage of inverting amplifier is

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

$$= -\left(\frac{4.7}{2}\times 1 + \frac{4.7}{1}\times 2 + \frac{4.7}{2}(-2).\right)\text{V}$$

$$= -7.05 \text{ V}$$

Example 7.6 Figure 7.11 shows an operational amplifier circuit with $R_1 = 1$ kΩ, $R_2 = 2$ kΩ, and $R_f = 10$ kΩ. Derive the output voltage V_O expression in terms of V_1 and V_2.

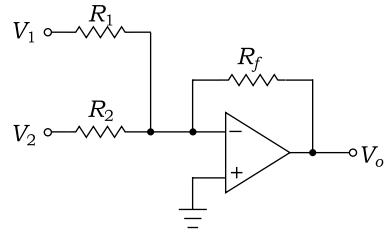


Fig. 7.11

Sol. The output voltage of the amplifier can be expressed as

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right)$$

$$= -\left(\frac{10\times 10^3}{1\times 10^3}\times V_1 + \frac{10\times 10^3}{2\times 10^3}\times V_2\right)\text{V} = -(10V_1 + 5V_2)$$

Example 7.7 Implement the equation $V_O = -2V_1 - 7V_2$ using an operational amplifier circuit. Assume minimum value of resistance is 5 kΩ.

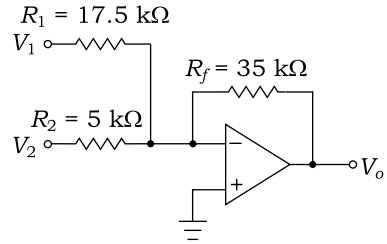


Fig. 7.12

Sol. The output voltage of the amplifier circuit with two input voltages V_1 and V_2 as shown in Fig. 7.12 can be expressed as

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right) = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$$

The given output voltage is $V_O = -2V_1 - 7V_2$

Therefore, $\frac{R_f}{R_1} = 2$ and $\frac{R_f}{R_2} = 7$

Assume the value of resistance R_2 is 5 kΩ

Then feedback resistance is equal to $R_f = 7R_2 = 7 \times 5$ kΩ = 35 kΩ

The resistance of R_1 will be $R_1 = \frac{R_f}{2} = \frac{35}{2}\text{k}\Omega = 17.5$ kΩ

Example 7.8 Figure 7.13 shows an amplifier circuit. Determine the output voltage V_O and currents I_L and I_O.

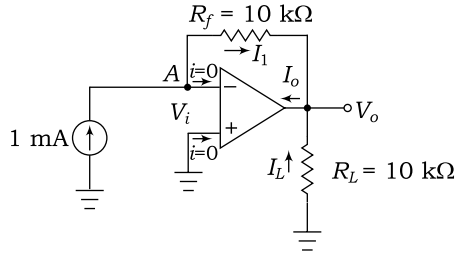


Fig. 7.13

Sol. In an ideal operational amplifier, input impedance is infinite and the input current, i is equal to zero. Hence, the source current 1 mA flows through $R_f = 10$ kΩ.

The output voltage of the amplifier circuit is

$$V_O = -I_f R_f = -1 \times 10^{-3} \times 10 \times 10^3 = -10 \text{ V}$$

The load current is

$$I_L = \frac{V_O}{R_L} = \frac{10}{10 \times 10^3} = 1 \text{ mA}$$

The current I_O is equal to

$$I_O = I_f + I_L = (1 + 1) = 2 \text{ mA}$$

Example 7.9 An operational amplifier circuit is shown in Fig. 7.14. Determine the output voltage V_O and current flows through R_1, R_2, R_3 and R_f. Assume $V_1 = 2$ V, $V_2 = -2$ and $V_3 = 3$ V

Sol. The current flows through R_1 is

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1} = \frac{2}{5 \times 10^3} \text{A} = 0.4 \text{ mA}$$

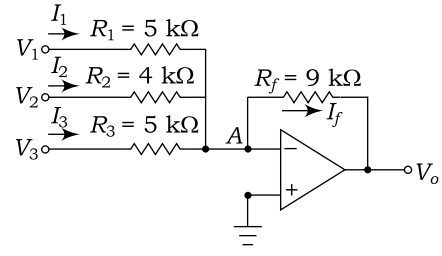


Fig. 7.14

The current flows through R_2 is

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2 - 0}{R_2} = \frac{V_2}{R_2} = \frac{-2}{4 \times 10^3} \text{A} = -0.5 \text{ mA}$$

The current flows through R_3 is

$$I_3 = \frac{V_3 - V_A}{R_3} = \frac{V_3 - 0}{R_3} = \frac{V_3}{R_3} = \frac{3}{5 \times 10^3} \text{A} = 0.6 \text{ mA}$$

The current flows through R_f is

$$I_1 + I_2 + I_3 = I_f = (0.4 - 0.5 + 0.6) \text{ mA} = 0.5 \text{ mA}$$

The output voltage is equal to

$$V_O = -I_f R_f = -0.5 \times 10^{-3} \times 9 \times 10^3 \text{ V} = -4.5 \text{ V}$$

7.6 SUBTRACTOR OR DIFFERENCE AMPLIFIER

A difference amplifier is a circuit that amplifies the difference between two signals. It is also called a *differential amplifier* or a subtractor. Figure 7.15 shows a typical difference amplifier. In this circuit, the voltage V_1 is applied to operational amplifier –A (OP-AMP-A) with a gain = 1. Output of OP-AMP-*A* is V_{o1} and V_2 voltages are applied to OP-AMP-B with a gain = 1. Then output voltage of OP-AMP-B will be the difference between V_1 and V_2.

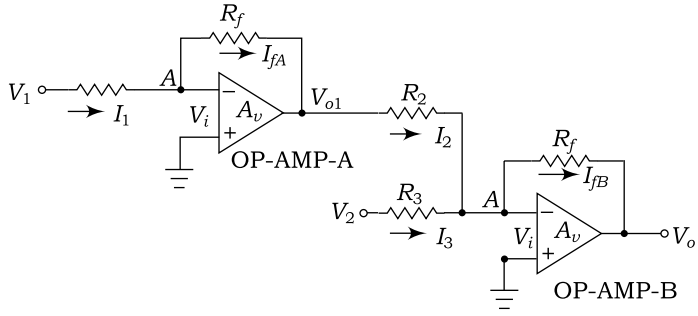


Fig. 7.15 Difference amplifier using two OP-AMP

The output voltage of OP-AMP-A is

$$V_{o1} = -\frac{R_f}{R_1} V_1 \tag{7.13}$$

If $R_f = R_1$, $\quad V_{o1} = -V_1$

The output voltage of OP-AMP-B is V_o

$$V = -\frac{R_f}{R_2} V_{o1} - \frac{R_f}{R_3} V_2 \tag{7.14}$$

If $R_f = R_2 = R_3$, $\quad V_o = V_{o1} - V_2$

As $V_{o1} = -V_1$, we can write $V_o = -(-V_1) - V_2 = V_1 - V_2$ (7.15)

7.7 DIFFERENCE AMPLIFIER WITH ONE OP-AMP

A typical differential amplifier with one operational amplifier is shown in Fig. 7.16. Assume the differential voltage between inverting (–) and non-inverting (+) terminals of operational amplifier is zero. Potential at A and potential at B are same, so that $V_A = V_B$.

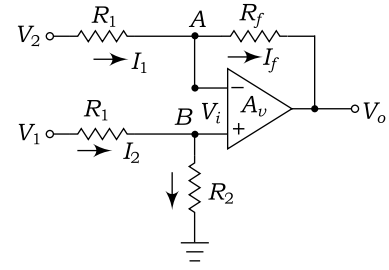


Fig. 7.16 Difference amplifier using one OP-AMP

The nodal equation at the node B is

$$\frac{V_1 - V_B}{R_1} = \frac{V_B - 0}{R_2}$$

or $$\frac{V_1}{R_1} = \frac{V_B}{R_1} + \frac{V_B}{R_2} = V_B\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = V_B \frac{R_1 + R_2}{R_1 R_2}$$

or $$V_B = V_1 \frac{R_2}{R_1 + R_2} \tag{7.16}$$

or $$V_A = V_1 \frac{R_2}{R_1 + R_2} \text{ as } V_A = V_B \tag{7.17}$$

Applying KCL at node A we can write

$$I_1 = I_f$$

or
$$\frac{V_2 - V_A}{R_1} = \frac{V_A - V_o}{R_f}$$

or
$$\frac{R_f}{R_1}V_2 - \frac{R_f}{R_1}V_A - V_A = -V_o$$

or
$$V_o = \left(1 + \frac{R_f}{R_1}\right)V_A - \frac{R_f}{R_1}V_2$$
$$= \left(1 + \frac{R_f}{R_1}\right)\frac{R_2}{R_1 + R_2}V_1 - \frac{R_f}{R_1}V_2 \quad (7.18)$$

If $R_f = R_2$, the output voltage $V_o = \frac{R_2}{R_1}V_1 - \frac{R_2}{R_1}V_2 = \frac{R_2}{R_1}(V_1 - V_2)$ (7.19)

This circuit is very useful to detect a very small difference between two signals as the gain $\frac{R_2}{R_1}$ can be considered a large value. For example, when R_2 = 100 kΩ and R_1 = 1 kΩ and gain is 100, the difference potential $(V_1 - V_2)$ will be amplified by 100 times.

7.8 ADDER-SUBTRACTOR

Operational amplifiers can also be used to perform addition and subtraction simultaneously. Figure 7.17 shows the adder cum subtractor circuit. To determine the output voltage, usually superposition theorem is used. Therefore, to find the output voltage V_O, the input voltages V_1, V_2, V_3 and V_4 are applied separately. When one voltage is applied, other voltages are zero. For example, when V_1 is present in the circuit, the input voltages V_2, V_3 and V_4 are at ground potential. Then output voltage is V_{o1}. Figure 7.18 shows the circuit diagram for this case and its equivalent is depicted in Fig. 7.19.

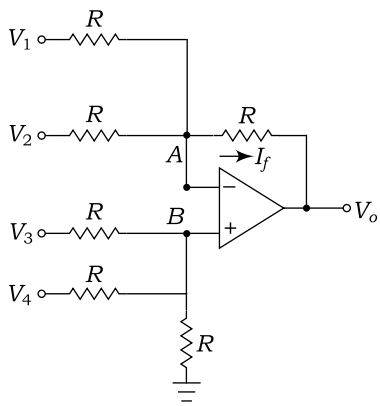


Fig. 7.17 Adder-subtractor circuit

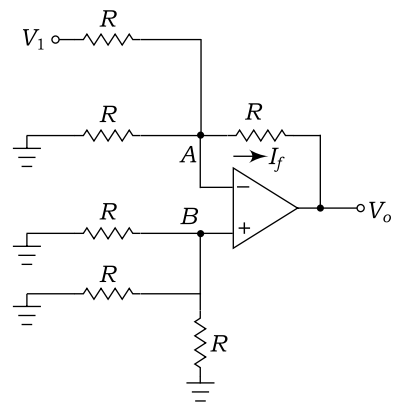


Fig. 7.18 Adder-subtractor circuit with $V_2 = V_3 = V_4 = 0$

The output voltage

$$V_{o1} = -\frac{R}{\frac{R}{2}}\frac{V_1}{2} = -V_1 \quad \text{as } R_f = R \quad (7.20)$$

Similarly the output voltage for input voltage V_2 is

$$V_{o2} = -V_2. \tag{7.21}$$

Figure 7.20 shows the circuit diagram when V_3 is present and other voltages are zero. This circuit behaves as a non-inverting amplifier. The voltage at the node B is

$$V_B = \frac{\frac{R}{2}}{R + \frac{R}{2}} V_3 = \frac{V_3}{3} \tag{7.22}$$

As the voltage difference between A and B is zero, $V_A = V_B$.

Hence, $V_A = V_B = \dfrac{V_3}{3}$

The output voltage due to the input voltage V_3 is

$$V_{o3} = \left(1 + \frac{R}{\frac{R}{2}}\right) V_A = 3V_A = 3\frac{V_3}{3} = V_3 \tag{7.23}$$

In the same way, the output voltage due to the input voltage V_4 is $V_{o4} = V_4$.

After that, applying the superposition theorem, we can find the output voltage V_o due to all four input voltages as given below:

$$\begin{aligned} V_o &= V_{o1} + V_{o2} + V_{o3} + V_{o4} \\ &= -V_1 - V_2 + V_3 + V_4 \\ &= (V_3 + V_4) - (V_1 + V_2) \end{aligned} \tag{7.24}$$

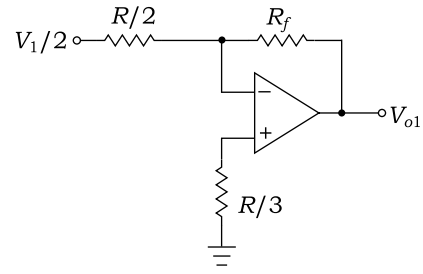


Fig. 7.19 Equivalent circuit of Fig. 7.18

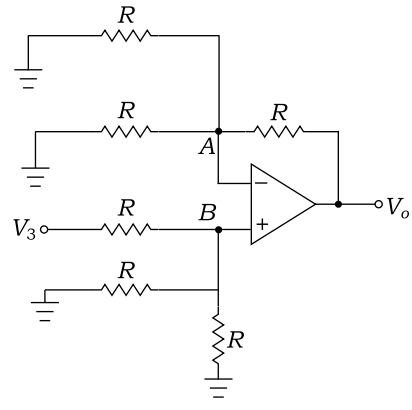


Fig. 7.20 Adder-subtractor circuit with $V_1 = V_2 = V_4 = 0$

Example 7.10 Determine the output voltage V_O for the operational amplifier circuit as shown in Fig. 7.21. Assume $V_1 = 2$ V and $V_2 = -1$ V.

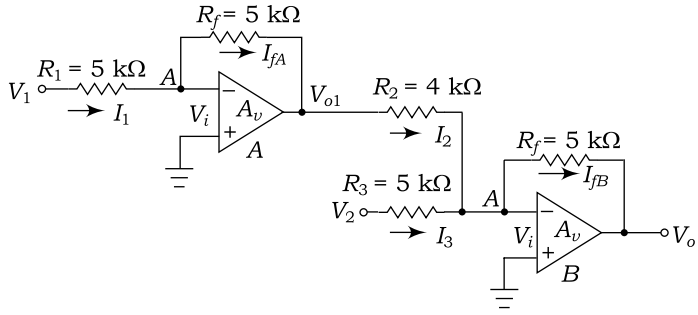


Fig. 7.21

Sol. The output voltage of operational amplifier –A is V_{O1}

$$V_{O1} = -\frac{R_f}{R_1} V_1 = -\frac{5}{5} \times 2 = -2\,\text{V}$$

The output voltage of operational amplifier –B is V_O

$$V_O = -\frac{R_f}{R_2}V_{O1} - \frac{R_f}{R_3}V_2 = -\frac{5}{4}\times(-2) - \frac{5}{5}\times(-1)\text{ V} = 3.5\text{ V}$$

Example 7.11 Derive the expression of output voltage V_O for the operational amplifier circuit as shown in Fig. 7.22. Assume $R_1 = 10\text{ k}\Omega$, $R_2 = 5\text{ k}\Omega$, $R_3 = 10\text{ k}\Omega$ and $R_f = 10\text{ k}\Omega$.

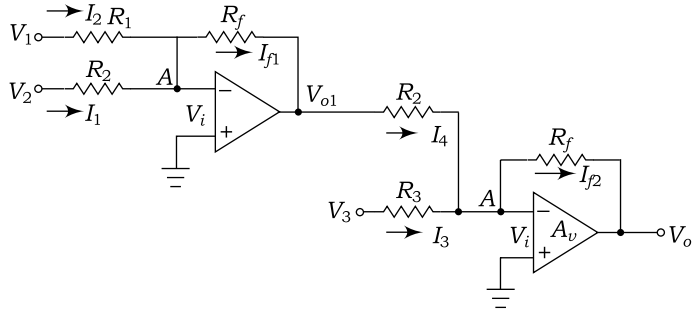


Fig. 7.22

Sol. The output voltage of the first operational amplifier is V_{O1}

$$V_{o1} = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$$
$$= -\frac{10}{10}v_1 - \frac{10}{5}V_2 = -V_1 - 2V_2$$

The output voltage of the second operational amplifier is V_O

$$V_O = -\frac{R_f}{R_2}V_{O1} - \frac{R_f}{R_3}V_3$$
$$= -\frac{10}{5}V_{O1} - \frac{10}{10}V_3$$
$$= -2V_{O1} - V_3 = -2(-V_1 - 2V_2) - V_3$$
$$= 2V_1 + 4V_2 - V_3$$

Example 7.12 Figure 7.23 shows an operational amplifier circuit. Determine the current I_f and the output voltage V_O when $V_1 = 4$ V and $V_2 = 5$ V.

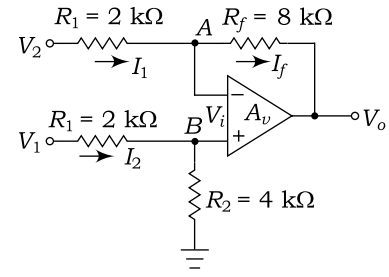


Fig. 7.23

Sol. The voltage at the point *B* is

$$V_B = \frac{R_2}{R_1 + R_2}V_1 = \frac{4}{4+2}\times 4\text{ V} = 2.66\text{ V}$$

In an ideal operational amplifier, the inverting terminal voltage V_A is equal to the non-inverting terminal voltage V_B. Hence, $V_A = V_B = 2.66$ V.

The current I_1 is

$$I_1 = \frac{V_2 - V_A}{R_1} = \frac{5 - 2.66}{2 \times 10^3} \text{A} = 1.17 \text{ mA}$$

As the current input to inverting terminal is zero, $I_f = I_1$

Therefore, $I_f = 1.17$ mA,

the output voltage of the operational amplifier is V_O.

As $I_f = \frac{V_A - V_o}{R_f}$, the output voltage is $V_O = -I_f R_f + V_A$

$$= (-1.17 \times 10^{-3} \times 8 \times 10^3 + 2.66) \text{ V} = (-9.36 + 2.66)\text{V} = 6.7 \text{ V}$$

Example 7.13 Determine the common-mode rejection ratio (*CMRR*) of the differential amplifier as shown in Fig. 7.24.

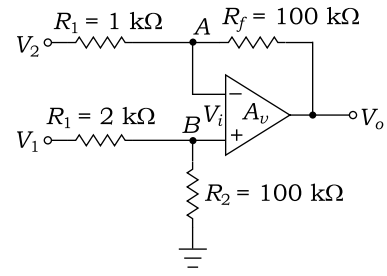


Fig. 7.24

Sol. The voltage at the point *B* is

$$V_B = \frac{R_2}{R_1 + R_2} V_1 = \frac{100}{100 + 2} V_1 = \frac{100}{102} V_1$$

In an ideal operational amplifier, the inverting terminal voltage V_A is equal to the non-inverting terminal voltage V_B. Hence, $V_A = V_B = \frac{100}{102} V_1$.

The current through the resistance R_f is

$$I_f = \frac{V_A - V_O}{R_f} = \frac{V_2 - V_A}{R_1}$$

Therefore, $$V_A - V_O = \frac{R_f}{R_1}(V_2 - V_A) = \frac{100}{1}(V_2 - V_A) = 100V_2 - 100V_A$$

Then output voltage is equal to

$$V_O = V_A + 100V_A - 100V_2 = 101V_A - 100V_2$$

After substituting V_A, we get

$$V_O = 101 \times \frac{100}{102} V_1 - 100V_2 = 99.01V_1 - 100V_2$$

Assume $V_1 = V_C + \frac{V_d}{2}$ and $V_2 = V_C - \frac{V_d}{2}$

The output voltage in terms of V_C and V_d is

$$V_O = 99.019V_1 - 100V_2$$

$$= 99.019\left(V_C + \frac{V_d}{2}\right) - 100\left(V_C - \frac{V_d}{2}\right)$$

$$= (99.019 - 100)\, V_C + (45.5095 + 50)\, V_d = -0.981\, V_C + 95.5095\, V_d$$

This output voltage can also be expressed as

$$V_o = A_C V_C + A_d V_d$$

Therefore, $A_C = 0.981$ and $A_d = 95.5095$

The common-mode rejection ratio is

$$CMRR = \frac{A_d}{A_C} = \frac{95.5095}{0.981} = 97.35$$

Example 7.14 Figure 7.25 shows an operational amplifier circuit. Determine the output voltage V_O.

Sol. If the input voltages $V_3 = V_4 = 0$, the output voltage of operational amplifier circuit is

$$V_{O12} = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$$

$$= -\frac{100}{1}V_1 - \frac{100}{2}V_2 = -100V_1 - 50V_2$$

When input voltages $V_1 = V_2 = 0$, the equivalent circuit is shown in Fig. 7.26 while V_3 is present in the circuit and $V_4 = 0$.

The potential at the point B is

$$V_B = \frac{R_5 \parallel R_4}{R_5 \parallel R_4 + R_3}V_3 = \frac{2 \parallel 2}{2 \parallel 2 + 1}V_3 = \frac{V_3}{2}$$

As $R_5 \parallel R_4 = 2 \parallel 2 = 1\ \text{k}\Omega$

Then output voltage is

$$V_{O3} = \left(1 + \frac{R_f}{R_1 \parallel R_2}\right)V_A = \left(1 + \frac{100}{1 \parallel 2}\right)V_B \quad \text{As } V_A = V_B$$

Since $R_1 \parallel R_2 = 1 \parallel 2\ \text{k}\Omega = 0.67\ \text{k}\Omega$ and $V_B = \frac{V_3}{2}$, the output voltage is equal to

$$V_{O3} = \left(1 + \frac{100}{0.67}\right)\frac{V_3}{2} = 75.126V_3$$

Similarly, when input voltages $V_1 = V_2 = 0$, the equivalent circuit is shown in Fig. 7.27 while V_4 is present in the circuit and $V_3 = 0$.

The potential at the point B is

$$V_B = \frac{R_5 \parallel R_3}{R_5 \parallel R_3 + R_4}V_4$$

$$= \frac{2 \parallel 1}{2 \parallel 1 + 2}V_4 = \frac{0.67}{0.67 + 2}V_4 = 0.250V_4$$

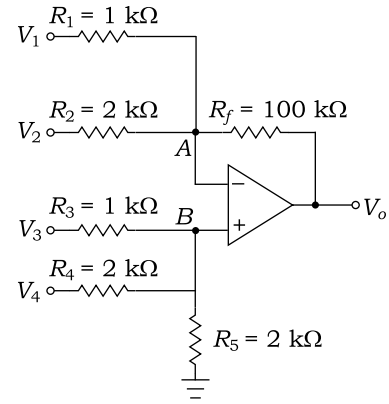


Fig. 7.25

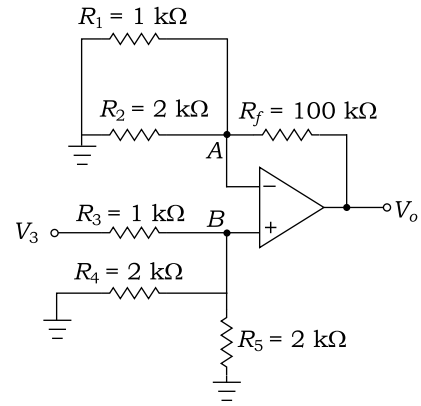


Fig. 7.26

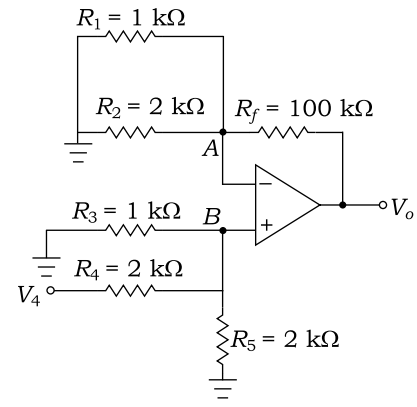


Fig. 7.27

As $R_5 \| R_3 = 2 \| 1 = 0.67\ \text{k}\Omega$

Then output voltage is

$$V_{O4} = \left(1 + \frac{R_f}{R_1 \| R_2}\right) V_A = \left(1 + \frac{100}{1 \| 2}\right) V_B \quad \text{As } V_A = V_B$$

Since $R_1 \| R_2 = 1 \| 2\ \text{k}\Omega = 0.67\ \text{k}\Omega$ and $V_B = 0.250\ V_4$, the output voltage is equal to

$$V_{O3} = \left(1 + \frac{100}{0.67}\right) \times 0.250 V_4 = 37.563\ V_4$$

Then output voltage V_O is equal to

$$V_O = V_{O12} + V_{O3} + V_{O4}$$
$$= -100\ V_1 - 50\ V_2 + 75.126\ V_3 + 37.563\ V_4$$

7.9 VOLTAGE-TO-CURRENT CONVERTER

Voltage-to-current converters are commonly used for analog systems, meters and relays, etc. Figure 7.28 shows the circuit diagram of a voltage-to-current converter.

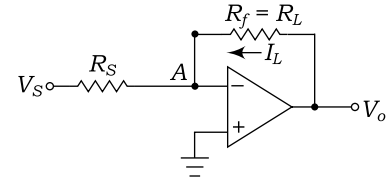


Fig. 7.28 Voltage-to-current converter

The current flow through the resistance R_L is equal to

$$\frac{V_S - V_A}{R_S} = \frac{V_A - V_o}{R_L} = -I_L \tag{7.25}$$

Since $V_A = 0$, the above equation can be written as $\frac{V_S - 0}{R_S} = \frac{0 - V_o}{R_L} = -I_L$

or $$\frac{V_S}{R_S} = -\frac{V_o}{R_L} = -I_L$$

or $$I_L = -\frac{V_S}{R_S} \tag{7.26}$$

It is clear from the above expression that the output current is independent of the load resistance R_L and the circuit acts as a constant current source as V_S is constant. When one end of the load is grounded and the load current is controlled by input voltage, a different circuit will be used for a voltage to current converter. Figure 7.29 shows the voltage-to-current converter when the load is not floating type.

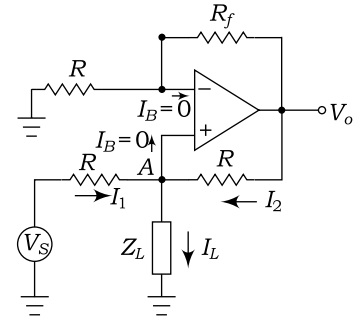


Fig. 7.29

Applying KCL at the node A, we get $I_1 + I_2 = I_L$ (7.27)

where, current $I_1 = \frac{V_S - V_A}{R}$, current $I_2 = \frac{V_o - V_A}{R}$ and current $I_L = \frac{V_A}{Z_L}$

After substituting the value of I_1, I_2 and I_L, in Eq. (7.28) we obtain

$$\frac{V_S - V_A}{R} + \frac{V_o - V_A}{R} = I_L$$

or $$\frac{V_S + V_o - 2V_A}{R} = I_L$$

or $$V_A = \frac{V_S + V_o - I_L R}{2} \tag{7.28a}$$

Since the operational amplifier operates in non-inverting mode, the gain of the circuit is

$$\left(1 + \frac{R_f}{R}\right) \tag{7.29}$$

If $R_f = R$, the gain of the circuit will be 2 and the output voltage can be expressed as

$$V_o = \left(1 + \frac{R_f}{R}\right) V_A = 2V_A$$

or $$V_o = 2V_A = 2\left(\frac{V_S + V_o - I_L R}{2}\right) \quad \text{as } V_A = (V_s + V_o - I_L R)/2$$

or $$V_o = V_S + V_o - I_L R \tag{7.30}$$

Therefore, $V_s = I_L R$ and load current will be

$$I_L = \frac{V_S}{R} \tag{7.31}$$

This equation states that the load current depends on the input voltage V_s and resistor R only.

7.10 CURRENT-TO-VOLTAGE CONVERTER

The output signal of photocells, photodiodes and photovoltaic cells is current and its magnitude is directly proportional to the intensity of light or incident radiant energy. The current output from these devices can be converted to voltage by using a voltage-to-current converter. Then voltage will be measured to indicate the intensity of light or radiant energy incident on the photodevices.

The current-to-voltage (I to V) converter is shown in Fig. 7.30. As inverting terminal is virtually ground, current flow through R_s is zero and I_s current flow through the feedback resistance R_f.

Hence, the output voltage can be expressed as $V_o = -I_s R_f$. The I to V converters are commonly used in Digital-to-Analog Converter (DAC) as DAC output is current signal which is proportional to the digital input.

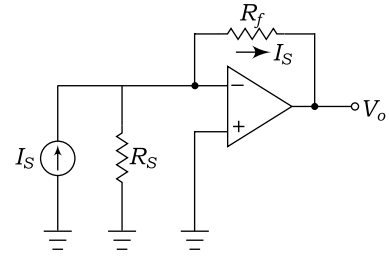


Fig. 7.30 Current to voltage converter

7.11 INTEGRATOR

7.11.1 Inverting Integrator

When the feedback resistance R_f is interchanged with a capacitor in an ideal inverting mode operational amplifier, the circuit works as an integrator. Figure 7.31 shows an integrator circuit where input voltage is V_{in}.

The current flows through R_1 is

$$I_1 = \frac{V_{in} - V_A}{R_1} \tag{7.32}$$

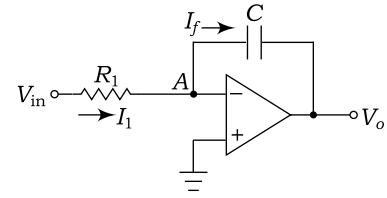


Fig. 7.31 Integrator

As the non-inverting terminal is at ground potential, the node A will also be at ground potential or virtual ground. Then, $V_A = 0$.

So that $$I_1 = \frac{V_{\text{in}}}{R_1}$$

The current flows through the capacitor is

$$I_f = C\frac{d(V_A - V_o)}{dt} = -C\frac{dV_o}{dt} \tag{7.33}$$

Applying KCL at the node A, we get

$$I_1 = I_f$$

or $$\frac{V_{\text{in}}}{R_1} = -C\frac{dV_o}{dt}$$

or $$\frac{dV_o}{dt} = -\frac{1}{R_1 C}V_{\text{in}} \tag{7.34}$$

After integrating both sides, we get

$$\int dV_o = -\frac{1}{R_1 C}\int V_{\text{in}}\,dt$$

So, $$V_o(t) = -\frac{1}{R_1 C}\int_0^t V_{\text{in}}\,dt + V_0(0) \tag{7.35}$$

where, $V_o(0)$ is the initial output voltage. Therefore, this circuit provides an output signal which is the integral of the input voltage.

7.11.2 Non-inverting Integrator

Figure 7.32 shows the circuit diagram of a non-inverting integrator. In this circuit, the negative input terminal is connected to ground through R. The input voltage V_{in} is applied through the resistor R. The voltage at non-inverting terminal is same as inverting terminal voltage which is equal to V_A.

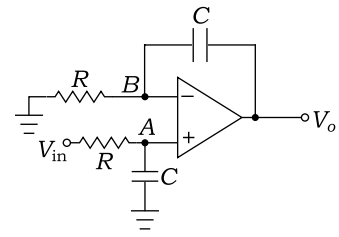


Fig. 7.32 Non-inverting integrator

Applying KCL at the node A, we can write

$$\frac{V_{\text{in}} - V_A}{R} = \frac{V_A - 0}{\frac{1}{sC}}$$

or $$V_{\text{in}} - V_A = sCRV_A$$

or $$V_{\text{in}} = (1 + sCR)V_A \tag{7.36}$$

Applying KCL at the node B, we get

$$\frac{V_o - V_B}{\frac{1}{sC}} = \frac{V_B - 0}{R}$$

or $$V_o - V_B = \frac{1}{sC}\frac{V_B}{R} = \frac{V_B}{sCR} \tag{7.37}$$

or $$V_o = V_B + \frac{V_B}{sCR} = \left(1 + \frac{1}{sCR}\right)V_B = \frac{sCR+1}{sCR}V_B$$

As $V_A = V_B$, we can write

$$V_o = \frac{sCR+1}{sCR}V_A$$

or $$V_O = \frac{sCR+1}{sCR}\frac{V_{\text{in}}}{sCR+1} = \frac{V_{\text{in}}}{sCR} \quad \text{as} \quad V_A = \frac{V_{\text{in}}}{1+sCR} \tag{7.38}$$

Since $\frac{1}{s} = \int$, we can write $V_o = \frac{1}{CR}\int V_{\text{in}}\,dt$

7.11.3 Practical Integrator

There are two sources of error at output voltage in an ideal integrator as given below:

1. A very small dc offset voltage is present at the operational amplifier input.
2. Input bias current flow through the feedback capacitor

The above two effects will be integrated with respect of time and generate a continuously rising output voltage till the operational amplifier saturates. Therefore, this ideal integrator circuit can be used as an integrator over a time range and before starting operation, the circuit must be recycled. Recycling can limit the output error voltage within an acceptable range. The bias current can be minimised by increasing C_f and simultaneously reducing the value of R_1. The limitations of an ideal integrator can be minimised if the feedback capacitor C_f is shunted by resistance R_f as depicted in Fig. 7.33.

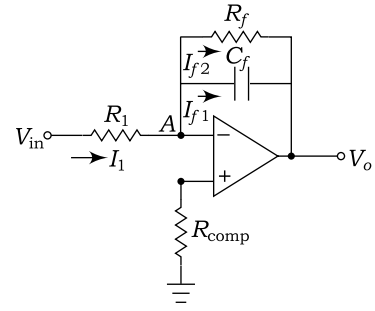


Fig. 7.33 Practical integrator

The parallel combination of R_f and C_f works like a practical capacitor, and the circuit is also known as *lossy integrator*. The R_f resistor limits the low-frequency gain operational amplifier to $\frac{R_f}{R_1}$. The resistance R_{comp} is used to reduce the error due to bias current.

The equivalent impedance is equal to

$$Z_{\text{eq}} = R_f \| C_f$$

$$= \frac{R_f \frac{1}{sC_f}}{R_f + \frac{1}{sC_f}} = \frac{\frac{R_f}{sC_f}}{\frac{sC_fR_f+1}{sC_f}}$$

$$= \frac{R_f}{1+sC_fR_f} \tag{7.39}$$

Applying KCL at the node A, we get

$$\frac{V_{\text{in}} - V_A}{R_1} = \frac{V_A - V_o}{Z_{\text{eq}}}$$

or $$\frac{V_{\text{in}} - 0}{R_1} = \frac{0 - V_o}{Z_{\text{eq}}}$$

As the node A is virtual ground, $V_A = 0$

or $$\frac{V_{\text{in}}}{R_1} = -\frac{V_o}{Z_{\text{eq}}} \tag{7.40}$$

The output voltage can be expressed as

$$V_o = -Z_{\text{eq}} \frac{V_{\text{in}}}{R_1} \tag{7.41}$$

After substituting the value of Z_{eq} in the above equation, we get

$$V_o = -\frac{R_f}{1 + sC_f R_f} \frac{V_{\text{in}}}{R_1} \qquad \text{As } Z_{\text{eq}} = \frac{R_f}{1 + sC_f R_f}$$

$$= -\frac{R_f}{R_1} \frac{1}{1 + sC_f R_f} V_{\text{in}}$$

$$= -\frac{R_f}{R_1 + sC_f R_f R_1} V_{\text{in}}$$

$$= -\frac{1}{\frac{R_1}{R_f} + sC_f R_1} V_{\text{in}} \tag{7.42}$$

If R_f is very large, $\frac{R_1}{R_f}$ can be neglected and the lossy integrator behaves as an ideal integrator. Then output voltage is equal to

$$V_O = -\frac{1}{sC_f R_1} V_{\text{in}}$$

As $\frac{1}{s} = \int dt$, we can write $V_o = -\frac{1}{R_1 C_f} \int V_{\text{in}} dt$ (7.43)

After substituting $s = j\omega$, the magnitude of the gain of lossy integrator can be computed as

$$|A| = \left| \frac{V_o}{V_{\text{in}}} \right| = \frac{\frac{R_f}{R_1}}{\sqrt{1 + \omega^2 {C_f}^2 {R_f}^2}} \tag{7.44}$$

Practical integrators are commonly used in

- Analog computation
- Ramp waveform generator
- ADC (Analog-to-Digital converter)
- Different wave-shaping circuits

7.11.4 Summing Integrator

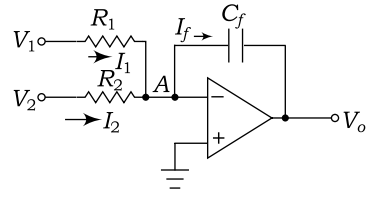


Fig. 7.34 Summing integrator

The summing integrator amplifier can be used to integrate more than one input signal. A typical two-input summing integral circuits is given in Fig. 7.34, where V_1 and V_2 are inputs.

Assume inverting terminal of operation amplifier is at virtual ground so that, $V_A = 0$.

Applying KCL at the node *A,* we get

$$I_1 + I_2 = I_f$$

After substituting the value of the currents, we obtain

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} = \frac{V_A - V_o}{\frac{1}{sC_f}}$$

or

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = -sC_f V_o$$

or

$$V_O = -\frac{1}{sC_f R_1} V_1 - \frac{1}{sC_f R_2} V_2 \tag{7.45}$$

As $\frac{1}{s} = \int dt$, we can write

$$V_o = -\frac{1}{R_1 C_f}\int V_1 dt - \frac{1}{R_2 C_f}\int V_2 dt$$

$$= -\frac{1}{C_f}\int\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)dt \tag{7.46}$$

It is clear from the above expression that the output voltage is sum of integration of two input signals. In the same way, more than two voltages will also be integrated.

Example 7.15 Derive the output voltage of the integrating operational amplifier circuit as shown in Fig. 7.35. Assume the operational amplifier is an ideal one.

Sol. The current flows through the resistance R_1 is

$$I_1 = \frac{V_1}{R_1} = \frac{V_1}{10}\text{mA}$$

The current flows through the resistance R_2 is

$$I_2 = \frac{V_2}{R_2} = \frac{V_2}{5}\text{mA}$$

The current flows through the resistance R_3 is

$$I_3 = \frac{V_3}{R_3} = \frac{V_3}{10}\text{mA}$$

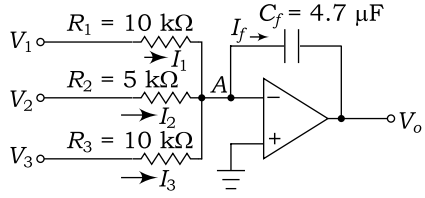


Fig. 7.35

Then current flows through the capacitor C_f is

$$I_f = I_1 + I_2 + I_3$$
$$= \frac{V_1}{10} + \frac{V_2}{5} + \frac{V_3}{10}\text{mA}$$

The output voltage will be

$$V_o = -\frac{1}{R_1 C_f}\int V_1 dt - \frac{1}{R_2 C_f}\int V_2 dt - \frac{1}{R_3 C_f}\int V_3 dt$$
$$= -\frac{1}{C_f}\int\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)dt \qquad \text{as } C_f = 4.7\ \mu\text{F}$$
$$= -\frac{1}{4.7\times10^{-6}}\int\left(\frac{V_1}{10} + \frac{V_2}{5} + \frac{V_3}{10}\right)\times10^{-3}\,dt$$
$$= -\int(21.276V_1 + 42.552V_2 + 21.276V_3)\,dt$$

Example 7.16 Prove that the operational amplifier circuit as shown in Fig. 7.36 is an integrator. Assume the operational amplifier is an ideal one.

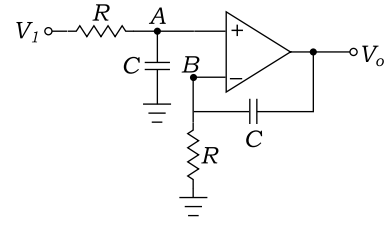


Fig. 7.36

Sol. The voltage at the node *A* is

$$V_A = \frac{\frac{1}{sC}}{R + \frac{1}{sC}}V_1 = \frac{1}{1 + sCR}V_1$$

As operational amplifier is an ideal one, the voltage at node *B* is equal to the voltage at node *A*.

Hence, $V_B = V_A = \frac{1}{1 + sCR}V_1$

The output voltage can be expressed as

$$V_O = \left(1 + \frac{\frac{1}{sC}}{R}\right)V_A = \frac{1 + sCR}{sCR}V_A$$

After substituting the value of V_A, we get

$$V_O = \frac{1 + sCR}{sCR}V_A = \frac{1 + sCR}{sCR}\frac{1}{1 + sCR}V_1 = \frac{1}{sCR}V_1$$

As $\frac{1}{s} = \int dt$, we can write

$$V_o = \frac{1}{RC}\int V_1 dt$$

Hence, it is proved that the operational amplifier circuit as shown in Fig. 7.36 is an integrator.

Example 7.17 Prove that the output voltage of Fig. 7.37 is $V_O = \frac{2}{CR}\int V_1 dt$

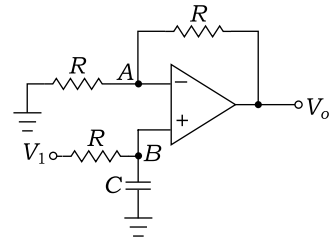


Fig. 7.37

Sol. The potential at the node B is

$$V_B = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_1 = \frac{1}{1 + sCR} V_1$$

Since operational amplifier is an ideal one, the voltage at the node A is equal to that at the node B.

Therefore, $$V_B = V_A = \frac{1}{1 + sCR} V_1$$

The output voltage can be expressed as

$$V_O = \left(1 + \frac{R}{R}\right) V_A = 2V_A$$

After substituting the value of V_A, we get

$$V_O = \frac{2}{1 + sCR} V_1 = \frac{2}{sCR} V_1 \quad \text{assuming } sCR >> 1$$

As $\frac{1}{s} = \int dt$, we can write

$$V_o = \frac{2}{CR}\int V_1 dt$$

Example 7.18 In an integrator circuit as shown in Fig. 7.38, the value of RC is 1 second. Find out the output voltage at t = 1 second, t = 2 seconds and t = 3 seconds when input voltage is 2 V.

Sol. Given RC = 1 second and V_{in} = 2 V

The output voltage of the integrator is

$$V_o = -\frac{1}{RC}\int V_{in} dt = -\frac{1}{1}\int 2dt \text{ V} = -\int 2dt \text{ V}$$

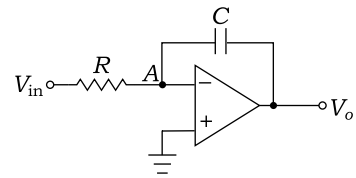


Fig. 7.38

The output voltage at t = 1 second

$$V_O = -\int_0^1 2dt = -2 \text{ V}$$

The output voltage at t = 2 seconds is

$$V_O = -\int_0^2 2dt = -4 \text{ V}$$

The output voltage at t = 3 seconds is

$$V_O = -\int_0^3 2dt = -6 \text{ V}$$

Example 7.19 Figure 7.39 shows an integrator circuit. Find out the output voltage when input voltage is 2 sin 1000 πt and show the output voltage waveform.

Sol. The input voltage is $V_{in} = 2 \sin 1000\ \pi t$

The output voltage is

$$V_o = -\frac{1}{RC}\int V_{in} dt$$

$$= -\frac{1}{5\times10^3\times1\times10^{-6}}\int (2\sin 1000\pi t)dt$$

$$= -400\int \sin 1000\pi t dt$$

$$= -400\times\frac{1}{1000\pi}\times(-\cos 1000\pi t) = 0.1273\cos 1000\pi t \text{ V}$$

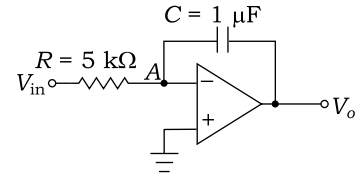


Fig. 7.39

The waveform of input voltage and output voltage are shown in Fig. 7.40(a) and (b).

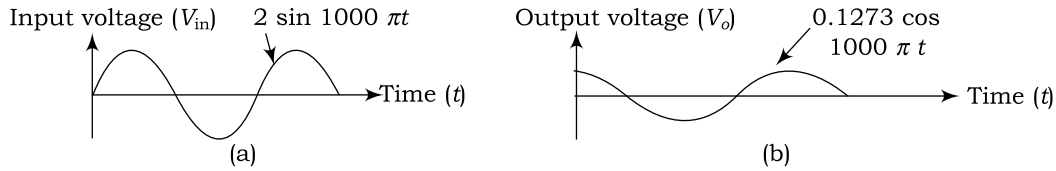


Fig. 7.40

Example 7.20 When a step voltage input is applied to an integrator circuit from 0 to 0.5 ms as shown in Fig. 7.41, find out the output voltage at $t = 0.5$ millisecond.

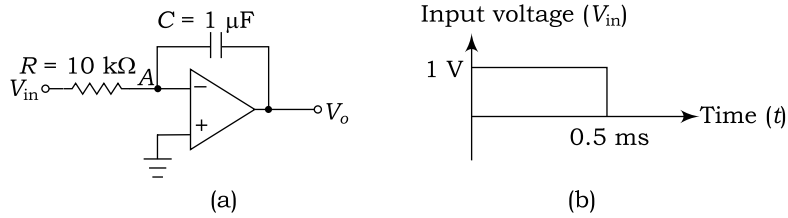


Fig. 7.41

Sol. The output voltage is

$$V_o = -\frac{1}{RC}\int V_{in} dt$$

$$= -\frac{1}{10\times10^3\times1\times10^{-6}}\int_0^{0.5\text{ms}} 1dt \text{ V}$$

$$= -100\left[t\right]_0^{0.5\text{ms}} \text{ V} = -100\times0.5\times10^{-3} \text{ V} = -50 \text{ mV}$$

Example 7.21 If a square wave is applied as input voltage to an integrator circuit as shown in Fig. 7.42, find out the output voltage. Assume $RC = 0.1$ second.

Sol. During $t = 0$ to $t = 1$ ms, the input voltage, V_{in} is 1 V.

At $t = 1$ ms, the output voltage is

$$V_o = -\frac{1}{RC}\int V_{in} dt$$

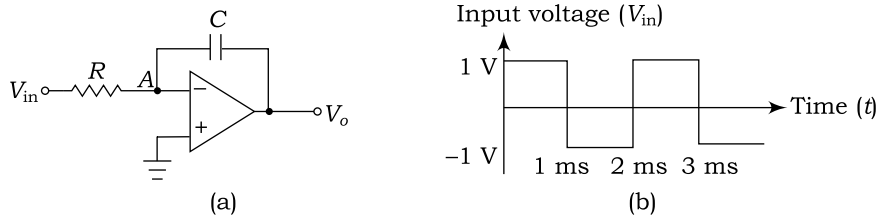


Fig. 7.42

$$= -\frac{1}{0.1}\int_0^{1ms} 1dt \text{ V} \qquad \text{as } RC = 0.1 \text{ second}$$

$$= -10[t]_0^{1ms} \text{ V} = -10 \times 1 \times 10^{-3} \text{ V} = -10 \text{ mV}$$

During $t = 1$ ms to $t = 2$ ms, the input voltage, V_{in} is –1 V.

At $t = 2$ ms, the output voltage is

$$V_o = -\frac{1}{RC}\int V_{in} dt$$

$$= -\frac{1}{0.1}\int_{1ms}^{2ms} (-1)dt + V_o(t = 1\text{ms}) \text{ V} \qquad \text{as } RC = 0.1 \text{ second}$$

$$= 10[t]_{1ms}^{2ms} + V_o(t = 1ms) \text{ V} = 10 \times 1 \times 10^{-3} \text{ V} - 10 \text{ mV} = 0 \text{ V}$$

The output voltage waveform will be triangular in nature as shown in Fig. 7.43.

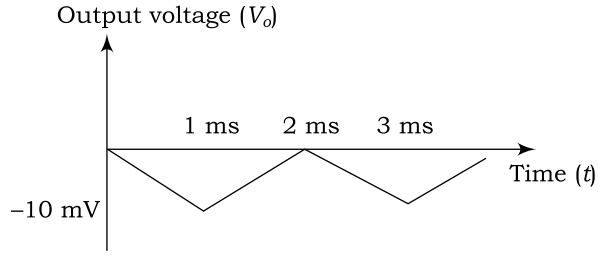


Fig. 7.43

7.12 DIFFERENTIATOR

When the positions of resistor R and capacitor C in the integrator are interchanged, the integrator works as a *differentiator*. The circuit diagram of a differentiator is shown in Fig. 7.44. The potential at A is V_A and it is zero as inverting terminal of operational amplifier is virtually ground.

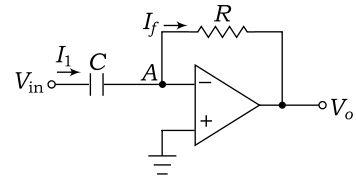


Fig. 7.44 Differentiator

Applying KCL at the node A, we get

$$I_1 = I_f$$

or

$$C\frac{d(V_{in} - V_A)}{dt} = \frac{V_A - V_o}{R}$$

or $$C\frac{dV_{\text{in}}}{dt} = -\frac{V_o}{R}$$

or $$V_o = -CR\frac{dV_{\text{in}}}{dt} \tag{7.47}$$

Hence, the output voltage is proportional to the derivative of the input voltage V_{in}. When $V_{\text{in}} = \sin \omega t$ is applied at the input terminal of the differentiator, the output is $V_o = -CR\omega \cos \omega t$. It means that output voltage proportionately increases linearly with signal frequency. Due to high-frequency signal, a frequency noise component greatly enhances signal distortions. Therefore, differentials are usually avoided in high-frequency operations. At low frequency, the output voltage amplitude increases linearly with frequency, which leads to use the differentiator as frequency to voltage converter.

7.12.1 Practical Differentiator

The limitations of a differentiator circuit are stability and noise problems at high frequency. These limitations can be eliminated by using practical differentiation. Figure 7.45 shows the circuit diagram of a practical differentiator. In this circuit, the resistance R_1 in series with a capacitor and capacitor C_f is connected in parallel with resistance R_f. The R_{comp} is used for bias compensation.

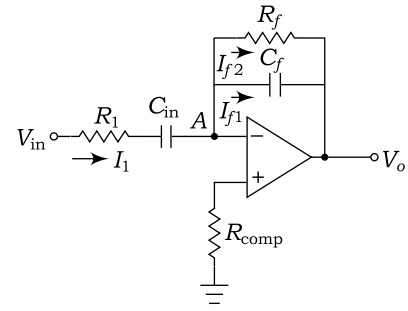


Fig. 7.45 Practical differentiator

As R_1 and C_1 are connected in series, the equivalent impedance is equal to

$$Z_1 = R_1 + \frac{1}{sC_{\text{in}}} = \frac{sC_{\text{in}}R_1 + 1}{sC_{\text{in}}} \tag{7.48}$$

Since R_f and C_f are connected in parallel, the equivalent impedance is

$$Z_2 = \frac{R_f \dfrac{1}{sC_f}}{R_f + \dfrac{1}{sC_f}} = \frac{R_f}{1 + sR_fC_f} \tag{7.49}$$

As the point A is virtual ground, $V_A = 0$

Applying KCL at the node A, we can write

$$\frac{V_{\text{in}} - V_A}{Z_1} = \frac{V_A - V_o}{Z_2}$$

or $$\frac{V_{\text{in}}}{Z_1} = \frac{-V_o}{Z_2}$$

or $$\frac{V_{\text{in}}}{\dfrac{sC_{\text{in}}R_1 + 1}{sC_{\text{in}}}} = -\frac{V_o}{\dfrac{R_f}{1 + sR_fC_f}}$$

or $$V_o = -\frac{R_f}{1 + sR_fC_f}\frac{sC_{\text{in}}}{sC_{\text{in}}R_1 + 1}V_{\text{in}}$$

or $$V_o = -\frac{sR_fC_{\text{in}}}{(1+sR_fC_f)(1+sC_{\text{in}}R_1)}V_{\text{in}}$$

If $R_fC_f = R_1C_{\text{in}}$, the output voltage can be expressed as

$$V_o = -\frac{sR_fC_{\text{in}}}{(1+sC_{\text{in}}R_1)^2}V_{\text{in}} \tag{7.50}$$

As the time constant R_fC_{in} is greater than R_fC_f or R_1C_{in}, the above equation becomes

$$V_o = -sR_fC_1V_{\text{in}} \tag{7.51}$$

Since $s = \frac{d}{dt}$, the output voltage can be expressed as $V_o = -R_fC_1\frac{d(V_{\text{in}})}{dt}$.

Hence, the output voltage is R_fC_1 times the differentiation of the input voltage. Practical differentiators are used in

- Rate-of-change detector in FM demodulations
- Different wave-shaping circuits

7.12.2 Summing Differentiator

The summing differentiator circuit is shown in Fig. 7.46.

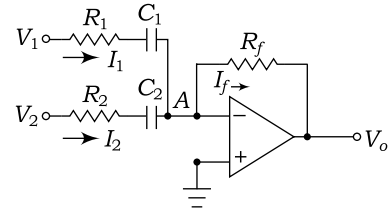


Fig. 7.46 Summing differentiator

Apply KCL at the node A, we can write

$$I_1 + I_2 = I_f$$

After substituting the values of currents I_1, I_2 and I_f, we get

$$\frac{V_1 - V_A}{Z_1} + \frac{V_2 - V_A}{Z_2} = \frac{V_A - V_o}{R_f} \tag{7.52}$$

Assume inverting terminal is virtually ground. So $V_A = 0$

Then $$\frac{V_1}{Z_1} + \frac{V_2}{Z_2} = -\frac{V_o}{R_f} \tag{7.53}$$

The equivalent impedance Z_1 is

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{sC_1R_1 + 1}{sC_1} \tag{7.54}$$

The equivalent impedance Z_2 is

$$Z_2 = R_2 + \frac{1}{sC_2} = \frac{sC_2R_2 + 1}{sC_2} \tag{7.55}$$

After substituting the values of currents Z_1 and Z_2 in Eq. (7.53), we obtain

$$\frac{V_1}{\frac{sC_1R_1+1}{sC_1}} + \frac{V_2}{\frac{sC_2R_2+1}{sC_2}} = -\frac{V_o}{R_f}$$

or $$\frac{sC_1}{1+sC_1R_1}V_1 + \frac{sC_2}{1+sC_2R_2}V_2 = -\frac{V_o}{R_f}$$

or $$V_o = -\frac{sC_1R_f}{1+sC_1R_1}V_1 - \frac{sC_2R_f}{1+sC_2R_2}V_2$$

If $C_1R_f >> C_1R_1$ and $C_2R_f >> C_2R_2$, we can get

$$V_o = -sC_1R_fV_1 - sC_2R_fV_2$$

As $s = \frac{d}{dt}$, the output voltage can be expressed as

$$V_o = -C_1R_f\frac{dV_1}{dt} - C_2R_f\frac{dV_2}{dt} \tag{7.56}$$

The above equation states that the output is the sum of the differentiation of input voltages V_1 and V_2.

Example 7.22 Figure 7.47 shows a differentiation circuit. Draw the output voltage waveform when input voltage is $V_{in} = 2 \sin 100\,\pi t$. Assume C$R$ = 0.01 second.

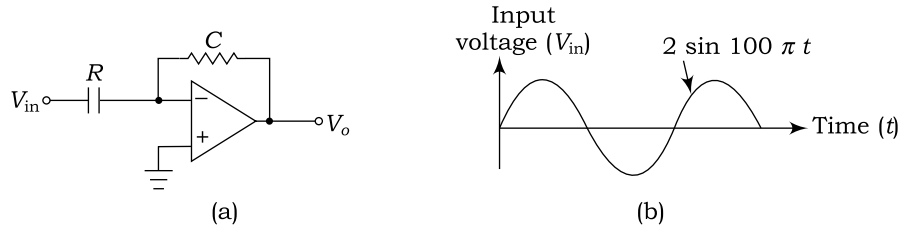


Fig. 7.47

Sol. The output voltage of the differentiation circuit is

$$\begin{aligned} V_o &= -CR\frac{dV_{in}}{dt} \\ &= -0.01\frac{d}{dt}(2\sin 100\pi t) \\ &= -0.01 \times 2 \times 100\pi \cos 100\pi t \\ &= -6.28\cos 100\pi t \end{aligned}$$

The output voltage waveform is shown in Fig. 7.48.

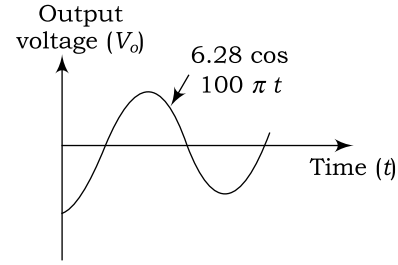


Fig. 7.48

Example 7.23 Figure 7.49(a) shows a differentiation circuit. When a square-wave input voltage as shown in Fig. 7.49(b) is applied to the differentiation circuit, what will be the output voltage waveform?

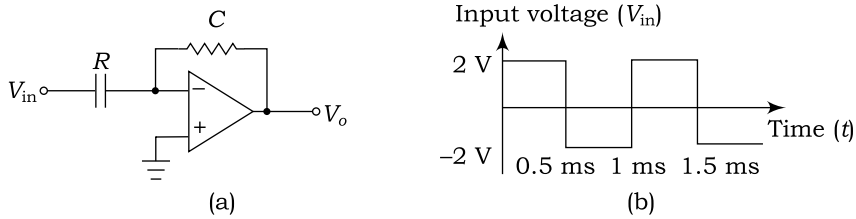


Fig. 7.49

Sol. The square-wave input voltage has 2 V peak voltage and 1 kHz frequency. When the square-wave input voltage is applied to the differentiation circuit, positive and negative spikes or impulse signals will be generated at output. The magnitude of the spikes will be about ± $V_{saturation}$ that is approximately ±13 V or ±15 V.

When the input voltage changes from –2 V to +2 V, impulse signal will be negative. While the input voltage changes from +2 V to –2 V, impulse signal will be positive. During the time periods for which input voltage is constant at either +2 V or –2 V, there will be no output voltage as the differentiated of input voltage is zero.

Figure 7.50(b) shows the output voltage waveform with respect to input voltage.

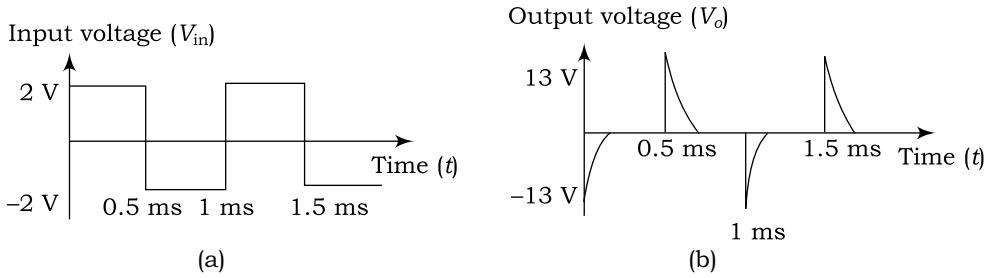


Fig. 7.50

7.13 LOGARITHMIC AMPLIFIER

The *log and antilog amplifiers* are nonlinear circuits where the output voltage is proportional to the exponent or logarithm of input voltage. Usually, to perform multiplication and division in electronic circuits, addition and subtraction of logs are used. The other applications of log amplifiers are powers, roots, compression, decompression, true rms detection and process control, etc. There are two basic circuits of logarithmic amplifiers such as

- Diode-connected transistor
- Transdiode

However, the most common log amplifiers are the diode-connected transistor log amplifiers. In this section, basic operation of a log amplifier is discussed.

In a logarithmic amplifier, the output voltage is directly proportional to the logarithm of the input voltage.

So
$$V_o \propto \log V_i \tag{7.57}$$

Where, V_i is the input voltage and V_o is output voltage

When the linear operational amplifier is combined with a nonlinear device such as a diode or transistor, a logarithmic amplifier circuit can be achieved.

Figure 7.51 shows a logarithmic amplifier. In this circuit, collector (C) and emitter (E) terminals are connected between inverting terminal and output. The base of the transistor (BJT) is grounded. The inverting terminal A is virtually ground and $V_A = 0$

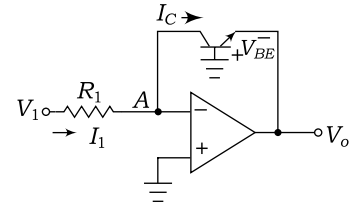


Fig. 7.51 Logarithmic amplifier

The transistor-emitter current is

$$I_E = I_S\left(e^{\frac{qV_{BE}}{KT}} - 1\right) \tag{7.58}$$

where I_s is emitter saturation current = 10^{-13} A
k is Boltzmann's constant = 8.62×10^{-5} eV/K or 1.38×10^{-23} J/K
T is absolute temperature in K
q is the charge of electron = 1.6×10^{-19}C

As base of the transistor is grounded, $I_E = I_C$

Therefore, transistor-collector current is equal to

$$I_C = I_S\left(e^{\frac{qV_{BE}}{KT}} - 1\right)$$

or
$$\frac{I_C}{I_S} = e^{\frac{qV_{BE}}{KT}} - 1$$

or
$$\frac{I_C}{I_S} + 1 = e^{\frac{qV_{BE}}{KT}} \tag{7.59}$$

As $I_C >> I_s$, we can write the above expression as $\frac{I_C}{I_S} = e^{\frac{qV_{BE}}{KT}}$

Taking log on both the sides, we find

$$\log\frac{I_C}{I_S} = \frac{qV_{BE}}{KT}$$

or
$$V_{BE} = \frac{KT}{q}\log\frac{I_C}{I_S} \tag{7.60}$$

The current flow through resistance R_1 is $I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1}$ (as $V_A = 0$)

Applying KCL at the node A, we get

$$I_1 = I_C = \frac{V_1}{R_1}$$

or
$$V_{BE} = \frac{KT}{q}\log\frac{V_1}{I_S R_1} \tag{7.61}$$

Since the emitter of BJT is connected to the output of the operational amplifier, the output voltage is equal to

$$V_O = -V_{BE} = -\frac{KT}{q}\log\left(\frac{V_1}{I_S R_1}\right)$$

Assume reference voltage $V_{\text{ref}} = I_s R_1$. Then, we can obtain the output voltage as

$$V_O = -\frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}} \tag{7.62}$$

From the above expression, it is clear that the output voltage is proportional to the logarithm of the input voltage.

7.13.1 Disadvantages of Logarithmic Amplifier

The disadvantages of this amplifier are the following:

1. The output voltage depends on temperature (T) and reverse saturation current (I_S).
2. The emitter saturation current varies from one transistor to another transistor and its magnitude also depends on the temperature (T).
3. Therefore, temperature effects on amplifier performance and accuracy of these effects can be reduced by temperature-compensating circuits.

In this section, temperature compensated logarithmic amplifier has been discussed.

Figure 7.52 shows a logarithmic amplifier with saturation current and temperature compensation. The input voltage V_1 is applied to one log-amplifier and a reference voltage V_{ref} is applied to another log amplifier. The two transistors T_1 and T_2 are integrated close together in the same silicon wafer. Hence, there is a close match of saturation currents and temperature tracking to ensure very good result.

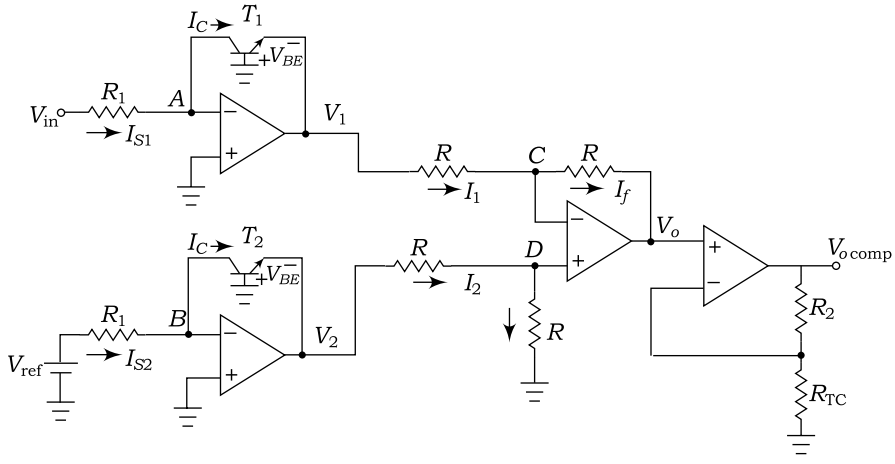


Fig. 7.52 Log amplifier with saturation and temperature compensation

Assume the saturation current of the transistor T_1 is equal to the saturation current of the transistor T_2. Therefore, $I_{s1} = I_{s2} = I_s$

The output voltage V_1 can be expressed as

$$V_1 = -\frac{KT}{q}\log\left(\frac{V_{in}}{I_S R_1}\right) \tag{7.63}$$

In the same way, the output voltage V_2 will be

$$V_2 = -\frac{KT}{q}\log\left(\frac{V_{ref}}{I_S R_1}\right) \tag{7.64}$$

Then output voltage $V_o = V_2 - V_1$

After substituting the values of V_1 and V_2 in the above equation, we get

$$V_O = \frac{KT}{q}\left[\log\left(\frac{V_{in}}{I_S R_1}\right) - \log\left(\frac{V_{ref}}{I_S R_1}\right)\right]$$

or

$$V_O = \frac{KT}{q}\log\left(\frac{V_{in}}{V_{ref}}\right) \tag{7.65}$$

Hence, the reference voltage level is now set with a single external voltage source. Consequently, output voltage does not depend on device emitter saturation current I_S. The voltage V_O is still dependent upon temperature and it is directly proportional to temperature (T). The temperature effect can be compensated by the last stage operational amplifier which provides a non-inverting gain $\left(1 + \frac{R_2}{R_{TC}}\right)$.

Then actual output voltage can be expressed as

$$V_{O\text{comp}} = \left(1 + \frac{R_2}{R_{\text{TC}}}\right)\frac{KT}{q}\log\left(\frac{V_{\text{in}}}{V_{\text{ref}}}\right) \tag{7.66}$$

where, R_{TC} = Temperature sensitive resistance. It has positive temperature coefficient so that slope of the above equation will be constant with the temperature changes.

As four operational amplifiers are used for a temperature-compensated logarithmic amplifier, this circuit becomes expensive if FET operational amplifiers are used for precision. To reduce the circuit cost, two operational amplifiers can be used for a log amplifier with same output voltage as depicted in Fig. 7.53.

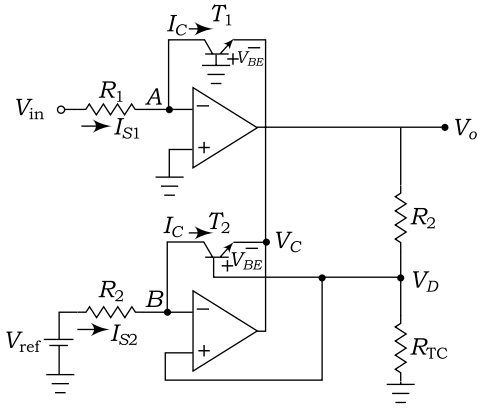


Fig. 7.53 Log amplifier using two operational amplifiers

7.14 ANTILOG AMPLIFIER

The antilog of a logarithmic number is a decimal number so that antilog amplifier performs reverse operation of a logarithmic amplifier. Figure 7.54 shows a typical antilog amplifier circuit using diode. In this circuit, the diode is connected between input signal and inverting terminal of operational amplifier. The feedback resistance R_f is connected between inverting and output terminals of the operational amplifier. As non-inverting terminal is grounded, the node A is at virtual ground and the potential at A is $V_A = 0$.

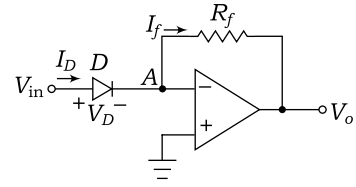


Fig. 7.54 Antilog amplifier

The current flow through diode is

$$I_D = I_O e^{\frac{V_D}{\tau V_T}} \tag{7.67}$$

where, I_{D} is diode current,
I_O is reverse saturation current,
V_{D} is diode voltage $\tau = 1$ for Ge diode,
$\tau = 2$ for Si diode,
V_{T} is voltage equivalent of temperature
k is the Boltzmann's constant, and
T is temperature in K.

Applying KCL at A, we get

$$I_f = I_D \tag{7.68}$$

The output voltage is

$$V_O = -I_f R_f = -I_O e^{\frac{V_{\text{in}}}{\tau V_T}} R_f \tag{7.69}$$

Taking log on both sides, we obtain

$$\log V_O = -I_O R_f \log e^{\left(\frac{V_{\text{in}}}{\tau V_T}\right)}$$

or $$\log V_O = -I_O R_f \frac{V_{\text{in}}}{\tau V_T}$$

Taking inverse log on both sides, we get

$$\log^{-1}(\log V_O) = -I_O R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right)$$

or $$V_O = -I_O R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right) \tag{7.70}$$

It is clear from above expression that the output V_O is the antilog of the input voltage and consequently the amplifier acts as an *antilog amplifier*.

7.15 ANTILOG AMPLIFIER USING TRANSISTOR

A typical antilog amplifier using transistor is shown in Fig. 7.55

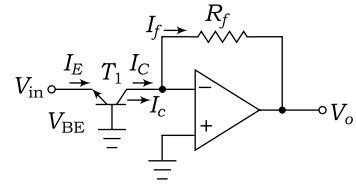


Fig. 7.55 Antilog amplifier using transistor

The collector current can be expressed as

$$I_C = I_O e^{\frac{V_{BE}}{\tau V_T}}$$

The non-inverting terminal is at ground potential. The node A is at virtual ground. Therefore, $V_A = 0$. The base of the transistor is at ground potential and the collector of transistor is at virtual ground. As a result, the voltage across base and emitter of the transistor is $V_{BE,}$ which is equal to input voltage V_{in} so that $V_{BE} = V_{\text{in}}$

Then collector current is equal to

$$I_C = I_O e^{\frac{V_{\text{in}}}{\tau V_T}} \tag{7.71}$$

The output voltage can be expressed as

$$V_o = -I_f R_f = -I_O e^{\frac{V_{\text{in}}}{\tau V_T}} R_f \quad (\text{as } I_C = I_f)$$

or $$V_o = -I_O R_f e^{\frac{V_{\text{in}}}{\tau V_T}}$$

Taking log on both sides, we get

$$\log V_o = -I_O R_f \log e^{\frac{V_{\text{in}}}{\tau V_T}}$$

or $$\log V_o = -I_O R_f \frac{V_{\text{in}}}{\tau V_T}$$

Taking inverse log on both side, we obtain

$$\log^{-1}(\log V_O) = -I_O R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right)$$

So the output voltage will be equal to

$$V_O = -I_O R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right) \tag{7.72}$$

It is very clear from above expression that the output voltage V_O is an inverse logarithm of the input voltage V_{in}. In the output voltage equation, I_O and V_T are present. The current I_O and voltage V_T are functions of temperature. Due to temperature changes, these parameters change and there are serious errors at the output voltage. Therefore, a temperature-compensation antilog amplifier must be used in place of a simple antilog amplifier.

7.16 ANALOG MULTIPLIER

An *analog voltage multiplier* is a circuit where the output voltage is directly proportional to the product of the two input voltages. Figure 7.56 shows the circuit diagram of an analog voltage multiplier which consists of log amplifiers, adder circuits and antilog amplifier.

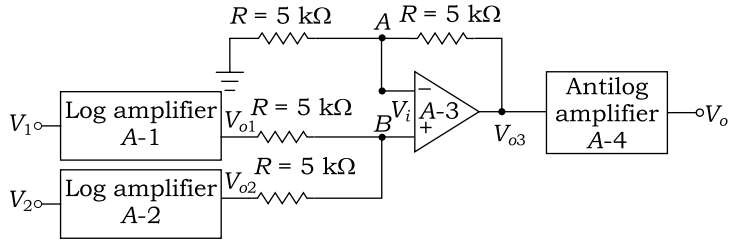


Fig. 7.56 Multiplier circuit

The output log amplifier A_1 is

$$V_{O1} = -\frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}} \tag{7.73}$$

The output log amplifier A_2 is

$$V_{O2} = -\frac{KT}{q}\log\frac{V_2}{V_{\text{ref}}} \tag{7.74}$$

The output voltage of the adder circuit is

$$V_{O3} = -V_{O1} - V_{O2}$$

After substituting the values of V_{O1} and V_{O2}, we get

$$\begin{aligned} V_{O3} &= -\left(-\frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}}\right) - \left(-\frac{KT}{q}\log\frac{V_2}{V_{\text{ref}}}\right) \\ &= \frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}} + \frac{KT}{q}\log\frac{V_2}{V_{\text{ref}}} \\ &= \frac{KT}{q}\log\left(\frac{V_1}{V_{\text{ref}}}\frac{V_2}{V_{\text{ref}}}\right) \quad (\text{as } \log(AB) = \log A + \log B) \end{aligned} \tag{7.75}$$

The output voltage of antilog amplifier is

$$V_O = -I_O R_f \log^{-1}\left(\frac{V_{O3}}{\tau V_T}\right)$$

After substituting V_{O3} in the above equation, we obtain

$$V_O = -I_O R_f \log^{-1}\left(\frac{1}{\tau V_T} \times \frac{KT}{q} \log\left(\frac{V_1 \times V_2}{V_{\text{ref}}^2}\right)\right)$$

Assuming $\frac{1}{\tau V_T} \times \frac{KT}{q}$ is about to 1, we get

$$V_O = -I_O R_f \log^{-1}\left(\log\left(\frac{V_1 \times V_2}{V_{\text{ref}}^2}\right)\right)$$

Applying $\log^{-1}$ (log) = 1, we find

$$V_O = -I_O R_f \frac{V_1 V_2}{V_{\text{ref}}^2} = K V_1 V_2 \quad \text{where} \quad K = \frac{I_o R_f}{V_{\text{ref}}^2} \tag{7.76}$$

Therefore, the output voltage is the product of two input voltages V_1 and V_2.

Analog multipliers are commonly used in

1. Amplitude modulation, frequency modulation, phase frequency modulation, and suppressed carrier frequency modulation
2. Phase detection circuit
3. Power measurement, velocity and acceleration measurement
4. Voltage-controlled attenuators and voltage controlled amplifiers
5. Gain of amplifier measurement
6. Voltage divider circuit, true rms calculation
7. Frequency converters and frequency-doubling circuits
8. Square and square-root calculations

7.17 ANALOG DIVIDER

An analog voltage divider is a circuit where the output voltage is directly proportional to the division of the two input voltages. Figure 7.57 shows the circuit diagram of an analog voltage divider which consists of log amplifiers, subtractor circuit and antilog amplifier.

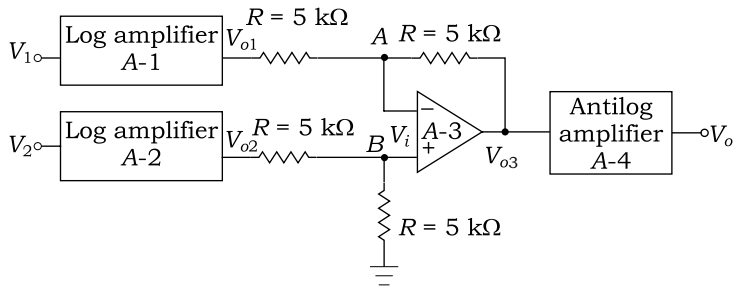


Fig. 7.57 Divider circuit

The output log amplifier A_1 is

$$V_{O1} = -\frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}} \tag{7.77}$$

The output log amplifier A_2 is

$$V_{O2} = -\frac{KT}{q}\log\frac{V_2}{V_{\text{ref}}} \tag{7.78}$$

The output voltage of subtractor circuit is

$$V_{O3} = K_1(V_{O2} - V_{O1}) \quad \text{where } K_1 \text{ is constant} \tag{7.79}$$

After substituting the value of V_{O1} and V_{O2} in the above equation, we get

$$V_{O3} = -K_1\frac{KT}{q}\left(\log\frac{V_2}{V_{\text{ref}}} - \log\frac{V_1}{V_{\text{ref}}}\right)$$

Applying as $\log\left(\frac{A}{B}\right) = (\log A - \log B)$ and $K_2 = -K_1\frac{KT}{q}$, we get

$$V_{O3} = K_2\left(\log\frac{V_2}{V_{\text{ref}}} \times \frac{V_{\text{ref}}}{V_1}\right) = K_2\left(\log\frac{V_2}{V_1}\right) \tag{7.80}$$

Hence, we can state that output voltage V_{O3} is directly proportional to $\left(\log\frac{V_2}{V_1}\right)$, and we can write

$$V_{O3} \propto \log\left(\frac{V_2}{V_1}\right)$$

The output of antilog amplifier is

$$V_O \propto \log^{-1}(V_{O3})$$

After substituting the value of V_{O3} in the above equation, we get

$$V_O \propto \log^{-1}\left(\log\left(\frac{V_2}{V_1}\right)\right)$$

Applying $\log^{-1}(\log) = 1$, we can express the output voltage as

$$V_O \propto \left(\frac{V_2}{V_1}\right) \tag{7.81}$$

Hence, the output voltage is proportional to the division of the two analog input voltages V_1 and V_2.

Example 7.24 Figure 7.58 shows a log amplifier using an OP-AMP and diode. The characteristics of diode is expressed as $I = I_S\left(e^{\frac{qV_D}{KT}} - 1\right)$.

(a) Determine the output voltage in terms of input voltage V_{in}.

(b) Calculate the output voltage when $\frac{KT}{q}$ = 20 mV, R = 10 kΩ and I_S = 1 μA

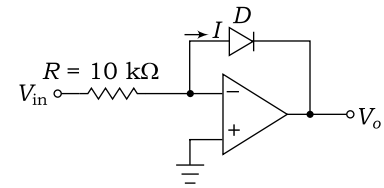


Fig. 7.58

Sol.

(a) The current flow through the diode is $I = I_S\left(e^{\frac{qV_D}{KT}} - 1\right)$

Therefore $\frac{I}{I_S} + 1 = e^{\frac{qV_D}{KT}}$

Taking log both the sides, we get

$$\log\left(\frac{I}{I_S} + 1\right) = \log\left(e^{\frac{qV_D}{KT}}\right)$$

or $$\frac{qV_D}{KT} = \log\left(\frac{I}{I_S}\right) \qquad \text{as } I >> I_S$$

or $$V_D = \frac{KT}{q}\log\left(\frac{I}{I_S}\right)$$

As current $I = \frac{V_{\text{in}}}{R}$, the output voltage V_O is equal to V_D and it can be expressed as

$$V_O = V_D = \frac{KT}{q}\log\left(\frac{V_{\text{in}}}{RI_S}\right)$$

(b) Given $\frac{KT}{q}$ = 20 mV, R = 10 kΩ and I_S = 1 μA

The output voltage is

$$V_O = \frac{KT}{q}\log\left(\frac{V_{\text{in}}}{RI_S}\right)$$ Assume V_{in} = 0.4 V and compute the log value in e-base

$$= 20 \times 10^{-3}\log\left(\frac{0.4}{10 \times 10^3 \times 1 \times 10^{-6}}\right) = 73.77 \text{ mV}$$

Example 7.25 Determine the output voltage V_O of a log amplifier using OP-AMP and transistor as shown in Fig. 7.59. Assume V_{in} = 100 mV, R = 10 kΩ, T = 300 k and $I_S = 10^{-13}$ A.

Sol. The output voltage V_O of a log amplifier is

$$V_O = -V_{BE} = -\frac{KT}{q}\log\left(\frac{V_1}{I_S R_1}\right)$$

$$= -\frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}}\log\left(\frac{100 \times 10^{-3}}{10^{-13} \times 10 \times 10^3}\right)$$

$$= -476.635 \text{ mV}$$ (Assume e-base to compute log value)

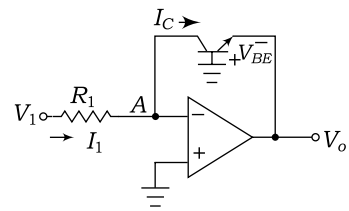


Fig. 7.59

Example 7.26 Determine the output voltage V_O of an antilog amplifier using OP-AMP and transistor as shown in Fig. 7.60. Assume $V_{in} = 500$ mV, $R_f = 10$ kΩ, $\tau = 1$, $V_T = 25$ mV and $I_O = 10^{-13}$ A

Sol. The output voltage V_O of a log amplifier is

$$V_O = -I_O R_f \log^{-1}\left(\frac{V_{in}}{\tau V_T}\right)$$

$$= -10^{-13} \times 10 \times 10^3 \times \log^{-1}\left(\frac{500 \times 10^{-3}}{1 \times 25 \times 10^{-3}}\right) \text{V}$$

$$= -0.485 \text{ V} \quad \text{(Assume e-base to compute antilog value)}$$

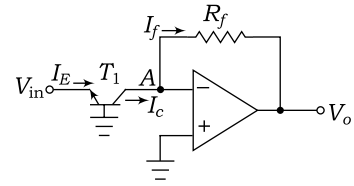


Fig. 7.60

7.18 COMPARATOR

A *comparator* is an electronic circuit which can compare an input voltage signal (V_{in}) with a known reference voltage (V_{ref}). It is basically an open-loop operational amplifier. The input voltage is applied to one of the input terminals of an OP-AMP and the reference voltage is applied at the other terminal of the OP-AMP. The ideal characteristic of a comparator is shown in Fig. 7.61. When the input voltage $V_{in} > V_{ref}$, the output voltage is $+V_{saturation}$ ($+V_{sat}$). If the input voltage $V_{in} < V_{ref}$, the output voltage is $-V_{saturation}$ ($-V_{sat}$). Generally, there are two types of comparators such as

1. Non-inverting comparators
2. Inverting comparators

In this section, both inverting as well as non-inverting comparators are discussed elaborately.

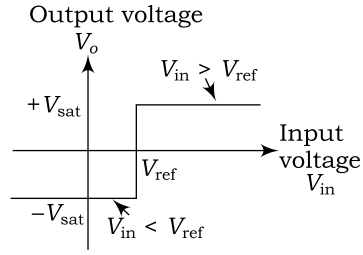


Fig. 7.61 Transfer characteristic of an ideal comparator when V_{ref} is positive voltage

7.18.1 Non-inverting Comparator

Figure 7.62 shows a non-inverting comparator. A fixed reference voltage V_{ref} is applied to inverting (–) terminal of OP-AMP through resistance R_2. The time varying input voltage V_{in} is also applied to non-inverting terminal through resistance R_1. When input voltage V_{in} is less than reference voltage V_{ref}, output voltage will be $-V_{sat}$ ($-V_{CC}$). If the input voltage V_{in} is greater than reference voltage V_{ref}, output voltage will be $+V_{sat}$ ($+V_{CC}$).

A sinusoidal input voltage $V_m \sin \omega t$ is applied to the positive (+) input terminal and the output voltage will be either $-V_{sat}$ ($-V_{CC}$) or $+V_{sat}$ ($+V_{CC}$) as shown in Fig. 7.63 when voltage V_{ref} is positive. While the reference voltage is negative, the output voltage waveform is as shown in Fig. 7.64.

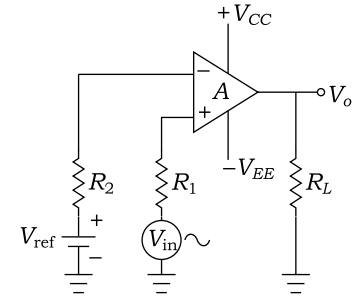


Fig. 7.62 Non-inverting comparator

In a practical comparator circuit (Fig. 7.65), V_{ref} can be obtained from a 10 kΩ variable resistance (potentiometer) which acts as a potential divider. In 10 kΩ potentiometer, $+V_{CC}$ and $-V_{CC}$ are connected with the two end terminals and the wiper is connected with the inverting (–) input terminal of OP-AMP as shown in Fig. 7.65. Hence, the reference voltage can be varied from $+V_{CC}$ to $-V_{CC}$. When V_{ref} is positive, the output voltage waveform is shown in Fig. 7.63. If V_{ref} is negative, the output voltage waveform is depicted in Fig. 7.64.

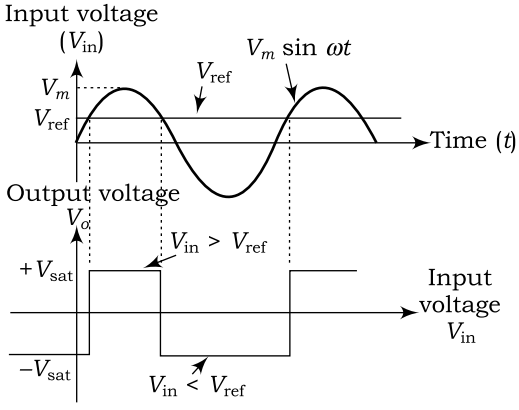


Fig. 7.63 Input and output voltage waveforms of non-inverting comparator when V_{ref} is positive

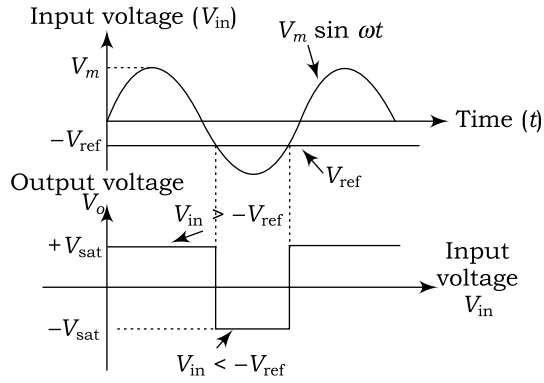


Fig. 7.64 Input and output voltage waveforms of non-inverting comparator when V_{ref} is negative

In this circuit (Fig. 7.65), diodes D_1 and D_2 protect the operational amplifier from excessive input voltage V_{in}. Due to diodes, difference input voltage of the operational amplifier is clamped to either +0.7 V or –0.7 V. Therefore, these diodes are called *clamp diodes*. The resistance R_1 is connected in series with input voltage V_{in} and it is used to limit the current through diodes D_1 and D_2. To reduce the offset problem, a resistance R_2 is connected in series with reference to voltage V_{ref}.

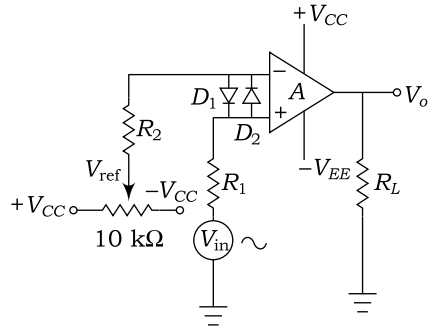


Fig. 7.65 Practical non-inverting comparator

7.18.2 Inverting Comparator

Figure 7.66 shows an inverting comparator. The input voltage V_{in} is applied to inverting (–) terminal through resistance R_1. The fixed reference voltage V_{ref} is applied to non-inverting (+) terminal of OP-AMP through resistance R_2. In a practical inverting comparator, the V_{ref} can be obtained from a 10 kΩ variable potentiometer which acts as a potential divider. In 10 kΩ potentiometer, $+V_{CC}$ and $-V_{CC}$ are connected with the two end terminals and the wiper is connected with the non-inverting (+) input terminal of the OP-AMP. Consequently, by varying the wiper position, the reference voltage can be varied from $+V_{CC}$ to $-V_{CC}$.

In inverting comparator, when input voltage V_{in} is less than reference voltage V_{ref}, output voltage will be $+V_{sat}$ ($+V_{CC}$). If the input voltage V_{in} is greater than reference voltage V_{ref}, output voltage will be $-V_{sat}$ ($-V_{CC}$). When a sinusoidal input voltage V_m sin ωt is applied to the negative (–) input terminal of the OP-AMP, the output voltage will be either $+V_{sat}$ ($+V_{CC}$) or $-V_{sat}$ ($-V_{CC}$) as shown in Fig. 7.67(a) and (b).

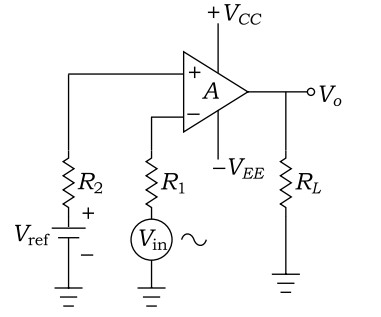


Fig. 7.66 Inverting comparator

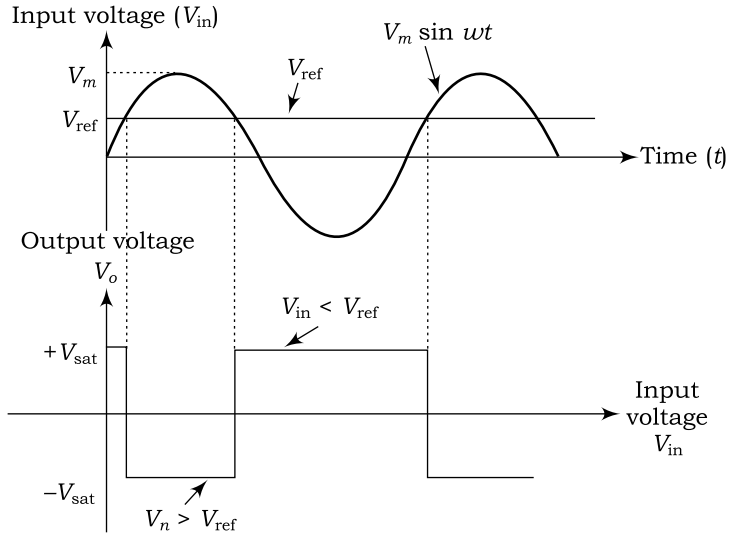


Fig. 7.67(a) Input and output voltage waveforms of inverting comparator when V_{ref} is positive

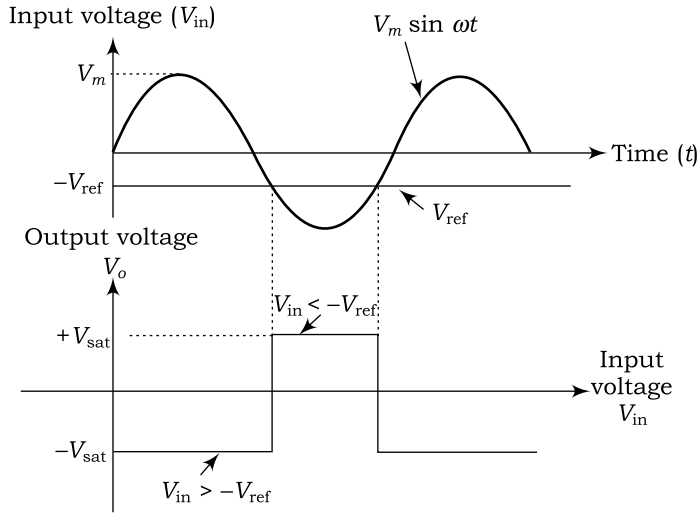


Fig. 7.67(b) Input and output voltage waveforms of inverting comparator when V_{ref} is negative

Figure 7.68 shows a practical inverting comparator. When two back-to-back zener diodes are connected at the output of the OP-AMP, the output voltage will be independent of supply voltage. The R is connected in series with zener diodes to limit the current flow through zener diodes. The limiting output voltage will be $(V_Z + V_D)$ and $-(V_Z + V_D)$ where V_D is the forward voltage drop of diode and V_Z is the voltage across zener diode.

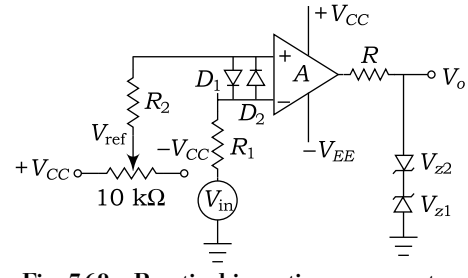


Fig. 7.68 Practical inverting comparator

7.18.3 Applications of Comparators

Comparators are commonly used in

- Zero-crossing detector circuits
- Window detector circuits
- Multivibrators
- Time-marker generators
- Phase meters
- Schmitt triggers

In this section, the operation of a Zero-Crossing-Detector (ZCD) circuit is explained.

Zero-Crossing Detector

The inverting or non-inverting comparator can be used as a *zero-crossing detector* circuit, when the reference voltage V_{ref} is zero. Figure 7.69 shows an inverting zero-crossing detector circuit where $V_{ref} = 0$. In the positive half cycle of supply voltage, $V_{in} > V_{ref}$ and the output voltage is $-V_{sat.}$ During the negative half cycle of supply voltage, $V_{in} < V_{ref}$ and the output voltage is $+V_{sat}$. The output voltage waveform is shown in Fig. 7.70. This circuit is known as *sine-wave to square-wave converter*.

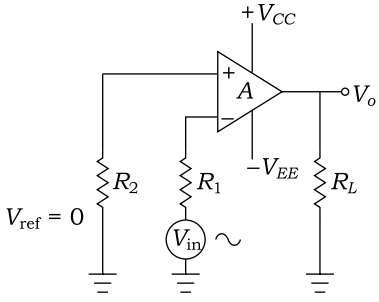


Fig. 7.69 Zero-crossing detector circuit

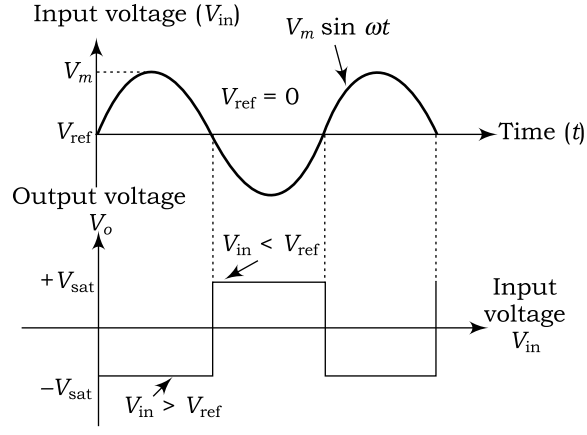


Fig. 7.70 Input and output voltage waveforms of a zero-crossing detector circuit

7.19 SCHMITT TRIGGER

In an analog comparator circuit, the applied input voltage is compared with a known reference voltage. When a noise voltage signal exists in the input voltage, the comparator output signal will be square wave with some unwanted signals. The comparator output state changes either from $+V_{sat}$ to $-V_{sat}$ or from $-V_{sat}$ to $+V_{sat}$ when, there is some millivolt change in the input voltage which is above the reference voltage or less than reference voltage. As noise signal is generated at random value, the output consists of a series of pulses of different width as shown in Fig. 7.71. This phenomenon is called *chattering*. This problem can be removed by a Schmitt trigger circuit. The positive feedback of a *Schmitt trigger circuit* can also speed up the response time of the system.

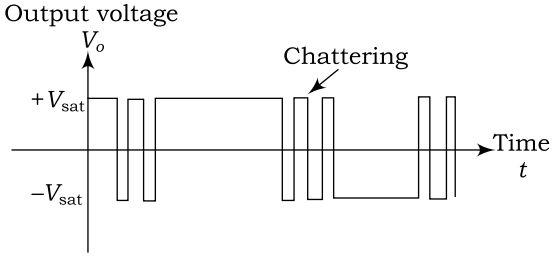


Fig. 7.71 Comparator output with chattering due to noise signal in input voltage

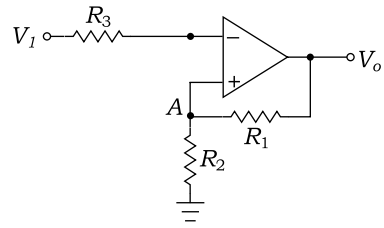


Fig. 7.72 Schmitt trigger circuit

Figure 7.72 shows a Schmitt trigger circuit. The input voltage is applied to the inverting (–) input terminal and feedback voltage is applied to the non-inverting (+) input terminal.

Assume the output voltage is $V_O = +V_{sat}$. Then the feedback voltage at non-inverting (+) input terminal will be

$$V_f = \frac{R_2}{R_1 + R_2} V_{sat} = V_{UT} \tag{7.82}$$

This voltage is also called as *upper threshold voltage*, V_{UT}. When the input voltage V_{in} is less than V_{UT} ($V_{in} < V_{UT}$), the output voltage V_O will be constant at $+V_{sat}$. If the input voltage V_{in} is just greater than V_{UT} ($V_{in} > V_{UT}$), the output voltage V_O of operational amplifier, switches from $+V_{sat}$ to $-V_{sat}$ and this circuit behaves as regenerative comparator. When $V_{in} > V_{UT}$, the output voltage V_O will be constant at $-V_{sat}$ as shown in Fig. 7.73.

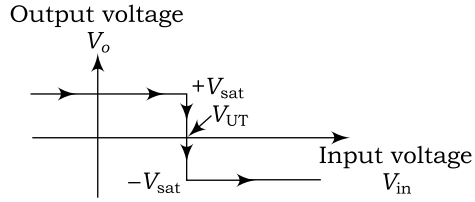


Fig. 7.73 Characteristics of Schmitt trigger for V_{in} increasing

Then the feedback voltage is

$$-\frac{R_2}{R_1 + R_2} V_{sat} = V_{LT} \tag{7.83}$$

This voltage is known as *lower threshold voltage*, V_{LT}. The output voltage V_O will be $-V_{sat}$ when $V_{in} > V_{LT}$. While the input voltage V_{in} is just less than V_{LT} ($V_{in} < V_{LT}$), the output voltage V_O of operational amplifier switches from $-V_{sat}$ to $+V_{sat}$ as shown in Fig. 7.74. Then output voltage V_O will be constant at $+V_{sat}$ till $V_{in} < V_{UT}$. The complete characteristics of Schmitt trigger is depicted in Fig. 7.75.

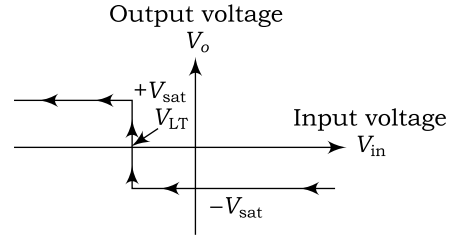


Fig. 7.74 Characteristics of Schmitt trigger for V_{in} decreasing

In this circuit the upper threshold voltage, V_{UT} must be greater lower threshold voltage, V_{LT}. The difference between V_{UT} and V_{LT} voltages is called as hysteresis width V_H and it can be expressed as

$$V_H = V_{UT} - V_{LT} = 2\frac{R_2}{R_1 + R_2} V_{sat} \tag{7.84}$$

and it will be constant as R_1, R_2, and V_{sat} are constant. If the input voltage V_{in} is just greater than V_{UT} ($V_{in} > V_{UT}$), the output voltage V_O of

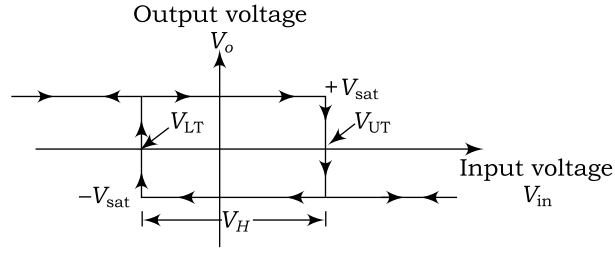


Fig. 7.75 Complete characteristics of Schmitt trigger

operational amplifier switches from $+V_{sat}$ to $-V_{sat}$ and this circuit behaves as *regenerative comparator*. When $V_{in} > V_{UT}$, the output voltage V_O will be constant at $-V_{sat}$.

Figure 7.76 shows a practical Schmitt trigger circuit. When two back to back zener diodes are connected at the output of OP-AMP, the output voltage will be independent of supply voltage ($+V_{sat}$ or $-V_{sat}$). The R is connected in series with zener diodes to limit the current flow through zener diodes. The limiting output voltage will be $(V_Z + V_D)$ and $-(V_Z + V_D)$ where V_D is the forward voltage drop of diode and V_Z is the voltage across zener diode.

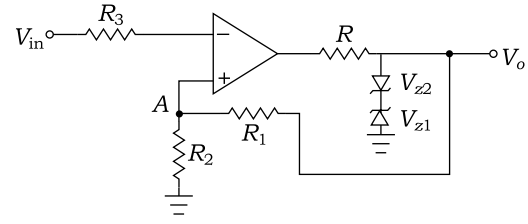


Fig. 7.76 Practical schmitt trigger circuit

Example 7.27 In a Schmitt trigger circuit as shown in Fig. 7.72, $R_1 = 10\ k\Omega$, $R_2 = 5\ k\Omega$, $V_{in} = 10 \sin \omega t$ saturation voltage ±15 V.

(a) Determine the threshold voltage V_{UT} and V_{LT}. Calculate hysteresis width V_H.

(b) Find the output voltage waveform.

Sol. (a) The upper threshold voltage, V_{UT} is

$$V_{UT} = \frac{R_2}{R_1 + R_2} V_{sat} = \frac{5}{10 + 5} \times 15\ V = 5\ V$$

The lower threshold voltage, V_{LT} is

$$V_{LT} = -\frac{R_2}{R_1 + R_2} V_{sat} = -\frac{5}{10 + 5} \times 15\ V = -5\ V$$

The hysteresis width V_H is

$$V_H = V_{UT} = V_{LT} = 5 - (-5)\ V = 10\ V$$

(b) The output voltage waveform is shown in Fig. 7.77.

Example 7.28 Figure 7.78 shows a Schmitt trigger circuit where $R_1 = 50\ k\Omega$, $R_2 = 10\ k\Omega$, $V_{ref} = +5$ V, saturation voltage ±14 V, and $V_{in} = 12 \sin \omega t$.

(a) Find the threshold voltages V_{UT} and V_{LT} and determine hysteresis width V_H

(b) Show the output voltage waveform.

Sol. (a) The upper threshold voltage, V_{UT} is

$$V_{UT} = V_{ref} + \frac{R_2}{R_1 + R_2}(V_{sat} - V_{ref}) = +5 + \frac{10}{50 + 10} \times (14 - 5)\ V = 6.5\ V$$

The lower threshold voltage, V_{LT} is

$$V_{LT} = V_{ref} - \frac{R_2}{R_1 + R_2}(V_{sat} + V_{ref}) = 5 - \frac{10}{50 + 10} \times (14 + 5)\ V = 1.83\ V$$

The hysteresis width V_H is

$$V_H = V_{UT} - V_{LT} = 6.5 - 1.83\ V = 4.67\ V$$

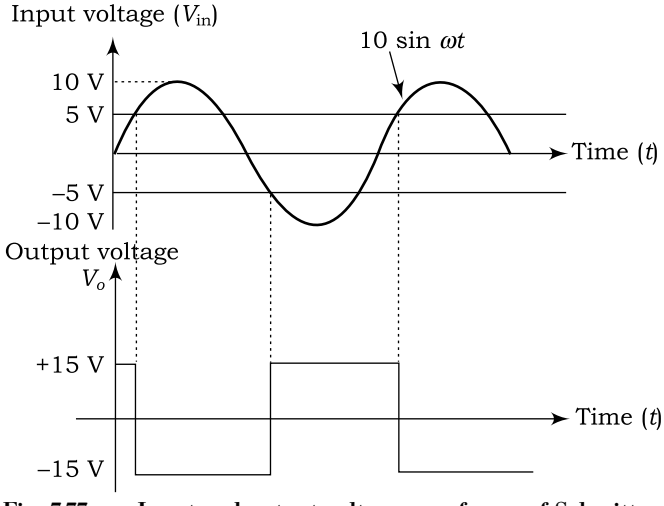


Fig. 7.77 Input and output voltage waveforms of Schmitt trigger circuit

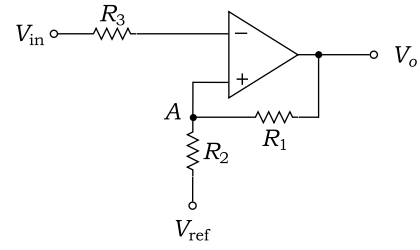


Fig. 7.78 Schmitt trigger circuit

(b) The output voltage waveform is shown in Fig. 7.79.

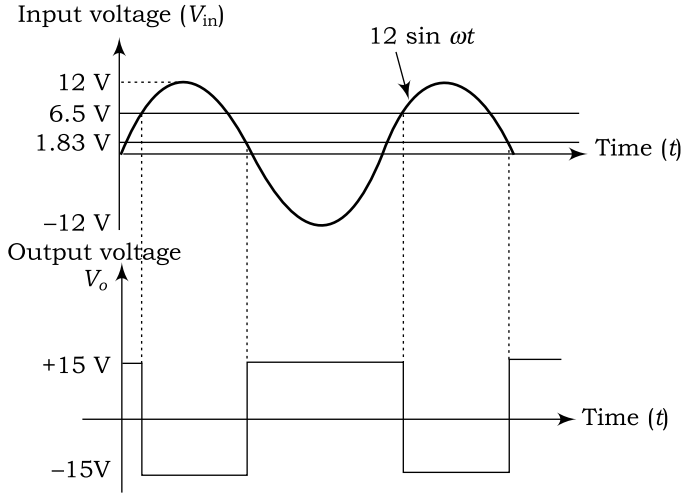


Fig. 7.79 Input and output voltage waveforms of Schmitt trigger circuit

7.20 INSTRUMENTATION AMPLIFIER

An **instrumentation amplifier** is a type of differential amplifier that has been outfitted with input buffer amplifiers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement.

The instrumentation amplifier is used to measure any physical quantities such as temperature, humidity, flow, intensity of light, displacement, etc. Actually any physical quantity is measured by using transducers. The output of transducer is in the range of certain mV and it cannot drive any indicating type instrument and

it cannot be displayed on display device. The instrumentation amplifier has to be used to amplify the output signal of transducers and the output of instrumentation amplifier can drive any display system or indicator. This amplifier has the following important features:

(i) high gain stability with low temperature coefficient
(ii) high gain accuracy
(iii) very high common mode rejection ratio (CMRR)
(iv) output impedance is very low
(v) very low dc offset
(vi) low drift and low noise
(vii) very high open-loop gain
(vii) very high input impedances

Instrumentation amplifiers are used where great accuracy and stability of the circuit both short- and long-term are required.

The instrumentation amplifier is usually shown schematically identical to a standard operational amplifier and the electronic instrumentation amplifier is almost always internally composed of 3 op-amps. Operational amplifiers are arranged in such a way that there is one op-amp to buffer each input (+,–) and one to produce the desired output with adequate impedance matching for the function.

Figure 7.79(a) shows an instrumentation amplifier and Fig. 7.79(b) shows the differential amplifier which is used in instrumentation amplifier. In Fig. 7.79, two non-inverting amplifiers A_1 and A_2 are used as the input stage and a difference amplifier A_3 is used in the second amplifying stage.

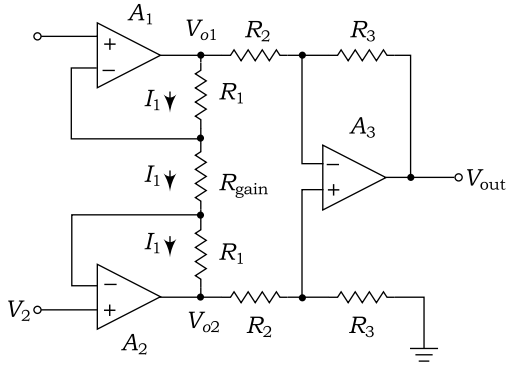


Fig. 7.79(a) An instrumentation amplifier

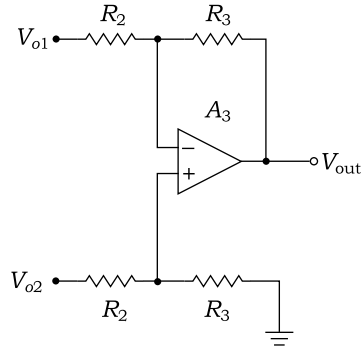


Fig. 7.79 (b) the differential amplifier which is used in instrumentation amplifier.

The current flows through resistance R_{gain} is

$$I_1 = \frac{V_1 - V_2}{R_{gain}}$$

The current in resistors $R_1$is equal to I_1. The output voltage of operational amplifier A_1 and A_2 are

$$V_{o1} = V_1 + I_1 R_1 = \left(1 + \frac{R_1}{R_{gain}}\right) V_1 - \frac{R_1}{R_{gain}} V_2$$

$$V_{o2} = V_2 - I_1 R_2 = \left(1 + \frac{R_1}{R_{gain}}\right) V_2 - \frac{R_1}{R_{gain}} V_1$$

The output of the difference amplifier is

$$V_{\text{out}} = \frac{R_3}{R_2}(V_{o2} - V_{o1})$$

After substituting the value of V_{o1} and V_{o2} in the above equation, we obtain

$$V_{\text{out}} = \frac{R_3}{R_2}\left(1 + 2\frac{R_1}{R_{\text{gain}}}\right)(V_2 - V_1)$$

As the input voltages are directly applied to the non-inverting terminals of A_1 and A_2, the input impedance is very large, ideally infinite, which is the most important characteristic of the instrumentation amplifier. The differential gain is a function of resistance R_{gain} which can be varied by using a potentiometer. Hence, an *instrumentation amplifier* is a differential op-amp circuit providing high input impedances with ease of gain adjustment through the variation of a single resistor

7.21 PRECISION RECTIFIER

A rectifier is used to convert ac voltage into dc voltage. The rectifier output is a dc voltage source, which can be represented as constant voltage source in series with a resistance. In microprocessor-based measurement system, it is necessary to rectify millivolt high frequency signal. When conventional diodes are used in rectifier circuit, always there is some voltage drop across forward bias diode, i.e., 0.2V for Ge diode and 0.7 V for Si diode. So that a milivolt signal cannot be able to forward bias the conventional diode. The switching speed of conventional diode is also low. If a diode is used in the forward path of an operational amplifier, cut-in-voltage of diode will be divided by the open loop gain, which is very large in operational amplifier. Then diode can operate in ideal mode with zero cut-in voltage. If a conventional diode is used in feedback path of operational amplifier, high frequency milivolt can be rectified. This rectifier is known as *precision rectifier*.

The precision rectifier is a circuit configuration obtained with an operational amplifier in order to have a circuit behave like an ideal diode and rectifier. The precision rectifier is also known as a *super diode*. It is useful for high-precision signal processing. There are two types of precision rectifier such as half wave rectifier and full wave rectifier.

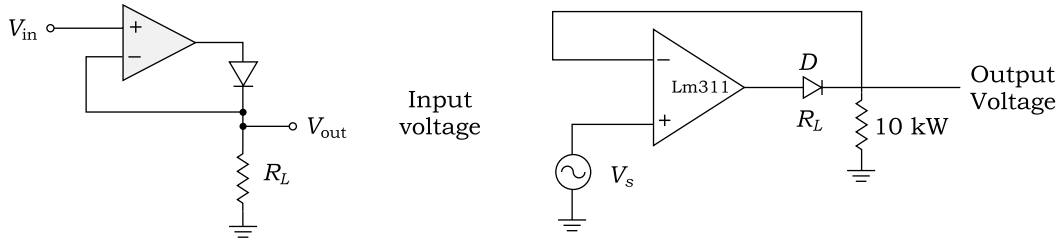


Fig. 7.80 Half wave precision rectifier

A simple precision rectifier circuit is shown in Fig. 7.80 where R_L can be used as load. Whenever the input voltage is negative, there is a negative voltage on the diode, so it works like an open circuit. Consequently, no current flows through the load and the output voltage is zero.

When the input voltage is positive, it is amplified by the operational amplifier which switches the diode on. Then current flows through the load. Due to the feedback, the output voltage is equal to the input voltage. The actual threshold of the super diode is very close to zero, but is not zero. It equals the actual threshold of the diode, divided by the gain of the operational amplifier.

The simple precision rectifier circuit has a problem so that it is not commonly used. Whenever the input becomes slightly negative, the operational amplifier runs open loop, as there is no feedback signal through the diode. Due to high open loop gain of operational amplifier, the output saturates. When the input voltage becomes positive again, the op-amp has to get out of the saturated state before positive amplification can take place again. Actually this change generates some ringing and it takes some time. Hence the frequency response of the circuit is greatly reduced.

An improved half wave precision rectifier circuit is shown in Fig. 7.81. When the input voltage is greater than zero, D_1 is OFF and D_2 is ON, so the output is zero as one side of resistance R_2 is connected to the virtual ground, and there is no current through it. If the input voltage is less than zero, D_1 is ON and D_2 is OFF, and the output voltage is just like the input voltage with an amplification of $-R_2/R_1$. The relationship between input voltage and output voltage is shown in Fig. 7.82.

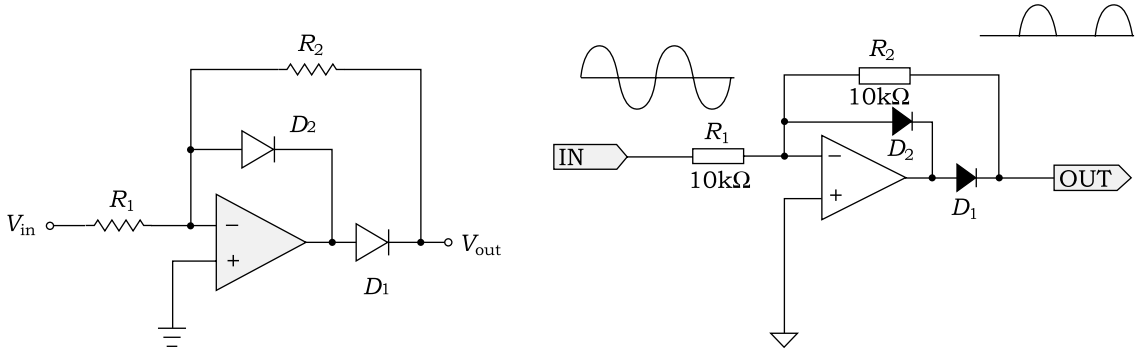


Fig. 7.81 An improved half wave precision rectifier circuit

The advantage of an improved half wave precision rectifier circuit is that the op-amp never goes into saturation, but its output must change by two diode voltage drops (about 1.2V) each time the input signal crosses zero. The slew rate of the operational amplifier, and its frequency response will limit high frequency performance. This circuit has an error of less than 1% at 100kHz especially for low signal levels.

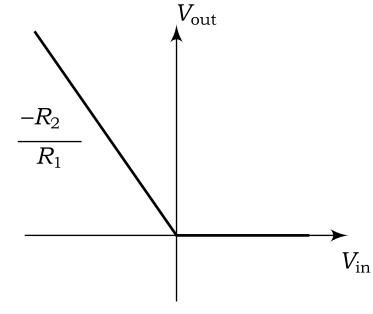


Fig. 7.82 Relationship between input voltage and output voltage

Full Wave Precision Rectifiers

Figure 7.83 shows the full wave precision rectifier which consists of two op amps, two diodes, and five *equal* resistors. Unfortunately, this circuit does not have high input resistance. For positive input voltage, diode D_P is ON and diode D_N is OFF and both the op-amps *A* and *B* act as inverter. Consequently output voltage is equal to input voltage.

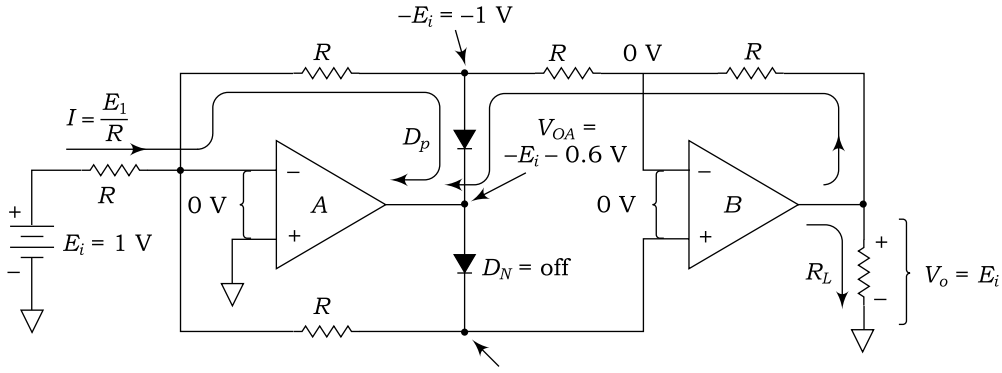
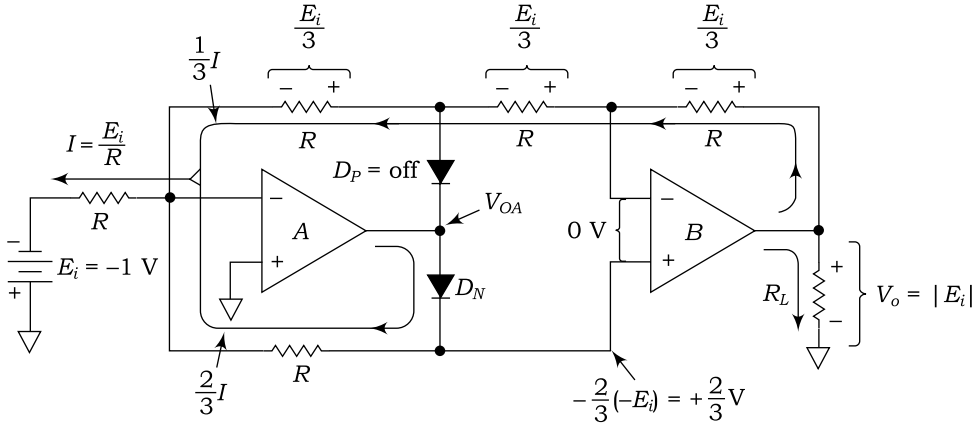


Fig. 7.83(a) For positive inputs D_P conducts; op amps A and B act as inverting amplifiers.

For negative input voltage, diode D_P is OFF and diode D_N is ON. The output voltage of op-amp A is V_{OA}. The differential input to B is zero, the inverting input terminal voltage is V_{OA}. The output voltage of op-amp B is $V_o = |E_i|$. The characteristics of an ideal precision rectifier are shown Fig. 7.84.



(b) For negative inputs. D_N conducts

Fig. 7.83(b) For negative inputs, D_V conducts.

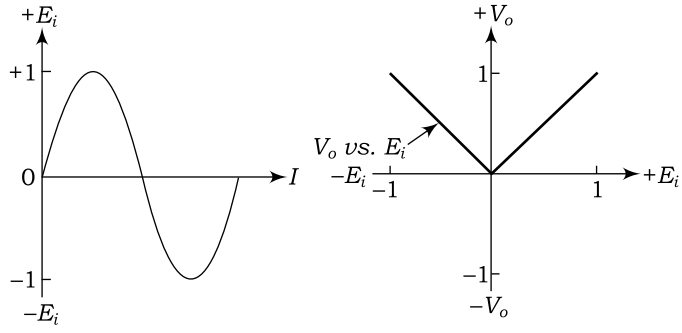


Fig. 7.84 Characteristics of an ideal precision rectifier

Figure 7.85 shows the simplified version of full wave precision rectifier. This circuit is used for most applications as linearity is very good at 20 mV, but speed is still limited by the op-amp. To obtain the best high frequency performance, this circuit requires a very fast op-amp and the reduce values of resistor.

Where very low levels are to be rectified, it is required that the signal must be amplified first. Since the use of Schottky diodes will improve low level and high frequency performance, it is very difficult to achieve perfect linearity from any rectifier circuit at extremely low levels. The operation up to 100 kHz is possible by using fast op-amps and diodes. R_1 is optional, and it is only needed if the source is ac coupled, so extremely high input impedance is possible.

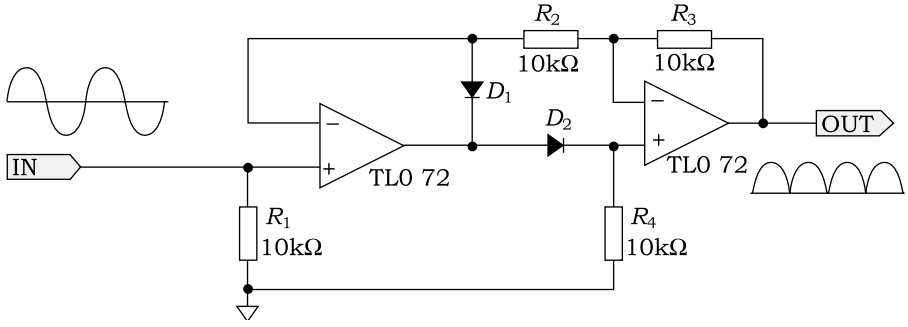


Fig. 7.85 The full wave precision rectifier

Example 7.29 An op-amp is used in non-inverting mode with R_1 = 1 kΩ, R_f = 10 kΩ, V_{CC} = ±12 V. Calculate the output voltage for the following inputs: (i) V_{in} = 100 mV (ii) V_{in} = 5 V

Sol. The gain of a non-inverting amplifier is $A_v = 1 + \dfrac{R_f}{R_1} = 1 + \dfrac{10\ \text{k}\Omega}{1\ \text{k}\Omega} = 11$

(i) When input voltage $V_{\text{in}} = 100\ \text{mV}, V_{\text{o}} = A_v \times V_{\text{in}} = 11 \times 100 \times 10^{-3}\ \text{V} = 1.1\ \text{V}$

(ii) When input voltage $V_{\text{in}} = 5\ \text{V}, V_{\text{o}} = A_v \times V_{\text{in}} = 11 \times 5\ \text{V} = 55\ \text{V}$
Since V_0 cannot be higher than $+V_{CC}$, V_0 = 12 V

Example 7.30 An op-amp is used in inverting mode with R_1 = 1 kΩ, R_f = 15 kΩ, V_{CC} = ±15 V. Calculate the output voltage for the following inputs: (i) V_{in} = 150 mV, (ii) V_{in} = 2 V.

Sol. The gain of an inverting amplifier is $A_v = -\dfrac{R_f}{R_1} = -\dfrac{15\ \text{k}\Omega}{1\ \text{k}\Omega} = -15$

(i) When input voltage $V_{\text{in}} = 150\ \text{mV}, V_{\text{o}} = A_v \times V_{\text{in}} = -15 \times 150 \times 10^{-3}\ \text{V} = -2.25\ \text{V}$

(ii) When input voltage $V_{\text{in}} = 2\ \text{V}, V_{\text{o}} = A_v \times V_{\text{in}} = -15 \times 2\ \text{V} = -30\ \text{V}$

Since V_0 cannot be higher than $\pm V_{\text{sat}}$, output voltage will be $-V_{\text{sat}}$

$-V_{\text{sat}} = 0.9 \times -V_{CC} = 0.9 \times -15 = -13.5\ \text{V}$, and $V_{\text{o}} = -13.5\ \text{V}$

Example 7.31 In the non-inverting summing amplifier V_1 = 2 V, V_2 = –4 V, V_3 = 5 V. Input resistors for all three input signals are same and are equal to 1 kΩ. The feedback resistor R_f is 2 kΩ. Determine the output voltage. Assume ideal op-amp.

Sol. Assume V_1 is present, V_2 and V_3 is to be shorted as shown in Fig. 7.87

$$V_A' = \frac{R_2 \,||\, R_3}{R_1 + R_2 \,||\, R_3} V_1 = \frac{1\ \text{k}\Omega || 1\ \text{k}\Omega}{1\ \text{k}\Omega + 1\ \text{k}\Omega || 1\ \text{k}\Omega} V_1 = \frac{V_1}{3}$$

Similarly $V_A'' = \frac{V_2}{3}$ when V_2 is present, V_1 and V_3 is to be shorted

and $V_A''' = \frac{V_3}{3}$ when V_3 is present, V_1 and V_2 is to be shorted.

If V_1, V_2 and V_3 are present, $V_A = \frac{V_1}{3} + \frac{V_2}{3} + \frac{V_3}{3} = \frac{1}{3}(V_1 + V_2 + V_3)$

The output voltage $V_o = \left(1 + \frac{R_f}{R_1}\right) V_A = \left(1 + \frac{2\ \text{k}\Omega}{1\ \text{k}\Omega}\right) \frac{2 - 4 + 5}{3} = 3\ \text{V}$

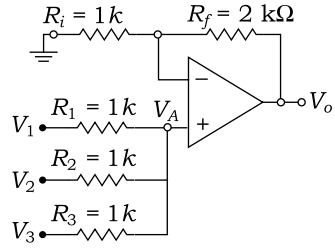


Fig. 7.86

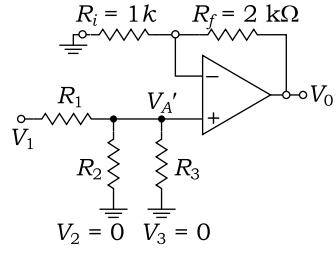


Fig. 7.87

Example 7.32 In the non-inverting summing amplifier, V_1 = 2 V, V_2 = 4 V, V_3 = 5 V. Input resistance for all three input signals are same and are equal to 1 kΩ, the feedback resistor R_f is 2 kΩ. Draw neat circuit diagram. Find output voltage.

Sol. Figure 7.88 shows the non-inverting summing amplifier with input voltages V_1 = 2 V, V_2 = 4 V, V_3 = 5 V.

The output voltage is

$$V_o = -\frac{R_f}{R_1}(V_1 + V_2 + V_3) = -\frac{2}{1}(2 + 4 + 5) = -22\ \text{V}$$

Since the maximum output voltage is $\pm V_{sat}$, the output voltage is $V_o = -V_{sat}$

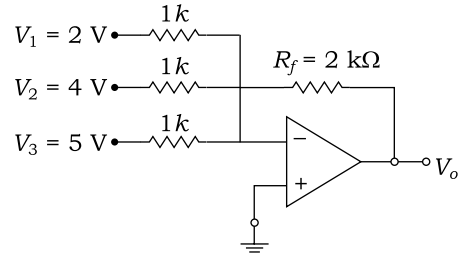


Fig. 7.88

Example 7.33 For the inverting amplifier using op-amp, if R_f = 100 kΩ, R_1 = 10 kΩ, V_{CC} = ±10 V, V_1 = 2 V_{dc}, Calculate output voltage, Is the result practically possible? Justify.

Sol. The output voltage $V_o = -\frac{R_f}{R_1} V_i = -\frac{100\ \text{k}\Omega}{10\ \text{k}\Omega} \times 2\ \text{V} = -20\ \text{V}$

The output voltage is restricted to ± V_{sat}. The maximum output voltage is

$$V_o = -0.9 V_{CC} = -0.9 \times 10 = -9\ \text{V} \quad \text{as } V_o = -V_{sat} = -0.9 V_{CC}$$

Example 7.34 For the inverting summing amplifier, if the following inputs are applied then calculate output voltage. V_{in1} = 1.5 V, V_{in2} = 3.5 V Given that $R_1 = R_2 = R_f$ = 5.2 kΩ.

Sol. Figure 7.89 shows the inverting summing amplifier with input voltages V_{in1} = 1.5 V, V_{in2} = 3.5 V.

The output voltage of the amplifier is

$$V_o = -\left(\frac{R_f}{R_1} V_{in1} + \frac{R_f}{R_2} V_{in2}\right) = -\left(\frac{5.2}{5.2} \times 1.5 + \frac{5.2}{5.2} \times 3.5\right) \text{V} = -5\ \text{V}$$

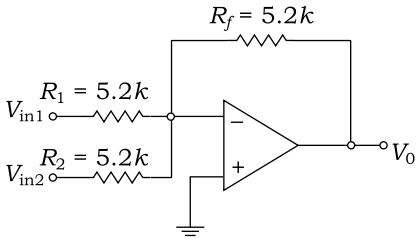


Fig. 7.89

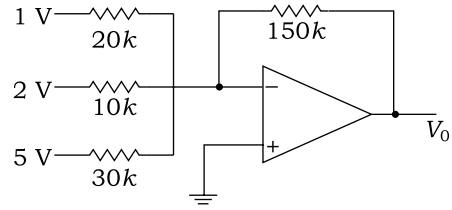


Fig. 7.90

Example 7.35 Find out the output voltage for the circuit given in Fig. 7.90. Derive necessary equations:

Sol. The output voltage is

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) = -\left(\frac{150}{20}\times 1 + \frac{150}{10}\times 2 + \frac{150}{30}\times 5\right) = -62.5 \text{ V}$$

The output voltage is always restricted to ± V_{sat}. Then maximum output voltage is $V_o = -0.9V_{CC}$ as $V_o = -V_{sat} = -0.9V_{CC}$

Example 7.36 Find the values of the resistors such that the circuit provides Vo = $2V_1 + V_2 - 4V_3$

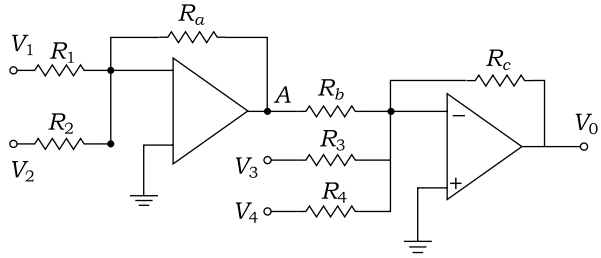


Fig. 7.91

Sol. The output voltage at *A* is

$$V_A = -\left(\frac{R_a}{R_1}V_1 + \frac{R_a}{R_2}V_2\right) \text{ and the output voltage } V_o = -\left(\frac{R_c}{R_b}V_A + \frac{R_c}{R_3}V_3 + \frac{R_c}{R_4}V_4\right)$$

or
$$V_o = -\left(-\frac{R_cR_a}{R_bR_1}V_1 - \frac{R_cR_a}{R_2R_b}V_2 + \frac{R_c}{R_3}V_3 + \frac{R_c}{R_4}V_4\right)$$

or
$$V_o = \left(\frac{R_cR_a}{R_bR_1}V_1 + \frac{R_cR_a}{R_2R_b}V_2 - \frac{R_c}{R_3}V_3 - \frac{R_c}{R_4}V_4\right) = 2V_1 + V_2 - 4V_3$$

Therefore, $\frac{R_cR_a}{R_bR_1} = 2, \frac{R_cR_a}{R_bR_2} = 1, \frac{R_c}{R_3} = 4$ and $V_4 = 0$

$\frac{R_2}{R_1} = 2$ or $R_2 = 2R_1$ *If* $R_1 = 4.7k, R_2 = 9.4k$

If $R_c = 10k,\ R_3 = 2.5k$

If $R_b = 2.2k, R_a = \frac{2R_bR_1}{R_c} = \frac{2\times 2.2\times 4.7}{10} = 2.068k$

Example 7.37 Determine V_o for the following circuit:

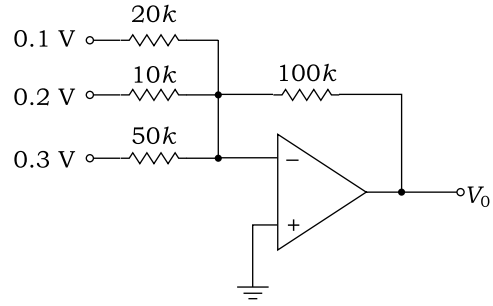


Fig. 7.92

Sol. The output voltage is $V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$

$$V_o = -\left(\frac{100k}{20k} \times 0.1 + \frac{100k}{10k} \times 0.2 + \frac{100k}{50k} \times 0.3\right) = -3.1 \text{ V}$$

Example 7.38 Find the output voltage of the following op-amp circuit shown in Fig. 7.93.

Sol. The potential at A is $V_A = \frac{1\ \text{k}\Omega}{5\ \text{k}\Omega + 1\ \text{k}\Omega}V_2 = \frac{V_2}{6}$

When V_1 is connected to ground, the output voltage is

$$V_{o2} = \left(1 + \frac{10\ \text{k}\Omega}{5\ \text{k}\Omega}\right)V_A = 3 \times \frac{V_2}{6} = \frac{V_2}{2}$$

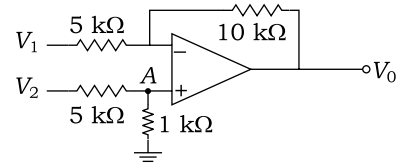


Fig. 7.93

When V_2 is connected to ground, the output voltage is

$$V_{o1} = -\frac{10\ \text{k}\Omega}{5\ \text{k}\Omega}V_1 = -2V_1$$

When V_1 and V_2 are present in the circuit, the output voltage is

$$V_o = V_{o1} + V_{o2} = -2V_1 + \frac{V_2}{2}$$

Example 7.39 For the circuit shown in Fig. 7.94, find V_o/V_{in}.

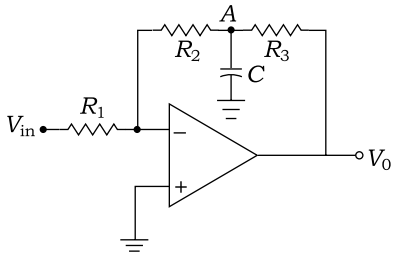


Fig. 7.94

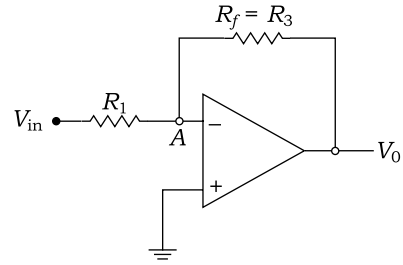


Fig. 7.95

Sol. Point A is at virtual ground, R_2 is shorted and C is replaced by a short circuit. Therefore, $R_f = R_3$. Figure 10 shows the equivalent circuit of Fig. 95. This circuit is an inverting amplifier.

The gain is $A_v = \dfrac{V_o}{V_{in}} = -\dfrac{R_f}{R_1} = -\dfrac{R_3}{R_1}$

Example 7.40 Calculate the output voltage using the circuit of Fig. 7.96 shown below for reset components of values: R_f= 470 kΩ, R_1 = 4.3 kΩ, R_2 = 33 kΩ and R_3 = 33 kΩ for an input of 80 μV.

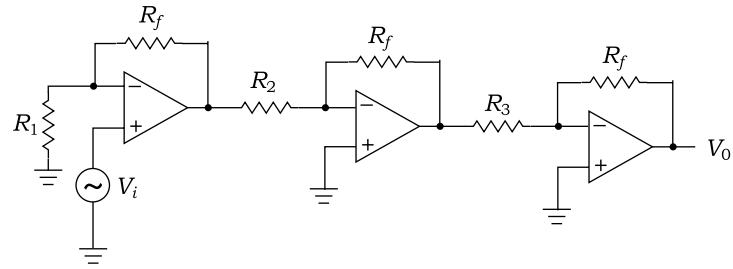


Fig. 7.96

Sol. The output voltage at the point A of Fig. 7.97 is

$$V_A = \left(1 + \frac{R_f}{R_1}\right) V_i$$

The output voltage at the point *B* of Fig. 7.97 is

$$V_B = -\frac{R_f}{R_2} V_A = -\frac{R_f}{R_2}\left(1 + \frac{R_f}{R_1}\right) V_1$$

The output voltage at the point *C* of Fig. 7.97 is

$$V_o = -\frac{R_f}{R_3} V_B = \frac{R_f}{R_3} \cdot \frac{R_f}{R_2}\left(1 + \frac{R_f}{R_1}\right) V_1$$

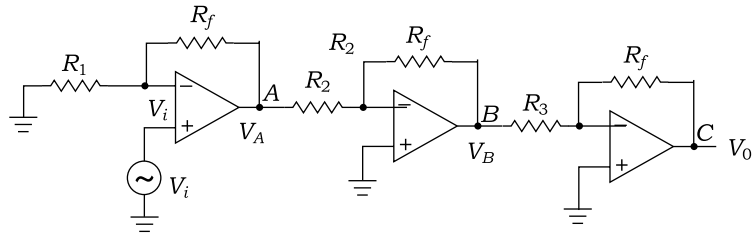


Fig. 7.97

After substituting the values of resistances R_f= 470 kΩ, R_1 = 4.3 kΩ, R_2 = 33 kΩ and R_3 = 33 kΩ for an input of 80 μV, we get

$$V_o = \frac{R_f}{R_3} \cdot \frac{R_f}{R_2}\left(1 + \frac{R_f}{R_1}\right)$$

$$= \frac{470}{33} \times \frac{470}{33} \times \left(1 + \frac{470}{4.3}\right) \times 80 \times 10^{-6}\ \text{V}$$

$$= 1.789\ \text{V}$$

Review Exercises

Short-Answer Questions

1. What is an adder amplifier?

Ans. An adder amplifier is an electronic circuit which generates an output voltage proportional to the algebraic sum of two or more input voltages multiplied by a constant gain.

2. What is an integrator?

Ans. An integrator is an electronic circuit that generates an output voltage which is the integration of input voltage.

3. Why is an OP-AMP used most commonly as an integrator and not as a differentiator?

Ans. When an OP-AMP is used as a differentiator at high frequency, gain is high. Then the high-frequency noise signal is amplified and more noise signal is present in output signal. Therefore, an OP-AMP is most commonly used as an integrator and not as a differentiator.

4. What will be the output of an integrator when a square-wave voltage signal is applied to an OP-AMP integrator?

Ans. When a square-wave voltage signal is applied to an OP-AMP integrator, the output of the integrator is a triangular wave.

5. What will be the output of an integrator when a sine-wave voltage signal is applied to an OP-AMP integrator?

Ans. When a sine-wave voltage signal is applied to an OP-AMP integrator, the output of the integrator is a cosine wave.

6. What will be the output of a differentiator when a square-wave voltage signal is applied to an OP-AMP differentiator?

Ans. When a square-wave voltage signal is applied to an OP-AMP differentiator, the output of differentiator is a spike pulse output wave.

7. What will be the output of a differentiator when a sine-wave voltage signal is applied to an OP-AMP differentiator?

Ans. When a sine-wave voltage signal is applied to an OP-AMP differentiator, the output of the differentiator is a cosine wave.

8. What is a current-to-voltage converter?

Ans. A current to voltage converter generates a voltage proportional to input current signal.

9. Why is the square-wave generator known as astable multivibrator?

Ans. Since the square-wave generator has two quasi-stable states, it is called an astable multivibrator.

10. Write the difference between a triangular wave and a sawtooth wave.

Ans. In a triangular wave, the rise time is always equal to its fall time, but in a sawtooth wave, the rise time is always different from its fall time.

11. What is a comparator? What are the applications of comparators?

Ans. A comparator is an electronic circuit which can compare an input voltage signal (V_{in}) with a known reference voltage (V_{ref}). It is basically an open-loop operational amplifier. The input voltage is applied to one of the input terminals of an OP-AMP and the reference voltage is applied at the other terminal of OP-AMP. Comparator is used in Schmitt triggers, analog-to-digital converters and oscillators or multivibrator circuits.

12. What is a zero-crossing detector?

Ans. Zero-crossing detectors are comparator with a reference voltage of zero volts. Diode clampers are used to protect the comparator circuit from large input voltage.

13. What is a Schmitt trigger?

Ans. A Schmitt trigger is comparator circuit with a positive feedback and it is used to convert an irregular waveform to a square waveform. This circuit is triggered every time when an input voltage is just greater than upper threshold voltage V_{UT} and is just lower than the threshold voltage $V_{LT.}$

14. Why is hysteresis required in a Schmitt trigger?

Ans. Hysteresis is required in a Schmitt trigger, to prevent noise from false triggering.

Multiple-Choice Questions

1. The linear application of an operational amplifier is
   (a) adder circuit (b) log amplifier
   (c) antilog amplifier (d) schmitt trigger
2. The non-linear application of an operational amplifier is
   (a) adder circuit (b) comparator
   (c) subtractor circuit (d) voltage-to-current converter
3. The output voltage of an inverting amplifier is
   (a) $V_o = -\frac{R_1}{R_f}V_1$ (b) $V_o = \frac{R_f}{R_1}V_1$
   (c) $V_o = -\frac{R_f}{R_1}V_1$ (d) $V_o = \left(1 + \frac{R_f}{R_1}\right)V_1$
4. The output voltage of a non-inverting amplifier is
   (a) $V_o = \left(1 + \frac{R_f}{R_1}\right)V_1$ (b) $V_o = \frac{R_f}{R_1}V_1$
   (c) $V_o = \left(1 - \frac{R_f}{R_1}\right)V_1$ (d) $V_o = \left(1 + \frac{R_1}{R_f}\right)V_1$
5. The output voltage of an OP-AMP circuit as shown in Fig. 7.98 is

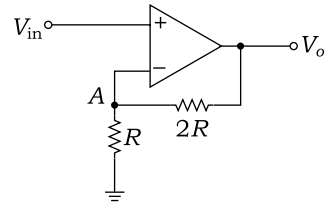


Fig. 7.98

(a) $V_o = 3\ V_{in}$ (b) $V_o = 2V_{in}$ (c) $V_o = -3V_{in}$ (d) $V_o = -V_{in}$

6. When $R_1 = R_2 = R_f = R$, the output voltage of an OP-AMP circuit as shown in Fig. 7.99 is

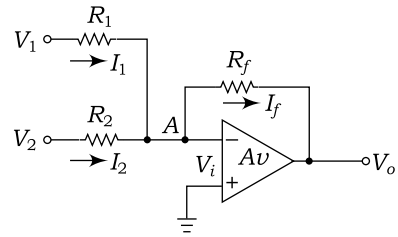


Fig. 7.99

(a) $V_o = -(V_1 + V_2)$ (b) $V_o = (V_1 + V_2)$ (c) $V_o = -(V_1 - V_2)$ (d) $V_o = (V_1 - V_2)$

7. Figure 7.98 shows an OP-AMP circuit. The output voltage of the OP-AMP is

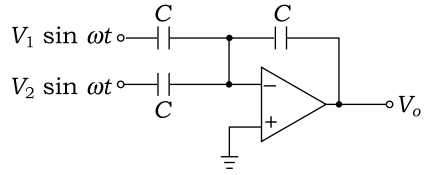


Fig. 7.100

(a) $V_o = (V_1 - V_2) \sin \omega t$ (b) $V_o = -(V_1 - V_2) \sin \omega t$
(c) $V_o = -(V_1 + V_2) \sin \omega t$ (d) $V_o = (V_1 + V_2) \sin \omega t$

8. The output voltage of a differentiator circuit using OP-AMP is

(a) $V_o(t) = -\frac{1}{R_1 C}\int_0^t V_{\text{in}} dt + V_0(0)$ (b) $V_o = -CR\frac{dV_{\text{in}}}{dt}$

(c) $V_o = CR\frac{dV_{\text{in}}}{dt}$ (d) $V_o(t) = \frac{1}{R_1 C}\int_0^t V_{\text{in}} dt + V_0(0)$

9. The output voltage of a integrator circuit using OP-AMP is

(a) $V_o(t) = -\frac{1}{R_1 C}\int_0^t V_{\text{in}} dt + V_0(0)$ (b) $V_o = -CR\frac{dV_{\text{in}}}{dt}$

(c) $V_o = CR\frac{dV_{\text{in}}}{dt}$ (d) $V_o(t) = \frac{1}{R_1 C}\int_0^t V_{\text{in}} dt + V_0(0)$

10. The Schmitt trigger circuit has
(a) positive feedback (b) negative feedback
(c) negative and positive feedback (d) None of these

11. The feedback element in a differentiator is
(a) a capacitor (b) an inductor (c) a diode (d) a resistance

12. The feedback element in an integrator is
(a) a capacitor (b) an inductor (c) a diode (d) a resistance

13. The inverting amplifiers can be used as
    (a) voltage followers (b) sample and hold circuits
    (c) buffers (d) summing amplifiers
14. When one of the input terminals of a comparator is connected with the ground, it becomes inverting amplifiers and can be used as
    (a) zero crossing detectors (b) sample-and-hold circuits
    (c) buffers (d) summing amplifiers
15. The log and antilog amplifiers can be used for
    (a) signal compression (b) multiplier
    (c) divider (d) summing amplifiers
16. An instrumentation amplifier
    (a) is a differential amplifier (b) has again less than 1
    (c) has very high output impedance (d) has low CMRR
17. The circuit shown in Fig. 7.101 uses an ideal OPAMP. For small positive values of V_i, the circuit works as
    (a) a half-wave rectifier (b) a differentiator
    (c) a logarithmic amplifier (d) an exponential amplifier

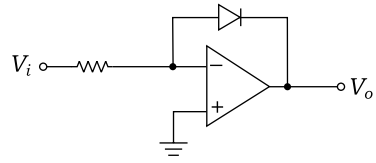


Fig. 7.101

Review Questions

1. What do you mean by a linear circuit? Give a list of linear applications of operational amplifiers.
2. What do you mean by a nonlinear circuit? What is the difference between linear circuit and nonlinear circuit? Write some nonlinear applications of operational amplifiers.
3. Draw the circuit diagram of an inverting amplifier. Derive the output voltage of an inverting amplifier in terms of input voltage and resistances.
4. Define a non-inverting amplifier. Write the difference between an inverting amplifier and non-inverting amplifier.
5. Explain the voltage-follower circuit. Justify the statement "voltage gain of the voltage-follower circuit is unity".
6. Explain the following amplifier circuits:
   (a) Inverting summing amplifier
   (b) Non-inverting summing amplifier
   (c) Difference amplifier
   (d) Adder cum subtractor circuit
7. Draw the circuit diagram of voltage-to-current converters and explain its operation.
8. Draw the circuit diagram of current-to-voltage converters and explain its operation. What are the applications of current-to-voltage converters?

9. Define integrator. What are the types of integrators? Write some applications of integrators.
10. Discuss the following integrators:
    (a) Inverting integrator
    (b) Non-inverting integrator
    (c) Practical integrator
    (d) Summing integrator amplifier
11. Define differentiator. Write some applications of a differentiator.
12. Explain the following differentiators:
    (a) Practical differentiator
    (b) Summing differentiator
13. Draw the circuit diagram of a logarithmic amplifier. Prove that the output voltage of a logarithmic amplifier is $V_O = -\frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}}$.
14. State the disadvantages of a logarithmic amplifier. Explain how the temperature-compensated logarithmic amplifier can reduce the disadvantages of a logarithmic amplifier.
15. Discuss antilog amplifier circuit using OP-AMP and transistor. Prove that the output voltage of an antilog amplifier is $V_O = -I_O R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right)$
16. Define analog multiplier. Draw a circuit to generate the output voltage $V_O = -I_O R_f \frac{V_1 V_2}{V_{\text{ref}}^2}$, where input voltages are V_1 and V_2.
17. Give a list for applications of multipliers. Discuss analog divider circuit. Prove that the output voltage of analog divider is $V_O \propto \left(\frac{V_2}{V_1}\right)$ where input voltages are V_1 and V_2.
18. Explain non-inverting comparators and inverting comparators. Write some disadvantages of comparator circuits.
19. What is the effect of noise in comparator circuits? Give a list for applications of comparator circuits.
20. Draw a practical Schmitt trigger circuit and explain its operation with waveforms. What is the difference between a comparator and Schmitt trigger?
21. Figure 7.102 shows the non-inverting amplifier, where R_1 = 10 kΩ, $R_L = R_f$ = 100 kΩ and V_1 = 5 V.
    Calculate (a) V_O, (b) gain, (c) I_1, (d) load current I_L, and (e) output current I_O.

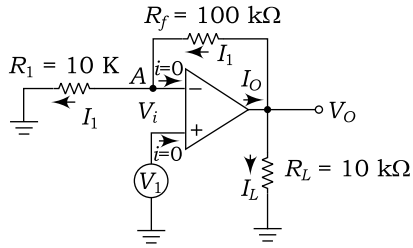


Fig. 7.102

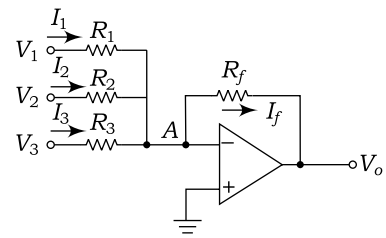


Fig. 7.103

22. Figure 7.103 shows an adder circuit with V_1 = 2 V, V_2 = –5 V and V_3 = 4 V. Determine the output voltage V_O. Assume R_1 = 20 kΩ, R_2 = 10 kΩ, R_3 = 20 kΩ and R_f = 10 kΩ

23. Implement the equation $V_o = -(6V_1 + 2V_2)$ using an operational amplifier circuit. Assume minimum value of resistance is 4.7 kΩ.
24. An operational amplifier circuit is shown in Fig. 7.104. Determine the output voltage V_O and current flows through R_1, R_2, R_3 and R_f. Assume $V_1 = 3$ V, $V_2 = -5$ and $V_3 = 2$ V

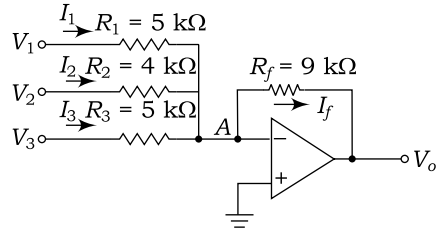


Fig. 7.104

25. Calculate the output voltage and common-mode rejection ratio (*CMRR*) of the differential amplifier as shown in Fig. 7.105. Assume $V_1 = 3$ V and $V_2 = 2$.

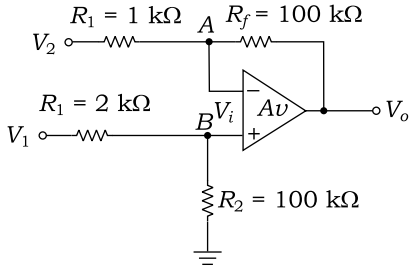


Fig. 7.105

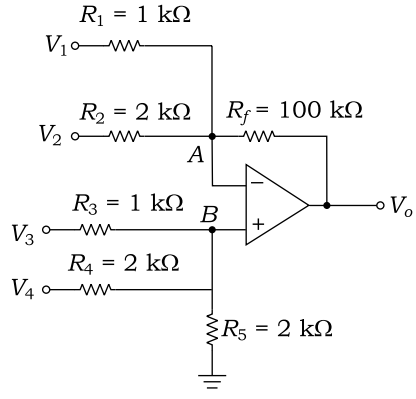


Fig. 7.106

26. Figure 7.106 shows an operational amplifier circuit. Determine the output voltage V_O. Assume $V_1 = 3$ V, $V_2 = -5$ V, $V_3 = 2$ V and $V_3 = -2$ V
27. In an integrator circuit, the value of *RC* is 1.5 second. Find out the output voltage at $t = 2$ seconds, $t = 4$ seconds and $t = 6$ seconds when input voltage is 5 V.
28. Figure 7.107 shows an integrator circuit. Find out the output voltage when input voltage is 5 sin 100 πt and show the output voltage waveform.
29. When a square wave, as shown in Fig. 7.108, is applied as input voltage to an integrator circuit, find out the output voltage. Assume $RC = 1$ second.

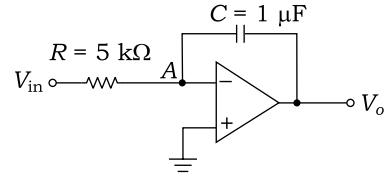


Fig. 7.107

30. Draw the output voltage waveform when input voltage of differentiation circuit is $V_{in} = 4 \sin 1000 \pi t$. Assume $CR = 0.01$ second.
31. When a square-wave input voltage as shown in Fig. 7.109 is applied to the differentiation circuit, what will be the output voltage waveform?

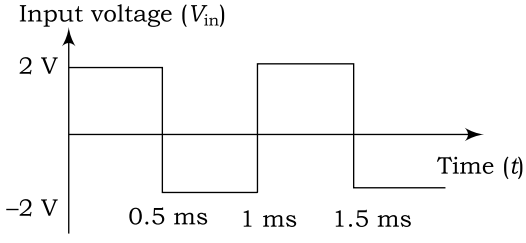


Fig. 7.108

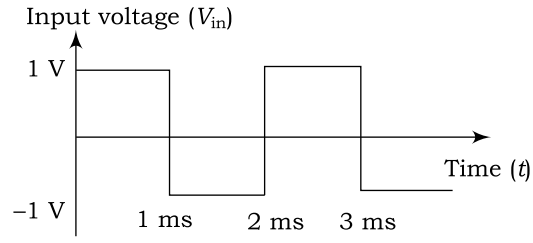


Fig. 7.109

32. Determine the output voltage V_O of a log amplifier using OP-AMP and transistor as shown in Fig. 7.110. Assume V_{in} = 500 mV, R = 10 kΩ, T = 290 K and $I_S = 10^{-13}$ A

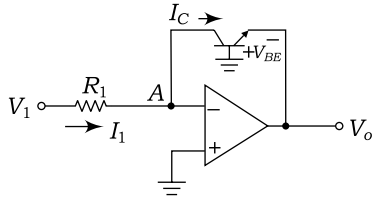


Fig. 7.110

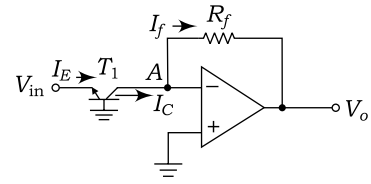


Fig. 7.111

33. Compute the output voltage V_O of an antilog amplifier using OP-AMP and transistor as shown in Fig. 7.111. Assume V_{in} = 200 mV, R_f = 10 K, τ = 1, V_T = 20 mV and $I_O = 10^{-13}$A
34. Figure 7.112 shows a comparator circuit where $V_{Z1} = V_{Z2}$ 10 V, V_D = 0.6 V, V_{ref} = +3 V, saturation voltage ±14 V, and $V_{in} = 2 \sin \omega t$.

    Draw the output voltage waveform.

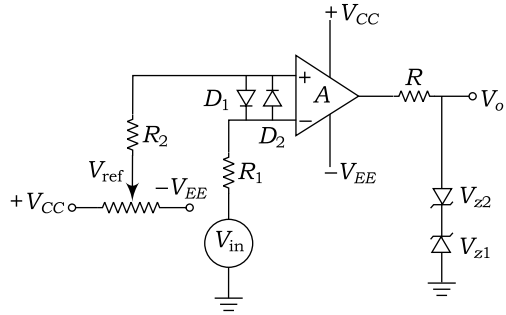


Fig. 7.112

35. A Schmitt trigger circuit is shown in Fig. 7.113 where R_1 = 12 kΩ, R_2 = 6 kΩ, V_{ref} = +4 V, saturation voltage ±15 V, and $V_{in} = 10 \sin \omega t$.
    (a) Find the threshold voltages V_{UT} and V_{LT} and determine hysteresis width V_H.
    (b) Show the output voltage waveform.

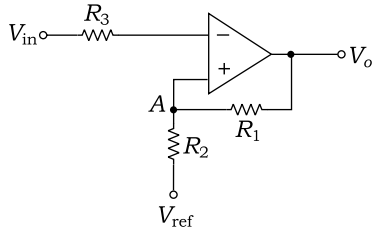


Fig. 7.113 Schmitt trigger circuit

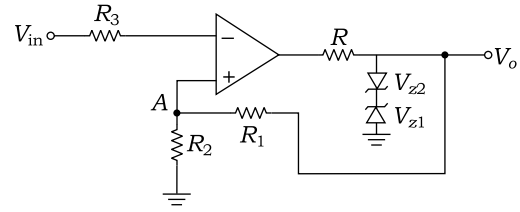


Fig. 7.114

36. In a Schmitt trigger circuit as shown in Fig. 7.114, $R_1 = 10$ kΩ, $R_2 = 5$ kΩ, $V_{in} = 5 \sin \omega t$, and saturation voltage ±15 V. Assume $V_{Z1} = V_{Z2} = 10$ V, $V_D = 0.6$ V
    (a) Determine the threshold voltage V_{UT} and V_{LT}. Calculate hysteresis width V_H.
    (b) Find the output voltage waveform.
37. Draw the circuit diagram of logarithmic amplifier and explain its operation.
38. Write short notes on the following
    (a) Precision rectifier
    (b) V-I and I-V converters
    (c) Logarithmic amplifier
39. What are the criteria of a good instrumentation amplifier?
40. Explain the operation of an inverting Schmitt trigger circuit. For the inverting Schmitt trigger circuit shown in Fig. 7.115, calculate R_z if $R_1 = 10$ kΩ and hysteresis voltage width = 4V. Assume saturation voltage to be +14 V and –14 V.
41. Draw the circuit diagram of a voltage to current converter and explain its operation.
42. Obtain the expression for output voltage of an integrator using OPAMP.
43. Draw the output waveforms if input of a differentiator is
    (i) Triangular wave
    (ii) Square wave

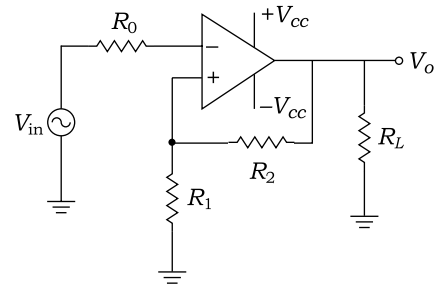


Fig. 7.115

44. With the circuit diagram, discuss the operation of an instrumentation amplifier and derive its gain equation. Discuss its merit and application.
45. Describe the function of an OPAMP on (i) an inverter (ii) an adder (iii) an integrator (iv) a differentiator and (v) an amplifier.
46. Realize multiplier using logarithmic amplifier. Mention application of analog multiplier.
47. Design a circuit to implement the function $f = 3x + \log x$

ANSWERS

Multiple-Choice Questions

1. (a)	2. (b)	3. (c)	4. (a)	5. (a)	6. (a)	7. (c)
8. (b)	9. (a)	10. (a)	11. (d)	12. (a)	13. (d)	14. (a)
15. (a,b,c)	16. (a)	17. (c)				

CHAPTER

8

Power Amplifier

8.1 INTRODUCTION

The small-signal analysis of a BJT amplifier circuit is discussed so far in Chapter 3. These small-signal amplifiers are used in early stages of any signal processing systems. These amplifiers are designed to provide good voltage gain; hence these amplifiers are known as *voltage amplifiers*. In the final stage of a signal-processing system, the output signal of the last-stage amplifier should drive a load such as a loudspeaker or a dc servo motor, which handles sufficient power. To get sufficient power, a large swing of voltage and current is required. Therefore, a *power amplifier* is required to handle a large swing of voltage and current.

Generally, a large-signal amplifier is capable of providing a substantial amount of power to a load such as a loudspeaker or a dc servo drive, etc. The large-signal amplifier is also known as power amplifier.

Usually, the power amplifier is used in the last stage of a public address system. A public address system consists of a microphone, multistage voltage amplifiers, power amplifier and a speaker as shown in Fig. 8.1. The microphone can convert sound signal to electrical signal within very low voltage of about few millivolts. This signal cannot drive the loudspeaker. Therefore, the output signal of a microphone is fed to a multi-stage amplifier for amplification. Then the multistage amplifier amplifies the ac input signal and the output received is used to drive the power amplifier as it has the capability to deliver a large amount of power to the speaker. The difference between a voltage amplifier and power amplifier is given in Table 8.1.

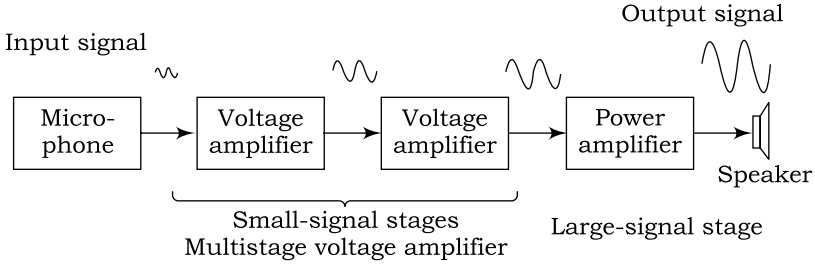


Fig. 8.1 Public address system

Table 8.1 Difference between voltage amplifier and power amplifier

Voltage Amplifier	*Power Amplifier*
A small-signal amplifier can use only 10% of ac load line for operation. These amplifiers are known as voltage amplifiers.	A large-signal amplifier uses a large part of ac load line for proper operation.
The current gain β of a transistor used in voltage amplifier is very large. The typical value of β is about 100.	The current gain β of a transistor used in a power amplifier is less than a voltage amplifier. The typical value of β is in the range of 20 to 50.
The input resistance of a voltage amplifier is low compared to output resistance.	The input resistance of a power amplifier is very large compared to output resistance.
The size of transistor used in a voltage amplifier is small. These transistors are known as low- or medium-power transistors.	The size of a transistor used in a power amplifier is large. A certain amount of heat is dissipated within the transistor, provided with a large cooling surface area required for heat dissipation. These transistors are known as power transistors.
In a voltage amplifier, *RC* coupling is used for inter-stage connection.	Transformer coupling is used for a power amplifier.
For analysis of small-signal amplifiers, the *h*-parameter (linear) model of a transistor is used.	For analysis of large-signal amplifiers, the output characteristic graphs of a transistor is used. The nonlinearity existing due to the output characteristics are not equidistant.

8.2 CLASSIFICATION OF POWER AMPLIFIERS

Based on transistor biasing condition and amplitude of input signal, the power amplifiers are classified as Class A, Class B, Class AB and Class C power amplifiers.

1. Class A Amplifier

In a Class A amplifier, the transistor bias and the amplitude of input signal is such that the output current flows for the complete cycle (360°) of the ac signal as shown in Fig. 8.2.

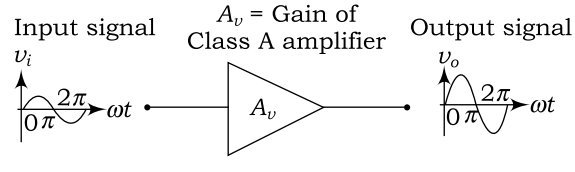


Fig. 8.2 Class A amplifier

2. Class B Amplifier

In a Class B amplifier, the transistor bias and the amplitude of input signal is such that the output current flows for one-half cycle (180°) of the ac signal as shown in Fig. 8.3.

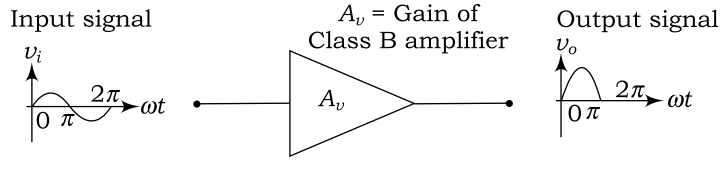


Fig. 8.3 Class B amplifier

3. Class AB Amplifier

In a Class AB amplifier, the transistor bias and the amplitude of input signal is such that the output current flows for more than half-cycle (180°) but less than the complete cycle (360°) of the ac signal.

4. Class C Amplifier

In a Class C amplifier, the transistor bias and the amplitude of input signal is such that the output current flows for less than one-half cycle (180°) of the ac signal as shown in Fig. 8.4.

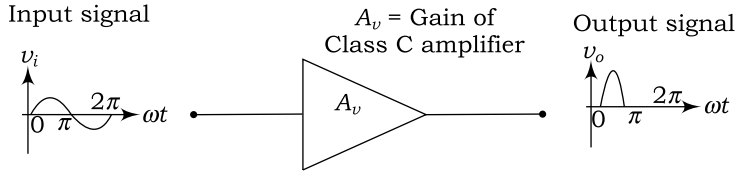


Fig. 8.4 Class C amplifier

8.3 CLASS A LARGE-SIGNAL AMPLIFIER

Figure 8.5 shows a common-emitter amplifier which can be used as the Class A amplifier. The transistor is used as a power amplifier; it has capability of operating in the range of few watts. This is called *series fed* as the load resistance R_L is connected directly in series with the collector of the transistor T_1. The resistances R_1, R_2, R_E and the capacitor C_E provide the biasing. In the Class A amplifier, the transistor biasing condition is such that the output current flows for the complete cycle 360° of the ac signal. The Q-point will be in the middle of load line.

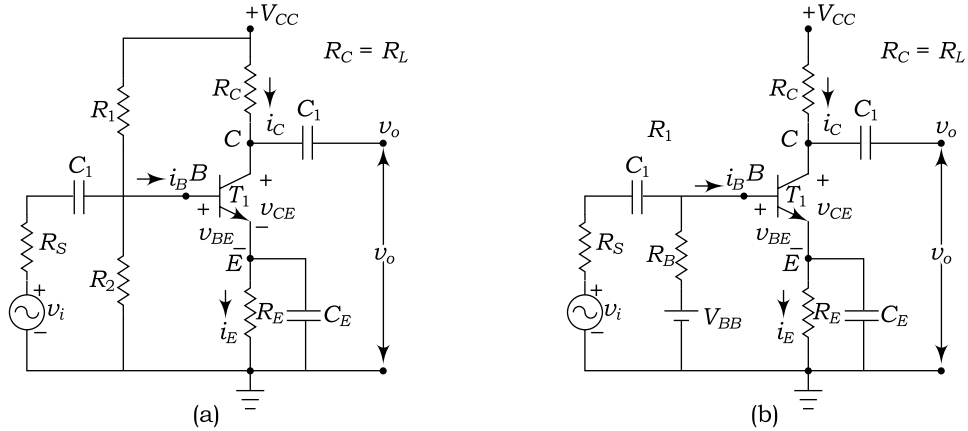


Fig. 8.5 (a) Class A amplifier (b) Alternative representation of Fig. 8.5(a)

Figure 8.5(b) shows the schematic diagram of the circuit as shown in Fig. 8.5(a) where R_B is the biasing resistance and V_{BB} is the biasing voltage. Actually $R_B = R_1 \| R_2 = \dfrac{R_1 R_2}{R_1 + R_2}$ and $V_{BB} = \dfrac{R_2}{R_1 + R_2} V_{CC}$.

Figure 8.6 shows the variation of the collector current i_C and the collector emitter voltage v_{CE}. When v_s is sinusoidal ac input voltage, the base current i_B, the output current i_C and output voltage v_o are also sinusoidal. At the operating point Q, I_{CQ} is quiescent collector current and V_{CEQ} is quiescent collector emitter voltage.

Assume that I_B, i_b and i_B are dc base current, ac base current and total base current respectively. It is also assumed that I_C, i_c and i_C are dc collector current, ac collector current and total collector current correspondingly.

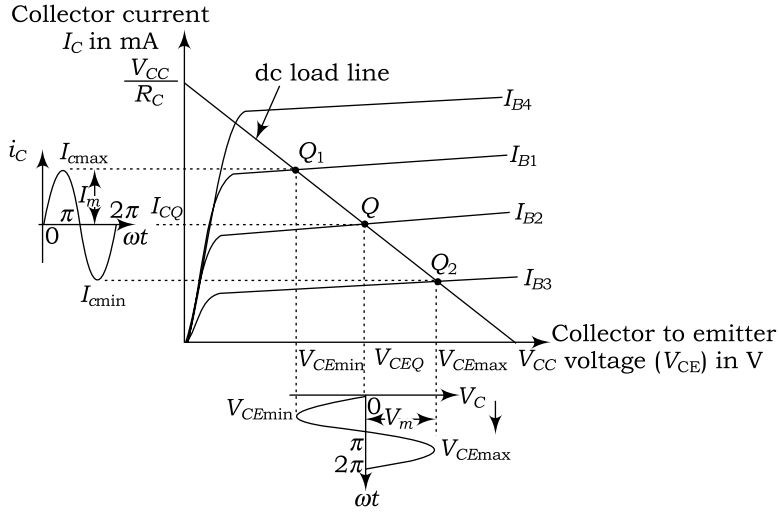


Fig. 8.6 Transistor output characteristics with dc load line, output collector current i_C and output collector-emitter voltage v_c

The maximum collector current is equal to $I_{C\max} = I_{CQ} + I_m$

The maximum collector current is $I_{C\min} = I_{CQ} - I_m$.

Therefore, $$I_m = \frac{I_{C\max} - I_{C\min}}{2} \tag{8.1}$$

The maximum collector-to-emitter voltage is equal to $V_{CE\max} = V_{CEQ} + V_m$

The minimum collector-to-emitter voltage is $V_{CE\min} = V_{CEQ} - V_m$.

Then, $$V_m = \frac{V_{CE\max} - V_{CE\min}}{2}. \tag{8.2}$$

The power output is $P = V_C I_C = I_C R_L \times I_C = I_C^2 R_L$

where, V_C is the rms value of output voltage v_c,

I_C is rms value of output current i_C, and $V_C = I_C R_L$

Since $V_C = \frac{V_m}{\sqrt{2}}$ and $I_C = \frac{I_m}{\sqrt{2}}$, we obtain

$$P = V_C I_C = \frac{V_m}{\sqrt{2}} \frac{I_m}{\sqrt{2}} = \frac{V_m I_m}{2} = \frac{I_m R_L \times I_m}{2} = \frac{I_m^2 R_L}{2} = \frac{V_m^2}{2R_L} \quad \text{as } V_m = I_m R_L \tag{8.3}$$

V_C and I_C are the rms values of the output voltage v_C and current i_C.

$$I_C = \frac{I_m}{\sqrt{2}} = \frac{I_{C\max} - I_{C\min}}{2\sqrt{2}} \quad \text{as} \quad I_m = \frac{I_{C\max} - I_{C\min}}{2}$$

$$V_C = \frac{V_m}{\sqrt{2}} = \frac{V_{CE\max} - V_{CE\min}}{2\sqrt{2}} \quad \text{as} \quad V_m = \frac{V_{CE\max} - V_{CE\min}}{2}$$

After substituting the values of V_C and I_C, we get

$$P = V_C I_C = \frac{V_{CE\max} - V_{CE\min}}{2\sqrt{2}} \times \frac{I_{C\max} - I_{C\min}}{2\sqrt{2}} = \frac{(V_{CE\max} - V_{CE\min})(I_{C\max} - I_{C\min})}{8} \quad (8.4)$$

The disadvantages of this circuit are given below:

1. Since the quiescent current I_{CQ} flows through the load resistance, there will be a certain power loss in the load resistance.
2. It is not preferable to pass dc current through load such as a loudspeaker.

8.4 CLASS A TRANSFORMER-COUPLED AUDIO POWER AMPLIFIER

In Fig. 8.5, the load resistance is connected directly in the output circuit of the power stage. As a result, the quiescent current passes through the load resistance and a certain amount of power will be wasted. This wasted power does not contribute to the ac signal component of power. Hence, the efficiency of the amplifier decreases. Usually, it not desirable to pass the dc component of current through the output device or load such as the voice coil of a loudspeaker. This problem can be solved by using a transformer which provides coupling between the load and amplifier. Figure 8.7 shows a transformer-coupled transistor amplifier. The primary winding of the transformer having negligible dc resistance is connected in the collector of transistor. The secondary winding of transformer is connected with load. As the load is not directly connected to the collector of transistor, the dc collector current cannot pass through the load. Therefore, the dc power loss in the load is zero.

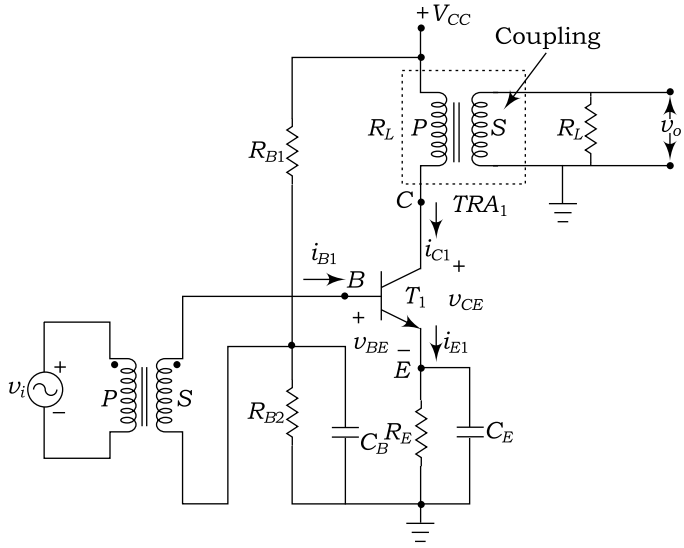


Fig. 8.7 Transformer-coupled Class A amplifier

Impedance Matching

To transfer sufficient amount of power to a load such as a loudspeaker with a voice coil, having an impedance of 5 Ω to 20 Ω, it is required to use an output impedance-matching transformer. Otherwise, the internal device resistance will be much higher than that of the loudspeaker and most of the power generated will be lost in the active device.

The impedance matching properties of ideal transformer should follow the following equations:

$$V_1 = \frac{N_1}{N_2} V_2 \text{ and } I_1 = \frac{N_2}{N_1} I_2 \text{ as } \frac{V_1}{V_2} = \frac{N_1}{N_2} \text{ and } V_1 I_1 = V_2 I_2 \tag{8.8}$$

where, V_1 is the primary voltage and V_2 secondary voltage,
I_1 is the primary current and I_2 secondary current, and N_1 is the primary number of turns and N_2 secondary number of turns

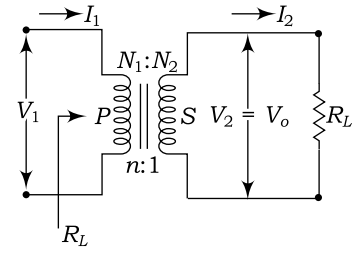


Fig. 8.8 Impedance-matched transformer

When $n = \frac{N_1}{N_2}$ is turns ratio, we can write $\frac{V_1}{I_1} = n^2 \frac{V_2}{I_2}$

As the effective load resistance in the primary side of the transformer (Fig. 8.8) is $R'_L = \frac{V_1}{I_1}$ and the actual load resistance is $R_L = \frac{V_2}{I_2}$, we can write $R'_L = n^2 R_L$

It is clear from the above equation that the effective load resistance R'_L appearing at the collector terminal of the transistor is n^2 times the load resistance connected to the secondary.

8.5 EFFICIENCY OF CLASS A LARGE-SIGNAL AMPLIFIER

The amplifier is supplying power to a pure resistive load. The average power input from dc supply is $V_{CC}I_C$.

The power absorbed by the output circuit is $I_C^2 R_L + V_c I_c$ where, V_c and I_c are the rms output voltage and current respectively. When the average power P_D is dissipated by active device, as per conservation of energy, we can write

$$V_{CC} I_C = I_C^2 R_L + V_c I_c + P_D \tag{8.8a}$$

At dc biasing condition, $V_{CC} = I_C R_L + V_C$

After substituting the value of $V_{CC} = I_C R_L + V_C$ in Eq. (8.8a), we get $(I_C R_L + V_C) I_C = I_C^2 R_L + V_c I_c + P_D$.

Then average power is dissipated by active device $P_D = V_C I_C - V_c I_c$.

8.5.1 Conversion Efficiency

It is the measure of the ability of an active device to convert the dc power of the supply into the ac power delivered to the load. It is also known as *theoretical efficiency* or *collector circuit efficiency* and it is represented by η. Then the percentage efficiency is equal to

$$\eta = \frac{\text{ac power delivered to load}}{\text{dc power supplied to output circuit}} \times 100\%$$

Since ac power delivered to load is P = rms.output.voltage × rms.output.current $= \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} = \frac{V_m I_m}{2}$ and dc power supplied to output circuit is equal to $V_{CC}I_C$, the efficiency of amplifier can be expressed as

$$\eta = \frac{\frac{V_m I_m}{2}}{V_{CC} I_C} \times 100\% = 50 \frac{V_m I_m}{V_{CC} I_C}\% \tag{8.9}$$

where, $V_m = \frac{V_{CE\max} - V_{CE\min}}{2}$ and $I_m = \frac{I_{C\max} - I_{C\min}}{2}$

The collector circuit efficiency differs from the overall efficiency as the power taken by the base does not incorporated in the denominator of Eq. (8.9).

8.5.2 Maximum Efficiency

Figure 8.9 shows the quiescent point and the load line to determine maximum efficiency. To obtain the maximum efficiency, the amplifier must be driven to its complete swing. In this condition, the $I_{C\,\min}$ and $V_{CE\,\min}$ are about zero.

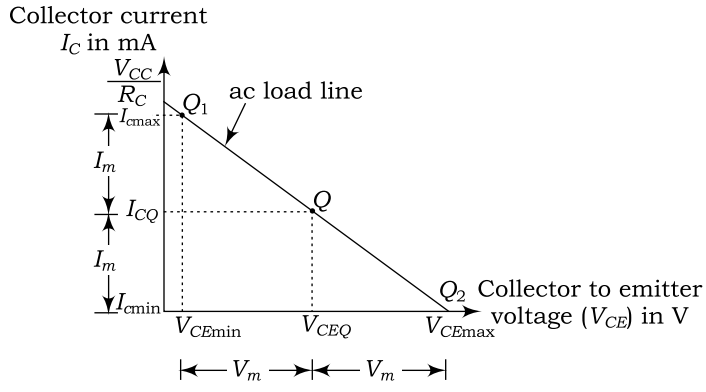


Fig. 8.9 Quiescent point and the load line to determine maximum efficiency

Since $I_m = \dfrac{I_{C\max}}{2} = I_{CQ} = I_C$, Eq. (8.9) can be written as

$$\eta = 50 \frac{\dfrac{V_{CE\,\max} - V_{CE\,\min}}{2} I_{CQ}}{V_{CC} I_{CQ}} \%$$

or $$\eta = 25 \frac{V_{CE\,\max} - V_{CE\,\min}}{V_{CC}} \% = 25 \frac{V_{CE\,\max}}{V_{CC}} \% \quad \text{as } V_{CE\,\max} >> V_{CE\,\min} \text{ and } V_{CE\,\min} \approx 0 \tag{8.10}$$

8.5.3 Series-Fed Load

In series load, the maximum value of $V_{CE\max}$ can be equal to V_{CC}.

Then efficiency is equal to $\eta = 25 \dfrac{V_{CC}}{V_{CC}} \% = 25\%$

Therefore, the maximum efficiency of a Class A amplifier with series-fed load is about 25%.

8.5.4 Transformer-Coupled Load

In transformer-coupled load, $V_{CC} = V_{CEQ} = \dfrac{V_{CE\,\max} + V_{CE\,\min}}{2}$

Then $$\eta = 25 \frac{V_{CE\,\max} - V_{CE\,\min}}{V_{CC}} \%$$

$$= 50 \frac{V_{CE\,\max} - V_{CE\,\min}}{V_{CE\,\max} + V_{CE\,\min}} \% \tag{8.11}$$

if $V_{CE\min} \to 0$, $\eta = 50\%$

Hence, the maximum efficiency of a Class A amplifier with transformer-coupled load is about 50%. Actually, in a series-fed load, there is continuous wastage of power in R_L due to quiescent current. In case of transformer-coupled load, the primary winding has negligible dc resistance and the power loss due to quiescent current is negligible. Consequently, the efficiency of a Class A amplifier with a transformer-coupled load is more than that with a series-fed load.

8.6 HARMONIC DISTORTION

The most important requirement of an amplifier is that the waveform of the output voltage should be the reproduction of input voltage in amplified form. But practically, the output voltage is amplified input voltage and the wave shape is slightly distorted as compared to input signal waveform. Therefore, if input voltage is completely sinusoidal, the output voltage waveform will be nonsinusoidal.

The transfer characteristic of an amplifier is the relationship between input signal (base current i_b) and output signal (collector current i_c). When the transfer characteristic is linear, the output signal will be sinusoidal with sinusoidal input signal. This can be expressed as

$$i_c = K_1 i_b \tag{8.12}$$

where, base current is $i_b = I_{bm} \cos \omega t$, and

i_c is collector current due to i_b.

Actually, the transfer characteristic of an amplifier is nonlinear. Due to the nonlinear characteristic, one half of the input signal is amplified more than the other half of input signal. Then the output signal contains a dc component along with fundamental component and harmonics. Frequencies which are integral multiples of input fundamental frequency signal are called *harmonics*. Due to presence of harmonics in output signal, the output voltage waveform will be distorted. This is called *harmonic distortion*. Usually, the type of distortion is analysed using Fourier series.

8.6.1 Second Harmonic Distortion

Figure 8.10 shows the dynamic transfer characteristics, which is nonlinear over the region of operation. This parabolic equation and the output voltage is different from input voltage and output is distorted in nature. This distortion is called *nonlinear distortion* or *amplitude distortion*. The output signal consists of fundamental and higher harmonics.

The relationship between ac collector current i_c and the input base current i_b is given by

$$i_c = K_1 i_b + K_2 i_b^2$$

where K_1 and K_2 are constant.

Since the base current is $i_b = I_{bm} \cos \omega t$, the collector current is

$$i_c = K_1 I_{bm} \cos \omega t + K_2 I_{bm}^2 \cos^2 \omega t \tag{8.13}$$

As $2 \cos^2 \omega t = 1 + \cos 2\omega t, \cos^2 \omega t = \frac{1}{2} + \frac{1}{2} \cos 2\omega t$

After substituting the value of $\cos^2 \omega t$ in Eq. (8.13), we get

$$i_c = K_1 I_{bm} \cos \omega t + K_2 I_{bm}^2 \left(\frac{1}{2} + \frac{1}{2} \cos 2\omega t \right)$$

$$i_c = K_1 I_{bm} \cos \omega t + \frac{1}{2} K_2 I_{bm}^2 + \frac{1}{2} K_2 I_{bm}^2 \cos 2\omega t$$

or $$i_c = B_o + B_1 \cos \omega t + B_2 \cos 2\omega t \quad \text{as} \quad B_o = \frac{1}{2} K_2 I_{bm}^2,$$

$$B_1 = K_1 I_{bm} \text{ and } B_2 = \frac{1}{2} K_2 I_{bm}^2 \tag{8.14}$$

Since the total collector current is sum of the ac collector current i_c and the quiescent collector current I_{CQ}, we can express $i_C = I_{CQ} + i_c$

Then $$i_C = I_{CQ} + B_o + B_1 \cos \omega t + B_2 \cos 2\omega t$$

or $$i_C = (I_{CQ} + B_o) + B_1 \cos \omega t + B_2 \cos 2\omega t \tag{8.15}$$

where, I_{CQ} is the dc component of collector current,
B_o is extra dc component due to rectification,
B_1 is amplitude of fundamental component, and
B_2 is amplitude of second harmonic component.

The values of B_o, B_1 and B_2 can be determined graphically using three-point method.

As per Fig. 8.10, we can find the value of collector current at $\omega t = 0$, $\omega t = \pi/2$ and π.

$$\text{At } \omega t = 0,\ i_C = I_{\max} \quad \text{and } I_{\max} = I_{CQ} + B_o + B_1 + B_2 \tag{8.16}$$

$$\text{At } \omega t = \pi/2,\ i_C = I_{CQ} \text{ and } \quad I_{CQ} = I_{CQ} + B_o - B_2 \tag{8.17}$$

$$\text{At } \omega t = \pi,\ i_C = I_{\min} \quad \text{and } \quad I_{\min} = I_{CQ} + B_o - B_1 + B_2 \tag{8.18}$$

After solving the Eq. (8.17), we find $B_o = B_2$

After subtraction Eq. (8.18) from Eq. (8.16), we obtain

$$B_1 = \frac{I_{\max} - I_{\min}}{2}$$

By using the value of B_1 and Eq. (8.16), we get $$B_o = B_2 = \frac{I_{\max} + I_{\min} - 2I_{CQ}}{2} \tag{8.19}$$

The second harmonic distortion is represented by D_2 which is the ratio of magnitude of the second harmonic component to the fundamental component. It is expressed by

$$D_2 \equiv \frac{|B_2|}{|B_1|} \text{ and the percentage of second harmonic is } D_2 \equiv \frac{|B_2|}{|B_1|} \times 100\% . \tag{8.20}$$

8.6.2 Higher Order Harmonic Distortion

In case of very limited distortion, the fundamental as well as the second harmonic component will be present in the output voltage. When the amplitude of a signal is very large, the transfer characteristic is nonlinear. The total harmonic distortion for large signals can be derived by the five-point method. Due to increased curvature of the dynamic transfer characteristics curve, the collector current can be expressed as

$$i_c = K_1 i_b + K_2 i_b^2 + K_3 i_b^3 + K_4 i_b^4 + \cdots \tag{8.21}$$

where K_1, K_2, K_3 and K_4 are constant.

Since the base current is $i_b = I_{bm} \cos \omega t$, the collector current is

$$i_c = K_1 I_{bm} \cos \omega t + K_2 I_{bm}^2 \cos^2 \omega t + K_3 I_{bm}^3 \cos^3 \omega t + K_4 I_{bm}^4 \cos^4 \omega t + \cdots$$

The above equation can be written as

$$i_c = B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + B_4 \cos 4\omega t + \cdots \tag{8.22}$$

As the total collector current is sum of the ac collector current i_c and the quiescent collector current I_{CQ}, we can express $i_C = I_{CQ} + i_c$

Then $$i_C = I_{CQ} + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + B_4 \cos 4\omega t + \cdots \quad (8.23)$$

The values of B_o, B_1, B_2, B_3 and B_4 can be determined graphically using the five-point method.

As per Fig. 8.10, we can find the value of collector current at $\omega t = 0$, $\omega t = \pi/3$, $\omega t = \pi/2$, $\omega t = 2\pi/3$ and $\omega t = \pi$.

At $\omega t = 0$, $i_C = I_{\max}$

At $\omega t = \pi/3$, $i_C = I_{\frac{1}{2}}$

At $\omega t = \pi/2$, $i_C = I_{CQ}$

At $\omega t = 2\pi/3$, $i_C = I_{-\frac{1}{2}}$

At $\omega t = \pi$, $i_C = I_{\min}$

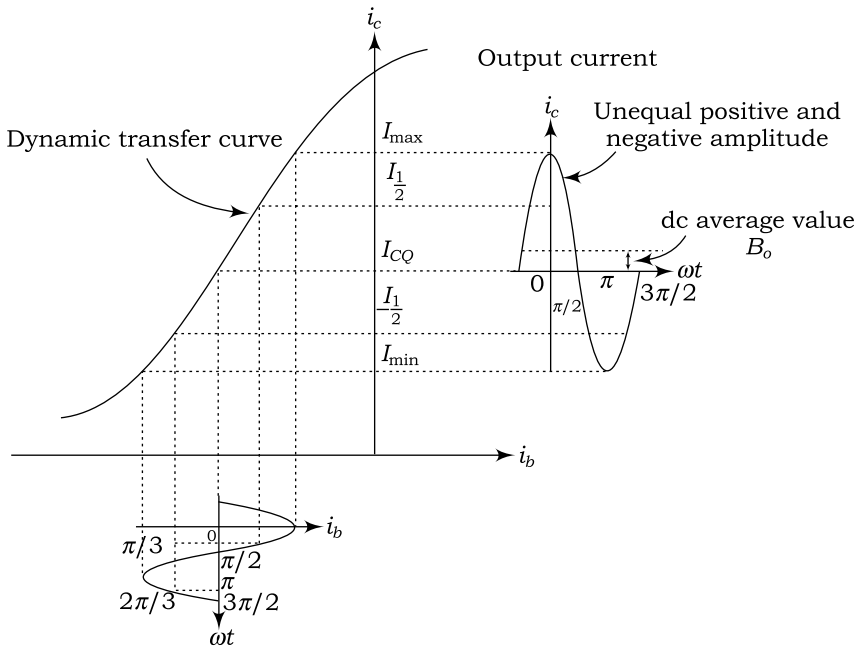


Fig. 8.10 Dynamic transfer curve with input current i_b and output current i_c

After substituting the above values of i_C in Eq. (8.23), we get five different equations. After solving these equations, we obtain

$$B_o = \frac{1}{6}(I_{\max} + 2I_{1/2} + 2I_{-1/2} + I_{\min}) - I_{CQ} \quad (8.24)$$

$$B_1 = \frac{1}{3}(I_{\max} + I_{1/2} - I_{-1/2} - I_{\min})$$

$$B_2 = \frac{1}{4}(I_{\max} - 2I_{CQ} + I_{\min})$$

$$B_3 = \frac{1}{6}(I_{\max} - 2I_{1/2} + 2I_{-1/2} - I_{\min})$$

$$B_4 = \frac{1}{12}(I_{\max} - 4I_{1/2} + 6I_{CQ} - 4I_{-1/2} + I_{\min})$$

Then second harmonic distortion is $D_2 \equiv \frac{|B_2|}{|B_1|}$,

third harmonic distortion is $D_3 \equiv \frac{|B_3|}{|B_1|}$, and

fourth harmonic distortion is $D_4 \equiv \frac{|B_4|}{|B_1|}$.

8.6.3 Power Output

When the distortion is negligible, the power output at the fundamental frequency is

$$P_1 = \frac{1}{2} B_1^2 R_L \,. \tag{8.25}$$

The power delivered at second harmonic frequency is $P_2 = \frac{1}{2} B_2^2 R_L$. Similarly, other higher harmonics power can be computed. The total power output is the sum of power output at each harmonics and it can be expressed as

$$P = P_1 + P_2 + P_3 + P_4 + \cdots$$

$$P = \frac{1}{2} B_1^2 R_L + \frac{1}{2} B_2^2 R_L + \frac{1}{2} B_3^2 R_L + \frac{1}{2} B_4^2 R_L + \cdots$$

Since $P_1 = \frac{1}{2} B_1^2 R_L, P_2 = \frac{1}{2} B_2^2 R_L, P_3 = \frac{1}{2} B_3^2 R_L$ and $P_4 = \frac{1}{2} B_4^2 R_L$

$$P = \frac{1}{2} B_1^2 R_L + \frac{1}{2} B_2^2 R_L + \frac{1}{2} B_3^2 R_L + \frac{1}{2} B_4^2 R_L + \cdots$$

or $$P = (B_1^2 + B_2^2 + B_3^2 + B_4^2 + \cdots) \frac{1}{2} R_L$$

$$= \left(1 + \frac{B_2^2}{B_1^2} + \frac{B_3^2}{B_1^2} + \frac{B_4^2}{B_1^2} + \cdots \right) \frac{1}{2} B_1^2 R_L$$

$$= (1 + D_2^2 + D_3^2 + D_4^2 + \cdots) P_1 \quad \text{as} \quad D_2^2 = \frac{B_2^2}{B_1^2}, D_3^2 = \frac{B_3^2}{B_1^2}, D_4^2 = \frac{B_4^2}{B_1^2} \text{ and } P_1 = \frac{1}{2} B_1^2 R_L \tag{8.26}$$

Then $P = (1 + D^2)P_1$ where total harmonic distortion or distortion factor is

$$D = \sqrt{(D_2^2 + D_3^2 + D_4^2 + \cdots)} \tag{8.27}$$

If the distortion factor is 10%, the power output $P = (1 + 0.1^2)P_1 = 1.01P_1$ (8.28)

Therefore, the power output contains higher harmonics power which is only 1% of the fundamental power.

8.7 CLASS B LARGE-SIGNAL AMPLIFIER

In a Class B amplifier, the transistor is biased in such a way that it remains forward biased only for positive half-cycle of input signal and its conduction angle is 180°. The operating *Q*-point is set at cut-off or lower end of load line. During positive half-cycle of the input signal, transistor is forward biased and collector current

flows. In the same way, during negative half-cycle of the input signal, the transistor is reverse biased and collector current becomes zero.

Figure 8.11 shows the graphical construction to determine the output voltage waveforms of a Class B transistor amplifier. Assume that the dynamic transfer curve is a straight line and the minimum collector current is zero. When a sinusoidal ac voltage is applied, the output is sinusoidal during the positive half-cycle of the input signal and output is zero during negative half cycle of input signal.

If load resistance R_L is connected across the secondary of the transformer TRA_1, the effective load resistance referred to primary is $R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = n^2 R_L$ where, $\left(\frac{N_1}{N_2}\right) = n$

Figure 8.11 shows the output waveforms for the transistor T_1. The output of transistor T_2 is in series of sine loop pulses and 180° out of phase with respect to output of T_1.

The power output is

$$P = V_{\text{rms}} I_{\text{rms}} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} = \frac{V_m I_m}{2} = \frac{I_m}{2}(V_{CC} - V_{\min}) \quad \text{as } V_m = V_{CC} - V_{\min} \tag{8.29}$$

The dc current in each transistor under load is the average value of sine wave.

Then
$$I_{\text{dc}} = \frac{1}{2\pi}\int_0^{\pi} I_{C\max} \sin \omega t \cdot d\omega t = \frac{1}{2\pi}\int_0^{\pi} I_{C\max} \sin\theta \cdot d\theta = \frac{I_{C\max}}{2\pi}[-\cos\theta]_0^{\pi} = \frac{I_{C\max}}{\pi} \tag{8.30}$$

The total dc current for two transistors used in a push-pull system is $\frac{2I_{C\max}}{\pi}$ and dc power supplied to output circuit is equal to $P_i = 2V_{CC} I_{\text{dc}} = \frac{2V_{CC} I_{C\max}}{\pi}$

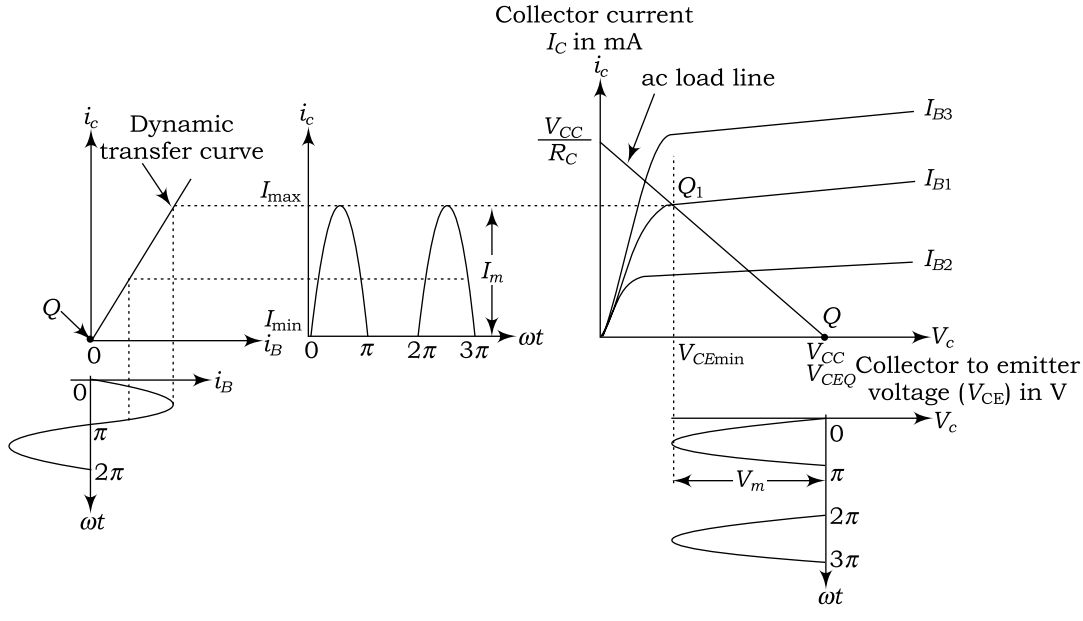


Fig. 8.11 Graphical construction to determine output voltage of a Class B amplifier

The efficiency is equal to $\eta = \frac{P}{P_i} \times 100\% = \frac{I_{C\max}}{2}(V_{CC} - V_{\min}) \times \frac{\pi}{2V_{CC}I_{C\max}} \times 100\%$

$$= \frac{\pi}{4}\frac{(V_{CC} - V_{\min})}{V_{CC}} \times 100\% = \frac{\pi}{4}\left(1 - \frac{V_{\min}}{V_{CC}}\right) \times 100\% \tag{8.31}$$

Since $V_{CC} >> V_{\min}$ and $V_{\min} \to 0$, the maximum conversion efficiency of a Class B amplifier is $\eta_{\max} = 25\pi\% = 78.5\%$.

When there is no excitation, there is no current. In a Class A amplifier, when there is no excitation, an I_{CQ} current is drawn from the power supply. In case of a Class B amplifier, the power dissipation at the collector is zero in the quiescent state and it increases with excitation.

The collector power dissipation for both transistors T_1 and T_2 is the difference between power input to the circuit (P_i) and power delivered to load (P) and it can be expressed as

$$P_D = P_i - P = \frac{2V_{CC}V_m}{\pi R_L'} - \frac{V_m^2}{2R_L'} \quad \text{as } I_{C\max} = I_m = \frac{V_m}{R_L'} \tag{8.32}$$

The collector power dissipation is about zero when there is no excitation ($V_m = 0$) and it is maximum at $V_m = \frac{2V_{CC}}{\pi}$. Therefore, maximum power dissipation is $P_D = \frac{2V_{CC}^2}{\pi^2 R_L'}$ (8.33)

The maximum power can be delivered at $V_m = V_{CC}$ and $V_{\min} \to 0$ and its value is equal to

$$P_{\max} = \frac{I_m V_{CC}}{2} = \frac{V_m}{R_L'}\frac{V_{CC}}{2} = \frac{V_{CC}^2}{2R_L'} \tag{8.34}$$

Then maximum power dissipation is

$$P_D = \frac{2V_{CC}^2}{\pi^2 R_L'} = \frac{4P_{\max}}{\pi^2} \approx 0.4P_{\max} \quad \text{as } \frac{V_{CC}^2}{R_L'} = 2P_{\max} \tag{5.35}$$

8.8 CLASS A PUSH-PULL AMPLIFIER

The distortion introduced by the nonlinearity can be eliminated by push-pull circuit configuration. Figure 8.12 shows a push-pull amplifier which consists of two transistors T_1 and T_2. The load resistance is connected to the secondary of the transformer TRA_1 and the primary winding of TRA_1 is centre-tapped. The midpoint is connected to V_{CC} and two ends are connected to collectors of transistor T_1 and T_2 respectively. Hence, each half of the transformer primary winding acts as a transformer-coupled load.

The input signal is applied to transistors T_1 and T_2 through a centre-tapped transformer as depicted in Fig. 8.12. The biasing arrangement is provided by the resistances R_1 and R_2 which are connected across V_{CC}. The input signal v_i is applied to the primary winding of the input transformer. The secondary winding voltage of the input transformer is applied to the base terminals of transistor T_1 and T_2.

When an input signal $i_{b1} = I_{bm} \cos \omega t$ is applied to the transistor T_1, the output current from the transistor is

$$i_1 = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \cdots \tag{8.36}$$

where B_0, B_1, B_2, B_3, ... are constants and these parameters can be determined by the nonlinearity of the transistor.

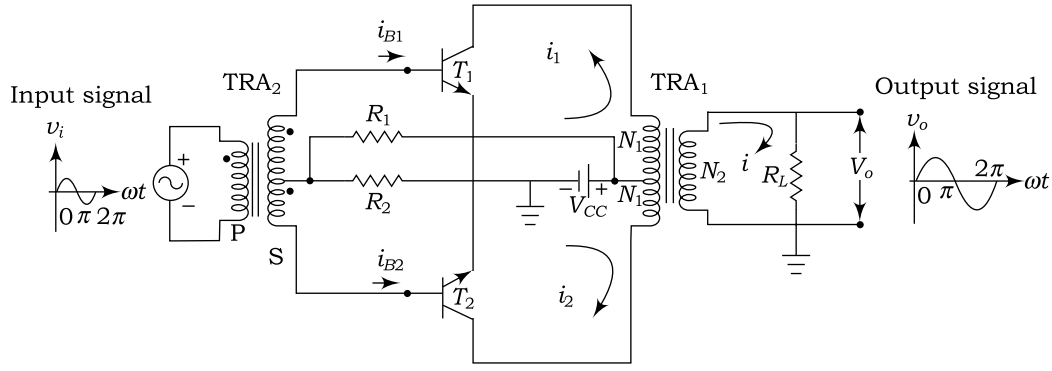


Fig. 8.12 Class A push-pull amplifier

It is clear from the above equation that in addition to fundamental frequency ω signal, higher order harmonics signals 2ω, 3ω, etc.., are present in the output. Therefore, the output waveform is distorted in nature with respect to the input waveform. This type of distortion is known as *harmonic distortion,* which must be minimised.

In the same way, the input signal $i_{b2} = -i_{b1} = I_{bm} \cos(\omega t + \pi)$ is applied to the transistor T_2 through the lower half of the input transformer. Since i_{b2} is equal and opposite to that to T_1, the output current from the transistor T_2 is

$$i_2 = I_{CQ} + B_0 + B_1 \cos(\omega t + \pi) + B_2 \cos 2(\omega t + \pi) + B_3 \cos 3(\omega t + \pi) + \cdots$$

or
$$i_2 = I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + \cdots \quad (8.37)$$

The currents i_1 and i_2 flow in opposite direction through the two halves of the primary winding of the output transformer. The total output current i in the secondary is directly proportional to the difference between the two collector currents and it can be expressed as

$$i = k(i_1 - i_2) = 2k(B_1 \cos \omega t + B_3 \cos 3\omega t + \cdots) \quad (8.38)$$

The above equation does not contain even harmonics. Therefore, push-pull circuit configuration conceals all even harmonics in the output. Since amplitude of third harmonics is greater than other odd harmonics, the third harmonics acts as a primary source of distortion.

8.8.1 Advantages of Class A Push-Pull Amplifier

1. The push-pull circuit arrangement provides less distortion for a given output power.
2. The dc component of the collector current of transistors T_1 and T_2 flow in the opposite direction. Therefore, there is no net dc magnetisation or core saturation. Hence, the core saturation tendency can be eliminated in the presence of nonlinear distortion.
3. Only odd harmonics are present in the output and all even harmonics are cancelled.
4. We obtain more output per transistor for a given amount of distortion.
5. The effect of ripple voltages that may be contained in the power supply due to inadequate filter will be balanced out.

8.9 CLASS B PUSH-PULL AMPLIFIER

Figure 8.13 shows a transformer-coupled Class B push-pull amplifier. This circuit consists of two centre-tapped transformers and two identical transistors T_1 and T_2. Transformer TRA_1 is an input transformer and it is called *phase splitter*. This transformer provides two signals, which are 180° out of phase with each other. These voltage signals have opposite polarity and are connected to the base of transistors T_1 and T_2. Transformer TRA_2 is an output transformer and this transformer is required to couple the ac output signal from the collector to the load.

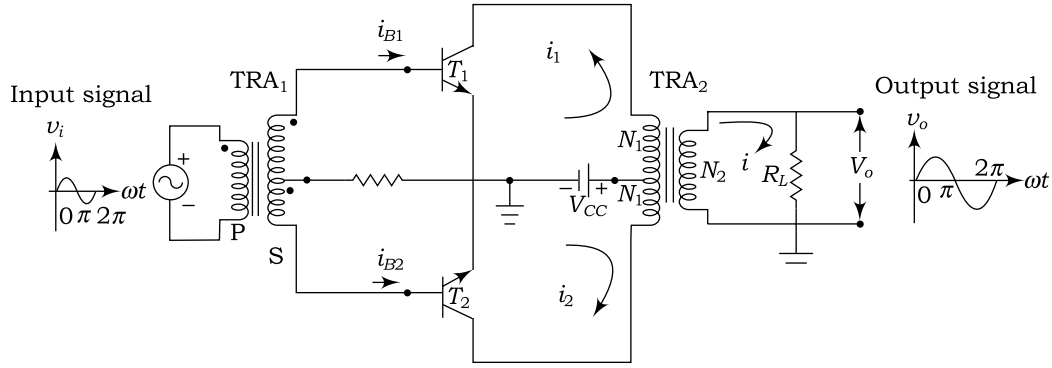


Fig. 8.13 Class B push-pull amplifier

Transistors T_1 and T_2 operate at cut-off providing zero bias on the base of each transistor. The zero bias can be achieved by connecting the emitter and base terminals of the transistor. To make a balance circuit, emitters of transistors are connected to the centre-tap of transformer secondary and the V_{CC}.

While there is no input signal, both transistors T_1 and T_2 are cut-off and no current is drawn from dc power supply. Therefore, there is no wastage of power. When both transistors T_1 and T_2 are biased, just above the cut-off points, transformers still operate at about zero flux. Since dc bias current flows in opposite directions through the secondary of the transformer T_2, magnetic flux is developed by these currents and opposite flux flows through the magnetic core. Then net flux is zero. Hence, it is not required to handle a large flux by the transformer. Consequently, transformer core size is small and biased to operate near zero flux.

During the positive half-cycle of the input voltage, the base of the transistor T_1 is positive and the base of the transistor T_2 is negative. Then T_1 conducts and T_2 is OFF. In the negative half-cycle of the input voltage, the base of the transistor T_2 is positive and the base of the transistor T_1 is negative. Then T_2 conducts and T_1 is OFF. Hence, each transistor conducts for one-half of input voltage. The output transformer incorporates positive as well as negative halves and generates a full sine wave across load resistance. Since the joining of outputs of two transistors T_1 and T_2 is not perfect, the output waveform will be distorted in nature.

A Class B push-pull amplifier is also known as double-ended Class-B amplifier. This amplifier is used in the final stages of amplifier circuits of Public Address Systems (PAS).

8.9.1 Advantages of Class B Push-Pull Amplifiers

1. The conversion efficiency of a Class B push-pull amplifier is 78.5% whereas the conversion efficiency of a Class A amplifier is 25%. This is possible as no power is drawn from dc power supply when there is no input signal.

2. All even harmonics are eliminated in the ac output signal of a Class B push-pull amplifier.
3. Due to absence of even harmonics, this amplifier circuit provides more output per transistor for a given amount of distortion.
4. Since dc components of currents i_1 and i_2 flow in opposite direction through the two halves of the primary of the transformer TRA_2, there is no dc current in the output signal. Therefore, there is no possibility of core saturation in the transformer T_2 and a small-size core transformer can be used in this amplifier circuit.

8.10 CROSSOVER DISTORTION

An ideal amplifier should generate an output signal waveform which will be a replica of input signal waveform in all respects except amplitude. Due to presence of nonlinear characteristics of active devices (transistors), an output signal waveform of amplifier differs from the input signal in respect of waveform or frequency content. The difference between the input signal waveform and output signal waveform in an amplifier is called *distortion*.

The crossover distortion will be present in the output signal as a result of nonlinearity of input characteristics of transistors. Transistors are not turned on at zero applied voltage across the base-emitter junction. When the base-emitter junction is forward biased and it value is greater than cut-in voltage $V_\gamma = 0.3$ V for germanium and $V_\gamma = 0.7$ V for silicon, transistors are turned on.

Figure 8.14 shows nonlinearity of input characteristics of transistors. When a sinusoidal base voltage is applied to transistors, the output current is nonsinusoidal as depicted in Fig. 8.14. If input voltage $v_B < V_\gamma$, the input current is negligible and output current is also neglected. This effect is known as *crossover distortion*.

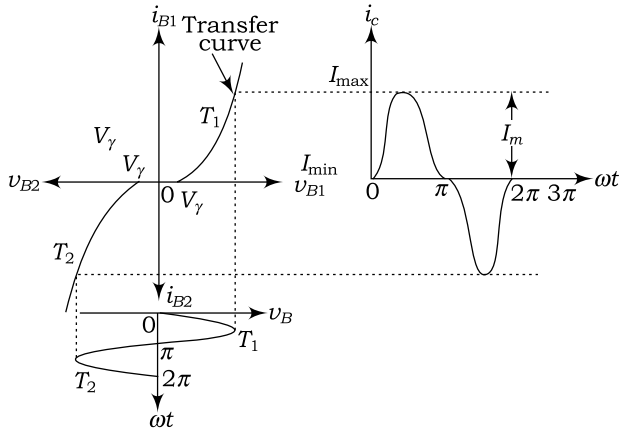


Fig. 8.14 Crossover distortion

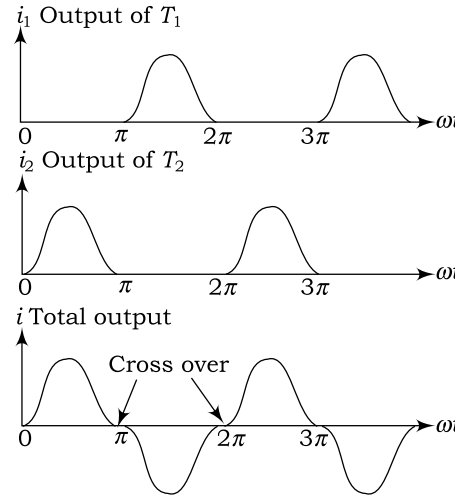


Fig. 8.15 Crossover distortion in Class B amplifier

In a Class B push-pull amplifier, one transistor is completely cut off before conduction of the other transistor. Figure 8.15 shows the crossover distortion in a Class B amplifier. Actually, distortion is introduced during the time when the operation crosses over from one transistor to the other transistor. To reduce the crossover distortion, the transistors should be operating in Class AB mode where a very small current flows under zero excitation or input signal. Subsequently, there is a waste of standby power and the conversion efficient will be reduced.

8.11 COMPLEMENTARY CLASS B PUSH-PULL AMPLIFIER

Figure 8.16 shows a complementary Class B push-pull amplifier which consists of a *PNP-NPN* transistor pair. When common emitter configuration is used in a push-pull amplifier, it is very difficult to match the output impedance for maximum power transfer without an output transformer. In a complementary Class B push-pull amplifier, transistors are connected in common-collector configuration. Since the common-collector configuration has low output impedance, impedance matching is possible.

In push-pull configuration, the input transformer generates two signals of 180° out of phase. For this, one transistor is ON and the other transistor is OFF. As the same input signal is applied to the base of transistors T_1 and T_2 and one transistor is *NPN*-type and the other is *PNP*-type, the operation of one transistor will be opposite of other transistor.

In the positive half-cycle of input voltage, the base-emitter junction of the *NPN* transistor would be forward biased and the base-emitter junction of the *PNP* transistor would be reverse biased. Similarly during negative half cycle of input voltage, the base-emitter junction of the *PNP* transistor would be forward biased and the base-emitter junction of the *NPN* transistor would be reverse biased. For proper operation of amplifier, transistors should be identical in all respects.

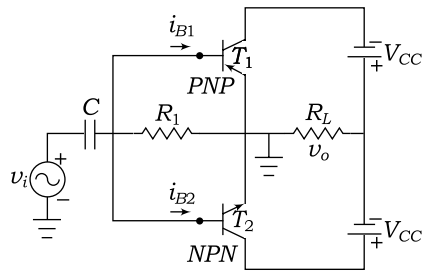


Fig. 8.16 Complementary Class B push-pull amplifier

The ac power output is $$P_{ac} = \frac{1}{2}\frac{V_{CC}^2}{R_L} \tag{8.39}$$

If $V_m = V_{CC}$, the output power is maximum.

The dc power is $$P_{dc} = \frac{2}{\pi}V_{CC}I_m = \frac{2}{\pi}\frac{V_{CC}^2}{R_L} \quad \text{as } I_m = \frac{V_m}{R_L} = \frac{V_{CC}}{R_L}. \tag{8.40}$$

Power dissipated at collector is $$P_D = P_{dc} - P_{ac}. \tag{8.41}$$

Efficiency is $$\eta = \frac{P_{ac}}{P_{dc}} \times 100\% = \frac{1}{2}\frac{V_{CC}^2}{R_L} \times \frac{\pi R_L}{2V_{CC}^2} \times 100\% = 25\pi\% = 78.5\% \tag{8.42}$$

8.11.1 Advantages of Complementary Class B Push-Pull Amplifier

1. As there is no transformer in a complementary Class B push-pull amplifier, the size and cost of the circuit is low compared to a Class B push-pull amplifier.
2. As common-collector configuration has low impedance, impedance matching is possible.
3. The frequency response is improved due to absence of transformers in complementary Class B push-pull amplifier.

8.11.2 Disadvantages of Complementary Class B Push-Pull Amplifier

1. This circuit requires two separate dc supplies.
2. The output signal waveform is distorted due to crossover distortion.

8.12 CLASS D AMPLIFIER

In a Class D amplifier, transistors act as a switch instead of current source. Since the power dissipation in an ideal switch is about zero, the efficiency of a Class D amplifier is about 100%. Due to very high efficiency, this type of amplifier is commonly used in a transmitter. Figure 8.17 shows a Class D amplifier where two push-pull transistor switches are used to generate a square wave. Then this square wave is filtered to produce the fundamental frequency output signal. A push-pull configuration consists of two complementary transistors and an RF transformer which couples the input signal to the base of transistors T_1 and T_2.

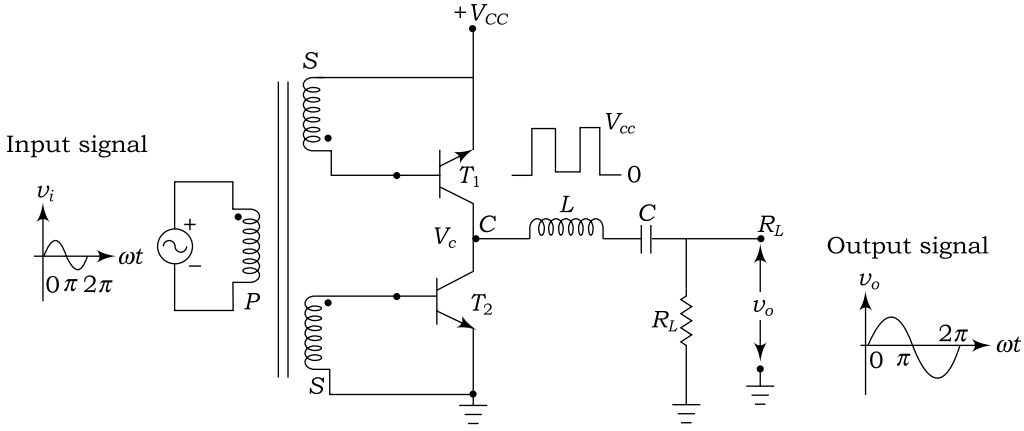


Fig. 8.17 Class D amplifier

In the positive half-cycle of input voltage, the upper transistor T_1 operates in cut-off and the lower transistor T_2 operates in saturation. Similarly, during negative half-cycle of input voltage, the upper transistor T_2 operates in saturation and the lower transistor T_2 operates in cut-off. Consequently, the output voltage at C is a square wave which alternates between 0 V and V_{BB}. After that, the square wave signal is fed to high Q series resonance circuits, which only passes the fundamental frequency and block the higher order harmonics.

The square wave can be expressed as

$$V = 0.636V_{CC}\left(\sin\theta + \frac{1}{3}\sin 3\theta + \frac{1}{5}\sin 5\theta + \cdots\right) \tag{8.43}$$

Then the output voltage of the circuit is

$$V = 0.636V_{CC}\sin\theta\,. \tag{8.44}$$

Example 8.1 A Class A power amplifier has zero signal collector current of 50 mA. If the collector supply voltage is 5 V, find (i) the maximum ac power output, (ii) power rating of the transistor, and (iii) maximum collector efficiency.

Sol. Given: $I_C = 50$ mA and $V_{CC} = 5$ mA

Maximum ac power output $P_{\text{ac(max)}} = \dfrac{V_{CC}I_C}{2} = \dfrac{5V \times 50\text{ mA}}{2} = 125\text{ mW}$

The dc input power is $P_{\text{dc}} = V_{\text{dc}}I_C = 5\text{ V} \times 50\text{ mA} = 250\text{ mW}$

Since the maximum power is dissipated in the zero signal conditions, power rating of the transistor is 250 mW.

As $P_{ac(max)} = \frac{P_{dissipation}}{2}$, the power rating of the transistor is twice than the maximum ac output power.

Maximum collector efficiency is $\eta = \frac{P_{ac(max)}}{P_{dc}} \times 100 = \frac{125\text{ mW}}{250\text{ mW}} \times 100 = 50\%$

Example 8.2 If the total harmonic distortion is 10% , prove that the power delivered to the load increases by 1%.

Sol. The power delivered to the load with 0% distortion is

$$P = (1 + D^2)P_1 = P_1 \text{ as } D = 0\%$$

When the harmonic distortion is 10%,

$$P' = (1 + D^2)P_1 = [1 + (0.1)^2]P_1 = 1.01P_1$$

Then increase in load power is

$$P' - P = 1.01P_1 - P_1 = 0.01P_1, \text{ i.e., 1\% increase.}$$

Example 8.3 Figure 8.18 shows a Class A power amplifier. Determine V_{CEQ}, I_{CQ}, P_{dc}, P_{ac} and efficiency if $\beta = 50$ and the rms base current due to ac input is 2.5 mA.

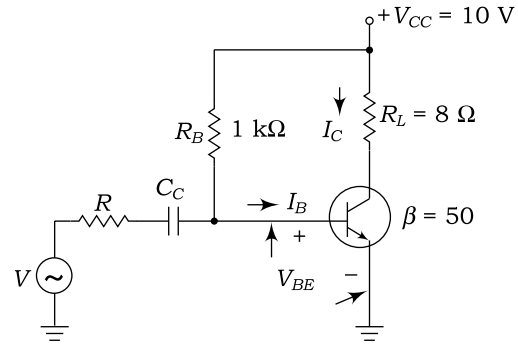


Fig. 8.18

Sol.
$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{1 \times 10^3} = 9.3\text{ mA}$$

$$I_{CQ} = \beta I_{BQ} = 50 \times 9.3 = 465\text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ}R_L = 10 - 0.465 \times 8 = 6.28\text{ V}$$

$$P_{dc} = V_{CC}I_{CQ} = 10 \times 465 \times 10^{-3} = 4.65\text{ W}$$

$$I_{B(rms)} = 2.5\text{ mA}, I_{C(rms)} = \beta I_{B(rms)} = 50 \times 2.5\text{ mA} = 125\text{ mA}$$

$$P_{ac} = I_{Crms}^2 R_L = (125 \times 10^{-3})^2 \times 8 = 0.125\text{ W}$$

$$\eta = \frac{P_{ac}}{P_{dc}} \times 100\% = \frac{0.125}{4.65} \times 100 = 2.688\%$$

Example 8.4 In a transformer-coupled Class A power amplifier, if the load resistance is 10 Ω and the turns ratio of the transformer N_1:N_2 = 100:1, determine the reflected load resistance to the primary side.

Sol. Given: $R_L = 10\ \Omega$, $N_1 : N_2 = 100:1$

Reflected resistance to the primary side is $R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = 100^2 \times 10\ \Omega = 100\text{ k}\Omega$

Example 8.5 A transformer is used for impedance matching of about 960 Ω resistance on the primary side to a 15 Ω resistance on the secondary side. Find the required turn's ratio of the transformer. What is the type of the transformer?

Sol. $R'_L = 960\ \Omega$, $R_L = 16\ \Omega$,

We know that $R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L$. Therefore, $\left(\frac{N_1}{N_2}\right)^2 = \frac{R'_L}{R_L} = \frac{960}{15} = 64$

Then $\frac{N_1}{N_2} = 8$

Example 8.6 A Class B push-pull amplifier has the supply voltage V_{CC} = +20 V and this amplifier drives a loudspeaker of 10 Ω resistance as load. When the turns ratio of the primary-to-secondary winding of the output transformer is 5:1, determine the dc input power, ac output power, efficiency and power dissipation per transistor.

Sol. $V_{CC} = 20$ V, $R_L = 10\ \Omega$, $N_1 : N_2 = 5 : 1$

$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = 5^2 \times 10 = 250\Omega$$

$$P_{ac} = \frac{V_m^2}{2R'_L} = \frac{V_{CC}^2}{2R'_L} = \frac{20^2}{2 \times 250} = 0.8 \text{ W}$$

As $$P_{ac} = \frac{1}{2} I_m^2 R'_L,\ I_m^2 = \frac{2P_{ac}}{R'_L} = \frac{2 \times 0.8}{250} = 0.0064 \quad \text{or } I_m = 0.08 \text{ A}$$

$$P_{dc} = \frac{2V_{CC} I_m}{\pi} = \frac{2 \times 20 \times 0.08}{\pi} = 1.019 \text{ W}$$

$$\% \ \eta = \frac{P_{ac}}{P_{dc}} \times 100\% = \frac{0.8}{1.019} \times 100 = 78.5\%$$

Power dissipation is $P_d = P_{dc} - P_{ac} = 1.019 - 0.8 = 0.219$ W

Power dissipation per transistor is $\frac{P_d}{2} = \frac{0.219}{2} = 0.1095$ W

8.13 TUNED AMPLIFIER

The tuned amplifier is used to amplify a specific frequency or a narrow band of frequencies, for which it is tuned. Tuned amplifiers are most commonly used for amplification of high frequency or radio frequency signals (30kHz to 300MHz), because radio frequencies are generally single and tuned circuits allow the desired radio frequency signal while rejecting all other frequency signals. There are two types tuned amplifiers such as

1. Single tuned voltage amplifier
2. Double tuned voltage amplifier

In this section, both single tuned and double tuned voltage amplifiers are explained in detail.

8.13.1 Single Tuned Voltage Amplifier

Figure 8.19 shows the single tuned voltage amplifier with capacitive coupled using bipolar junction transistor. This circuit is also called capacitive coupled tuned amplifier. This circuit consists of a transistor amplifier and the tuned circuit as a load. The values of capacitor (C) and inductance (L) of a tuned circuit can be selected in such a way that the resonant frequency of the tuned circuit is equal to the frequency to be selected and amplified. The resistance R_1, R_2 and R_E are called biasing resistors. The biasing resistors provide the dc operating currents and voltages for the transistor.

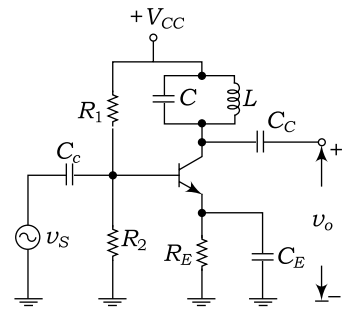


Fig. 8.19 Single tuned voltage amplifier with capacitive coupled

The operating principle of single tuned voltage amplifier can be understood by considering a radio frequency signal, to be amplified. The radio frequency signal is applied at the input of the amplifier. The resonant frequency of single tuned voltage amplifier circuit is equal to the frequency of the input signal by changing the value of capacitance (C) or inductance (L). At the instant the frequency of the tuned circuit is equal to that of the input signal; a large signal will be output at the output terminals. If the input signal is a complex wave i.e. contains many frequency signals, the signal frequency which is equal to the resonant frequency will be amplified and other frequency signals will be rejected by the tuned circuit.

The voltage gain of single tuned voltage amplifier depends upon the current gain β, input resistance R_i and ac load resistance.

The voltage of amplifier is

$$A_v = \beta \frac{r_L}{R_i}$$

The ac load resistance of a parallel resonant or tuned circuit is equal to

$$r_L = Z_p = \frac{L}{CR}$$

Where, L is the value of inductance

C is the value of capacitance

R is the value of effective resistance of inductor.

Usually, the value of impedance of tuned circuit $Z_p = \frac{L}{CR}$ is very high at resonant frequency and its value decreases when the frequency is above or below the resonant frequency. Consequently, the voltage gain of a tuned amplifier is very high at resonant frequency and decreases when frequency changes above or below the resonant frequency.

Figure 8.20 shows the frequency response of a tuned voltage amplifier. The bandwidth of a tuned voltage amplifier is expressed by

$$BW = \Delta f = f_2 - f_1 = \frac{f_0}{Q_0}$$

Where, f_0 is the resonance frequency and Q_0 is the quality factor of tuned circuit.

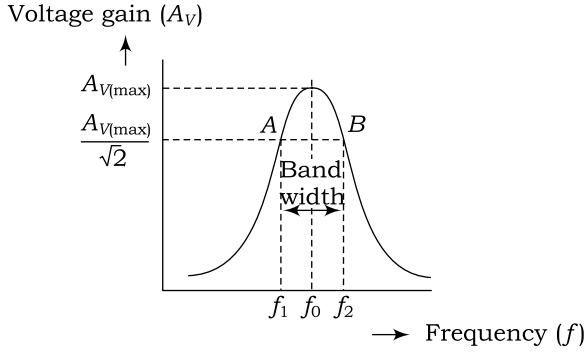


Fig. 8.20 Frequency response of a tuned voltage amplifier

Figure 8.21 shows the inductively coupled tuned amplifier as output is taken across inductance. Tuned voltage amplifiers are used in radio-frequency stage of wireless communication systems and used to select the desired carrier frequency and amplifying the complete band of frequencies around the selected carrier frequency. Hence, tuned voltage amplifiers are required to be highly selective. For high selectivity, a tuned circuit should have a high Q factor. The high Q factor provides a high voltage gain and it provides reduced bandwidth as the bandwidth is inversely proportional to the Q-factor. Therefore, a tuned amplifier with reduced bandwidth can not be able to amplify equally the complete band of signals. This is known as the potential *instability* in tuned amplifiers.

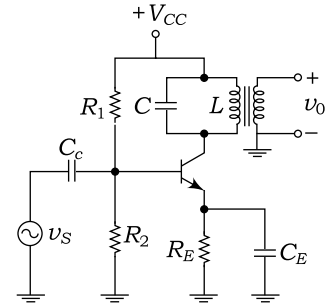


Fig. 8.21 Single tuned voltage amplifier with inductive coupled

8.13.2 Double Tuned Voltage Amplifier

Figure 8.22 shows the double tuned voltage amplifier. This circuit consists of a transistor amplifier and two tuned circuits. $L_1 - C_1$ is a tuned circuit which is used as the collector load and other tuned circuit $L_2 - C_2$ is used as output. The resistance R_1, R_2 and R_E are called biasing resistors. The biasing resistors provide the dc operating currents and voltages for the transistor.

The signal is applied to the input terminal through the coupling capacitor Cc. The resonant frequency of the tuned circuit $L_1 - C_1$ is equal to frequency of input signal. The tuned circuit offers very high impedance to the input signal. Therefore, a large output appears across the tuned circuit $L_1 - C_1$. The output of the tuned circuit $L_1 - C_1$ is inductively coupled to $L_2 - C_2$ tuned circuit.

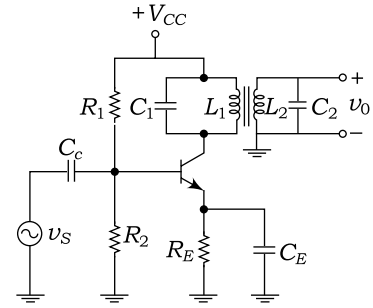


Fig. 8.22 The double tuned voltage amplifier

The frequency response of double tuned voltage amplifier depends on the coefficient of coupling between the two tuned circuits. The degree of coupling provides the information about the amount of energy transferred between two tuned circuits. Figure 8.23 shows the frequency response of double tuned voltage amplifier for tight coupling, critical coupling and loose coupling. Figure 8.23(a) shows the frequency response for tight coupling and the resonance occurs at two frequencies f_0' and f_0'' which are different from resonance frequency f_0. If the degree of coupling decreases, the frequencies f_0' and f_0'' will be come closer and try to merge into one frequency f_0 at critical coupling. The frequency response of critical coupling is depicted in Fig. 8.23(b). When the degree of coupling decreases below the critical coupling, a single peak of reduced amplitude is obtained as depicted in Fig. 8.23(c).

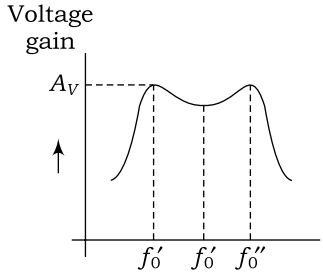


Fig. 8.23(a) Frequency response for tight coupling

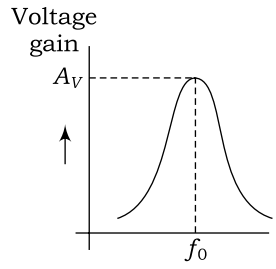


Fig. 8.23(b) Frequency response for critical coupling

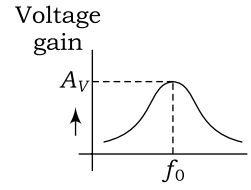


Fig. 8.23(c) Frequency response for loose coupling

The frequency response of a double tuned voltage amplifier is shown in Fig. 8.24. This type of frequency response of double tuned voltage amplifier has high selectivity, high gain and relatively large bandwidth. The bandwidth of double tuned voltage amplifier is $BW = f_2 - f_1$. The double voltage tuned voltage amplifier are used in IF amplifiers in radio and television receivers.

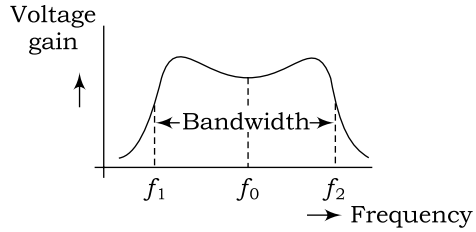


Fig. 8.24 Frequency response double tuned voltage amplifier

Review Exercises

Short-Answer Questions

1. What is the maximum efficiency of transformer-coupled Class A power amplifier?

Ans. The maximum efficiency of a transformer-coupled Class A power amplifier is 50%.

2. Comment the maximum efficiency of a Class B amplifier with respect to Class A amplifier.

Ans. With zero excitation, there is no current in Class B operation whereas power is drawn from supply source in a Class A amplifier. Therefore, efficiency of Class B amplifier is greater than the efficiency of a Class A amplifier. The maximum efficiency of Class B amplifier is 78.5%.

3. What is the application of a Class C amplifier?

Ans. The Class C amplifier is used for fixed frequency operation such as communication circuit.

4. Why is a Class D power amplifier most popular?

Ans. The Class D power amplifier is most popular due to high efficiency about 95%.

5. What is a Class A push-pull amplifier?

Ans. In push-pull amplifier, two transistors are used. This amplifier requires two input signals having 180° phase difference and usually output of a centre-tap transformer is used as input. In a Class A push-pull amplifier, current flows in the output of each transistor for the complete input cycle.

6. What is a complementary push-pull amplifier?

Ans. The complementary push-pull amplifier uses two transistors: one *NPN* transistor and another *PNP* transistor. The term c*omplementary* arises from the fact that one transistor is *NPN* and the other one is *PNP*.

7. What is the maximum efficiency of complementary push-pull amplifier?

Ans. The maximum efficiency of complementary push-pull amplifier is 78.5%.

8. What is crossover distortion? How it can be minimised?

Ans. The crossover distortion occurs in Class B push-pull amplifier's output signal as a result of nonlinearity of input characteristics of transistors. Transistors are not turned on at zero applied voltage across

the base-emitter junction. When the base-emitter junction is forward biased and it value is greater than cut-in voltage $V_\gamma = 0.3$ V for germanium and $V_\gamma = 0.7$ V for silicon, transistors turn on. When a sinusoidal base voltage is applied to transistors, the output current is nonsinusoidal. If input voltage $< V_\gamma$, the input current is negligible and output current is also neglected and this effect is known as *crossover distortion*.

To minimise the crossover distortion, it is necessary to add a small amount of forward bias to take transistors to the average conduction. Actually, the transistor operates in between Class A and Class B or Class AB.

Multiple-Choice Questions

1. In a Class A amplifier, the current flows through output circuit for
   (a) 90° (b) 180° (c) 360° (d) None of these
2. The maximum efficiency of a transformer-coupled Class A amplifier is
   (a) 25% (b) 50% (c) 78.5% (d) None of these
3. Crossover distortion occurs in _____ amplifier
   (a) Class A (b) Class B (c) Class AB (d) push-pull
4. The maximum efficiency of a Class B push-pull amplifier is
   (a) 25% (b) 50% (c) 78.5% (d) None of these
5. A Class AB amplifier is often used in large signal or power amplifiers to
   (a) get maximum efficiency (b) remove even harmonics
   (c) minimise crossover distortion (d) reduce collector dissipation
6. The type of power amplifier which exhibits crossover distortion in its output is
   (a) Class A (b) Class B (c) Class AB (d) Class C

Review Questions

1. Why is a large-signal amplifier called power amplifier? Write the difference between voltage amplifier and power amplifier.
2. What are the types of large-signal amplifier?
3. Draw the circuit diagram of a Class A amplifier and explain its operation briefly. Derive the equation for efficiency of a Class A amplifier.
4. Draw the circuit diagram of a Class A push pull-amplifier and explain its operation briefly.
5. Why is nonlinear distortion called harmonic distortion? How are five-point methods used to calculate harmonic distortion. What do you mean by $I_{\frac{1}{2}}$ and $I_{-\frac{1}{2}}$?
6. What is second harmonic distortion? What is total harmonic distortion?
7. Draw the circuit diagram of a Class A push-pull amplifier and explain its operation briefly. Derive the equation for efficiency of a Class B amplifier.
8. Prove that maximum collector efficiency of a Class B amplifier is 78.5%.
9. Write the advantages and disadvantages of a push-pull power amplifier.
10. Discuss crossover distortion in power amplifier. How can this distortion be minimised?
11. Draw the circuit diagram of a class B push-pull power amplifier and determine the maximum conversion efficiency of the circuit.

12. Write short notes on the following:
    (a) Cross over distortion
    (b) Push-pull amplifier
13. What is a power amplifier? Mention the advantages of push-pull power amplifier.
14. Compare between Class A, Class B and Class AB amplifier.

ANSWERS

Multiple-Choice Questions

1. (c) 2. (b) 3. (d) 4. (c) 5. (c) 6. (b)

CHAPTER

9

Multivibrators

9.1 INTRODUCTION

The output of sequential logic circuits depends on the present input states and previous history. The logic circuits operation can be controlled by a train of clock pulses. When the clock pulses are applied, the outputs of sequential logic circuit changes from one state to next state. These clock pulses are generated by clock generators or oscillators. The clock generators are frequently called as astable or free running multivibrator. In this chapter, clock oscillators using TTL and CMOS, astable, monostable, bistable multivibrators and their applications, operation of 555 timer and its applications have been explained.

9.2 CLASSIFICATION OF MULTIVIBRATORS

There are three types multivibrators, namely astable multivibrator, monostable multivibrator, and bistable multivibrator. These multivibrators are most commonly used in timing applications.

Astable Multivibrator

Astable multivibrator is known as free running multivibrator. It has two quasi-stable states and it continues to oscillate between two stable states. This multivibrator has no stable state and external trigger pulses are not required to change the states. This device can be used to generate square wave and the time duration depends upon circuit parameters. The continuously generated pulses are used as clock pulses in flip-flops, registers, counters and other digital circuits where the clock pulse is required for operation. Figure 9.1 shows the output voltage waveform of an astable multivibrator which oscillate between 0V and 5V without application of any trigger pulse.

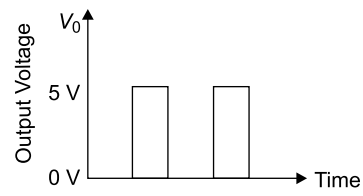


Fig. 9.1 Astable multivibrator

Monostable Multivibrator

Monostable multivibrator has a single stable state and a quasi-stable state. In this multivibrator, trigger signal is applied to switch from stable state to quasi-stable state. After a short time, the circuit reverts back to its stable

state. Hence, a single output pulsed is generated when a trigger pulse is applied to it. Therefore, it is known as one shot or single shot multivibrator circuit. The output pulse width can be controlled by internal circuit parameters and trigger pulse has no control over the pulse width of output waveform. As a result, a small pulse width or a sharp trigger pulse can be converted into an output of longer pulse width. So, this multivibrator is also called as pulse stretcher. Figure 9.2 shows the output voltage waveform and trigger signal of a monostable multivibrator. At time t_1, when the trigger pulse is applied, output of monostable multivibrator changes from 0 V to 5 V and its output stay at 5 V for certain time T_1 depending on circuit parameters. After T_1 time, output changes from 5 V to 0 V without application of any trigger pulse.

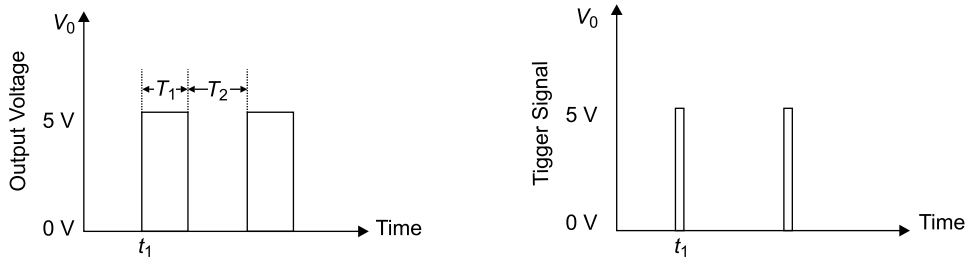


Fig. 9.2 Monostable multivibrator

Bistable Multivibrator

A bistable multivibrator has two stable states. When external trigger pulses are applied, the multivibrator changes one stable state to other stable state. Therefore, two external triggers are required for this multivibrator and bistable multivibrator is not an oscillator. The output voltage waveform and trigger signal of a bistable multivibrator are illustrated in Fig. 9.3. Assume the two stable states are 0 V and 5 V and initially multivibrator output is 0 V. At time $t_{1,}$ when the trigger pulse is applied, output of bistable multivibrator changes from 0 V to 5 V and its output continue at 5 V for T_1 time depending on the next trigger pulse. At time $t_{2,}$ if the next trigger pulse is applied, output changes from 5 V to 0 V.

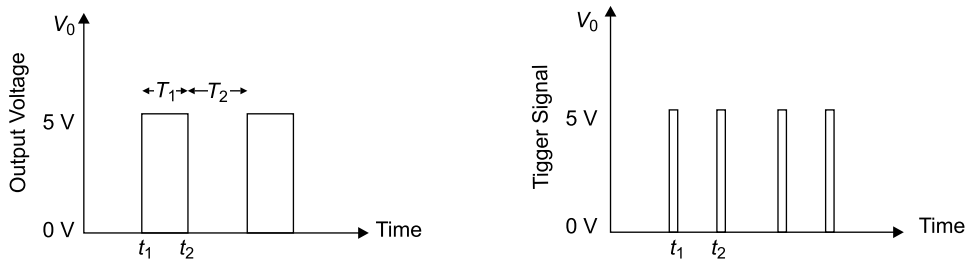


Fig. 9.3 Bistable multivibrator

Figure 9.4 shows the block diagram of a multivibrator, which consists of two inverting amplifiers A_1 and A_2 and two networks N_1 and N_2, which are used to develop a regenerative feedback loop. The type of multivibrator depends on the nature of coupling used in network. If the circuit behaves as bistable multivibrator, N_1 and N_2 will be resistance. In monostable multivibrator N_1 or N_2 will be capacitance. But in astable multivibrator N_1 and N_2 are capacitance. The operation of astable, monostable and bistable multivibrators are explained in this chapter.

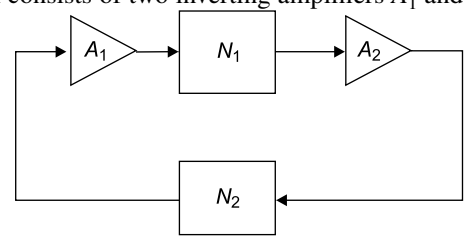


Fig. 9.4 Block diagram of multivibrator

9.3 CLOCK OSCILLATOR USING BJTs

Generally, clock oscillator is a two stage switching circuit in which the output of the first stage is fed to the input of the second stage and vice versa. The outputs of both the stages are complementary. Figure 9.5 shows the clock oscillator using NPN transistors. This free running oscillator generate square wave without any external triggering pulse. The circuit has two states and switches back and forth from one state to another. The switch should remain in each state for a time depending upon the discharging of capacitor through a resistance. Hence, clock oscillators are used to generate clock pulses.

The circuit as depicted in Fig. 9.5 also behaves as a simple astable circuit. The working principle as follows:

Consider that T_1 is turned on and T_2 is off. The collector voltage of T_1 will be approximately zero, and C_1 is charging through R_1 and collector-emitter of T_1. The charge on C_1 will be increased and the voltage at the base of T_2 will also be increased. As T_2 is not conducting, the capacitor C_2 will charge through R_4 and the base-emitter of T_1. The charging of C_2 will be very fast due to small R_4. Consequently, the collector voltage of T_2 will be +Vcc with respect to the base of T_1 at the end of charging C_2. While the base voltage of T_2 is more than 0.6 volts, the transistor T_2 switch becomes on. The voltage at the collector of T_2 will be approximately zero. Therefore, one end of C_2 is 0 volts and the other end is a voltage -Vcc due to capacitor charging. Then T_1 switches off.

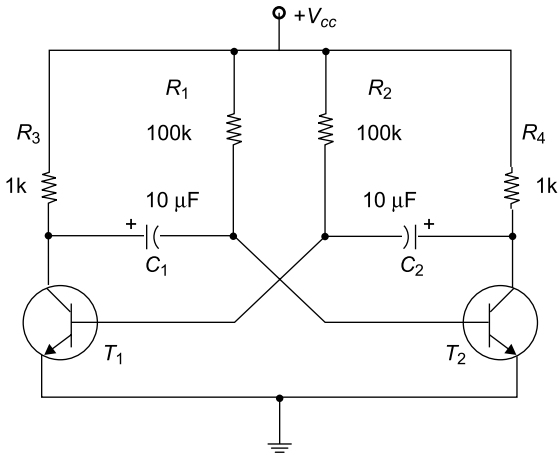


Fig. 9.5 Clock oscillator using NPN transistors

After that, capacitor C_2 starts charging through R_2 and the collector-emitter of T_2 and its voltage changes from negative to zero and then positive. When C_2 charges about 0.6V, T_1 will switch on and again the cycle continues. The charging and discharging of C_1 and C_2 are shown in Fig. 9.6 when T_1 is turned on and T_2 is off. Figure 9.7 shows charging and discharging of C_1 and C_2 when T_1 is off and T_2 is turned on.

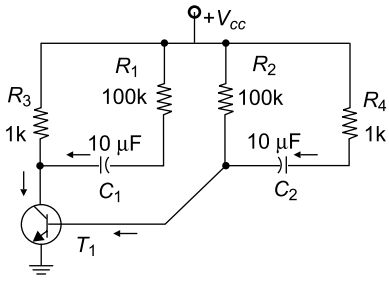


Fig. 9.6 Charging and discharging of C_1 and C_2 when T_1 is turned on and T_2 is off

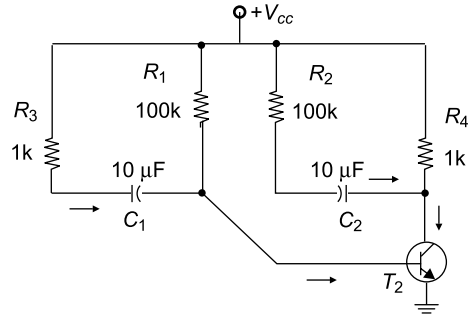


Fig. 9.7 Charging and discharging of C_1 and C_2 when T_1 is off and T_2 turned on

The voltage across capacitor, C and resistor, R must be equal to the applied voltage, Vcc. The mathematical relationship as given below:

$$V_{cc} = IR + \frac{Q}{C}$$

$$V_{cc} = R\frac{dQ}{dt} + \frac{Q}{C}, \text{ where, } Q \text{ is charge and } I = \frac{dQ}{dt}$$

After integrating the above expression, the voltage across the capacitor can be expressed as

$$V(t) = V_{CC} - (V_{CC} - V_0)\, e^{-t/RC}.$$

where, V_0 is the voltage across the capacitor at $t = 0$. In this case, the initial voltage $V_0 = -V_{cc}$. If $t = \log 2 \times RC = 0.693$RC, $V(t) = 0$ V . In this oscillator, when T_1 is ON, T_2 is OFF and when T_1 is OFF and T_2 is ON. The on time and off time are calculated by the following expressions as given below:

$$t_1 = 0.693\ R_1\ C_1 \text{ and } t_2 = 0.693\ R_2\ C_2.$$

The total time period, $T = t_1 + t_2 = 0.693(R_1\ C_1 + R_2\ C_2)$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$T = 1.386RC$ and the clock frequency, $f = 1/T = 0.721/RC$.

The cyclic switching of T_1 and T_2 produces a square wave at the collectors of transistors T_1 and T_2. The waveform of collector of T_1 and T_2 is shown in Fig. 9.8. The output of transistor T_1 is complement of T_2. Therefore this circuit is called as astable multivibrator. The astable multivibrator using PNP transistor is depicted in Fig. 9.9.

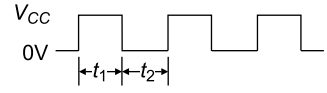


Fig. 9.8 Wave form of astable multivibrator

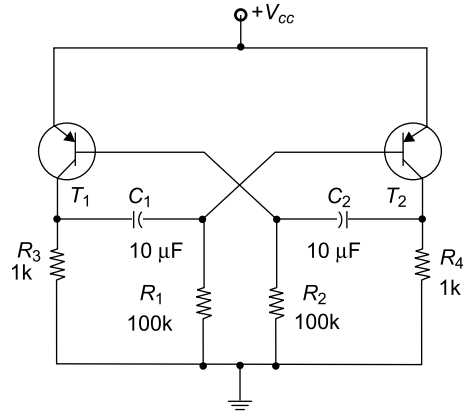


Fig. 9.9 Clock oscillator using PNP transistors

Example 9.1 In an astable multivibrator using NPN transistors as shown in Fig. 9.5, the resistance $R_1 = R_2 =$ 10 K and $C_1 = C_2 = 0.01$ µF and $R_3 = R_4 = 1$ Kohm, determine the clock frequency.

Sol. $t_1 = 0.693\ R_1\ C_1 = 69.3$ µs and $t_2 = 0.693\ R_2\ C_2 = 69.3$ µs.

Total time period, $T = t_1 + t_2 = 69.3$ µs + 69.3 µs = 138.6 µs

The clock frequency, $f = \dfrac{1}{t_1 + t_2}$ =1/138.6 µs =7. 215 KHz

9.4 MONOSTABLE MULTIVIBRATOR USING BJTs

Figure 9.10 shows the monostable multivibrator using BJTs. It has one stable state when T_1 is in cut-off and T_2 operates in saturation. If the trigger pulse is applied, T_2 cut-off and T_1 saturation and output will be quasi-stable. After some time, the circuit returns back to stable state. The detail circuit operation explained below:

Just after switch on the power supply, the circuit operates in stable state until a trigger pulse is applied as T_1 cut-off and T_2 saturation. To operate in saturation, R_1 value is selected in such a way that can supply required base current. The capacitor is charging through R_1 and base emitter junction of transistor T_2. When T_2 is in saturation, the collector output voltage of T_2 will be 0 V.

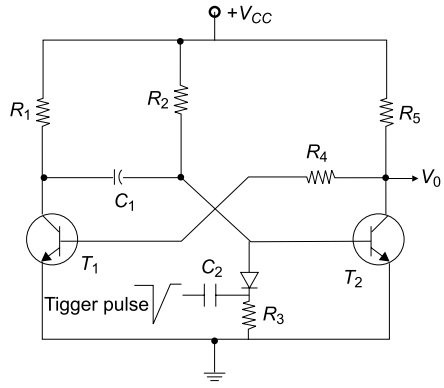


Fig. 9.10 Monostable multivibrator using BJTs

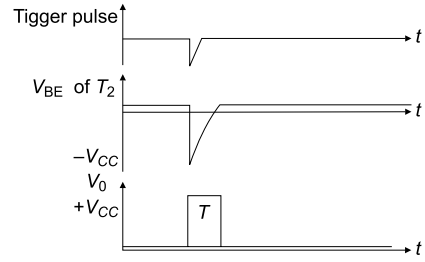


Fig. 9.11 Waveform of monostable multivibrator

When a negative trigger pulse is applied, C_2 act as short circuit, diode D is forward biased and conducting. Then the voltage at base of transistor T_2 will be reduced. Then transistor T_2 will operate in cut-off. The collector voltage of T_2 increases to $+V_{CC}$ and the base current of T_1 increases. The collector potential will be reduced and capacitor C_2 starts to discharge through T_1. Then T_1 is in saturation and T_2 is in cut-off. After completely discharged capacitor C_2, it starts to charge in the opposite direction through R_2. Therefore, potential at the base of T_2 starts to increase. When it is 0.7 V, T_2 starts conducting. So T_2 operates in saturation and T_1 is in cut-off. Then the circuit again operates in stable state. Figure 9.11 shows the waveform of monostable multivibrator. The duration of pulse width is equal to $T = 0.7\ RC$ approximately.

9.5 BISTABLE MULTIVIBRATOR USING BJTs

Figure 9.12 shows the Schmitt trigger circuit**.** Schmitt Trigger is also called an emitter coupled binary trigger circuit. It has two stable states that happened when transistor T_1 may be ON and T_2 OFF or vice versa. When input voltage does not applied to transistor T_1, the voltage divider network R_3 and R_4 along with R_2 maintains the base of T_2 at a slightly positive potential with respect to emitter. Therefore, T_2 operates in the saturation region. Due to the current flow in T_2, the voltage developed across the common emitter resistor, and T_1 is at cut-off. As the base of T_1 is at ground potential, it is negative with respect to the emitter. In this way, the circuit operates in a stable state when input signal is absent and T_2 ON and T_1 OFF. The output voltage is in the low state. Raising or lowering the bias on T_1, it may start the switching action.

When a time varying input voltage is applied, as soon as the input voltage reaches a value equal to the sum of the voltages across R_3 and R_6, T_1 will be turns ON as its base is more positive with respect to the emitter. T_1 is switched ON and operates in the saturation region. The collector voltage of T_1 decreases, which interns the base voltage of T_2 is also decreases. Hence, T_2 is driven to cut-off until the input voltage is greater than the sum of the voltages across R_3 and R_4. When T_2 is in cut-off, output voltage switches to the difference between V_{cc} and the voltage across R_5.

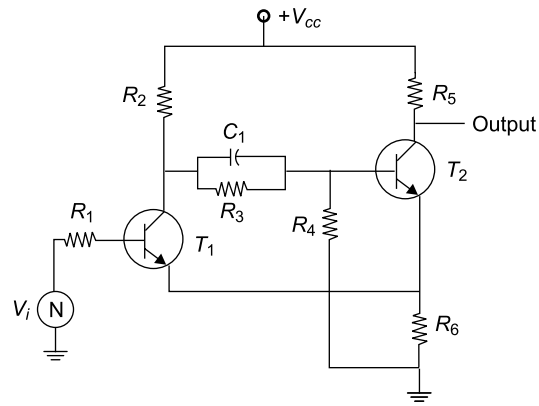


Fig. 9.12 Schmitt trigger (bistable multivibrator) using BJTs

If the input voltage drops below the sum of the voltages across R_1 and R_6, T_1 turns OFF and T_2 again turns ON due to regenerative action. Then output voltage returns to the sum of the voltages across R_6 and the saturation voltage of T_2. Thus, a square wave is produced. The turn ON voltage is usually called the upper trigger point or UTP. The turn OFF voltage is also called lower trigger point or LTP. UTP is always greater than LTP. The UTP = $I_{C(\text{sat})} R_6 + V_{BE(\text{ON})}$ and LTP=$V_{BE} + I_E R_6$. If Vcc=12 V, UTP=5 V, LTP=3 V and input voltage is varied in sinusoidal manner, the output waveform of bistable multivibrator is shown in Fig. 9.13.

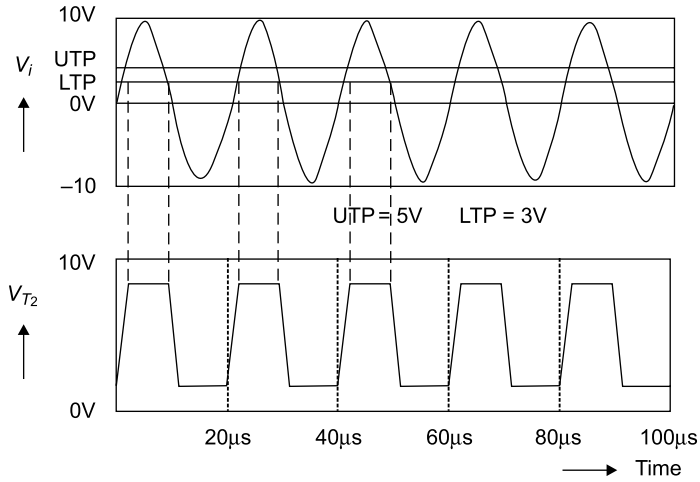


Fig. 9.13 Waveform of Schmitt trigger (bistable multivibrator): V_i = input signal and V_{T2} = output signal

9.6 ASTABLE MULTRIVIBRATOR USING NOT GATES

Figure 9.14 shows the astable multivibrator or clock oscillator using NOT gates. It consists of two inverters, which are connected, in cascade. Inverter provides a phase shift of 180° between input and output. When a square wave signal is used as input, an inverter output signal will be obtained with 180° phase shift after a very small propagation delay. The propagation delay varies in between 4 ns to 60 ns for different TTL ICs. If propagation delay of each TTL NOT gate is t_{pd} = 25 ns, then a total time delay = 2 t_{pd} = 2 × 25=50 ns will be achieved. When output is used as input V_1, then positive feedback is achieved and circuit behaves as feedback oscillators. Then time period will be 2 × 50=100 ns for 360° phase shift and frequency of oscillation =1/100 ns=10 MHz. Figure 9.15 shows the waveform of V_1, V_2 and V_0 for two cascade connected inverters.

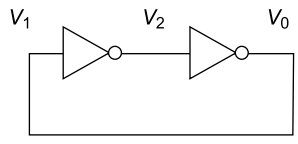


Fig. 9.14 Cascade connection of two inverters

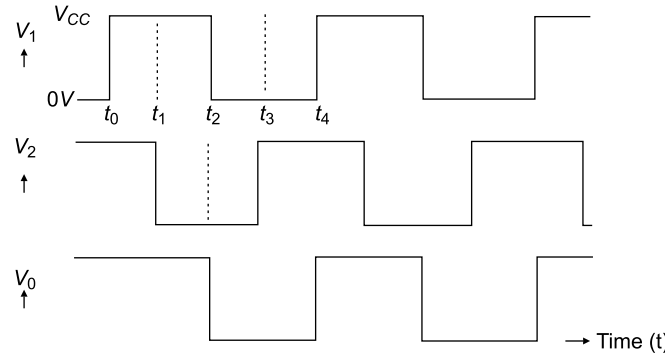


Fig. 9.15 Waveform of V_1, V_2 and V_0

Similarly, astable multivibrator using three and five NOT gates are shown in Figs 9.16 and 9.18 respectively and its waveforms are also depicted in Figs 9.17 and 9.19. In these circuits, NOT gates are connected in cascade and the output of third and fifth NOT gate are used as input of first NOT gate which forms a closed loop system. If propagation delay of each NOT gate is 25 ns, then a total 3×25=75 ns time delay can be achieved for Fig. 9.17 and 5×25=125 ns for Fig. 9.19. Then time period will be 150 ns and 250 ns and oscillation frequency =1/150ns=6.666 MHz for Fig. 9.17 and f=1/250ns= 4 MHz for Fig. 9.19.

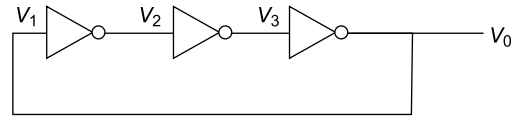


Fig. 9.16 Cascade connection three inverters (NOT gates)

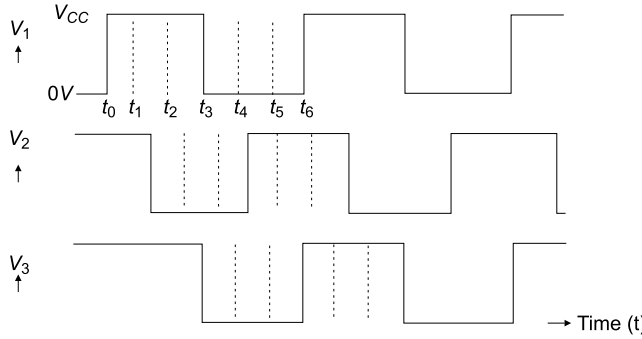


Fig. 9.17 Waveforms of three cascaded inverters (NOT gates): V_1, V_2 and V_3

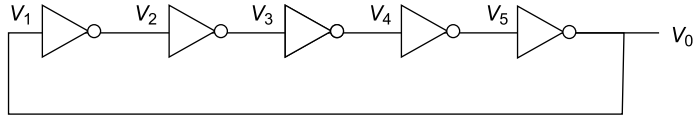


Fig. 9.18 Cascade connection of five inverters (NOT gates)

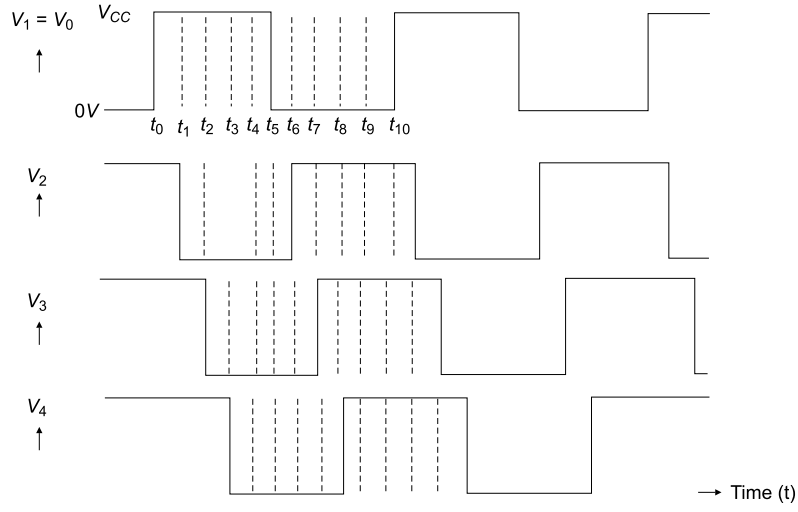


Fig. 9.19 Output waveform of multivibrator using cascade connection of five inverters, $V_1 = V_0$, V_2, V_3, V_4 and V_5

The disadvantage of these circuits is that the frequency of output waveform cannot be controlled externally. Actually, external circuits cannot control propagation delay and therefore frequency is uncontrolled.

Figure 9.20 shows the modification of astable multivibrator circuit using inverters, R and C elements. When the resistance and capacitance are incorporated in the circuit, there will be some control in frequency. When the power is switched on C_2 begins to charge through R_2, the input voltage of inverter-2 begins to rise, the output will stay high till the input voltage to the inverter INV_2 reaches a high logic level voltage. The duration of high output voltage depends upon the time constant C_2R_2. When input voltage of INV_2 arrives at the high logic level voltage, inverter output changes from high to low.

Then capacitor C_1 start to charge through R_1 and input voltage of INV_1 increases. The output of INV_1 will be high till the input voltage of INV_1 reaches a high logic level voltage. The inverter output voltage changes from high to low when input voltage of INV_1 arrive at high logic level voltage. The time period of output voltage depends upon the time constant R_1C_1.Therefore, alternately capacitors C_1 and C_2 will be charged. As a result, clock pulses will be produced. The frequency of clock pulse is

$$f = \frac{1}{t_1 + t_2} = \frac{1}{0.7R_1C_1 + 0.7R_2C_2} = \frac{1}{0.7(R_1C_1 + R_2C_2)}$$

where $t_1 = 0.7R_1C_1$ and $t_2 = 0.7R_2C_2$

if $R_1 = R_2 = R$ and $C_1 = C_2 = C$, frequency $f = \frac{1}{1.4RC}$

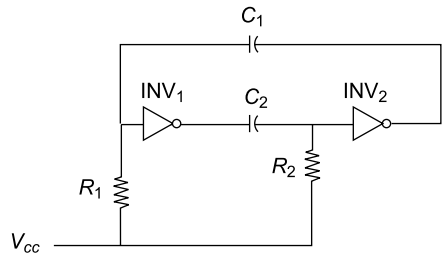


Fig. 9.20 Modified TTL clock oscillator

As frequency depends on the circuit parameters such as resistances and capacitances, the frequency stability is not good. To increase frequency stability, quartz crystal is used as shown in Fig. 9.21. The oscillator frequency is same as the quartz crystal. The oscillation frequency can be expressed as $f = 1/2RC$. When the frequency is known, the value of R and C can be determined from this expression.

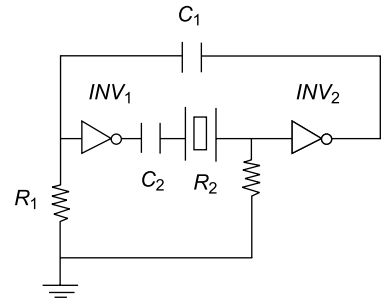


Fig. 9.21 TTL clock oscillator with crystal control

When CMOS inverters replace TTL inverters, the Fig. 9.20 and Fig. 9.21 also behave as oscillator or astable multivibrator. Due to different propagation delay of CMOS ICs, the frequency of this oscillator will be different. The output frequency depends on the supply voltage and temperature, but this variation is very narrow range. Therefore, this circuit has very little control over the output frequency. The frequency control range can be increased by using resistances and capacitance as shown in Fig. 9.22 and the oscillation frequency can be determined from the expression $f = 0.559/RC$.

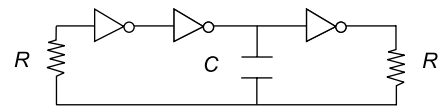


Fig. 9.22 CMOS oscillator

Figure 9.23 shows the astable multivibrator using AND and NOT gate. Initially, consider the capacitor is uncharged and $V_C = 0$V. After switch on the power supply, $V_C = 0$V. So the input voltage of inverter is low, inverter output voltage is high. This high voltage fed to AND gate as input. Then output of AND is

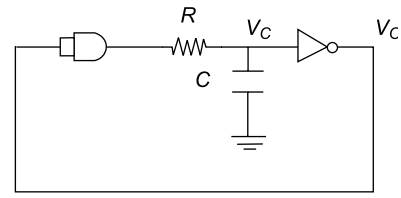


Fig. 9.23 Astable multivibrator using AND and NOT gates

high and this voltage applied across the *RC* circuit and capacitor voltage starts increasing due to charging. The output of inverter will be high till capacitor voltage reaches the high logic level voltage (V_H). When V_C cross the high logic level voltage V_H at time t_1, inverter output changes from high to low. Then AND gate output will be low and capacitor starts discharging. The inverter output voltage will be low till capacitor voltage reaches the low logic level voltage (V_L). When V_C arrives the low logic level voltage V_L at time t_2, inverter output changes from low to high and the next cycle of operation begins. The voltage across the capacitor V_C and output voltage V_O are shown in Fig. 9.24.

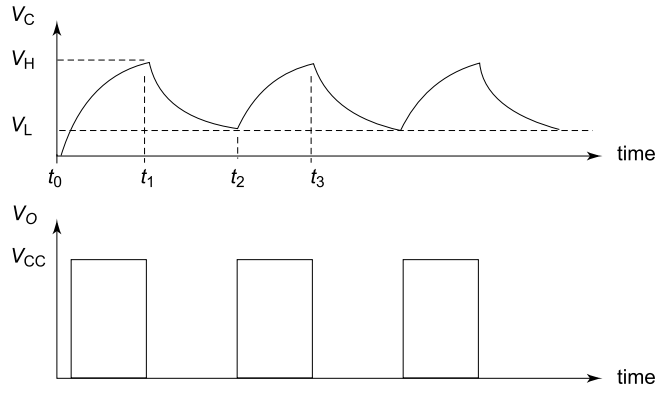


Fig. 9.24 Voltage across capacitor V_C and output voltage V_O

9.7 MONOSTABLE MULTRIVIBRATOR USING NAND GATES

Figure 9.25 shows the monostable multivibrator using two NAND gates. Trigger pulse is connected with one terminal of first NAND gate and other input terminal is used for feedback. Output of this NAND gate is applied to RC circuit. The second NAND is used as a NOT gate. Therefore, both input terminals are shorted and voltage across resistance is applied as input of the second NAND gate.

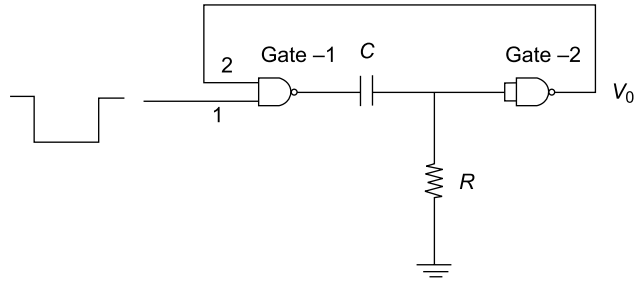


Fig. 9.25 Monostable multivibrator using NAND gates

The negative trigger pulse is applied at $t=t_0$, output of Gate-1 changes from low to high. Then high voltage applied across RC and capacitor starts to charge. The voltage across resistance and capacitance is shown in Fig. 9.26. At $t=t_1$, trigger pulse changes from low to high and then terminal 1 becomes high but terminal 2 is low. Then output voltage of Gate-1 is high. As output voltage is high, the capacitor is continuously charged through resistance *R*. At $t=t_2$, capacitor is fully charged and the voltage across resistance becomes zero. Consequently, the output of Gate-2 will be high. Therefore, during $t_2 - t_0$, the output of multivibrator is low.

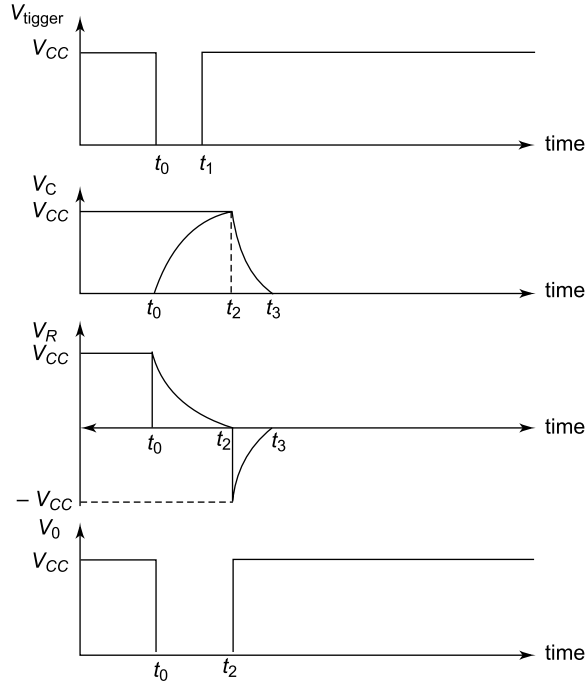


Fig. 9.26 Waveforms of monostable multivibrator

9.8 MULTIVIBRATOR USING OP AMPs

The operational amplifier is generally known as OP AMP which is most commonly used to perform mathematical operations such as addition, subtraction, integration and differentiation, etc. This is also used in analogue computers. The op-amp is a linear amplifier and its dc open-loop voltage gain is very high in the range of 10^3 to 10^6. The op-amp is constructed from several transistor stages namely differential-input stage, an intermediate-gain stage and a push-pull output stage. The differential amplifier consists of a pair of bipolar transistors or FETs. The push-pull amplifier transmits a large current to the load and hence has small output impedance. An ideal amplifier has following properties: large input impedance $Z_{in} \rightarrow \infty$, small output impedance $Z_{out} \rightarrow 0$, wide bandwidth, infinite gain $A \rightarrow \infty$, and infinite CMRR (common mode rejection ratio).

741 operational amplifier ICs are readily available in market and most commonly used in analog circuits. This device operates from DC to about 20 KHz, but the high-performance operational amplifiers operate up to 50 MHz.

Figure 9.27 shows the symbol of an operational amplifier. It has two inputs namely inverting (-) and non-inverting (+) and one output terminal V_0. Input voltages V_1 and V_2 are applied between inverting terminal and ground, and between non-inverting terminal and ground respectively. The output voltage V_O is measured in between output terminal and ground. The input terminals are known as differential inputs and the output is single ended. The output voltage V_O can be expressed as

$V_0 = A\ V_i$, where A = the voltage gain of the amplifier and $V_i = V_1 - V_2$.

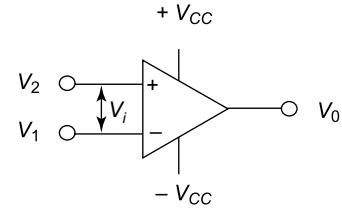


Fig. 9.27 Symbol of operational amplifier

As A is extremely high, about 200,000, the differential input voltage V_i is very small ($V_i \rightarrow 0$) and output voltage will be varied between positive and negative saturation voltages $+V_{CC}$ and $-V_{CC}$ respectively. In this diagram, $+V_{CC}$=+15 V (DC) and $-V_{CC}$=–15 V (DC). The positive and negative voltages are necessary to allow the amplification of both positive and negative signals without special biasing.

9.8.1 OP AMPs as Comparators

A comparator compares the value of input signal to a reference voltage. If the input signal voltage is larger than the reference voltage, comparator output will be HIGH. If the input signal voltage is smaller than the reference voltage, comparator output will be LOW.

Figure 9.28 shows the comparator circuit using an ideal operational amplifier. Since the open-loop gain of the ideal operational amplifier is infinite, the following equations can be expressed:

$$V_i > V_{ref}, \text{ then } V_d > 0 \text{ and } V_o = +V_{CC}$$
$$V_i < V_{ref}, \text{ then } V_d < 0 \text{ and } V_o = -V_{CC}$$

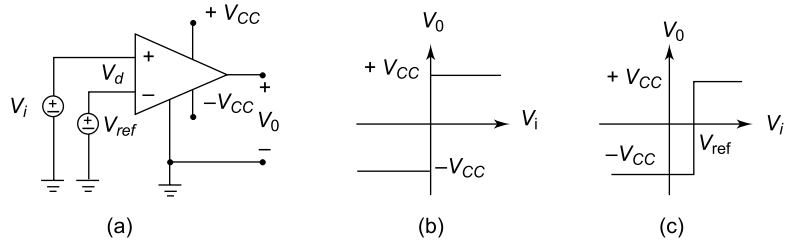


Fig. 9.28 (a) Comparator circuit (b) Characteristics of comparator when $V_{ref} = 0$ V (c) Characteristics of comparator when $V_{ref} = +ve$

The operational amplifier compares the input signal with the reference voltage. If $V_{ref} = 0$ and $V_i > 0$, the V_d is positive, the operational amplifier output will be high or $V_0 = +V_{CC}$. If $V_{ref} = 0$ and $V_i < 0$, the V_d is negative, the operational amplifier output will be low or $V_o = -V_{CC}$. When $+V_{CC}$ =15 V and $-V_{CC}$ = –15, the output voltage will be either +15V or –15V. Figure 9.28(b) shows the output characteristics when $V_{ref} = 0$V.

When $V_{ref} = +ve$, the output characteristics of comparator is depicted in Fig. 9.28(c). The output characteristics can be reversed when V_{ref} and V_i are interchanged as shown in Fig. 9.29(a) and its characteristics are shown in Fig. 9.29(b). When $V_{ref} = +ve$, the output characteristics can be expressed as

$$V_i > V_{ref}, \text{ then } V_d < 0 \text{ and } V_o = -V_{CC}$$
$$V_i < V_{ref}, \text{ then } V_d > 0 \text{ and } V_o = +V_{CC}$$

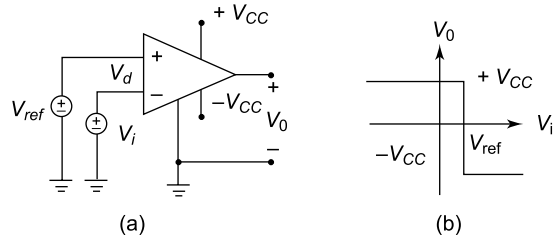


Fig. 9.29 (a) Comparator circuit (b) Characteristics of comparator when $V_{ref} = +ve$

Example 9.2 If V_{ref} = 2 V and V_i = 10 sin ωt in Figs 9.28 and 9.29, draw the output waveforms. Assume f = 50Hz.

Sol. Figure 9.30 shows the output voltage waveform, when V_{ref}=2 V and V_i=10 sin ωt in Fig. 9.28. When input voltage V_i is greater than V_{ref}=2 V, output voltage is 10 V. While input voltage V_i is less than V_{ref}=2 V, output voltage is –10 V. Figure 9.31 shows the output voltage waveform, when V_{ref} = 2 V and V_i=10 sin ωt in Fig. 9.29. If input voltage V_i is less than V_{ref} = 2 V, output voltage is 10 V. When input voltage V_i is greater than V_{ref} =2 V, output voltage is –10 V.

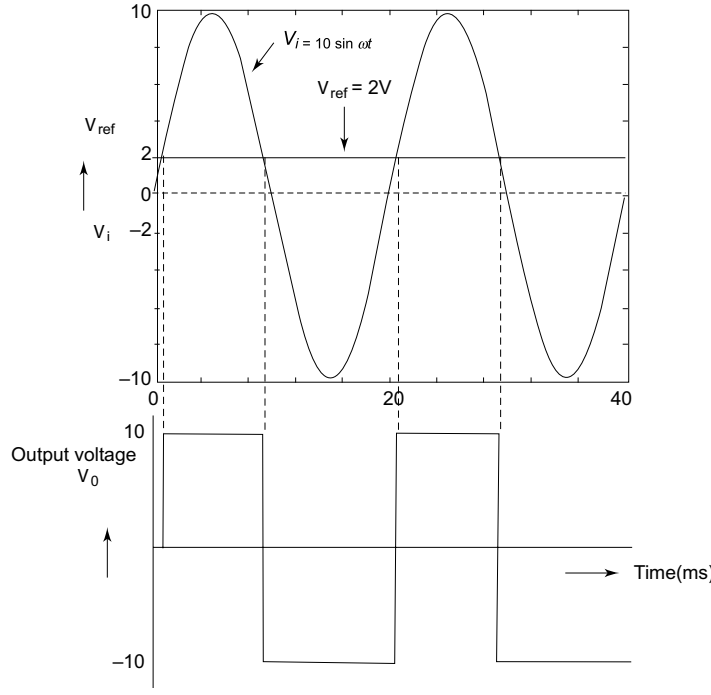


Fig. 9.30 Input and output voltage waveforms

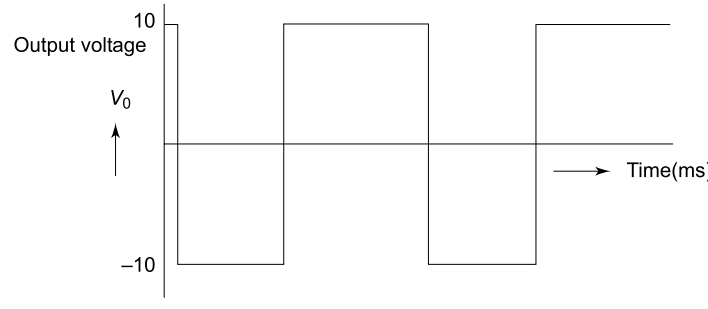


Fig. 9.31 Output voltage waveform

9.8.2 OP AMPs as BISTABLE

Figure 9.32 shows the bistable circuit using operational amplifier. This circuit has +ve feedback as the output of operational amplifier is connected to the non-inverting terminal. The virtual short principle between inverting and non-inverting terminals will not be applied due to absence of negative feedback and $V+ \neq V-$.

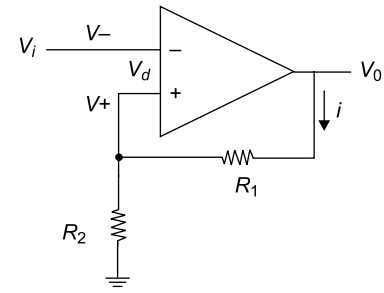


Fig. 9.32 Bistable circuit

In this operational amplifier circuit, R_1 and R_2 behave as voltage dividers. The voltage at non-inverting terminal will be

$$V_+ = \frac{R_2}{R_1 + R_2} V_0 = \beta V_0, \text{ where } \beta = \frac{R_2}{R_1 + R_2}$$

If the output of circuit is $+V_{CC}$ or $V_0 = V_{CC}$, then $V_+ = \beta V_0$. As long as $V_d = (V_+ - V_-) > 0$, circuit output will be $+V_{CC}$. If V_i is increasing, after some time $V_+ = V_- = \beta V_{CC}$. As V_i is continuously increasing, when V_i is greater than V_+, $V_d = (V_+ - V_-) < 0$ or becomes negative. Then output of operational amplifier will be changed from $+V_{CC}$ to $-V_{CC}$. Then $V_+ = -\beta V_0 = -\beta V_{CC}$. As V_+ becomes negative and force the output of operational amplifier to become negative. This is continuing until operational amplifier is saturated. Then output voltage is $V_0 = -V_{CC}$. Figure 9.33 shows the transfer characteristics of circuit.

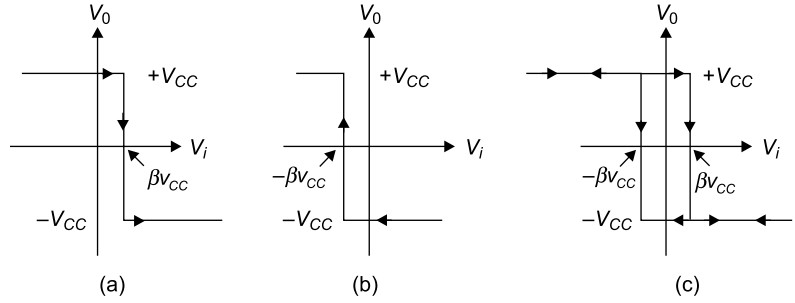


Fig. 9.33 Input-output characteristics (a) increasing V_i (b) decreasing V_i (c) complete characteristics

The transfer characteristics of the bistable circuit is hysteresis as the output changes state at different values of V_i depending on whether V_i is decreasing or increasing. The bistable circuit has two switching points: $+\beta V_{CC}$ and $-\beta V_{CC}$. The operation of the bistable circuit are shown in Fig. 9.33(a) and (b). The complete operation is also shown in Fig. 9.33(c). When V_i in between $+\beta V_0$ and $-\beta V_0$, the circuit will be in one of its two possible states. The output state of the circuit can be changed by applying an input signal $V_i > \beta V_{CC}$ to the circuit. This input pulse can be of a very short duration. This input signal is referred to as a trigger signal. On the other hand, the state of the circuit can also be changed by applying a negative pulse with $V_i < -\beta V_{CC}$.

The center of the hysteresis band can be shifted at different voltage by adding a reference voltage to the circuit as shown in Fig. 9.34. This circuit is also called a *Schmitt Trigger*. The operation of the circuit

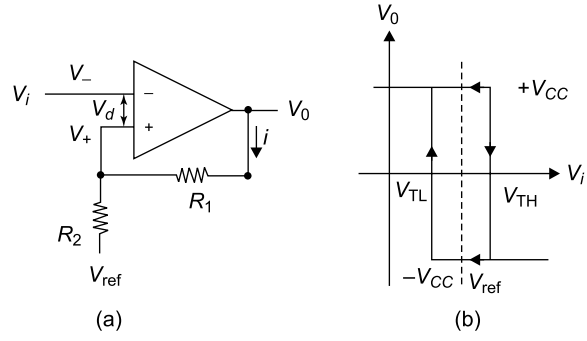


Fig. 9.34 (a) Bistable circuit with V_{ref} (b) Complete input-output transfer characteristics

is explained in this section. Consider the initial state output is V_0. Determine $V+$ and find the range of V_i for which V_d is positive. When V_i in this range, the comparator output state cannot be changed. When V_i is out of range, the sign of V_d changes from positive to negative. Then only the comparator output changes.

Here, $V_d = V_+ - V_- = V_+ - V_i$

The current through R_1 and R_2 is $i = \dfrac{V_0 - V_{ref}}{R_1 + R_2}$

Then $V_+ - V_{ref} = iR_2 = \dfrac{R_2}{R_1 + R_2}(V_0 - V_{ref})$ and we get $V_+ = \dfrac{R_2}{R_1 + R_2}V_0 + \dfrac{R_1}{R_1 + R_2}V_{ref}$

If $V_0 = V_{CC}$ and $V_d > 0$; $V_d = V_+ - V_- = V_+ - V_i > 0$, and the range of V_i for the Schmitt trigger will remain in this state, can be determined form $V_i < V_+$ where, $V_+ = \dfrac{R_2}{R_1 + R_2}V_{CC} + \dfrac{R_1}{R_1 + R_2}V_{ref}$

Therefore, the comparator output is in the high state and it stays in the high state until the condition of $V_i < V_{TH}$ is violated. The transfer characteristic is shown in Fig. 9.34(b).

Consider $V_0 = V_s^- = -V_{CC}$ and $V_d < 0$

Then $V_+ = \dfrac{R_2}{R_1 + R_2}V_s^- + \dfrac{R_1}{R_1 + R_2}V_{ref}$

As $V_d = V_+ - V_- = V_+ - V_i < 0$, the range of V_i for the Schmitt trigger will stay in the current state can be determined from $V_i > V_+$.

$$V_i > V_{TL} = V_+ = \frac{R_2}{R_1 + R_2}V_s^- + \frac{R_1}{R_1 + R_2}V_{\text{ref}}$$

As a result, the comparator is in the low state and stays in the same state until $V_i > V_{TL}$.

The range of V_i is $V_{TL} < V_i < V_{TH}$

or $\dfrac{R_2}{R_1 + R_2}V_s^- + \dfrac{R_1}{R_1 + R_2}V_{ref} < V_i < \dfrac{R_2}{R_1 + R_2}V_s^+ + \dfrac{R_1}{R_1 + R_2}V_{ref}$ Where $V_s^- = -V_{CC}$ and $V_s^+ = V_{CC}$

The range of V_i is called the dead band. The input signal should pass completely through this band before the output of trigger switches from one state to another. The value of V_s^- and V_s^+ are always chosen based on the desired value of the comparator output voltages.

Example 9.3 In Fig. 9.34, $V_{\text{ref}} = 4$V and a $V_i = 10 \sin \omega t$, determine V_{TL} and V_{TH}. Draw the output voltage waveform. Consider $R_1 = R_2 = 1$ KΩ.

Sol. The V_{TL} and V_{TH} voltages can be expressed as

$$V_{TL} = \frac{R_2}{R_1 + R_2}V_S^- + \frac{R_1}{R_1 + R_2}V_{ref}; \quad V_{TH} = \frac{R_2}{R_1 + R_2}V_S^+ + \frac{R_1}{R_1 + R_2}V_{ref}$$

As $R_1 = R_2 = 1$ KΩ, $V_S^- = -10$V, $V_S^+ = +10V$ and $V_{\text{ref}} = 4$ V

$$V_{TL} = -\frac{10}{2} + \frac{4}{2} = -3V: \quad V_{TH} = \frac{10}{2} + \frac{4}{2} = 7V.$$

Figure 9.35 shows the output waveform when $V_{\text{ref}} = 4$ V and a $V_i = 10 \sin \omega t$

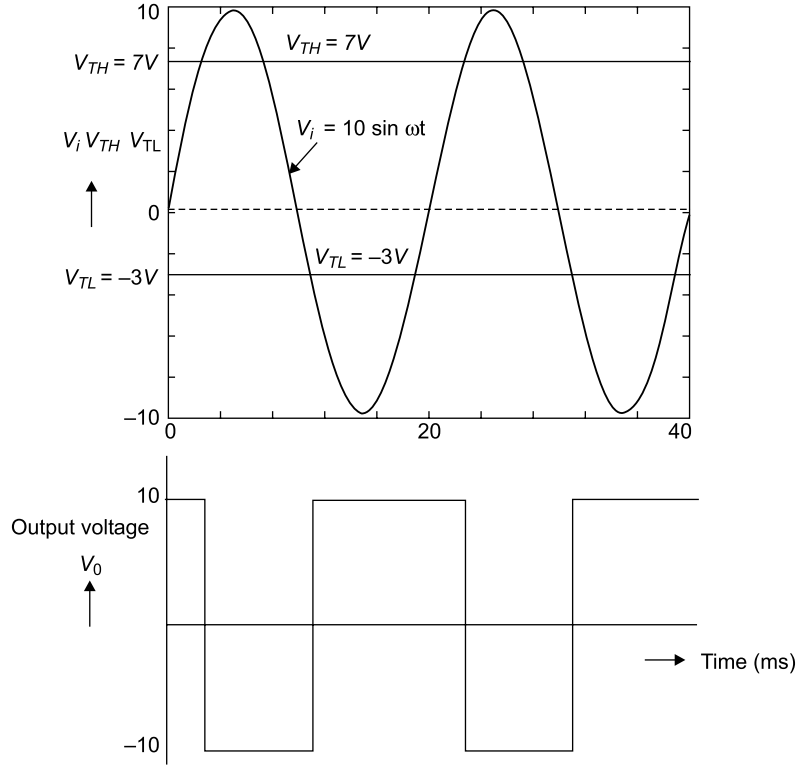


Fig. 9.35

9.8.3 OP AMPs as ASTABLE Multivibrator

Figure 9.36 shows astable multivibrator which consists of bistable circuit and a *RC* feedback loop. This circuit can be used to generate square waveform. The operation of the circuit is explained below:

The bistable circuit has two states $+V_{CC}$ and $-V_{CC}$. Initially, consider that the output of bistable circuit is $+V_{CC}$. Then the capacitor is charged through resistance and the voltage across the capacitor increases with a time constant RC. The voltage of capacitor moves toward $+V_{CC}$. The capacitor voltage is used as input of bistable circuit. When the capacitor voltage is more than the threshold voltage, V_{TH}, the bistable circuit is triggered and its output voltage changes from $+V_{CC}$ to $-V_{CC}$. As $-V_{CC}$ is applied to the capacitor, the capacitor discharges with the constant RC. Then the voltage of capacitor moves toward $-V_{CC}$. As soon as the voltage across the capacitor is V_{TL}, the bistable is triggered again and output changes from $-V_{CC}$ to $+V_{CC}$. In this way, the switching takes place and a square wave will be generated at the output of the bistable circuit. As this circuit has no stable state, it is called astable multivibrator. Therefore, an astable multivibrator is a combination of a Schmidt trigger and an RC circuit. Figure 9.37 shows the astable circuit. This circuit has both negative and positive feedback.

In Fig. 9.37, resistance R_2 and R_3 act as a voltage divider. Therefore, the voltage at non-inverting terminal is $V_+ = \dfrac{R_2}{R_2 + R_3} V_0$

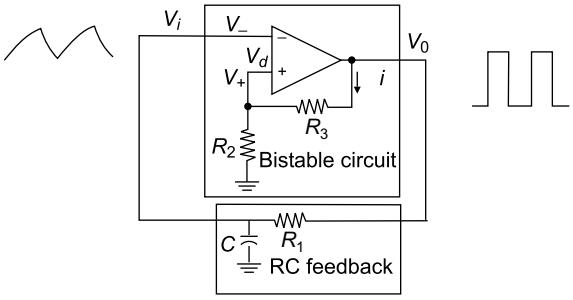


Fig. 9.36 Bistable circuit with RC feedback

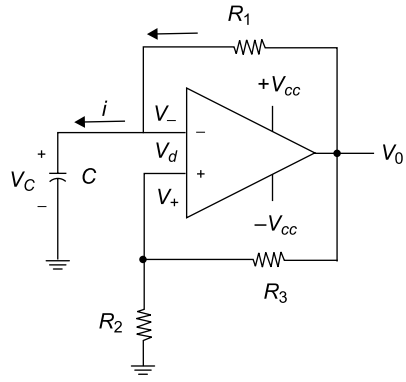


Fig. 9.37 Astable multivibrator

The current input to inverting and non-inverting terminals is zero (i_+=i_-=0). So, RC part of the circuit acts independently. Initial voltage across the capacitor is $V_c(t_0)$ at $t=t_0$. When voltage V_o is applied to this circuit, the voltage across the capacitor at time t will be

$$V_c(t) = V_0 + [V_c(t_0) - V_0]e^{-\frac{t-t_0}{\tau}} \quad \text{as capacitor is charging.}$$

where $\tau = R_1C$ the time constant of the RC circuit.

If V_d>0, $V_0 = V_s^+$. The RC circuit and voltage divider R_2 and R_3 operate differently. So, sudden change in output voltage can effect on sudden change in V_+ . But V_- cannot changes suddenly as the voltage across the capacitor has to be continuously charged or discharged. There is some delay in the response of RC circuit. Actually this delay is used to generate the square wave output. The voltage across capacitor V_C and output voltage V_O are depicted in Fig. 9.38.

At t_0=0, $V_c(t_0)$=0 and $V_0 = V_s^+ = V_{CC}$, the voltage across capacitor can be expressed as

$$V_- = V_c(t) = V_s - V_s e^{-\frac{t}{\tau}}$$

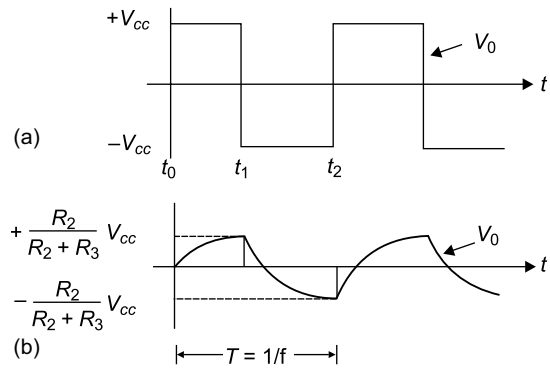


Fig. 9.38 (a) Output voltage (b) Capacitor voltage

At time t = 0, V_- = 0. When time increases, V_- increases. At time t_1, capacitor voltage will exceed $V_+ = \frac{R_2}{R_2 + R_3}V_s^+$. Then V_d is negative and it forces the comparator output to become $V_s^-(-V_{CC})$.

The time period of square wave is T=2(t_2-t_1) and its expression can be derived as follows:

$$V_-(t_2) = V_C(t_2) = -V_{CC} + (V_{CC}\frac{R_2}{R_2 + R_3} + V_{CC})e^{-\frac{t_2-t_1}{\tau}}$$

$$V_+(t_2^-) = -V_{CC}\frac{R_2}{R_2 + R_3}$$

Where t_2^- is the time very close to t_2 but smaller than t_2. The comparator switches to other state if $V_-(t_2) = V_+(t_2^-)$. After equating the above equations for $V_-(t_2)$ and $V_+(t_2^-)$, we get

$$-V_{CC} + (V_{CC}\frac{R_2}{R_2+R_3} + V_{CC})e^{-\frac{t_2-t_1}{\tau}} = -V_{CC}\frac{R_2}{R_2+R_3}$$

$$\text{Or} \quad (\frac{R_2}{R_2+R_3}+1)e^{-\frac{t_2-t_1}{\tau}} = 1 - \frac{R_2}{R_2+R_3} = \frac{R_3}{R_2+R_3}$$

$$\text{Or} \quad e^{-\frac{t_2-t_1}{\tau}} = \frac{R_3}{2R_2+R_3} \quad \text{Or} \quad \frac{t_2-t_1}{\tau} = \ln\frac{2R_2+R_3}{R_3}$$

Therefore, $T = 2(t_2 - t_1) = 2\tau \ln\left(\frac{2R_2}{R_3}+1\right)$ where $\tau = R_1C$

In this way, a square-wave is generated by the circuit. The amplitude of the square wave is set by the saturation voltage of the Op Amp (V_s^+ and V_s^-) and a period T can be determined by the above formula. The period of this oscillator is controlled by R_2 and R_3. Generally, R_2 and R_3 are chosen in the range of tens of K ohm.

When two zener diodes (V_{Z1} and V_{Z2}) are connected back to back across the output, the output voltage will be depend on forward biased and reverse biased voltage of zener diodes as shown in Fig. 9.39. When *V*+ is greater than *V*-, the output voltage is positive and can be expressed as $V_0 = V_D + V_Z$. When V_+ is less than *V*-, the output voltage will be negative and can be expressed as $V_0 = -(V_D + V_Z)$ where V_D is the voltage across forward bias zener diode and V_Z is the Zener voltage.

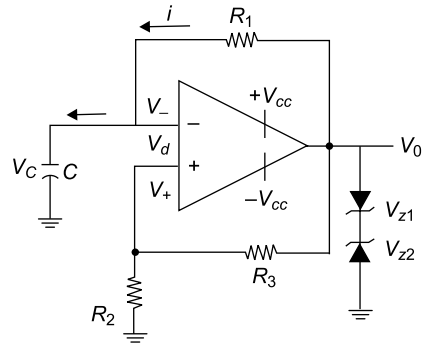


Fig. 9.39 Astable multivibrator using operational amplifier with output voltage limiter, Zener diode

9.8.4 OP AMPs as MONOSTABLE Multivibrator

Figure 9.40 shows the monostable multi-vibrator using operational amplifier. This circuit has one stable state (HIGH) and one quasi stable state (LOW). When external trigger pulse is applied, the output changes states from stable state to quasi-stable state or HIGH to LOW and after certain time depending upon the circuit parameters, output return back to stable state.

When no trigger pulse is applied, the input voltage V_+ is greater than V_- and output is V_0, i.e., positive and the circuit is under steady state condition. In this case, the capacitor C charges through R_1, but the capacitor voltage can not able to increase than the forward voltage drop across D_1 (V_D). The resistance values are selected in such a way that V_+ is greater than V_D.

As soon as a negative trigger pulse is applied, the non-inverting input voltage, V_+ becomes less

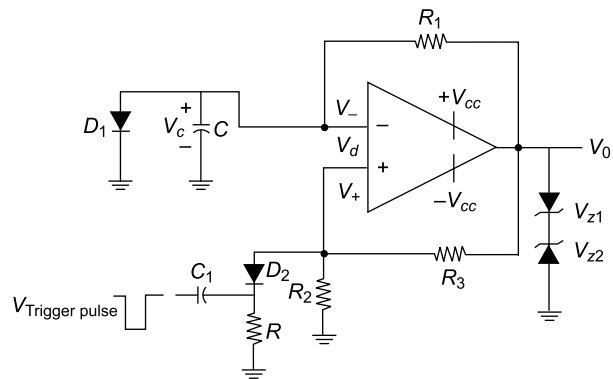


Fig. 9.40 Monostable multivibrator using operational amplifier

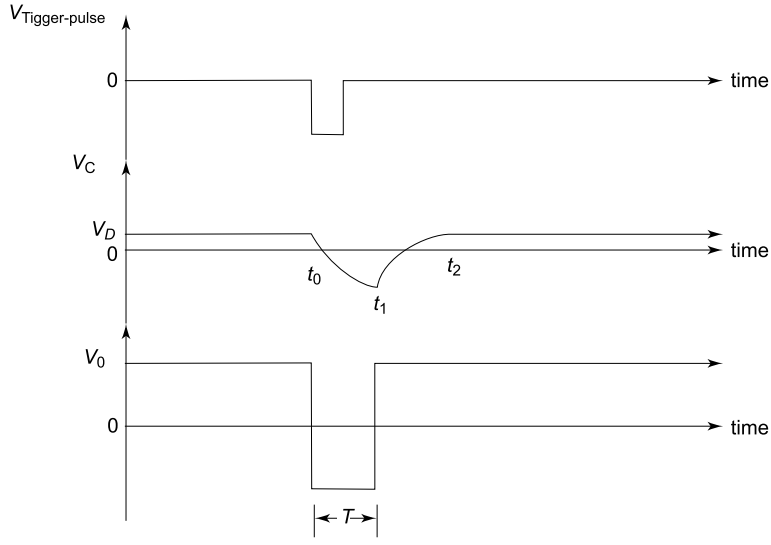


Fig. 9.41 Waveforms of monostable multivibrator

than inverting voltage, *V*- and output voltage changes from $+V_0$ to $-V_0$. The capacitor *C* stars to charge through R_1 and moves towards $-V_0$. In this condition, diode D_1 is reverse biased and acts as open circuit. After some time, the voltage across capacitor *C*, (V_C) or *V*- becomes more negative than V_+, then the output again changes from low quasi-stable state to high stable state. Figure 9.41 shows the waveform of the monostable multivibator.

The voltage across the capacitor can be expressed as

$$V_C = -V_0 + (V_0 + V_D)e^{-\frac{t}{\tau}}$$

where, $\tau = R_1C$

At time $t = t_1$, $V_C = -\beta V_0$

The pulse width duration is *T* and can be expressed as

$$T = \tau \ln\left(\frac{1 + V_D / V_0}{1 - \beta}\right)$$

where, V_D is the forward bias voltage drop across diode D_1 and V_0 is the output voltage

and $\beta = \dfrac{R_2}{R_3 + R_2}$

As $V_0 >> V_D$, and if $R_3 = R_2$, the time period can be expressed as

$$T = \tau \ln\left(\frac{1}{1 - \frac{1}{2}}\right), \text{as } V_D / V_0 = 0 \text{ and } \beta = \frac{1}{2}$$

$$T = 0.69R_1C$$

Example 9.4 Figure 9.40 shows monostable multivibrator. Determine the circuit elements for T = 10μs and draw the voltage across capacitor and output voltage waveform. Assume V_D = 0.6 V and V_Z = 9 V.

Sol. We know that $T = \tau \ln\left(\frac{1 + V_D / V_0}{1 - \beta}\right)$

and $\beta = \frac{R_2}{R_3 + R_2} = \frac{1}{2}$ as R_2=R_3=10 K ohms

After substituting V_D= 0.6V and V_Z=9V=V_O , we get

$$T = \tau \ln\left(\frac{1 + 0.6/9}{1 - \frac{1}{2}}\right) = \tau \ln\left(\frac{1.0667}{0.5}\right) = 0.7576\tau = 0.7576 R_1 C$$

As T=10μs , 10μs = $0.7576 R_1 C$

If C=10pF, R_1=1.32K ohm.

Figure 9.42 shows the voltage across the capacitor and output voltage.

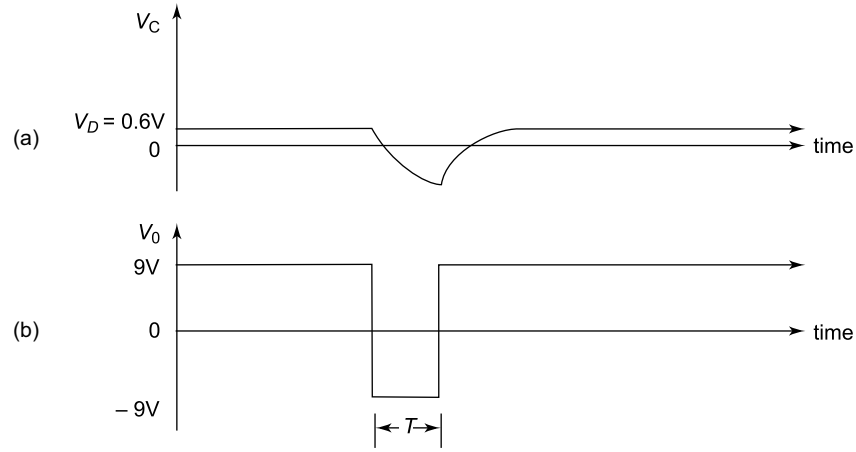


Fig. 9.42 (a) Voltage across capacitor (b) Output voltage

9.9 555 TIMER

The pin diagram of IC 555 is shown in Fig. 9.43. Figure 9.44 shows the block diagram of 555 timers. The 555 timers consist of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network. The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator (COMP-1) is referenced internally at 2/3 of supply voltage level (2/3 V_{CC}) and the trigger comparator (COMP-2) is referenced at 1/3 of supply voltage (1/3 V_{CC}). The outputs of the comparators are tied to the bistable flip-flop. When the trigger voltage is moved below 1/3 of the supply, the comparator - 2 changes state and sets the flip-flop driving the output to a high state. The threshold pin normally monitors the capacitor

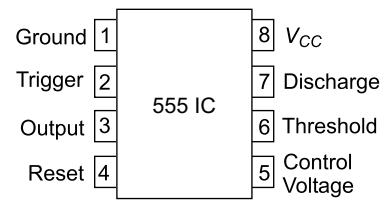


Fig. 9.43 Pin diagram of 555 IC

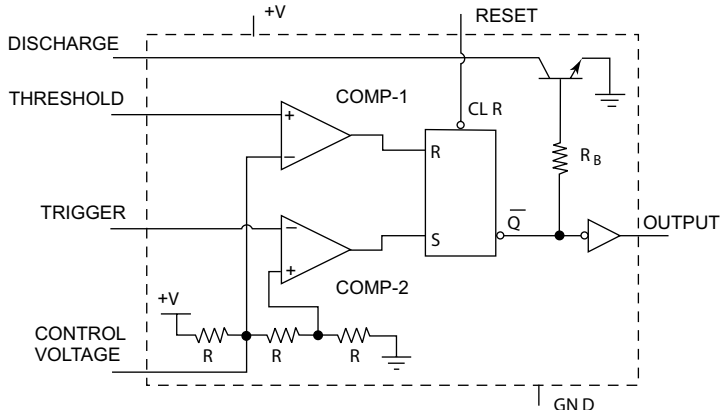


Fig. 9.44 Block diagram of 555 timer IC

voltage of the RC timing network. When the capacitor voltage exceeds 2/3 of the supply voltage, the threshold comparator (COMP-1) resets the flip-flop, which in turn drives the output to a low state. When the output is in a low state, the discharge transistor is "on", in that way discharging the external timing capacitor. Once the capacitor is discharged to 1/3 of supply voltage, the timer will again triggered and the next timing cycle will be started.

9.9.1 Astable Operation Of 555 Timer

Figure 9.45 shows the 555 timers IC that is operate in astable mode. Here, pin 5 is not used. The three internal resistances (R's) divide the voltage into three parts. Therefore, $V_7=2V_{CC}/3$ and $V_2=V_{CC}/3$. While the capacitor is charging and the capacitor voltage is in between $2V_{CC}/3$ and $V_{CC}/3$, the output of neither of the comparator undergoes a change in the sign of their output, which is negative and therefore logic 0. If the capacitor is charging and its voltage tends to rise above $2V_{CC}/3$, the comparator-1 (COMP-1) output jumps to positive saturation value, i.e., it is logic 1 at R input of flip-flop. Similarly, when the capacitor is discharging and its voltage tends to fall below $V_{CC}/3$ and the comparator-2 (COMP-2) output jumps to positive saturation value or logic 1 at S input of flip-flop.

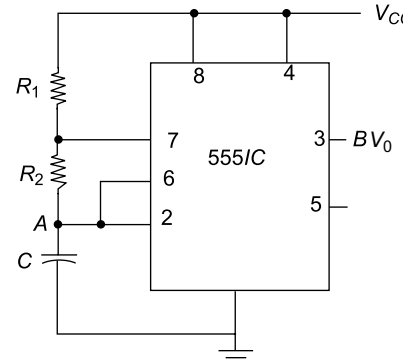


Fig. 9.45 Astable operation of 555 timer IC

Initially, consider R=S=0 and the capacitor voltage must be $V_{CC}/3 < V_C < 2V_{CC}/3$. The flip-flop output $\bar{Q}=0$ and Q=1. As voltage applied to the base of transistor is 0, it is in OFF state. Therefore, the capacitor continuously charging through resistance R_1 and R_2. Then output voltage V_0 is high.

When the capacitor voltage reaches $2V_{CC}/3$, output of comparator -1 (COMP-1) changes from 0 to 1. Hence R=1, S=0 and $\bar{Q}$=1. As a result, the transistor goes ON and output voltage Vo becomes low. Then capacitor starts to discharges towards 0V through the resistance R_2. Hence capacitor voltage starts to decrease. As the capacitor voltage decreases, the output of comparator-1 (COMP-1) changes from 1 to 0. In this time, R=0, S=0. and the flip-flop output Q=0 and $\bar{Q}$=1.

As soon as the capacitor voltage becomes less than $V_{CC}/3$, the comparator-2 (COMP-2) output goes to 1. Then R=0, S=1 and the flip-flop output $\bar{Q}$ is equal to 0. Consequently, the transistor goes OFF and output voltage V_0 becomes high. After that, next cycle of operation is started again. Figure 9.46 shows the output voltage V_0 and capacitor voltage V_C waveforms.

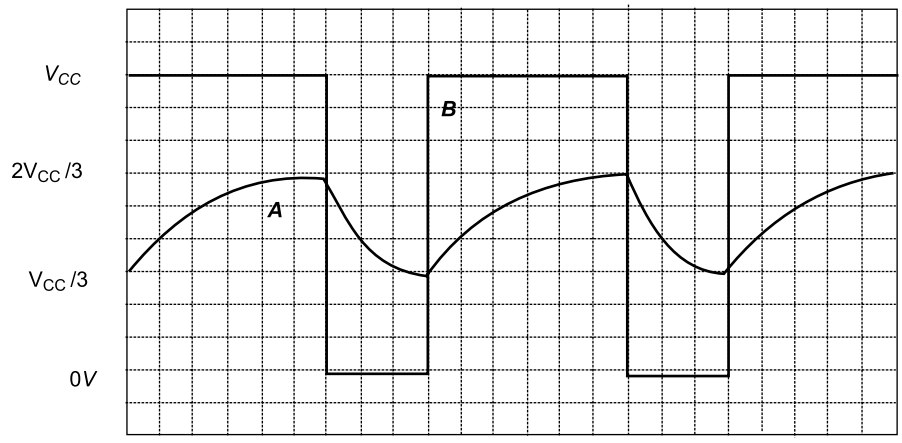


Fig. 9. 46 Capacitor voltage waveform V_C as shown as A and Output voltage waveform Vo as shown as B

When the capacitor is charging, voltage may be expressed as

$$V_C(t) = \frac{2}{3}V_{CC}(1 - e^{-t/(R_1 + R_2)C}) + \frac{1}{3}V_{CC}$$

At a time $t = T_1 \quad V_C = \frac{2}{3}V_{CC}$

After substituting $t = T_1$ and $V_C = \frac{2}{3}V_{CC}$ in the above equation, we get

$$T_1 = C(R_1+R_2).\ ln\ 2 = 0.693C\ (R_1+R_2)$$

During discharging the capacitor voltage is

$$V_C(t) = \frac{2}{3}V_{CC}e^{-t/R_2C}$$

At $t = T_2$, capacitor voltage $V_C = \frac{1}{3}V_{CC}$

After substituting $t=T_2$ and $V_C = \frac{1}{3}V_{CC}$ in the above equation, we find $T_2 = R_2C\ \ln 2 = 0.693CR_2$

The total time period $T= T_1+T_2= 0.693(R_1+2R_2)\ C$

Output frequency, $f = \frac{1}{T_1 + T_2} = \frac{1}{0.693C(R_1 + 2R_2)}$

Duty cycle, $D = \frac{T_1}{T_1 + T_2}$

As the capacitor charges through resistors R_1 and R_2 and discharges through resistor R_2 only, the charging and discharging times are not equal. As a consequence, the output is not a symmetrical square wave. This is possible if R_1 is nearly zero. But it is not possible. To obtain an square wave output, R_1 will be very small compared to R_2. Then charging and discharging times depends on R_2 and C. The frequency of the square wave is approximately $1/0.693(R_1+2R_2)C$.

The other alternative method to generate a square waveform is that the charging path of astable multivibrator is independent of R_2 as shown in Fig. 9.47. Then charging and discharging time can be expressed as given below:

Charging time $T_1 = 0.693R_1C$ and discharging time $T_2 = 0.693R_2C$

When $R_1 = R_2$, T_1 is equal to T_2

To achieve a square waveform, two diodes are connected as shown in Fig. 9.48. There is independent control of the charge and discharge times. The timing capacitor charges through D_1 and R_1 and discharges through R_2 and D_2.

The total time period = $T_1 + T_2 = 1.386\ R_2C$

Output frequency $f = \dfrac{1}{T} = \dfrac{0.722}{R_2C}$

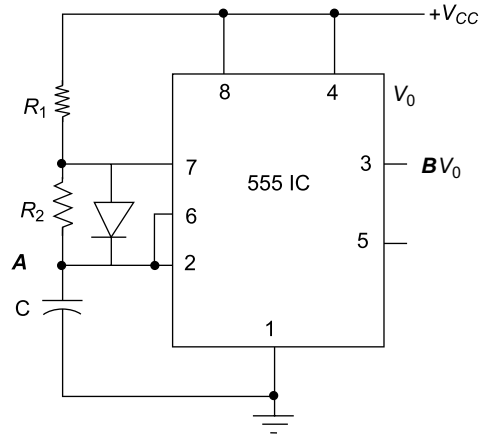


Fig. 9.47 Duty cycle reduction of 555IC

To get a absolutely symmetrical square wave, the timer output is to connect to a toggle flip-flop.

Voltage Controlled Oscillations

To vary the frequency of astable multivibrator output, the control terminal pin - 5 of the 555 timers IC is used. Consider pin - 5 is connected to V volts and $V_{CC} \geq V$. Then threshold voltage of the comparators 1 and 2 are $+V$ and $+V/2$ respectively. The output voltage and capacitor voltage waveforms are shown in Fig. 9.49 when for $2V_{CC}/3 > V$. Then charging and discharging time as follows

$$T_1 = C(R_1 + R_2)\ln\left[\frac{1 - \dfrac{V}{2V_{CC}}}{1 - \dfrac{V}{V_{CC}}}\right]$$

$$T_2 = CR_2\ln 2.$$

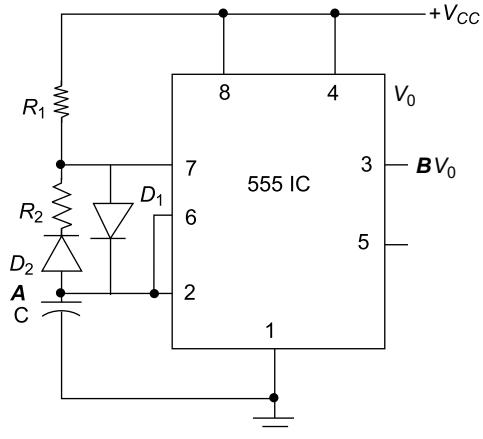


Fig. 9.48 Improved square wave using 555 timer

It is clear from the charging time equation that the charging time is reduced but discharging time does not affected. Therefore, controlling voltage at pin 5 can vary the oscillator frequency. This circuit can be used as *voltage to frequency converter*.

The square wave with different frequency can be generated by proper selection of R_1, R_2 and C. R_1 and R_2 can be varied widely and its range is 1Kohm to 1Mohm. But the capacitance choice is very limited as capacitance is available in few ranges. Therefore, during the design of multivibrator, initially choose the capacitance value. The different values of C are 0.001μF, 0.01μF, 0.1μF, 1μF, and 10μF. Then determine the resistance value using the following expression

$$R_2 = \frac{0.7}{fC},\ \text{when } R_1 \text{ is smaller than } R_2.$$

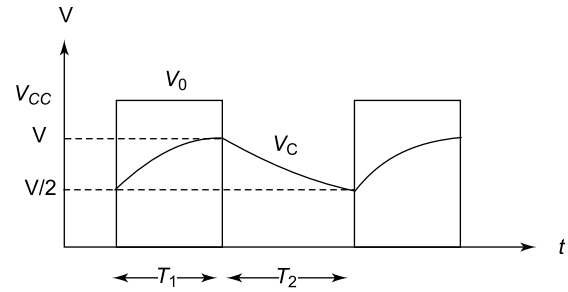


Fig. 9.49 Voltage control oscillator waveforms when pin 5 used to control frequency

If the required on time is greater than off time, choose resistance R_1 which will be approximately ten times of R_2. During the selection of variable resistance, it is best if R_2 is variable. If R_1 is variable, a fixed resistance about fraction of 1Kohm is connected in series with variable resistance. Table 9.1 shows the frequency of astable multivibrator at different value of capacitance and resistances.

Table 9.1 Frequency of astable multivibrator 555

Capacitance C	R_1=1K, R_2=10K	R_1=5K, R_2=50K	R_1=10K, R_2=100K	R_1=5K, R_2=500K	R_1=100K, R_2=1M
0.001μF	68 kHz	13.7 kHz	6.8kHz	1.37 kHz	680Hz
0.01μF	6.8 kHz	1.37 kHz	680Hz	137 Hz	68Hz
0.1μF	680Hz	137 kHz	68Hz	13.7Hz	6.8Hz
1μF	68Hz	13.7 Hz	6.8Hz	1.37 Hz	0.68Hz
10μF	6.8Hz	1.37 Hz	0.68Hz	.137 Hz	0.068Hz

The application of astable multivibrator is the clock signal of flip-flops registers and counters. The low frequency astable multivibrator (f<10Hz) can be used to turn on and off LED and develop flash. The audio frequency astable multivibrator (20KHz ≥ f ≥ 20Hz) can be used to develop sounds from a speaker or a piezo transducer.

Example 9.5 Calculate the frequency and duty cycle of the output of an astable multivibrator using timer 555. Assume R_1=25 K ohm, R_2=50 K ohm and C=0.1μF.

Sol. The frequency is equal to

$$f = \frac{1}{0.693(R_1 + 2R_2)C} = \frac{1.443}{(R_1 + 2R_2)C} = \frac{1.443}{(25 + 2 \times 50) \times 0.1} \text{KHz} = 0.1154\,\text{KHz}$$

$$\text{and Duty cycle} = \frac{R_1 + R_2}{R_1 + 2R_2} = \frac{25 + 50}{25 + 2 \times 50} = 0.6 = 60\%$$

Example 9.6 An astable is shown in Fig. 9.45. It has output frequency 10KHz with duty ratio 60%. Calculate the value of R_2 and C if R_1=3 K ohm.

Sol. Time period = $T = T_1 + T_2 = 0.693\ (R_1 + 2R_2)\ C = \frac{1}{f} = \frac{1}{10}$ ms

Choose $C = 0.01\mu F$

Therefore $(R_1 + 2R_2)$ = 14.43 K ohms

As R_1=3 K ohm , R_2 will be 5.7 K ohms

$$\text{Duty ratio, } D = \frac{R_1 + R_2}{R_1 + 2R_2} = \frac{3 + 5.7}{14.43} = 0.6029 = 60.29\%$$

Example 9.7 The clock output frequency of an astable oscillator is 100KHz , R_1 is 2K and R_2 is 5K. Determine the timing capacitor required for the astable oscillator.

Sol. The capacitor value is equal to

$$C = \frac{1.443}{f(R_1 + 2R_2)} = \frac{1.433}{100(2 + 2 \times 5)}\ \mu\text{F} = 0.0012\ \mu\text{F}$$

9.9.2 Monostable Operation Of 555 Timer

The monostable multivibrator has a stable and a quasi-stable state. Therefore, it is also called one shot. When the output Q is logic 0, flip-flop is in reset state. If the trigger pulse is applied, the output will be high state or Q=1 and it will return to low state after a fixed duration of time. The duration of the pulse is called the time period (T) and this can be determined by using resistor R_1 and capacitor C.

Figure 9.50 shows the monostable multivibrator using 555 timer IC. Initially, consider the trigger voltage is more than $V_{CC}/3$ and output voltage V_0 is low as Q=0 and $\bar{Q}$ =1. As $\bar{Q}$ =1, the transistor Q_1 is ON and the capacitor will be fully discharged. The threshold and trigger comparator outputs are low. Hence $R = 0$ and $S = 0$. The monostable multivibrator can be triggered when the trigger input is less than $V_{CC}/3$.

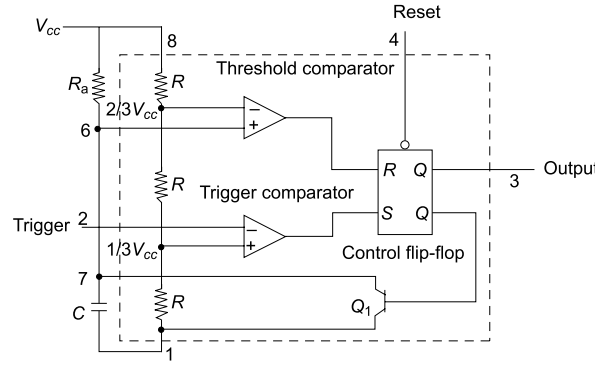


Fig. 9.50 Monostable multivibrator

After the trigger applied, the trigger comparator output momentarily changes from low to high and flip-flops inputs are R=0, S=1. Accordingly, Q=1 and $\bar{Q}$=0, the transistor Q_1 will be OFF and capacitor starts to charge towards V_{CC} through R_1.

When capacitor voltage V_C reaches the value of $2V_{CC}/3$, the threshold comparator output will be high and flip-flops inputs will be R=1, S=0. Then output voltage V_0 becomes low as Q=0 and $\bar{Q}$=1. The transistor Q_1 is ON due to $\bar{Q}$=1 and the capacitor is fully discharged very firstly as turn on resistance of the transistor is small. In this way, cycle will be completed and the capacitor is ready for the next trigger. Figure 9.51 shows the capacitor voltage and output voltage waveforms of monostable multivibrator.

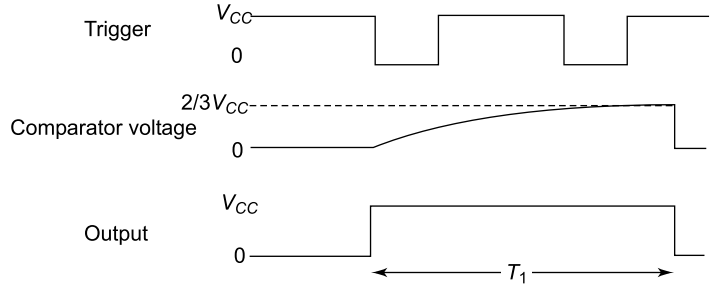


Fig. 9.51 Waveform of monostable multivibrator

The capacitor voltage during charging can be expressed as

$$V_C(t) = V_{CC}\left[1 - e^{-\frac{t}{R_1 C}}\right]$$

At $t = T_1$, capacitor voltage $V_C = 2V_{CC}/3$.

So, $T_1 = R_1 C \ln 3 = 1.1R_1C$

Time period of the pulse is $T_1 = 1.1R_1C$.

The pulse width of monostable multivibrator output can be varied by using the control pin - 5. If a positive voltage V is applied to pin no. - 5, the threshold of the comparator will be changed from $2V_{CC}/3$ to V volts. Therefore, the pulse width of the waveform will be changed to T_1' which can be determined by the expression given below:

$$T_1' = R_1 C \ln\left[\frac{V_{CC}}{V_{CC} - V}\right]$$

9.9.3 Bistable (Flip-flop) Operation Of 555 Timer

Figure 9.52 shows the bistable multivibrator using 555 timer and it has two stable states: output high and output low. Therefore, it is also called as flip-flop. This circuit has two inputs: trigger and reset. Initially, output is low. Tigger makes the output high when trigger input voltage is less than $V_{CC}/3$, 555-timer output will be changed from low to high. Reset makes the output low when reset pin voltage is less than $0.7V_{CC}$, output will be changed from high to low.

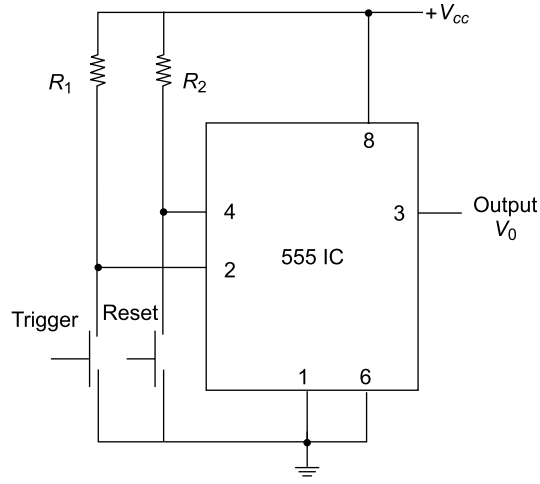


Fig. 9.52 Bistable multivibrator using 555 timer

Example 9.8 Determine the pulse width of the output waveform of a monostable multivibrator as shown in Fig. 9.50 if $R_1 = 100$ K and $C = 0.1$ μF

Sol. Pulse width of the output waveform is $T = 1.1\ R_1 C = 1.1 \times 100 \times 0.1$ ms = 11 ms

9.10 APPLICATIONS OF 555 TIMER

The 555 timers can be used in electronic circuits in different ways. The basic broad use of the 555 timer circuit is either monostable or astable multivibrator. The other applications are missing pulse detector, precision timing, pulse generation, sequential timing, time delay generation, pulse width modulation, pulse position modulation, linear ramp generator, dark detector, power alarm, electric eye alarm, tilt switch, metronome, 10-minute timer, continuous wave oscillator, Schmitt trigger, etc. Some of the above applications are explained below.

Missing Pulse Detector Figure 9.53 shows the missing pulse detector. This circuit is one shot and it is continuously retriggered by the input pulse train. A missing pulse can prevents retriggering before completion of the timing cycle. Then output will be low till a new input pulse arrives and continuous alarms will be developed for a missing pulse.

Electric Eye Alarm Figure 9.54 shows the electric eye alarm. A light dependent resistance (LDR) is used to sense light. When light falls on the LDR, it will be shorted and the timer circuit will be reset. The pitch of speaker can be controlled by varying resistance R_2.

Dark Detector Dark detector circuit is shown in Fig. 9.55. It is used to detect darkness all of a sudden. The light dependent resistance (LDR) is used to detect darkness or illumination below a limit value. Due to absence of light, LDR will be short and circuit will be reset. Then speaker develop the alarm.

Metronome Metronome is used in the music industry to produce the rhythm by a 'toc-toc' sound. The speed of sound can be adjusted by the potentiometer R_1 as shown in Fig.9.56.

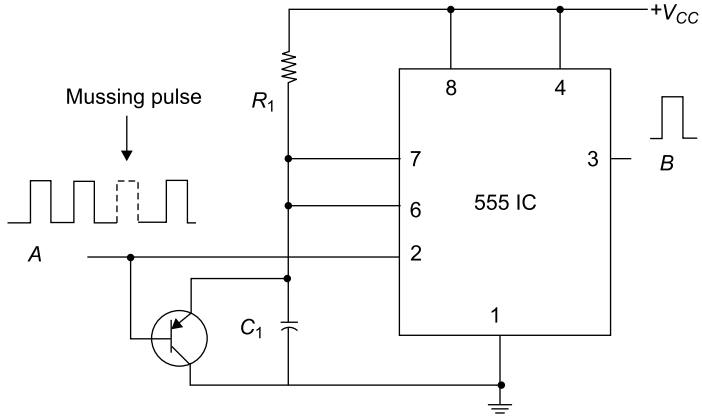


Fig. 9.53 Missing pulse detector

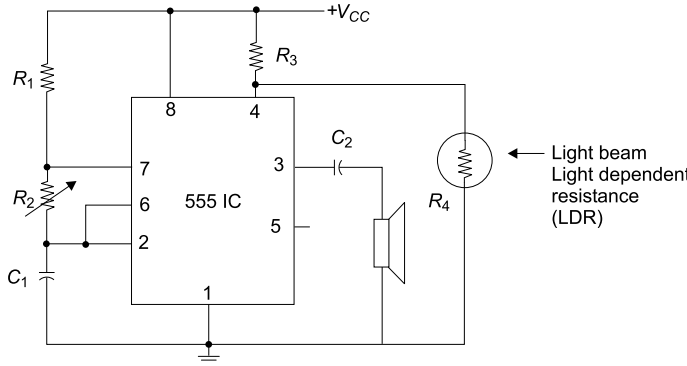


Fig. 9.54 Electric eye alarm

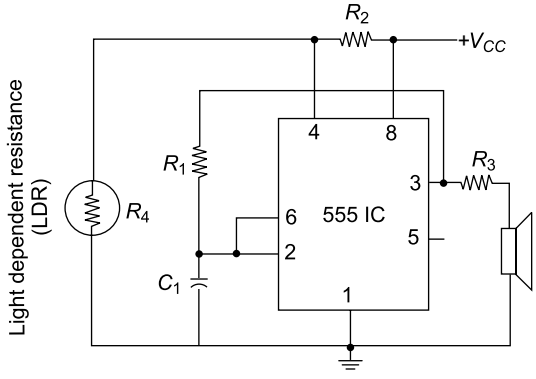


Fig. 9.55 Dark detector

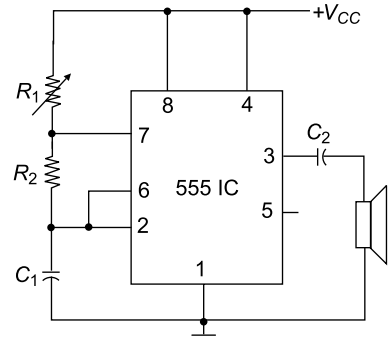


Fig. 9.56 Metronome

10-minute Timer Figure 9.57 shows the 10-minute timer circuit. This circuit can be used as a time-out warning at every ten minutes. It is difficult to keep track of time for longer duration. When the reset switch is pressed, the green light (D_2) ON and time cycle will start. After 10 minutes, Red light (D_1) will be ON to warn the operator for specific operation.

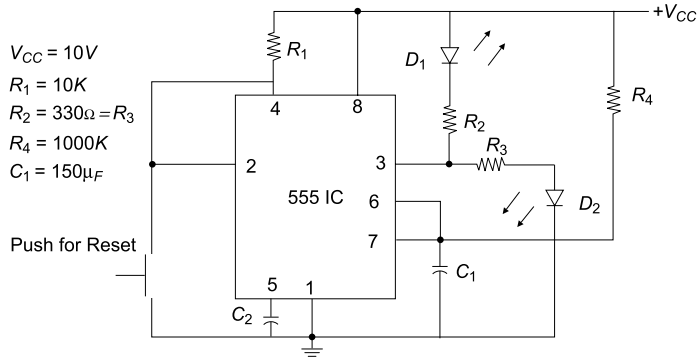


Fig. 9.57 The 10-minute timer

Schmitt Trigger Figure 9.58 shows Schmitt trigger. It removes any noise signal in input and it generates square wave output signal. The output frequency is input frequency divide by 2.

Pulse Sequencer Sometimes, the sequence of pulses are required in certain digital circuits. The pulse widths may be equal width or unequal width, but they must comes one after the other. Generally, pulse sequencer is used to generate a series of pulses in time sequence. Figure 9.59 shows a pulse sequencer circuit, which is actually cascade connection of monostable multivibrators. Here, only two pulses *A* and *B* are sequentially generated as shown Fig. 9.60.

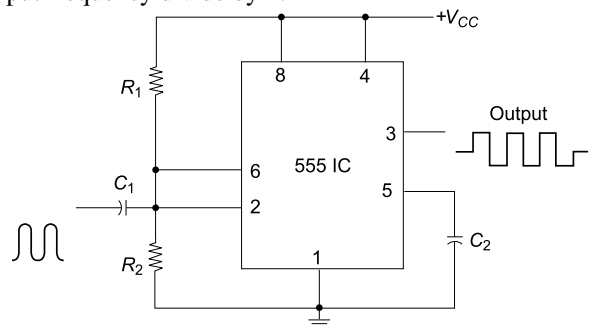


Fig. 9.58 Schmitt trigger

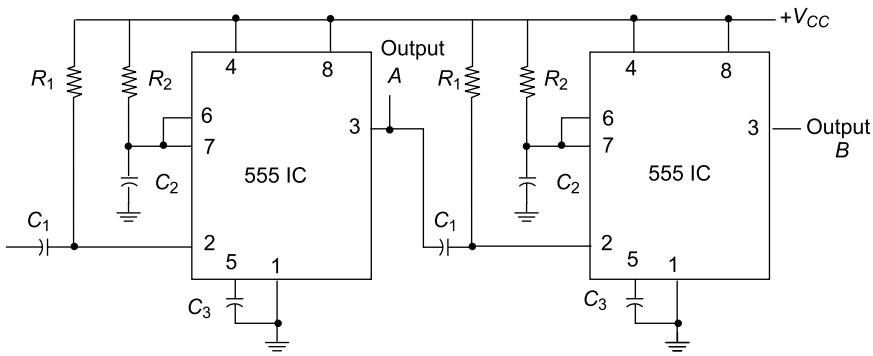


Fig. 9.59 Pulse sequencer circuit

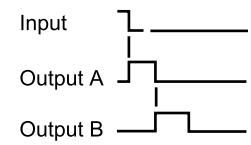


Fig. 9.60 Pulse sequencer output waveform

The sequence starts with the falling edge of the trigger pulse. The first monostable multivibrator is edge triggered and output *A* changes from low to high. Output *A* will remain high for certain duration depending upon the circuit parameters and then return back to low state. At that time, the next monostable multivibrator will be triggered and output *B* changes from low to high. Then output *B* will remain high for certain duration depending upon resistance and capacitance and again return back to low state. In this way, two sequence pulses are generated. At the end of the output *B*, the sequence is completed and all timers again wait for the next triggering signal.

Review Exercises

Short-Answer Questions

1. What are the types of multivibrators?

Ans. There are three types of multivibrators such as astable multivibrator, monostable multivibrator and bistable multivibrators.

2. What is other name of astable multivibrators?

Ans. Astable multivibrator is also known as free running multivibrator.

3. Why an astable multivibrator is also called a square wave generator?

Ans. An astable multivibrator has two quasi-stable states and it continues to oscillate between two stable states. This multivibrator has no stable state and external trigger pulses are not required to change the states. This device can be used to generate square wave and the time duration depends upon circuit parameters. Therefore, an astable multivibrator is also called a square wave generator.

4. How an astable multivibrator can be converted into monostable multivibrator?

Ans. A monostable multivibrator can be obtained from an astable multivibrator by replacing R-C timing circuit by dc voltage divider.

5. Why are monostable multivibrators called the one-shot multivibrator?

Ans. Monostable multivibrators can be used to generate one output pulse for each trigger pulse. Therefore, monostable multivibrators are sometimes called the one-shot multivibrator.

6. Why monostable multivibrator is called a delay circuit?

Ans. As monostable multivibrator can be used to generate a fast transition at a predetermined time T after applying the input trigger, monostable multivibrator is called a delay circuit.

7. Why bistable multivibrator is called a flip-flop multivibrator?

Ans. In a bistabe multivibrator, when a trigger pulse is applied, the multivibrator state changes from one stable to the other stable state. When the next trigger pulse is applied, it changes from present stable state to its original state. Therefore, it is called the flip-flop multivibrator.

8 What are the applications of 555 timer?

Ans. The applications of 555 timer are missing pulse detector, electric eye alarm, dark detector, metro-name, 10-minute timer, Schmitt trigger, and pulse sequencer.

9. Give a list of applications of the Schmitt trigger circuit?

Ans. The applications of the Schmitt trigger circuit are

- Amplitude comparator
- Level detector,
- Flip-flop circuit
- Rectangular or square waveshapes generator

10. What is multivibrator?

Ans. Multivibrator is basically a two-stage amplifier where output of one amplifier is used as feedback to the input of the other.

Multiple-Choice Questions

1. An astable multivibrator has
   (a) One stable state (c) One quasi-stable state
   (b) Two stable state (d) Two quasi-stable state
2. An monostable multivibrator has
   (a) One stable state (c) One quasi-stable state
   (b) Two stable state (d) Two quasi-stable state
3. An bistable multivibrator has
   (a) One stable state (c) One quasi-stable state
   (b) Two stable state (d) Two quasi-stable state
4. If an multivibrator has one stable and one quasi-stable, the circuit is called as
   (a) Astable multivibrator (c) Bi-stable multivibrator
   (b) Monostable multivibrator (d) None of these
5. Pulse stretches is the alternative name of
   (a) Monostable multivibrator (c) 555 timer
   (b) Flip-flop (d) Schmitt-trigger
6. A 555 timer consists of
   (a) Two comparator, one flip-flop and one transistor
   (b) Only operational amplifiers
   (c) One comparator, one flip-flop
   (d) None of these
7. Which multivibraor can able to convert 10μs pulse into a 10ms pulse?
   (a) Astable multivibrator (c) Bi-stable multivibrator
   (b) Monostable multivibrator (d) None of these
8. A 556 timer IC consists of
   (a) Two 555 timer (b) Three 555 timer
   (c) Four 555 timer (d) None of these
9. A monostable multivibrator consists of
   (a) Operational amplifiers (c) 555 timer
   (b) Logic gates (d) All of these
10. A Schmitt trigger circuit is a
    (a) Monostable multivibrator (c) Free-running multivibrators
    (b) Bi-stable multivibrator (d) None of these
11. If RESET pin of 555IC is made low, then
    (a) output is high (b) output is low
    (c) IC will not work (d) IC may be damaged
12. Multivibrators
    (a) generate square wave (b) convert sine to square wave
    (c) convert triangular to sine wave (d) convert triangular to square wave

Review Questions

1 Define multivibrator. What are the types of multivibrator? Explain any one multivibrator with circuit diagram and waveforms.

2 Draw the circuit diagram of monostable multivibrator using BJT and explain its operation.

3 Justify that Fig. 9.61 behaves as an monostable multivibrator

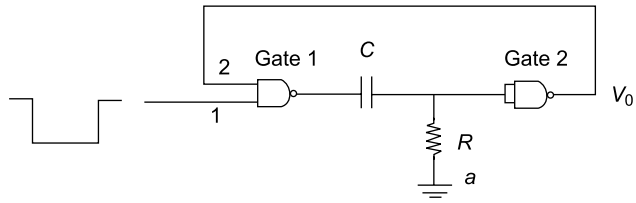


Fig. 9.61

4. Verify that Fig. 9.62 behaves as an astable multivibrator
5. Explain application of operational amplifier in monostable multivibrator circuit. Why Zener diodes are used in this circuit?
6. Draw the functional block diagram of 555 timer. Explain the operation of different section of 555 timer.
7. Describe the monostable operation of 555 timer. Derive a expression to determine the pulse width.
8. Draw the voltage waveforms of the Fig. 9.63 at *A* and *B*.
9. What are the applications of 555 timer? Explain any two applications briefly.
10. What is pulse sequencer? Draw a pulse sequencer circuit and explain it's operation.
11. Consider IC 555 timer is operating in stable mode with R_1=4.7 K ohms and R_2=2.2 K ohms. If the timing capacitor is 0.47μF, determine the frequency of oscillations of the multivibrator circuit
12. If IC 555 timer is operating as an monostable multivibrator to generate a pulse width of 25μs, give details of the circuit.
13. What are the advantages of Schmitt trigger circuit? Explain the operation of a schmitt trigger circuit using operational amplifier.
14. What is the difference between non-triggerable and re-triggerable monostable multivibrator circuit? Explain with necessary diagram.

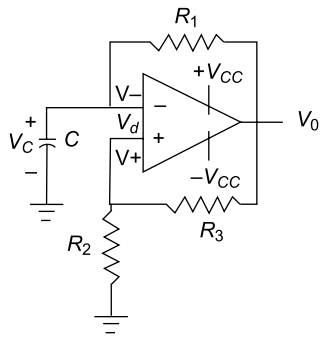


Fig. 9.62

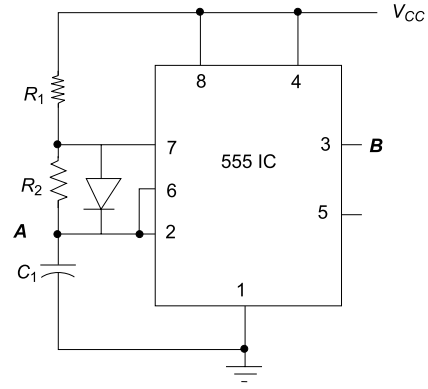


Fig. 9.63

15. Determine the frequency and duty cycle of the output of an astable multivibrator-using timer 555 if $R_1 = 205$ K ohm, $R_2 = 40$K ohm and $C = 0.1\mu$F.
16. Determine the timing capacitor of an astable oscillator when the clock output frequency is 50 KHz. Assume resistance R_1 and R_2 as per requirement.
17. If $V_{ref} = -2$ V and $V_i = 5 \sin \omega t$ in Fig. 9.64, draw the output waveform.
18. How 555IC can be used as a monostable multivibrator? Derive an expression for duration of output pulse.

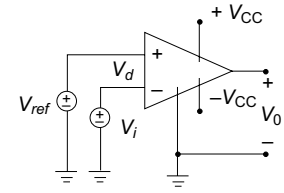


Fig. 9.64

19. The 555IC is connected with external resistance R_1 = 100 kΩ, R_2 = 30 kΩ and C = 100 nF. What is the frequency of the output signal? What is the duty cycle.
20. Draw the circuit diagram of an astable multivibrator using 555 timer. Derive the expression for the frequency of oscillation of the astable multivibrator. Prove that duty cycle of the output is always greater than 50%. How the duty cycle can be 50% by adding a diode?
21. Give the internal construction of 555 timer and explain its function.
22. (a) Draw the circuit and explain the operation of a monostable multivibrator using two *npn* transistors.
    (b) Draw and explain the operation of a monostable multivibrator using 741IC. What are its uses?
    (c) In 555 timer monostable multivibrator using R = 100 kΩ and time delay = 100 μs. Calculate the value of C.

ANSWERS

Multiple-Choice Questions

1. (d)	2. (a)	3. (b)	4. (b)	5. (a)	6. (a)
7. (b)	8. (a)	9. (d)	10. (b)	11. (b)	12. (a)

CHAPTER

10

Phase Locked Loops and VCO

10.1 INTRODUCTION

Phase Locked Loop (PLL) principle is used in different applications such as radar synchronisation and communication applications, frequency modulation (FM) stereo decoder, motor speed control, frequency synthesised transmitters and receivers, tracking filters, frequency modulation and demodulators and frequency shift keyine (FSK) decoders. PLL is also used for generation of local oscillator frequencies in TV and in FM tuners and also in satellite communication systems. Now a days, the phase locked loop is available in a single package IC. For example, NE 560 series (560, 561, 562, 564, 565 and 567) and SE 560 series ICs are commercially available.

10.2 OPERATING PRINCIPLE OF PLL

The schematic block diagram of a PLL is shown in Fig. 10.1 which consists of

- Phase detector/Comparator
- A low pass filter
- An error amplifier
- A voltage controlled oscillator (VCO)

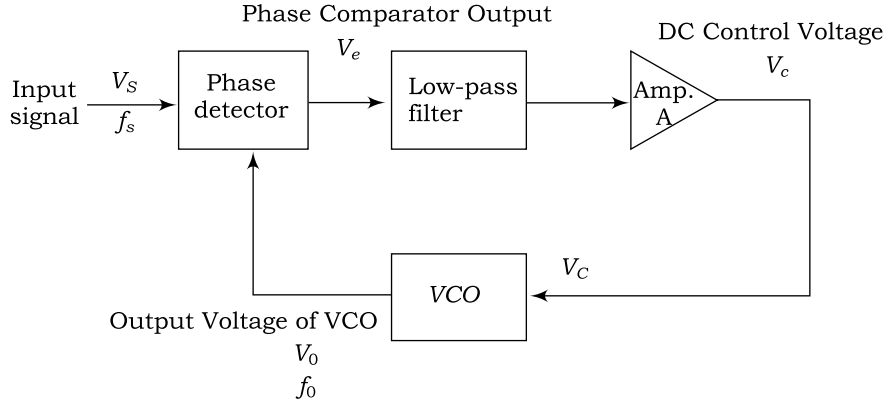


Fig. 10.1 Block diagram of Phase Locked Loop (PLL)

Input signal V_s having frequency f_s is applied to phase detector. The output of VCO is V_O and its frequency is f_o. The phase detector compares the phase and frequency of the in coming signal and output signal and generate an error voltage V_e. The phase detector circuit generates the frequency sum $f_s + f_o$ and difference $f_s - f_o$. The low pass filter is used to remove the high frequency signal. The output of low pass filter is $f_s - f_o$ frequency signal which is applied to a amplifier for amplification. The amplifier output is V_c which is fed to voltage controlled oscillator (VCO).

The amplitude of V_c shifts the VCO frequency in the direction so that the frequency difference between f_s and f_o reduces. If this action starts, the signal operates in *capture range*.

The frequency of VCO output changes continuously till the output frequency is exactly equal to the frequency of input signal. As soon as $f_s = f_o$, the circuit becomes locked. Once the locked occurs, the output frequency f_o of VCO is same as f_s, but there is a finite phase difference ϕ. The phase difference ϕ generates a corrective control voltage V_c to shift the output frequency of VCO from f_o to f_s and the lock will be maintained.

Once the circuit is locked, PLL tracks the frequency changes of the input signal. Hence PLL operates in three stages- free running, capture and locked or tracking.

The capture transient of PLL is depicted in Fig. 10.2. When capture starts, a small sine wave appears due to the difference frequency between the output frequency of VCO and the frequency of input signal. The amplifier output, i.e., dc component drives the VCO towards the lock. Each successive cycle generates the VCO frequency to move closer to the input signal frequency. When the difference in frequency becomes smaller, large dc component is passed through filter and the output frequency of VCO is again shifted. This process continues until VCO locks on to the signal.

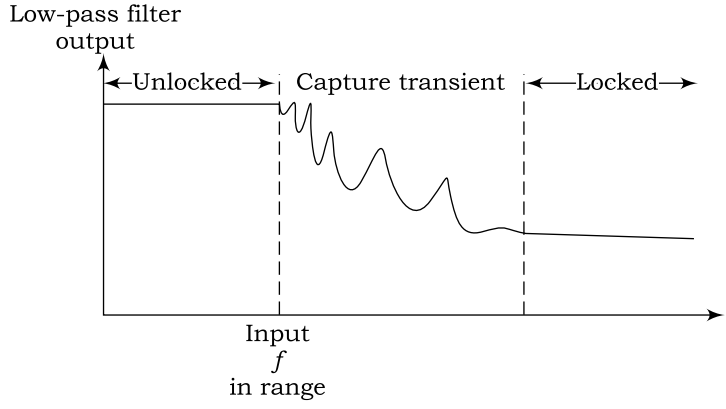


Fig. 10.2 Capture transient of PLL

Actually the low pass filter controls the capture range. The VCO frequency is far away, the frequency will be too high to pass through the filter and PLL will not respond. Then the signal is out of the capture band. But once locked occurs, the filter no longer restricts the PLL. Hence VCO can able to track the signal beyond the capture band and the tracking range is always larger than the capture range.

Lock-in range: When PLL is locked, it can track frequency changes in the input signal. There is a range of frequencies over which PLL can maintain lock with the input signal is called the lock in range or *tracking range*. Generally, the lock range is represented by a percentage of f_o, output frequency of VCO.

Capture range: The capture range is the range of frequencies over which the PLL can acquire lock with an input signal. This is also expressed as percentage of f_o.

Pull in Time: The pull in time is the total time taken by the PLL to establish lock. This time depends on the initial phase difference and frequency difference between the two signals, the overall loop gain and filter characteristics.

10.3 PHASE DETECTOR

The phase detection is the most essential part of any PLL system. There are two types of phase detectors such as analog phase detector and digital phase detector. These phase detectors are commonly used in PLL.

10.3.1 Analog Phase Detector

Figure 10.3 shows the operating principle of analog phase detection, the electronic switches are opened and closed by the signal coming from VCO, i.e., square wave. The input signal is chopped at a repetition rate determined by VCO frequency.

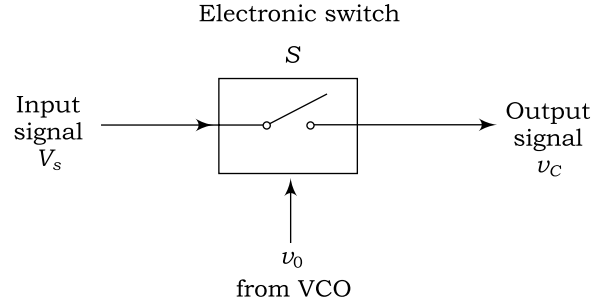


Fig. 10.3 Analog phase detector

When the input signal V_s is in phase with VCO output voltage V_o, phase difference is $\phi = 0°$. Switch S is closed while the VCO output is positive and the output voltage waveform V_e will have positive half of sinusoidal signal. For phase difference $\phi = 90°$, the output voltage waveform is shown in Fig. 10.4.

When the phase difference $\phi = 180°$, the output voltage waveform V_e will be negative half of sinusoidal signal while the VCO output is positive.

This type of phase detector is called a half wave detector, as the phase information for only one-half of the input waveform is detected and averaged. The output of phase detector is filtered through a low pass filter; the output signal of filter is an error signal which is the average value of the output waveform as depicted in Fig. 10.4.

At phase difference $\phi = 0°$, error voltage V_e is positive

At phase difference $\phi = 90°$, error voltage V_e is zero

At phase difference $\phi = 180°$, error voltage V_e is negative

Analysis of Analog Phase Detection

Actually phase detector or comparator is a multiplier which can multiply the input signal by the output signal of VCO.

After multiplication, the output signal is

$$V_e = kV_sV_o \sin(2\pi f_s t)\sin(2\pi f_o t + \phi)$$

Where, k is the phase comparator gain

ϕ is the phase shift between the input signal and the VCO output.

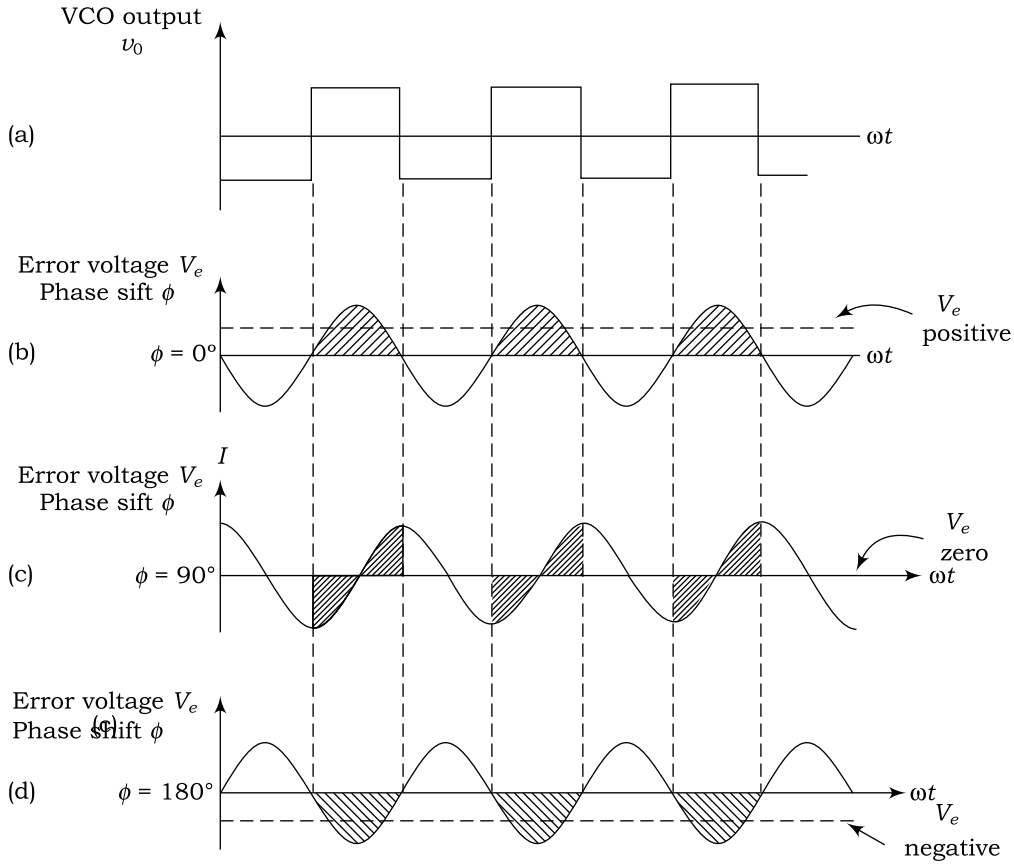


Fig. 10.4 Analog phase detector (a) VCO output voltage V_o (b) Error voltage V_e at $\phi = 0°$ (c) Error voltage V_e at $\phi = 90°$ (d) Error voltage V_e at $\phi = 180°$

The above expression can be written as

$$V_e = \frac{1}{2} kV_s V_o [\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)]$$

When the circuit is locked, $f_o = f_s$

$$V_e = \frac{1}{2} kV_s V_o [\cos(-\phi) - \cos(4\pi f_o t + \phi)]$$

The phase detector output contains a double frequency term and a dc component $V_e = \frac{1}{2} kV_s V_o \cos\phi$ which varies as a function of ϕ. When the output of phase detector passes through the low pass filter, the dc signal will be output from filter. Then the dc signal is applied to the modulating input terminal of a VCO.

When a perfect locked occurs and $f_o = f_s$, the phase shift is $\phi = 90°$ and error signal is zero $V_e = 0$.

The output voltage V_e is directly proportional to the input signal amplitude V_s. The phase detector gain and the loop gain dependent on the input signal amplitude. The output voltage V_e is directly proportional to cos ϕ and the relationship between V_e and cos ϕ is non-linear.

The above problems can be removed by limiting the amplitude of the input signal. Therefore, input signal is converted into a constant amplitude square wave. Figure 10.5 shows a phase detector circuit with square wave inputs.

This circuit is also known as a *balanced modulator* and it is used as full wave switching phase detector. The input signal is applied to the differential pair T_1 and T_2.

SPDT (Single Pole Double Through) Switch

Transistors $T_3 - T_4$ and $T_5 - T_6$ act as single pole double through switch. These switches are activated by the VCO output. The amplitude of V_o and V_s is such that transistors will be fully on and off.

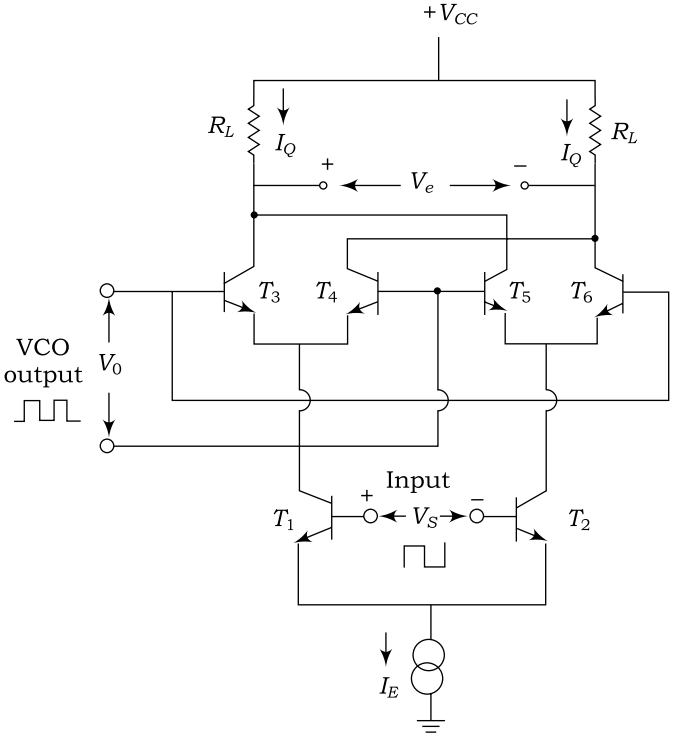


Fig. 10.5 Analog phase comparator

From the time 0 to $\pi - \phi$, transistors T_1 and T_3 are ON and current I_E flows through T_1 and T_3. Then the output voltage is $V_e = -I_E R_L$.

During time from $\pi - \phi$ to π, V_s is high and V_o is low. Transistors T_1 and T_4 are ON and the output voltage is $V_e = I_E R_L$

The average value of phase detector output voltage is

$$V_e = \frac{1}{\pi}(A_1 + A_2) = \frac{1}{\pi}[I_E R_L \phi + (-I_E R_L)(\pi - \phi)]$$

$$= \left(\frac{2\phi}{\pi} - 1\right) I_E R_L = \left(\frac{2\phi}{\pi} - 1\right) 2 I_Q R_L$$

$$= \frac{4}{\pi} I_Q R_L \left(\phi - \frac{\pi}{2}\right) = K_\phi \left(\phi - \frac{\pi}{2}\right)$$

Where, K_ϕ is constant

The relationship between V_e and ϕ is linear as shown in Fig. 10.7.

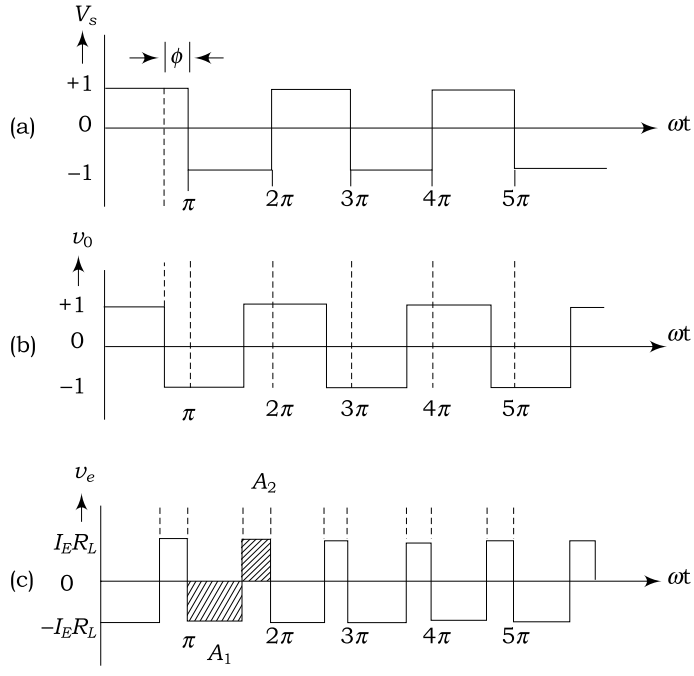


Fig. 10.6 Timing diagram for (a) V_s (b) V_o and (c) V_e

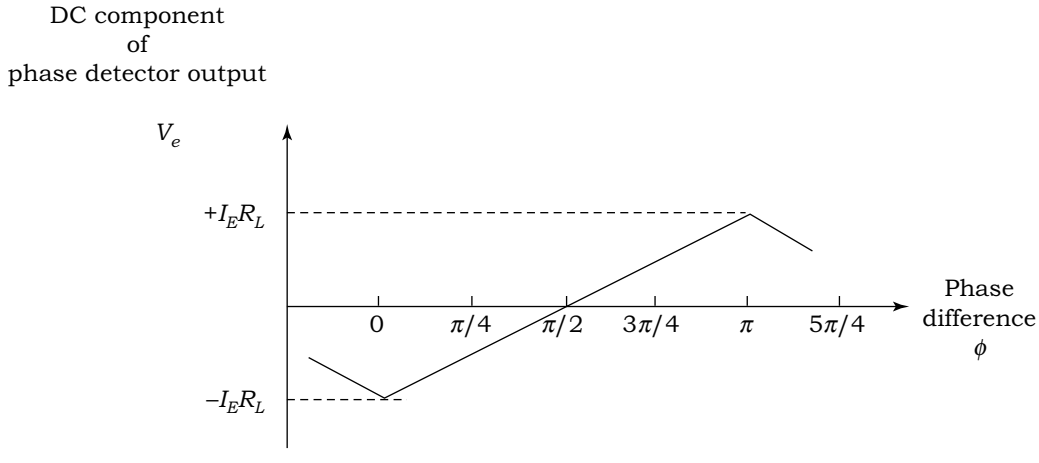


Fig. 10.7 Relationship between V_e and ϕ

10.3.2 Digital Phase Detector

XOR gate can be used in digital phase detector as shown in Fig. 10.8. The output of the XOR gate is high, when any one of the two input signals f_o or f_s is high. Both the input signals are square wave. The phase difference between two signals is ϕ. The variation of output voltage depends on the phase difference as shown in Fig. 10.8. When the phase difference between two signals is ϕ, the variation of output voltage depends on

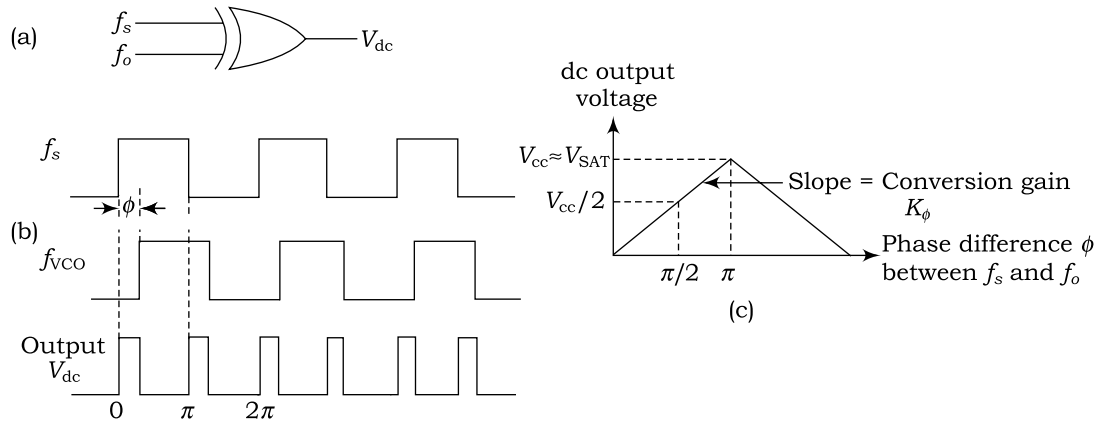


Fig. 10.8 Digital phase detector (a) Ex-OR gate (b) Input and output waveforms (c) Relationship between dc output voltage and phase difference.

the phase difference ϕ as shown in Fig. 10.8(c). When the phase difference is $\phi = 180°$, the output is the maximum dc output voltage. The slope of the curve K_ϕ of the phase detector with the supply voltage $V_C = 5$ V is

$$K_\phi = \frac{5}{\pi} = 1.59\text{V/rad}$$

10.4 VOLTAGE CONTROLLED OSCILLATOR (VCO)

The block diagram of VCO is shown in Fig. 10.9 and the PIN diagram of 566 VCO is depicted in Fig. 10.10. The timing capacitor C_T is linearly charged or discharged by constant current source or sink. The amount of current can be controlled by changing the voltage V_C applied at the modulating input or by changing the value of resistance R_T. The voltage at pin 6 is equal to the voltage at pin 5. If the modulating voltage at pin 5 increases, the voltage at pin 6 also increases.

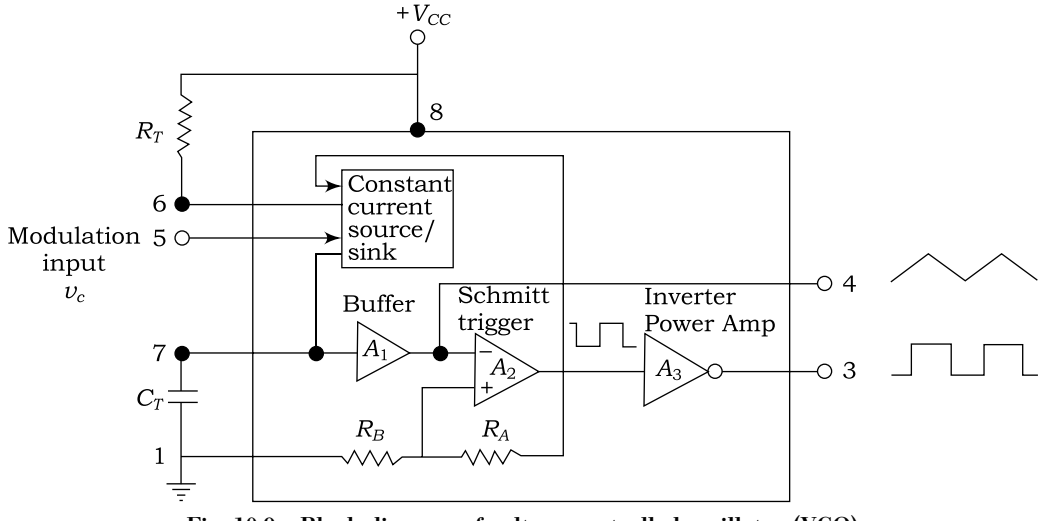


Fig. 10.9 Block diagram of voltage controlled oscillator (VCO)

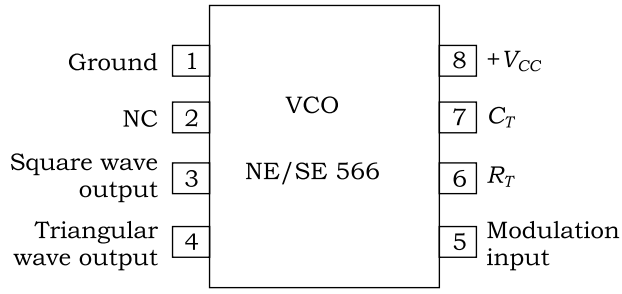


Fig. 10.10 Pin diagram of voltage controlled oscillator (VCO)

The voltage across C_T is also applied to the inverting input terminal of Schmitt trigger A_2 through a buffer A_1. The output voltage swing of the Schmitt trigger is varied in between +0.5 V_{CC} and V_{CC}. When resistance R_A is equal to R_B in the positive feedback loop, the voltage at non-inverting terminal of Schmitt trigger A_2 varies between from $0.5V_{CC}$ to $0.25V_{CC}$. When the voltage across capacitor C_T is greater than $0.5V_{CC}$ during charging, the output of Schmitt trigger becomes low, i.e., $0.5V_{CC}$. After that capacitor starts to discharge and when it reaches at $0.25V_{CC}$, the output of Schmitt trigger becomes high, i.e., V_{CC}. The source and sink currents are equal, the charging time of capacitor is equal to discharging time of capacitor.

Therefore, the voltage across C_T is a triangular wave, which is available at output terminal. The output Schmitt trigger is a square wave which is inverted by inverter A_3. Hence a square wave output voltage is available at pin 3. The output waveforms at pin 4 and pin 3 are shown in Fig. 10.12. The voltage across capacitor charges from $0.25V_{CC}$ to $0.5V_{CC}$. The change in voltage is $\Delta V = 0.25V_{CC}$

Assume the capacitor changes with a constant current source i

Then $$i = \frac{\Delta V}{\Delta t} C_T \text{ as } i = C\frac{dV}{dt}$$

Or, $$i = \frac{0.25V_{CC}}{\Delta t} C_T$$

Or, $$\Delta t = \frac{0.25V_{CC}}{i} C_T$$

The time period of triangular waveform is

$$T = 2\Delta t = \frac{0.5V_{CC}}{i} C_T$$

The frequency of oscillator is

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t}$$

Therefore, $$f_o = \frac{i}{0.5V_{CC}C_T} = \frac{2i}{V_{CC}C_T}$$

Since current $i = \frac{V_{CC} - v_c}{R_T} C_T$, $f_o = \frac{2i}{V_{CC}C_T} = \frac{2}{R_T C_T}\frac{(V_{CC} - v_c)}{V_{CC}}$ (10.1)

It is clear from equation (10.1) that the output frequency of the VCO can be changed by-
(i) R_T (ii) C_T (iii) the voltage at the modulating input terminal.

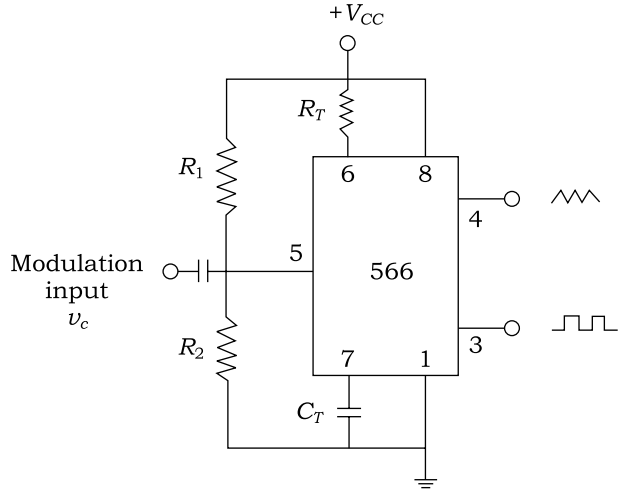


Fig. 10.11 Connection diagram of IC 566

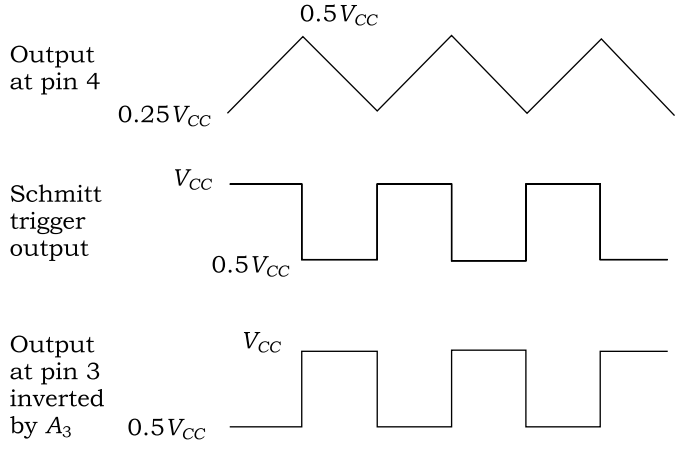


Fig. 10.12 Voltage Waveforms

The voltage V_c can be varied by resistance R_1 and R_2. The value of R_T and C_T are selected in such a way that the output frequency of VCO lies in the centre of the operating frequency range. Usually modulating input voltage can be varied from $0.75V_{CC}$ to V_{CC} and frequency variation will be about 10 to 1.

If there is no modulating signal, the voltage at pin 5 is $\frac{7}{8}V_{CC}$, the VCO output frequency is

$$f_o = \frac{2}{R_T C_T} \frac{V_{CC} - \frac{7}{8}V_{CC}}{V_{CC}} = \frac{1}{4R_T C_T} = \frac{0.25}{R_T C_T}$$

Hence, $$R_T C_T = \frac{0.25}{f_o}$$

Voltage to Frequency (V to f) Conversion Factor

The most important parameter of V to f conversion factor is K_v and it is expressed by

$$K_V = \frac{\Delta f_o}{\Delta V_c}$$

Where, ΔV_C is the modulation voltage required to generate the frequency shift Δf_o.

If the original frequency is f_o and the new frequency is f_i, the frequency shift is equal to

$$\Delta f_o = f_i - f_o$$

After substituting the value of f_i and f_o,

$$\begin{aligned}\Delta f_o &= f_i - f_o \\ &= \frac{2(V_{CC} - V_C + \Delta V_c)}{R_T C_T V_{CC}} - \frac{2(V_{CC} - V_C)}{R_T C_T V_{CC}} \\ &= \frac{2\Delta V_c}{R_T C_T V_{CC}}\end{aligned}$$

Therefore, $$\Delta V_C = \frac{\Delta f_o R_T C_T V_{CC}}{2}$$

Since $$R_T C_T = \frac{0.25}{f_o},\ \Delta V_C = \frac{\Delta f_o V_{CC}}{2}\frac{0.25}{f_o}$$

Therefore, $$\frac{\Delta f_o}{\Delta V_C} = \frac{8 f_o}{V_{CC}}$$

10.5 LOW PASS FILTER

The low pass filter is used in PLL to remove the high frequency components and noise. It is also used to control the dynamic characteristics of PLL. The main characteristics of PLL are:

- Capture and lock range
- Band-width
- Transient response

When the bandwidth of filter reduces, the response time increases. But with the reduction of bandwidth of filter, the capture range of the PLL reduces. The storage charge on the filter capacitor provides a short time memory to the PLL.

When the signal is less than noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO. Hence high noise immunity and locking stability will be achieved. Usually passive and active filters are used in PLL as depicted in Figs 10.13 and 10.14 respectively.

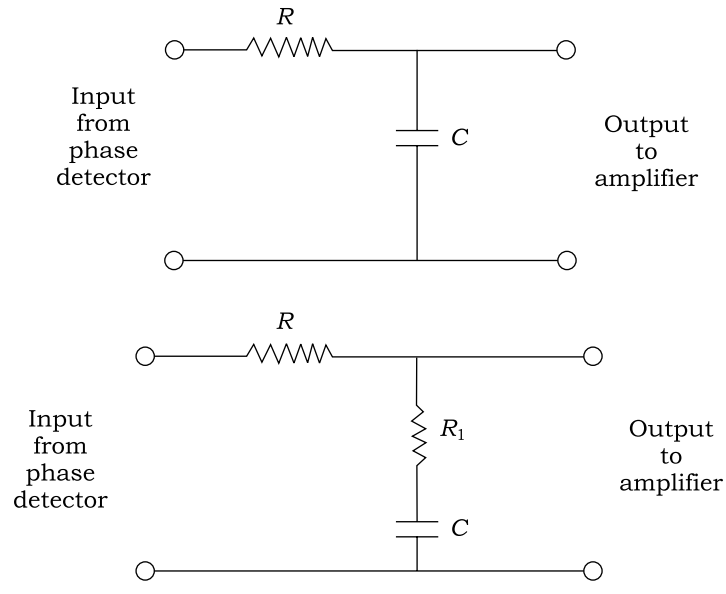


Fig. 10.13 Passive filter

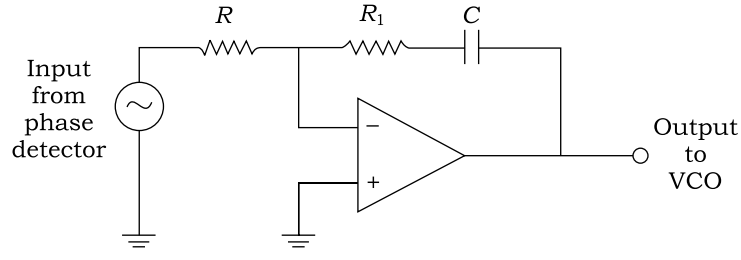


Fig. 10.14 Active filter

10.6 MONOLITHIC PHASE LOCKED LOOP

All building blocks of a PLL are placed in an independent IC package and these blocks can be externally interconnected to get a PLL which is known as monolithic PLL. The most commonly used monolithic PLL ICs are SE/NE 560 series ICs such as SE/NE 560, 561, 562, 564, 565 and 567 and LM560 series ICs. In this section, the operating principle of 565 PLL IC is discussed briefly.

The block diagram of 565 PLL IC is shown in Fig. 10.15. This IC available as a 14 –pair DIP package and as a 10-pair metal can package. The pin diagram of 565 PLL IC is depicted in Fig. 10.16. The important electrical parameters of 565 PLL IC are given below:

Table 10.1 Electrical parameters of 565 PLL IC

Electrical Parameters	*Range*
Operating frequency range	0.001 Hz to 500 kHz
Operating voltage range	± 6 V to ± 12 V
Input level required for Tracking	10 mV rms minimum to 3 V peak-to-peak maximim

(Contd.)

(Contd.)

Input impedance	10 kΩ typical
Output sink current	1 mA typical
Output source current	10 mA typical
Drift in VCO centre frequency with temperature	300 ppm/°C (parts per million per degree centigrade)
Drift in VCO centre frequency with supply voltage	1.5%/ V maximum
Triangular wave amplitude	2.4 V_{PP} at ± 6 V supply voltage
Square wave amplitude	5.4 V_{PP} at ± 6 V supply voltage
Bandwidth adjustment range	< ±1 to ±60%

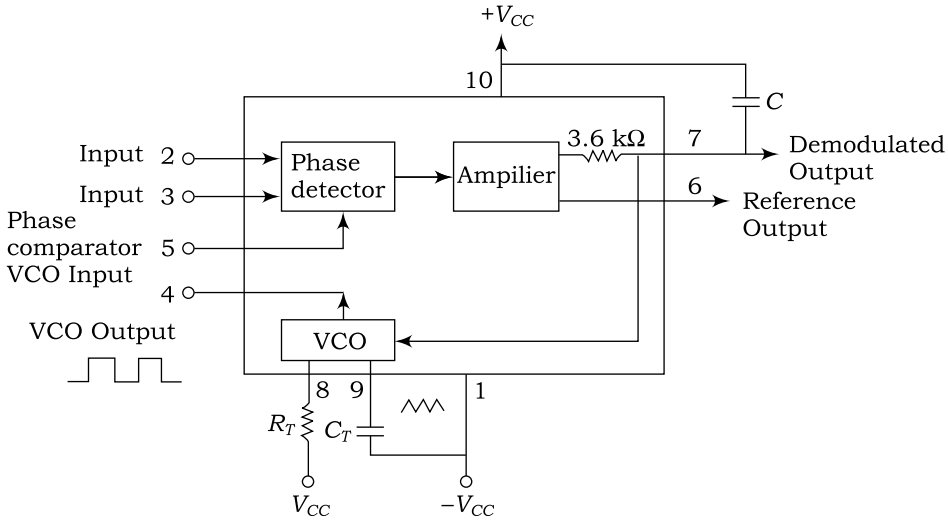


Fig. 10.15 Block diagram of 565 PLL IC

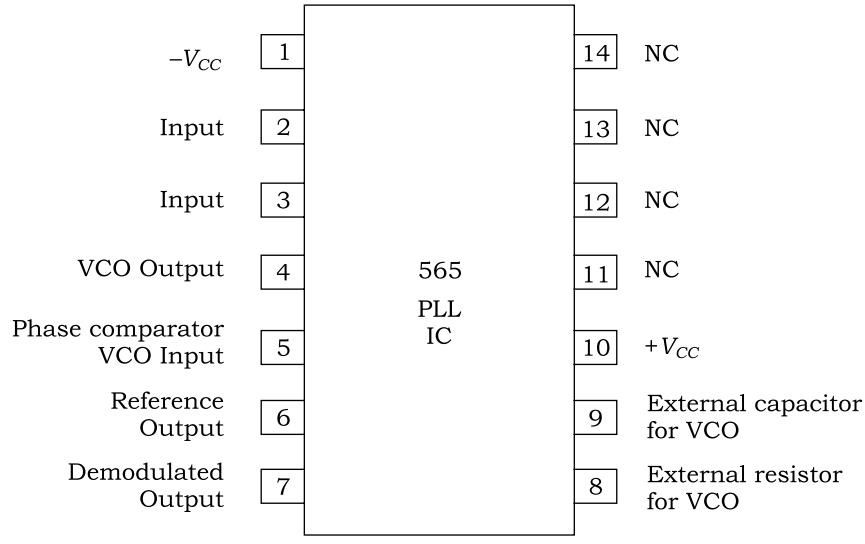


Fig. 10.16 PIN diagram of 565 PLL IC

The centre frequency of PLL is determined by the free running frequency of VCO and it is expressed by

$$f_o = \frac{0.25}{R_T C_T} \text{ Hz}$$

Where, R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. The VCO free running frequency can be varied by adjusting R_T and C_T to be at the centre of the input frequency range. C_T can be any value but the value of R_T must be lies in between 2 kΩ to 20 kΩ. A capacitor C is connected between pin 7 and pin 10 forms a first order low pass filter with the internal resistance of 3.6 kΩ. The value of filter capacitor should be large enough to eliminate variations in the demodulated output voltage at pin 7 in order to stabilize the VCO frequency.

10.6.1 Derivation of Lock-in Range

The lock-in range of PLL can be defined as the range of frequencies over which PLL can be maintaining lock with the incoming signal. If the ϕ radians are the phase difference between the signal and the VCO voltage, the analog output voltage of the analog phase detector is expressed as

$$V_e = K_\phi \left(\phi - \frac{\pi}{2} \right)$$

Where, K_ϕ is the phase angle to voltage transfer coefficient of the phase detector.

The control voltage to voltage control oscillator (VCO) is

$$V_C = AK_\phi \left(\phi - \frac{\pi}{2} \right)$$

Where, A is the voltage gain of amplifier

The control voltage V_C shifts VCO frequency from its free running frequency f_o to a frequency f is given by

$$f = f_o + K_V V_C$$

Where, K_V is the voltage to frequency transfer coefficient of the VCO.

Assume that PLL is locked in to signal frequency f_s and then

$$f = f_s = f_o + K_V V_C$$

Or,
$$V_C = \frac{f_s - f_o}{K_V} = AK_\phi \left(\phi - \frac{\pi}{2} \right)$$

Or,
$$\frac{f_s - f_o}{K_V A K_\phi} = \left(\phi - \frac{\pi}{2} \right)$$

Therefore,
$$\phi = \frac{\pi}{2} + \frac{f_s - f_o}{K_V A K_\phi}$$

The maximum output voltage available from the phase detector occurs for $\phi = \pi$ and $\phi = 0$ radian. The maximum control voltage to drive the VCO is

$$V_{C(\max)} = \pm \frac{\pi}{2} K_\phi A$$

The maximum swing of VCO frequency is

$$(f - f_o)_{\max} = \Delta f_L = K_V V_{C(\max)} = K_V K_\phi A \frac{\pi}{2}$$

Or,
$$2\Delta f_L = K_V K_\phi A \pi$$

Where, $2\Delta f_L$ will be the lock in frequency range

The maximum range of signal frequencies over which the PLL can remain locked is

$$f_s = f_o \pm (f - f_o)_{\max} = f_o \pm \Delta f_L = f_o \pm K_V K_\phi A \frac{\pi}{2}$$

With respect to VCO free running frequency f_o the lock-in range is symmetrically located. For the 565 PLL IC,

$$K_V = \frac{8 f_o}{V} \qquad \text{where, } V = +V_{CC} - (-V_{CC})$$

$$K_\phi = \frac{1.4}{\pi} \text{ and } A = 1.4$$

Therefore, the lock in range is equal to

$$\Delta f_L = \pm K_V K_\phi A \frac{\pi}{2} = \pm \frac{8 f_o}{V} \times \frac{1.4}{\pi} \times 1.4 \times \frac{\pi}{2} = \pm 7.8 \frac{f_o}{V}$$

10.6.2 Derivation of Capture Range

When PLL is not initially locked to the signal, the frequency of voltage controlled oscillator will be free running frequency f_o. The phase angle difference between the signal and VCO output signal is equal to

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o)t + (\theta_s - \theta_o)$$

Or,
$$\phi = (\omega_s - \omega_o)t + \Delta\theta \quad \text{As } \Delta\theta = (\theta_s - \theta_o)$$

The phase angle difference is not remains constant but will change with time at a rate is given by

$$\frac{d\phi}{dt} = (\omega_s - \omega_o)$$

The phase detector output voltage will not have a dc component and it produce an ac voltage with a triangular waveform of peak amplitude K_ϕ and a fundamental frequency $f_s - f_o = \Delta f$.

The low pass filter which is used in a PLL circuit is a simple RC network. The low pass filter has the transfer function of

$$TF[jf] = \frac{1}{1 + j\frac{f}{f_1}}$$

Where $f_1 = \frac{1}{2\pi RC}$, i.e., 3dB point of low pass filter.

In the slope portion of LPF $\left(\frac{f}{f_1}\right)^2 >> 1$, then

$$TF[jf] \cong \frac{f_1}{jf}$$

When the fundamental frequency component is supplied to the low pass filter by the phase detector, the difference frequency will be

$$f_s - f_o = \Delta f$$

If $\Delta f > 3f_1$, the low pass filter transfer function will be

$$TF[\Delta f] = \frac{f_1}{\Delta f} = \frac{f_1}{f_s - f_o}$$

The control voltage V_C required to drive the voltage controlled oscillator is

$$V_C = V_e \times TF[f] \times A$$

Or,
$$V_{C(\max)} = V_{e(\max)} \times TF[f] \times A = \pm K_\phi \frac{\pi}{2} A \frac{f_1}{\Delta f}$$

Therefore, the corresponding value of the maximum VCO frequency shift is

$$(f - f_o)_{(\max)} = K_V V_{c(\max)} = \pm K_V K_\phi \frac{\pi}{2} A \frac{f_1}{\Delta f}$$

When $f = f_s$, the maximum signal frequency range that can be acquired by PLL is

$$(f_s - f_o)_{(\max)} = \pm K_V K_\phi \frac{\pi}{2} A \frac{f_1}{\Delta f_c}$$

Where, $\Delta f_c = (f_s - f_o)_{(\max)}$

Therefore, $(\Delta f_c)^2 = \pm K_V K_\phi \frac{\pi}{2} A f_1$

As $\Delta f_L = \pm K_V K_\phi \frac{\pi}{2} A$, $\Delta f_c = \pm \sqrt{f_1 \Delta f_L}$

Where the lock-in range is equal to $2\Delta f_L = \pm K_V K_\phi \pi A$

For the IC PLL 565, R = 3.6 kΩ, the capture range is given by

$\Delta f_c = \pm \left(\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times C} \right)$ where, C is in farads.

The capture range is symmetrically located with respect to voltage controlled oscillator free running frequency f_o as depicted in Fig. 10.17. The PLL can not able to acquire a signal outside the capture range. Once the signal is captured, it will hold on till the signal frequency goes beyond the lock-in range. To increase the ability of lock in range, large capture range is required. The large capture range will make the PLL more susceptible to noise and undesirable signal. Therefore a compromise is made between these two opposing requirements of the capture range.

Usually the pass filter bandwidth is first set for a large value for initial acquisition of signal. Once the signal is captured, the band width of low pass filter is reduced significantly. It will minimise the interference of undesirable noise and signals.

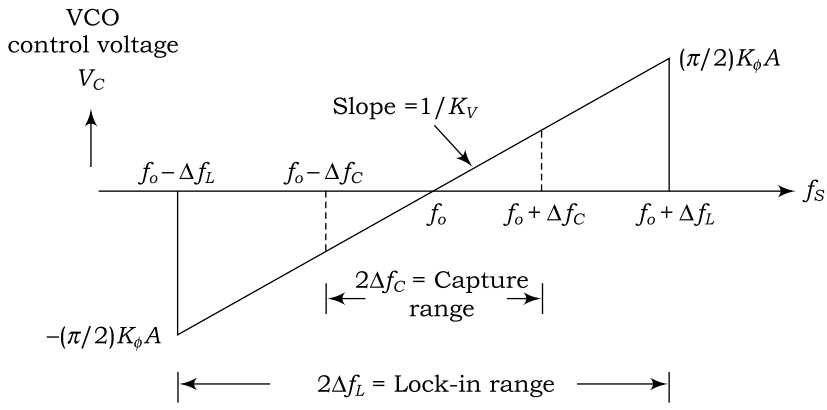


Fig. 10.17 Lock-in range and capture range of PLL

10.7 PLL APPLICATIONS

The output of a PLL system can be obtained as the voltage signal V_C corresponding to the error voltage in the feedback loop. The output of a PLL can also be a frequency signal at VCO output terminal. The voltage output of a PLL is used in frequency discriminator application. But the output frequency is used in signal conditioning, frequency synthesis and clock recovery applications.

While the output of a PLL system is voltage signal and PLL is locked to an input frequency, the error voltage V_C is directly proportional to $f_s - f_o$. When the input frequency is varied in FM signal, the voltage signal V_C will also vary in order to maintain the lock. Hence the voltage output can be used as a frequency discriminator which converts the changes in input frequency to voltage changes.

When the output of a PLL system is frequency signal and the input signal is consists of many frequency components degraded with noise and other disturbances, the PLL can be ready to lock, selectively on one particular frequency component at the input. Then the voltage controlled oscillator may regenerate that particular frequency and attenuate significantly other frequencies. Hence VCO output can be used for regenerating a desired frequency signal out of many undesirable frequency signals. PLL systems are most commonly used in frequency multiplication, frequency division, frequency translation, AM detection, FM detection and frequency shift keying (FSK) demodulator.

10.7.1 Frequency Multiplication

The block diagram of a frequency multiplier using PLL is shown in Fig. 10.18. A divide by N network or frequency divider is incorporated between the output signal of VCO and the phase comparator input. During the locked state, the VCO output frequency f_o is expressed by

$$f_o = Nf_s$$

Where, N is the scaling factor of the counter

Frequency multiplication can also be achieved by using PLL in its harmonic locking mode. When the input signal such as square wave and pulse train contains harmonics, the voltage controlled oscillator (VCO) can be directly locked to the n^{th} harmonic of the input signal without connecting any frequency divider in between.

Since the amplitude of the higher order harmonics becomes less, the effective locking may not take place for high value of n. Usually, the value of n is less than 10.

Figure 10.18 can also be used for frequency division. As the VCO output is rich in harmonics, it may be possible to lock the m^{th} harmonic of the VCO output with the input signal f_s. The output of VCO is expressed by

$$f_o = \frac{f_s}{m}$$

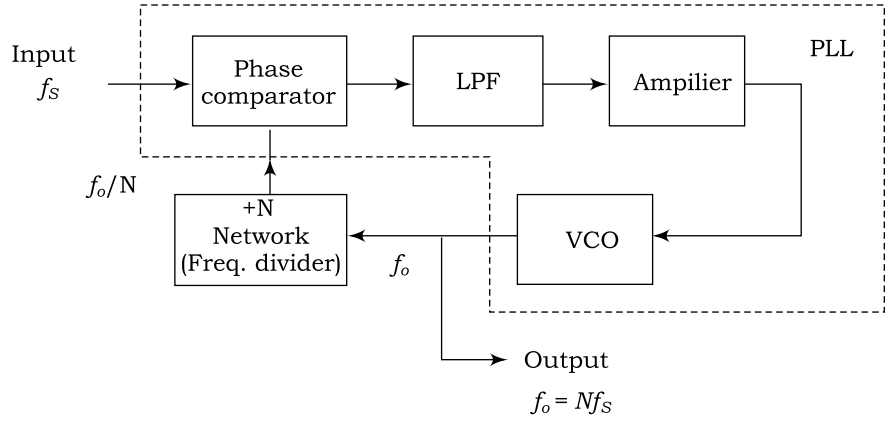


Fig. 10.18 Frequency multiplier using PLL

10.7.2 Frequency Translation

A schematic block diagram of frequency translator is shown in Fig. 10.19. The frequency translator is used for shifting the frequency of an oscillator by a small factor. It is clear from Fig. 10.19 that a mixer or multiplier and a low pass filter are connected externally to the PLL. The input signal f_s which may be shifted and the output frequency f_o of the VCO are applied as inputs to the mixer. The output of the mixer will be the sum and difference of f_s and f_o, i.e., $f_o + f_s$ and $f_o - f_s$. But the output of low pass filter (LPF) contains only the difference signal frequency $f_o - f_s$. Assume that the translation or offset frequency f_1 is applied to the phase comparator and $f_1 << f_s$. If the PLL is in locked state, the relationship between f_s, f_o and f_1 is

$$f_o - f_s = f_1$$

Therefore, $f_o = f_s + f_1$

Hence, it is possible to shift the incoming frequency signal f_s by f_1.

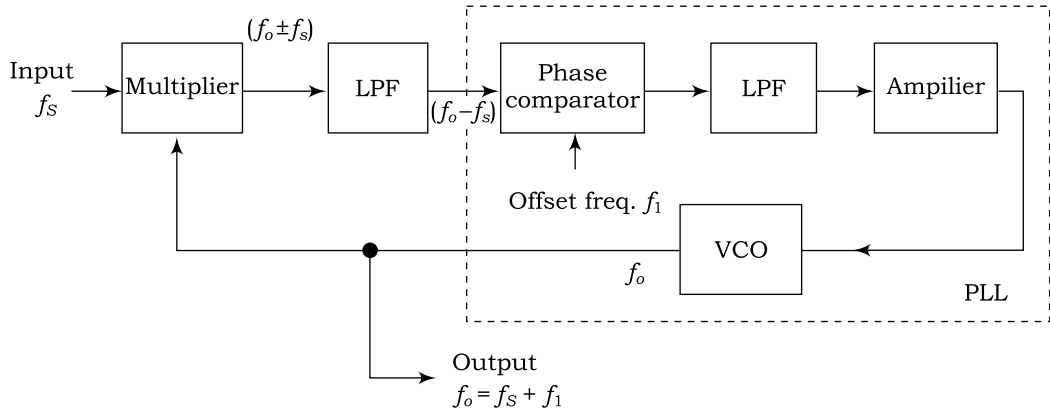


Fig. 10.19 Schematic block diagram of frequency translator

10.7.3 AM Detection

A PLL can be used to demodulate AM signals. Figure 10.20 shows the PLL used as AM demodulator. In this operating mode, the PLL is locked to the carrier frequency of the incoming AM signal and generates a reference signal at the VCO output. The output of VCO has the same frequency as the carrier and it is an un-modulated signal which is fed to the multiplier. Since the output signal of VCO is always 90° out of phase with the input AM signal under the locked condition, the AM input signal has to be shifted in phase by 90° before being fed to the multiplier as depicted in Fig. 10.20. Therefore, both the signals applied to the multiplier are in same phase. The output of multiplier has both the sum and the difference frequency signals and the demodulated output can be obtained after filtering high frequency components by the low pass filter. As the PLL responds only to the carrier frequencies which are very close to the voltage controlled oscillator (VCO) output frequency f_o, the phase-locked AM detector exhibits a high degree of selectivity centred at f_o. This PLL AM detector provides a high degree of noise immunity which is not possible with conventional peak detector type AM modulators used in conventional radio receivers.

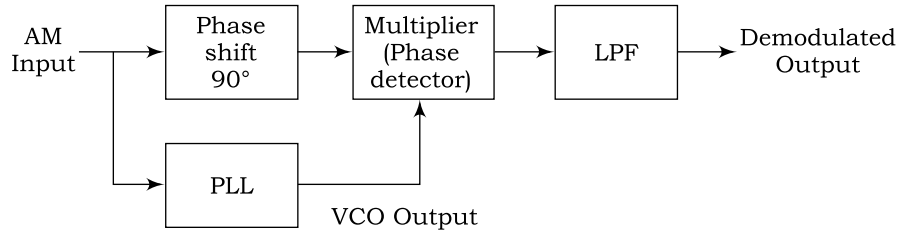


Fig. 10.20 PLL used as AM demodulator

10.7.4 FM Demodulation

The block diagram of FM detector is shown in Fig. 10.21. This PLL system cal also be used for FM demodulator. When the PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The VCO is controlled by the filtered error voltage. The error voltage also maintains lock with the input signal. The VCO transfer characteristics controls the linearity of the demodulated output. As VCO used in PLL IC is highly linear, it is possible to implement highly linear FM demodulators.

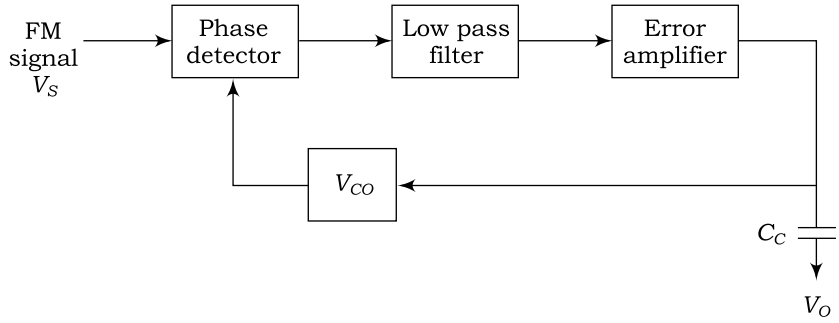


Fig. 10.21 Block diagram of FM detector

Review Exercises

Short-Answer Questions

1. What is pull in time of PLL?

Ans. Pull in time of a PLL is defined as the total time taken by the PLL to establish lock.

2. What are the function blocks of a PLL?

Ans. The function blocks of a PLL are phase comparator, low pass filter, error amplifier and voltage controlled oscillator.

3. Give a list of applications of a PLL.

Ans. The applications of PLL are

Frequency translation, Frequency division, Frequency multiplication, AM detection, FM detection and FSK demodulator.

4. What is the range of modulating input voltage applied to a voltage controlled oscillator?

Ans. The range of modulating input voltage applied to a voltage controlled oscillator is $0.75V_{CC}$ to V_{CC}.

5. What are the three different stages of operation in a PLL?

Ans. the three different stages of operation in a PLL are free running range, capture range, locked or tracking range.

6. What is lock-in range of PLL?

Ans. The range of frequency over which the PLL can maintain lock with the incoming signal is called the lock-in range.

7. What is capture range of PLL?

Ans. The range of frequency over which the PLL can acquire lock with an input signal is called capture range.

8. What are the different types of phase detectors?

Ans. There are two types of phase detectors such as analog phase detector and digital phase detector.

9. What will be the phase difference between the input signal and voltage controlled oscillator output to active lock?

Ans. The input signal and voltage controlled oscillator output should be 90° out of phase each other.

10. A PLL has free running frequency of 500kHz and bandwidth of the low pass filter is 10kHz. Will the loop acquire lock for an input signal of 600kHz? Justify the answer. Assume that the phase detector produces sum and difference frequency components.

Ans. The phase detector output is

$f_s + f_o$ = 600 kHz + 500 kHz = 1100 kHz

$f_s - f_o$ = 600 kHz – 500 kHz = 100 kHz

Since both the frequency components are outside the pass band of low pass filter, the PLL will not acquire lock.

11. What is low pass filter?

Ans. A low pass filter is a RC network which passes all frequencies from zero to cutoff frequency.

12. What is the need for a low pass filter in a PLL?

Ans. When the loop is trying to achieve lock, the output of the phase detector contains frequency components at the sum and difference of signals. A low pass filter exists in a PLL to pass only the low-frequency component of the signal so that the loop can obtain lock between input and VCO signals. The low pass filter can able to remove high frequency signals.

Multiple-Choice Questions

1. A PLL consists of
   (a) Comparator (b) Low Pass Filter (c) VCO (d) All of these
2. IC NE/SE 566 is a
   (a) Voltage controlled oscillator
   (b) Schmitt Trigger
   (c) IF Amplifier
   (d) Video Amplifier
3. A device whose frequency is changed by a variable dc voltage is known as
   (a) Crystal Oscillator
   (b) Error detector
   (c) Voltage Controlled Oscillator
   (d) Power amplifier
4. If the control voltage is V_C, the VCO output frequency is directly proportional to
   (a) V_C (b) $\frac{1}{V_C}$ (c) V_C^2 (d) $\sqrt{V_C}$
5. An application of _____ is FSK demodulation
   (a) LPF (b) PLL (c) BPF (d) Timer
6. The first stage in a PLL is _____ followed by _____
   (a) comparator, low pass filter
   (b) low pass filter, comparator
   (c) phase detector, low pass filter
   (d) VCO, low pass filter
7. The lock-in range in a PLL is always _____ capture range
   (a) less than (b) greater than
   (c) equal to (d) greater than and equal to
8. Frequency multiplication is an important application of _____
   (a) 565 IC (b) 555 IC (c) 741 IC (d) 7490 IC
9. Application of PLL is
   (a) Frequency multiplication (b) Frequency division
   (c) Frequency translation (d) All of these

Review Questions

1. Draw the block diagram of a PLL? Explain the working principle of PLL.
2. List the building blocks of a PLL.
3. Define pull-in time, capture range and lock range.
4. List the applications of a PLL.
5. Which is greater “capture range” or “Lock range”?
6. Explain how can you obtain frequency multiplier using 565 PLL?
7. Draw the circuit diagram of a PLL AM detector and explain its operation.

8. Write short notes on the following:
   (a) Voltage controlled oscillator (VCO)
   (b) Voltage to frequency converter
   (c) PLL

ANSWERS

Multiple-Choice Questions

1. (d) 2. (a) 3. (c) 4. (b) 5. (b)
6. (a) 7. (a) 8. (a) 9. (d)

Solution of 2011 WBUT Paper (EC304)

Group A

(Multiple-Choice Type Questions)

1. Choose the correct alternatives for any ten of the following: $10 \times 1 = 10$

(i) In active region of a BJT the emitter junction is in _____ bias and collector junction is _____ bias.

(a) forward, reverse (b) forward, forward

(c) reverse, forward (d) reverse, reverse

Ans. (a) forward, reverse

(ii) The maximum theoretical efficiency of a class B push-pull transistor amplifier is approximately

(a) 25% (b) 50% (c) 70.7% (d) 78.5%

Ans. (d) 78.5%

(iii) The type of power amplifier which exhibits cross-over distortion in its output is

(a) class A (b) class B (c) class C (d) class AB

Ans. (b) class B

(iv) An amplifier without feedback has a voltage gain of 50, input resistance of 1 kΩ and output resistance of 2.5 kΩ. The input resistance of the current-shunt negative feedback amplifier using the above amplifier with a feedback factor of 0.2 is

(a) $\frac{1}{11}$ kΩ (b) $\frac{1}{5}$ kΩ (c) 5 kΩ (d) 11 kΩ

Ans. (a) $\frac{1}{11}$ kΩ

(v) In the analysis of a power amplifier, we prefer

(a) equivalent circuit analysis

(b) graphical method using load line

(c) equivalent circuit analysis and graphical methods using load line

(d) None of these

Ans. (b) graphical method using load line

(vi) A instrumentation amplifier

(a) is a differential amplifier (b) has a gain less than 1

(c) has very high output impedance (d) has low CMRR

Ans. (a) is a differential amplifier

(vii) Which one of the following oscillator is used for the generation of high frequencies?

(a) R-C phase shift (b) Blocking oscillator

(c) Wien bridge (d) LC oscillator

Ans. (d) LC oscillator

(viii) Operational amplifiers are used to amplify

(a) ac signals only (b) dc signals only

(c) both ac and dc signals (d) None of these

Ans. (c) both ac and dc signals

(ix) An ideal regulated power supply should have regulation which

(a) maximum (b) 50% (c) zero (d) 75%

Ans. (c) zero

(x) A Class B push-pull amplifier has an ac output of 10 W. The dc power drum from the power supply under ideal condition is

(a) 10 W (b) 12.5 W (c) 15 W (d) 20 W

Ans. (b) 12.5 Watts

(xi) The output voltage of IC7915 is

(a) 15V (b) –15V (c) 5V (d) –5V

Ans. (b) –15V

(xii) The Schmitt trigger is also known as

(a) squiring circuit (b) blocking oscillator

(c) sweep circuit (d) astable multivibrator

Ans. (b) blocking oscillator

Group B

(Short Answer Type Questions)

Answer any three of the following: $3 \times 5 = 15$

1. With a neat diagram, explain the principle of operation of an antilog amplifier.

Ans. Refer to Sections 7.14 and 7.15

2. Explain the operation of transformer coupled class-A power amplifier.

Ans. Refer to Section 8.4

3. Sketch the circuit of Wein-bridge oscillator. Explain the principle of operation and find an expression for the frequency of oscillation.

Ans. Refer to Section 5.9

4. A phase shift oscillator using a transistor has the following parameter values:
R_L = 3.3 kΩ, R = 5.6 kΩ, C = 0.01 μF. Calculate the frequency of oscillators and h_{fe} required for operation of an amplifier.

Ans. Given: R_L = 3.3 kΩ, R = 5.6 kΩ and C = 0.01 μF

$$K = \frac{R_L}{R} = \frac{3.3\ \text{k}\Omega}{5.6\ \text{k}\Omega} = 0.5982$$

The frequency of oscillator is $f = \dfrac{1}{2\pi RC\sqrt{6+4K}}$

$$= \frac{1}{2\pi \times 5.6 \times 10^3 \times 0.01 \times 10^{-6}\sqrt{6+4\times 0.5982}}$$

$$= 980.63\ \text{Hz}$$

h_{fe} required for operation of an amplifier is

$$h_{fe} = 23 + 29\frac{R}{R_L} + 4\frac{R_L}{R}$$

$$= 23 + 29\frac{5.6k\Omega}{3.3k\Omega} + 4\frac{3.3k\Omega}{5.6k\Omega} = 74.569$$

5. (a) What are the differences between series and shunt regulator?

Ans. The differences between series and shunt regulator are given in Table 1.

Table 1

Series regulator	*Shunt regulator*
In a transistor series regulator, the output voltage V_O is the difference of zener voltage V_Z and the base emitter voltage V_{BE} i.e. $V_O = V_Z - V_{BE}$	In a transistor shunt regulator, the output voltage V_O is the sum of zener voltage V_Z and the base emitter voltage V_{BE}, i.e., $V_O = V_Z + V_{BE}$
In a transistor series regulator, transistor is connected in series with the load.	In a transistor shunt regulator, transistor is connected in parallel with the load.

(b) Draw a circuit diagram of a shunt regulator and explain its operation.

Ans. Refer to Section 1.10

Group C

(Long-Answer Type Questions)

Answer any three of the following: $3 \times 15 = 45$

6. (a) Explain the need for biasing of a transistor.

Ans. Refer to Section 2.10

(b) Mention different schemes for biasing a transistor.

Ans. Refer to Section 2.14

(c) Compare their merits and demerits.

Ans. The *fixed bias configuration* is the most simplest of transistor biasing arrangement, but it is quite unstable due to its sensitivity to β at the operating point. The stability factor S for a CE circuit using fixed bias is $S = (\beta + 1)$. This method provides poor stability, as there is no means to stop a self-increase in collector current I_C owing to temperature rise. There are good chances of thermal runway due to high stability factor.

The *voltage divider bias* circuit is the most commonly used biasing arrangement. It is very popular due to its low sensitivity to variation in β from one transistor to another. The stability factor of voltage divider is less than $(\beta + 1)$. The voltage divider biasing circuit has better stability compared to fixed bias circuit.

From the stability point of view, the emitter bias circuit is the best biasing circuit, but it has one drawback that it requires two power supplies.

(d) Define stability factors.

Ans. Refer to Section 2.13

(e) Explain the self biasing arrangement of the transistor.

Ans. Refer to Section 2.16

8. (a) Draw the functional block diagram of 555 timer.

Ans. Refer to Section 9.9

(b) Explain the operation of astable multivibrator using 555 timer. Derive the expressions for frequency in case of the output waveform.

Ans. Refer to Section 9.9.1

(c) How can you modify the above circuit for 50% duty cycle?

Ans. When a diode D is connected across resistance R_2, the charging time of capacitor $T_1 = 0.693\, R_1 C$ and the discharging time of capacitor $T_2 = 0.693 R_2 C$.

For 50% duty cycle,

$$T_1 = 0.693 R_1 C \;=\; T_2 = 0.693 R_2 C\,.$$

Therefore, if $R_1 = R_2$ and diode D is connected across resistance R_2, duty cycle of output voltage wave from is 50%.

9. (a) Derive the maximum efficiency of a class B push-pull amplifier.

Ans. Refer to Sections 8.9 and 8.11

What is the major drawback of class B operation and how it can be avoided?

Ans. Refer to Section 8.10

(b) Explain the importance of $P_{C,\,\max}$ in designing the power amplifier.

Ans. The maximum power dissipation capability with the zero input signal conditions in a transistor is the power rating of the transistor. The relation between $P_{C,\,\max}$ and $P_{\text{Dissipation, max}}$ is $P_{C,\,\max} = \dfrac{P_{\text{Dissipation,max}}}{2}$. Hence the power rating of the transistor is twice than the maximum ac output power $P_{C,\,\max}$. During design of a power amplifier, the maximum ac output power $P_{C,\,\max}$ should be half of the power rating of transistor.

(c) What is the function of tuned amplifier?

Ans. Refer to Section 8.13

(d) A transformer coupled class A power amplifier has maximum and minimum values of collector-emitter voltage of 25V and 2.5V respectively. Determine its collector efficiency.

Ans. Given: $V_{CE\max} = 25$ V and $V_{CE\min} = 2.5$ V

Collector efficiency of a transformer coupled class A power amplifier is

$$\eta = 25\frac{V_{CE\max} - V_{CE\min}}{V_{CC}}\%$$

$$= 25\frac{25 - 2.5}{25}\% = 22.5\%$$

10. (a) What are the characteristics of an ideal op-amp?

Ans. Refer to Section 6.2

(b) Describe the functions of an op-amp:

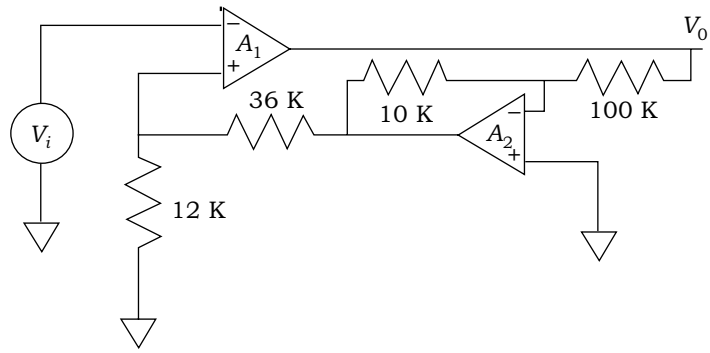
(i) adder

Ans. Refer Section 7.5

(ii) integrator

Ans. Refer to Section 7.11

(c) Determine the value of the voltage gain $\frac{V_o}{V_i}$ for the following circuit:



Ans. KCL equation at Node A is

$$\frac{V_A}{12} = \frac{V_A - V_B}{36}$$

Since $V_A = V_i$, we get $\frac{V_i}{12} = \frac{V_i - V_B}{36}$

KCL equation at Node B is

$$\frac{V_A - V_B}{36} = \frac{V_B - 0}{10}$$

or, $$\frac{V_i - V_B}{36} = \frac{V_B}{10} \text{ or, } \frac{V_i}{36} = \frac{V_B}{10} + \frac{V_B}{36}$$

or, $$V_i = \frac{36}{10}V_B + V_B = 4.6V_B$$

KCL equation at Node C is

$$\frac{V_B - 0}{10} = \frac{V_O - 0}{100}$$

or, $$V_B = 10V_O$$

Since $$V_i = 4.6V_B\,,\ V_B = 10V_O = \frac{V_i}{4.6}$$

Therefore, $$\frac{V_o}{V_i} = \frac{1}{46}$$

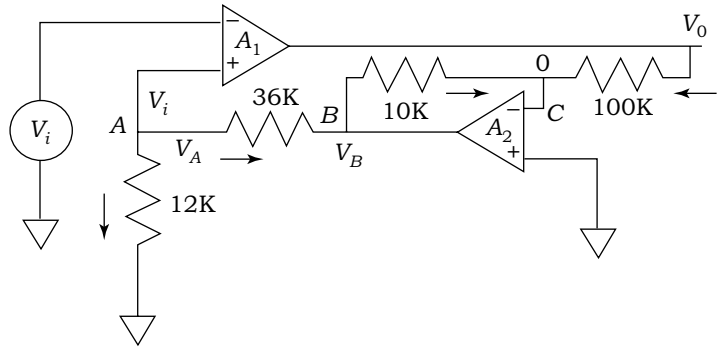


Fig. 1

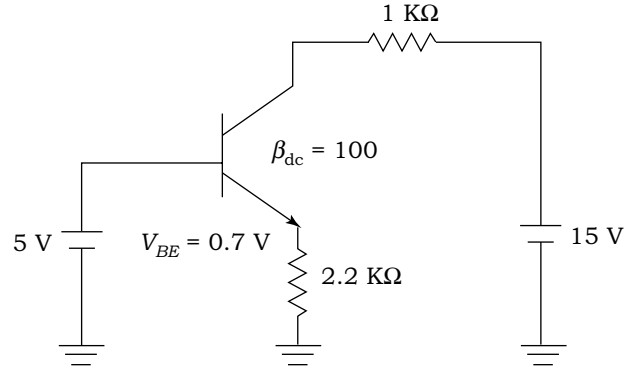
(d) Explain logarithmic amplifier with circuit diagram.

Ans. Refer to Section 7.13

11. (a) Explain quiescent point and load line of a transistor amplifier.

Ans. Refer to Section 2.11

Find the *Q* point of the given emitter bias circuit.



Ans. The KVL equation in the base emitter circuit is

$$5 = V_{BE} + I_E R_E$$

As $I_E = (1+\beta) I_B, V_{BE} = 0.7 \text{ V}$ and $R_E = 2.2 \text{ k}\Omega$, we get

$$5 = V_{BE} + I_E R_E = 0.7 + (1+\beta) I_B R_E$$

or, $$5 = 0.7 + (1+100) I_B \times 2.2 \times 10^3$$

$$I_B = \frac{5 - 0.7}{101 \times 2.2 \times 10^3} = 0.01935 \text{ mA}$$

The KVL equation in the collector emitter circuit is

$$15 = I_C R_C + V_{CE} + I_E R_E \qquad I_C = \beta I_B \quad \text{and} \quad R_C = 1 \text{ k}\Omega$$

or, $$15 = \beta I_B R_C + V_{CE} + (1+\beta) I_B R_E$$

or, $$15 = 100 \times 0.01935 \times 10^{-3} \times 1 \times 10^3 + V_{CE} + (1+100) \times 0.01935 \times 2.2 \times 10^3$$

or, $$15 = 1.935 + V_{CE} + 4.299$$

or, $$V_{CE} = 8.766$$

$$I_C = \beta I_B = 100 \times 0.01935 \text{ mA} = 1.935 \text{ mA}$$

The Q point of the given emitter bias circuit is $(V_{CE}, I_C) = (8.766 \text{ V}, 1.935 \text{ mA})$

(b) Define hybrid parameters for basic transistor circuit in common emitter configuration and give its hybrid model.

Ans. Refer to Section 2.19.2

12. Write short notes on any three of the following:

(a) Switched mode power supply

Ans. Refer to Section 1.12

(b) RC phase shift oscillator

Ans. Refer to Section 5.7

(c) Voltage controlled oscillator

Ans. Refer to Section 10.4

(d) Phase locked loop

Ans. Refer to Sections 10.1 and 10.2

(e) Wave shaper

Ans. A *triangular waveform* can be generated by integrating a square waveform. The figure below shows a triangular waveform generator which consists of a square-wave generator and an integrator. The amplitude of the square-wave swings between $+V_{\text{sat}}$ $(+V_{CC})$ and $-V_{\text{sat}}$ $(-V_{CC})$. The time period and frequency of a triangular wave is same as the time period and frequency of square wave. The peak-to-peak value of the triangular wave is $V_{\text{peak-to-peak}} = \frac{V_{\text{in}}}{4 f R_5 C_2}$.

The output waveform of integrator is triangular when $5R_4C_2 > \frac{T}{2}$ where, T is time period of square wave and resistance R_5 must be equal to $10R_4$.

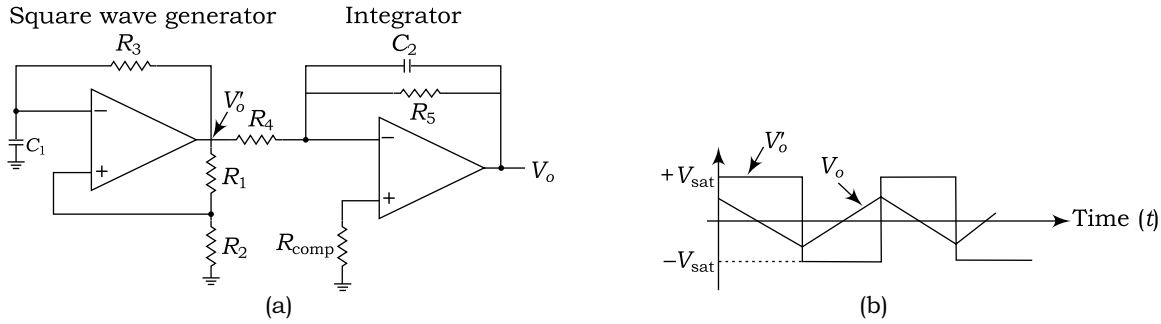


Fig. 2 (a) Triangular wave generator (b) Output waveform

Figure 3 shows another *triangular waveform generator* using less number of components. Actually, this circuit consists of a two-level comparator followed by an integrator. The output of the comparator is a square wave whose amplitude swings between $+V_{sat}$ and $-V_{sat}$. When the generated square wave is applied to the inverting input terminal of an integrator, a triangular wave is generated. Then this triangular wave is fed back as input to the comparator through a potential divider $R_1 - R_2$.

At $t = t_0$, the output of the comparator is $+V_{sat}$, the integrator output will be a negative-going ramp as depicted in Fig. 3(b). In this time, one end of the potential divider is $+V_{sat}$ and the other end is at the negative-going ramp. The output voltage at A is equal to

$$V_A = -V_{ramp} + \frac{R_1}{R_1 + R_2}[+V_{sat} - (-V_{ramp})] \tag{1}$$

At $t = t_1$, the negative-going ramp reaches the negative peak value of ramp, $-V_{ramp}$ and the voltage at the point A is slightly less than 0 V. Then the comparator output changes from positive saturation $+V_{sat}$ to negative saturation $-V_{sat}$ and the integrator output will be a positive-going ramp. As $V_A = 0$, we can write

$$0 = -V_{ramp} + \frac{R_1}{R_1 + R_2}[+V_{sat} - (-V_{ramp})]$$

or
$$-V_{ramp} = -\frac{R_1}{R_2}(+V_{sat}) = -\frac{R_1}{R_2}V_{sat} \tag{2}$$

At $t = t_2$, the positive-going ramp reaches the positive peak value of the ramp, $+V_{ramp}$ and the voltage at the point A is just greater than 0 V. Subsequently, the comparator output changes from negative saturation $-V_{sat}$ to positive saturation $+V_{sat}$ and again the integrator output will be a positive-going ramp. After that, the cycle repeats and generates a triangular wave.

As $V_A = 0$, $+V_{ramp} = -\frac{R_1}{R_2}(-V_{sat}) = \frac{R_1}{R_2}V_{sat}$.

The peak-to-peak amplitude of triangular wave is $V_{peak\text{-}peak} = +V_{ramp} - (-V_{ramp}) = 2\frac{R_1}{R_2}V_{sat}$

As the integrator output varies from $-V_{ramp}$ to $+V_{ramp}$ within half of the time period $\left(\frac{T}{2}\right)$, the integrator output is equal to

$$V_{\text{peak-peak}} = -\frac{1}{RC}\int_0^{T/2}(-V_{\text{sat}})dt = \frac{V_{\text{sat}}}{RC}\frac{T}{2}$$

As $V_{\text{peak-peak}} = 2\frac{R_1}{R_2}V_{\text{sat}}$, we obtain $\frac{V_{\text{sat}}}{RC}\frac{T}{2} = 2\frac{R_1}{R_2}V_{\text{sat}}$. (3)

Then time period T is equal to $T = \frac{4RCR_1}{R_2}$ and frequency is $f = \frac{1}{T} = \frac{R_2}{4RCR_1}$

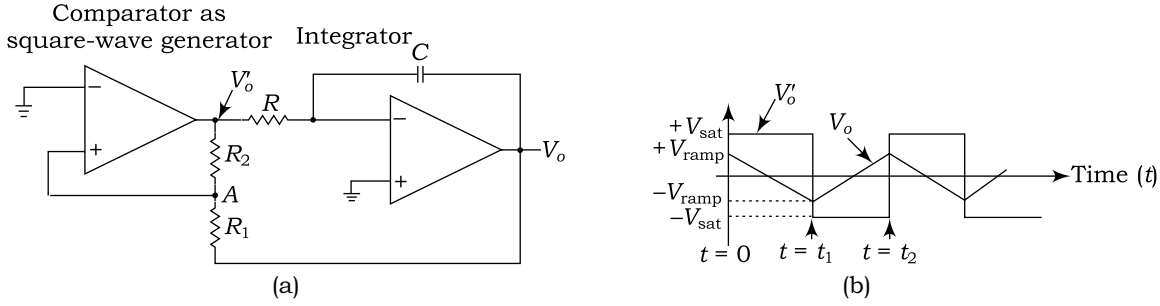


Fig. 3 (a) Triangular wave generator using comparator (b) Output waveform

(f) Colpitts oscillators

Ans. Refer to Section 5.11.1

Solution of 2012 WBUT Paper (EC304)

Group A

Multiple-Choice Type Questions

1. Choose the correct alternatives for any ten of the following: $10 \times 1 = 10$

(i) An instrumentation amplifier has a high

(a) supply voltage (b) power gain (c) CMRR (d) output impedance

Ans. (c) CMRR

(ii) A transistor is said to be quiescent state when

(a) no signal is applied to the input

(b) no currents are following

(c) it is unbiased

(d) emitter junction and collector junction biased are equal

Ans. (a) no signal is applied to the input

(iii) If three cascaded stages of amplifier have gains 10, 20, 30 the overall gain will be

(a) 200 (b) 400 (c) 1200 (d) 6000

Ans. (d) 6000

(iv) Which of the following configuration can be used as buffer?

(a) CE (b) CB (c) CC (d) All of these

Ans. (c) CC

(v) An astable multivibrator generates

(a) triangular waveform (b) sinusoidal waveform

(c) square waveform (d) None of these

Ans. (c) square waveform

(vi) For phase locked loop

(a) capture range is greater than lock range (b) capture range is less than lock range

(c) capture range is equal to lock range (d) no relationship between them

Ans. (b) capture range is less than lock range

(vii) The output impedance of an OP-AMP is

(a) medium (b) very low (c) very high

Ans. (b) very low

(viii) CMRR for an Op-AMP should be

(a) as small as possible (b) closed to unity

(c) close to zero (d) as large as possible

Ans. (d) as large as possible

(ix) In an active RC filter, the active element is

(a) the resistance R (b) the capacitor C (c) the Op-Amp (d) None of these

Ans. (c) the Op-Amp

(x) An ideal regulated power supply should have regulation which is

(a) maximum (b) 50% (c) zero (d) 75%

Ans. (c) zero

Group B

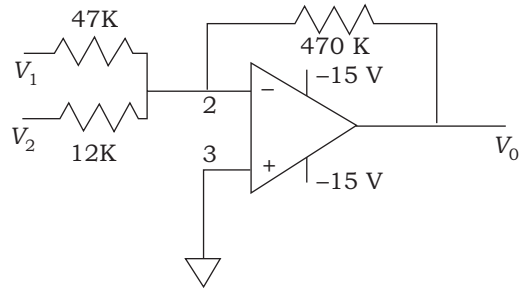
Short-Answer Type Questions

Answer any three of the following: $3 \times 5 = 15$

1. What is ripple? How it can be removed from the output of a rectifier? Explain with suitable diagram.

Ans. Refer to Sections 1.1 and 1.3

2. Calculate the output voltage of circuit shown below, where $V_1 = 40$ mV, $V_2 = 20$ mV



Given: $V_1 = 40$ mV, $V_2 = 20$ mV

The output voltage is $V_o = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$

$$= -\frac{470}{47} \times 40 \times 10^{-3} - \frac{470}{12} \times 20 \times 10^{-3} \text{ V}$$

$$= -1.1833\text{V}$$

3. Draw and explain the Schmitt trigger circuit using Op-Amp.

Ans. Refer to Section 7.19

4. Draw the circuit diagram of an emitter follower and state the nature of feedback in the circuit. Derive the expression of the voltage gain of the circuit from the concept of feedback.

Ans. Refer to Section 4.9.2

5. (a) What is regulated power supply?

Ans. Refer to Section 1.7

(b) Draw a series voltage regulator and explain its operation.

Ans. Refer to Section 1.11

GROUP C

Long-Answer Type Questions

Answer any three of the following: $3 \times 15 = 45$

1. (a) Sketch the circuit of Wein-bridge oscillator. Explain the principle of operation and find an expression for the frequency of oscillation.

Ans. Refer to Section 5.9

(b) Prove that the amplifier gain in a phase shift oscillator is at least 29 for sustained oscillation.

Ans. Refer to Section 5.6

(c) A phase shift oscillator using a transistor has the following parameter values:

$$R_L = 3.3\ \text{k}\Omega, \quad R = 5.6\ \text{k}\Omega \quad \text{and} \quad C = 0.01\ \mu\text{F}$$

Ans. Given: $R_L = 3.3\ \text{k}\Omega$, $R = 5.6\ \text{k}\Omega$ and $C = 0.01\ \mu\text{F}$

$$K = \frac{R_L}{R} = \frac{3.3\ \text{k}\Omega}{5.6\ \text{k}\Omega} = 0.5982$$

The frequency of oscillator is $f = \dfrac{1}{2\pi RC\sqrt{6 + 4K}}$

$$= \frac{1}{2\pi \times 5.6 \times 10^3 \times 0.01 \times 10^{-6}\sqrt{6 + 4 \times 0.5982}}$$

$$= 980.63\ \text{Hz}$$

h_{fe} required for operation of an amplifier is

$$h_{fe} = 23 + 29\frac{R}{R_L} + 4\frac{R_L}{R}$$

$$= 23 + 29\frac{5.6\ \text{k}\Omega}{3.3\ \text{k}\Omega} + 4\frac{3.3\ \text{k}\Omega}{5.6\ \text{k}\Omega} = 74.569$$

2. (a) What is the function of a voltage regulator?

Ans. Refer Section 1.7

(b) Draw and explain the operation of a series regulated power supply

Ans. Refer to Section 1.11

(c) Compare series and shunt regulated power supply.

Ans. The comparison between series and shunt regulated power supply are given in Table 1.

Table 1

Series regulator	*Shunt regulator*
In a transistor series regulator, the output voltage V_O is the difference of zener voltage V_Z and the base emitter voltage V_{BE} i.e. $V_O = V_Z - V_{BE}$	In a transistor shunt regulator, the output voltage V_O is the sum of zener voltage V_Z and the base emitter voltage V_{BE} i.e. $V_O = V_Z + V_{BE}$
In a transistor series regulator, transistor is connected in series with the load.	In a transistor shunt regulator, transistor is connected in parallel with the load.

(d) Calculate the ripple factor of a rectifier using capacitor filter with figure.

Ans. Refer to Section 1.3

3. (a) What is meant by Thermal runway? How it can be avoided?

Ans. Refer to Section 2.30.4

(b) Draw and explain self-bias circuit of an NPN transistor in CE configuration.

Ans. Refer to Section 2.16

(c) Derive an expression for the stability factor $S = \dfrac{\partial I_C}{\partial I_{Co}}$ for self-bias circuit.

Ans. Refer to Section 2.16

4. (a) Explain the operation of a transformer coupled class A power amplifier.

Ans. Refer to Section 8.4

(b) What is the cross-over distortion found in a class B amplifier? How it can be avoided?

Sol Refer to Section 8.10

(c) In which respect class B push-pull amplifier is better than a class A amplifier?

Ans. Refer to Section 8.9

5. Write short notes on any three of the following:

(a) Schmitt trigger

Ans. Refer to Section 7.19

(b) High frequency model of transistors

Ans. Refer to Section 2.29

(c) Hartley oscillator

Ans. Refer to Section 5.11.2

(d) Four basic feedback topologies

Ans. Refer to Section 4.5

(e) SMPS

Ans. Refer to Section 1.12

(f) Current mirror

Ans. Refer to Section 6.9

Solution of 2012 WBUT Paper (EC(EE)301)

Group A

Multiple-Choice Type Questions

1. Choose the correct alternatives for any ten of the following: $10 \times 1 = 10$

(i) An ideal regulated power supply should have regulation which is

(a) maximum (b) 50% (c) zero (d) 75%

Ans. (c) zero

(ii) Thermal runway in a transistor is due to

(a) heating of the transistor

(b) changes in β which increases with temperature

(c) increase in reverse collector saturation current due to rise in temperature

(d) None of these

Ans. (c) increase in reverse collector saturation current due to rise in temperature

(iii) In amplifier blocking capacitors are used

(a) to increase the bandwidth (b) to match the impedance

(c) to increase the gain (d) to avoid dc mixing with input or output

Ans. (d) to avoid dc mixing with input or output

(iv) The condition of oscillator

(a) $A\beta = 1$

(b) Feedback must be regenerate

(c) phase angle must be zero or integral multiple of 360°

(d) All of these

Ans. (d) All of these

(v) The expression of closed loop gain A_f for negative feedback amplifier is

(a) $\frac{A}{1 + A\beta}$ (b) $\frac{A}{1 - A\beta}$ (c) $\frac{1}{1 + A\beta}$ (d) $\frac{1}{1 - A\beta}$

Ans. (a) $\frac{A}{1 + A\beta}$

(vi) A Schmitt trigger uses
(a) Negative feedback (b) Positive feedback
(c) Pull up resistor (d) Compensating capacitor
Ans. (b) Positive feedback

(vii) Differential amplifier can be used to amplify
(a) only ac signal (b) only dc signal
(c) both ac and dc signal (d) None of these
Ans. (c) both ac and dc signals

(viii) Most efficient power amplifier is
(a) Class A (b) Class B (c) Class C (d) Class AB
Ans. (c) Class C

(ix) The maximum theoretical efficiency of a push-pull class B power amplifier
(a) 50% (b) 78.5% (c) 60% (d) 25%
Ans. (b) 78.5%

(x) Which one of the following feedback topologies offer high input impedance?
(a) Voltage series (b) Voltage shunt (c) Current series (d) Current shunt
Ans. (c) Current series

(xi) In the astable multivibrator the capacitor charges up to
(a) $\frac{1}{3}V_{CC}$ (b) $\frac{2}{3}V_{CC}$ (c) V_{CC} (d) None of these
Ans. (b) $\frac{2}{3}V_{CC}$

(xii) In VCO, the frequency is dependent on the value of
(a) Resistance (b) Capacitance (c) Voltage (d) None of these
Ans. (c) Voltage

Group B

Short-Answer Type Questions

Answer any three of the following: $3 \times 5 = 15$

1. (a) Explain the need of biasing of a transistor.

Ans. Refer to Section 2.10

(b) Draw any one type of transistor biasing arrangement and determine its stability factor.

Ans. Refer to Section 2.15

2. Draw the *h*- parameter equivalent circuit of low frequency CE mode transistor amplifier and hence calculate the current gain in terms of *h*- parameters.

Ans. Refer to Sections 2.19.2 and 2.20

3. What is VCO? What are the basic differences between VCO and fixed frequency oscillator?

Ans. Refer to Section 10.4

The basic differences between VCO and fixed frequency oscillator is given in Table 1.

Table 1

Voltage Controlled Oscilator	*Fixed Frequency Oscillator*
A voltage controlled oscillator is a circuit which generates a varying output signal (square wave or triangular wave) whose frequency can be adjusted over a range controlled by a dc voltage.	A fixed frequency oscillator is a circuit which generates a output signal (square wave or triangular wave) at fixed frequency.
The voltage controlled oscillator can be programmed over a 10 to 1 frequency range by proper selection of an external resistor and capacitor and then modulated over a 10 to 1 frequency range by a control voltage, V_C.	The frequency of fixed frequency oscillator can be set by external resistor and capacitor. It does not depend on applied voltage.

4. What is cross-over distortion? How does cross-over distortion arise in class B power amplifier? Suggest one method to avoid cross-over distortion.

Ans. Refer to Section 8.10

5. Draw the electrical equivalent circuit of a vibrating crystal and state the significance of each component. What are f_s and f_p?

Ans. Refer to Section 5.12

GROUP C

Long-Answer Type Questions

Answer any three of the following: $3 \times 15 = 45$

1. (a) Describe the working principle of π– filter with diagram.

Ans. Refer to Section 1.5

(b) Draw the current of shunt regulator and explain its operation.

Ans. Refer to Section 1.10

(c) What are the merits of switched mode power supply (SMPS) over regulated power supply? With the help of a neat circuit diagram briefly explain the operation of switched mode power supply.

Ans. Refer to Section 1.12

2. (a) Why voltage divider bias circuit is known as self-bias circuit?

Ans. Refer to Section 2.16

A silicon transistor with $\beta = 50$, $V_{BE} = 0.6$V, $V_{CC} = 22.5$V and $R_C = 5.6$ kΩ is used for self-biasing circuit. It is desired to establish a Q point at $V_{CE} = 12$V, $I_C = 1.5$ mA and a stability factor $S \leq 3$. Find $R_E = R_1$ and R_2.

(The symbols have their usual meanings)

Ans. Given: $\beta = 50$, $V_{BE} = 0.6$V, $V_{CC} = 22.5$V, $R_C = 5.6$ kΩ, $V_{CE} = 12$V, $I_C = 1.5$ mA and $S \leq 3$.

The emitter current is $I_E = \dfrac{1+\beta}{\beta} I_C = \dfrac{1+50}{50} \times 1.5 = 1.53$ mA

We know that $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

or, $$R_E = \frac{V_{CC} - V_{CE} - I_C R_C}{I_E} = \frac{22.5 - 12 - 1.5 \times 5.6}{1.53 \times 10^{-3}} = 1.372 \text{ k}\Omega$$

The stability factor is

$$S = \frac{1 + \beta}{1 + \beta \dfrac{R_E}{R_E + R_B}}$$

or, $$1 + \beta \frac{R_E}{R_E + R_B} = \frac{1 + \beta}{S}$$

or, $$\beta \frac{R_E}{R_E + R_B} = \frac{1 + \beta}{S} - 1 = \frac{1 + 50}{3} - 1 = 16$$

or, $$\frac{R_E}{R_E + R_B} = \frac{16}{\beta} = \frac{16}{50} = 0.32$$

Therefore, $R_E = 0.32 R_E + 0.32 R_B$

or, $$R_B = \frac{1 - 0.32}{0.32} R_E = 2.125 R_E = 2.125 \times 1.372 \text{ k}\Omega = 2.9155 \text{ k}\Omega$$

For good voltage stabilizer, $R_2 = 0.1 \beta R_E = 0.1 \times 50 \times 1.372 \text{ k}\Omega = 6.86 \text{ k}\Omega$

We know that, $R_B = R_1 \| R_2 = \dfrac{R_1 R_2}{R_1 + R_2}$

or, $$R_1 R_B + R_2 R_B = R_1 R_2$$

or, $$R_1 (R_B - R_2) = - R_2 R_B$$

or, $$R_1 = \frac{R_2 R_B}{R_2 - R_B} = \frac{6.86 \times 2.9155}{6.86 - 2.9155} = 5.070 \text{ k}\Omega$$

(b) Find the upper cut-off frequency of a two stage common-emitter RC coupled amplifier.

Ans. The upper cut-off frequency f_2 is the frequency at which the magnitude of the voltage gain in the high frequency range falls off to 0.707 times the magnitude of the gain in the mid frequency range.

At $$f = f_2, \quad A_{\text{vh}} = \frac{1}{\sqrt{2}} A_{\text{vm}} = 0.707 A_{\text{vm}}$$

The value of A_{vh} is equal to

$$A_{\text{vh}} = \frac{h_{fe} R_C}{(h_{ie} + R_C) \left[1 + \left(\dfrac{2\pi f C_d h_{ie} R_C}{h_{ie} + R_C} \right)^2 \right]^{1/2}}$$

$$A_{vm} = \frac{h_{fe} R_C}{h_{ie} + R_C}$$

Using above two equations, we obtain

$$\frac{A_{vh}}{A_{vm}} = \frac{1}{\left[1+\left(\frac{2\pi f C_d h_{ie} R_C}{h_{ie}+R_C}\right)^2\right]^{1/2}}$$

When the upper cut-off frequency is f_2

$$\frac{A_{\text{vh}}}{A_{\text{vm}}} = 0.707 = \frac{1}{\left[1+\left(\frac{2\pi f_2 C_d h_{ie} R_C}{h_{ie}+R_C}\right)^2\right]^{1/2}}$$

or, $$\frac{2\pi f_2 C_d h_{ie} R_C}{h_{ie}+R_C} = 1$$

The upper cut-off frequency is

$$f_2 = \frac{h_{ie}+R_C}{2\pi C_d h_{ie} R_C} = \frac{1}{2\pi C_d}\left(\frac{1}{h_{ie}}+\frac{1}{R_C}\right)$$

(c) A two stage common-emitter RC coupled amplifier uses transistor of the type BC 149 C of which the h parameters and the internal capacitances are $h_{fe} = 600$, $h_{ie} = 10\ \text{k}\Omega$, $C_{bc} = 2.5\ \text{pF}$, $C_{be} = 9\text{pF}$. If the coupling capacitor is $0.5\ \mu\text{F}$ and the load resistance is $10\ \text{k}\Omega$. Find the upper cut-off frequency and its gain.

Ans. Given: $h_{fe} = 600, h_{ie} = 10\ \text{k}\Omega, C_{bc} = 2.5\ \text{pF}, C_{be} = 9\ \text{pF}\ C_C = 0.5\ \mu\text{F}$ and $R_L = 10\ \text{k}\Omega$

Gain is $A_m = \frac{h_{fe} R_C}{h_{ie}+R_C} = \frac{600 \times 10 \times 10^3}{10 \times 10^3 + 10 \times 10^3} = 300$

$$C_d = C_{bc} + (1 - A_m)C_{be} = 2.5\ \text{pF} + (1-(-300)) \times 9\ \text{pF} = 2706.5\ \text{pF}$$

The upper cut-off frequency is

$$f_2 = \frac{1}{2\pi C_d}\left(\frac{1}{h_{ie}}+\frac{1}{R_C}\right) = \frac{1}{2\pi \times 2706.5 \times 10^{-12}}\left(\frac{1}{10 \times 10^3}+\frac{1}{10 \times 10^3}\right) = 11.756\ \text{kHz}$$

3. (a) Give the circuit of Colpitt's oscillator and explain its operation. Derive the condition for sustained oscillation and the expression for the frequency of oscillation of it.

Ans. Refer to Section 5.11.1

(b) What is the difference between Hartley and Colpitt's oscillator.

Ans. The difference between Hartley and Colpitt's oscillator is given in Table 1.

Hartley oscillator	*Colpitt oscillator*
Hartley oscillator is a tuned oscillator which consists of two inductances L_1 and L_2 and one capacitor C where $X_1 = \omega L_1$, $X_2 = \omega L_2$ and $X_3 = \frac{1}{\omega C}$	Colpitt oscillator is a tuned oscillator which consists of two capacitors C_1 and C_2 and one inductance L where $X_1 = \frac{1}{\omega C_1}$, $X_2 = \frac{1}{\omega C_2}$ and $X_3 = \omega L$
The frequency of oscillation is $f_o = \frac{1}{2\pi\sqrt{L_{eq}C}}$ where $L_{\text{eq}} = L_1 + L_2 + 2M$	The frequency of oscillation is $f_o = \frac{1}{2\pi\sqrt{LC_{eq}}}$ where $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$

(c) A Hartle oscillator is designed with $L_1 = 20$ μH, $L_2 = 2$ mH and a variable capacitor. Determine the range of capacitance values if the frequency is varied between 950 – 2050 kHz.

Ans. Given: $L_1 = 20$ μH, $L_2 = 2$ mH and frequency range 950 kHz – 2050 kHz

The frequency of Hartle oscillation is

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C}} \quad \text{where} \quad L_{\text{eq}} = L_1 + L_2 = 20\ \mu\text{H} + 2\ \text{mH} = 2.02\ \text{mH}$$

When $f_o = 950$ kHz , $f_o = \dfrac{1}{2\pi\sqrt{L_{eq}C}}$, or, $f_o^2 = \dfrac{1}{(2\pi)^2 L_{eq}C}$

$$C = \frac{1}{(2\pi)^2 L_{eq} f_o{}^2} = \frac{1}{(2\pi)^2 \times 2.02 \times 10^{-3} \times (950 \times 10^3)^2} = 28.095\ \text{pF}$$

When $f_o = 2050$ kHz , the value of capacitance is

$$C = \frac{1}{(2\pi)^2 L_{eq} f_o{}^2} = \frac{1}{(2\pi)^2 \times 2.02 \times 10^{-3} \times (2050 \times 10^3)^2} = 6.033\ \text{pF}$$

If the frequency is varied between 950 – 2050 kHz, the range of capacitance values is 28.095 pF to 6.033 pF.

4. (a) What is power amplifier? How does it differ from a voltage amplifier?

Ans. Refer to Section 8.1

(b) Explain with circuit diagram the operation of a transformer coupled class A power amplifier and calculate its maximum power efficiency.

Ans. Refer to Section 8.4

(c) Two transistor operate in class B push pull circuit with a collector supply voltage $V_{CC} = 15$ Volt. The turns ratio of the output transformer is 3:1 and the load resistance is 9 ohm. Determine maximum dc power supplied and the maximum output power. Also find out efficiency.

Ans. Given $V_{CC} = 15$ Volt, $R_L = 9\Omega$ and $N_1 : N_2 = 3 : 1$

$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = 3^2 \times 9\ \Omega = 81\ \Omega$$

The output power $P_{\text{ac}} = \dfrac{V_{CC}{}^2}{2R'_L} = \dfrac{15^2}{2 \times 81} = 1.3888$ Watt

Since $P_{\text{ac}} = \dfrac{1}{2} I_m{}^2 R'_L$, $I_m^2 = \dfrac{2P_{\text{ac}}}{R'_L} = \dfrac{2 \times 1.3888}{81}$ or, $I_m = 0.1851$ A

The dc power supplied $P_{\text{dc}} = \dfrac{2V_{CC}I_m}{\pi} = \dfrac{2 \times 15 \times 0.1851}{\pi}$ Watt = 1.7668 Watt

Efficiency $\eta = \dfrac{P_{\text{ac}}}{P_{\text{dc}}} \times 100\% = \dfrac{1.3888}{1.7668} \times 100\% = 78.6\ \%$

5. (a) What are the criteria of a good instrumentation amplifier? Describe the steps for building an instrumentation amplifier starting from the basic differential amplifier.

Ans. Refer to Section 6.2

(b) Draw the circuit diagram of an astable multivibrator using 555 timer and derive the expression of its frequency of oscillation.

Ans. Refer to Section 9.9

(c) For an astable multi-vibrator using 555 timer, $R_A = 6.8\ \text{k}\Omega$, $R_B = 3.3\ \text{k}\Omega$ and $C = 0.1\ \mu\text{F}$, Calculate

(i) t_{HIGH} (ii) t_{LOW} (iii) free running frequency (iv) duty cycle, D

Ans. Given $R_A = 6.8\ \text{k}\Omega$, $R_B = 3.3\ \text{k}\Omega$ and $C = 0.1\ \mu\text{F}$

(i) $t_{\text{HIGH}} = 0.693C(R_A + R_B) = 0.693 \times 0.1 \times 10^{-6}(6.8 \times 10^3 + 3.3 \times 10^3) = 0.69993$ ms

(ii) $t_{\text{LOW}} = 0.693CR_B = 0.693 \times 0.1 \times 10^{-6} \times 3.3 \times 10^3 = 0.22869$ ms

(iii) The free running frequency is equal to

$$f = \frac{1}{0.693(R_A + 2R_B)C} = \frac{1}{0.693(6.8 \times 10^3 + 2 \times 3.3 \times 10^3) \times 0.1 \times 10^{-6}}$$

$$= 1076.866 \text{ Hz}$$

(iv) Duty cycle $D = \dfrac{R_A + R_B}{R_A + 2R_B} = \dfrac{6.8 \times 10^3 + 3.3 \times 10^3}{6.8 \times 10^3 + 2 \times 3.3 \times 10^3} = 75.373\%$

6. Write short notes on any three of the following

(a) PLL

Ans. Refer to Sections 10.1 and 10.2

(b) Phase-shift oscillator

Ans. Refer to Section 5.5

(c) Tuned amplifier

Ans. Refer to Section 8.13

(d) Current mirror circuit

Ans. Refer to Section 6.9

(e) Trans-conductance multiplier

Ans. Refer to Section 7.16

Solution of 2013 WBUT Paper (EC(EE)301)

Group A

Multiple-Choice Type Questions

1. Choose the correct alternatives for any *ten* of the following: $10 \times 1 = 10$

(i) Gain of the emitter follower is approximately equal to

(a) α (b) $\beta + 1$ (c) β (d) $\frac{1}{(1-\alpha)}$

Ans. (a) α

(ii) To improve the efficiency of an amplifier, we have to reduce

(a) the power dissipation rating (b) supply voltage

(c) the load power (d) unwanted power loss

Ans. (d) unwanted power loss

(iii) An instrumentation amplifier

(a) is a differential amplifier (b) has a gain less than one

(c) has very high output impedance (d) has low CMRR

Ans. (a) is a differential amplifier

(iv) Saturation region of a BJT implies

(a) base-emitter is junction forward biased, base-collector is junction reverse biased

(b) base-emitter junction is forward biased, base collector junction is forward biased

(c) base-emitter junction is reverse biased, base-collector junction is reverse biased

(d) none of these

Ans. (b) base-emitter junction is forward biased, base collector junction is forward biased

(v) A differential amplifier has the differential amplifier gain of 100. If its CMRR = 240 then the common mode gain is

(a) 0.24 (b) 0.417 (c) 2400 (d) 1

Ans. (b) 0.417

(vi) A full-wave rectifier supplies 0.2 A current at 30 V dc. The ripple factor to be expected when two 100 μF capacitor and one 5 H inductor are used in a π-filter with a 50 Hz supply is

(a) 0 0.0076% (b) 0.076% (c) 0.76% (d) 76%

Ans. (b) 0.076%

(vii) The *Q*-point in a voltage amplifier is selected in the middle of the active region because

(a) it gives better stability

(b) the circuit needs a better small signal dc voltage

(c) the biasing circuit needs a small dc voltage

(d) it gives distortion-less output

Ans. (a) it gives better stability

(viii) The current gain of a bipolar transistor drops at high frequencies because of

(a) transistor capacitances (b) high current effects in the base

(c) parasitic inductive elements (d) the early effect

Ans. (a) transistor capacitances

(ix) The gain required for sustained oscillation in a Wien-Bridge oscillator is

(a) 29 (b) 3 (c) 1 (d) 1.5

Ans. (b) 3

(x) A dc power supply has no-load voltage of 30 V and a full-load voltage of 25 V at full-load current of 1 A. Its output resistance and load regulation respectively are

(a) 5 Ω and 20% (b) 25 Ω and 20%

(c) 5 Ω and 16.7% (d) 25 Ω and 16.7%

Ans. (b) 25 Ω and 20%

(xi) The output voltage of an IC 7915 is

(a) 15 V (b) –15 V (c) 79 V (d) –79 V

Ans. (b) –15 V

(xii) An instrumentation amplifier has a high

(a) supply voltage (b) power gain

(c) CMRR (d) Output impedance

Ans. (c) CMRR

Group B

Short-Answer-Type Questions

Answer any *three* of the following: $3 \times 5 = 15$

2. (a) Write down the effect of base width modulation.

Ans. The potential variation of the biased transistor is depicted in Fig. 1. The potential before applying the bias potential, is the dotted curve. It is evident from Fig. 1 that the forward biasing of the emitter junction decreases the emitter base potential barrier by V_{EB}. The reverse biasing of the collector junction increases the collector base potential barrier by V_{CB}. Therefore, the emitter junction barrier voltage is $V_0 - V_{EB}$ and the collector junction barrier voltage is $V_0 + V_{CB}$.

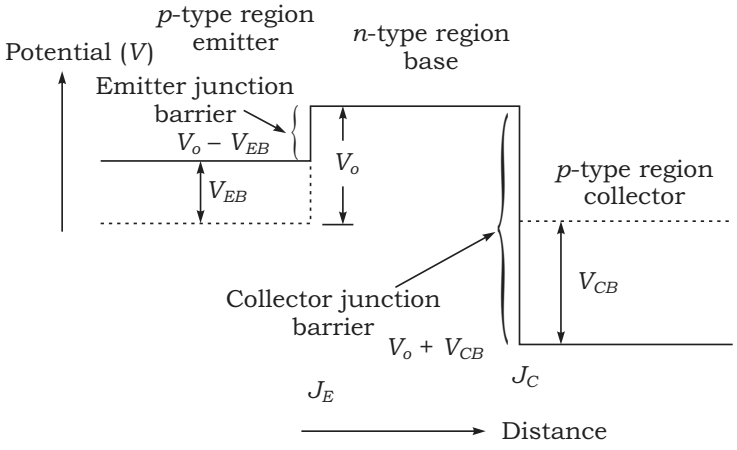


Fig. 1 The potential of a *p-n-p* transistor at biased condition

In Fig. 1, the space charge regions on the emitter-base junction (J_E) and collector-base junction (J_C) are neglected. When the width of the depletion layer is present at J_E and J_C junctions, Fig. 1 will be modified. We know that the width of depletion layer of a *p-n* junction is increased with increasing the reverse bias voltage, but the depletion layer width decreases with increasing forward bias voltage. As the emitter-base junction is forward biased, the depletion layer or barrier width of J_E is neglected. Since the collector-base junction is reverse biased, the depletion layer or space charge width increases and exist at junction J_C.

The transition region at junction J_C has a region of uncovered charges on the both sides of the junction. When the reverse bias voltage across the junction increases, the transition region can penetrate deeper into the base and collector region as depicted in Fig. 2.

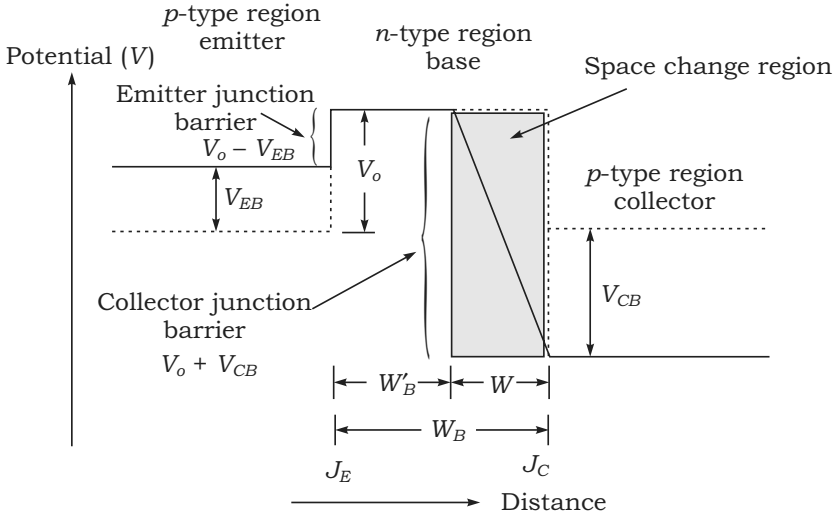


Fig. 2 The potential barrier of a *p-n-p* transistor with space charge width *W*

As the neutrality of charge must be retained, the net charge must be zero and the number of uncovered charges on each side must be equal. Since the doping concentration in the base region is comparatively small with respect to the collector, the penetration of depletion layer or space charge region into the base region is very large compared to the space charge region in the collector region. Therefore, the depletion layer width in the collector region can be neglected.

When the metallurgical base width is W_B and W is the width of the transition region, the effective electrical base width becomes $W'_B = W_B - W$. The modulation of the effective base width due to the reverse bias voltage across collector-base junction (J_C) is called *base width modulation* or *early effect*. The reduction in effective base width with increasing reverse collector-base voltage has the following consequences:

- There is very small possibility for recombination of electrons and holes in the base region. Consequently, α increases with increasing collector-base voltage (V_{CB}).
- The concentration gradient of minority carriers p_n increases within the base. The hole concentration p_n is zero at a distance d, which is in between W_B and W'_B, but the potential at J_C becomes below V_O. Figure 3 shows the minority carrier density within base region at low reverse-bias and high reverse-bias conditions.
- The hole current injected across the emitter is proportional to the gradient of p_n at J_E and I_E increases with increasing reverse collector-base voltage.
- For very high voltage, W'_B becomes zero causing voltage breakdown in the transistor. This phenomenon is called *punch through*.

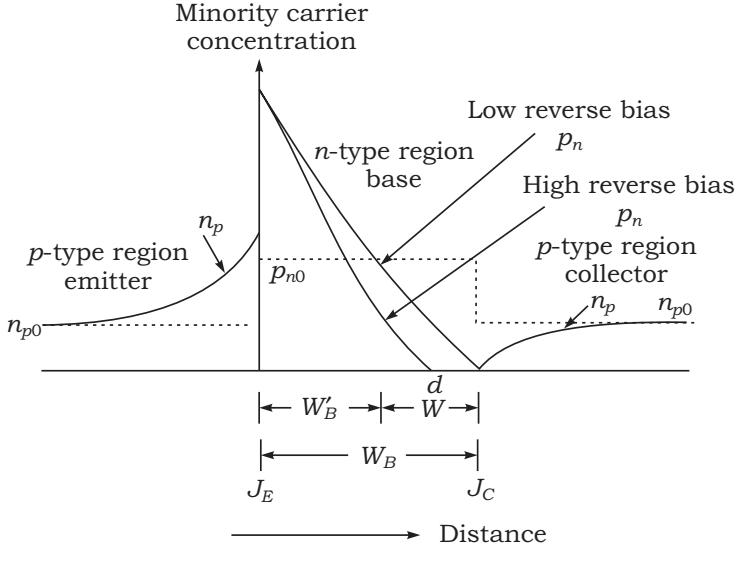


Fig. 3 The minority carrier density within base region at low reverse bias and high reverse bias

(b) Explain the compensation technique using Thermistor.

Ans. Refer Section 2.18.2 (Page 2.41)

3. What are the criteria of a good instrumentation amplifier? Why is it needed? Draw the circuit diagram of an instrumentation amplifier.

Ans. Refer Section 7.20 (Page 7.43–7.45)

4. (a) What is a multivibrator?

Ans. Refer Section 9.1 (Page 9.1)

(b) Explain the operation of a monostable multivibrator using 555 timer and draw the output voltage waveform.

Ans. Refer Section 9.9.2 (Page 9.24)

5. What are the differences between series and shunt regulators? Draw a circuit of a shunt regulator and explain its operation.

Ans. Refer Solution of 2011 WBUT Paper (EC 304) Question No. 5 (Page SL3)

6. Draw and explain the Schmitt trigger circuit using OP-AMP

Ans. Refer Section 7.19 (Page 7.40–Page 7.41)

GROUP C

Long-Answer-Type Questions

Answer any *three* of the following: $3 \times 15 = 45$

7. (a) Explain Barkhausen criteria for oscillation and find out frequency of oscillation in phase shift oscillator and also prove that the amplifier gain in a phase shift oscillator is 29 for sustained oscillation.

Ans. Refer Section 5.4 (Page 5.5) and Refer Section 5.6 (Page 5.7)

(b) Discuss the advantages of switched mode power supply (SMPS) over regulated power supply.

Ans. Refer Section 1.12.3 and Section 1.12.4 (Page 1.23)

(c) Using a circuit diagram explain in short the operation of SMPS.

Ans. Refer Section 1.12 (Page 1.21) and Section 1.12.2 (Page 1.22)

8. (a) What do you mean by regulation? Draw and explain a CLC or π-filter.

Ans. Refer Section 1.7 and Section 1.5

(b) Draw and explain the operation of shunt regulated power supply.

Ans. Refer Section 1.9

9. (a) Explain the operation of a class B push-pull amplifier and prove that the efficiency is 78.5%.

Ans. Refer Section 8.9 and Section 8.11

(b) What is cross-over distortion in class B amplifier and how can we remove the problem?

Ans. Refer Section 8.10

(c) Compare different types of power amplifier in respect of efficiency and phase response.

Ans. The comparison between different types of power amplifier in respect of efficiency and phase response is given in Table 1.

Table 1 Comparison between different types of power amplifier

Parameter	*Class A amplifier*	*Class B amplifier*	*Class AB amplifier*	*Class C amplifier*	*Class D amplifier*
Efficiency	25%	78.5%	Between that of Class A and Class B	about 75%	100%
Phase response	Zero phase shift. Output transistor conducts for the entire cycle of the input signal	Zero phase shift. Output transistor conducts for only one-half of each sine wave input cycle	Output transistor conducts for slightly more than half a cycle	Non-linear phase response. Output transistor conducts for less than half a cycle	Zero Phase Shift

10. In what respects Class B push-pull amplifier configuration is better than Class A push-pull amplifier? What are the major drawbacks of Class B operation and how is it remedied? Prove that the maximum efficiency of a Class B amplifier is 78.5%.

Ans. Refer Section 8.9.1, Section 8.10 and Section 8.11

(b) What is the function of a tuned amplifier?

Ans. Refer Section 8.13

11. Write short notes on any three of the following 3×5

(a) Clamping and clipping circuit

Ans. The *PN* junction diodes are extensively used in non-linear wave shaping circuits. These non-linear wave-shaping circuits perform *clipping*, *limiting* and *clamping* operations. The clipping circuit is a circuit in which the output voltage waveform is developed by clipping or removing a certain portion of the input voltage signal. This circuit can also be used to limit the amplitude of output voltage and the circuit is called as *limiter*. The clipping circuits most commonly used in analog electronics circuits, radio and television receivers, radars, and digital logic circuits. There are four types of clipping circuits such as

(i) Positive clipping circuit
(ii) Negative clipping circuit
(iii) Biased clipping circuit
(iv) Combination clipping circuit

Positive Clipping Circuit

Figure 4 shows the positive clipping circuit which consists of a diode (D) and a resistance R_L and the output is obtained from the voltage across the resistance R_L. Assume the diode (D) behaves as an ideal switch. When the input voltage is negative ($V_i < 0$), the diode is forward biased and it acts as a closed switch. If the input voltage $V_i > 0$, diode is reverse bias and it acts as an open switch.

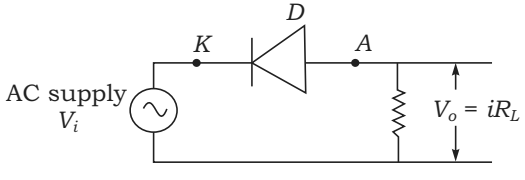


Fig. 4 The series positive clipping circuit

Figure 5 shows the input and output voltage waveforms. During the positive half cycle of the input applied voltage, cathode (K) is positive with respect to anode (A). Therefore, all the input applied voltage drops across the diode and the voltage across resistance R_L is zero. Hence, during the positive half cycle, there is no output voltage. In the negative half cycle of the input applied voltage, the anode (A) is positive with respect to cathode (K). Consequently, there is no voltage drop across diode during negative half cycle of the input applied voltage. All the input applied voltage drops across the resistance (R_L) as depicted in Fig. 5(b).

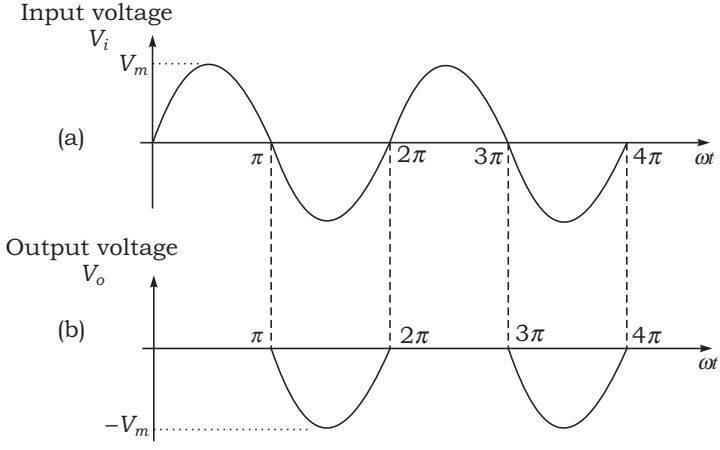


Fig. 5 Input and output voltage waveforms of positive clipper

It is clear from the output voltage waveform that the positive clipper circuit can only pass the negative half cycle of the input applied voltage and clipped the positive half cycle of the input applied voltage. In this circuit the diode acts as a series switch between the supply voltage and load resistance, it is called *series positive clipper*.

The positive clipper circuit is also possible to connect a diode as a shunt switch between the supply voltage and load resistance R_L as depicted in Fig. 6. This circuit is called *shunt positive clipper*.

When the input voltage is positive ($V_i \geq 0$), diode is forward bias and it acts as a closed switch. If the input voltage is negative or less than zero ($V_i < 0$), the diode is reverse bias and it acts as an open switch. The output voltage waveform will be same as that of a series positive clipper circuit.

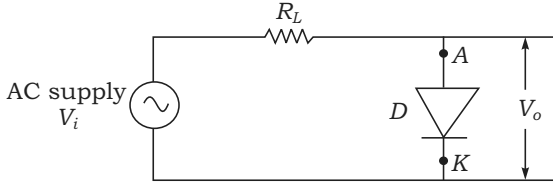


Fig. 6 The shunt positive clipping circuit

Clamping Circuit

The clamping circuit is a circuit in which the output voltage can be shifted in such a way that a certain part of it must be maintained at a specified voltage level. Actually, a clamping circuit restores a dc level to an ac signal. Therefore, this circuit is also called dc restorer. Figure 7 shows the input signal varies in between +5 V to –5 V. The corresponding positive clamped ac signal is shown in Figure 8.

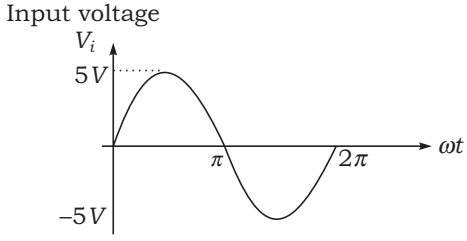


Fig. 7 Input voltage signal

Positive Clamper Circuit

Figure 8 shows a positive clamper circuit which consists of a diode and a capacitor. The clamping action can be verified when the diode is forward biased. During the negative half cycle of input voltage, the diode is forward biased and current flows through the circuit.

The capacitor is charged to a voltage which is equal to the negative peak value ($-V_m$). Once the capacitor is fully charged to the negative peak voltage ($-V_m$), the capacitor cannot be discharged as the diode conducts only in the forward direction. Consequently, the capacitor behaves as a battery voltage $-V_m$ so that the output voltage is equal to the sum of ac input voltage and the capacitor voltage V_m. Then the output voltage is given by

$$V_O = V_i + V_m = V_m \sin \omega t + V_m$$

It is clear from the above equation that the dc voltage V_m is introduced to the input voltage signal. Hence, the output voltage waveform is clamped positively at 0 V as depicted in Fig. 8(b).

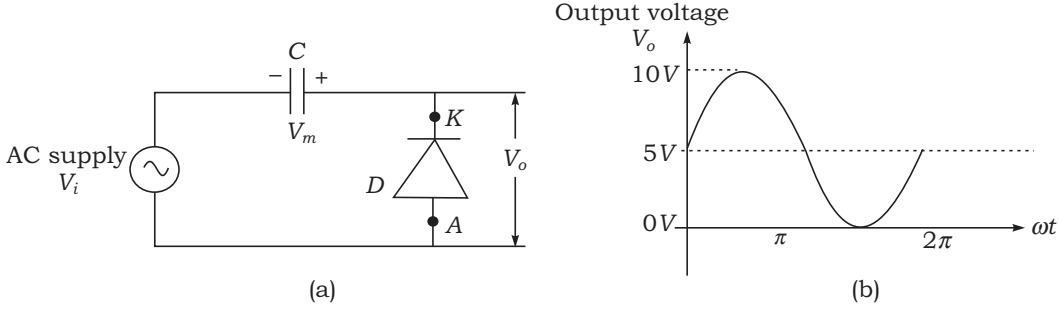


Fig. 8 (a) Positive clamper circuit (b) Output voltage as $V_m = 5$ V

(b) Tuned amplifier

Ans. Refer Section 8.13

(c) Antilog Amplifier

Ans. Refer Section 7.143

(d) Precision rectifier

Ans. Refer Section 7.21

(e) Triangular wave generator

Ans. Refer Solution of 2011 WBUT Paper (EC 304) Question 12(e) (Page SL7)

Solution of 2014 WBUT Paper (EC304)

Group A

Multiple-Choice Type Questions

1. Choose the correct alternatives for any *ten* of the following: $10 \times 1 = 10$

(i) A 1 ms pulse can be stretched to a 1 s pulse by using

(a) an astable multivibrator (b) a monostable multivibrator

(c) a bistable multivibrator (d) a schmitt trigger

Ans. (b) A monostable multivibrator

(ii) Which one of the following power amplifiers has the maximum efficiency?

(a) Class A (b) Class B

(c) Class AB (d) Class C

Ans. (d) Class C

(iii) Which one of the following oscillators is used for generation of high frequencies?

(a) *RC* phase shift oscillator (b) Wein bridge oscillator

(c) *LC* oscillator (d) Blocking oscillator

Ans. (c) *LC* oscillator

(iv) An amplifier with an initial open-loop gain of 400 is used as a negative feedback amplifier. The feedback factor is 0.05. If the gain of the amplifier changes by 10% due to temperature then the closed-loop gain will change approximately by

(a) 0.05% (b) 0.1%

(c) 0.5% (d) 1%

Ans. (c) 0.5%

(v) Thermal runway in a transistor biases in the active region is due to

(a) heating of the transistor

(b) changes which increase with temperature

(c) base emitter voltages V_{BE}, which decreases with rise in temperature

(d) change in reverse saturation current due to rise in temperature

Ans. (d) change in reverse saturation current due to rise in temperature

(vi) The ideal characteristics of a stabilizer is
  (a) constant output voltage with low internal resistance
  (b) constant output voltage with high internal resistance
  (c) constant internal resistance with variable output voltage
  (d) none of these

Ans. (a) constant output voltage with low internal resistance

(vii) Removing bypass capacitor across the emitter log resistor in a CE amplifier causes
  (a) increase in current gain (b) decrease in current gain
  (c) increase in voltage gain (d) decrease in voltage gain

Ans. (d) decrease in voltage gain

(viii) An instrumentation amplifier
  (a) is a differential amplifier (b) has a gain less than one
  (c) has very high output impedance (d) has low CMRR

Ans. (a) is a differential amplifier

(ix) The value of V_o for the circuit in Fig. 1 is given by

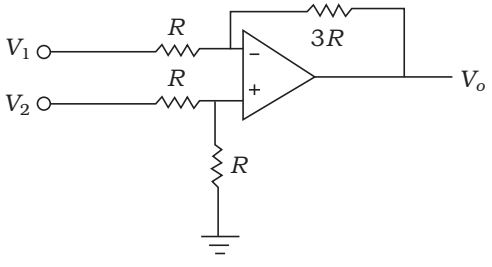


Fig. 1

  (a) $-3V_1 + 2V_2$ (b) $-3V_2$
  (c) $-2.25V_1 + 1.5V_2$ (d) $-2V_1 + 3V_2$

Ans. (a) $-3V_1 + 2V_2$

(x) A Schmitt trigger uses
  (a) negative feedback (b) positive feedback
  (c) pull-up resistor (d) compensating capacitor

Ans. (b) positive feedback

(xi) Base-to-emitter V_{BE} in a forward-biased transistor decreases with increase of temperature at the following rate:
  (a) 25 mV/°C (b) 0.25 mV/°C (c) 2.5 mV/°C (d) 0.6 mV/°C

(xii) Which of the following configurations can be used as buffer?
  (a) CE (b) CB (c) CC (d) All of these

Ans. (c) CC

Group B

Short-Answer-Type Questions

Answer any *three* of the following: 3 × 5 = 15

2. In the circuit shown in Fig. 2, V_{cc} = 10 V, R_c = 2.5 kΩ, R_F = 200 kΩ, β = 99, V_{EB} = 0.6 V. Determine the operating point (V_C, I_C).

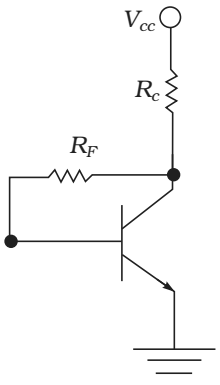


Fig. 2

Ans. Given: V_{cc} = 10 V, R_c = 2.5 kΩ, R_F = 200 kΩ, β = 99, V_{EB} = 0.6 V. Applying Kirchhoff's voltage law in the base-emitter circuit, we obtain

$$V_{CC} = V_{BE} + I_B R_F + I_C R_C$$

We know $V_{CC} = V_{CE} + I_C R_C$ and $I_C = \beta I_B$

Therefore, $V_{CC} = V_{BE} + I_B R_F + I_C R_C = V_{BE} + I_B R_F + \beta I_B R_C$

or, $V_{CC} = V_{BE} + I_B(R_F + \beta R_C)$

Then base current $I_B = \dfrac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \dfrac{10 - 0.6}{200 \times 10^3 + 99 \times 2.5 \times 10^3} = 0.021$ mA

The current $I_C = \beta I_B = 99 \times 0.021 = 2.079$ mA

The voltage $V_{CE} = V_{CC} - I_C R_C = 10 - 2.079 \times 10^{-3} \times 2.5 \times 10^3 = 4.8025$ V

The operating point (V_C, I_C) is (4.8025 V, 2.079 mA)

3. How does the negative feedback affect the characteristics of an amplifier?

Ans. The negative feedback affects the following characteristics of an amplifier:

- Reduction in frequency distortion
- Reduction in noise and non-linear distortion
- Effect of negative feedback on gain and bandwidth
- Gain stability with feedback
- Reduction in phase distortion

Refer Sections 4.7.1, 4.7.2, 4.7.3.

4. What is Common Mode Rejection Ratio (CMRR) and slew rate of an operational amplifier?

Ans. Common Mode Rejecting Ratio (CMRR): Refer Section 6.12.6.

Slew rate: Refer Section 6.12.8.

5. (a) Write a note with related mathematical derivation of op-amp as a non-inverting amplifier.

Ans. Refer Section 7.3.

What is buffer?

Ans. Refer Section 7.4.

6. What is PLL? Define the terms: (i) capture range (ii) lock-in range (iii) pull-in time

Ans. Refer Sections 10.1 and 10.2.

GROUP C

Long-Answer-Type Questions

Answer any *three* of the following: $3 \times 15 = 45$

7. (a) Explain the operation of an astable multivibrator using a 555 timer. Derive the expressions for frequency in case of output waveform.

Ans. Refer Section 9.9.1.

(b) Draw and explain the operation of a monostable multivibrator using a 555 timer.

Ans. Refer Section 9.9.2.

8. (a) What is a power amplifier?

Ans. Refer Section 8.1.

Draw and explain a Class A power amplifier.

Ans. Refer Section 8.3.

(b) What are the advantages of a push-pull amplifier? Why is the push-pull circuit called so?

Ans. Refer Sections 8.8.1 and 8.8.

(c) What is cross-over distortion in a Class B amplifier? How is it eliminated?

Ans. Refer Section 8.10.

9. (a) Sketch the circuit of a Wien bridge oscillator. Explain the principle of operation and prove that the gain of the amplifier used in a Wien bridge oscillator must be greater than 3 for sustained oscillations.

Ans. Refer Section 5.9.

(b) Explain the operation of a crystal oscillator. Mention its two advantages.

Ans. Refer Section 5.12.

Two advantages of a crystal oscillator are

(i) Very high operating frequency range

(ii) Frequency stability

(c) A Wien bridge oscillator is to span a range of frequencies from 30 Hz to 30 kHz. The variable capacitance can be changed from 50 pF to 500 pF. Find the resistance needed to span the frequency range. If the gain of the amplifier is 6, what must be the ratio of the resistance in the other arms of the bridge?

Ans. Given capacitor range is 50 pF to 500 pF and range of frequency is 30 Hz to 30 kHz.

The frequency of oscillation is $f = \dfrac{1}{2\pi RC}$

If $f = 30$ Hz, $C = 50$ pF, the value of the required resistance is

$$R = \frac{1}{2\pi fC} = \frac{1}{2 \times 3.14 \times 30 \times 50 \times 10^{-9}} = 106.2 \text{ k}\Omega$$

The capacitance varies in the ratio 50 pF to 500 pF = 1:10. Then the oscillator frequency range will be 30 Hz to 300 Hz with $R = 106.2$ kΩ.

Therefore, to generate output signal in the frequency range from 300 Hz to 3 kHz, the value of R will be $\frac{1}{10}$ of 106.2 kΩ = 10.62 kΩ.

In the same way, for the output frequency range from 3 kHz to 30 kHz, the value of R will be $\frac{1}{10}$ of 10.62 kΩ = 1.062 kΩ.

Since the gain of the amplifier is $A = 6$, for oscillations, $\delta = A = 6$ and

$$\frac{R_4}{R_3 + R_4} = \frac{1}{3} - \frac{1}{\delta} = \frac{1}{3} - \frac{1}{6} = \frac{1}{3} = 0.333$$

or $$1 + \frac{R_3}{R_4} = 3$$

Therefore, the ratio of the resistance in the other arms of the bridge $\frac{R_3}{R_4} = 2$

10. (a) Define hybrid parameters for a basic transistor circuit in common-emitter configuration and give its hybrid model.

Ans. Refer Section 2.27.

(b) Explain the quiescent point and load line of a transistor amplifier.

Ans. Refer Section 2.11.

(c) Design a self-bias circuit to establish the Q-point at I_c = 1 mA using a collector supply V_{cc} = 12 V. Assume $\beta = 100$, $V_{BE} = 0.7$ V.

Ans. Given: I_c = 1 mA, V_{cc} = 12 V, $\beta = 100$, $V_{BE} = 0.7$ V.

The voltage across the emitter is $V_E = I_E R_E$. Assume R_E = 500 Ω and $I_E = I_C$ = 1 mA

Therefore, $V_E = I_E R_E = 1 \times 10^{-3} \times 500 = 0.5$ V

The potential across R_2 is $V_B + V_{BE} + V_E = 0.7 + 0.5 = 1.2$ V

The voltage V_B can be expressed by

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2} = 12 \frac{R_2}{R_1 + R_2} = 1.2$$

or, $$\frac{12}{1.2} = \frac{R_1 + R_2}{R_2} = 1 + \frac{R_1}{R_2}$$

Therefore, $$\frac{R_1}{R_2} = 9$$

If R_2 = 1 kΩ, R_1 = 9 kΩ, assuming R_c = 1.5 kΩ, the KVL equation across the collector emitter is

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 12 - 1 \times 10^{-3} \times 1.5 \times 10^{-3} - 0.5 = 10 \text{ V}$$

The collector voltage $V_C = V_{CE} + I_E R_E = 10 + 0.5 = 10.5$ V

11. Write short notes on any *three* of the following:

(a) High-frequency model of a transistor

Ans. Refer Section 2.29.

(b) Current mirror

Ans. Refer Section 6.9.

(c) Comparator

Ans. Refer Section 7.18.

(d) Class C amplifier

Ans. Refer Section 8.3.

(e) Capacitor filter and π-section filter

Ans. Refer Sections 1.3 and 1.5.