BASIC ELECTRONICS

About the Author

Ravish Aradhya H V is currently working as Associate Professor in the Electronics & Communication Engineering Department at RV College of Engineering, Bangalore, one of the most reputed engineering colleges in India. The Electronics & Communication Engineering Department at RV College of Engineering is the most sought-after branch among the student community, particularly among those appearing for CET (Common Entrance Test) in Karnataka. The author has been associated with this premier institution for the past 18 years.

With a vast teaching experience spanning 22 years, the author has understood the basic needs of students in learning technology. He has set up various laboratories like Digital Circuits Lab, Microprocessors Lab, Microcontrollers Lab, Computer Communication Networks Lab, Analog Circuits Lab and prepared study material for these subjects in the department. He received the "BEST TEACHER" award for Excellence in Teaching from CAREER LAUNCHER (India), Ltd.

Prof. Aradhya headed the Computer Organisation team in Visweswaraiah Technological University's EDUSAT programme. He has a very rich experience in teaching students at various levels because of his opportunities as a visiting faculty to prestigious organisations like C-DAC, Honeywel (India), Manipal University of Advanced Studies, and University Visveswaraiah College of Engineering. He is a member of Board Of Studies (BOS) at RV Autonomous Institution; Board Of Examiners (BOE) at RV Autonomous Institution, IETE, New Delhi, and various other institutions. He is a life member of professional organisations like Indian Society for Technical Education (ISTE) and Institution of Electronics and Telecommunication Engineers (IETE).

Prof. Aradhya's research area is low-power VLSI design and he has submitted his research thesis on Reversible Logic Design to Visvesvaraya Technological University (VTU), Belgaum, Karnataka, for evaluation. The author, to his credit, has presented papers in 11 international and 17 national conferences. He has guided a number of postgraduate and undergraduate projects, and also several projects executed by his students for various reputed organisations like ISRO, INTEL, TI, ADA, ADE, BEL, NAL, etc. His areas of interest include Electronic Devices and Circuit Theory, VLSI Design, Microprocessor and Microcontroller Applications, Embedded Systems and Computer Networking.

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Preface

Overview

Basic Electronics is a common course for all engineering disciplines. Students of all engineering disciplines, particularly non-electrical engineering disciplines, find it very difficult to understand the basic concepts of this subject. Most of the currently available textbooks provide high-end information, but fail to provide elaborate and detailed explanation on most topics. Also, there is *no single book* that covers the entire syllabus of any university and provides all the necessary information.

Even for the students of electrical engineering disciplines, there is a need for catering to strong fundamentals, so that they can be more comfortable at higher semester levels. Most current titles have not given enough scope for the basics. Hence, a thorough attempt has been made to cover the entire syllabus in one book, with a lot of emphasis on basics. This text covers the Basic Electronics syllabi of more than 12 different leading universities of India. Much effort has been made to present the information in a lucid and easily understandable way, so that it is effective for the students at the first/second semester levels. Also, the content is designed to help all classes of students at lower and even in higher semester levels.

Aim of the Book

This book mainly intends to be a text for a first course in electronics of all electronics and electrical sciences students. The text grows around the electronics first-course syllabi offered at various technical and science universities. The book aims to cater to the needs of mainly undergraduate students—providing the internal behaviour of important electronic devices, the principles of operation and design concepts, and analysis of circuits/systems built using these devices.

Many available books on the first course on basics of *electronic devices* and *principles of circuit theory* require significant improvements in pedagogy and content. This book is an attempt to cater to the changing curriculum and examination requirements—primarily to improve the manner in which the material is presented.

About the Book

I have given considerable thought to the pedagogy of presentation: the **system of notations** is consistently maintained, the **circuit behaviour** is explained with in-depth coverage, and the worked-out **illustrative examples** provide detailed insight to the subject. The **diagrams** present a thorough understanding of the concepts, and the **tables** are carefully prepared to illustrate the topics. The **chapter summary** helps the reader recall the concepts studied after each chapter. The **multiple-choice questions** are prepared with an intensive coverage, meant to create increasing confidence in the reader. The quiz offers **short answers to questions** framed to increase readers' knowledge on the concepts and subject. All these elements summarise the concepts taught and help in future review.

Salient Features

- **Complete coverage of subject** as per requirements of all technical universities and science colleges
- **Elaborate coverage, lucid presentation** and **easy flow** maintained
- Stress on the **foundation principles of electronics**
- **Applications of fundamental principles** interspersed within the content
- **Important topics** like LED Characteristics, MOSFET, Power Semiconductor Devices, Feedback Amplifiers and Oscillators, Shift Registers and Counters discussed in detail
- **Goals and objectives** at the beginning, and chapter-end **Summary** provided for each chapter
- Helpful guide for **competitive examinations**
- Numerous **block diagrams** and **circuit diagrams** to enhance understanding
- Pedagogy includes
  - 300 Diagrams
  - 320 Solved Examples
  - 450 Multiple-Choice Questions
  - 225 Review Questions
  - 185 Problems
  - 250 Short-Answer Questions

Chapter Organisation

The book is organised into 10 well-designed chapters, covering almost all the needs of a first course in electronics. The overview of each chapter is outlined below:

Chapter 1 covers the fundamentals of semiconductor physics, charge carriers in semiconductors and doping concepts. The *PN*-junction formation, its behaviour under different biasing conditions, characteristics and equivalent circuits are discussed.

Chapter 2 deals with the fundamentals of a semiconductor *PN*-junction diode, its characteristics and load-line analysis. All important applications of junction diodes such as rectifiers, voltage multipliers, wave-shaping circuits and basic logic gates are covered with maximum care. The other sub-systems of power supply, such as filters and regulators, are also designed and analysed.

Chapter 3 presents another very important semiconductor three-terminal device, the Bipolar Junction Transistor (BJT). The fundamentals of device construction, characteristics, and configurations of operation are covered. Different biasing methods and applications of BJT are covered to a large extent.

Chapter 4 introduces applications of BJT such as amplifiers, oscillators and feedback concepts. Amplifier classification, design analysis, feedback concepts, effect of feedback on the performance of BJT circuits is discussed. Oscillator classification and design analysis are also presented in this chapter.

Chapter 5 explains fundamentals of communication, modulation/demodulation methods and their performance comparison. The chapter also discusses radio and television communication applications.

Chapter 6 covers fundamentals of important linear integrated circuits such as operational amplifier, timer and Phase-Locked Loops (PLLs). The internal architecture, characteristics and useful applications of these devices are discussed. The worked examples, multiple-choice questions and chapter-end summary aims to make the reader more confident in using these ICs in real-life applications.

Chapter 7 presents the fundamentals of switching theory and logic design, covering basics to real-world applications, both in combinational and sequential systems. Applications such as arithmetic circuits, latches, flip-flops, registers, counters, etc. are also discussed.

Chapter 8 deals with fundamentals of measuring and display instruments. Measuring instruments like voltmeters, ammeters, multimeters and display instruments like cathode ray oscilloscopes are discussed in this chapter. Measurements such as frequency and phase angle for signals are covered thoroughly.

Chapter 9 explains fundamentals of transducers. In real-world applications, transducers play a vital role and the chapter provides a very good introduction for readers.

Chapter 10 covers fundamentals of other very important semiconductor devices such as Field Effect Transistors (FETs), Metal Oxide Semiconductor FETs (MOSFETs), Unijunction Transistors (UJTs), etc. The fundamentals of device construction, characteristics, and configurations of operation are dealt with. Different biasing methods and applications of FETs are discussed to a large extent. Silicon Controlled Rectifier (SCR), another very important semiconductor device that finds strong applications in power electronics, is also presented in this chapter.

Considerable efforts have been put in to the layout of different chapters, preparation of the material and of presentation pedagogy. A large variety of exercise problems provided at the end of each chapter will certainly help the reader develop strong fundamental knowledge. I expect and hope that all readers would highly benefit from these pedagogical features during self-study. Budding engineers will find the text very useful in updating their knowledge base.

Online Learning Centre

The text is accompanied by an exhaustive Online Learning Centre which can be accessed at https://www.mhhe.com/aradhya/be1

This website contains the Solution Manual and PowerPoint Lecture slides.

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First, I thank all the reviewers responsible for making the text acceptable to a large user community. Their names are given below:

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Thanks are also due to the student community and my teachers who made *me* a teacher. I sincerely acknowledge the contribution of my family who supported the cause largely. In this regard, my wife, Smt. Vijayalakshmi, who is a source of inspiration in all my endeavours, deserves a special mention.

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Ravish Aradhya HV

Publisher's Note

Do you have any further request or a suggestion? We are always open to new ideas (the best ones come from you!). You may send your comments to *tmh.elefeedback@gmail.com*

Piracy-related issues may also be reported!

Guided Tour

curve

1.13.4 Light-Emitting Diode

Unlike all other class and forms of diodes, there is one particular class of diode that is the light emitting diode, popularly called LED which is very important in current-day applications. Semiconductor materials like Gallium Arsenide Phosphide (GaAsP) and Gallium Phosphide (GaP) are used in the manufacture of visible coloured LEDs such as red LED, green LED and orange LED. Recombination

10.3 MOSFETs

A field effect transistor can be constructed with the gate terminal insulated from the channel. A metal oxide semiconductor FET (MOSFET) or IGFET extension bits very high i/p impedance because of insulated gate terminal.

A MOSFET can be of two types:

(i) Depletion MOSFET

7.13 COUNTERS

A counter is a logic circuit that is used to count the sequence of operations. Normally, a *T*-FF is the basic building block of a counter. A counter is one of the most useful and versatile subsystems in a digital system. A counter driven by a clock can be used to count the number of external events. Since the clock pulses occur at known intervals of time, a counter can be used as an instrument for measuring time and, therefore, period or frequency. Based on the way the clock pulses are connected to individual *T*-FF, counters can be classified into two types: asynchronous or ripple counters and synchronous counters. A

7.14 SHIFT REGISTERS

A register is a group of flip-flops arranged so that the binary numbers stored in the flip-flop are shifted from one flip-flop to the next for every clock pulse. Figure 7.51(a) shows a 4-bit shift register using *JK* flip-flops working as *D*-FF. The flip-flops are arranged such that the output of FF-A is transferred into FF-*B*, the output of FF-*B* is transferred into FF-C and the output of FF-*C* is transferred into FF-D when a clock pulse is applied. There are a number of commercial shift registers available and IC-7495 is one

BJT Amplifiers, Feedback and Oscillators

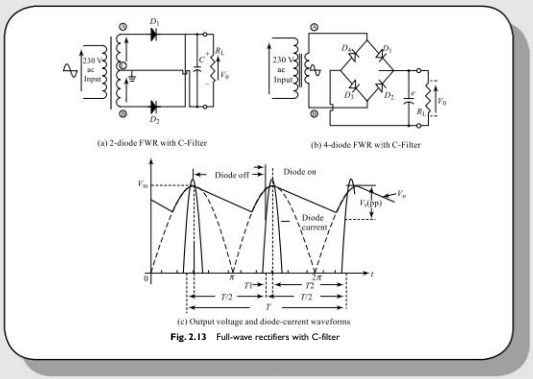
4

Goals and Objectives

Upon completion of this chapter, the reader is expected to

- Recall all the basic concepts of bipolar junction transistors from Chapter 3
- Understand the basic need for BJT biasing and importance of Q-point
- Define the terms *amplifier, gain* and *decibel* and compute the gain of an amplifier
- Understand the basic principles and need of an amplifier
- Understand the parameters used for various classification of amplifiers
- Understand the applications of audio-frequency amplifiers and radio-frequency amplifiers
- Differentiate between single-stage and multistage amplifiers

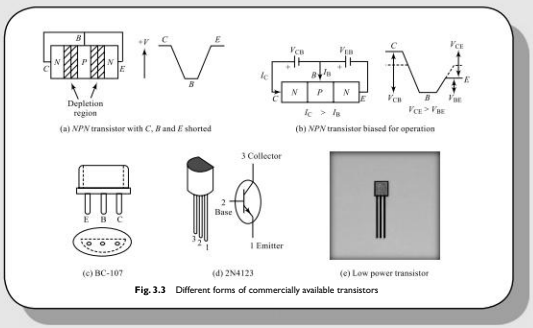
Important topics like LED Characteristics, MOSFET, Power Semiconductor Devices, Feedback Amplifiers and Oscillators, Shift Registers and Counters discussed in detail



(a) 2-diode FWR with C-Filter (b) 4-diode FWR with C-Filter

(c) Output voltage and diode-current waveforms

Fig. 2.13 Full-wave rectifiers with C-filter



(a) *NPN* transistor with *C*, *B* and *E* shorted (b) *NPN* transistor biased for operation

(c) BC-107 (d) 2N4123 (e) Low power transistor

Fig. 3.3 Different forms of commercially available transistors

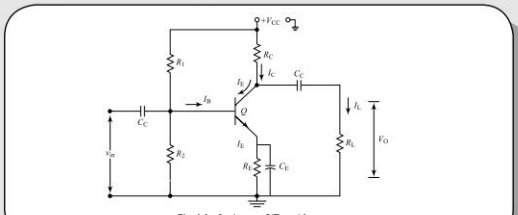


Fig. 4.6 Single-stage BJT amplifier

300 block diagrams and circuit diagrams to enhance understanding

Semiconductor Physics and *PN* Junction

1

Goals and Objectives

Upon completion of this chapter, the reader of the book is expected to

- Understand the importance of electronics in everyday life
- Review the basics of atomic structure and energy levels of different materials
- Understand the general characteristics of important semiconductor materials like silicon, germanium, gallium arsenide, etc
- Understand the principle of electron and hole conduction
- Differentiate between *N*-type and *P*-type semiconductor materials
- Understand the characteristics of a *PN* junction under unbiased, forward-biased and reverse-biased conditions
- Understand the importance and draw an equivalent circuit of a *PN* junction
- Understand the use of diode as a switch in electronic applications
- Understand the importance of diode capacitances: diffusion capacitance and transition capacitance
- Understand the use of diode capacitances in applications such as FM generation
- Understand the effect of reverse recovery time on performance of diode circuits
- Understand the working principle and characteristics of other semiconductor diodes
- Understand the concepts of Zener regulator, FM generation, LED display, etc.
- Understand the reading and interpretation of diode-specification sheets
- Do physical interpretation of concepts with a good number of examples provided
- Feel confident in moving to the next chapter on **diode applications**

Goals and Objectives at the beginning of each chapter to introduce the topics

320 Solved Examples spread across the text to help students solve numerical problems related to the topics

Example 1.5

Find the current flowing through a *PN* junction when a potential of 0.2 V is applied across the junction at room temperature, given the junction current of 5×10^{-7} A when a large reverse bias applied across the junction.

Solution Given $I_O = 5 \times 10^{-7}$ A, $V = 0.2$ V and $T = 27°C$

We have Eq. (1.4); $V_T = T/11600 = 26$ mV

We have diode current equation given by Eq. (1.2):

$$I_D = I_O\,(e^{V/\eta V_T} - 1)\ \text{A};\ \eta = 1 \text{ for germanium}$$

$$= 5 \times 10^{-7}(e^{0.2/1\times 26\ \text{mV}} - 1)\ \text{A} = 5 \times 10^{-7}(2191.426 - 1)\ \text{A}$$

$$\boxed{I_D = 1.095\ \text{mA}}$$

In summary, the most important characteristic of a *PN* junction diode is its ability to offer very little resistance for the current flow in the forward direction and maximum resistance to current flow in the reverse direction. This property can be exploited in using the diode as an electronic switch.

Example 4.2

A single-stage amplifier with an input of 250 mV produces an output of 1.5 V. What is the gain?

Solution Given $v_{in} = 250$ mV and $v_o = 1.5$ V

From Eq. 4.2(a), the voltage gain is

$$A_v = \frac{v_o}{v_{in}}$$

$$= \frac{1.5}{250 \times 10^{-3}} = 6$$

Example 4.3

A single-stage amplifier offering a stage gain of 7.5 dB produces an output of 0.5 V. What is the input voltage needed?

Solution Given $A_V = 7.5$ dB and $v_o = 500$ mV

From Eq. (4.5) $A_V = 20 \log\left(\frac{v_o}{v_{in}}\right)$ dB

Summary

After a detailed study of the complete concepts in this chapter, the following important inferences may be drawn:

- The conductivity of a semiconductor material lies in between that of a good conductor and an insulator.
- A covalent bond is a formed by the process of bonding of atoms through the electrons sharing between the neighbouring atoms.
- Atomic number of a semiconductor decides the number of valence electrons in its outermost orbit.
- The number of free electrons in a semiconductor material and its conductivity can be significantly increased by increasing the temperature.
- For a majority of semiconductor materials, the resistance decreases with an increase in temperature (negative temperature coefficient -α).
- An intrinsic material is a pure form of a semiconductor with zero or very low level of impurity.
- An extrinsic material is an impure form of a semiconductor with an impurity added by a process called doping.
- An *N*-type material is formed by adding a pentavalent impurity (donor atoms). In an *N*-type material, electrons are the majority carriers and holes are the minority carriers.
- A *P*-type material is formed by adding a trivalent impurity (acceptor atoms). In a *P*-type material, holes are the majority carriers and electrons are the minority carriers.
- The region near the *PN* junction that has very few carriers is called the depletion region.
- In the forward-bias region, the diode current exponentially increases with increase in the bias voltage.

Chapter-end Summary provided for each chapter for quick recap of the concepts

Guided Tour

225 Review Questions to enhance theoretical grasp of the concepts

Review Questions

1. Sketch the output waveform for the circuit of Fig. P6.1 for a sinusoidal input of $2V_{(peak)}$.
2. Sketch the output waveform for the circuit of Fig. P6.1 for a sinusoidal input of $2V_{(peak)}$ when R_{in} is increased tenfold.
3. Sketch the output waveform for the circuit of Fig. P6.1 for a sinusoidal input of $2V_{(peak)}$ when R_f is decreased tenfold.
4. For the circuit of Fig. P6.1, what is the maximum input signal that results in an undistorted output?
5. What is the role of level shifter in an op-amp? Explain.
6. What is the meaning of virtual ground? On what assumption do we arrive at this concept?
7. Sketch the output waveform for the circuit of Fig. P6.7 for a sinusoidal input of $2V_{(peak)}$.
8. Sketch the output waveform for the circuit Fig. P6.7 for a sinusoidal input of $2V_{(peak)}$ when R_{in} is increased tenfold.
9. Sketch the output waveform for the circuit of Fig. P6.7 for a sinusoidal input of $2V_{(peak)}$ when R_f is decreased tenfold.
10. For the circuit of Fig. P6.7, what is the maximum input signal that results in an undistorted output?
11. List the major functions of each block in an op-amp.
12. Obtain the operating point for a dual input, balanced output DA.
13. What is the significance of off sets in an op-amp?
14. What is the significance of input impedance in an op-amp?
15. What is the significance of output impedance in an op-amp?
16. What is the significance of slew rate in an op-amp?
17. What is the significance of CMRR in an op-amp?
18. What is the significance of PSRR an op-amp?
19. What is the significance of unity gain bandwidth 'f_U' in an op-amp?
20. What is the significance of full power bandwidth 'f_P' in an op-amp?
21. Draw the transfer characteristics for an op-amp and comment on region of uncertainty.
22. What is the role of a buffer in system design using op-amps?
23. Explain how a buffer is different from a non-inverter.
24. An even number of buffers are cascaded together. What is the output expected for a sine-wave input?
25. An integrator with a square-wave input is driving a differentiator. What is the expected output of this cascaded combination?
26. Comment whether designing an Inverting type Op-Amp Summer is complex or a Non-Inverting type Op-Amp Summer?

185 Exercise Problems to help students have practice in solving numerical problems

Exercise Problems

1. Calculate the amount of energy required to move a charge of 5 coulombs through a field set by a potential difference of 5 V.
2. A total energy of 36 eV is spent in moving a charge of x coulombs through a field set by a potential difference of 10 V. Determine the value of charge x.
3. Calculate the amount of the diode current at 10°C for a silicon diode with I_o of 200 nA and an applied forward-bias voltage of 0.6 V.
4. Repeat Problem 3 for temperatures of (i) 27°C (room temperature), and (ii) 100°C (boiling point of water).
5. Repeat Problem 3 for a temperature of 100°C assuming that Io has increased to 500 nA.
6. (a) Calculate the amount of the diode current at 20°C for a silicon diode with I_o = 200 nA and a reverse-bias potential of 10 V.
   (b) Comment on the result critically.
7. (a) In the reverse-bias region, the saturation current of a silicon diode is about 0.1 mA at a temperature of 20°C. Determine its approximate value if the temperature is doubled.
   (b) Check whether the theory 'current doubles for every 10°C rise in temperature' holds good in the answer to part (a).
8. If the reverse-bias potential for a diode changes from 10 V to 100 V, what will be the percentage change in the reverse saturation current of the diode?
9. Determine the forward voltage drop across a diode at temperatures of 27°C, 100°C and 125°C given a diode current of 10 mA.
10. Determine the static or dc resistance of a diode whose *VI* characteristics is given in Table P10 below at a forward current of 2 mA.

Table P10

Sl. No.	V_D in volts	I_D in mA
1	0	0
2	0.1	0.01
3	0.2	0.02
4	0.3	0.04
5	0.4	0.5
6	0.5	1.0
7	0.6	10.0
8	0.7	28
9	0.75	59
10	0.78	99

11. Determine the dynamic or ac resistance of a diode whose *VI* characteristics is given in Table P10 above around a forward current of 2 mA.
12. Draw the piecewise linear equivalent circuit for the diode in Problem 10.
13. Determine the dynamic (ac) resistance of the diode of Fig. P1.13 at a forward current of 10 mA using the equation $r_{ac} = (\Delta V_D/\Delta I_D)\Omega$.

450 Multiple-Choice Questions to practice for competitive examinations

Multiple-Choice Questions

1. All electronic circuits for their working and operation require
   (a) ac source (b) dc source (c) both (a) and (b) (d) no source
2. The electronic circuit that generates dc power from an available ac source is
   (a) power supply (b) amplifier (c) oscillator (d) all the above
3. A power-supply unit consists of
   (a) a rectifier (b) a filter (c) a regulator (d) all the above
4. The output of which unit of a power supply contains maximum dc components?
   (a) A rectifier (b) A transformer (c) A filter (d) None
5. A transformer in a power-supply unit necessarily
   (a) isolates high-tension unit from low-tension units
   (b) steps down i/p
   (c) amplifies i/p
   (d) both (a) and (b)
6. The turns ratio in a transformer is related to primary and secondary parameters through
   (a) $N_1/N_2 = I_1/I_2 = V_1/V_2$ (b) $N_1/N_2 = I_2/I_1 = V_2/V_1$
   (c) $N_1/N_2 = I_2/I_1 = V_1/V_2$ (d) none
7. The rectifier of a power-supply unit is also called
   (a) a converter (b) a transformer (c) an inverter (d) none
8. The output of a rectifier in a power-supply unit is
   (a) a pure ac (b) a pure dc (c) a pulsating dc (d) none
9. The unit in a power supply that minimises the ripples is
   (a) a rectifier (b) a transformer (c) a regulator (d) a filter
10. The ripple factor in a rectifier output is the signal ratio of
    (a) output ac to output dc (b) output dc to output ac
    (c) output ac to input ac (d) none
11. The unit in a power supply that provides constant dc against certain variations is
    (a) a rectifier (b) a transformer (c) a filter (d) a regulator
12. The conversion efficiency of a full-wave rectifier output is ideally
    (a) 0.48 (b) 1.21 (c) 0.812 (d) 0.406
13. The TUF in a half-wave rectifier is ideally
    (a) 0.48 (b) 1.21 (c) 0.286 (d) 0.693

Quiz Questions (Short-answer Questions)

Chapter 1: Semiconductor Physics and *PN* Junction

1.1 **Classify solid materials based on electrical properties**

Ans Solid materials may be classified into the following three types: (i) Insulators, (ii) Conductors, and (iii) Semiconductors.

1.2 **What do you mean by atomic number?**

Ans The number of protons or electrons in an atom is called the "atomic number".

1.3 **Give the atomic number for silicon, carbon and aluminium.**

Ans The atomic number for silicon is 14, for carbon it is 5, and for aluminium it is 13.

1.4 **What do you mean by forbidden energy gap?**

Ans The energy gap between the conduction band and the valence band is called 'forbidden energy gap'. In conductors this gap is zero; in insulators, it is too high; and in semiconductors, it is reasonably small.

1.5 **Give the forbidden-energy-gap value for silicon and germanium**

250 Short-Answer Questions for easy recap of definitions and terms

Semiconductor Physics and *PN* Junction

1

Goals and Objectives

Upon completion of this chapter, the reader of the book is expected to

- Understand the importance of electronics in everyday life
- Review the basics of atomic structure and energy levels of different materials
- Understand the general characteristics of important semiconductor materials like silicon, germanium, gallium arsenide, etc
- Understand the principle of electron and hole conduction
- Differentiate between *N*-type and *P*-type semiconductor materials
- Understand the characteristics of a *PN* junction under unbiased, forward-biased and reverse-biased conditions
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- Understand the reading and interpretation of diode-specification sheets
- Do physical interpretation of concepts with a good number of examples provided
- Feel confident in moving to the next chapter on **diode applications**

1.1 INTRODUCTION—ELECTRONICS AND ITS EVOLUTION

Almost every object we touch in our day-to-day life carries **electronics** in it. Be it a television, an air cooler, a refrigerator, a microwave oven, or an automobile, there is electronics involved in it. This means that electronics has become part and parcel of everyday life. It is important to note that the fundamental principles of electronics change very little over time. With the advances in technology, systems are becoming incredibly smaller while their speed of operation is increasing remarkably. Most devices today are simply an improvement over their predecessors rather than a new development. The major changes have been in the understanding how these devices work, their full range of capabilities and in improved methods of teaching, the **fundamentals** associated with them. The device miniaturisation in the field of electronics in recent years leaves us to wonder about its limits. Starting with gigantic vacuum tubes way back in the 1930s, tremendous developments have taken place till today. Invention of solid-state devices like semiconductor diodes in the early 1940s, bipolar junction transistors in 1945 and the field effect transistor in 1955, clearly indicate device shrinking. Then started the era of Integrated Circuits (ICs)—analog ICs such as Op-Amps, timers, phase-locked loops—and these are all results of continued innovations. Digital ICs such as basic gates, combinational circuits like multiplexers, de-multiplexers, encoders, decoders, Arithmetic Logic Units (ALUs), etc; and sequential circuits like flip-flops, counters, shift registers, memories, etc. have also been developed. Continuous developments started from ALU, later a microprocessor (μP) which is a system built around the ALU, then a microcontroller (μC) which is a system built around the μP, then an Application Specific IC (ASIC) and finally a System-On-Chip (SOC). Complete systems now appear on wafers that are much smaller than the single element of earlier networks. The first integrated circuit was developed in 1958 which contained only a few transistors on it, but today, processors like Intel's Dual Core and Extreme quad-core have approximately 410 million transistors. Later, in the early 1960s, the microprocessor was developed. From then, a lot of developments resulted in microcontrollers, single-board micro-computers, ASICs and System-On-Chip (SOC). Today, we see System-On-Package (SOP), System-On-Board (SOB), System-On-Network (SON), etc. where a huge amount of functionality is packed into a small wafer. Therefore, we have obviously reached a point where the primary purpose of the integration is simply to provide some means to miniaturise the device or the system and to provide a mechanism for further enhancement of the network based on system requirements. On the surface, it appears that miniaturisation is limited by three factors: the quality of the semiconductor material used, the network design technique and the limits of the manufacturing and processing equipments. However, recent trends and developments in Very Large Scale Integration (VLSI) technology and Ultra Large Scale Integration (ULSI) technology reveal that there are other important limiting factors also; they are connectivity, path capacitances, path resistances and many more.

Table 1.1 Evolution of electronics

Sl. No.	Device	Year	Inventor
1	Vacuum-tube diode	1904	J A Fleming
2	Junction diode	Early 1940s	Russel Ohl
3	Junction transistor	1945	William Shockley, John Bradeen and Walter H Brattain
4	Field Effect Transistor (FET)	1955	Ian M. Ross and G C Dacey
5	Integrated Circuit (IC)	Late 1950s	Jack St. Kilby

Diode Applications

2

Goals and Objectives

Upon completion of this chapter, the reader is expected to

- Recall all the basic concepts of conventional *PN* junction diodes from Chapter 1
- Understand the concept of diode load line and its analysis
- Understand the basic block diagram of a power-supply unit
- Understand the importance of each unit in a power-supply unit
- Understand the process of rectification and classify rectifiers
- Understand the working of half-wave and full-wave rectifiers
- Understand performance parameters like ripple factor and efficiency of rectifiers
- Understand performance parameters like form factor and TUF of rectifiers
- Compare different types of rectifiers and choose the best for an application
- Understand the need and the process of filtering in a power-supply unit
- Understand the working of different forms of filters
- Understand the importance of minimising ripple factor in the rectifier output
- Compare different types of filters and choose the best for an application
- Understand the need and process of regulation in a power-supply unit
- Understand the working of a Zener voltage regulator
- Understand performance-parameter voltage regulation in regulators
- Understand the limitations of a Zener voltage regulator
- Understand the need and process of a voltage multiplier circuit
- Understand the need and process of a clipping circuit
- Be able to predict the output response of a clipper circuit for a given input
- Understand the need and process of a clamping circuit
- Be able to predict the output response of a clamper circuit for a given input
- Become familiar with some basic gate circuits using diodes
- Become familiar with some other important applications of diodes
- Feel confident in moving to the next chapter, i.e. BJTs

2.1 INTRODUCTION

In Chapter 1, the construction, *VI* characteristics and energy-band diagrams of various important semiconductor diodes were introduced. Based on the knowledge gathered from Chapter 1, you will be able to study a few of the chapters to come in this text. In Chapter 2, we will develop and understand various applications of these diodes and in particular we will design and develop important applications of a conventional *PN* junction diode such as a rectifier, a voltage multiplier, a clipper, a clamper, etc. The concepts used in analysis of the circuits to be introduced in this chapter are very important and prove to be fundamentals. Once we understand the basic behaviour of a device, it is then very easy to examine and verify the function and response in a variety of configurations. Now, with the basic knowledge of the behaviour and characteristics of a diode, we will study and examine some of the most important applications such as rectifiers, regulators, voltage multipliers, wave shaping circuits (clippers and clampers), etc. In the analysis of these electronic circuits, we can use either the actual characteristics or an approximate model for the device without much differences in the results obtained. In the beginning, we will include the actual characteristics of the diode in order to clearly demonstrate how the device characteristics and the circuit parameters are interconnected. After gaining confidence in the results so obtained, the approximate piecewise linear model can be employed to verify the results. The results obtained using the actual characteristics may be at the most slightly different from those obtained using a series of approximations. This is because the characteristics obtained for a device will certainly have a slight deviation from that of an actual device given in the specification sheet. Also, the other elements of the network like resistors, supply sources, etc. do have some tolerance levels mentioned for them and hence a response obtained using an approximate models readily acceptable for most practical applications.

This chapter starts with an introduction to power-supply unit. In Section 2.2, a power-supply block diagram is presented; it contains various blocks that form any basic power supply. Later, in the following sections, each block from the power supply is discussed thoroughly and the related design aspects are also presented. Further, other diode applications such as voltage multipliers, wave-shaping circuits like clipping circuits and clamping circuits, short-circuit protections, etc. are considered. The chapter concludes with a summary.

2.2 POWER-SUPPLY BLOCK DIAGRAM

A power-supply unit basically converts the available input ac signal into the dc signal that is much needed for all electronic circuits, devices and applications. The block diagram of a conventional power supply is presented in Fig. 2.1 and consists of blocks for rectification, smoothening the rectified signal and regulation.

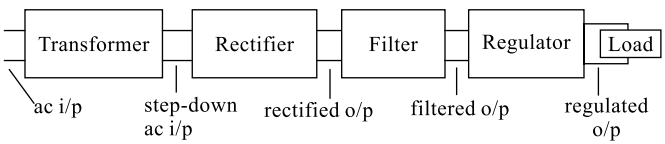
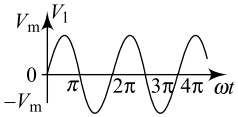
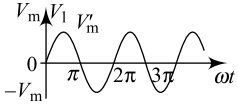
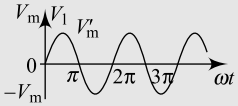
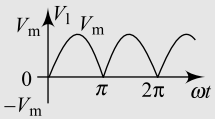
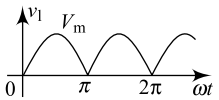
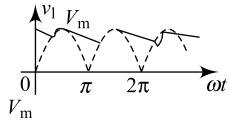
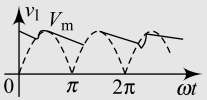
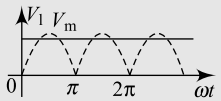


Fig. 2.1 Power-supply block diagram

Table 2.1 illustrates the complete input and output waveforms for various blocks in a power supply. It can be observed here that a pure and stable dc output is obtained at the output of the regulator.

Table 2.1 Waveforms at various points in a power supply.

Sl. No	Block Name	Input Waveform	Output Waveform	Remarks
1	Transformer			$V_m' < V_m$ if $N_2 < N_1$ and $V_m' > V_m$ if $N_2 > N_1$ (depends on the turns ratio).
2	Rectifier			For HWR, there will be only half-rectified output.
3	Filter			Depending on the filter type, the output may slightly vary.
4	Regulator			Amount of dc output depends mainly on filter and regulation of regulator.

1. Transformer

Most electronic circuits require considerably lower power and voltage. The transformer used here serves to convert the ac line voltage available to a voltage level that is more appropriate to the needs of the circuit under design. And also, the transformer provides an electrical isolation between the ac line and the circuit being powered, thereby avoiding any risk of shocks, which is an important safety consideration. The output of the transformer is still an ac signal and now an appropriate magnitude for the circuit to be powered is obtained by using a step-down transformer. The load voltage required decides the transformer secondary voltage and is obtained by using a suitable turns ratio (ratio of primary to secondary turns) for the transformer. The number of primary turns N_1, the number of secondary turns N_2, the primary current I_1, the secondary current I_2, the primary voltage V_1 and the secondary voltage V_2 in a transformer are related to each other through the following relationship:

$$\frac{N_1}{N_2} = \frac{V_1}{V_2} = \frac{I_2}{I_1} \tag{2.1}$$

2. Rectifier

The stepped-down signal from the transformer is then fed to a rectifier which is the next block in the power-supply unit. A rectifier is a circuit that converts the input ac (bipolar) signal into a dc (unipolar) signal and is available in several different forms. The output of the rectifier is a pulsating dc with a lot of variations called **ripples**. These ripples can be minimised and the output can be smoothened by using a circuit called a **filter**. This is clearly indicated in the waveforms shown in Fig. 2.1.

3. Filter

The output from the rectifier is still not suitable to power the actual load circuit because it is a pulsating dc. The pulsations typically vary from 0 volts to the peak output voltage of the transformer V_m. This being very undesirable, a smoothing circuit called filter is used and the ripples are minimised. A filter is a circuit that minimises the amount of ac components from the rectified dc signal and hence improves the

quality of the output signal. Several forms of filters are commercially available and some of the *RLC* filters will be discussed in this text. *RLC* filters are passive filters and are very cost-effective to implement. The pulsations are now reduced to a very small value as indicated in the diagram.

4. Regulator

The pulsating dc output from the rectifier can be filtered to an extent where the ripples are negligible and the output almost looks like a straight line. This is what is desirable for all applications; however, this dc output voltage is very sensitive to any fluctuations in the input-line voltage or the output load demand and needs a measure to control this fluctuation. The circuit used to stabilise such a fluctuation is called a regulator that follows the filter as indicated in the block diagram. Several forms of regulators are commercially available and we will consider only a simple Zener voltage regulator.

2.3 LOAD-LINE ANALYSIS

The circuit shown in Fig. 2.2 is a simple diode configuration in which the circuit elements are a voltage source *V* and a resistor *R*. It will be used to describe the analysis of a diode circuit using its actual characteristics. After the analysis (solving for different voltages and currents), an approximate model can be derived and we can replace the actual characteristics by this approximate model for the diode and compare solutions. Solving the circuit of Fig. 2.2(a) means finding the current and voltage levels that will satisfy both the characteristics of the diode and the chosen network parameters at the same time.

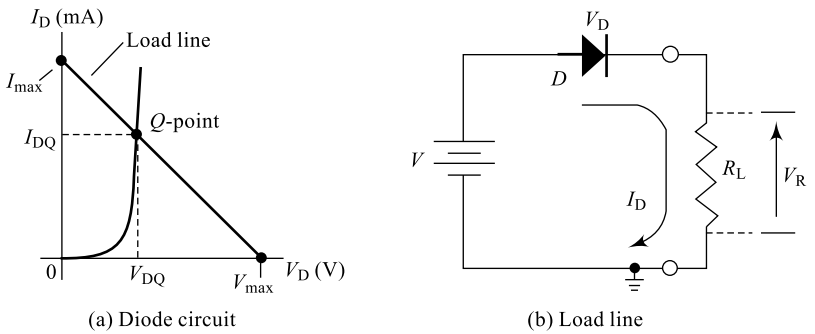


Fig. 2.2 Load-line analysis

In Fig. 2.2, the diode *VI* characteristics are placed on the same set of axes as that of the straight line defined by the circuit parameters. The straight line is drawn by considering two points V_{max} and I_{max} based on the circuit conditions. V_{max} corresponds to a point where the circuit voltage is obtained by using Kirchhoff's voltage law given by Eq. (2.2) and it is $V_{max} = V$ which is possible only when V_D is zero or in other words when R_f is zero. Similarly, I_{max} corresponds to a point where the circuit current is given by V/R (using Ohm's law) which is possible only when V_D is zero or in other words when R_f is zero as given by Eq. (2.3). Now, a straight line can be drawn joining these two points and every point on this line corresponds to an ordinate representing a voltage and a corresponding circuit current. This line is called load line because every point on this line represents a load and a corresponding voltage and the analysis using this line is, therefore, called **load-line analysis**. Applying Kirchoff's voltage law to the circuit of Fig. 2.2(a), we can write the following relations:

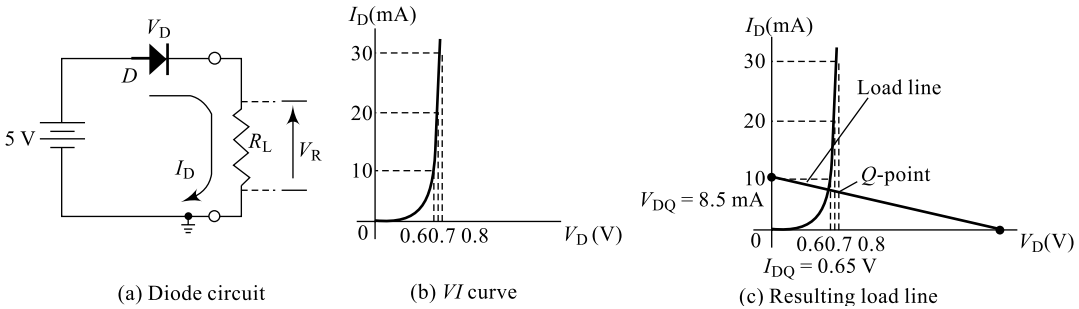
$$V = V_D + V_R \tag{2.2}$$

$$V = I_D R_f + I_D R_L \tag{2.3}$$

In Fig. 2.2(a), the external dc supply connected establishes a conventional current I_D in the direction indicated in the diagram. The direction of this current or the applied voltage forward biases the diode resulting in a voltage across the diode V_Y (approximately around 0.7 V for Si diode). The intersections of the load line on the characteristics of Fig. 2.2 can be determined by applying Kirchhoff's voltage law. The two variables of Eq. (2.2) and Eq. (2.3), V_D and I_D, are the same as the diode axis variables of Fig. 2.2(b). This similarity permits plotting Eq. (2.3) on the same characteristics of Fig. 2.2(a). The intersections of the load line on the characteristics can easily be determined. If we set the voltage $V_D = 0$ (i.e. $R_f = 0$)in Eq. (2.3) and solve for I_D, we have the magnitude of I_D on the vertical axis as given by $I_{max} = V/R_L$. Similarly, if we set the current $I_D = 0$ in Eq. (2.3) and solve for V_D, we have the magnitude of V_D on the horizontal axis as given by $V_D = V = V_{max}$. A straight line drawn between the two points will define the load line as depicted in Fig. 2.2(b) and any change in the level of R (the load), the intersection on the vertical axis will change. The result will be a change in the slope of the load line. The current I_D is in reality, the current through the circuit, i.e. through a series-connected diode and the load resistor of Fig. 2.2(a). The point of operation is called the **quiescent point** (**Q-point**) or **operating point**. The solution obtained at the intersection of the two curves is the same as would be obtained by solving a simultaneous mathematical solution. The load-line analysis described above provides a solution with a minimum effort.

Example 2.1

Assuming a silicon diode, for the diode circuit shown in Fig. 2.3, determine the operating point Q; given the value of load resistor as 500 Ω.



(a) Diode circuit (b) *VI* curve (c) Resulting load line

Fig. 2.3 For Example 2.1

Solution Using Eq. (2.3) and assuming $R_f = 0$, we get

$$I_{max} = \frac{V}{R_L} = \frac{5}{500}$$

$$I_{max} = 10 \text{ mA}$$

Similarly, using Eq. (2.2) with $V_D = 0$, $= V_{max} = 5$ V

Plotting the load line on the given *VI* curve, the point of intersection can be obtained; this results in the Q-point

$$V_{DQ} = 0.65 \text{ V} \quad \text{and} \quad I_{DQ} = 8.5 \text{ mA}$$

as indicated in Fig. 2.3(c).

Note:

1. Since ideal diode is assumed for approximate analysis, whether it is a Si or Ge diode will not really matter.
2. Now, with $V_{DQ} = 0.65$ V and $I_{DQ} = 8.5$ mA, the diode resistance is given by

$$R_f = \frac{V_{DQ}}{I_{DQ}} = \frac{0.65}{8} \cdot 5 \text{ mA} = 76.47\ \Omega$$

This will slightly tilt the load line and this tilt is negligible.

Example 2.2

Assuming a silicon diode, for the diode circuit shown in Fig. 2.4, determine the values of V_D, I_D and V_R given the value of the load resistor as 1800 Ω.

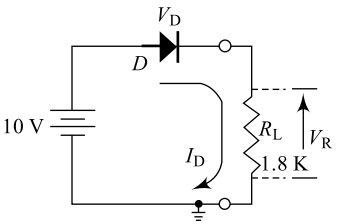


Fig. 2.4 For Example 2.2

Solution With the applied source of 10 V, the diode will be forward biased and being a silicon diode

$$V_D = 0.7 \text{ V}$$

Now, using Eq. (2.2), we can write

$$V_R = V - V_D$$
$$= (10 - 0.7) \text{ V} = 9.3 \text{ V}$$

Now, using Eq. (2.3), we can write

$$V_R = I_D \times R_L$$

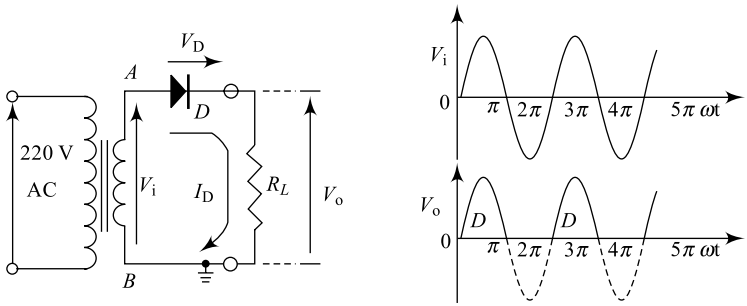
i.e. $$I_D = I_R = \frac{V_R}{R_L} = \frac{9.3}{1800} = 5.17 \text{ mA}$$

2.4 RECTIFIERS: HALF-WAVE RECTIFIER

As shown in Fig. 2.1, the first block in the power-supply unit is a rectifier or a converter. A **rectifier** is a circuit that converts the ac (bipolar) signal at the input into a dc (unipolar) signal at the output. Rectifiers can be broadly classified into two types: single-phase rectifiers and polyphase rectifiers; controlled rectifiers and uncontrolled (conventional) rectifiers. A polyphase rectifier converts each phase of the ac signal into a dc signal; it is beyond the scope of this text and hence will not be discussed; however, controlled rectifier basics will be discussed in Chapter 10. In this chapter, single-phase rectifier types, its working, performance analysis and design issues are completely discussed. Rectifiers (single-phase and polyphase) can be further classified into two types: half-wave rectifiers and full-wave rectifiers. A **Half-Wave Rectifier** (**HWR**) converts only one-half cycle (either positive or negative) of the input bipolar ac into a dc output. The circuit diagram and the input/output waveforms of a half-wave rectifier are shown in Fig. 2.5. The circuit contains a transformer that steps down the input ac magnitude depending on the requirement and provides the necessary isolation avoiding any risk of shocks. The turns ratio for the transformer decides the magnitude of the secondary voltage V_i. R_L represents the load for the circuit and it is assumed to be a pure resistor for simplicity and ease of analysis.

Working

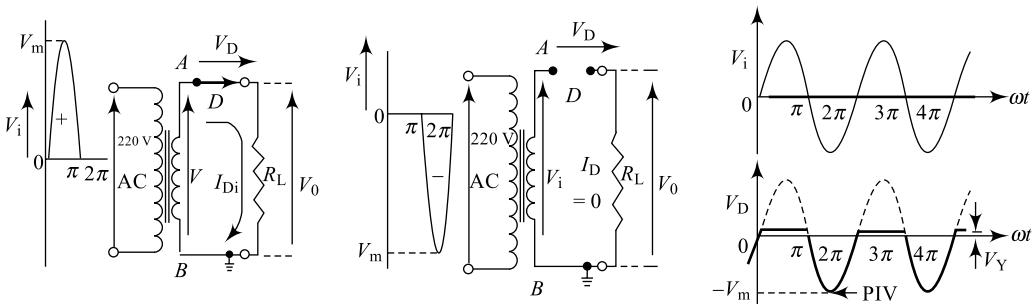
Let $V_i = V_m \sin \omega t$ be the input signal at the transformer secondary; it is a sinusoidal signal with maximum amplitude V_m. During the positive half-cycle of the input, the point *A* being positive with respect



(a) Circuit diagram (b) Input/output waveforms

Fig. 2.5 Half-wave rectifier

to the point *B*, the diode will be forward biased. Diode starts conduction resulting in a current I_D flowing through the load resistor R_L and the diode continues to conduct for the entire positive half-cycle, i.e. from $\omega t = 0$ to Π. During the negative half-cycle of the input, the point *A* will be negative with respect to the point *B* and the diode will be reverse biased. The diode stops conduction and hence there is no current flowing through the load R_L for the entire negative half cycle. Thus, between $\omega t = \Pi$ to 2Π, the circuit current is zero and the output V_0 is also zero as indicated in Fig. 2.5(b). It can, therefore, be observed that for one cycle of input, there is a current flowing for one half-cycle, hence the name half-wave rectifier. This can be further substantiated using the equivalent circuits shown in Fig. 2.6. During positive half-cycle, the diode is a closed switch and the voltage across the conducting diode is simply equal to V_Y. Similarly, during the negative half-cycle, the diode is an open switch and the voltage across the nonconducting diode is simply equal to $-V_i$. During the negative half-cycle of the input, the open-circuited diode observes a reverse voltage which is following the input voltage and has its maximum value V_m. This maximum reverse voltage across the diode is known as the **Peak Inverse Voltage** (PIV) and is indicated in Fig. 2.6(c). It is essential to note that PIV rating for a diode will be available in the manufacturer's specification sheet, but the circuit in which the diode is working will decide the maximum value of PIV that is appearing across the reverse biased diode. This value should be well below the specification in the data sheet so that the diode is not damaged. Thus, the diode used for a half-wave rectifier should have a PIV rating that is greater than or at least equal to V_m so that the device is not damaged.



(a) Positive half-cycle (b) Negative half-cycle (c) V_D waveform

Fig. 2.6 Half-wave rectifier equivalent circuits

$$\text{PIV} = V_m \tag{2.4(a)}$$

Looking at the output waveform, it is clear that for every cycle of the input, there are two cycles of output and hence we have the output frequency

$$f_O = f_i \tag{2.4(b)}$$

Now, the performance of a half-wave rectifier can be determined by measuring various parameters such as the rectification efficiency, ripple factor, transformer utilisation factor, form factor, etc. The estimation of these parameters is done in the following sections from 2.4.1 to 2.4.6.

2.4.1 Rectification Efficiency of HWR (η_{HWR})

One of the important parameters that can be used to measure the performance of a rectifier is the conversion efficiency. It speaks about the ability of a rectifier in converting an ac input into useful dc output. The rectification efficiency of a rectifier is defined as the ratio of the dc power at the output to the ac power at the input. It is represented by the Greek letter η.

$$\eta = \frac{\text{dc power output}}{\text{ac power input}} \times 100\%$$

$$\eta = \frac{P_{dc}\,\text{output}}{P_{ac}\,\text{input}} \times 100\%$$

$$\eta = \frac{I_{dc}^2\,(R_L)\text{ at the } O/P}{I_{rms}^2\,(R_L + R_f + R_S)\text{ at the } I/P} \times 100\% \tag{2.5}$$

where R_f is diode forward resistance and R_s is transformer secondary winding resistance; practically, $R_S << R_f$ and can be neglected.

Average Output Voltage

Now, the average output voltage or the dc output voltage, across the load, is obtained by integrating the output voltage waveform between 0 and 2Π and averaging it over 2Π (the repetitive period).

$$V_{o(avg)} = V_{o(dc)} = \frac{1}{2\Pi}\int_0^{2\Pi} V_o\, d\omega t$$

Since the diode is assumed to be ideal, V_o is replica of V_i and hence;

$$V_{o(dc)} = \frac{1}{2\Pi}\int_0^{2\Pi} V_i\, d\omega t$$

$$= \frac{V_m}{2\Pi}\left[\int_0^{\Pi}\left[\sin \omega t/2\; d\Pi + \int_{\Pi}^{2\Pi} \sin \omega t\; d\omega t\right]\right]$$

$$= \frac{V_m}{2\Pi}[-\cos \omega t]_0^{\Pi} = \frac{V_m}{(2\Pi)(1+1)}$$

$$V_{o(dc)} = \frac{V_m}{\Pi} = 0.318\, V_m = 0.45\, V_s \tag{2.6}$$

Here, V_S is the transformer secondary rms voltage (rated voltage). Similarly, the average or the dc current through the load is given by integrating the output current between 0 and 2Π and averaging it over 2Π.

$$I_{o(dc)} = \frac{1}{2\Pi}\int_0^{2\Pi} I_o \, d\omega t$$

$$I_{o(dc)} = \frac{I_m}{\Pi} = 0.318\, I_m = 0.45\, I_s \tag{2.7}$$

Here, I_S is the transformer secondary rms current (rated current).

For a half-rectified sine wave, we can calculate the rms value of output voltage at the load resistance as below;

$$V_{(rms)} = \frac{1}{2\Pi}\sqrt{\int_0^{2\Pi} (V_i)^2 \, d\omega t}$$

$$V_{(rms)} = \frac{1}{2\Pi}\sqrt{\int_0^{2\Pi} (V_m \sin \omega t)^2 \, d\omega t}$$

$$V_{(rms)} = \frac{V_m}{2\Pi}\sqrt{\int_0^{2\Pi} (1 - \cos 2\omega t)\, d\omega t}$$

$$V_{(rms)} = \frac{V_m}{2} \tag{2.8(a)}$$

Similarly, the rms value of output current through the load resistance is

$$I_{(rms)} = \frac{I_m}{2} \tag{2.8(b)}$$

Using Eq. (2.7) and Eq. [2.8(b)] in Eq. (2.5), the final expression for efficiency can obtained:

$$\eta = \frac{\dfrac{[I]_m^2}{[\pi]}(R_L) \text{ at the } o/p}{\dfrac{[I]_m^2}{[2]}(R_L + R_f) \text{ at the } i/p} \times 100\%$$

$$\eta = \frac{4}{\pi^2\left(1 + \dfrac{R_f}{R_L}\right)} \times 100\% \tag{2.9}$$

But, $R_f << R_L$ and hence can be neglected; this results in a maximum efficiency

$$\eta_{max} = \frac{4}{n^2} \times 100\% = 40.6\% \tag{2.10}$$

Equation (2.10) clearly indicates that the maximum achievable conversion efficiency is only 40.6% in HWR and hence this rectifier is not a better choice for many applications.

2.4.2 Ripple Factor of HWR (γ_{HWR})

Another important parameter that can be used to measure the performance of a rectifier is the ripple factor. It speaks about the quality of the dc output of a rectifier. The ripple factor of a rectifier is defined as the ratio of rms value of ac component in the output to the dc component present in the output. It is represented by the Greek letter γ.

$$\gamma = \frac{\text{rms value ac component in output}}{\text{Actual dc component in output}} \times 100\%$$

$$\gamma = \frac{V_{ac}\,(O/P)}{V_{o\,dc}\,\text{dc}\,(O/P)} \times 100\% \tag{2.11}$$

From the basics of electrical sciences, we can write the relationship between rms value, average value and the ac value of a voltage signal as below:

$$V_{rms}^2 = V_{ac}^2 + V_{dc}^2$$

$$V_{ac} = V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2} \tag{2.12}$$

Substituting Eq. (2.6) and Eq. (2.12) in Eq. 2.11, we obtain

$$\gamma = \sqrt{\frac{V_{rms}^2}{V_{o\,dc}^2} - 1} \tag{2.13}$$

Substituting Eq. (2.6) and Eq. (2.13) in Eq. (2.12), we obtain

$$\gamma = \sqrt{\left(\frac{V_m/2}{V_m/\pi}\right)^2 - 1}$$

$$\gamma = \sqrt{\left[\left(\frac{\pi}{2}\right)^2 - 1\right]}$$

$$\gamma = 1.21 \tag{2.14}$$

Thus, Eq. (2.14) obtained for ripple factor clearly indicates that the output of a half-wave rectifier is of poor quality since it contains more ac components than the required dc components. Once again, this result makes the HWR unsuitable for many applications.

2.4.3 Transformer Utilisation Factor of HWR (TUF_{HWR})

Another very important parameter that can be used to analyse the performance of a rectifier circuit is the transformer utilisation factor, popularly called the TUF. A TUF indicates the ability of the rectifier circuit in utilising the available transformer secondary power. It is defined as the ratio of the dc power output to the rated ac power for the transformer secondary.

$$\text{TUF} = \frac{P_{dc}\,(O/P)}{P_{ac}\,(\text{rated})} \times 100\%$$

The rated voltage of the transformer secondary is given by $V_{S(rated)} = \frac{V_m}{\sqrt{2}}$

But, the rms current drawn actually from the winding is only $I_{rms} = \frac{I_m}{2}$

$$\text{TUF} = \frac{I_{dc}^2 \times R_L}{V_{rms} \times I_{rms}} \times 100\%$$

$$= \frac{\frac{I_m^2}{\Pi^2} \times R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{2}} \times 100\%$$

$$= \frac{\frac{V_m^2}{\Pi^2} \times \frac{1}{R_L}}{\frac{V_m}{\sqrt{2}} \times \frac{V_m}{2R_L}} \times 100\% = \frac{2\sqrt{2}}{\pi^2} \times 100\%$$

$$\text{TUF} = 0.287 \tag{2.15}$$

Thus, Eq. (2.15) obtained for transformer utilisation factor clearly indicates that in a half-wave rectifier, the utility of the available transformer secondary power is very poor and is only 28.7%. Hence, it is very essential to look for an alternate form of rectifier circuit that best utilises the available transformer secondary power.

Example 2.3

In the circuit of Fig. 2.5(a), if the transformer has a turns ratio of 10:1, find the transformer secondary voltage and rectification efficiency. The Si diode used is assumed to have a forward resistance of 12 Ω and load resistance is 2 kΩ.

Solution Using Eq. (2.1), we can write

$$\frac{N_1}{N_2} = \frac{V_1}{V_2} = \frac{I_2}{I_1}$$

$$\therefore \quad V_2 = \frac{N_2}{N_1} \times V_1 = \frac{1}{10} \times 220 = 22 \text{ V}$$

Using Eq. (2.9), we can write

$$\eta = \frac{4}{\pi^2 \left(1 + \frac{R_f}{R_L}\right)} \times 100\%$$

$$= \frac{4}{\pi^2 \left(1 + \frac{12}{2000}\right)} \times 100\%$$

$$\eta = 40.287\%$$

2.4.4 Form Factor of HWR (F_{HWR})

Form factor of a rectifier can be defined as the ratio of the rms value of the signal at the output to the average value or dc value of the signal at the output. Mathematically, a form factor can, therefore, be given by the equation

$$F = \frac{V_{\text{rms}}(O/P)}{V_{\text{dc}}(O/P)} \times 100\%$$

$$F = \frac{\left(\frac{V_{\text{m}}}{2}\right)}{\left(V_{\text{m}}\frac{V_{\text{m}}}{\Pi}\right)} \times 100\% = \frac{\Pi}{2} \times 100\% = 1.57 \times 100\% \tag{2.16}$$

A form factor is related to ripple factor through the equation $\gamma = \sqrt{F^2 - 1}$

2.4.5 Peak Factor of HWR

Peak factor in an HWR is given as the ratio of peak value of the signal to its rms value.

$$\text{Peak factor} = \frac{\text{Peak value } (V_{\text{m}})}{\text{rms value } (V_{\text{s}})} \times 100\% = \frac{V_{\text{m}}}{\left(\frac{V_m}{2}\right)} \times 100\%$$

$$\text{Peak factor} = 2 \times 100\% \tag{2.17}$$

where V_{max} is the maximum voltage value of the ac supply and V_{S} is the rms value of the supply voltage.

2.4.6 Regulation of HWR

The variation of the dc output voltage with respect to the dc load is termed voltage regulation for a rectifier. It can be defined as the ratio of change in output voltage from no-load condition to full-load condition expressed as a percentage with respect to the full-load voltage.

$$\text{Regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{full load}}} \times 100\% \tag{2.18}$$

In a half-wave rectifier, the variation of V_{dc} as function of I_{dc} can be given as follows;

$$I_{\text{dc}} = \frac{I_{\text{m}}}{\Pi} = \frac{\left(\frac{V_{\text{m}}}{R_{\text{L}} + R_{\text{f}}}\right)}{\Pi}$$

Solving the above equation for $V_{\text{dc}} = I_{\text{dc}} \times R_{\text{L}}$, we get

$$V_{\text{dc}} = \frac{V_{\text{m}}}{\Pi} - I_{\text{dc}} \times R_{\text{f}} \tag{2.19}$$

$$\text{Regulation} = \frac{\left[\frac{V_m}{\Pi}\right] - \left[\frac{V_m}{\Pi} - I_{dc} \times R_f\right]}{\left[\frac{V_m}{\Pi} - I_{dc} \times R_f\right]} \times 100\%$$

$\therefore$

$$\text{Regulation} = \left[\frac{R_s + R_f}{R_L}\right] \times 100\% \qquad (2.20)$$

It is interesting to note that in Fig. 2.5(a), the HWR, the positive half-cycle of the input is rectified and appears at the output while the negative half-cycle is removed from the output. In the circuit provided, reversing the direction of diode results in a half-rectified output which is for the negative half-cycle of input. Here, the positive half-cycle of the input is removed from the output and produces a negative output. This is indicated in Fig. 2.7; where the diode D_1 results in a conventional output and the diode D_2 results in an inverted form of output.

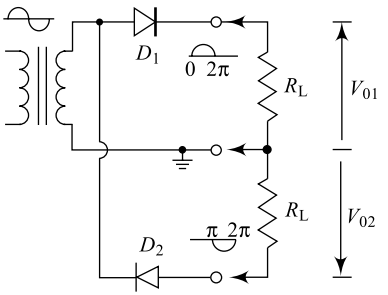


Fig. 2.7 Two half-wave rectifiers forming an FWR

Example 2.4

Calculate the dc current (I_{dc}) flowing through a 100 Ω resistor and the power consumed by the load connected to a 240 V single-phase half-wave rectifier as shown in Fig. 2.5(a).

Solution Using Eq. (2.6), we can write

$$V_{0(dc)} = \frac{V_m}{\Pi} = 0.318\ V_m = 0.45\ V_s$$

$$V_{0(dc)} = 0.45\ V_s = 0.45 \times 240$$

$$V_{0(dc)} = 108\ \text{V}$$

Similarly, $$I_{0(dc)} = \frac{V_{dc}}{R_L} = \frac{108}{100} = 1.08\ \text{A}$$

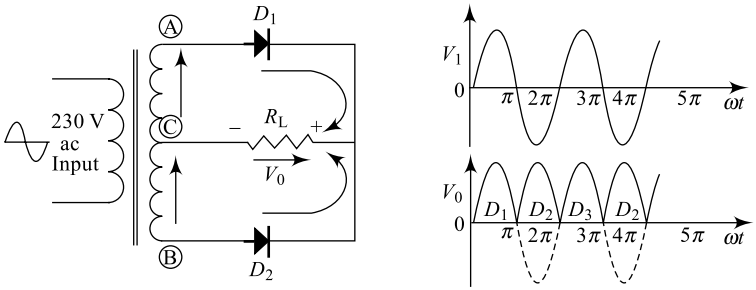
Power $$P = I^2 R_L$$

$$= 1.08^2 \times 100 = 116\ \text{W}$$

2.5 RECTIFIERS: CENTRE-TAPPED FULL-WAVE RECTIFIER

It is observed from Eq. (2.6) that the dc level in the output of an HWR is merely $0.45V_S$ and from Eq. (2.14), the ripple factor is 1.21. Both these results indicate a need for improving the dc level and reducing the ac components. The dc level obtained from a sinusoidal input can be improved 100% using another circuit called full-wave rectifier. A **Full-Wave Rectifier** (**FWR**) converts the entire input bipolar ac (both positive and negative half-cycles of the input) into a dc output. The circuit diagram and the input/output waveforms of a full-wave rectifier are shown in Fig. 2.8. The circuit contains a transformer that steps down the input ac magnitude depending on the requirement and provides the necessary isolation avoiding any risk of shocks. Unlike in the case of an HWR, here the transformer is a centre-tapped one and thus provides two ac signals at the secondary named V_1 and V_2. The two signals

are almost equal in magnitude and exactly phase opposite to each other ($V_1 = -V_2$). The turns ratio for the transformer decides the magnitude of the secondary voltages V_1 and V_2. R_L represents the load for the circuit and it is assumed to be a pure resistor for simplicity and ease of analysis.

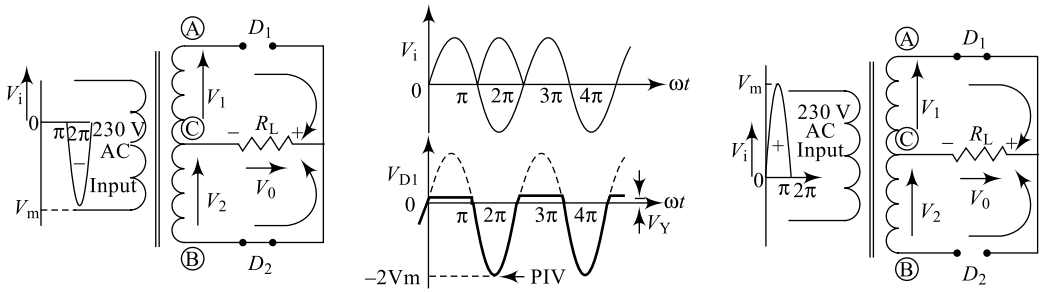


(a) Circuit diagram (b) Input/Output waveforms

Fig. 2.8 Centre-tapped full-wave rectifier

Working

Let $V_i = V_1 = V_m \sin \omega t$ be the input signal at the transformer secondary ($V_2 = V_m \sin \omega t \pm \omega t$); it is a sinusoidal signal with maximum amplitude V_m. During the positive half-cycle of the input, the point *A* being positive with respect to the point *C*, the diode D_1 will be forward biased, however, the point *B* being negative with respect to the point *C*, the diode D_2 will be reverse biased. Diode D_1 starts conduction resulting in a current I_D flowing through the load resistor R_L in the direction marked for the entire positive half cycle, i.e. from $\omega t = 0$ to Π, and the diode D_2 will be in OFF condition. During the negative half-cycle of the input, the point *B* will be positive with respect to the point *C* and the diode D_2 will be forward biased, the point *A* will be negative with respect to the point *C* and the diode D_1 will be reverse biased. Diode D_2 starts conduction resulting in a current I_D flowing through the load resistor R_L again in the same direction (as earlier) for the entire negative half-cycle, i.e. from $\omega t = \Pi$ to 2Π and the diode D_1 will be in OFF condition. Thus, between $\omega t = 0$ to Π, D_1 conducts and results in an output, between $\omega t = \Pi$ to 2Π, D_2 conducts and results in an output. V_o is also zero as indicated in Fig. 2.8(b). It can therefore be observed that for both cycles of input, there is a current flowing, hence the name full-wave rectifier. This can be further substantiated using the equivalent circuits shown in Fig. 2.9. During the positive half-cycle of the input diode D_1 is a closed switch and the voltage across the conducting diode is simply equal to V_γ; also, the diode D_2 is an open switch and the voltage across the nonconducting diode is simply equal to secondary transformer voltage ($V_1 + V_2$). Similarly, during negative half-cycle, the diode D_2 is a closed switch and the voltage across the conducting diode is simply equal to V_γ; also, the diode D_1 is an open switch and the voltage across the nonconducting diode is simply equal to the secondary transformer voltage ($V_1 + V_2$). During the positive half-cycle of the input, the open-circuited diode D_2 observes a reverse voltage which has a maximum value of $2V_m$ and during the negative half-cycle of the input, the open-circuited diode D_1 observes a reverse voltage which has a maximum value of $2V_m$. This maximum reverse voltage across the diodes is known as the **Peak Inverse Voltage** (PIV). As already mentioned, it is important to note that PIV rating for a diode will be available in the manufacturer's specification sheet, but the circuit in which the diode is working will decide the maximum value of PIV that is appearing across the reverse-biased diode. This value should be well below the specification in data sheet so that the diode is not damaged. Thus, the diode used for a full-wave rectifier should have a PIV rating that is greater than or at least equal to $2V_m$ as against just V_m in an HWR, so that the device is not damaged.



(a) Circuit diagram (b) Input/output waveforms (c) V_D waveforms

Fig. 2.9 Full-wave rectifier equivalent circuits

$$\text{PIV} = 2V_m \qquad [2.21(a)]$$

Looking at the output waveform, it is clear that for every cycle of the input, there are two cycles of output and hence we have the output frequency

$$f_O = 2 \times f_i \qquad [2.21(b)]$$

Now, the performance of a centre-tapped (two-diode FWR) full-wave rectifier can be determined by measuring various parameters such as the rectification efficiency, ripple factor, transformer utilisation factor, form factor, etc. just like in the case of an HWR. The estimation of these parameters is done in the following sections from 2.5.1 to 2.5.6.

Example 2.5

In the circuit of Fig. 2.8(a), if the transformer secondary has a voltage $V_1 = 15 \sin 100t$, find the dc output voltage, rectification efficiency and output frequency of the rectifier. The Si diodes used are assumed to have a forward resistances of 15 Ω each and load resistance is 1.5 kΩ.

Solution Using Eq. (2.23), we can write

$$V_{o(dc)} = \frac{2V_m}{\Pi} = 0.637V_m = 0.9003\ Vs$$

$$V_{o(dc)} = 0.637V_m = 0.637 \times 15$$

$$V_{o(dc)} = 9.56 \text{ V}$$

Similarly, $I_{o(dc)} = \dfrac{V_{odc}}{R_L} = \dfrac{9.56}{100}$ 95.6 mA

$$\text{Power } P = I^2 R_L$$

$$= 95.6 \text{ mA}^2 \times 100 = 0.914 \text{ W}$$

Using Eq. (2.26), we can write

$$\eta = \frac{8}{\pi^2 \left(1 + \dfrac{R_f}{R_L}\right)} \times 100\%$$

$$= \frac{8}{\pi^2 \left(1 + \dfrac{15}{1500}\right)} \times 100\%$$

$$\eta = 80.2544\%$$

Using Eq. [2.21(b)], we can write for an FWR $f_O = 2 \times f_i$

But, $$f_i = \frac{\omega}{2\Pi} = \frac{100}{2\Pi}$$

$$= 15.92 = 16 \text{ Hz}$$

$\therefore$ $$f_O = 2 \times f_i$$

$$= 2 \times 16$$

$$f_O = 32 \text{ Hz}$$

It is again interesting to note that in Fig. 2.8(a), the FWR, reversing the direction of diodes result in positive full-rectified output. In Fig. 2.10, two sets of diodes are used to produce both positive and negative outputs; diodes D_1 and D_2 produce positive output, while diodes D_1' and D_2' produce negative output as indicated. This form of the output is useful for certain applications where negative power supply is needed.

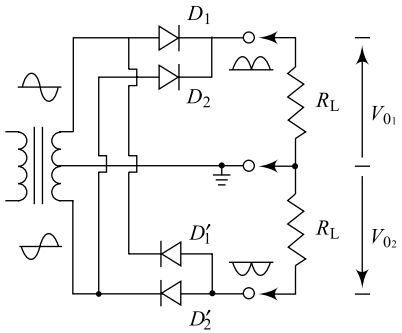


Fig. 2.10 Full-wave rectifier—an alternate form

2.5.1 Rectification Efficiency for FWR(η_{CTFwR})

As already discussed in Section 2.4.1, one important parameter that can be used to measure the performance of a rectifier is its conversion efficiency. It speaks about the ability of a rectifier in converting an ac input into useful dc output. The rectification efficiency of a rectifier is defined as the ratio of the dc power at the output to the ac power at the input(η).

$$\eta = \frac{\text{dc power output}}{\text{ac power input}} \times 100\%$$

$$\eta = \frac{P_{dc}\,(O/P)}{P_{ac}\,(I/P)} \times 100\%$$

$$\eta = \frac{[I_{dc}^2 \text{RL}] \text{ at the } O/P}{[I_{rms}^2\,(R_L + R_f + R_S)] \text{ at the } I/P} \times 100\% \qquad (2.22)$$

where R_f is the diode forward resistance and R_s is the transformer secondary winding resistance; practically, $R_S << R_f$ and can be neglected.

Average Output Voltage

Now, the average output voltage, or the dc output voltage across the load for an FWR, is obtained by integrating the output voltage waveform between (the repetitive period) 0 and Π and averaging it over Π.

$$V_{o(avg)} = V_{o(dc)} = \frac{1}{\pi}\int_0^{\Pi} V_o \, d\omega t$$

Since the diode is assumed to be ideal, V_o is a replica of V_i and hence,

$$V_{o(dc)} = \frac{1}{\pi}\int_0^{\pi} V_i \, d\omega t$$

$$= \frac{V_m}{\pi}\int_0^{\pi} \sin \omega t \, d\omega t$$

$$= \frac{V_m}{\pi}[-\cos \omega t]_0^{\pi} = \frac{V_m}{(\pi)(1+1)}$$

$$V_{o(dc)} = \frac{2V_m}{\pi} = 0.637\, V_m = 0.9003\, V_s \tag{2.23}$$

Similarly, the average or the dc current through the load is given by integrating the output current between (the repetitive period) 0 and Π and averaging it over Π.

$$I_{o(dc)} = \frac{1}{\pi}\int_0^{\pi} I_o \, d\omega t$$

$$I_{o(dc)} = \frac{2I_m}{\pi} = 0.637\, I_m = 0.9003\, I_s \tag{2.24}$$

For a full-rectified sine wave, we can calculate the rms value of output voltage at the load resistance as

$$V_{rms} = \frac{1}{\pi}\sqrt{\int_0^{\pi} (V_i)^2 \, d\omega t}$$

$$V_{rms} = \frac{1}{\pi}\sqrt{\int_0^{\pi} (V_m \sin \omega t)^2 \, d\omega t}$$

$$V_{rms} = \frac{V_m}{\pi}\sqrt{\int_0^{\pi} (1 - \cos 2\omega t) \, d\omega t}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} \tag{2.25(a)}$$

Similarly, the rms value of output current through the load resistance is

$$I_{rms} = \frac{I_m}{\sqrt{2}} \tag{2.25(b)}$$

Using Eq. (2.24) and Eq. [2.25(b)] in Eq. (2.22), we can arrive at the final expression for efficiency:

$$\eta = \frac{\dfrac{[2I]_m^2}{[\pi]}(R_L) \text{ at the } O/P}{\dfrac{[I]_m^2}{[\sqrt{2}]}(R_L + R_f) \text{ at the } I/P}$$

$$\therefore \quad \eta = \frac{8}{\pi^2\left(1 + \dfrac{R_f}{R_L}\right)} \times 100\% \tag{2.26}$$

But, $R_f << R_L$ and hence can be neglected; this results in a maximum efficiency

$$\eta_{max} = \frac{8}{\pi^2} \times 100\% = 81.2\% \tag{2.27}$$

Equation 2.27 clearly indicates that the maximum achievable conversion efficiency is now 81.2% in an FWR against 40.6% in an HWR. This is exactly doubled and hence this rectifier is a better choice for an application.

Example 2.6

Calculate the dc current (I_{dc}) flowing through a 100 Ω resistor and the power consumed by the load connected to a 240 V single-phase full-wave rectifier as shown in Fig. 2.8(a). Estimate the PIV for each diode.

Solution Using Eq. (2.23), we can write

$$V_{dc} = 0.637 V_m$$
$$= 0.673 \times 15 = 9.556 \text{ V}$$

Similarly, we have

$$I_{dc} = V_{dc}/R_L$$
$$= 9.556/100 = 95.56 \text{ mA}$$

Now, power is given by

$$P = V_{dc} \times I_{dc}$$
$$= 9.556 \times 95.56 \text{ mA} = 0.9131 \text{ W}$$

Using Eq. 2.21(a), we can observe that each diode faces a

$$\text{PIV} = 2V_m$$
$$= 2 \times 15 = 30 \text{ V}$$

2.5.2 Ripple Factor for FWR(γ_{CTFWR})

Another important parameter that can be used to measure the performance of a rectifier is its ripple factor. It speaks about the quality of the dc output of a rectifier. The ripple factor of a rectifier is defined as the ratio of rms value of ac component at the output to the dc component present in the output. It is represented by the Greek letter γ.

$$\gamma = \frac{\text{rms value ac component in output}}{\text{Actual dc component in output}} \times 100\%$$
$$\gamma = \frac{V_{ac}(O/P)}{V_{dc}(O/P)} \times 100\% \tag{2.28}$$

From the basics of electrical sciences, we can write the relationship between rms value, average value and the ac value of a voltage signal as below:

$$V_{rms}^2 = V_{ac}^2 + V_{dc}^2$$

$$\therefore \quad V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2} \tag{2.29}$$

Substituting Eq. (2.23) and Eq. (2.29) in Eq. (2.28), we obtain

$$\gamma = \sqrt{\frac{V_{\text{rms}}^2}{V_{\text{o dc}}^2} - 1} \tag{2.30}$$

$$\gamma = \sqrt{\frac{\left(\frac{[V]_m}{[\sqrt{2}]}\right)^2}{\left[\frac{2V_{\text{m}}}{\pi}\right]^2} - 1}$$

$$\gamma = \sqrt{\left(\left[\left(\frac{\pi}{8}\right)\right]^2 - 1\right)}$$

$$\gamma = 0.482 \tag{2.31}$$

Thus, Eq. (2.31) obtained for ripple factor clearly indicates that the output of a full-wave rectifier is relatively of good quality in comparison to that of an HWR. It contains only 48.2% of ac components as against 121% in an HWR.

2.5.3 Transformer Utilisation Factor for FWR(TUF_{CTFWR})

Another very important parameter that can be used to analyse the performance of a rectifier circuit is the Transformer Utilisation Factor (TUF). A TUF indicates the ability of the rectifier circuit in utilising the available transformer secondary power. It is defined as the ratio of the dc power output to the rated ac power for the transformer secondary.

$$\text{TUF} = \frac{P_{\text{dc}}\,(O/P)}{P_{\text{ac}}\,(\text{rated})} \times 100\%$$

The rated (rms) voltage of the transformer secondary is given by $V_{\text{S(rated)}} = \dfrac{V_{\text{m}}}{\sqrt{2}}$

But, the actual rms current flowing through the winding is only $I_{\text{rms}} = \dfrac{I_{\text{m}}}{\sqrt{2}}$

$$\text{TUF} = \frac{I_{\text{dc}}^2 \times R_{\text{L}}}{I_{\text{rms}} \times V_{\text{rms}}} \times 100\%$$

$$= \frac{\frac{(2I_{\text{m}})^2}{\pi^2} \times R_{\text{L}}}{\frac{V_{\text{m}}}{\sqrt{2}} \times \frac{I_{\text{m}}}{\sqrt{2}}} \times 100\%$$

$$= \frac{\frac{4V_{\text{m}}^2}{\pi^2} \times \frac{1}{R_{\text{L}}}}{\frac{V_{\text{m}}}{\sqrt{2}} \times \frac{V_{\text{m}}}{\sqrt{2}R_{\text{L}}}} \times 100\% = \frac{8}{\pi^2} \times 100\% = 0.811$$

But, secondary of a two-diode FWR contains two windings resulting in two HWRs and hence its actual TUF can be twice that of an HWR: 0.574. The average of these two values can, therefore, be taken as the effective TUF for this FWR.

$$\therefore \quad \text{TUF} = \frac{0.574 + 0.811}{2} = 0.693 \tag{2.32}$$

Thus, Eq. (2.32) obtained for transformer utilisation factor clearly indicates that in a centre-tapped full-wave rectifier, the utility of the available transformer secondary power is relatively improved and is around 69.3% as against 28.7% in an HWR. This improvement is just because of using both half cycles of the input, however, in a two-diode rectifier, full transformer secondary power is still not fully utilised. Hence, it is very essential to look for an alternate form of a full-wave rectifier circuit that best utilises the transformer secondary power and that is a four-diode FWR or a bridge-type FWR discussed in Section 2.6.

2.5.4 Form Factor for FWR(F_{CTFWR})

Form factor of a rectifier can be defined as the ratio of the rms value at output to the average or dc value of the output. A form factor is therefore given by

$$F = \frac{V_{\text{rms}}(O/P)}{V_{\text{dc}}(O/P)} \times 100\%$$

$$F = \frac{\dfrac{V_{\text{m}}}{\sqrt{2}}}{\dfrac{2V_{\text{m}}}{\pi}} \times 100\% = \frac{p}{2\sqrt{2}} \times 100\% = 1.1107 \times 100\% \tag{2.33}$$

A form factor is related to ripple factor through the equation $\gamma = \sqrt{F^2 - 1}$

2.5.5 Peak Factor of FWR

Peak factor is given as the ratio of peak value to the rms value:

$$\text{Peak factor} = \frac{\text{Peak value } (V_{\text{m}})}{\text{rms value } (V_{\text{s}})} \times 100\% = \frac{V_{\text{m}}}{\dfrac{V_{\text{m}}}{\sqrt{2}}} \times 100\%$$

$$\text{Peak factor} = \sqrt{2} \times 100\% = 1.414 \times 100\% \tag{2.34}$$

where V_{max} is the maximum voltage value of the ac supply, and V_{S} is the rms value of the supply voltage.

2.5.6 Regulation of FWR

The variation of the dc output voltage with respect to the dc load is termed as voltage regulation for a rectifier. It can be defined as the ratio of change in output voltage from no-load condition to full-load condition expressed as a percentage with respect to the full-load voltage.

$$\text{Regulation} = \frac{V_{\text{no-load}} - V_{\text{full-load}}}{V_{\text{full-load}}} \times 100\% \tag{2.35}$$

In a full-wave rectifier, the variation of V_{dc} as function of I_{dc} can be given as follows:

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi(R_L + R_f)}$$

Solving the above equation for $V_{dc} = I_{dc} \times R_L$, we get

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc} \times R_f \tag{2.36}$$

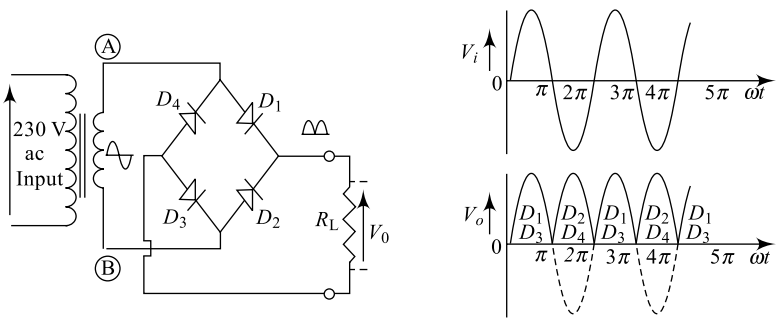
$$\therefore \quad \text{Regulation} = \frac{\left[\frac{2V_m}{\pi}\right] - \left[\frac{2V_m}{\pi} - I_{dc} \times R_f\right]}{\left[\frac{2V_m}{\pi} - I_{dc} \times R_f\right]} \times 100\%$$

$$\text{Regulation} = \frac{R_s + R_f}{R_L} \times 100\% \tag{2.37}$$

2.6 RECTIFIERS: BRIDGE-TYPE FULL-WAVE RECTIFIER

The dc level obtained from a sinusoidal input can be improved 100% using full-wave rectification. One of the forms of an FWR, the two-diode rectifier and its performance are already discussed in Section 2.5 and it is observed that there is an improvement in the efficiency and ripple factor. But, in order to improve the PIV requirement and the TUF, another familiar network, called a bridge rectifier, is used.

The circuit diagram and the input/output waveforms of a full-wave bridge rectifier are shown in Fig. 2.11; the four diodes D_1, D_2, D_3 and D_4 are arranged in a bridge configuration and hence the name. The circuit contains a transformer that steps down the input ac magnitude depending on the requirement and provides the necessary isolation avoiding any risk of shocks. Unlike in the case of a two-diode FWR, here the transformer is not a centre-tapped one and thus provides an ac signal at the secondary named V_i. The turns ratio for the transformer decides the magnitude of the secondary voltages V_i. R_L represents the load for the circuit and as usual it is assumed to be a pure resistor for simplicity and ease of analysis.

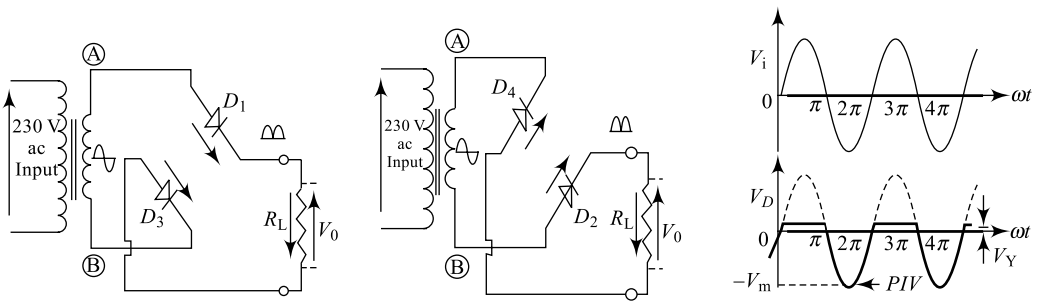


(a) Bridge rectifier circuit (b) Input/output waveforms

Fig. 2.11 Bridge-type full-wave rectifier

Working

Let $V_i = V_m \sin \omega t$ be the input signal at the transformer secondary, it is a sinusoidal signal with maximum amplitude V_m. During the positive half-cycle of the input, the point *A* being positive with respect to the point *B*, the diodes D_1 and D_3 will be forward biased; however, the diodes D_2 and D_4 will be reverse biased. The pair of diodes D_1 and D_3 start conduction resulting in a current I_D flowing through the load resistor R_L in the direction marked for the entire positive half-cycle, i.e. from $\omega t = 0$ to Π and the diodes D_2 and D_4 will be in OFF condition. During the negative half-cycle of the input, the point *B* will be positive with respect to the point *A* and the diodes D_2 and D_4 will be forward biased, and the diodes D_1 and D_3 will be reverse biased. Diodes D_2 and D_4 start conduction resulting in a current I_D flowing through the load resistor R_L again in the same direction (as earlier) for the entire negative half-cycle, i.e. from $\omega t = \Pi$ to 2Π and the diodes D_1 and D_3 will be in OFF condition. Thus, between $\omega t = 0$ to Π, D_1 and D_3 conduct and result in an output, between $\omega t = \Pi$ to 2Π, D_2 and D_4 conduct and result in an output V_o as indicated in Fig. 2.12(b). It can therefore be observed that for both cycles of input, there is a current flowing, hence the name full-wave rectifier. This can be further substantiated using the equivalent circuits shown in Fig. 2.12. During positive half-cycle of input diodes D_1 and D_3 will be closed switches and the voltage across the conducting diodes is simply equal to V_γ; also, diodes D_2 and D_4 are open switches and the voltage across the nonconducting diodes is simply equal to secondary transformer voltage V_m. Similarly, during negative half-cycle, diodes D_2 and D_4 are closed switches and the voltage across the conducting diodes is simply equal to V_γ; also, diodes D_1 and D_3 are open switches and the voltage across the nonconducting diodes is simply equal to secondary transformer voltage V_m. During the positive half-cycle of the input, the open-circuited diodes D_2 and D_4 observe a reverse voltage which has a maximum value of V_m and during the negative half-cycle of the input, the open-circuited diodes D_1 and D_3 observe a reverse voltage which has a maximum value of V_m. This maximum reverse voltage across the diodes is known as the **Peak Inverse Voltage** (PIV). Thus, the diodes used for a bridge-type full-wave rectifier should have a PIV rating that is greater than or at least equal to V_m as against just $2V_m$ in a centre-tapped FWR, so that the device is not damaged.



(a) Positive half-cycle (b) Negative half-cycle (c) Diode waveforms

Fig. 2.12 Bridge-type full-wave rectifier

$$\text{PIV} = V_m \qquad [2.38(a)]$$

Looking at the output waveform, it is clear that for every cycle of the input, there are two cycles of output and hence we have the output frequency. Now, the performance of a bridge-type (four-diode FWR) full-wave rectifier can be determined by measuring various parameters such as the rectification efficiency, ripple factor, transformer utilisation factor, form factor, etc. just like in the case of an HWR

or a two-diode FWR. The estimation of these parameters is done in the following sections from 2.6.1 to 2.6.6.

$$f_O = 2 \times f_i \qquad [2.38(b)]$$

Example 2.7

In the circuit of Fig. 2.11(a), if the transformer secondary has a voltage $V_1 = 15 \sin 100t$, find the dc output voltage, rectification efficiency and output frequency of the rectifier. The Si diodes used are assumed to have a forward resistances of 15 Ω each and load resistance is 1.5 kΩ.

Solution Using Eq. (2.40), we can write

$$V_{o(dc)} = \frac{2V_m}{\pi} = 0.637 V_m = 0.9003 V_s$$

$$V_{o(dc)} = 0.637\ V_m = 0.6.37 \times 15$$

$$V_{o(dc)} = 9.56 \text{ V}$$

Similarly, $I_{o(dc)} = \dfrac{V_{odc}}{R_L} = \dfrac{9.56}{100} = 95.6 \text{ mA}$

$$\text{Power } P = I^2 R_L$$

$$= 95.6 \text{ mA}^2 \times 100 = 0.914 \text{ W}$$

Using Eq. (2.42), we can write

$$\eta = \frac{8}{\pi^2 \left(1 + \dfrac{2R_f}{R_L}\right)} \times 100\%$$

$$= \frac{8}{\pi^2 \left(1 + \dfrac{2 \times 15}{1500}\right)} \times 100\%$$

$$\eta = 79.468\%$$

Using Eq. [2.38(b)], we can write for an FWR, $f_O = 2 \times f_i$

But, $$f_i = \frac{\omega}{2\pi} = \frac{100}{2\pi}$$

$$= 15.92 = 16 \text{ Hz}$$

$\therefore$ $$f_O = 2 \times f_i$$

$$= 2 \times 16$$

$$f_O = 32 \text{ Hz}$$

2.6.1 Rectification Efficiency for FWR(η_{BFWR})

As already discussed in Section 2.4.1, one important factor that can be used to measure the performance of a rectifier is its conversion efficiency. It speaks about the ability of a rectifier in converting an ac input into useful dc output. The rectification efficiency of a rectifier is defined as the ratio of the dc power at the output to the ac power at the input(η).

$$\eta = \frac{\text{dc power output}}{\text{ac power input}} \times 100\%$$

$$\eta = \frac{P_{dc}(O/P)}{P_{ac}(I/P)} \times 100\%$$

$$\eta = \frac{I_{dc}^2 (R_L) \text{ at the } O/P}{I_{rms}^2 (R_L + 2R_f + R_s) \text{ at the } I/P} \times 100\% \tag{2.39}$$

where R_f is the average diode forward resistance and R_S is transformer secondary winding resistance; practically $R_S << R_f$ and can be neglected as already stated earlier.

Average Output Voltage

Now, the average output voltage, the dc output current, conversion efficiency and ripple factor for the bridge-type FWR can be obtained as already presented in Section 2.5.1.

$$V_{o(dc)} = V_{o(dc)} = \frac{1}{\pi}\int_0^{\pi} V_o \, d\omega t$$

$$V_{o(dc)} = \frac{2V_m}{\pi} = 0.637 V_m = 0.9003 \text{ Vs} \tag{2.40}$$

and

$$I_{o(ac)} = \frac{1}{\pi}\int_0^{\pi} I_o \, d\omega t$$

$$I_{o(dc)} = \frac{2I_m}{\pi} = 0.637 I_m = 0.9003 I_s \tag{2.41}$$

Using Eq (2.24) and Eq. [2.25(b)] in Eq. (2.39), we can arrive at the final expression for efficiency;

$$\eta = \frac{\left[\left(\frac{2I_m}{(\pi)}\right)^2 R_L\right] \text{at the } O/P}{\left[\left(\frac{I_m}{(\sqrt{2})}\right)^2 (R_L + 2R_L)\right] \text{at the } I/P} \times 100\%$$

$$\therefore \quad \eta = \frac{8}{\pi^2\left(1 + \frac{2R_L}{R_L}\right)} \times 100\% \tag{2.42}$$

But, $R_f << R_L$ and hence can be neglected resulting in a maximum value of efficiency

$$\eta_{max} = \frac{8}{\pi^2} \times 100\% = 81.2\% \tag{2.43}$$

Equation (2.43) clearly indicates that the maximum achievable conversion efficiency is now 81.2% in an FWR against 40.6% in an HWR. This is exactly doubled and hence this rectifier is a better choice for an application.

Example 2.8

Calculate the dc current (I_{dc}) flowing through a 100 Ω resistor and the power consumed by the load connected to a 240 V single-phase full-wave rectifier as shown in Fig. 2.11(a). Estimate the PIV for each diode.

Solution Using Eq. (2.40), we can write

$$V_{dc} = 0.637V_m$$
$$= 0.673 \times 15 = 9.556 \text{ V}$$

Similarly, we have

$$I_{dc} = V_{dc}/R_L$$
$$= 9.556/100 = 95.56 \text{ mA}$$

Now, power is given by

$$P = V_{dc} \times I_{dc}$$
$$= 9.556 \times 95.56 \text{ mA} = 0.9131 \text{ W}$$

Using Eq. [2.38(a)], we can observe that each diode faces a

$$\text{PIV} = V_m$$
$$= 15 \text{ V}$$

2.6.2 Ripple Factor for FWR(γ_{BFwR})

Another important factor that can be used to measure the performance of a rectifier is its ripple factor. It speaks about the quality of the dc output of a rectifier. The ripple factor of a rectifier is defined as the ratio of rms value of ac component at the output to the dc component present in the output. It is represented by the Greek letter γ.

$$\gamma = \frac{\text{rms value ac component in output}}{\text{Actual dc component in output}} \times 100\%$$

$$\gamma = \frac{V_{rms}\,(O/P)}{V_{odc}\,(O/P)} \times 100\% \tag{2.44}$$

From the basics of electrical sciences, we can write the relationship between rms value, average value and the ac value of a voltage signal as below;

$$V_{rms}^2 = V_{ac}^2 + V_{dc}^2$$

$$\therefore \quad V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2} \tag{2.45}$$

Substituting Eq. (2.23) and Eq. (2.28) in Eq. (2.27), we obtain

$$\gamma = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1} \tag{2.46}$$

For a full-rectified sine wave, the rms value of output voltage at the load resistance is (from Eq. 2.25(a))

$$V_{(rms)} = \frac{V_m}{\sqrt{2}} \tag{2.47}$$

Substituting Eq. (2.40) and Eq. (2.47) in Eq. (2.46), we obtain

$$\gamma = \sqrt{\left(\frac{\frac{V_m}{\sqrt{2}}}{\frac{2V_m}{\Pi}}\right)^2 - 1}$$

$$\gamma = \sqrt{\left[\left(\frac{\pi}{8}\right)^2 - 1\right]}$$

$$\gamma = 0.482 \tag{2.48}$$

Thus, Eq. (2.48) obtained for ripple factor clearly indicates that the output of a full-wave rectifier is same for both types of FWRs and is of relatively good quality in comparison to that of an HWR. It contains only 48.2% ac components as against 121% in an HWR.

2.6.3 Transformer Utilisation Factor for FWR(TUF_{BFWR})

Another very important parameter that can be used to analyse the performance of a rectifier circuit is the Transformer Utilisation Factor (the TUF). A TUF indicates the ability of the rectifier circuit in utilising the available transformer secondary power. It is defined as the ratio of the dc power output to the rated ac power for the transformer secondary.

$$\text{TUF} = \frac{P_{\text{dc}}\ (o/p)}{P_{\text{ac}}\ (\text{rated})} \times 100\%$$

The rated (rms) voltage of the transformer secondary is given by $V_{\text{S(rated)}} = \frac{V_{\text{m}}}{\sqrt{2}}$

But, the actual rms current flowing through the winding is only $I_{\text{rms}} = \frac{I_{\text{m}}}{\sqrt{2}}$

$$\text{TUF} = \frac{I_{\text{dc}}^2 \times R_L}{I_{\text{rms}} \times V_{\text{rms}}} \times 100\%$$

$$= \frac{\frac{(2I_{\text{m}})^2}{\pi^2} \times R_{\text{L}}}{\frac{V_{\text{m}}}{\sqrt{2}} \times \frac{I_{\text{m}}}{\sqrt{2}}} \times 100\%$$

$$= \frac{\frac{4V_{\text{m}}^2}{\pi^2} \times \frac{1}{R_{\text{L}}}}{\frac{V_{\text{m}}}{\sqrt{2}} \times \frac{V_{\text{m}}}{\sqrt{2}R_{\text{L}}}} \times 100\% = \frac{8}{\pi^2} \times 100\%$$

$$\text{TUF} = 0.812 \tag{2.49}$$

Thus, Eq. (2.49) obtained for transformer utilisation factor clearly indicates that in a bridge-type full-wave rectifier, the utility of the available transformer secondary power is improved largely and is around 81.2% as against 69.3% in a two-diode FWR and 28.7% in an HWR. This improvement is just because of using both half cycles of the input and maximum utilisation of transformer secondary power. Hence, it is always recommended to use a bridge type of FWR for most of the applications.

2.6.4 Form Factor for FWR(F_{BFWR})

Form factor of a rectifier can be defined as the ratio of the rms value at output to the average or dc value of the output. A form factor is therefore given by

$$F = \frac{V_{\text{rms}}\,(O/P)}{V_{\text{dc}}\,(O/P)} \times 100\%$$

$$F = \frac{\left(\frac{V_{\text{m}}}{\sqrt{2}}\right)}{\left(\frac{2V_{\text{m}}}{\pi}\right)} \times 100\% = \frac{\pi}{2\sqrt{2}} \times 100\% = 1.1107 \times 100\% \tag{2.50}$$

A form factor is related to ripple factor through the equation $\gamma = \sqrt{F^2 - 1}$

2.6.5 Peak Factor for FWR

Peak factor is given as the ratio of peak value to the rms value.

$$\text{Peak factor} = \frac{\text{Peak value}\,(V_{\text{m}})}{\text{rms value}\,(V_{\text{s}})} \times 100\% = \frac{V_{\text{m}}}{\frac{V_{\text{m}}}{\sqrt{2}}} \times 100\%$$

$$\text{Peak factor} = \sqrt{2} \times 100\% = 1.414 \times 100\% \tag{2.51}$$

where V_{max} is the maximum voltage value of the ac supply, and V_{S} is the rms value of the supply voltage.

2.6.6 Regulation for FWR

The variation of the dc output voltage with respect to the dc load is termed voltage regulation for a rectifier. It can be defined as the ratio of change in output voltage from no-load condition to full-load condition expressed as a percentage with respect to the full-load voltage.

$$\text{Regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{full load}}} \times 100\% \tag{2.52}$$

In a full-wave rectifier, the variation of V_{dc} as function of I_{dc} can be given as follows;

$$I_{\text{dc}} = \frac{2I_{\text{m}}}{\pi} = \frac{2V_{\text{m}}}{\pi(R_{\text{L}} + R_{\text{f}})}$$

Solving the above equation for $V_{\text{dc}} = I_{\text{dc}} \times R_{\text{L}}$, we get

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc} \times R_f \tag{2.53}$$

$$\therefore \quad \text{Regulation} = \frac{\left[\frac{2V_m}{\pi}\right] - \left[\frac{2V_m}{\pi} - I_{dc} \times R_f\right]}{\left[\frac{2V_m}{\pi} - I_{dc} \times R_f\right]} \times 100\%$$

$$\text{Regulation} = \frac{R_s + R_f}{R_L} \times 100\% \tag{2.54}$$

Considering Eq. (2.20), Eq. (2.37) and Eq. (2.54), it is interesting to note that the regulation for both HWR and FWR circuits can be approximated to only

$$= \frac{R_f}{R_L}. \tag{2.55}$$

Example 2.9

Prove that the regulation of output voltage in any rectifier (either HWR or FWR) is given approximately by Eq. (2.55).

Solution We have

$$\text{Regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{full load}}} \times 100\%$$

In a full-wave rectifier, the variation of V_{dc} as function of I_{dc} can be given as follows:

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi(R_L + R_f)}$$

Solving the above equation for $V_{dc} = I_{dc} \times R_L$, we get

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc} \times R_f \tag{2.56}$$

Similarly, in an HWR $V_{dc} = \frac{V_m}{\pi} - I_{dc} \times R_f$ (2.57)

The no-load dc voltages for both HWR and FWR can be obtained by substituting I_{dc}= 0 in Eq. (2.56) and Eq. (2.57). For an FWR, now the regulation can be obtained as

$$\text{Regulation} = \frac{\left[\frac{2V_m}{\pi}\right] - \left[\frac{2V_m}{\pi} - I_{dc} \times R_f\right]}{\left[\frac{2V_m}{\pi} - I_{dc} \times R_f\right]} \times 100\%$$

$$\therefore \quad \text{Regulation} = \frac{I_{dc} \times R_f}{I_{dc} \times R_L} \times 100\%$$

But $V_{\text{full-load}} = I_{\text{dc}} \times R_{\text{L}}$, hence

$$\text{Regulation} = \frac{R_{\text{f}}}{R_{\text{L}}} \times 100\% \tag{2.58}$$

$$\text{Regulation} = \frac{\left[\frac{V_{\text{m}}}{\pi}\right] - \left[\frac{V_{\text{m}}}{\pi} - I_{\text{dc}} \times R_{\text{f}}\right]}{\left[\frac{V_{\text{m}}}{\pi} - I_{\text{dc}} \times R_{\text{f}}\right]} \times 100\%$$

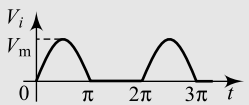
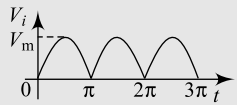
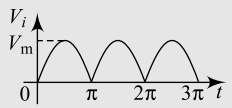
Similarly, for an HWR,

$$\text{Regulation} = \frac{R_{\text{f}}}{R_{\text{L}}} \times 100\% \tag{2.59}$$

Comparing Eq. (2.58) and Eq. (2.59), the statement above in Eq. (2.55) is proved.

Now, having studied different single-phase rectifiers, the summary can be illustrated as in the Table 2.2.

Table 2.2 Performance comparison of different rectifiers.

Sl.No.	Comparison	HWR	FWR—centre tapped	FWR—bridge
1	Number of diodes	One	Two	Four
2	Output waveform			
3	Average output V_{dc} (I_{dc})	$\frac{V_{\text{m}}}{\pi}\left[\frac{I_{\text{m}}}{\pi}\right]$	$\frac{2V_{\text{m}}}{\pi}\left[\frac{2I_{\text{m}}}{\pi}\right]$	$\frac{2V_{\text{m}}}{\pi}\left[\frac{2I_{\text{m}}}{\pi}\right]$
4	Rectification efficiency (η)	$\eta = \frac{4}{\pi^2\left(1+\frac{R_{\text{f}}}{R_{\text{L}}}\right)} \times 100$	$\eta = \frac{8}{\pi^2\left(1+\frac{R_{\text{f}}}{R_{\text{L}}}\right)} \times 100$	$\eta = \frac{8}{\pi^2\left(1+\frac{2R_{\text{f}}}{R_{\text{L}}}\right)} \times 100$
5	Ripple factor (γ)	1.21	0.48	0.48
6	PIV	V_{m}	$2V_{\text{m}}$	V_{m}
7	TUF	0.287	0.693	0.812
8	Diode resistance	R_{f}	R_{f}	$2R_{\text{f}}$
9	Output frequency	f_{i}	$2f_{\text{i}}$	$2f_{\text{i}}$

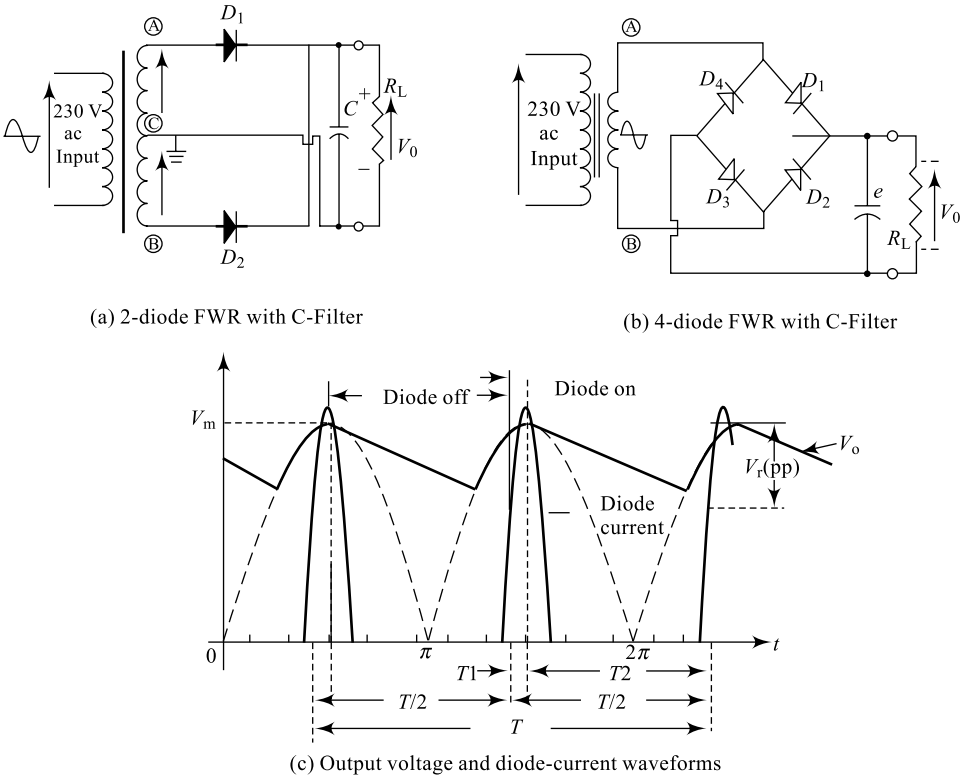
2.7 FILTERS: *RLC* FILTERS

Output of a rectifier is a pulsating dc, contains plenty of ac components and in view of better performance of any electronic circuit, it is necessary to reduce these ripple components. In Section 2.4.1, it is observed that the average output voltage for a single-phase half-wave rectifier is just $0.318V_{\text{m}}$ and the amount of ripple content in the output is very high. Using a full-wave rectifier, these values are

improved considerably; as observed in sections 2.5 and 2.6, the dc level of output increased to $0.636V_m$ and the ripple is reduced to 0.48. But, still the quality of output obtained is not very satisfying and requires further smoothening; the ripple magnitude has to be kept minimum using additional circuits. The circuit used to minimise the ac components and improve the dc contents in a rectified output is called a **filter**. Filter circuits are generally classified in to two types: active filters and passive filters. **Active filters** are discussed in Chapter 6, Section 6.19 and only **passive filters** are discussed in this section. A passive filter is constructed using passive components such as resistors (*R*), inductors (*L*) and capacitors (*C*). Different configurations of these passive components result in several filter types; such as *C*-filter, *L*-filter, *LC*-filter, *CLC*-filter, etc. Some of the most popular filters will be considered in the discussions to follow.

2.7.1 Full Wave Rectifier with Capacitor Filter

The circuit diagram of an FWR with C-filter and the corresponding output voltage and diode current waveforms are shown in Fig. 2.13. The smoothing capacitor converts the full-wave rectified pulsating output into a smooth dc output voltage. A capacitor always offers a smooth path for an ac signal and blocks any dc signal; hence, it is always connected in parallel to the load. Two important parameters are to be considered in selecting a suitable a capacitor for filtering; they are its **working voltage** *(V)*, which must be higher than the no-load output value of the rectifier and its **capacitance value** *(C)*, which determines the amount of ripple that will appear superimposed on top of the dc voltage.



(a) 2-diode FWR with C-Filter

(b) 4-diode FWR with C-Filter

(c) Output voltage and diode-current waveforms

Fig. 2.13 Full-wave rectifiers with C-filter

Working

During the positive half-cycle of the input, the diode D_1 (D_1 and D_3 in Fig. 2.13(b)) conducts and hence capacitor charges up to V_m. At $\omega t = \Pi/2$, the output voltage falls below V_m and hence the capacitor will try to maintain the voltage on it. However, the voltage on the capacitor will be discharged at a rate decided by R_L and C till once again there is a rise in the output voltage after a time $T/2$. Here, diode D_2 (D_2 and D_4 in Fig. 2.13(b)) conducts and once again capacitor charges up to V_m and the process repeats resulting in a waveform shown in Fig. 2.13(c).

The charges accumulated by the capacitor during T_1 is

$$Q_{\text{charge}} = V_{r(pp)} \times C$$

The charges lost during T_2 (discharged) by the capacitor is

$$Q_{\text{discharge}} = I_{dc} \times T_2$$

But, charges accumulated will be equal to the charges lost and hence

$$Q_{\text{charge}} = Q_{\text{discharge}}$$

$$V_{r(pp)} \times C = I_{dc} \times T_2$$

$$V_{r(pp)} = \frac{I_{dc}}{C} \times T_2$$

It is clear from the diagram that

$$\frac{T}{2} = T_1 + T_2 \quad \text{and} \quad T_1 << T_2;$$

hence $$T_2 \cong \frac{T}{2} = \frac{1}{2f}$$

$$\therefore \qquad V_{r(pp)} = \frac{I_{dc}}{2fC}$$

From the above assumptions, the ripple waveform will be triangular and its rms value is given by the equation

$$V_{r\,(rms)} = \frac{V_{r\,(pp)}}{2\sqrt{3}}$$

$$V_{r\,(rms)} = \frac{\frac{I_{dc}}{2fC}}{2\sqrt{3}}$$

$$V_{r\,(rms)} = \frac{I_{dc}}{4fC\sqrt{3}}$$

$$V_{r\,(rms)} = \frac{\frac{V_{dc}}{R_L}}{4fC\sqrt{3}}$$

But, we have the ripple factor given by $\gamma = \frac{V_{r\,(rms)}}{V_{dc}}$

$$\gamma = \frac{\frac{V_{dc}}{R_L}}{4fC\sqrt{3}} \times \frac{1}{V_{dc}}$$

$$\gamma = \frac{1}{4R_L fC\sqrt{3}} \tag{2.60}$$

If the value of the capacitor is fairly large then the value of the ripple will be very low, and if the value of the capacitor is fairly small then the value of the ripple will be very high. The ripple may be controlled by controlling C or R_L (or both) with a resulting increase in the dc output voltage.

Example 2.10

Find the size of the C-filter in an FWR needed to keep ripple values within 3%; the circuit is operating at a frequency of 10 kHz, delivering a load of 10 mA at 10 V.

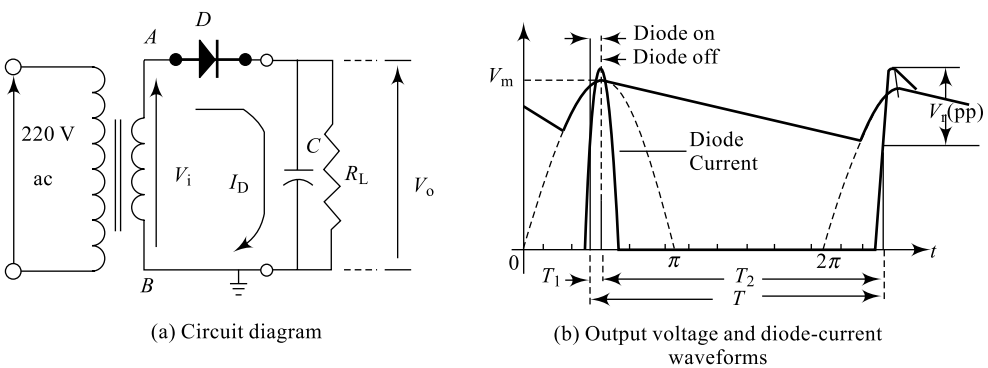
Solution We have from Eq. (2.60),

$$C = \frac{1}{4R_L f\gamma\sqrt{3}}$$

But $$R_L = \frac{V_{o\,dc}}{I_{dc}} = \frac{10}{10\text{ mA}} = 1\text{ k}\Omega$$

Now, $$C = \frac{1}{4(1\text{ k}\Omega)(10\text{ kHz})(0.03)\sqrt{3}} = 0.48113\ \mu\text{F}$$

2.7.2 Half-Wave Rectifier with Capacitor Filter



(a) Circuit diagram

(b) Output voltage and diode-current waveforms

Fig. 2.14 Half-wave rectifier with C-filter

The charges accumulated by the capacitor during T_1 is $Q_{charge} = V_{r(pp)} \times C$
The charges lost during T_2 (discharged) by the capacitor is $Q_{discharge} = I_{dc} \times T_2$
But, charges accumulated will be equal to the charges lost and hence

$$Q_{charge} = Q_{discharge}$$
$$V_{r(pp)} \times C = I_{dc} \times T_2$$

$$V_{r\,(\mathrm{pp})} = \frac{I_{\mathrm{dc}}}{C} \times T_2$$

It is clear from the diagram that $T = T_1 + T_2$ and $T_1 << T_2$; hence $T_2 \cong T = \frac{1}{f}$

$$\therefore \qquad V_{r(\mathrm{pp})} = \frac{I_{\mathrm{dc}}}{fC}$$

From the above assumptions, the ripple waveform will be triangular and its rms value is given by the equation

$$V_{r(\mathrm{rms})} = \frac{V_{r(\mathrm{pp})}}{2\sqrt{3}}$$

$$V_{r(\mathrm{rms})} = \frac{\frac{I_{\mathrm{dc}}}{2fC}}{2\sqrt{3}}$$

$$V_{r(\mathrm{rms})} = \frac{I_{\mathrm{dc}}}{2fC\sqrt{3}}$$

$$V_{r(\mathrm{rms})} = \frac{\frac{V_{\mathrm{dc}}}{R_{\mathrm{L}}}}{2fC\sqrt{3}}$$

But, we have the ripple factor given by $\gamma = \frac{V_{r(\mathrm{rms})}}{V_{\mathrm{dc}}}$

$$\gamma = \frac{\frac{V_{\mathrm{dc}}}{R_{\mathrm{L}}}}{2fC\sqrt{3}} \times \frac{1}{V_{\mathrm{dc}}}$$

$$\gamma = \frac{1}{2R_{\mathrm{L}}\,fC\sqrt{3}} \tag{2.61}$$

The ripple may be decreased by increasing C or R_{L} (both) with a resulting increase in the dc output voltage.

Example 2.11

Estimate the ripple value in an HWR with 10 μC C-filter given the input frequency for the rectifier is 100 Hz and the load is 15 V at 5 mA

Solution We have from Eq. (2.61),

$$\gamma = \frac{1}{2\,R_{\mathrm{L}}\,fC\sqrt{3}}$$

But $$R_L = \frac{V_{dc}}{I_{dc}} = \frac{15\text{ V}}{5\text{ mA}} = 3000\ \Omega$$

$$\gamma = \frac{1}{2(3000) \times 100 \times (10\ \mu\text{F})\sqrt{3}} = 0.09623$$

Table 2.3 illustrates the various other forms of passive filters available and their performances.

1. Critical inductance (L_C)

In a filter involving an inductor, there should be a continuous current flowing and this requires that there need to be a minimum amount of inductance called as **critical inductance** (L_C). The value of L_C depends on the supply frequency and the load resistance R_L and is given by the expression

$$L_C = \frac{R_L}{3\omega} \tag{2.62}$$

2. Bleeder Resistor (R_B)

The performance of an inductor is dependent on the current flowing through it and for best functioning, ther should be a minimum current flowing through the inductor. In order that this minimum current flows through the inductor, a resistor R_B called the bleeder resistor is connected as shown in Fig. 2.15. The three important functions that R_B can serve are (i) it helps optimising the filter performance by maintaining a minimum current through ***L***, (ii) it provides discharging path for capacitors so that the voltage across the output terminals do not remain for a longer period once the load is disconnected, and (iii) it acts as a voltage divider circuit providing a variable output voltage.

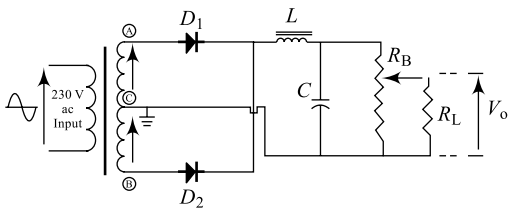


Fig. 2.15 Full-wave rectifier with bleeder resistor

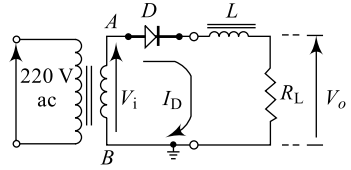
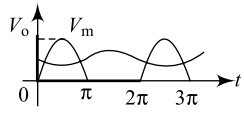
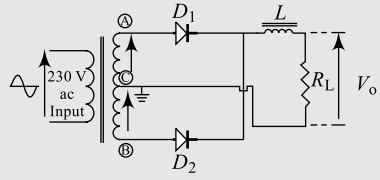
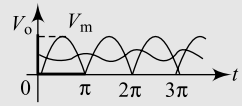
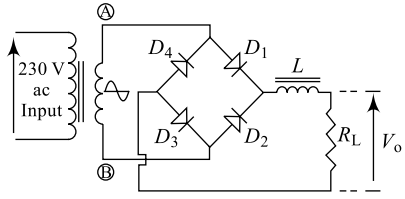
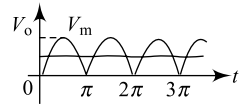
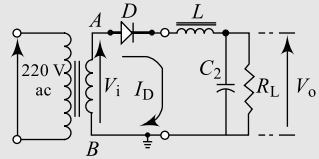
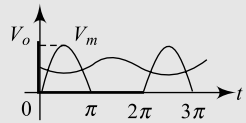
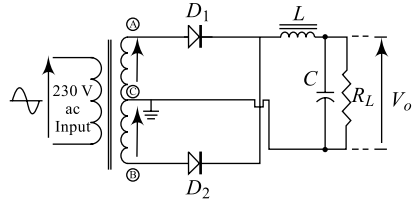
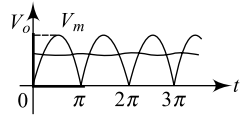
2.8 REGULATORS

A regulator is a circuit that can be used to maintain a constant output voltage even when there are changes in either the supply voltage or the load. Within the specified ranges, a regulator circuit maintains a constant and steady output voltage even when there are changes in the input line voltage or when there is a change in the load itself. This process is called regulation. Regulation can be defined as the change in the output voltage from no-load (I_L = minimum) condition to the full-load (I_L = maximum). Regulation is expressed as a percentage with respect to full-load condition. There are several forms of regulators that can be constructed and we consider here only a simple Zener regulator for our discussion.

2.8.1 Zener Voltage Regulator

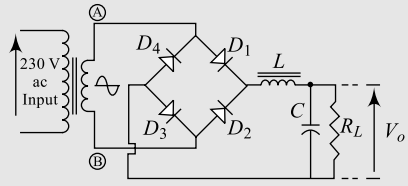
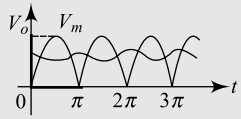
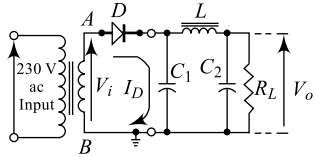
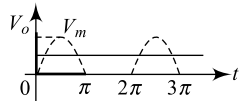
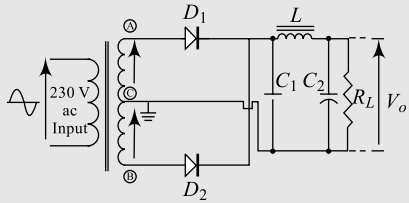
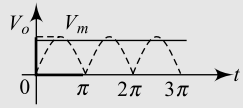
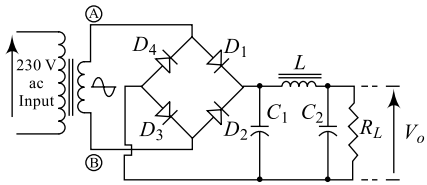
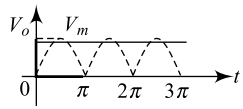
In the previous chapter, we saw that a "reverse-biased" diode passes very little current but will suffer a breakdown or junction damage if the reverse voltage applied across it exceeds the PIV limit. However, **Zener diodes** or "breakdown diodes" as they are sometimes called, are basically the similar to the standard junction diodes, but are specially made to have a low pre-determined **reverse breakdown voltage**, called the "Zener voltage" (V_z). In the forward direction, it behaves just like a normal signal diode

Table 2.3 Different forms of filters and their performances

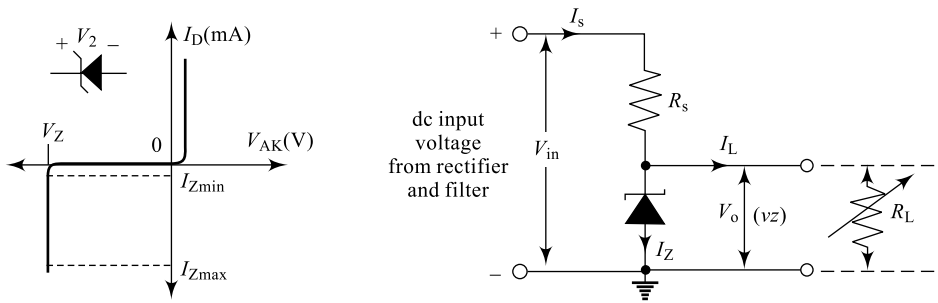
Sl. No.	Filter name	Circuit diagram	Output waveform	Remarks
1	**HWR with inductor (*L*) filter**			Relatively poor dc output.
2	**2 diode FWR with inductor (*L*) filter**			Better dc output is compared to an HWR, because there will be output for both the half cycles.
3	**4 diode FWR with inductor (*L*) Filter**			The dc output is similar to case-2, the 2-diode FWR.
4	**HWR with choke input (*LC*) filter**			There is an improvement in the dc output compared to Case-1
5	**2 diode FWR with choke input (*LC*) filter**			The dc output is improved in this case compared to Case-2. $\gamma = \frac{1}{6(\omega)^2 LC\sqrt{2}}$

(*Contd.*)

(*Contd.*)

6	**FWR with choke input (*LC*) filter**			The dc output is improved in this case compared to Case-3. $\gamma = \frac{1}{6(\omega)^2 LC\sqrt{2}}$
7	**HWR with Pi (*CLC*) filter**			Better output compared to the previous two filters. (6 Cases)
8	**FWR with Pi (*CLC*) filter**			Better output compared to any other case.
9	**FWR with Pi (*CLC*) filter**			Better output compared to any other case.

passing current, but when the reverse voltage applied to it exceeds the selected reverse breakdown voltage, a process called **avalanche breakdown** occurs in the depletion layer and the current through the diode increases to the maximum circuit value; this current is usually limited by a series resistor. The point at which current flows can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes construction giving it a specific **Zener breakdown** voltage (V_z) ranging from a few volts up to a few hundred volts. The *VI* characteristics are depicted in Chapter 1, Section 1.13.1. Zener diodes are used in the reverse-bias mode, we can see that the Zener diode has a region in its reverse-bias characteristics of almost a constant voltage regardless of the current flowing through the diode and is reproduced in Fig. 2.16(a). This voltage across the diode called Zener voltage V_z remains nearly constant even with changes in current through the diode caused by variations in the supply voltage or load. This ability of the diode to regulate the source voltage can be best utilised in stabilising a voltage source against supply or load variations. The diode will continue to regulate until the diode current falls below the $I_{z(min)}$ value, a minimum value that keeps the diode in the reverse breakdown region.



(a) Zener diode *VI* characteristics (b) Zener voltage regulator

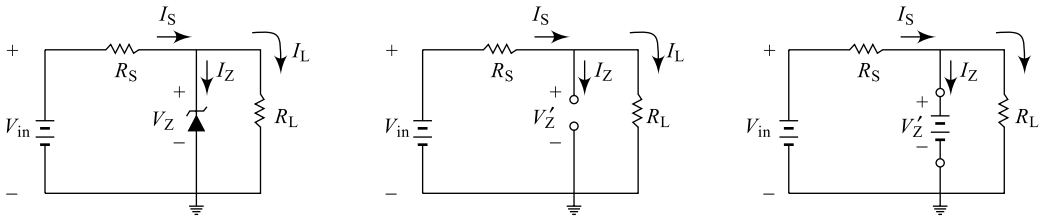
Fig. 2.16 Zener voltage regulator

The resistor R_S is connected in series with the Zener diode to limit the current flow with the output from the voltage source V_{in} being connected across the combination while the stabilised output voltage V_O is taken across the Zener diode. The Zener diode is connected across the load with its cathode terminal connected to the positive rail of the dc supply; so, it is operating in its reverse-biased condition. The series resistor R_S is so selected as to limit the current flowing in the circuit and hence the Zener diode well within maximum value $I_{Z(max)}$. When the load resistance R_L very high, there is minimum current flowing through R_L (no-load current I_L = minimum or 0) and all the circuit current passes through the Zener diode which is $I_{Z(max)}$ and dissipates maximum power in Zener. Care must be taken when selecting the appropriate value of resistance that the Zener maximum power rating is not exceeded under this "no-load" condition. When the load resistance R_L very low, there is maximum current flowing through R_L (full-load current I_L = maximum) and only a small current passes through the Zener diode which is $I_{Z(min)}$. Care again must be taken when selecting the appropriate value of resistance so that the stabilisation of the voltage is effective and the Zener current must stay above this value operating the diode within its breakdown region at all times. In order to achieve this, both R_S and R_L should be properly selected.

A Zener diode regulator analysis and design can be best studied under the following three conditions:

1. Both V_{in} and R_S Fixed

The simplest of Zener diode regulator networks appears in Fig. 2.17(a). The applied input dc voltage V_{in} is fixed, as is the load resistor. The analysis for this circuit can be done as given below:



(a) Basic Zener diode regulator (b) Calculating Zener voltage V_Z (c) Equivalent circuit

Fig. 2.17 Zener voltage regulator

First, find the open-circuit voltage across the Zener diode by using the circuit shown in Fig. 2.17(b). Applying the voltage divider rule to the circuit results in the following equation:

$$V_o = \frac{R_L \times V_{in}}{R_S + R_L} = V_Z' \tag{2.63}$$

Then, substitute the appropriate equivalent circuit and solve for all the required unknowns.
Using Kirchoff's current law to circuit of Fig. 2.17(a), we can write

$$\begin{aligned} I_S &= I_Z + I_L \\ I_Z &= I_S - I_L \end{aligned} \tag{2.64}$$

where $I_L = \dfrac{V_o}{R_L}$ and $I_S = \dfrac{V_R}{R_S} = \dfrac{V_{in} - V_o}{R_S}$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z \times I_Z \tag{2.65}$$

Example 2.12

For the Zener diode network of Fig. 2.17(a), the Zener breakdown voltage is 10 V, the maximum Zener power is 30 mW, series resistance is 1000 Ω and load resistance is 1200 Ω. Determine V_L, V_{Rs}, I_Z and P_Z.

Solution Referring to Fig. 2.17(b) and using Eq. (2.63), we can find

$$V_Z' = \frac{R_L \times V_{in}}{R_S + R_L} = \frac{1200 \times 16}{1000 \times 1200} = 8.73 \text{ V} = V_L$$

Now, the drop across R_S is given by

$$V_{RS} = V_{in} - V_L = 16 - 8.73 \text{ V} = 7.27 \text{ V}$$

Since $V_Z' < V_Z$, the Zener diode will not be in the breakdown region and hence the Zener current can be approximately zero; $I_Z = 0$ A.

And the power dissipated by the zener will be

$$P_Z = V_Z \times I_Z = 10 \times 0 = 0 \text{ W}$$

2. Fixed V_{in} and Variable R_L

Due to the reference voltage V_Z, there is a specific range of resistor values for R_L and hence the load current that will ensure the Zener is in the "ON" state. A smaller value of load resistance R_L will result in a voltage V_O across the load resistor less than V_Z and the Zener diode will be in the "OFF" state. The minimum load resistance that will turn the Zener diode ON can be calculated referring to Fig. 2.17(a) as below:

$$V_o = V_z = \frac{R_L \times V_{in}}{R_S + R_L}$$

Solving for R_L, we have

$$R_{Lmin} = \frac{R_S \times V_z}{V_{in} \times V_z} \tag{2.66}$$

Any load resistance value greater than the R_{Lmin} will ensure that the Zener diode is in the "ON" state and the diode can be replaced by its V_Z source equivalent. The condition defined by Eq. (2.66) establishes the minimum R_L, in other words specifies the maximum I_L as

$$I_{Lmax} = \frac{V_o}{R_{Lmin}} \tag{2.67}$$

Once the diode is in the "on" state, the voltage across R_S remains fixed at

$$V_{RS} = V_{in} - V_Z \tag{2.68}$$

and I_R remains fixed at $I_R = \dfrac{V_o}{R_{Lmin}}$

The Zener current is given by $I_Z = I_R - I_L$ and will be a minimum I_{Zmin} when I_L is a maximum and a maximum I_{Zmax} when I_L is a minimum value, since I_R is constant. Since I_Z is limited to I_Z(rated) as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_Z(rated) for I_Z establishes the minimum I_L as

$$I_{Lmin} = I_R - I_{Z(rated)}$$

and the maximum load resistance as

$$R_{Lmax} = \frac{V_z}{I_{Lmin}} \tag{2.69}$$

3. Variable V_{in} and Fixed R_L

For fixed values of R_L in Fig. 2.17, the voltage V_i must be sufficiently large to turn the Zener diode ON. The minimum turn-on voltage is determined by the equation

$$V_z = \frac{V_i \times R_L}{R_L + R} \tag{2.70}$$

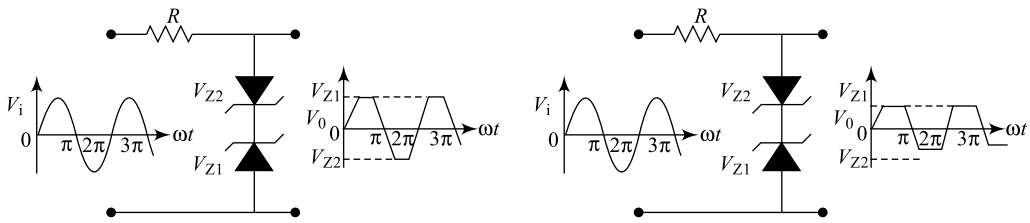
This results in a minimum value of V_i as

$$V_{i(min)} = \frac{V_z\,[(R_L] + R)}{R_L}$$

Similarly,
$$V_{i(max)} = V_{R(max)} + V_Z = I_{R(max)} \times R + V_Z \tag{2.71}$$

2.8.2 AC Regulator and Square-Wave Generator

Two back-to-back connected Zener diodes can function as an ac regulator and can be used to regulate an ac input source as shown in Fig. 2.18(a). For the sinusoidal signal V_i shown, during positive half-cycle, the Zener Z_2 will be forward biased offering a low-resistance path and Z_1 will be reverse biased regulating the signal to V_{Z1}. Similarly, during negative half-cycle, the Zener Z_1 will be forward biased offering a low-resistance path and Z_2 will be reverse biased regulating the signal to V_{Z2}. The resulting output for the full range of V_i is provided in the figure. Note that the waveform is not purely sinusoidal, but its root mean square (rms) value is lower than that associated with a full peak signal. The network is effectively limiting the rms value of the available voltage. The network of Fig. 2.18(a) can be extended to that of a simple square-wave convertor (due to the clipping action) if the signal V_i is increased to perhaps a very high peak with input and output waveforms as shown in Fig. 2.18(b).



(a) Zener ac voltage regulator (b) Square-wave converter

Fig. 2.18 Zener ac voltage regulator

2.9 VOLTAGE-MULTIPLIER CIRCUITS

A *voltage multiplier* is a specialised rectifier circuit producing a dc output which is theoretically an integer times the ac peak input, for example 2, 3 or 4 times the ac peak input. Thus, it is possible to get 200 V dc output from a 100 V_{peak} ac source using a doubler, 400 V dc from a quadrupler and so on; however, the current level remains unchanged. A voltage multiplier finds its application in areas like television (TV) sets where a large dc voltage supply is required (colour TV sets use voltages in the order of few 10s of kVs) and producing such high voltages using conventional transformers will be bulky and noisy. The voltage multiplier circuits are very compact and cost-effective requiring only diodes and capacitors.

2.9.1 Voltage Doubler

A half-wave voltage doubler circuit is shown in Fig. 2.19(a); it consists of two circuits: a clamper formed using a diode D_2 and a capacitor C_2, and a peak detector (half-wave rectifier) formed using a diode D_1 and a capacitor C_1. During the positive voltage half-cycle of the input voltage, the diode D_1 conducts and the diode D_2 is cut off, charging capacitor C_1 up to the peak rectified voltage (V_m). Diode D_1 is ideally a short during this half-cycle, and the input voltage charges capacitor C_1 to V_m. During the negative half-cycle of the input voltage, the diode D_1 is cut off and the diode D_2 conducts the charging capacitor C_2. Since the diode D_2 acts as a short during the negative half-cycle and the diode D_1 is open, we can sum the voltages around the outside loop from which we obtain $V_{C2} = 2V_m$. On the next positive half-cycle, the diode D_2 is not conducting and the capacitor C_2 will discharge through the load. If no load is connected across capacitor the C_2, both capacitors stay charged—C_1 to V_m and C_2 to $2V_m$. If

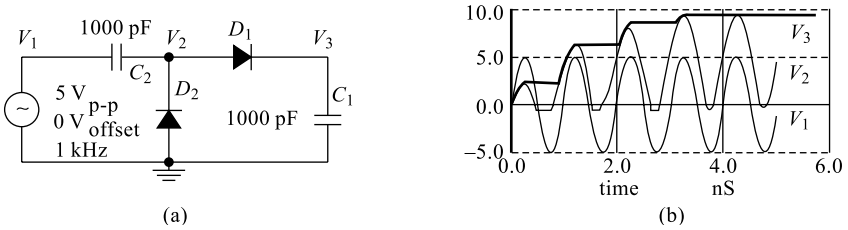


Fig. 2.19 (a) Half-wave Voltage doubler (b) Waveforms: V_1—input, V_2—clamper o/p and V_3—final o/p

there is a load connected to the output of the voltage doubler, the voltage across the capacitor C_2 drops during the positive half-cycle at the input and the capacitor is recharged up to $2V_m$ during the negative half-cycle. The output waveform across the capacitor C_2 is that of a half-wave signal filtered by a capacitor filter. The peak inverse voltage across each diode is $2V_m$.

Referring to diagrams shown above, C_2 charges to 5 V (considering an ideal diode) on the negative half cycle of ac input due to the clamping action. The right end is grounded by the conducting D_2 and the left end is charged at the negative peak of the ac input. During the positive half-cycle, the half-wave rectifier comes into play and the diode D_2 is out of the circuit since it is reverse biased. C_2 is now in series with the voltage source and note the polarities of the generator and C_2, series aiding. Thus, the rectifier D_1 sees a total of 10 V at the peak of the sine wave, 5 V from generator and 5 V from C_2. D_1 conducts the waveform V, charging C_1 to the peak of the sine wave riding on 5 V dc. This waveform is the output of the doubler, which stabilises at 10 V after a few cycles of sine wave input.

A **full-wave voltage doubler** is composed of a pair of series-stacked half-wave rectifiers and is indicated in Fig. 2.20 along with the waveforms. The bottom rectifier charges C_1 on the negative half-cycle of the input. The top rectifier charges C_2 on the positive half-cycle. Each capacitor takes on a charge of 5 V. The output at the node 2 is the series total of $C_1 + C_2$ or 10 V.

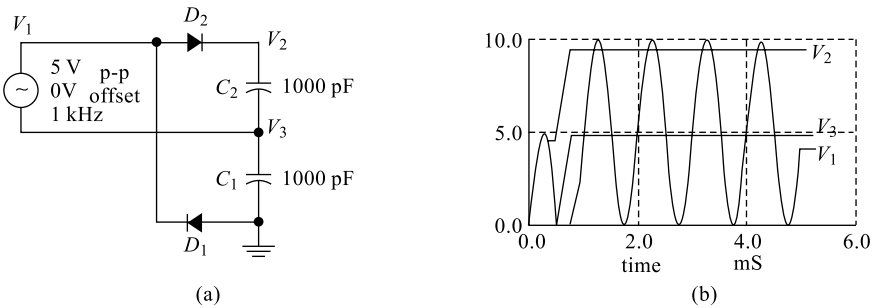


Fig. 2.20 (a) Full-wave voltage doubler (b) Waveforms: V_1—input and V_2—final output

Note that the output V_2 in the diagram reaches full value within one cycle of the input V_1 excursion. This figure illustrates the derivation of the full-wave doubler from a pair of opposite polarity half-wave rectifiers. The negative rectifier is re-wired to share one voltage source with the positive rectifier. This yields a ±5 V power supply; though, 10 V is measurable between the two outputs. The ground reference point is moved so that +10 V is available with respect to ground.

2.9.2 Voltage Tripler

A voltage tripler is built from a combination of a doubler and a half-wave rectifier (C_3, D_3). The half-wave rectifier produces 5 V (4.3 V) at the node 3. The doubler provides another 10 V (8.4 V) between nodes 2 and 3 for a total of 15 V (12.9 V) at the output node 2 with respect to ground.

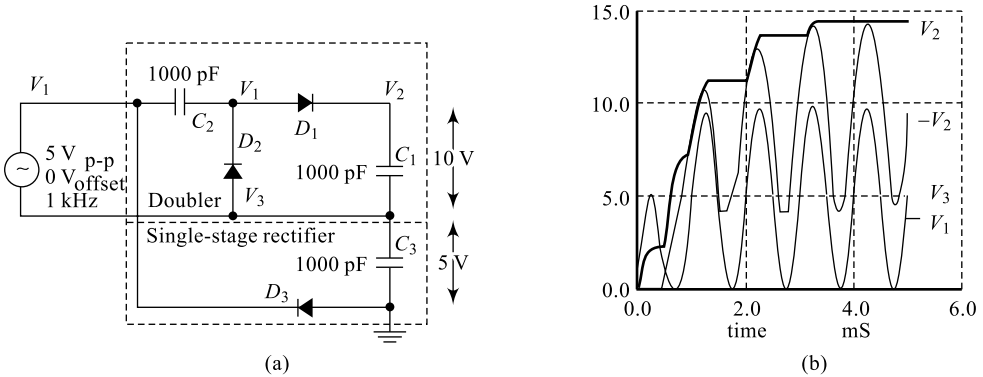


Fig. 2.21 (a) Voltage tripler circuit (b) Voltage tripler output waveforms

Note that $V(3)$ in Fig. 2.21(b) rises to 5 V (4.3 V) on the first negative half-cycle. Input $V(4)$ is shifted upward by 5 V (4.3 V) due to 5 V from the half-wave rectifier. And 5 V more at $V(1)$ due to the clamper (C_2, D_2). D_1 charges C_1 (waveform $V(2)$) to the peak value of $V(1)$.

2.9.3 Voltage Quadrupler

A voltage quadrupler is a stacked combination of two doublers shown in Fig. 2.22(a). Each doubler provides an output of 10 V for a series total at the node 2 so that the total output V_2 with respect to ground is 20 V. The waveforms of the quadrupler are shown in Fig. 2.22(b).

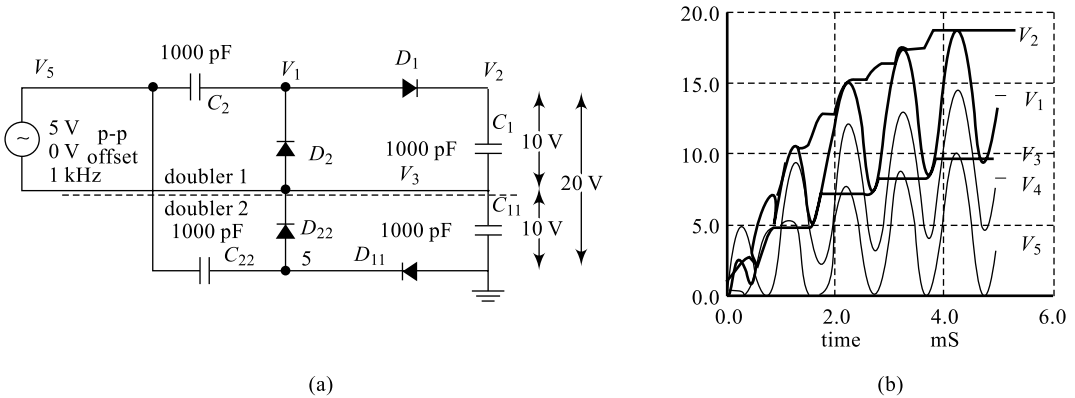


Fig. 2. 22 (a) Voltage quadrupler (b) Voltage-quadrupler output waveforms

It is worthwhile to point out some of the important notes on these voltage multipliers at this point. The circuit parameters used in the examples (V = 5 V, 1 kHz, C = 1000 pf) do not provide much current,

a current in the order of only microamperes is available. Furthermore, load resistors are not included as a part of the circuit, loading reduces the voltages from those indicated. If the circuits are to be driven by a kHz source at low voltage, as in the examples, the capacitors are usually 0.1 to 1.0 μF so that few milliamperes of currents are available at the output. If the multipliers are driven from 50/60 Hz, the capacitor are a few hundred to a few thousand microfarads to provide hundreds of milliamperes of output current. If driven from line voltage, pay attention to the polarity and voltage ratings of the capacitors. Finally, any direct line driven power supply (no transformer) is dangerous to the experimenter and line-operated test equipment. Commercial direct-driven supplies are safe because the hazardous circuitry is in an enclosure to protect the user. When bread-boarding these circuits with electrolytic capacitors of any voltage, the capacitors will explode if the polarity is reversed. Such circuits should be powered up behind a safety shield.

A voltage multiplier of cascaded half-wave doublers of arbitrary length is known as a Cockcroft-Walton multiplier and is shown in Fig. 2.23. This multiplier is used when a high voltage at low current is required. The advantage over a conventional supply is that an expensive high-voltage transformer is not required—at least not as high as the output.

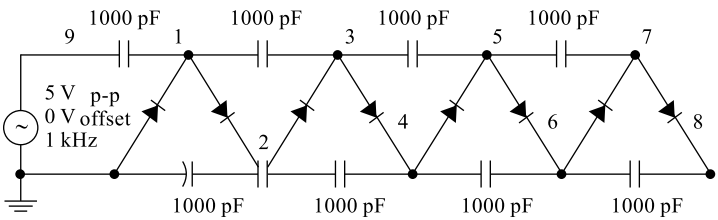


Fig. 2.23 Cockcroft-Walton *x*8 voltage multiplier

The pair of diodes and capacitors to the left of nodes 1 and 2 in the diagram constitute a half-wave doubler. Four of the doubler sections are cascaded to the right for a theoretical *x*8 multiplication factor so that the output voltage is V_{in} *x* 8. Node 1 has a clamper waveform, a sine wave shifted up by 1*x* (5 V). The other odd-numbered nodes are sine waves clamped to successively higher voltages. Node 2, the output of the first doubler, is a 2*x* dc voltage. Successive even-numbered nodes charge to successively higher voltages: Without diode drops, each doubler yields $2V_{in}$ or 10 V and for a total of 4 doublers, one expects an ideal output of 40 V. The major drawback of the Cockcroft-Walton multiplier is that each additional stage adds less than the previous stage. Thus, a practical limit to the number of stages exist. It is possible to overcome this limitation with a modification to the basic circuit. Also note the time scale of 40 ms compared with 5 ms for previous circuits. It required 40 ms for the voltages to rise to a terminal value for this circuit. The Cockcroft-Walton multiplier serves as a more efficient high-voltage source for photomultiplier tubes requiring up to 2000 V. Moreover, the tube has numerous **dynodes**, terminals requiring connection to the lower voltage "even-numbered" nodes. The series string of multiplier taps replaces a heat generating resistive voltage divider of previous designs. Voltage-multiplier circuits are employed to maintain a relatively low-transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.

2.10 CLIPPING CIRCUITS

In sections 2.4 to 2.6 on rectifiers, it is clearly observed that diodes can be used as switches for wave-shaping applications of an input waveform. Here, in this section on clippers we will further elaborate

on the wave-shaping capabilities of diodes. Clipping is a process in which one or two parts of the input waveform is eliminated(clipped) above or below certain reference level and rest of the waveform is passed to the output without any distortion. Thus, **clippers** are the circuits that clip or remove away a portion of an input signalwithout distorting the remaining part of the applied waveform. These circuits can also be referred to as waveform **limiters** or amplitude **selectors** or waveform **slicers**. An ideal diode exhibits a discontinuity in slope at the cut-in voltage and is called **break point**. There are two general forms of clippers: **series clippers** and **parallel clippers**. In a series clipper, the diode will be in series with the load and in a parallel clipper, the diode will be in shunt with the load; there is nothing much to choose between the two.

Transfer Characteristics of a Diode Clipper

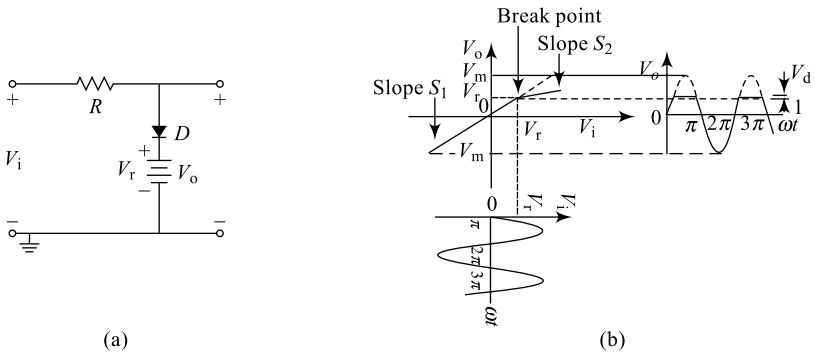


Fig. 2.24 (a) Diode Clipper (b) Transfer characteristics

Consider the diode clipper circuit shown in Fig. 2.24 (a) with the input signal $V_i = V_m \sin \omega t$; diode D has a cut-in voltage V_d, a forward resistance R_f and a reverse resistance R_r. For all values of $V_i < (V_r + V_d)$, diode will be reverse biased and the equivalent circuit in Fig. 2.24(a) can be used to obtain the output. Referring to the equivalent circuit, the output is given by

$$V_o = V_i \times \frac{R_r}{R + R_r} \tag{2.72}$$

Here, $\dfrac{R_r}{R + R_r}$ represents slope of the transfer curve; normally $R_r >> R$ and hence slope $s_1 \approx 1$ resulting in $V_o \approx V_i$.

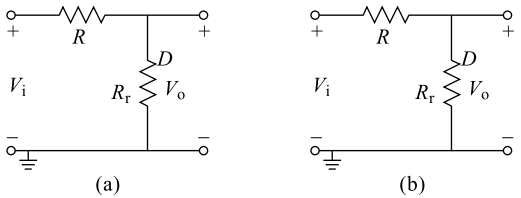


Fig. 2.25 (a) OFF-STATE equivalent cicuit (b) ON-STATE equivalent cicuit

Similarly, for all values of $V_i > (V_r + V_d)$, diode will be forward biased and the equivalent circuit in Fig. 2.25 (a) can be used to obtain the output. Referring to the equivalent circuit, the output is given by

$$V_o = V_i \times \frac{R_f}{R + R_L} \tag{2.73}$$

Here, $\frac{R_f}{R + R_f}$ represents slope of the transfer curve; normally $R_f << R$ and hence slope $s_2 \approx 0$ resulting in $V_o \approx V_r$. In summary, for all values of $V_i < (V_r + V_d)$, $V_o \approx V_i$ and for all values of $V_i > (V_r + V_d)$, $V_o \approx V_r$.

Selection of R

For clipping to be sharper magnitude of $V_i >> V_\gamma$, R should be larger than R_f when the diode is ON and for output to follow input R should be lesser than R_r when diode is OFF; hence the following two conditions are used:

$$R_r >> R \text{ say } R_r = k\,R \quad \Rightarrow \quad k = \frac{R_f}{R} \text{ and}$$
$$R >> R_f \text{ say } R = k\,R_f$$

$$R = \frac{R_f}{R} \times R_f$$

which implies that

$$R = \sqrt{R_r \times R_f} \tag{2.74}$$

Table 2.4 illustrates some of the important clipping circuits and their corresponding output waveforms. It can be observed here that in examples, the switching element diode can be either in series or parallel.

Example 2.13

For the network of Fig. 2.24(a), draw the output waveform if $V_r = 4.3$ V, $R = 1000\ \Omega$ and $V_i = 25 \sin \omega t$. Assume an Si diode is used.

Solution To determine the value of slope, diode resistances are required; since no information is available on the diode resistances, slope is taken as one and the resulting output waveform is drawn and is as shown in Fig. 2.26. The diode drop $V = 0.7$ V and hence the output is limited to $V = V_r + V_d = 4.3 + 0.7 = 5$ V on the positive half-cycle side. However, for $V_i < V$, diode is conducting and output just follows the input.

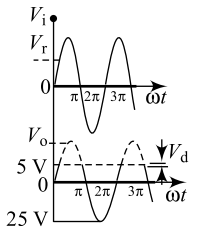
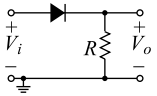
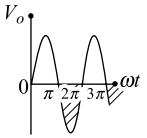
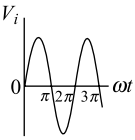
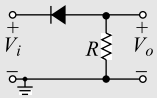
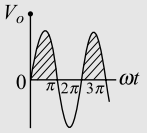
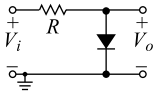
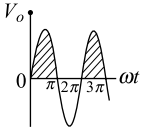
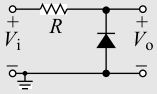
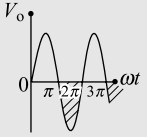
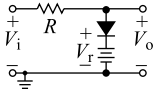
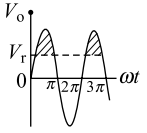
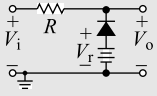
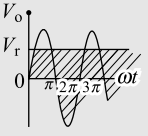
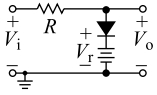
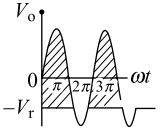
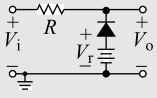
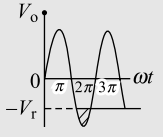


Fig. 2.26 Input-output waveforms for Example 2.13

2.11 CLAMPING CIRCUITS

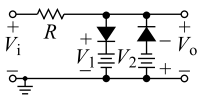
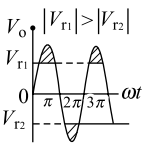
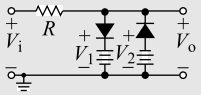
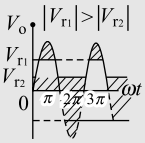
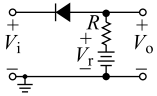
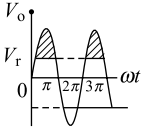
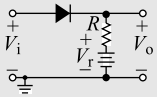
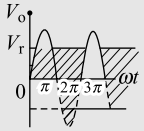
The previous section investigated a number of diode configurations that clipped off a portion of the applied signal without changing the remaining part of the waveform. This section will examine a variety of diode configurations that shift the dc level of an applied input signal to any required new dc level. The circuit diagram and the corresponding input, output waveforms for a basic clamper is shown in Fig. 2.27. Since the circuit is used to re-insert or restore the dc level to the input signal, the circuit can also be called **dc restorer** or **a dc re-inserter**.

Table 2.4 Different forms of clipping circuits

Sl. No.	Circuit	Output waveform	Remarks
1			 Input to all circuits shown is a sine wave. Series clipper, eliminates negative portions of the input.
2			Diode is assumed to be ideal in all cases. Series clipper, eliminates positive portions of the input.
3			Unbiased shunt clipper; eliminates positive portions of the input.
4			Unbiased shunt clipper; eliminates negative portions of the input.
5			Biased shunt clipper; eliminates positive portions of the input over a fixed reference V_r. (Circuits 5, 6, 7, 8, 11 and 12 are single-level clippers and use one reference)
6			Biased shunt clipper; eliminates negative portions of the input below a fixed reference V_r.
7			Biased shunt clipper; eliminates positive portions of the input over a fixed negative reference $-V_r$.
8			Biased shunt clipper; eliminates negative portions of the input below a fixed negative reference $-V_r$.

(*Contd.*)

(*Contd.*)

9			Biased shunt clipper; eliminates positive portions of the input over a fixed positive reference V_{r1} and negative portions of the input below a fixed negative reference $-V_r$.
10			Biased shunt clipper; eliminates positive portions of the input over a fixed positive reference V_{r1} and negative portions of the input below a fixed positive reference V_r. (Circuits 9 and 10 are two-level clippers and use two references)
11			Biased series clipper; eliminates positive portions of the input over a fixed reference V_r.
12			Biased series clipper; eliminates negative portions of the input below a fixed reference V_r.

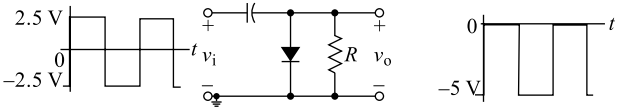


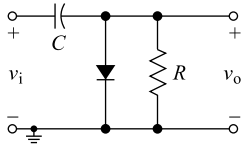
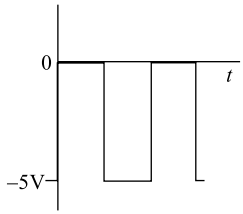
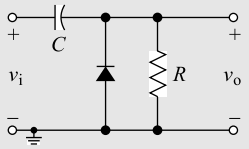
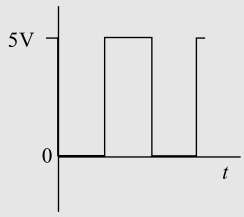
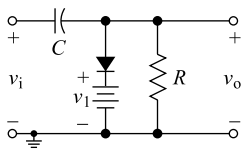
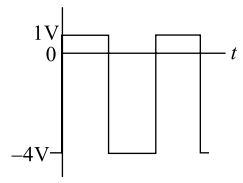
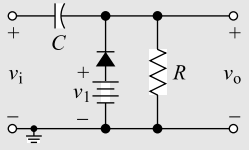
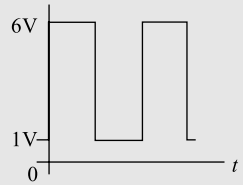
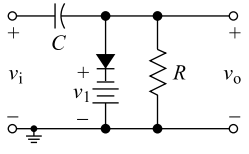
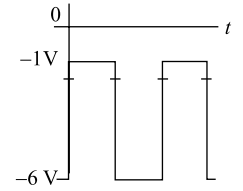
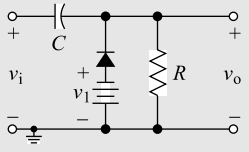
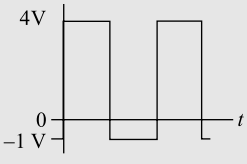
Fig. 2.27 Clamping circuit with input and output waveforms

A clamper is a network constructed using a diode, a resistor and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Additional shifts can also be obtained by introducing a dc supply to the basic structure. The resistor and capacitor of the network must be so chosen that the network time constant τ (product of R and C) is sufficiently large so that the voltage across the capacitor does not discharge significantly when the diode is in OFF state. Throughout the analysis, we assume that for all practical purposes, the diode is ideal and the capacitor fully charges or discharges in 5τ. Clamping networks have a capacitor connected directly from input to output with a resistor in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

For the network of Fig. 2.27, the diode will be forward biased for the positive portion of the applied signal. For the interval 0 to T_1, the diode is forward biased resulting in an effective resistance of approximately R_f ($R_f \parallel R$) and the time constant is very small because the resistor R_f is very small. The result is that the capacitor will quickly charge to the peak value of V volts. For the interval T_1 to T_2, the diode is reverse biased resulting in an effective resistance of approximately R ($R_r \parallel R$) and the time constant is very large because the resistor R is relatively large. The result is that the capacitor will not quickly discharge resulting in an output that is summation of $-V$ from source and $-V$ from the capacitor which is $2V$ volts. Table 2.5 illustrates different forms of biased and unbiased clippers along with their

Table 2.5 Different forms of clamping circuits

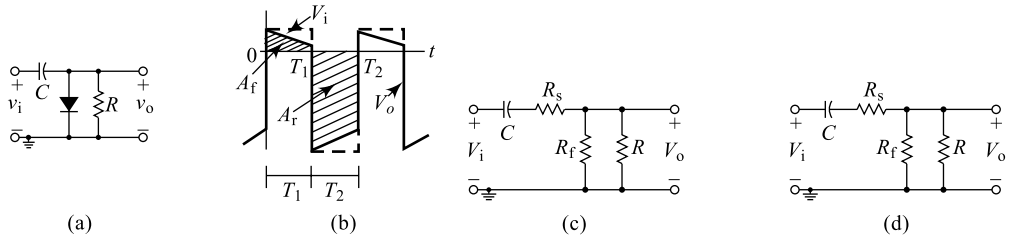
Sl.No.	Circuit	Output Waveform	Remarks
1			POSITIVE clamper (Unbiased)
2			NEGATIVE clamper (Unbiased)
3			A reference voltage of V_r = 1 V is assumed
4			A reference voltage of V_r = 1 V is assumed
5			A reference voltage of V_r = –1 V is assumed
6			A reference voltage of V_r = –1 V is assumed

output waveforms. The input shown for the basic circuit is only considered and a reference voltage with a magnitude of 1 V is assumed for simplicity. Circuits 1 and 2 are unbiased clampers and 3 to 6 are all biased clampers.

Clamping Theorem

Based on the working principle of a clamping network, the clamping theorem is proposed and it states. *In a clamping network with a square-wave input, the ratio of the area under the forward output curve (A_f) to the area under the reverse curve (A_r) will be equal to the ratio of forward resistance (R_f) to the external resistance of the circuit (R).*

$$\frac{A_f}{A_r} = \frac{R_f}{R_r} \tag{2.75}$$



(a) (b) (c) (d)

Fig. 2.28 (a) Clamping Circuit (b) Practical input and output waveforms (c) FB equivalent circuit (d) RB equivalent circuit

Proof: Consider the basic clamping circuit and its practical output waveform shown in Fig. 2.28; taking into account that the forward area and the reverse area are marked. In steady state, the output waveform being repetitive, the net accumulation of charges on the capacitor will be zero; the charges accumulated when the diode is forward biased will be given away when the diode is reverse biased and it can be given as below;

$$\Delta Q_f = \Delta Q_r$$

$$\int_0^{T_1} i_f\, dt = \int_{T_1}^{T_2} i_r\, dt$$

$$\int_0^{T_1} \frac{V_f}{R_f} dt = \int_{T_1}^{T_2} \frac{V_r}{R \| R_T} dt; \quad \text{since } R \| R_r \approx R \text{ we can write}$$

$$\frac{1}{R_f} \int_0^{T_1} V_f\, dt = \frac{1}{R} \int_{T_1}^{T_2} V_r\, dt \tag{2.76}$$

The terms under integration represent the respective areas and hence the equation can be re-written as

$$\frac{1}{R_f} A_f = \frac{1}{R} A_r$$

$$\frac{A_f}{A_r} = \frac{R_f}{R} \quad \text{Hence, the proof.}$$

Summary

- The network in which the device works determines the point of operation of the device.
- The operating point of a network is determined by the intersection of the network governing equation and an equation defining the device characteristics.
- An ideal diode is one which offers zero cut-in voltage, zero forward resistance and infinitely large reverse resistance.
- To determine the state of a diode, simply consider it as a resistor and find the polarity of the voltage across it; if the voltage across it has a forward-bias polarity then the diode is ON else it is OFF.
- Rectification is a process wherein an applied bipolar waveform (zero average value) is converted into an unipolar output (one that has a dc level).
- Practically, for applied signals of less than the cut-in voltage of a diode, rectification is not possible. For voltages less than $V\gamma$, special circuits called precession rectifiers (to be discussed in Chapter 6) have to be used.
- It is very important that the PIV rating of a diode be checked when choosing a diode for a particular application so that the device junction is not spoiled.
- For the conventional half-wave rectifier and full-wave bridge rectifier, PIV is the peak value of the input signal; but for the Centre Tapped (CT) transformer full-wave rectifier, it is twice the peak value of the input signal. A diode used for the first two types of rectifiers may not be straightaway used for a CT transformer FWR.
- Filter circuits are the networks that reduce the ripple components and increase the dc component in the rectified output input signal.
- Different forms of filters can be constructed of which the simplest form is C-filter.
- Clipping circuits are the networks that eliminate away a part of the input signal (maintaining the remaining part) either to create a specific type of signal or to limit the voltage that can be applied to a network.
- Clamping circuits are networks that push the input signal to a different dc level maintaining the peak-to-peak swing and the shape of the input signal.
- Zener diodes are diodes that have the Zener breakdown and used for voltage-regulation application. They are used in reverse-biased condition and the polarity under conduction is opposite to that of the conventional diode.
- A Zener diode can also be used for voltage references in improved forms of voltage regulators.
- To determine the state of a Zener diode in a dc network, determine the open-circuit voltage between the two points where the Zener diode is connected; if it is more than the Zener potential and has the correct polarity, then the Zener diode is ON.
- A voltage multiplier is a circuit used to increase voltage output, however, the current level is unaltered.
- A half-wave or full-wave voltage doubler uses two capacitors, a tripler uses three capacitors and a quadrupler uses four capacitors. The number of capacitors and diodes will be equal and depends on the multiplication value.
- Clipping and clamping circuits are both called nonlinear wave-shaping circuits since they employ the nonlinear device.
- A voltage multiplier is a circuit which does not use bulky transformers to increase voltage output and find a good number of applications.
- A clamping circuit is also called a dc restorer or dc re-inserter or a dc re-instater since it reintroduces dc level to the signal.

Review Questions

1. If the silicon diode in the circuit shown in Fig. 2.3 is replaced by a germanium diode, what changes do you observe in the circuit performance?
2. If the silicon diode in the circuit shown in Fig. 2.4 is replaced by a germanium diode, what changes do you observe in the circuit performance?
3. If the diode in the circuits shown in Fig. 2.3 and Fig. 2.4 is replaced by an ideal germanium diode, what changes do you observe in the circuit performance?
4. If the diode in the circuit shown in Fig. 2.5 is reverse connected by mistake, what changes do you observe in the circuit performance?
5. If the diode in the circuit shown in Fig. 2.5 has a reverse maximum voltage of 230 V and suddenly the supply voltage increases to 250 V, what is the effect of this on the circuit performance?
6. If the diode in the circuit shown in Fig. 2.5 has a nonzero forward resistance and the supply transformer has a nonzero secondary winding resistance. If both these resistances put together increase up to a value equal to R_L, what is the effect of this on the circuit conversion efficiency?
7. If the diodes in the circuit shown in Fig. 2.9 have different reverse maximum voltages of V_{m1} and V_{m2}, what is the effect of this on the circuit performance?
8. If the diodes in the circuit shown in Fig. 2.9 have different reverse maximum voltages of V_{m1} and V_{m2}, where $V_{m1} > V_{m2}$ and suddenly the supply voltage increases to V_{m1}, what is the effect of this on the circuit performance?
9. If the diodes in the circuit shown in Fig. 2.9 have a forward resistance and the secondary transformer resistance sum equal to load resistance then what is the effect of this on the circuit performance?
10. If the diodes in the circuit shown in Fig. 2.11 have a reverse maximum voltage of 230 V and suddenly the supply voltage increases to 250 V, what is the effect of this on the circuit performance?
11. If the diodes in the circuit shown in Fig. 2.11 have different reverse maximum voltages of $V_{m1,}$ $V_{m2,}$ V_{m3} and V_{m4}, what is the effect of this on the circuit performance?
12. If the two sets of diodes (D_1 and D_3) and (D_2 and D_4) in the circuit shown in Fig. 2.11 have different reverse maximum voltages of V_{m1} and V_{m2}, where $V_{m1} > V_{m2}$ and suddenly the supply voltage increases to V_{m1}, what is the effect of this on the circuit performance?
13. If the two sets of diodes (D_1 and D_3) and (D_2 and D_4) in the circuit shown in Fig. 2.11 have a forward resistance and the secondary transformer resistance sum equal to load resistance then what is the effect of this on the circuit performance?
14. Can we use the two sets of diodes (D_1 and D_3) and (D_2 and D_4) in the circuit shown in Fig. 2.11 in the circuit of Fig. 2.9? If yes then what is the care to be taken to safeguard the diodes?
15. The supply and output terminals of the circuit shown in Fig. 2.11 are interchanged by mistake; does the circuit still work as an FWR? Explain clearly.
16. The output waveforms of a FWR with C-filter is shown in Fig. 2.13, explain how do you get the output waveform.
17. In filter circuits, ***C*** is connected across (parallel to) the load and ***L*** is connected in series with the load; why?
18. What do you mean by regulation? Explain.
19. A Zener regulator has got very limited applications? Explain clearly.

Exercise Problems

1. A full-wave centre-tapped rectifier with a 220 V sinusoidal input has a load resistor of 5*k*.
   (a) If silicon diodes are employed, what is the dc voltage available at the load?
   (b) If ideal diodes are employed, what is the dc voltage available at the load?
2. A full-wave bridge rectifier with a 120 V rms sinusoidal input has a load resistor of 1*k* .
   (a) If silicon diodes are employed, what is the dc voltage available at the load?
   (b) If germanium diodes are employed, what is the dc voltage available at the load?
3. (a) Determine the required PIV rating of each diode and the maximum current through each diode during conduction in Problem 1.
   (b) What is the required power rating of each diode?
4. (a) Determine the required PIV rating of each diode and the maximum current through each diode during conduction in Problem 1.
   (b) What is the required power rating of each diode?
5. (a) A capacitor filter is to be used with an FWR working at 100 Hz to provide an output voltage of 10 V at a load of 1 mA. If the maximum allowable ripple is 0.1%, what is the size of the filter?
   (b) If the ripple voltage is to be kept below 0.01% in Part (a), what is the new value of capacitor required?
6. (a) A capacitor filter is to be used with an HWR working at 100 Hz to provide an output voltage of 10 V at a load of 1 mA. If the maximum allowable ripple is 0.1%, what is the size of the filter?
   (b) If the ripple voltage is to be kept below 0.01% in Part (a), what is the new value of capacitor required?
7. In the circuit of Fig. P2.7, the filter size varies from 2.5 μF to 25 μF. Estimate the resulting maximum and minimum ripple values if the load is 2.2 kΩ.

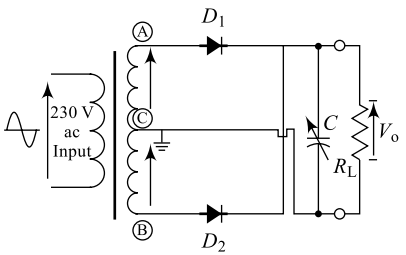


Fig. P2.7

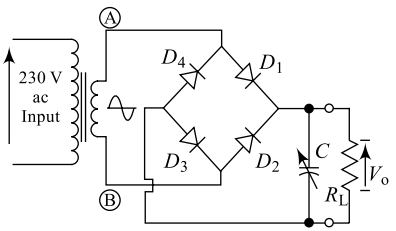


Fig. P2.8

8. In the circuit of Fig. P2.8, the filter size varies as 2.5 μF to 25 μF. Estimate the resulting maximum and minimum ripple values if the load is 2.2 kΩ.
9. In the circuit of Fig. P2.8, if the 4-diode FWR is replaced by a 2-diode FWR, what difference do you need to maintain for the diodes, maintaining all other constraints.
10. In the circuit of Fig. P2.8, if FWR is replaced by an HWR, what difference do you observe in the resulting maximum and minimum ripple values?
11. (a) A bridge rectifier with a C-filter is working at a frequency of 100 Hz and is supplying a load of 10 mA at 10 V. If the present ripple factor of 2% is to be halved, suggest a suitable filter size.

(b) Assuming capacitors are available only in one standard value, indicate a suitable filter connection.

12. (a) How do you define for a regulator?
    (b) There are two regulators; reg-A with +5% regulation and reg-B with +3% regulation. Which one is a better regulator and why?
13. For the network of Fig. P2.13, determine the range of V_i that will maintain V_L at 8 V and not exceed the maximum power rating of the Zener diode.

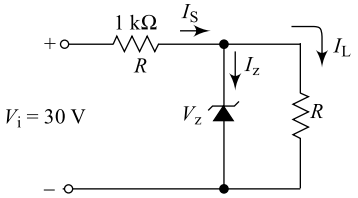


Fig. P2.13

14. For the Zener diode network of Fig. 2.17(a), the Zener breakdown voltage is reduced from 10 V to 6.3 V with all other parameters maintained, Determine V_L, V_{Rs}, I_Z and P_Z.
15. For the network of Fig. P2.15, determine the range of R_L and I_L that will result in a V_{RL} of 10 V.

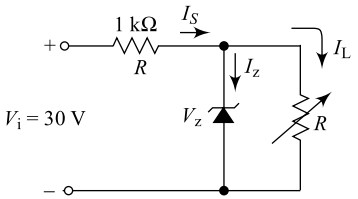


Fig. P2.15

16. Determine the maximum wattage rating of the Zener diode in Problem 15.
17. The network shown in Fig. P2.17 uses an Si diode and the magnitude of the reference voltage is 5 V. The input is a sine wave of 20 V peak; sketch the output waveform.

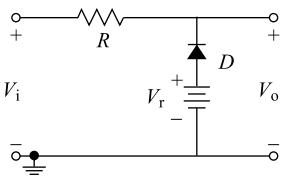


Fig. P2.17

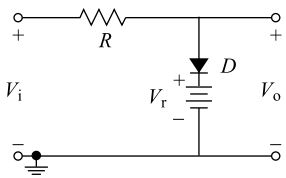


Fig. P2.18

18. (a) The network shown in Fig. P2.18 uses an ideal Ge diode and the magnitude of the reference voltage is 5 V. The input is a sine wave of 20 V peak; sketch the output waveform.
    (b) If by mistake the supply voltage is reversed, what is the effect on the output?

19. The network shown in Fig. P2.19 uses an Si diode; sketch the output waveform if the input is a sine wave of 20 V peak to peak.

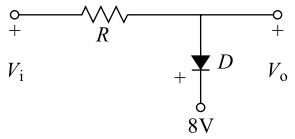


Fig. P2.19

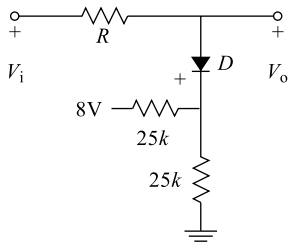


Fig. P2.20

20. The network shown in Fig. P2.20 uses a Si diode. Sketch the output waveform if the input is a sine wave of 20 V peak to peak.
21. The network shown in Fig. P2.21 uses an Si diode. Sketch the output waveform if the input is a sine wave of 20 V peak to peak.

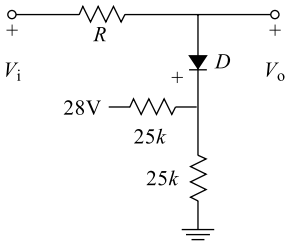


Fig. P2.21

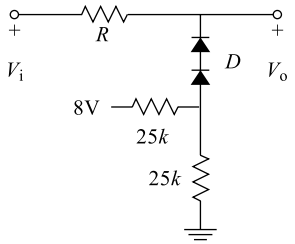


Fig. P2.22

22. The network shown in Fig. P2.22 uses an Si diode. Sketch the output waveform if the input is a sine wave of 20 V peak to peak.
23. The clamper networks shown in Fig. P2.23 use an Si diode. Sketch the output waveform if the input is a sine wave of 20 V peak to peak.

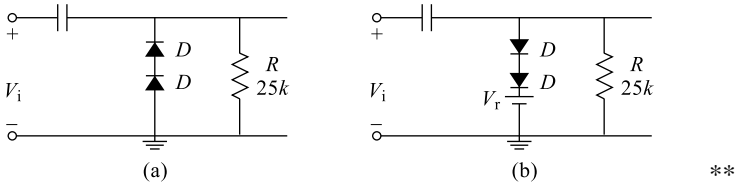


Fig. P2.23

**

24. (a) Find the voltage limiting levels for the network shown in Fig. P2.24; the diode used are Si diodes.
    (b) Sketch the output waveform if the input is a sine wave of 20 V peak to peak.

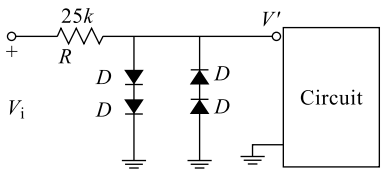


Fig. P2.24

25. (a) Find the voltage-limiting levels for the network shown in Fig. P2.25; the diodes used are Si diodes.
    (b) Sketch the output waveform if the input is a sine wave of 120 mV peak.

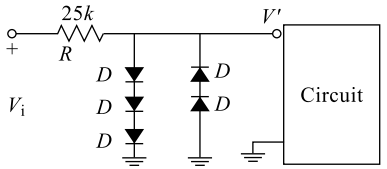


Fig. P2.25

Multiple-Choice Questions

1. All electronic circuits for their working and operation require
   (a) ac source (b) dc source (c) both (a) and (b) (d) no source
2. The electronic circuit that generates dc power from an available ac source is
   (a) power supply (b) amplifier (c) oscillator (d) all the above
3. A power-supply unit consists of
   (a) a rectifier (b) a filter (c) a regulator (d) all the above
4. The output of which unit of a power supply contains maximum dc components?
   (a) A rectifier (b) A transformer (c) A filter (d) None
5. A transformer in a power-supply unit necessarily
   (a) isolates high-tension unit from low-tension units
   (b) steps down i/p
   (c) amplifies i/p
   (d) both (a) and (b)
6. The turns ratio in a transformer is related to primary and secondary parameters through
   (a) $N_1/N_2 = I_1/I_2 = V_1/V_2$ (b) $N_1/N_2 = I_2/I_1 = V_2/V_1$
   (c) $N_1/N_2 = I_2/I_1 = V_1/V_2$ (d) none
7. The rectifier of a power-supply unit is also called
   (a) a converter (b) a transformer (c) an inverter (d) none
8. The output of a rectifier in a power-supply unit is
   (a) a pure ac (b) a pure dc (c) a pulsating dc (d) none
9. The unit in a power supply that minimises the ripples is
   (a) a rectifier (b) a transformer (c) a regulator (d) a filter
10. The ripple factor in a rectifier output is the signal ratio of
    (a) output ac to output dc (b) output dc to output ac
    (c) output ac to input ac (d) none
11. The unit in a power supply that provides constant dc against certain variations is
    (a) a rectifier (b) a transformer (c) a filter (d) a regulator
12. The conversion efficiency of a full-wave rectifier output is ideally
    (a) 0.48 (b) 1.21 (c) 0.812 (d) 0.406
13. The TUF in a half-wave rectifier is ideally
    (a) 0.48 (b) 1.21 (c) 0.286 (d) 0.693

14. The TUF in a centre-tapped full-wave rectifier is ideally
(a) 0.48 (b) 1.21 (c) 0.286 (d) 0.693
15. The TUF in a bridge-type full-wave rectifier is ideally
(a) 0.812 (b) 1.21 (c) 0.286 (d) 0.693
16. The PIV in a half-wave rectifier is ideally equal to
(a) $0.25V_m$ (b) $0.5V_m$ (c) $2V_m$ (d) V_m
17. The TUF in a centre-tapped full-wave rectifier is ideally
(a) $0.25V_m$ (b) $0.5V_m$ (c) $2V_m$ (d) V_m
18. The TUF in a bridge-type full-wave rectifier is ideally
(a) $0.25V_m$ (b) $0.5V_m$ (c) $2V_m$ (d) V_m
19. In a half-wave rectifier without a filter, if the transformer secondary has a peak ac voltage of $15\sqrt{2}$ V then the maximum dc output voltage is
(a) $15/\sqrt{2}$ V (b) $15 \times \sqrt{2}$ V (c) 66.64 V (d) 6.75 V
20. In a centre-tapped full-wave rectifier without a filter, if the transformer secondary has a peak ac voltage of $15\sqrt{2}$ V then the maximum dc output voltage is
(a) $15/\sqrt{2}$ V (b) 13.5 V (c) $15 \times \sqrt{2}$ V (d) 6.75 V
21. In a bridge-type full-wave rectifier without a filter, if the transformer secondary has a peak ac voltage of $15\sqrt{2}$ V then the maximum dc output voltage is
(a) $15/\sqrt{2}$ V (b) 13.5 V (c) $15 \times \sqrt{2}$ V (d) 6.75 V
22. The output frequency of a half-wave rectifier working with 1 kHz i/p signal is
(a) 1 kHz (b) 2 kHz (c) 500 Hz (d) zero
23. The output frequency of a centre-tapped full-wave rectifier working with 1 kHz i/p signal
(a) 1 kHz (b) 2 kHz (c) 500 Hz (d) zero
24. The output frequency of a bridge-type full-wave rectifier working with 1 kHz i/p signal is
(a) 1 kHz (b) 500 Hz (c) 2 kHz (d) zero
25. In the construction of a filter circuit inductor L is always connected in _____ and a capacitor C is always connected in _____ with the load.
(a) series, shunt (b) shunt, series (c) shunt, shunt (d) series, series
26. The clamping circuit is also known as
(a) an ac restorer (b) a dc restorer (c) an inverter (d) a converter
27. A Zener diode in a power supply is mainly used for
(a) dc restoring (b) rectification (c) regulation (d) filtering
28. The clamping theorem relates A_f, A_r, R_f and R_r in the following way:
(a) $A_f/A_r = R_f/R_r$ (b) $A_f/A_r = R_r/R_f$ (c) $A_f/A_r = 1/(R_f \times R_r)$ (d) $A_f/A_r = R_f/R_r$
29. The function of a bleeder resistor in a filter of a power supply is to
(a) decrease the performance of the filter
(b) increase the ripple factor
(c) maintain minimum current drain for the inductor
(d) to serve as load
30. The output frequency of a bridge-type full-wave rectifier working with 1 kHz i/p signal is
(a) 1 kHz (b) 500 Hz (c) 2 kHz (d) zero
31. If the input frequency of a bridge-type full-wave rectifier with a C-filter is doubled maintaining all other circuit components same then its ripple factor is
(a) doubled (b) halved (c) remains same (d) zero

32. If the filter size of a bridge-type full-wave rectifier with a C-filter is doubled maintaining all other circuit components same then its ripple factor is
    (a) doubled (b) zero (c) remains same (d) halved
33. Inductor/Choke input filters are not recommended to work with low-frequency rectifiers, because _____ and will be difficult to maintain.
    (a) **L** size will be large (b) **C** size will be large
    (c) **L** size will be small (d) **C** size will be large
34. The regulation of an ideal regulator should be
    (a) maximum (b) minimum (c) zero (d) nonzero

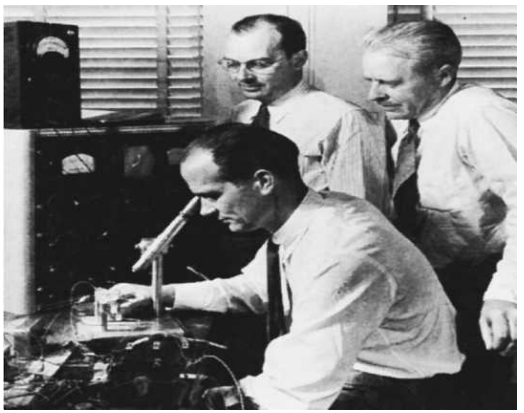
Bipolar Junction Transistors

3

Goals and Objectives

Upon completion of this chapter, the reader of the book is expected to

- Recall all the basic concepts of semiconductor materials and a *PN* junction from Chapter 1
- Understand the construction of the bipolar junction transistor (BJT)
- Understand the basic operation of the bipolar junction transistor
- Understand the active region, the saturation region and the cut-off region of BJT operation
- Understand the proper biasing that ensures BJT operation in the active region
- Draw and analyze the load line for a BJT
- Draw and explain the characteristics of *NPN* or *PNP* transistors
- Understand the important parameters of a BJT such as current gain, voltage gain, etc.
- Understand different BJT configurations namely CE, CB and CC configurations
- Compare performances of different BJT configurations namely CE, CB and CC configurations
- Understand the working and design procedure for BJT amplifiers
- Understand the basic operation of a transistor as a switch
- Perform the load-line analysis of different BJT configurations and fix up the *Q*-point
- Understand the concept of stability and importance of stability factors
- Understand the concept of circuit designs using *NPN* and *PNP* transistors
- Compare performance of different BJT biasing methods
- Understand the concept and need of bias stabilisation
- Feel confident of moving to the applications (next) chapter



Co-inventors of the first transistor at Bell Laboratories: (Courtesy of AT&T Archives.)

Dr. Shockley Born: (seated) **London**, England, 1910
PhD Harvard, 1936

Dr. Bardeen Born: (left) **Madison**, Wisconsin, 1908
PhD Princeton, 1936

Dr. Brattain Born: Amoy, China, 1902
PhD University of Minnesota, 1928

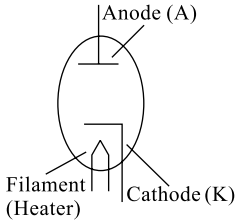
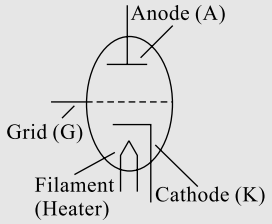
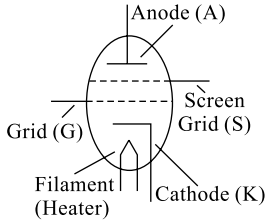
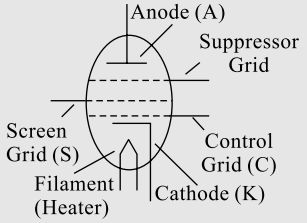
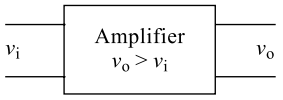
All shared the Nobel Prize in 1956 for this contribution

3.1 INTRODUCTION

In previous chapters, you learnt that a semiconductor diode with one junction and two terminals can be used in rectification of an ac signal, clipping an input signal, clamping an input signal (wave-shaping applications), etc. But, the two-terminal device fails to increase the strength of a weak signal (amplification) and hence a three-terminal device such as a transistor can be used to provide the required amplification. A transistor is a three-terminal, two-junction semiconductor device that is mainly used for amplification. On December 23, 1947, Walter H Brattain and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories. This three-terminal solid-state device had a number of advantages over the vacuum tubes: it was smaller in size and lightweight, it had no heater required and heater loss, it had a rugged construction, it was more efficient since less power was absorbed by the device itself and it required no warm-up period and operated at lower voltages. The components such as a resistor, a capacitor or an inductor are all passive and dissipate power; even a transformer that is capable of giving a voltage gain to a circuit is not an active element. Active elements in a circuit increase the power by controlling or modulating the flow of power from an additional power supply into the circuit. An **amplifier** (device that increases the voltage, current or power level) will be an example of an active device and all amplifiers have at least three terminals, with one controlling the flow between the other two. It is already mentioned that before the invention of the transistor in 1947, vacuum tubes had been used for more than 40 years (during 1904 to 1947). Table 3.1 illustrates the vacuum tube generation and their inventors. Vacuum-tubes were replaced by solid-state devices and that led to a revolution in the electronics industry.

Transistors are active circuit elements that are typically made from silicon or germanium materials and available in two forms; the *NPN* and *PNP*. The Bipolar Junction Transistor (BJT) controls the current by varying the number of charge carriers and the Field Effect Transistor (FET) controls the current by varying the shape of the conducting volume. This chapter includes all the basics of a transistor: construction, its working principle, different configurations and the biasing techniques used to fix up the operating point for the device.

Table 3.1 Transistor ancestors

Sl. No.	Device Name	Year of Invention	Inventor
1	 vacuum-tube diode	1904	J A Fleming
2	 vacuum-tube triode	1906	Lee De Forest
3	 vacuum-tube tetrode	1927	Dr Hull
4	 vacuum-tube pentode	1929	Dr Hull
5	 Amplification	23.12.1947	Walter H Brattain and John Bardeen

3.2 TRANSISTOR CONSTRUCTION AND OPERATION

A Bipolar Junction Transistor (BJT) is a three-layer, two-junction semiconductor device consisting of either two *N*-type and one *P*-type layers of material (*NPN* transistor) or two *P*-type and one *N*-type layers of material (*PNP* transistor). A transistor can be visualised as two back-to-back connected diodes; by placing two *PN* junctions together, we can create a bipolar transistor with the three terminals—emitter, base and collector. The term *bipolar* is to justify the fact that holes and electrons participate in the injection process into the oppositely polarised material. If only one carrier is employed (electron or hole), it is considered a unipolar device. For proper working of the transistor, the two junctions of the transistor should be properly biased, the **base-emitter (J_1) junction** should be forward biased and the **base-collector (J_2) junction** should be reverse biased. In a *PNP* transistor, the majority charge carriers are holes and germanium is favoured for these devices. In an *NPN* transistor the majority charge carriers are electrons and silicon is best for *NPN* transistors. The thin and lightly doped middle layer is known as the base (*B*) and the two outer regions are known as the emitter (*E*) and the collector (*C*). The outer layers have widths much greater than the middle *P*-type or *N*-type layer and the doping of this base layer is also considerably less than that of the outer layers (typically, l0: l or less). The lower doping level limits the number of free charge carriers in this layer and decreases the conductivity (increases the resistance) of this material. Under the proper operating conditions, the emitter region emits or injects majority charge carriers into the base region and because the base is very thin, most of these electrons will ultimately reach the collector. The emitter is highly doped to reduce resistance and emit more majority charge carriers. The collector is lightly doped to reduce the junction capacitance of the collector-base junction. The schematics and the circuit symbols for bipolar transistors are shown in Fig. 3.1. The arrows on the schematic symbols indicate the direction of emitter-current flow. The collector is usually at a higher voltage than the emitter and for proper operation, the base-emitter junction is forward biased while the collector-base junction is reverse biased.

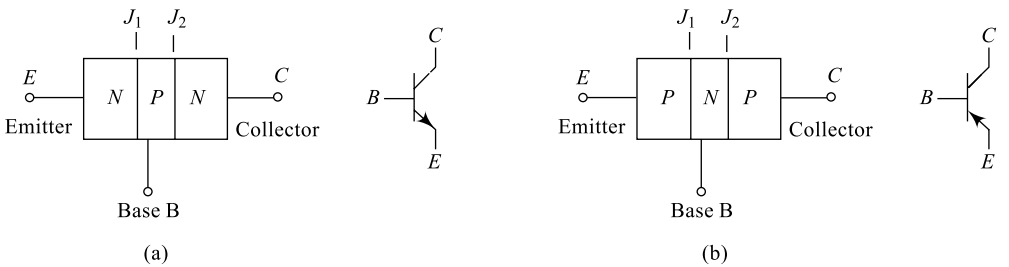


Fig. 3.1 (a) *NPN* transistor and symbol (b) *PNP* transistor and symbol

We will find later in this chapter that dc biasing is necessary to establish the proper region of operation for ac amplification. The basic operation of the transistor will now be described using the *PNP* transistor, and the operation of the *NPN* transistor is exactly similar if the roles played by the electrons and holes are interchanged. Consider only the forward bias applied to J_1 as shown in Fig. 3.2(a). The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the *P*-type to the *N*-type material. Let us now remove the base-to-emitter bias of the transistor and apply a reverse bias to J_2; the flow of majority carriers is now zero, resulting in only a minority-carrier flow, as indicated in Fig. 3.2(b).

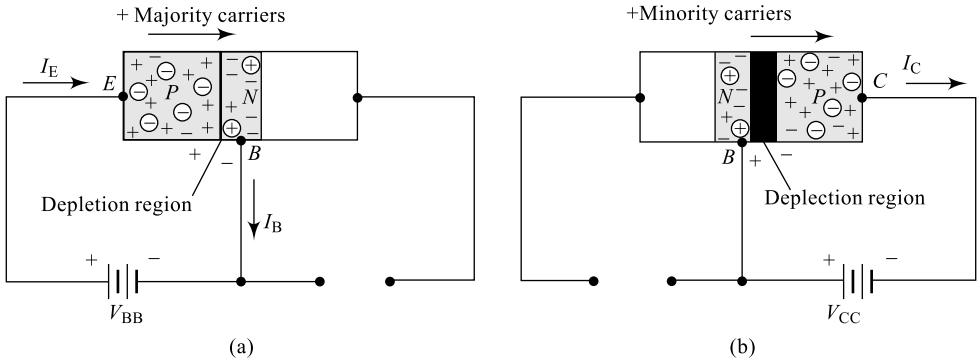


Fig. 3.2 (a) *PNP* transistor with forward-biased J_1 (b) *PNP* transistor with reverse-biased J_2

When biasing potentials to both the junctions are applied to a *PNP* transistor, the resulting current contains both majority and minority charge carrier flow; a large number of majority carriers will diffuse across the forward-biased *PN* junction into the *N*-type material. Since the middle *N*-type material is very thin and has a high resistivity, a very small number of these carriers will take this path of high resistance to the base terminal constituting a very small base current I_B. The magnitude of this base current is typically of the order of microamperes. A large number of these majority carriers will diffuse across the reverse-biased junction into the *P*-type material connected to the collector terminal constituting a collector current I_C, the magnitude of which will be in the order of milliamperes. Applying Kirchhoff's current law to the base of the transistor, we obtain

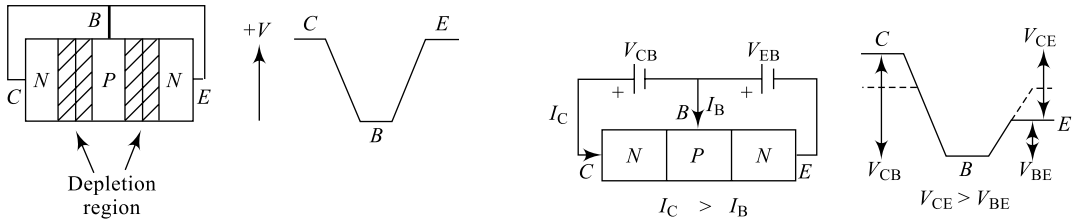
$$\boldsymbol{I_E = I_C + I_B} \tag{3.1}$$

Here, we find that the emitter current is the sum of the collector and base currents and the collector current consists of both the majority and the minority carriers. The minority current component is called the **leakage current**, represented by the symbol I_{CO} (collector current with emitter terminal open). The total collector current is, therefore, given by

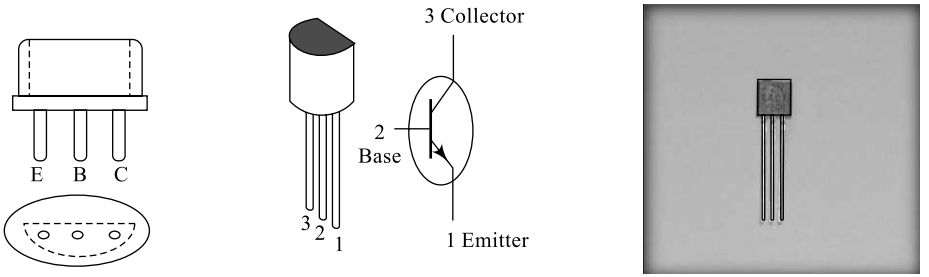
$$I'_C = I_{C\ \text{majority}} + I_{CO\ \text{minority}}$$
$$I'_C = I_C + I_{CO} \tag{3.2}$$

Generally, I_C will in the order of milliamperes and I_{CO} will in the order of microamperes or nanoamperes. I_{CO} (and hence I_C) is highly temperature sensitive and must be controlled carefully when wide temperature applications are involved, otherwise it can severely affect the stability of a system at high temperatures. If the collector, emitter and base of an *NPN* transistor are shorted together as shown in Fig. 3.3(a), the diffusion process described earlier for diodes results in the formation of two depletion regions that surround the base as shown. The diffusion of negative carriers into the base and positive carriers out of the base results in a relative electric potential as shown in Fig. 3.2(b). The voltage levels developed under different conditions are also indicated.

When the transistor is biased for normal operation as in Fig. 3.3(b), the base terminal is slightly positive with respect to the emitter (about 0.6 V for silicon), and the collector is positive by several volts. When properly biased, the transistor acts to make $I_C >> I_B$. The depletion region at the reverse-biased base-collector junction grows and is able to support the increased electric potential change indicated in Fig. 3.3(b). For a typical transistor, 95% to 99% of the charge carriers from the emitter make it to the collector and constitute almost all the collector current I_C; I_C is less than I_E by I_B. A small current flow into the base controls a much larger current flow into the collector and thus a **BJT is a current-**



(a) *NPN* transistor with *C*, *B* and *E* shorted (b) *NPN* transistor biased for operation



(c) BC-107 (d) 2N4123 (e) Low power transistor

Fig. 3.3 Different forms of commercially available transistors

controlled device. After the transistor has been manufactured, gold or an aluminum or nickel leads are then attached and the entire structure is encapsulated in a casing with a notch to identify the emitter, collector and base terminals of a transistor. Figs 3.3(c), (d) and (e) show commercially available transistors.

3.3 TRANSISTOR CONFIGURATIONS

A transistor can be considered and analysed as a two-port network with an input port and an output port. In order to configure a transistor as a two-port network, one of the terminals need to be common between input and output. Accordingly, there are three different configurations possible for a transistor connection in any application; they are

(i) Common-Base (CB) configuration
(ii) Common-Emitter (CE) configuration
(iii) Common-Collector (CC) configuration

3.3.1 Common-Base Configuration

In the common base (CB) configuration, the base terminal is common to both the input and output ports. The arrangement shown in Fig. 3.4 is a common-base configuration, its input and output *VI* characteristics. The battery V_{EE} used on the input side maintains a forward bias on the *BE* junction and resistor R_E is to limit the emitter current. Similarly, the battery V_{CC} used on the output side maintains a reverse bias on the CB junction and the resistor R_C is to limit the collector current.

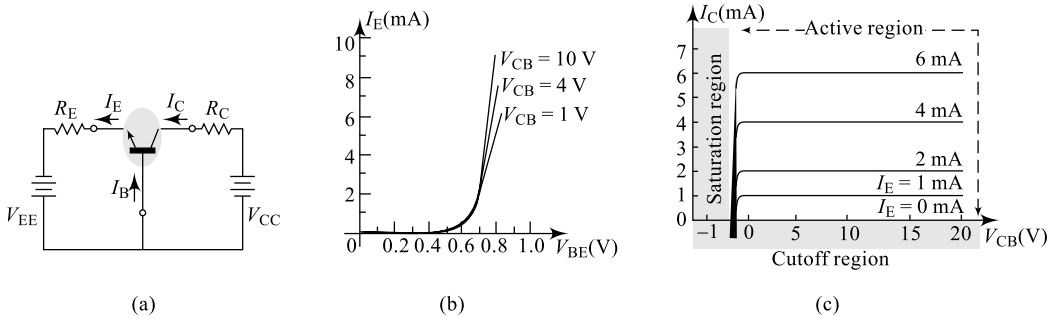


Fig. 3.4 (a) Transistor in CB configuration (b) Input characteristics (c) Output characteristics

Conventional current flow will be opposite to electron flow throughout this textbook, meaning all current directions will refer to conventional hole flow rather than electron flow and the arrows in all electronic symbols have a direction defined by this convention. All the current directions appearing in Fig. 3.4(a) are the actual directions as defined by the choice of conventional flow. Note that the applied biasing voltages are in such a way as to establish current in the direction indicated for each branch. In order to clearly understand the working of the common-base configuration, two sets of characteristics are used; the input characteristics for the driving point or input parameters and the output characteristics for the output side or the load side. The input characteristics for the common-base amplifier are shown in Fig. 3.4(b); this relates the input current I_E to the input voltage V_{BE} for various levels of output voltage V_{CB}. The output characteristics shown in Fig. 3.4(c) relates the output current I_C to the output voltage V_{CB} for various values of V_{BE}. The output or collector characteristics has three basic regions of interest; the active region, the cut-off region and the saturation region. The region close to *X*-axis with $I_E \cong 0$ is cut-off region, the region close to *Y*-axis with $V_{CE} \cong 0$ is saturation region and the in-between region (shown by dashed line) is the active region. The active region is normally employed for applications like amplifiers, oscillators, etc. The saturation and cut-off regions are employed for switching applications. In the active region, the base–emitter junction is forward biased, whereas the collector–base junction is reverse biased. The regions of operation are selected by fixing the operating point (zero signal values of I_C and V_{CE}) using the biasing arrangements. At the lower end of the active region, the emitter current (I_E) is zero and the collector current is simply that due to the reverse saturation current I_{CO} represented as I_{CBO} is indicated in Fig. 3.4(c). In addition, I_{CBO} (reverse leakage current) is temperature sensitive. At higher temperatures the effect of I_{CBO} may become an important factor since it increases so rapidly with temperature. Notice in the output characteristics that as the emitter current increases above zero, the collector current also increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor current relations. In the active region, the effect of V_{CB} on the collector current is almost negligible. The curves clearly indicate that a first approximation to the relationship between I_E and I_C in the active region is given by the relation

$$\boldsymbol{I_E \cong I_C} \tag{3.3}$$

In the cut-off region, the collector current is zero and the base–emitter junction and collector–base junction both are reverse-biased. The saturation region is the region to the left of the *Y*-axis, i.e. $V_{CB} = 0$ V. In the saturation region, the base–emitter junction and collector–base junction both are forward biased. The input characteristics of Fig. 3.4(c) clearly indicate that for a given value of collector-base voltage V_{CB}, the emitter current I_E increases with the base-emitter voltage (resembles the diode characteristics) and once a transistor is in the ON state, the base-emitter voltage will be $V_{BE} = 0.7$ V.

Example 3.1

An *NPN* transistor has a dc current gain of $\alpha = 0.989$. Calculate the input current I_E required to switch a resistive load of 4 mA in the collector circuit.

Solution We have, in CB configuration from Eq. (3.4),

$$\alpha_{dc} = \left.\frac{I_C}{I_E}\right|_{V_{CB}}$$

$$I_E = \frac{I_C}{\alpha_{dc}} = \frac{4\text{ mA}}{0.989} = 0.045\text{ mA}$$

An emitter current of 4.045 mA results in a collector current of 4 mA and drives the load.

Common-Base Current Gain—α

The current gain alpha (α) is defined for the common-base configuration of a BJT and can be defined in two forms: the dc current amplification factor (α_{dc}) and the ac current amplification factor (α_{ac}). The dc current gain α_{dc} is defined as the ratio of collector current to emitter current at a constant V_{CB} under dc biasing conditions.

$$\alpha_{dc} = \left.\frac{I_C}{I_E}\right|_{V_{CB}} \tag{3.4}$$

Similarly, the ac current gain α_{ac} is defined as the ratio of change in collector current to a corresponding change in emitter current at a given V_{CB} under ac signal conditions.

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}} \tag{3.5}$$

Equation 3.5 indicates that a relatively small change in collector current I_C is divided by the corresponding change in emitter current I_E with a constant collector-to-base voltage V_{CB}. For most situations, the magnitudes of both I_E and I_C are so close that one can be approximated to the other, resulting in a maximum value for the $\alpha_{max} = 1$; hence

$$\alpha \leq 1 \tag{3.6}$$

Consider Eq. (3.2), $I_C' = I_C + I_{CO}$

But from Eq. (3.4), $I_C = \alpha_{dc} \times I_E$ and from Eq. (3.1), $\boldsymbol{I_E = I_C + I_B}$. Hence, we can write

$$\begin{aligned} I_C' &= \alpha_{dc} \times I_E + I_{CO} \\ &= \alpha_{dc}(I_C + I_B) + I_{CO} \end{aligned}$$

$$I_C' = \frac{\alpha_{dc} \times I_B}{1 - \alpha_{dc}} + \frac{I_{co}}{1 - \alpha_{dc}} \tag{3.7}$$

A common-base configuration offers the following characteristics: the transistor circuit will have a very low-input impedance, very high output impedance, unity (or less) current gain, high-voltage gain and very good high-frequency response and hence finds dominant applications in RF amplifiers and high-frequency circuits.

Example 3.2

An *NPN* transistor has a dc base bias voltage, $V_B = 10$ V and an input base resistor, $R_B = 100$ kΩ. What will be the value of the base current into the transistor?

Solution We have, at base circuit of the transistor

$$I_B = \frac{V_B - V_{BE}}{R_B}$$

$$I_B = \frac{10 - 0.07}{100\,k} = 93\,\mu A$$

3.3.2 Common-Emitter Configuration

In the common-emitter (CE) configuration, the emitter terminal is common to both the input and output ports. The arrangement shown in Fig. 3.5 is a common-emitter configuration, its input and output *VI* characteristics. The battery V_{BB} used on the input side maintains a forward bias on BE junction and resistor R_B is to limit the base current (drive). Similarly, the battery V_{CC} used on the output side maintains a reverse bias on the CB junction and resistor R_C is to limit the collector current.

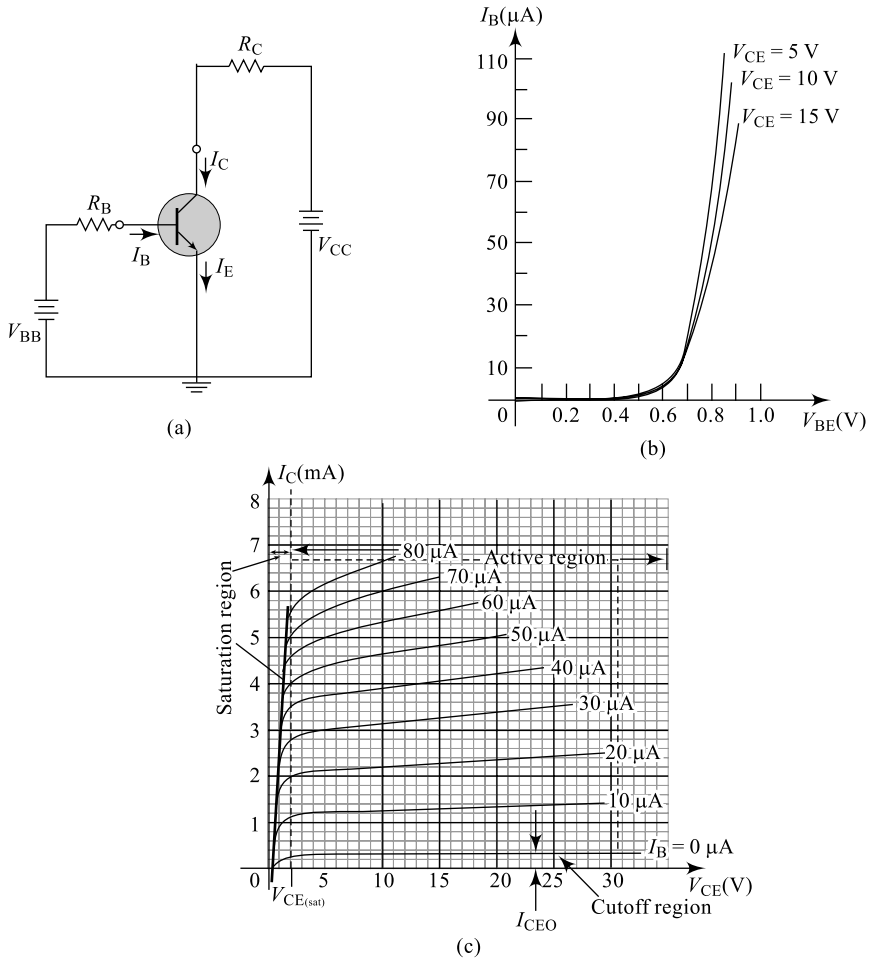


Fig. 3.5 (a) Transistor in CE configuration (b) Input characteristics (c) Output characteristics

Common-emitter configuration is the most commonly used transistor configuration since it offers a relatively better performance among all the three configurations. In order to clearly understand the working of the common-emitter configuration, two sets of characteristics is used; the input characteristics for the driving point or input parameters and the output characteristics for the output side or the load side. The input characteristics for the common-emitter amplifier is shown in Fig. 3.5(b); this relates the input current I_B to the input voltage V_{BE} for various levels of output voltage V_{CE}. The output characteristics shown in Fig. 3.5(c) relates the output current I_C to the output voltage V_{CE} for various values of I_B. The output or collector characteristic has three basic regions of interest; the active region, the cut-off region and the saturation region as marked in Fig. 3.5(c). The emitter, collector and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. Notice that the curves of I_B are not as flat as those obtained for I_E in the common-base configuration; this indicates that the influence of voltage V_{CE} on the collector current is more compared to the voltage V_{CB}. The region to the left of V_{CEsat} is called the **saturation region**. In the active region of a common-emitter amplifier, the base–emitter junction is forward biased and the collector–base junction is reverse biased. The active region of the common-emitter configuration can be employed for voltage, current or power amplification. The cut-off region for the common-emitter configuration is not as well defined as for the common-base configuration. When employed as a switch in the logic circuits, the transistor will have to be operated between the cut-off and the saturation regions.

Example 3.3

A *PNP* transistor has a dc current gain of $\beta = 200$; a relay of 4 mA connected in the collector circuit has to be driven by this device as shown in Fig. 3.6. Calculate the base current I_B required to switch the relay in the collector circuit.

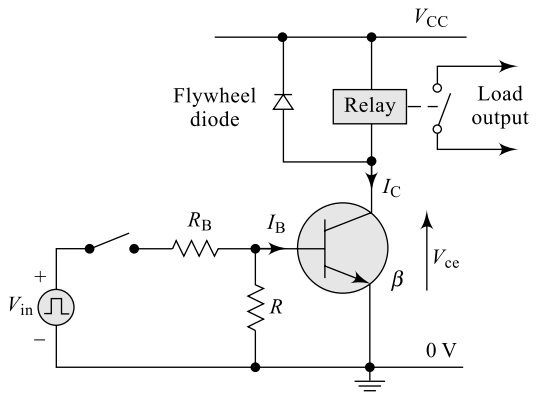


Fig. 3.6 For Example 3.3

Solution We have, in CE configuration from Eq. (3.8),

$$\beta_{dc} = \left.\frac{I_C}{I_B}\right|_{V_{CE}}$$

$$I_B = \frac{I_C}{\beta_{dc}} = \frac{4\text{ mA}}{200} = 20\ \mu\text{A}$$

A base current of 20 μA results in a collector current of 4 mA and drives the load.

1. Common Emitter Current Gain—β

The current gain, beta (β), is defined for the common-emitter configuration of a BJT and can be defined in two forms: the dc current amplification factor (β_{dc}) and the ac current amplification factor (β_{ac}). The dc current gain β_{dc} is defined as the ratio of collector current to base current at a constant V_{CE} under dc biasing conditions.

$$\beta_{dc} = \left.\frac{I_C}{I_B}\right|_{V_{CE}} \tag{3.8}$$

Here, I_C and I_B are determined at a particular operating point on the *VI* characteristics. For practical devices, the value of β typically ranges from about 50 to over 400. The parameter β reveals the relative magnitude of one current with respect to the other; for a device with a β of 100, the collector current is 100 times the magnitude of the base current. On specification sheets, this parameter is represented as h_{fe}, the hybrid parameter obtained using a hybrid equivalent circuit (to be introduced in Chapter 4). Similarly, the ac current gain β_{ac} is defined as the ratio of change in collector current to a corresponding change in base current at a given V_{CE} under ac signal conditions.

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}} \tag{3.9}$$

Since the collector current is the output current for a common-emitter configuration and the base current is the input current, the term *amplification* is included in the nomenclature above. On specification sheets, it is normally referred to as h_{fe}.

A common-emitter configuration offers the following characteristics: the transistor circuit will have a moderately high input impedance, low output impedance, moderately high current gain, moderately high voltage gain and very good and wide range of frequency response and hence finds dominant applications in voltage, current and power amplifiers.

Example 3.4

An *NPN* transistor has a set of input characteristics shown in Fig. 3.7. Calculate (a) base current at V_{BE} = 0.75 V and V_{CE} = 1.0 V, and (b) input dc resistance of the device at V_{BE} = 0.75 V and V_{CE} = 1.0 V.

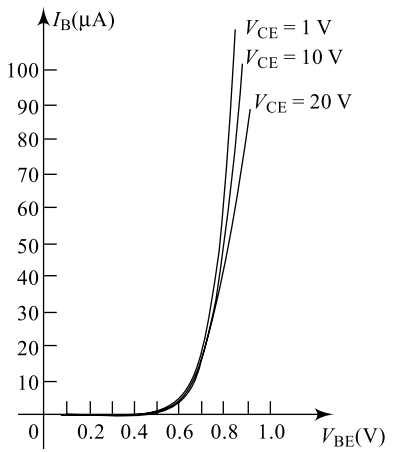


Fig. 3.7 For Example 3.4

Solution

(a) We have, from the graph at V_{BE} = 0.75 V, a line erected vertically touches V_{CE} = 1 V line at a point which intersects the *y*-axis at I_B = **40 μA**.

(b) The corresponding input resistance can be calculated using the relation

$$R_{in} = \frac{V_{BE}}{I_B} = 0.\frac{75}{40\ \mu A} = 18.75\ k\Omega$$

2. Relationship between α and β

A relationship can be developed between α and β using the basic relationships introduced so far. Using Eq. (3.4) and Eq. (3.7), we can rewrite Eq. (3.1) as below:

$$I_E = I_C + I_B$$

$$\frac{I_C}{\alpha_{dc}} = I_C + \frac{I_C}{\beta_{dc}}$$

$$\frac{I_C}{\alpha_{dc}} = I_C \left(1 + \frac{1}{\beta_{dc}}\right)$$

$$\frac{1}{\alpha_{dc}} = \frac{(1+\beta_{dc})}{\beta_{dc}}$$

Re-arranging,

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} \tag{3.10}$$

or,

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} \tag{3.11}$$

Example 3.5

An *NPN* transistor has a set of output characteristics shown in Fig. 3.8. Calculate (a) collector current at $I_B = 40\ \mu A$ and $V_{CE} = 7.5$ V, and (b) the corresponding output dc resistance of the device.

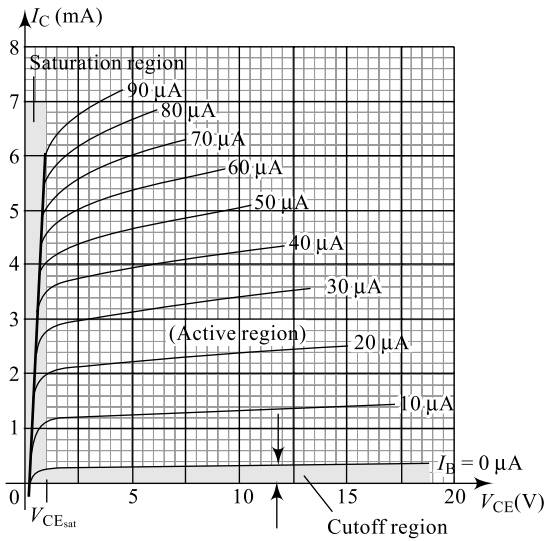


Fig. 3.8 For Example 3.5

Solution

(a) We have, from the graph with $V_{CE} = 7.5$ V, a line erected vertically touches the $I_B = 40\ \mu A$ line at a point which intersects *y*-axis at $I_C = \mathbf{4.10}$ mA.

(b) The corresponding output resistance can be calculated using the relation

$$R_O = \frac{V_{CE}}{I_C} = 7.\frac{5}{40\ \mu A} = 1.705\ k\Omega$$

3.3.3 Common-Collector Configuration

In the common-emitter (CC) configuration, the emitter terminal is common to both the input and output ports. The arrangement shown in Fig. 3.9 is a common-collector configuration. The battery V_{BB} used on the input side maintains a forward bias on the BE junction and the resistor R_B is to limit the base current (drive). Similarly, the battery V_{CC} used on the output side maintains a reverse bias on the CB junction and the resistor R_E is used to collect the output. Notice that in a CC configuration, there is no collector resistor and the output is measured across emitter resistor.

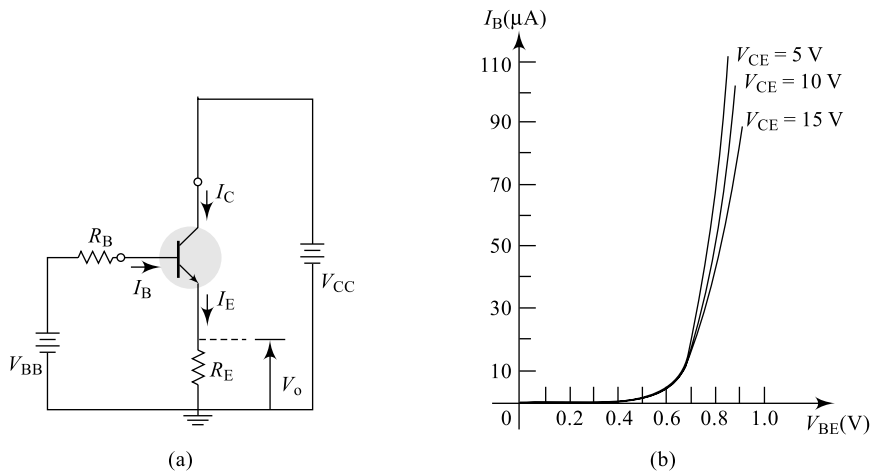


Fig. 3.9 (a) Transistor in CC configuration (b) Input characteristics

In order to clearly understand the working of the common-collector configuration, two sets of characteristics are used: the input characteristics for the driving point or input parameters and the output characteristics for the output side or the load side. The input characteristics for the common-collector amplifier is shown in Fig. 3.9(b); this relates the input current I_B to the input voltage V_{BE} for various levels of output voltage V_{CE}. The output characteristics for a CC circuit relates the output current I_E (I_C in CE mode) to the output voltage V_{CE} for various values of I_B. Since I_C is almost equal to I_E, the output characteristics for a CC mode are almost similar to that of a CE mode. The CC configuration is also commonly known as the **emitter follower** or the **voltage follower**. This is because the output signal across the emitter is almost the replica of the input signal with little loss. In other words, the output voltage follows the input voltage and hence the voltage gain will be a maximum of one.

1. Common Collector Current Gain—γ

The current gain beta (γ) is defined for the common-emitter configuration of a BJT and can be defined in two forms: the dc current amplification factor (γ_{dc}) and the ac current amplification factor (γ_{ac}). The dc current gain β_{dc} is defined as the ratio of emitter current to base current at a constant V_{CE} under dc biasing conditions.

$$\gamma_{dc} = \left.\frac{I_E}{I_B}\right|_{V_{CE}} \tag{3.12}$$

For practical devices, the value of γ typically ranges from about 50 to over 400 (one greater than β). Similarly, the ac current gain γ_{ac} is defined as the ratio of change in emitter current to a corresponding change in base current at a given V_{CE} under ac signal conditions.

$$\gamma_{ac} = \left.\frac{\Delta I_E}{\Delta I_B}\right|_{V_{CE}} \tag{3.13}$$

A common-collector configuration offers the following characteristics: the transistor circuit will have a very high input impedance, very low output impedance, moderately high current gain, unity voltage gain and very good and wide range of frequency response and hence finds dominant applications in current amplifiers. Because of good impedance-matching properties, this circuit is widely used as driver (buffer) stage in many applications.

2. Phase Shifts

In both the common-base and the common-collector (emitter follower) configurations, the input and output signals are in phase, but in the common-emitter configuration, the input and output signals are phase shifted by 180° (inverted); a positive input resulting in a negative output and vice versa. Table 3.2 illustrates a comparison between all the three transistor configurations:

Table 3.2 Comparison between CE, CB and CC transistor configurations

Sl. No.	Parameter	CE mode	CB mode	CC mode
1	Between input and output, the common terminal	Emitter	Base	Collector
2	Voltage gain	Moderate	High (50 to 300)	Unity (≤ 1)
3	Current gain	Moderate	Unity (≤ 1)	High
4	Power gain	Possible	No	No
5	Input impedance	Moderate	Low	High
6	Output impedance	Low	High	Low
7	Phase shift	180°	No	No
8	Applications	Almost all applications like amplifiers, oscillators, etc.	High-frequency applications.	Impedance matching, driver stages, etc.

3.4 TRANSISTOR AS AN AMPLIFIER

Amplification is the process of increasing the strength of a weak signal and the circuit which performs this is called as an amplifier. Amplification can be for either a voltage signal or a current signal; a circuit which offers amplification to the voltage signal is a voltage amplifier and that for a current signal is a current amplifier. However, a power amplifier amplifies both current and voltage levels of the input signal. For simplicity, the common-emitter configuration is considered. The basic amplifying action was produced by transferring the source current I_i from a low-resistance to a high-resistance circuit; and that is how the term *transistor* refers to transfer of resistance (from low to high). An amplifier performance is determined mainly by the selection of Q-point (zero signal values of I_C and V_{CE}), input impedance and output impedance. The ac input resistance determined by the input characteristics of Fig. 3.5(b), is quite moderate and typically few kΩ. The output resistance, as determined by the curves of Fig. 3.5(c), is quite small and typically a few 100 Ω. Figure 3.10 indicates the block representation of an amplifier and a detailed discussion on transistor amplifiers is presented further in Chapter 4. For each transistor,

there is a region of operation on its characteristics which will ensure that the device maximum ratings are not exceeded and the output signal is zero or minimum distorted. All such regions of (the limits of) operation are defined on typical transistor specification sheets. Some of the limits of operation are maximum collector current or continuous collector current I_{Cmax}, maximum collector-to-emitter voltage V_{CEO} or $V(BR)_{CEO}$. The level of V_{CEsat} is typically in the neighbourhood of 0.1 V for germanium transistor and 0.2 V to 0.3 V for silicon transistors. The maximum dissipation level is given by

$$P_{max} = I_{Cmax}\, V_{CEmax} \tag{3.14}$$

Amplifier Gain

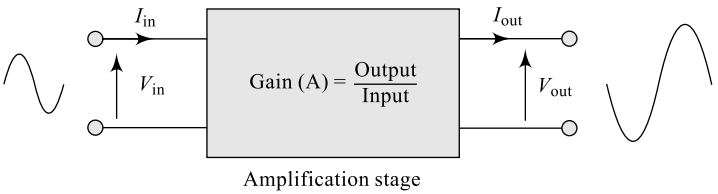


Fig. 3.10 Amplifier gain

Amplifier Voltage Gain

$$\text{Voltage gain } A_V = \frac{\text{Output Voltage}}{\text{Input Voltage}} = \frac{V_{OUT}}{V_{in}}$$

Amplifier Current Gain

$$\text{Current gain } A_i = \frac{\text{Output Current}}{\text{Input Current}} = \frac{I_{OUT}}{I_{in}}$$

Amplifier Power Gain

$$\text{Power gain } A_p = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{OUT}}{P_{in}}$$

Note that the power gain can also be expressed as the product of voltage gain and current gains,

i.e. power gain $A_p = A_v \times A_i$

The amplifier gains can be expressed in **decibels** (**dB**). Bel is a logarithmic unit (base 10) of measurement that has no units but as bel is a large unit of measure, it has be prefixed with *deci* making it **decibels** with one decibel being one tenth (1/10th) of a Bel. To calculate the gain of the amplifier in decibels or dB, we can use the following expressions:

$$\text{Voltage gain in dB: } A'_v = 20 \log A_v$$
$$\text{Current gain in dB: } A'_i = 20 \log A_i$$
$$\text{Power gain in dB: } A'_p = 10 \log A_p$$

Example 3.6

Determine the voltage gain, current gain and power gain of an amplifier that has an input signal of 1 mA at 10 mV and a corresponding output signal of 10 mA at 1 V. Also, express all three gains in decibels (dB).

Solution

$$\text{Voltage gain } A_V = \frac{\text{Output Voltage}}{\text{Input Voltage}} = \frac{1}{0.01} = 100$$

$$\text{Current gain } A_i = \frac{\text{Output Current}}{\text{Input Current}} = \frac{10}{1} = 10$$

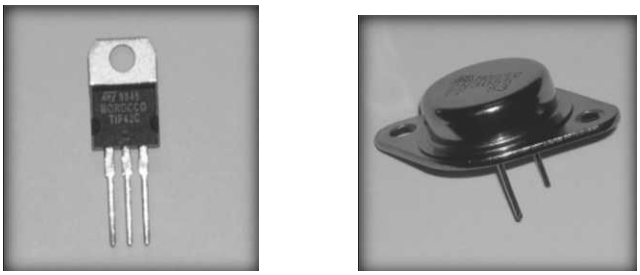
$$\text{Power gain } A_p = A_v \times A_i = 100 \times 10 = 1000$$

Amplifier gain in decibels (dB):

$$\text{Voltage gain in dB: } A_v' = 20 \log A_v = 20 \log 100 = 40 \text{ dB}$$

$$\text{Current gain in dB: } A_i' = 20 \log A_i = 20 \log 10 = 20 \text{ dB}$$

$$\text{Power gain in dB: } A_p' = 10 \log A_p = 10 \log 1000 = 30 \text{ dB}$$



(a) Medium-power transistor (b) High-power transistor

Fig. 3.11 Different forms of commercially available transistors

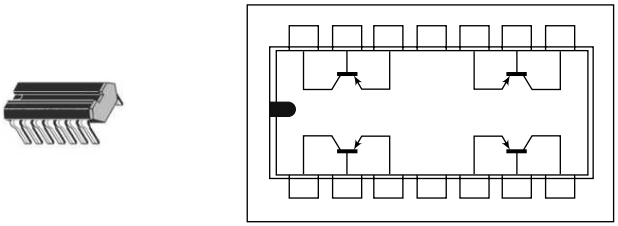


Fig. 3.12 A quad *PNP* Si transistor-Q2T2905: (a) IC form (b) Internal structure

Figure 3.11 and 3.12 present some commercially available power transistors. For high power transistor, the casing will be large for higher dissipation.

3.5 TRANSISTOR SPECIFICATION SHEET

Transistor Standards: Digit - Letter - Serial number - [suffix]

The transistor's first digit is one less than the number of connections the device has, except for 4N and 5N which are reserved for opto-couplers. The number 2 is most common. The letter is always N. The serial number runs from 100 to 9999 indicating its development date.

The suffix(optional) indicates the gain (h_{fe}) group of the device:

A = low gain

B = medium gain

C = high gain

No suffix = ungrouped (any gain)

Examples: 2N4401, 2N2222A, 2N104

2SAXXXX	*PNP*	type	high	frequency
2SBXXXX	*PNP*	type	low	frequency
2SCXXXX	*NPN*	type	high	frequency
2SDXXXX	*NPN*	type	low	frequency

The digit is one less than the number of connections, i.e. 2 for most. The letters indicate the application area according to the following code:

SA:	*PNP*	HF	Transistor
SB:	*PNP*	AF	Transistor
SC:	*NPN*	HF	Transistor
SD:	*NPN*	AF	Transistor
SE:			Diodes
SF:			Thyristors
SG:	Gunn		Devices
SH:			UJT
SJ:	*P*-channel		FET/MOSFET
SK:	*N*-channel		FET/MOSFET
SM:			Triac
SQ:			LED
SR:			Rectifier
SS:	Signal		Diodes
ST:	Avalanche		Diodes
SV:			Varicaps
SZ:			Zener diodes

The serial number runs from 10 to 9999.

Examples: 2SA2222, 2SB719, 2SC583, 2SC435, C 435.

Pro-electron.

(Ref: The Pro-Electron website.)

Two letters, [letter], Serial number, [suffix]

The first letter indicates the material:

A = Ge

B = Si

C = GaAs

R = Compound materials.

(Most common type is B.)

The second letter indicates the device application:

A: Diode RF

B: Variac
C: Transistor, AF, small signal
D: Transistor, AF, power
E: Tunnel diode
F: Transistor, HF, small signal
K: Hall effect device
L: Transistor, HF, power
N: Optocoupler
P: Radiation-sensitive device
Q: Radiation-producing device
R: Thyristor, low power
T: Thyristor, Power
U: Transistor, power, switching
Y: Rectifier
Z: Zener, or voltage regulator diode

The third letter, if used, is usually a W, X, Y or Z and indicates noncommercial use. The serial number runs from 100 to 9999. The suffix indicates the gain grouping, as for JEDEC.

Examples: BC204A, BAW45, BF299, BFY62

3.6 TRANSISTOR TESTING

As already discussed in Chapter 2 for diode testing, the transistor testing can also be done considering a transistor as a combination of two diodes. Mainly, there are three methods that can be used to test a transistor; they are use of an ohmmeter and a curve tracer.

1. Ohmmeter Testing

An ohmmeter is nothing but the resistance scales of a Digital MultiMeter (DMM); it can be used to check the state of a transistor. Recall that for a transistor in the active region, the base-to-emitter junction is forward biased and the base-to-collector junction is reverse biased. Essentially, therefore, the forward-biased junction should register a relatively low resistance, whereas the reverse-biased junction shows a much higher resistance. For an *NPN* transistor, the forward-biased junction (biased by the internal supply in the resistance mode) from base to emitter should be checked as shown in Fig. 3.13(a) and results in a reading that will typically fall in the range of 100 to a few kilo-ohms. The reverse-biased

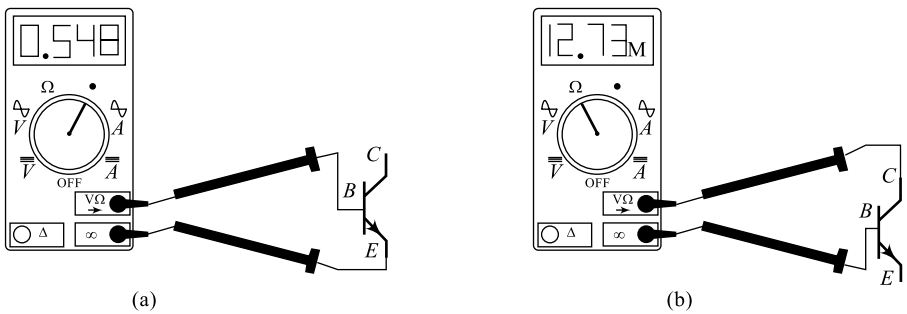


Fig. 3.13 (a) Forward-biased BE junction (b) Reverse-biased CB junction

base-to-collector junction (again reverse biased by the internal supply) should be checked as shown in Fig. 3.13(b) with a reading typically exceeding 100 kΩ. For a *PNP* transistor, the leads are reversed for each junction. Obviously, a faulty device indicates a large or small resistance in both directions (reversing the leads) for either junction of an *NPN* or *PNP* transistor.

If both junctions of a transistor result in the expected readings, the type of transistor can also be determined by simply noting the polarity of the leads as applied to the base-emitter junction. If the positive (+) lead is connected to the base and the negative lead (–) to the emitter, a low resistance reading would indicate an *NPN* transistor. A high resistance reading would indicate a *PNP* transistor. Although an ohmmeter can also be used to determine the leads (base, collector and emitter) of a transistor, it is assumed that this determination can be made by simply looking at the orientation of the leads on the casing.

2. Transistor Curve Tracer

The transistor curve tracer provides the direct display of input-output characteristics if all the necessary controls are properly set. Most of today's modern oscilloscopes (to be discussed in Chapter 8) come with these curve tracers and even some of these measuring devices provide an estimation of the current gain (β).

Apart from these, there are a variety of transistor testers available, some are simply in the form of digital meters and most of today's digital meters come with these testers.

Table 3.3 illustrates the applications of various regions of transistor operation. It can be observed here that active region of operation finds varieties of applications since the collector current and base current have a linear relationship in this region.

Table 3.3 Transistor operating regions and their applications

Sl. No.	Region	Applications
1	Cut-off region	No application, transistor will not be conducting.
2	Active region	Many applications; amplifiers, oscillators, etc.
3	Saturation region	Constant current sources
4	Cut-off and saturation region	Switching applications, invertor, etc.

3.7 INTRODUCTION TO BJT BIASING

The analysis or design of a transistor amplifier requires knowledge of both the dc and the ac response of the system. A transistor is a device that can amplify the level of the applied ac input using a set of resistors and an external dc energy source which fixes up the required dc conditions in the circuit. This zero signal values (no input ac signal) of collector current and the collector-emitter voltage are called ***Q*-point** or **operating point**. In reality, the increase in the output ac power level is the result of a transfer of energy from the applied dc supplies. The analysis and design of any electronic amplifier, therefore, has two parts: the dc part and the ac part. The dc analysis and the ac analysis can be separately carried out, but the design stages are dependent on each other. The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. Once the desired dc current and voltage levels are defined, a circuit must be constructed that will establish the desired operating point. The remaining sections of this chapter discuss a number of these circuits. Each design will also determine the stability of the system, that is, how sensitive the system

is to device parameters which, in turn, are sensitive to temperature variations. In most cases, the base current is the first important quantity to be determined; once I_B is known, the relationships between various device parameters [Eq. (3.1) to Eq. (3.12)] can be used to find the remaining parameters of the device. The similarities in analysis will be immediately obvious as we progress through the sections of the chapter. The primary goal of this chapter is to develop a level of familiarity with the BJT transistor that would help a dc analysis of any system employing the BJT device.

3.8 LOAD-LINE ANALYSIS AND OPERATING POINT

Biasing is a method to establish a fixed level of current and voltage in the device through the application of dc voltages. For these transistor circuits, the resulting dc current and voltage establish an operating point on the characteristics that define the region employing applications like amplification, switching, etc. Because the operating point is a fixed point on the characteristics, it is also called the quiescent point or *Q*-point. Figure 3.14(c) shows the fixing of an operating point on the output characteristics of a device. The external biasing circuit can be so designed to fix the device operation at any of the desired points like Q_1 or Q_2 or any other within the device active region. The chosen *Q*-point often depends on the intended application of the circuit, for example if no bias were used, the device would initially be completely off, resulting in Q_1 ($I_C = 0$ and $V_{CE} = 0$). For most applications, since it is necessary to bias a device so that it can respond to the entire range of an input signal, the point Q_1 would not be suitable. For the point Q_2, if a signal is applied to the circuit, the device will vary its current and voltage around the operating point values depending upon the polarity and the magnitude of the input signal. In general, it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same; the point Q_2 is a region of more largest possible voltage and current swing, linear spacing and, therefore, more linear operation. Variations in the device temperature cause the device parameters, such as the transistor current gain and the transistor leakage current, to change and hence it is necessary to take care of the effect of temperature into account. Higher temperatures result in increased leakage currents in the device; practically, it is true that the leakage current doubles for every 10°C rise in temperature, thereby changing the operating condition set by the biasing network. The result is that the device may be damaged or the circuit may result in unfaithful working; hence, care should also be taken to see that the network design must also provide a degree of temperature stability so that temperature changes result in minimum changes in the

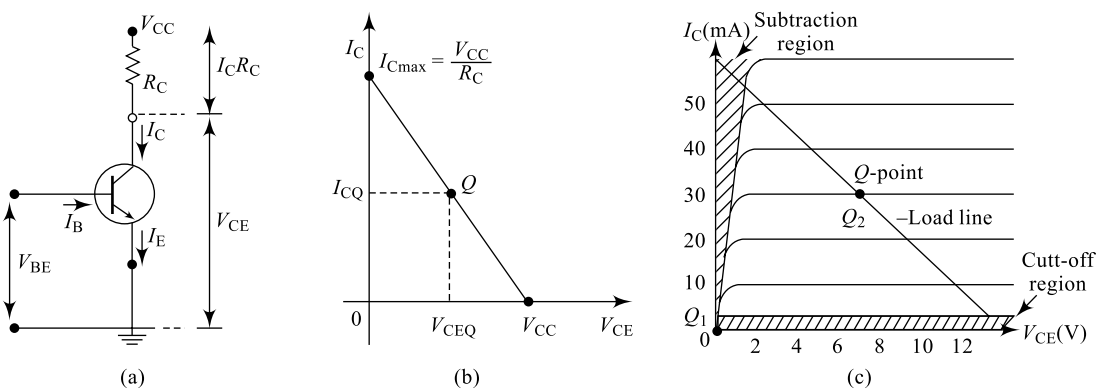


Fig. 3.14 (a) Simple CE circuit (b) The dc load line (c) Selection of a *Q*-point

operating point. This maintenance of the operating point can be specified by a stability factor S, which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable and the stability factor for such a circuit is theoretically zero. For the BJT to be biased in its linear or active operating region, the base–emitter junction must be forward biased (with a V_{BE} = 0.6 V to 0.7 V for an Si device and = 0.2 V to 0.3 V for a Ge device); the base–collector junction must be reverse biased.

Consider the CE circuit shown in Fig. 3.14(a); applying KVL to the output loop, we can write

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C \tag{3.15}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \tag{3.16}$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \tag{3.17}$$

Equation (3.15) represents a straight line $y = mx + c$ with $m = -1/R_C$, $x = V_{CE}$ and $c = V_{CC}/R_C$; the extreme points for the straight line are at $I_C = 0$ ($y = 0$), i.e. $V_{CE} = V_{CC}$ and $V_{CE} = 0$ ($x = 0$) or $I_C = V_{CC}/R_C$. Joining these two extreme points result in a straight line as indicated in Fig. 3.14(b) and co-ordinates of every point on this straight line represent an operating point. Sections 3.9 through 3.14 introduce different biasing circuits, their analysis and design; at the end, their performance analysis and comparison is also introduced. As already mentioned, the performance evaluation of these circuits can be done by obtaining the stability factor for the biasing circuit; stability factor indicates the variation of I_C with respect to device parameter changes. Transistor collector current I_C is sensitive to changes in the device parameters β, V_{BE} and I_{CO} which in turn are sensitive to temperature. Based on the parameter, three different stability factors can be defined:

(i) $S = \dfrac{\Delta I_C}{\Delta I_{CO}}$ /at β, V_{BE}

(ii) $s' = \dfrac{\Delta I_C}{\Delta V_{BE}}$ /at β, I_{CO}

(iii) $s = \dfrac{\Delta I_C}{\Delta \beta}$ /at V_{BE}, I_{CO}

Of the three, the equation (i) gains more importance since I_{CO} is more sensitive to temperature changes and hence needs an appropriate estimation.

Expression for S

An expression for S can be derived starting from the basic expression for collector current. The collector current in a transistor CE configuration is given by

$$I_C = \beta I_B + I_{CEO} \tag{3.18}$$

where I_{CEO} = collector to emitter leakage current

$$I_{CEO} = \frac{1}{(1 - \alpha)} I_{CO}; \; I_{CO} = \text{collector leakage current}$$

Differentiating Eq. (3.16) with respect to I_C, we get

$$1 = \beta \frac{\Delta I_B}{\Delta I_C} + (1 + \beta) \frac{\Delta I_{CO}}{\Delta I_C}$$

i.e. $$1 = \beta \frac{\Delta I_B}{\Delta I_C} + (1 + \beta) \frac{1}{S}$$

i.e. $$\frac{1}{S} = \frac{\left(1 - \beta \frac{\Delta I_B}{\Delta I_C}\right)}{(1 + \beta)}$$

i.e. $$S = \frac{(1 + \beta)}{\left(1 - \beta \frac{\Delta I_B}{\Delta I_C}\right)} \tag{3.19}$$

Equation 3.17 is the general expression for stability factor S which represents the variation of the collector current against collector leakage current and can be used to evaluate the performance of a biasing circuit. Smaller the value of S, more stable will be the Q-point and, hence, better will be the circuit performance.

3.9 TWO-BATTERY BIAS CONFIGURATION

As shown in Fig. 3.15, this method uses two separate batteries; V_{BB} to maintain forward bias on BE junction and V_{CC} to maintain reverse bias on CB junction. R_B limits the base drive to transistor, R_C limits collector current, and they help in establishing and maintaining Q-point. This method is obsolete because of two batteries; cost is more, stability of Q-point is determined by the quality of the two batteries and it consumes more space. For dc analysis, the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor for dc is ∞.

Applying KVL to input loop, we get

$$V_{BB} = I_B R_B + V_{BE}$$

$$I_B = (V_{BB} - V_{BE})/R_B \tag{3.20}$$

Similarly, Applying KVL to output loop, we get

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C \tag{3.21}$$

$$I_C = (V_{CC} - V_{CE})/R_C \tag{3.22}$$

Equations (3.18), (3.19) and (3.20) represent the Q-point for the circuit. In order to analyse the stability and performance of the circuit, let us find the stability factor of the circuit using Eq. (3.17). Differentiating Eq. (3.18) with respect to I_C, we get $\Delta I_B/\Delta I_C = 0$ and substituting this value in Eq. (3.17), we get stability factor

$$S = (1 + \beta) \tag{3.23}$$

Equation (3.21) clearly indicates S is large because β for transistor will be generally very high and, therefore, circuit stability is very poor.

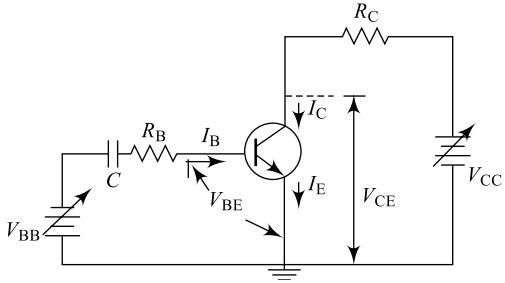


Fig. 3.15 Two-battery bias circuit

3.10 FIXED-BIAS CONFIGURATION

The fixed-bias circuit is shown in Fig. 3.16(a) and it is the simplest transistor dc bias configuration. Unlike in the previous case, here single battery provides the required forward bias for BE junction and reverse bias for BC junction. R_B is used to provide a fixed amount of base drive to the device and hence the name *fixed biasing*. In the network, an *NPN* transistor is used, but the equations and calculations apply equally well to a *PNP* transistor configuration merely by changing all current directions and voltage polarities. For dc analysis, the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor for dc is ∞.

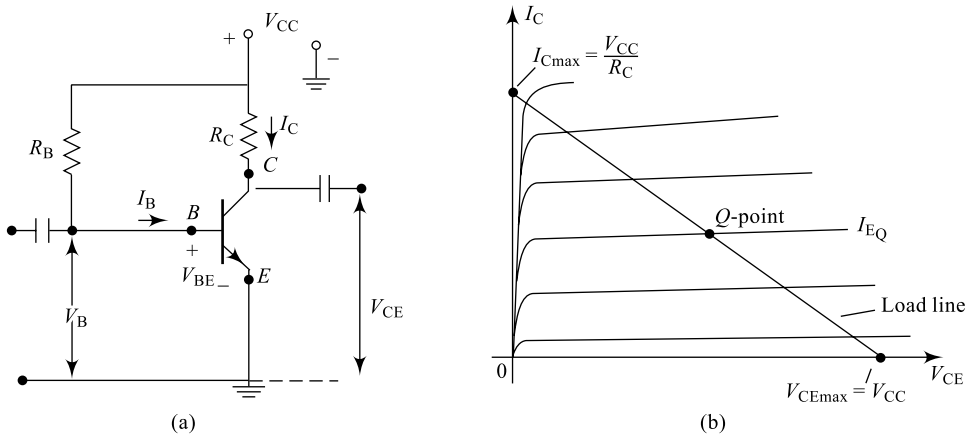


Fig. 3.16 (a) Fixed-bias circuit (b) Fixed-bias load line

Consider first the base-emitter circuit loop of Fig. 3.16; writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$V_{CC} = I_B R_B + V_{BE}$$
$$I_B = (V_{CC} - V_{BE})/R_B \tag{3.24}$$

Equation (3.22) is simply the base current and by Ohm's law, this current is the voltage across R_B divided by the resistance R_B. The selection of a base resistor R_B sets the level of base current for the operating point.

Similarly, applying KVL to the output loop, we can write

$$V_{CC} = I_C R_C + V_{CE}$$

$$I_C = (V_{CC} - V_{CE})/R_C \tag{3.25}$$

$$V_{CE} = V_{CC} - I_C R_C \tag{3.26}$$

Equations (3.22), (3.23) and (3.24) represent the Q-point for the circuit and these equations can be represented on the device output characteristics as indicated in Fig. 3.16(b). In order to analyse the stability and performance of the circuit, let us find the stability factor of the circuit using Eq. (3.17). Differentiating Eq. (3.22) with respect to I_C, we get $\frac{\Delta I_B}{\Delta I_C} = 0$ and substituting this value in Eq. (3.17), we get stability factor

$$S = (1 + \beta) \tag{3.27}$$

Equation (3.25) clearly indicates S is large because β for transistor will be generally very high and, therefore, circuit stability is very poor; however, the circuit is very simple to construct. It is important to note that I_B, the base current, is controlled by R_B. I_C is related to I_B by a constant β and I_C is not a function of R_C; hence, changing R_C will not affect I_B or I_C within the active region of the device, but it changes V_{CE}.

Example 3.7

A fixed-bias configuration for a BJT is shown in Fig. 3.17 determine the following parameters:

(a) the Q-point values: V_{CEQ}, I_{BQ} and I_{CQ}

(b) V_B and V_C

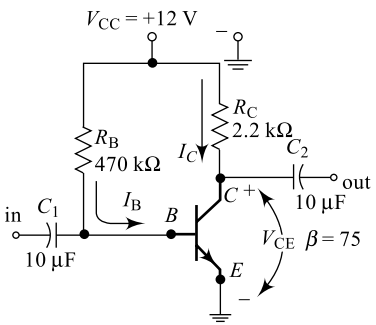


Fig. 3.17 For Example 3.7

Solution (a) We have from Eq. (3.24)

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{470\ k} = 24.04\ \mu A$$

From Eq. (3.8),

$$\beta = \frac{I_{CQ}}{I_{BQ}} = \frac{I_{CQ}}{24.04\ \mu A} = 75$$

$$I_{CQ} = 1.803\ mA$$

From Eq. (3.8),

$$V_{CEQ} = V_{CC} - I_C R_C$$

$$= 12 - 1.803\ mA \times 2.2k = 8.033\ V$$

(b) We have from the circuit,

$$V_C = V_{CEQ} = 8.033\ V$$

and $$V_B = V_{BE} = 0.7\ V$$

3.11 FEEDBACK-BIAS CONFIGURATION

In order to provide stability against variations in the output voltage, R_B can be connected as a feedback resistor. An improved level of stability can be obtained by introducing a feedback path from collector to base as shown in Fig. 3.18. Although the Q-point is not totally independent of beta, the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias configuration. It is important to note that the current through R_C is not simply the collector current, but it is the summation $I_C + I_B$. The analysis will again be performed by first analysing the base emitter or input loop; applying KVL to the input loop, we can write

$$\begin{aligned} V_{CE} &= V_C = I_B R_B + V_{BE} \\ I_B &= \frac{V_{CE} - V_{BE}}{R_B} \\ I_B &= \frac{[V_{CC}] - (I_C + I_B)[R_C] - V_{BE}}{R_B} \\ I_B &= \frac{V_{CC}}{R_B} - \frac{I_C R_C}{R_B} - \frac{I_B R_C}{R_B} - \frac{V_{BE}}{R_B} \end{aligned} \tag{3.28}$$

Re-arranging the terms, we get

$$I_B\left(1 + \frac{R_C}{R_B}\right) = \frac{V_{CC}}{R_B} - \frac{I_C R_C}{R_B} - \frac{V_{BE}}{R_B} \tag{3.29}$$

Equation (3.27) is simply the base current and by Ohm's law this current is the voltage across R_B divided by the resistance R_B, the selection of a base resistor R_B sets the level of base current for the operating point. Similarly, applying KVL to the output loop, we can write

$$\begin{aligned} V_{CC} &= IR_C + V_{CE} = (I_C + I_B)R_C + V_{CE} \\ V_{CE} &= V_{CC} - (I_C + I_B)R_C \\ (I_C + I_B)\mathrm{R}_C &= (V_{CC} - V_{CE}) \end{aligned} \tag{3.30}$$

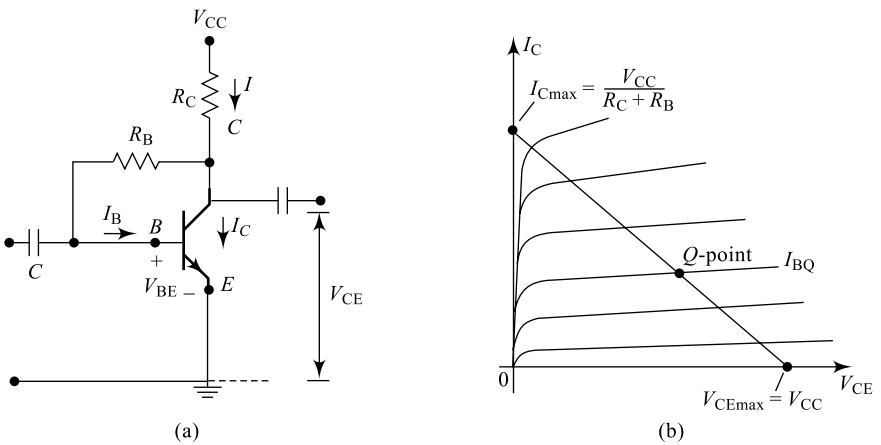


Fig. 3.18 (a) Feedback-bias circuit (a) Feedback-bias load line

Re-arranging, we get

$$I_C = \frac{V_{CC} - V_{CE} - I_B R_C}{R_B} \tag{3.31}$$

Equations (3.27), (3.28) and (3.29) represent the *Q*-point for the circuit and these equations can be represented on the device output characteristics as indicated in Fig. 3.18(b). In order to analyse the stability and performance of the circuit, let us find the stability factor of the circuit using Eq. (3.17). Differentiating Eq. (3.27) with respect to I_C, we get

$$\frac{\Delta I_B}{\Delta I_C}\left(1 + \frac{R_C}{R_B}\right) = 0 - 0 - \frac{R_C}{R_B}, \text{ i.e. } \frac{\Delta I_B}{\Delta I_C} = -\frac{R_C}{R_C + R_B}$$

Substituting this value in Eq. (3.17), we get the stability factor

$$S = \frac{(1+\beta)}{\left[1 - \beta\left(-\frac{R_C}{R_C + R_B}\right)\right]}$$

$$S = \frac{(1+\beta)}{\left[1 + \beta\left(\frac{R_C}{R_C + R_B}\right)\right]} \tag{3.32}$$

Equation (3.30) clearly indicates *S* is relatively large, but less as compared to the value obtained in fixed-biasing case. The *Q*-point stability is affected by load and output voltage variations; any change in the load has a direct impact on V_{CE}, and I_C and needs to be addressed which is done in the self-bias circuit.

Example 3.8

A feedback-bias (collector to base) configuration for a BJT is shown in Fig. 3.19; if the supply voltage is 10 V, β = 50, drop across R_C = 5 V, R_C = 2.45 kΩ, R_B = 110 kΩ and V_{BE} = 0.6 V, determine the operating point (*Q*-point).

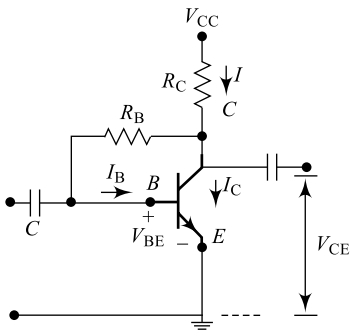


Fig. 3.19 For Example 3.8

Solution We have KVL to output loop resulting in

$$V_{CC} = V_{RC} + V_{CE}$$

i.e. $$V_{CEQ} = 10 - 5 = 5 \text{ V}$$

We have from Eq. (3.28),

$$I_{BQ} = \frac{V_{CE} - V_{BE}}{R_B} = \frac{5 - 0.6}{110\ k} = 40\ \mu\text{A}$$

From Eq. (3.8)

$$\beta = \frac{I_{CQ}}{I_{BQ}} = \frac{I_{CQ}}{40\ \mu\text{A}} = 50$$

$$I_{CQ} = 2.0 \text{ mA}$$

3.12 SELF-BIAS OR EMITTER-BIAS CONFIGURATION

A fixed-bias circuit fails to provide stability against load variations and this problem can be minimised by using an emitter resistor. The dc bias network of Fig. 3.20(a) contains an emitter resistor R_E to improve the stability level over that of the fixed-bias configuration. The analysis will be performed by first examining the base circuit; applying KVL to the loop containing V_{CC}, R_B and V_B, we get

$$V_{CC} = I_B R_B + V_B; \text{ where } V_B = (V_{BE} + V_E)$$

$$I_B = \frac{V_{CC} - (V_{BE} + V_E)}{R_B}$$

Substituting $V_E = I_E R_E$ and $I_E = (I_C + I_B)$ and re-arranging the terms, we get

$$I_B \left(1 + \frac{R_E}{R_B}\right) = \frac{V_{CC}}{R_B} - \frac{I_C R_C}{R_B} - \frac{V_{BE}}{R_B} \tag{3.33}$$

Equation (3.31) is simply the base current and by Ohm's law, this current is the voltage across R_B divided by the resistance R_B. The selection of a base resistor R_B sets the level of base current for the operating point. Similarly, applying KVL to the output loop, we can write

$$V_{CC} = I_C R_C + V_{CE} + V_E = (I_C + I_B) R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C - V_E \tag{3.34}$$

$$I_C R_C = (V_{CC} - V_{CE} - V_E)$$

Re-arranging, we get

$$I_C = \frac{V_{CC} - V_{CE} - V_E}{R_R} \tag{3.35}$$

Equations (3.31), (3.32) and (3.33) represent the *Q*-point for the circuit and these equations can be represented on the device output characteristics as indicated in Fig. 3.20(b). In order to analyse the stability and performance of the circuit, let us find the stability factor of the circuit using Eq. (3.17). Differentiating Eq. (3.31) with respect to I_C, we get

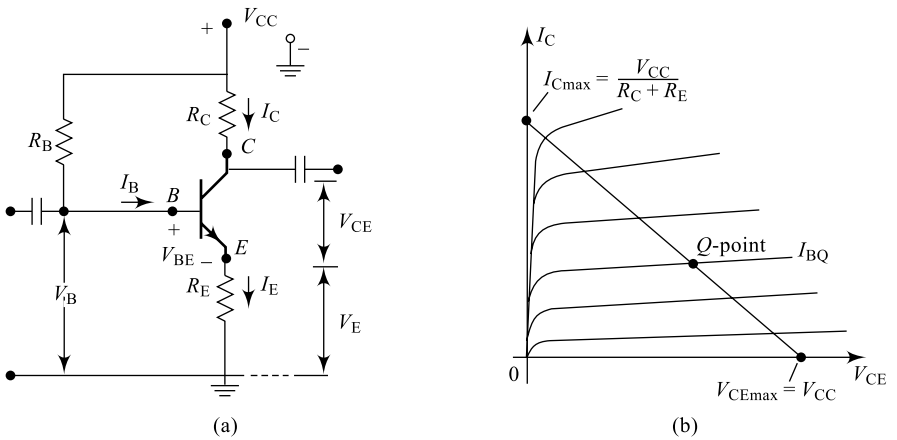


Fig. 3.20 (a) Self-bias circuit (b) Self-bias load line

$$\frac{\Delta I_B}{\Delta I_C}\left(1+\frac{R_C}{R_B}\right)=0-0-\frac{R_E}{R_B},\quad \text{i.e.}\ \frac{\Delta I_B}{\Delta I_C}=-\frac{R_E}{R_E+R_B}$$

Substituting this value in Eq. (3.17), we get the stability factor

$$S=\frac{(1+\beta)}{\left[1-\beta\left(-\frac{R_E}{R_E+R_B}\right)\right]}$$

$$S=\frac{(1+\beta)}{\left[1+\beta\left(\frac{R_E}{R_E+R_B}\right)\right]} \tag{3.36}$$

Equation (3.34) clearly indicates S is large, but certainly less as compared to the value obtained in fixed biasing and feedback biasing case. The Q-point stability is affected by β variations; any change in the β has a direct impact on V_{CE}, and I_C and needs to be addressed which is done in the self-bias circuit with a potential dividing network. The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change.

Example 3.9

A self-bias configuration for a BJT is shown in Fig. 3.21. If the supply voltage is 10 V, β = 50, R_C = 2.2 kΩ, R_B = 470 kΩ and V_{BE} = 0.7 V, determine (a) the operating point (Q-point), and (b) the base voltage V_B.

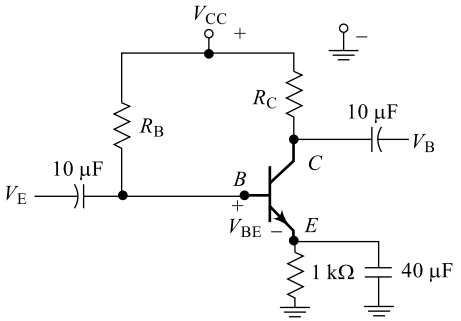


Fig. 3.21 For Example 3.9

Solution

(a) We have from Eq. (3.33),

$$I_{BQ}=\frac{V_{CE}-V_{BE}}{R_B+(1+\beta)R_E}$$

$$=\frac{10-07}{470k+(50+1)1k}$$

$$=17.853\ \mu A$$

From Eq. (3.8),

$$\beta=\frac{I_{CQ}}{I_{BQ}}=\frac{I_{CQ}}{17.853\ \mu A}=50$$

$$I_{CQ}=0.893\ \text{mA}$$

We have KVL to output loop resulting in

$$V_{CC}=V_{RC}+V_{CE}+V_E$$

i.e. $V_{CEQ}=V_{CC}-V_{RC}-V_E$

$$=10-0.893\ \text{mA}\times 2.2k-(0.893\ \text{mA}+17.853\ \mu A)k=7.125\ \text{V}$$

(b) We have

$$V_B=V_E+V_{BE}=0.91+0.7=1.61\ \text{V}$$

3.13 VOLTAGE DIVIDER-BIAS CONFIGURATION

In Eq. (3.34), it can be observed that S value is dependent on R_B. Generally, R_B is a large value which means S is large and hence variation of collector is large. In order to reduce the S value, R_B is split into two values, namely R_1 and R_2, forming a parallel combination. The resulting circuit is called a **potential divider-bias circuit** or voltage divider-bias configuration and is indicated in Fig. 3.22(a). In the previous bias configurations, the bias current and voltage were a function of the transistor current gain β. However, because β is temperature sensitive, especially for silicon transistors, it would be desirable to develop a bias circuit that is independent of β, the transistor gain. This circuit can be analysed either on exact basis or an approximation basis and if analysed on an exact basis, the sensitivity to changes in β is negligibly small. By properly choosing the circuit parameters, the resulting levels of I_C and V_{CE} can be made almost totally independent of β. As noted earlier, there are two methods that can be applied to analyse the voltage-divider configuration. The first method is the exact method, which can be applied to any voltage-divider configuration and the second method is an approximate method and can be applied only with specific circuit conditions. The approximate method is a more direct analysis which saves time and can be applied to the majority of situations.

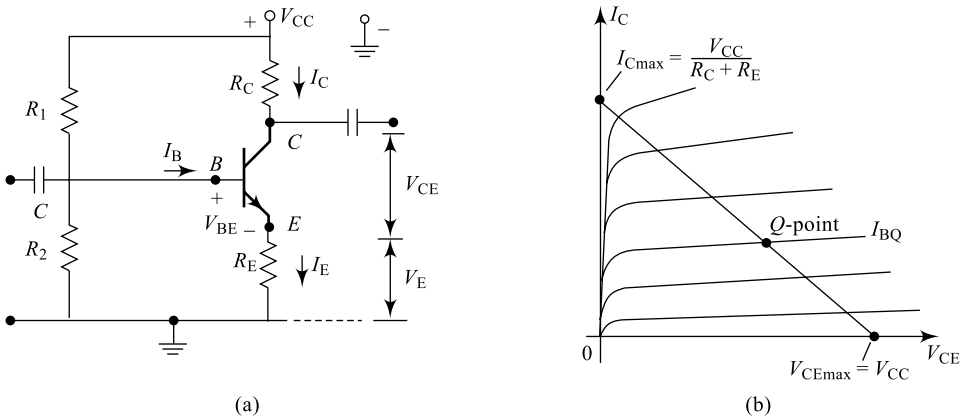


Fig. 3.22 (a) Potential divider-bias circuit (b) Potential divider-bias load line

3.13.1 Analysis Using Exact Method

Applying Thevenin's theorem at the input side of the circuit, we can draw the Thevenin's equivalent circuit; R_{TH} is the Thevenin's equivalent impedance and V_{TH} is the Thevenin's equivalent voltage. For dc analysis, the network of Fig. 3.22(a) can be redrawn as shown in Fig. 3.23.

The Thevenin's equivalent values are obtained as below:

$$R_{\downarrow TH} = R_{\downarrow}1 \| R_{\downarrow}2 = (R_{\downarrow}1\ R_{\downarrow}2)/(R_{\downarrow}(1) + R_{\downarrow}2) \tag{3.37}$$

and

$$V_{TH} = V_{R2} = \frac{V_{CC}\, R_2}{R_1 + R_2} \tag{3.38}$$

The analysis will be performed by first examining the base circuit; applying KVL to the input loop containing V_{TH}, R_{TH}, R_E and V_{BE}, we get

$$V_{TH} = V_B = I_B R_B + V_{BE} + V_E$$

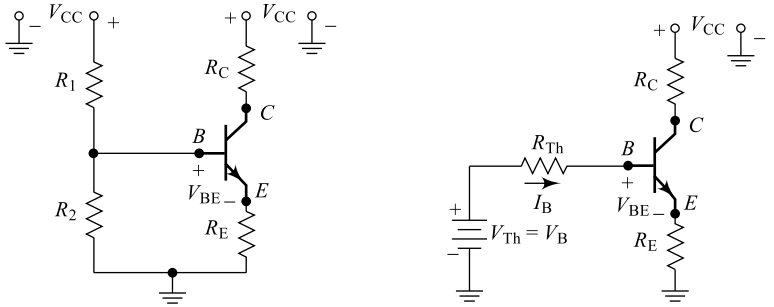


Fig. 3.23 (a) Voltage divider-bias circuit re-drawn (b) Thevinised circuit

Substituting $V_E = I_E R_E$ and $I_E = (I_C + I_B)$

$$V_{TH} = V_B = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$I_B = \frac{V_B \mid V_{BE} - I_C R_E}{(R_B + R_E)}$$

and re-arranging the terms, we get

$$I_{BQ} = \frac{V_B}{(R_B + R_E)} - \frac{V_{BE}}{(R_B + R_E)} - \frac{I_C R_E}{(R_B + R_E)} \tag{3.39}$$

Similarly, applying KVL to the output loop, we can write

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

$$V_{CC} = I_C R_C + V_{CE} + (I_C + I_B) R_C$$

$$V_{CEQ} = V_{CC} - I_C R_C - (I_C + I_B) R_C$$

$$V_{CEQ} = V_{CC} - I_B R_C - (R_E + R_C) I_C \tag{3.40}$$

$$I_{CQ} = (V_{CC} - V_{CE} - I_B R_E)$$

Re-arranging, we get

$$I_{CQ} = \frac{V_{CC} - V_{CE} - V_E}{(R_C + R_E)} \tag{3.41}$$

Equations (3.37), (3.38) and (3.39) represent the Q-point for the circuit and these equations can be represented on the device output characteristics as indicated in Fig. 3.22(b). In order to analyse the stability and performance of the circuit, let us find the stability factor of the circuit using Eq. (3.17). Differentiating Eq. (3.37) with respect to I_C, we get

$$\frac{\Delta I_B}{\Delta I_C} = 0 - 0 - \frac{R_E}{(R_C + R_E)} \quad \text{i.e.} \frac{\Delta I_B}{\Delta I_C} = -\frac{R_E}{R_E + R_B} \text{ where } R_B \text{ is given by Eq. (3.35).}$$

Substituting this value in Eq. (3.17), we get stability factor

$$S = \frac{(1 + \beta)}{\left[1 - \beta\left(-\frac{R_E}{R_E + R_B}\right)\right]}$$

$$S = \frac{(1+\beta)}{\left[1+\beta\left(\frac{R_E}{R_E+R_B}\right)\right]} \tag{3.42}$$

Equation (3.40) clearly indicates S is similar to the one in Eq. (3.34), but certainly less as compared to the value obtained in self-bias, fixed biasing and feedback biasing case. This is because R_B is small in this case and hence S, thereby offering better stability.

Example 3.10

A self-biasing configuration with potential divider circuit for a BJT is shown in Fig. 3.24. Determine for the circuit (a) Thevinised input equivalent circuit, (b) the operating point (Q-point), and (c) the base voltage V_B.

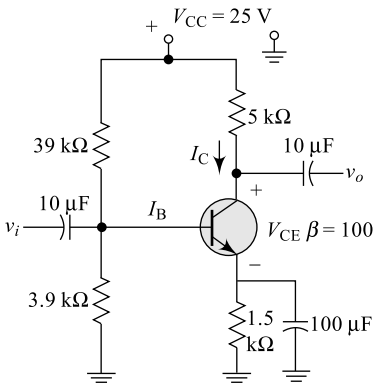


Fig. 3.24 For Example 3.10

Solution

(a) We have from Eq. (3.37),

$$R_{\downarrow TH} = R_{\downarrow}B = R_{\downarrow}1 \parallel R_{\downarrow}2 = (R_{\downarrow}1\ R_{\downarrow}2)/(R_{\downarrow}(1) + R_{\downarrow}2)$$

$$= (39k \times 3.9k)/(39k + 3.9k) = 3.55\ \text{k}\Omega$$

and from Eq. 3.38

$$V_{TH} = V_{R2} = \frac{V_{CC}\,R_2}{R_1 + R_2} = \frac{25 \times 3.9\,k}{39\,k + 3.9\,k} = 2.273\ \text{V}$$

(b) Applying KVL to the Thevinised input loop, we get

$$V_{TH} = V_B = I_B R_B + V_{BE} + (I_B + I_C)R_E = I_B R_B + V_{BE} + (I_B + \beta\, I_B)R_E$$

i.e. $$I_{BQ} = \frac{V_B - V_{BE}}{R_B + (1+\beta)\,R_E} = \frac{25 - 07}{3.55\,k + (100+1)1.5\,k} = 156.724\ \mu\text{A}$$

From Eq. (3.8)

$$\beta = \frac{I_{CQ}}{I_{BQ}} = \frac{I_{CQ}}{156.724\ \mu\text{A}} = 100$$

$$I_{CQ} = 15.673\ \text{mA}$$

From Eq. (3.40),

$$V_{CEQ} = V_{CC} - I_B R_C - (R_E + R_C)I_C$$

$$V_{CEQ} = 25 - 156.724\ \mu\text{A} \times 5k - (5k + 1.5k) \times 15.673\ \text{mA}$$

$$= 14.81\ \text{V}$$

(b) We have

$$V_B = V_E + V_{BE} = 2.37 + 0.7 = 3.07\ \text{V}$$

3.13.2 Analysis Using Approximate Method

In the approximate analysis, the input resistance of the transistor R_{in} measured between base terminal and ground is assumed to be much larger than R_2 (which is not true under most circumstances). The input section of the voltage divider-bias is represented as in Fig. 3.25(a) for simplicity. It can be shown

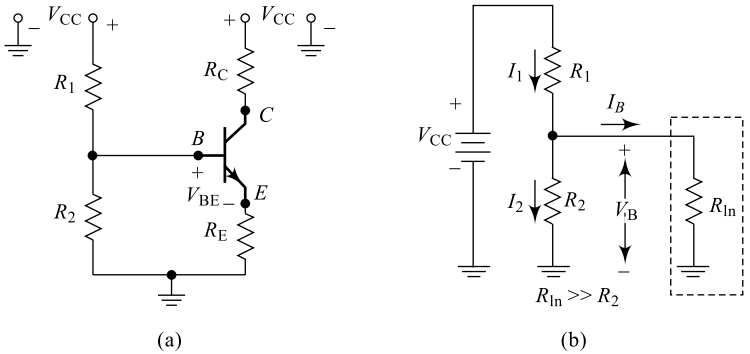


Fig. 3.25 (a) Voltage divider-bias circuit re-drawn (b) Approximated circuit

that the input resistance between base and emitter of a transistor is given by the equation containing the current gain as

$$R_{in} = (1 + \beta)R_E \cong \beta R_E \tag{3.43}$$

If R_{in} is much larger than R_2 ($\beta R_E >> 10R_2$) then most of I_1 flows through R_2 and only a negligible current flows into the base of the transistor. This implies that $I_B = 0$ and $I_1 = I_2$. Now, the voltage across R_2 can be estimated using voltage divider rule (hence, the name voltage divider or potential divider bias) as

$$V_B = V_{R2} = \frac{V_{CC} R_2}{R_1 + R_2} \tag{3.44}$$

Now, the voltage across R_E can be estimated as $V_E = V_B - V_{BE}$ (3.45)

The current through R_E can be estimated as $I_E = V_E/R_E \cong I_{CQ}$ (3.46)

The collector-emitter voltage is given by the equation

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E); \quad \because \qquad I_C \cong I_E \tag{3.47}$$

Equations (3.44) and (3.45) represent the Q-point and it is important to note that the bias circuit is independent of the current gain β of the transistor.

3.14 BIAS COMPENSATION

In the preceding sections, different biasing techniques which are necessary to maintain an operating point were discussed. The circuits used to fix up the Q-point, however, result in a form of negative feedback (to be discussed in Chapter 4, sections 4.6 and 4.7) and reduce the gain of the amplifier. In order to make stabilisation more effective and minimise the gain loss, it is necessary to provide compensation techniques and the circuits used to achieve this are called **bias-compensation circuits**. Different compensation techniques can be adapted and accordingly the circuits can be designed; some of the most commonly used compensation circuits are discussed in this section.

1. Diode Compensation for I_{CO}

A germanium device is more sensitive to temperature changes since its I_{CO} changes more compared to a silicon device. Similarly, in a silicon device, V_{BE} changes with temperature cause more serious

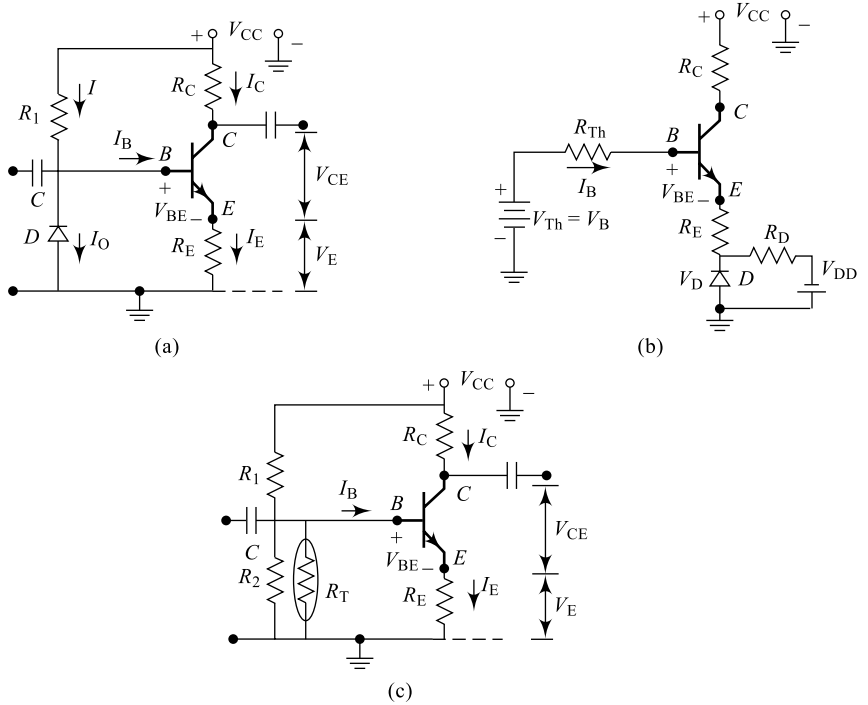


Fig. 3.26 (a) I_{CO} compensation (b) V_{BE} compensation (c) Temperature compensation

problems than in germanium devices. The arrangement shown in Fig. 3.26(a) is for I_{CO} compensation in a germanium transistor; use of a germanium diode between base and ground minimises the effect of I_{CO} on I_C. This diode gets reverse bias by V_{BE} allowing the reverse saturation current to flow through D to ground.

We have

$$I = \frac{V_{CC} - V_{BE}}{R_1} \cong \frac{V_{CC}}{R_1} \tag{3.48}$$

$\therefore$ $I_B = (I - I_O)$

Now $I_C = \beta I_B + (1 + \beta) I_{CO}$

$$I_C = \beta(I - I_O) + (1 + \beta) I_{CO} \tag{3.49}$$

If $\beta >> 1$ and if I_O of D and I_{CO} of transistor track each other over a desired temperature range then $I_C = \beta I \approx$ essentially remains constant. Thus, the dependence of I_C on I_{CO} and I_B is minimised; stability of Q-point is hence more.

2. Diode Compensation for V_{BE}

The effect of V_{BE} variations on Si transistors (which is more compared to a Ge transistor) can be minimised by using an Si diode in the emitter path as shown in Fig. 3.26(b). The diode D is forward biased by V_{DD} and R_d.

KVL to the base loop gives

$$V = V_{BE} + I_B R_b - V_D + (I_B + I_C) R_E$$

$$V - V_{BE} + V_D - I_C R_E = I_B (R_E + R_b)$$

$$I_B = \frac{V - V_{BE} - I_C R_E + V_D}{(R_b + R_F)} \tag{3.50}$$

Now

$$I_C = \beta I_B + (1 + \beta) I_{CO}$$

$$I_C = \beta \left(\frac{V - V_{BE} - I_C R_E + V_D}{(R_b + R_E)} \right) + (1 + \beta) I_{CO}$$

$$I_C = -\beta \left(\frac{I_C R_E}{(R_b + R_F)} \right) + \beta \left(\frac{V - V_{BE} + V_D}{(R_b + R_E)} \right) + (1 + \beta) I_{CO}$$

$$I_C = \beta \left(\frac{(V - V_{BE} + V_D + (R_b + R_E)(1 + \beta) I_{CQ})}{R_b + R_E (1 + \beta)} \right) \tag{3.51}$$

Since V_{BE} tracks V_D changes with respect to temperature, I_C becomes independent of V_{BE} variations; thus offering more stable Q-point.

3. Temperature Compensation

Here, in this case, a thermistor with negative temperature coefficient of resistance (α) is connected across R_2 as shown in Fig. 3.26(c). Under normal temperature conditions (room temperature), the required bias is applied to the device through ($R_2 \parallel R_T$); since R_T is very high during this condition, the parallel combination yields R_2. With increasing temperature, R_T reduces and drop across R_T also reduces. This reduces the forward bias on the BE junction and there will be no increase in I_C due to temperature.

3.15 EMITTER-FOLLOWER CONFIGURATION

Out of the three transistor configurations introduced in Section 3.3, the Common Collector (CC) configuration offers very good input and output impedance values that aid circuit performance. In most cases, the output voltage is typically taken at the collector terminal of the BJT, but in a CC configuration, the output is taken at the emitter terminal as shown in Fig. 3.27. It is already discussed in Section 3.3.3 that in a CC configuration, the voltage gain is not more than unity which implies that emitter (output) voltage follows the input voltage and, hence, the name *emitter follower circuit*. An emitter follower circuit is typically used for matching impedance between source and load, current amplification, for providing driving capabilities (driver or buffer), etc. It can be noticed that there is no R_C in the circuit and V_E is the output voltage. The following results (derivation is beyond the scope of this text) can be used for the network shown;

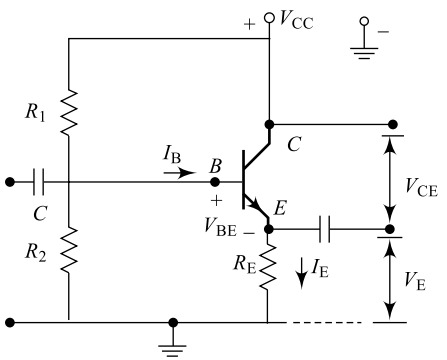


Fig. 3.27 Emitter follower circuit

$$\text{Input impedance } Z_{in} = \beta(r_e + R_E) \cong \beta(R_E) \tag{3.52}$$

$$\text{Output impedance } Z_O = R_E \parallel r_e \tag{3.53}$$

$$\text{Voltage gain } A_V = \frac{R_E}{R_E + r_e} \tag{3.54}$$

$$\text{Current gain } A_i = \gamma = (1 + \beta) \tag{3.55}$$

3.16 TRANSISTOR AS A SWITCH

A transistor can be used as an electronic switch when operated between its cut-off region and saturation region on its characteristics. When in cut-off region, Q is an OPEN switch and when in saturation region, Q is a CLOSED switch. When the switch is in the "ON" position, we have a fixed-bias situation where the base-to-emitter voltage is 0.7 V, the base current is controlled by the base resistor and the input impedance of the transistor. When the switch is in the "OFF" position, there is no current flowing through the device. The circuit diagram and the corresponding waveforms are shown in Fig. 3.28.

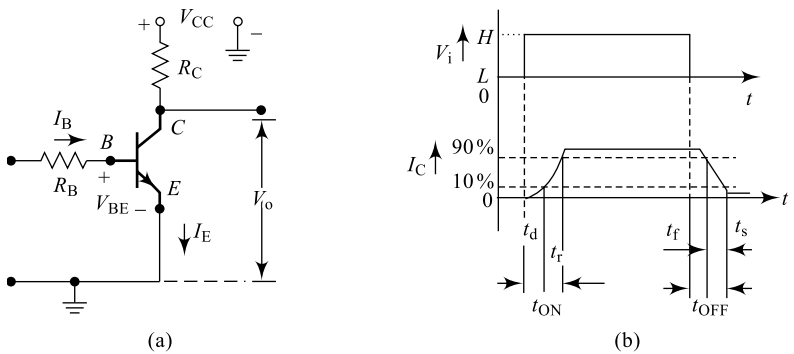


Fig. 3.28 (a) Transistor switch (b) Switching waveforms

With $V_i = 0$, the transistor will be in cut-off position and collector current $I_C = 0$; once V_i rises high, slowly the collector current builds and reaches maximum. It can be observed here that there is a non-zero device turn-on period because of device characteristics and the input signal. It is given by

$$t_{ON} = t_d + t_r \tag{3.56}$$

Here, t_d = **Delay time** depends on device characteristics like junction capacitance, time for charge carriers to reach collector region (transit time), time needed for I_C to build up to 10%, and

t_r = **Rise time** defined as time taken by the collector current to rise from 10 to 90% of its maximum value.

It is given by $t_r =$

$$\tau_r = h_{fe}\left(R_c C_c + \frac{1}{\omega T}\right) \tag{3.57}$$

Here, R_C is collector resistance, C_C is collector transition capacitance and ω is frequency at which current gain is one.

Similarly, when the device is turned OFF by withdrawing the input signal, it takes a definite amount of time. As indicated in the waveforms, the turn-off time is given by

$$t_{OFF} = t_f + t_S \tag{3.58}$$

Here, t_f = **Fall time** defined as time taken by the collector current to fall from 90 to 10% of its maximum value and

t_S = **Storage time** defined as time taken to eliminate completely all the stored charges from the base of the transistor ($t_S \approx 2$ to 3 t_r or t_f). t_{OFF} is also called **reverse recovery time** (t_{rr}) and it even includes time for I_C to fall up to 90%.

Example 3.11

Referring to Example 3.3, the *PNP* transistor is replaced by an *NPN* transistor as shown in Fig. 3.29 and other parameters remain unchanged. Find the value of the base resistor (R_B) required to switch the load ON when the input terminal voltage exceeds 2.5 V.

Solution We have the solution for $\beta = 200$, $I_C = 4$ mA and $I_b = 20$ μA

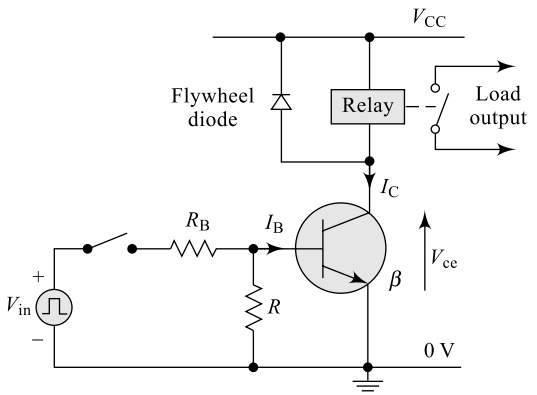


Fig. 3.29 For Example 3.11

Now, $R_B = \dfrac{V_{in} - V_{BE}}{I_B} = \dfrac{2.5 - 0.7}{20\ \mu A} = 90\ k\Omega$

Example 3.12

Again using the same values as in Example 3.11, find the minimum base current required to turn the transistor fully ON (saturated) for a load that requires 200 mA of current.

Solution $I_B = \dfrac{I_C}{\beta} = \dfrac{200\ mA}{200} = 1\ mA$

Table 3.4 Comparison between different biasing methods

Sl. No.	Parameter	Fixed Bias	Feedback Bias	Self-Bias	Potential Divider Bias
1	Number of resistors	Two	Two	Three	Four
2	$\frac{\Delta I_B}{\Delta I_C}$	Zero	$\frac{\Delta I_B}{\Delta I_C} = -\frac{R_C}{R_C + R_E}$	$\frac{\Delta I_B}{\Delta I_C} = -\frac{R_E}{R_E + R_B}$	$\frac{\Delta I_B}{\Delta I_C} = -\frac{R_E}{R_E + R_B}$
3	Stability Factor S	$S = (1 + \beta)$	$S = \frac{(1+\beta)}{\left[1+\beta\left(\frac{R_C}{R_C + R_B}\right)\right]}$	$S = \frac{(1+\beta)}{\left[1+\beta\left(\frac{R_E}{R_E + R_B}\right)\right]}$	$S = \frac{(1+\beta)}{\left[1+\beta\left(\frac{R_E}{R_E + R_B}\right)\right]}$
4	Performance	Poor	Poor	Better than the previous two	Best
5	Stability against load variations	No	No	Yes	Yes
6	Stability against β variations	No	No	No	Yes

Summary

- Semiconductor devices have played a great role in replacing vacuum-tube devices and have the following advantages: They are (a) of smaller size, (b) more lightweight, (c) more rugged, and (d) more efficient. In addition, they have (e) no warm-up period, (f) no heater element requirement, (g) lower operating voltages, and (h) lower operating powers.
- Transistors are two-junction, three-terminal and three-layer semiconductor devices with a base (B) or centre layer which is thinner than the other two layers. The outer two layers called the emitter (E) and the collector (C) are both of either N-type or P-type materials, while the centre layer is of opposite type.
- Out of the two PN junctions J_1 and J_2, the junction J_1 (also called BE junction) is forward biased and the junction J_2 (also called CB junction) is reverse biased.
- The dc emitter current which is the sum of the collector current and the base current is always the largest current of a transistor, whereas the base current is always the smallest.
- The collector current is made up of two components: the majority component and the minority current (also called the leakage current).
- The arrow in the transistor symbol is used to find the transistor type, either *NPN* or *PNP*, and it indicates the direction of conventional emitter current flow.
- There are three regions of operation for the device, namely the active region, the saturation region and the cut-off region.
- In the active region of a transistor, the base-emitter junction (J_1) is forward biased and the base-collector junction (J_2) is reverse biased.

- In the cut-off region, both the base-emitter junction (J_1) and base-collector junction (J_2) of the transistor are reverse biased.
- In the saturation region, both the base-emitter junction (J_1) and base-collector junction (J_2) are forward biased.
- On an average basis, the base-to-emitter voltage V_{BE} for a conducting silicon transistor will be approximately 0.7 V and that for a germanium transistor will be 0.3 V.
- The quantity alpha (α) is common-base current gain and relates the collector and emitter currents; its value is always a maximum of one.
- The quantity beta (β) is common-emitter current gain and relates the collector and base currents; its value is always large and normally in the range of 50 to 400.
- The quantity gamma (γ) is common-collector current gain and relates the base and emitter currents; its value is always one greater than beta.
- The dc beta is defined by a simple ratio of dc currents at an operating point, whereas the ac beta is sensitive to the characteristics in the region of interest. (For most applications, however, the two are considered equivalent as a first approximation.)
- The maximum rated power for a transistor is the product of V_{CE}, the collector-to-emitter voltage and I_C, the collector current.
- The Q-point (operating point) is the I_C, I_B and V_{CE} values for a transistor under dc conditions and is fixed up by an external dc supply and a set of resistors.
- In an amplifier, for linear amplification with minimum distortion (faithful amplification), the dc operating point should be exactly at the middle of the load line (not too close to the maximum power or voltage or current rating) and should be in the active region.
- The saturation and cut-off regions are suitable for switching applications of the transistor.
- The fixed-bias configuration is the simplest of transistor biasing arrangements, but it is unstable due to its high S value and sensitivity to β at the operating point.
- The equation for the load line of a transistor network can be found by applying Kirchhoff's voltage law (KVL) to the output or collector network. The Q-point is then determined by finding the intersection between the base current and the load line drawn on the device output characteristics.
- The emitter-stabilised biasing arrangement (self-bias) is less sensitive to changes in β providing more stability for the network.
- The self-bias circuit with voltage divider network is probably the most popular of all the configurations since it offers very good stability and β independence.
- A common-base configuration offers good voltage gain, poor current gain (no power amplification), and poor impedance matching; suitable for high-frequency applications.
- A common-emitter configuration offers good voltage gain, good current gain (suitable for power amplification) and moderate impedance matching; suitable for most applications.
- A common-collector configuration offers good current gain, poor voltage gain (no power amplification) and very good impedance matching; suitable for driver stages and buffering.
- When used as a switch, a transistor quickly moves between saturation and cut-off regions and the impedance between collector and emitter can be approximated as a short circuit for saturation and an open circuit for cut-off.
- The analysis of *PNP* configurations is exactly the same as that applied to *NPN* transistors with the exception that current directions will reverse and voltages will have the opposite polarities.
- V_{BE}, β and I_{CO} are the three temperature-sensitive parameters of the transistor; beta is very sensitive to temperature and the reverse saturation current doubles for every 10°C rise in temperature.
- A bias compensation is needed whenever a bias circuit is used.

Review Questions

1. Sketch the basic construction of both *NPN* and *PNP* transistors: Draw their circuit symbols and mark various current components (minority and majority carriers).
2. Name the unipolar and bipolar devices you know and what is the major difference between a bipolar and a unipolar device?
3. How many junctions, layers and terminals are there in a transistor? Name them. In order to realise a transistor amplifier, how do we bias the junctions of the transistor?
4. What is the source of the leakage current in a transistor? Sketch figures to indicate the majority and minority carrier flow in *PNP* and *NPN* transistors.
5. In a transistor, why is emitter current approximated to collector current? What is the equation that relates all the three currents?
6. Define current gains for all the three transistor configurations.
7. Write relations between all the three current gains.
8. Recalling diode resistances in Chapter 2, define input resistance for a transistor using transistor input characteristics.
9. Recalling diode resistances in Chapter 2, define output resistance for a transistor using transistor output characteristics.
10. Sketch the common-base BJT transistor configuration for an *NPN* transistor and indicate the polarity of the applied bias and resulting current directions.
11. Sketch the common-emitter BJT transistor configuration for an *NPN* transistor and indicate the polarity of the applied bias and resulting current directions.
12. Sketch the common-collector BJT transistor configuration for an *NPN* and indicate the polarity of the applied bias and resulting current directions.
13. Is BJT a current-controlled device or a voltage-controlled device?
14. Sketch the input–output characteristics of a common-emitter BJT transistor configuration.
15. Sketch the input–output characteristics of a common-base BJT transistor configuration
16. Define I_{CBO} and I_{CEO}. How are they different? How are they related? Are they typically close in magnitude?
17. Mark different regions of operation on the output characteristics of a transistor.
18. Why is it necessary to establish a dc condition in a transistor circuit?
19. What do you mean by an operating point? What is its importance?
20. Draw a load line on the characteristics for a fixed-bias configuration.
21. Draw a load line on the characteristics for a feedback-bias configuration.
22. Draw a load line on the characteristics for a self-bias configuration.
23. Draw a load line on the characteristics for a voltage divider-bias configuration.
24. Explain how do you measure the performance of a biasing network?
25. Explain why the operating point needs to be stable. What are the factors that affect *Q*-point stability?
26. Define stability factor for a bias network.
27. Derive the general expression for stability factor.
28. Derive the expression for stability factor of a fixed-bias circuit.
29. Derive the expression for stability factor of a feedback-bias circuit.
30. Derive the expression for stability factor of a self-bias circuit**.**
31. Derive the expression for stability factor of a self-bias circuit with voltage divider network.
32. What is the need for bias compensation?
33. Discuss different timing components related to transistor switch.

Exercise Problems

1. If the emitter current of a transistor is 10 mA and the base current is only 1% of the collector current, determine the values of base current and the collector current.
2. Find all the three current gains in the above case
3. If the emitter current of a transistor is 8 mA and alpha is 0.9988, determine the values of I_C and β.
4. **(a)** For a certain transistor, α_{dc} is 0.998, determine its collector current if $I_E = 5$ mA.
   (b) What is its I_E if $I_B = 50$ µA and α_{dc} is 0.989?
5. **(a)** A set of input characteristics is shown for a certain transistor in Fig. P3.5; using these characteristics, determine V_{BE} at 5 mA for $V_{CE} = 10$ V.
   (b) What percentage change do you observe in V_{BE} at 5 mA for $V_{CE} = 1$ V.
6. In Problem 5(a), if the collector-to-emitter voltage is doubled, what percentage change do you observe in V_{BE} at 5 mA?
7. **(a)** Calculate the voltage gain (A_V) for the CB configuration network of Fig. P3.7.
   (b) If the input impedance reduces to 20 Ω, what change do you observe in gain?

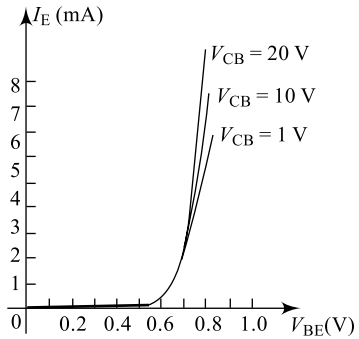


Fig. P3.5

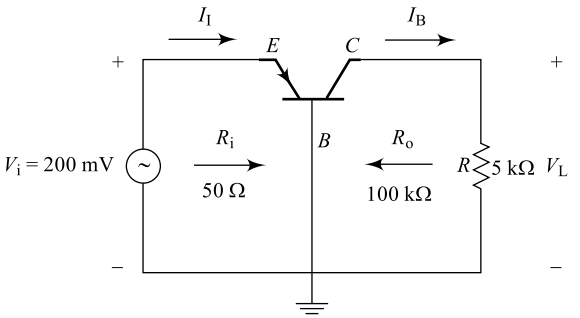


Fig. P3.7

8. **(a)** Using the characteristics of Fig. P3.8, determine the resulting collector current if $I_E = 5.5$ mA and $V_{CE} = 10$ V.
   (b) Find the corresponding β for the transistor.

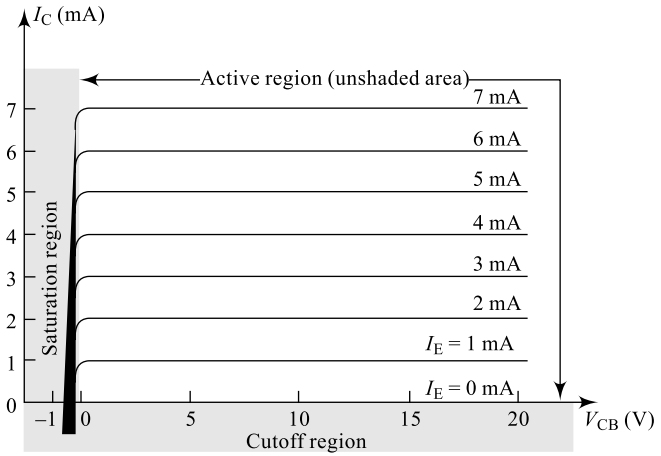


Fig. P3.8

9. In Problem 8(a), if the collector-to-emitter voltage is maintained at 10 V, what is the output impedance of the transistor you observe?

10. Using the input characteristics of a CE transistor configuration shown in Fig. P3.10,
(a) Find the value of I_B corresponding to V_{BE} = 800 mV and V_{CE} = 20 V.
(b) Find the corresponding value of input impedance.

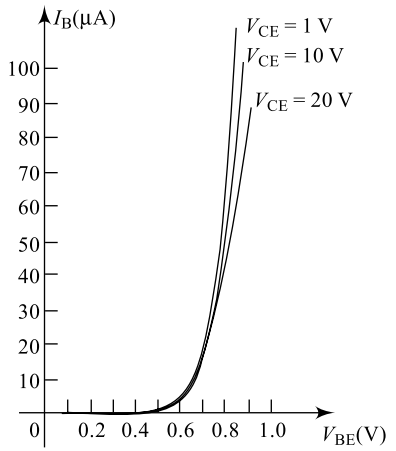


Fig. P3.10

11. **(a)** In Problem 10(a), if the collector-to-emitter voltage is halved, what percentage change do you observe in I_B at V_{BE} = 800 mV.
(b) Find the corresponding value of input impedance.

12. Using the output characteristics of a certain CE configuration shown in Fig. P3.12, determine collector current at V_{CE} = 5 V for I_B = 40 μA.

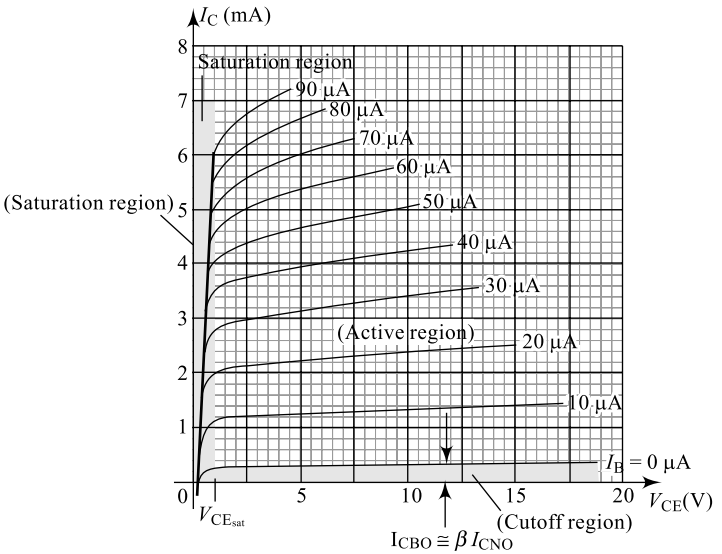


Fig. P3.12

13. **(a)** In Problem 12, if the collector-to-emitter voltage is maintained and the base current is increased to 150%, what percentage change do you observe in I_C?
(b) Find the corresponding value of output impedance.

14. For the fixed-bias configuration of Fig. P3.14, if β = 100, determine the operating point and stability factor S_{Ico}.

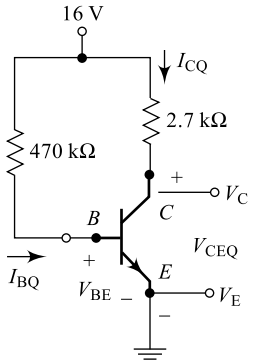


Fig. P3.14

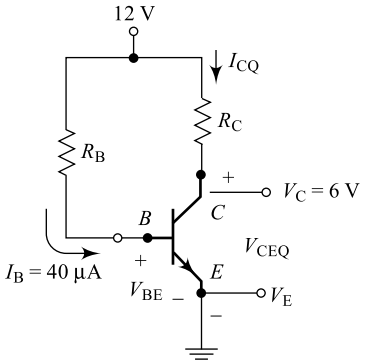


Fig. P3.16

15. In Problem 14, if the transistor is replaced with another having β = 150, what is the new operating point?

16. For the fixed-bias configuration of Fig. P3.16, if β = 100, then determine the values of R_C, R_B and I_C.

17. For the fixed-bias configuration of Fig. P3.17, determine the values of β, V_{CC} and R_B.

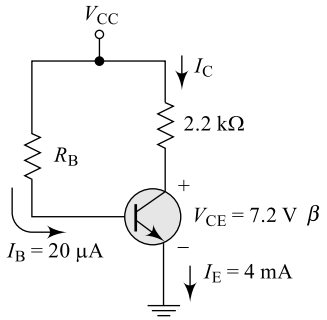


Fig. P3.17

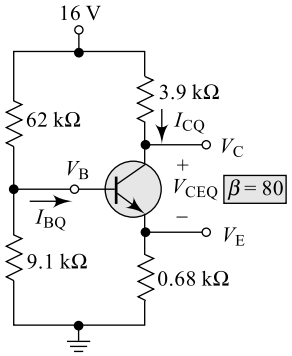


Fig. P3.19

18. For the bias configuration of Fig. P3.18, determine the operating point.

19. **(a)** For the potential divider-bias network shown in Fig. P3.19, determine the operating point
(b) What is the value of the stability factor S_{Ico}?

20. **(a)** In Problem 19, if the transistor is replaced with another having β = 150, what is the new operating point?
(b) What is the new value of the stability factor S_{Ico}?

Multiple-Choice Questions

1. A transistor is a three-layered three-terminal and _____ junction semiconductor device.
   (a) three (b) two (c) four (d) zero
2. An amplifier is a circuit that increases the level of an input _____.
   (a) voltage (b) current (c) both (a) and (b) (d) none of the above
3. The transistor configuration that is more suitable for amplification is _____.
   (a) CE configuration (b) CB configuration (c) CC configuration (d) all the above
4. The transistor configuration that is more suitable for high-frequency applications is _____.
   (a) CE configuration (b) CB configuration (c) CC configuration (d) all the above
5. The transistor configuration that is more suitable for driver stage is _____.
   (a) CE configuration (b) CB configuration (c) CC configuration (d) all the above
6. The transistor configuration that is more suitable for power amplification is _____.
   (a) CE configuration (b) CB configuration (c) CC configuration (d) all the above
7. The transistor configuration that is more suitable for impedance matching is _____.
   (a) CE configuration (b) CB configuration (c) CC configuration (d) all the above
8. The transistor configuration that is more suitable for current amplification is _____.
   (a) CE configuration (b) CB configuration (c) CC configuration (d) all the above
9. The transistor configuration which offers a phase reversal between input and output signal is _____.
   (a) CE configuration (b) CB configuration (c) CC configuration (d) all the above
10. The CB and CC transistor configurations introduce a phase shift of _____ between input and output signals.
    (a) 180° (b) 90° (c) 0 or 360° (d) none of the above
11. The transistor configuration that produces an output voltage which is almost a replica of the input voltage is _____.
    (a) CE configuration (b) CB configuration (c) CC configuration (d) all the above
12. The transistor configuration that produces an output current which is almost a replica of the input current is _____.
    (a) CE configuration (b) CB configuration (c) CC configuration (d) all the above
13. The transistor gains α and β are related to each other through the following equation:
    (a) $\beta_{dc} = \alpha_{dc}$ (b) $\beta_{dc} = \dfrac{\alpha_{dc}}{1 + \alpha_{dc}}$ (c) $\beta_{dc} = \dfrac{\alpha_{dc}}{1 - \alpha_{dc}}$ (d) $\beta_{dc} = \dfrac{\alpha_{dc}}{\alpha_{dc} - \alpha_{dc}}$
14. The transistor gains γ and β are related to each other through the following equation:
    (a) $\beta_{dc} = \gamma_{dc}$ (b) $[\gamma_{dc} = (1 + \beta]_{dc})$ (c) $\beta_{dc} = \dfrac{\alpha_{dc}}{\gamma_{dc} - \alpha_{dc}}$ (d) $\beta_{dc} = \dfrac{\alpha_{dc}}{\gamma_{dc} + \alpha_{dc}}$
15. If $\alpha = 0.987$ for a certain transistor then its β is _____.
    (a) 0.789 (b) 100.987 (c) 50.789 (d) 75.923
16. The transistor gains γ and α are related to each other through the following equation:
    (a) $\alpha_{dc} = \gamma_{dc}$ (b) $[\gamma_{dc} = (1 + \alpha]_{dc})$ (c) $\gamma_{dc} = \dfrac{1}{1 - \alpha_{dc}}$ (d) $\gamma_{dc} = \dfrac{\alpha_{dc}}{\gamma_{dc} - \alpha_{dc}}$
17. If $\alpha = 0.987$ for a certain transistor then its γ is _____.
    (a) 0.789 (b) 100.987 (c) 50.789 (d) 76.923

18. In a transistor biasing circuit, the measure of variation of I_C with respect to I_{CO} or V_{BE} or β is termed _____.
(a) stability factor (b) form factor (c) ripple factor (d) all the above

19. In a fixed-bias circuit, the stability factor is given by _____.
(a) $S = (1 + \beta)$ (b) $S = (1 - \beta)$ (c) $S = (1/\beta)$ (d) none of the above

20. In a feedback bias circuit, the stability factor is given by _____.
(a) $S = (1 + \beta)$ (b) $S = (1 - \beta)$
(c) $S = \dfrac{(1+\beta)}{\left[1+\beta\left(\dfrac{R_C}{R_C+R_B}\right)\right]}$ (d) none of the above

21. In a self-bias circuit, the stability factor is given by _____.
(a) $S = (1 + \beta)$ (b) $S = (1 - \beta)$
(c) $S = \dfrac{(1+\beta)}{\left[1+\beta\left(\dfrac{R_C}{R_C+R_B}\right)\right]}$ (d) $S = \dfrac{(1+\beta)}{\left[1+\beta\left(\dfrac{R_E}{R_E+R_B}\right)\right]}$

22. In a potential divider-bias circuit, the stability factor is given by _____.
(a) $S = (1 + \beta)$ (b) $S = (1 - \beta)$
(c) $S = \dfrac{(1+\beta)}{\left[1+\beta\left(\dfrac{R_C}{R_C+R_B}\right)\right]}$ (d) $S = \dfrac{(1+\beta)}{\left[1+\beta\left(\dfrac{R_E}{R_E+R_B}\right)\right]}$

23. The biasing circuit independent of gain (β) variations is _____.
(a) feedback bias circuit (b) potential divider bias circuit
(c) self bias circuit (d) fixed bias circuit

24. The CB mode current gain α_{dc} is the ratio of _____ to _____.
(a) I_C, I_E (b) I_C, I_B (c) I_B, I_E (d) I_E, I_C

25. The CE mode current gain β_{dc} is the ratio of _____ to _____.
(a) I_C, I_E (b) I_C, I_B (c) I_B, I_E (d) I_E, I_C

26. The CE mode current gain γ_{dc} is the ratio of _____ to _____.
(a) I_C, I_E (b) I_C, I_B (c) I_B, I_E (d) I_E, I_B

27. For a certain transistor if $\beta = 99$ and $I_B = 25$ μA then its emitter current is _____.
(a) 22 mA (b) 2.2 mA
(c) 2.5 mA (d) 0 mA

28. In a certain transistor circuit, the faulty transistor whose $\beta = 99$ and $I_B = 50$ μA is replaced by another transistor with $\beta = 50$; if the same Q-point is to be maintained then what is the new base current required?
(a) 49.5 mA (b) 49.5 μA
(c) 4.95 μA (d) 4.95 mA

29. In the feed-back bias circuit shown in Fig. 3.29, the value of R_B is _____.
(a) 110 Ω (b) 150 Ω
(c) 150 kΩ (d) 110 kΩ

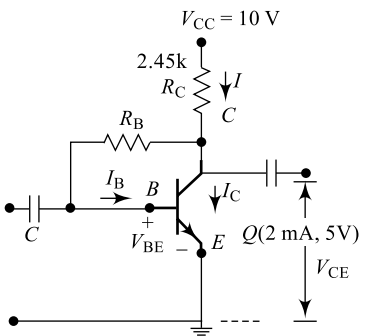


Fig. M3.29

30. If β of the transistor is 50 in the feedback biasing circuit of Fig. M3.29 then its S is _____.
    (a) 68.28 (b) 62.84
    (c) 26.84 (d) 28.64
31. In the fixed biasing circuit of Fig. M3.30, the base current I_B is _____.
    (a) 1.794 mA (b) 1.794 μA
    (c) 17.94 μA (d) 17.94 mA
32. If β of the transistor is 100 in the fixed biasing circuit of Fig. M3.30, then its collector current is _____.
    (a) 17.94 mA (b) 1.794 μA
    (c) 1.794 mA (d) 17.94 μA
33. If β of the transistor is 100 in the fixed biasing circuit of Fig. M3.30, then its operating point is _____.
    (a) (1.794 mA, 3.05 V)
    (b) (17.94 mA, 3.05 V)
    (c) (1.794 mA, 5.05 V)
    (d) (17.94 mA, 5.05 V)
34. If β of the transistor is 100 in the biasing circuit of Fig. M3.30 then its S is _____.
    (a) 50 (b) 26.84
    (c) 100 (d) 101
35. If β of the transistor is changed to 50 in the biasing circuit of Fig. M3.30 then its new value of S is _____.
    (a) 51 (b) 62.84
    (c) 26.84 (d) 102
36. For the load line shown in Fig. M3.36, find V_{CC} and maximum value of I_C.
    (a) 15 mA and 12.5 V
    (b) 15 mA and 15 V
    (c) 12.5 mA and 12.5 V
    (d) 10 mA and 10 V
37. For the load line shown in Fig. M3.36, find the operating point.
    (a) Q(16.5 V, 17 mA) (b) Q(6.5 V, 7 mA)
    (c) Q(6.5 m V, 7A) (d) Q(10 V, 10 mA)
38. For the load line shown in Fig. M3.36, find the value of R_C.
    (a) 1.6 kΩ (b) 10.6 kΩ
    (c) 1.6 kΩ (d) 834 Ω
39. For the load line shown in Fig. M3.36, find the value of R_B.
    (a) 1.6 kΩ (b) 100 kΩ
    (c) 160 kΩ (d) 590 kΩ
40. In the voltage divider-biasing circuit of Fig. M3.40, for the base circuit the R_{TH} and V_{TH} values are _____ and _____.
    (a) 1.6k and 3.6 V (b) 16k and 36 V
    (c) 16k and 0.36 V (d) 16k and 3.6 V

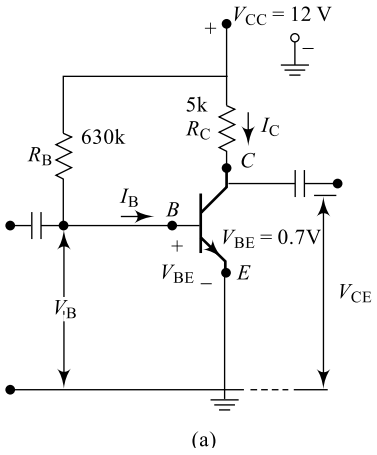


Fig. M3.30

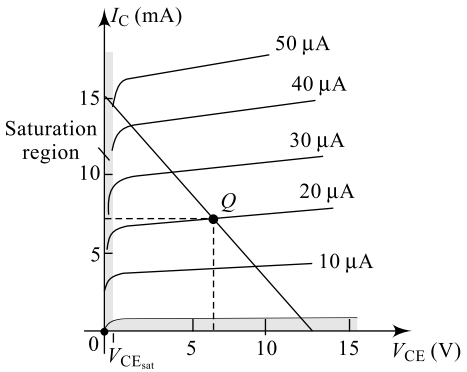


Fig. M3.36

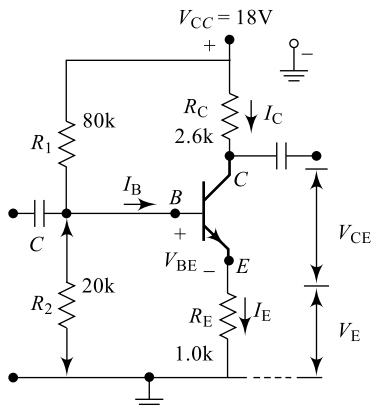


Fig. M3.40

41. In the voltage divider-biasing circuit of Fig. M3.40, for the Thevinised input circuit write the KVL equation.
    (a) $V_{TH} = I_B R_B + V_{BE} + I_E R_E + I_C R_C$ (b) $V_{CC} = I_B R_B + V_{BE} + I_E R_E$
    (c) $V_{CC} = I_B R_B + V_{BE} + I_C R_E$ (d) $V_{TH} = I_B R_B + V_{BE} + I_E R_E$
42. In the voltage divider-biasing circuit of Fig. M3.40, for the output circuit, write the KVL equation.
    (a) $V_{CC} = I_C R_C + V_{CE} + I_E R_E$ (b) $V_{TH} = I_B R_B + V_{BE} + I_E R_E + I_C R_C$
    (c) $V_{CC} = I_B R_B + V_{BE} + I_C R_E$ (d) $V_{TH} = I_B R_B + V_{BE} + I_E R_E$
43. In the voltage divider-biasing circuit of Fig. M3.40, if $\beta = 55$ then the operating point is given by _____.
    (a) Q(3.6 V, 2.32 mA) (b) Q(9.6 V, 3.32 mA)
    (c) Q(9.6 V, 2.32 mA) (d) Q(9.6 V, 3.2 mA)
44. In the voltage divider-biasing circuit of Fig. M3.40, if $\beta = 55$ then the S value is _____.
    (a) 16 (b) 13 (c) 14.22 (d) 13.2
45. In the voltage divider-biasing circuit of Fig. M3.40 if β is doubled then the S value is _____.
    (a) 14.86 (b) 13.2 (c) 1.42 (d) 1.32
46. In the voltage divider-biasing circuit of Fig. M3.40 if β is halved then the S value is _____.
    (a) 14.86 (b) 10.89 (c) 1.42 (d) 1.32
47. For switching application, a transistor is biased to work between _____ and _____ regions.
    (a) saturation, cut-off (b) saturation, active
    (c) active, cut-off (d) none
48. In a transistor switch, the collector current ON period is given by _____.
    (a) $t_{ON} = (t_d + t_f)$ (b) $t_{ON} = (t_f + t_r)$ (c) $t_{ON} = 0$ (d) $t_{ON} = (t_d + t_r)$
49. In a transistor switch, the collector current OFF period is given by _____.
    (a) $t_{OFF} = (t_f + t_S)$ (b) $t_{OFF} = (t_d + t_S)$ (c) $t_{OFF} = 0$ (d) $t_{OFF} = (t_d + t_f)$
50. The rise time t_r is defined as the time taken by the signal to rise from _____ to _____ of its maximum value.
    (a) 10%, 90% (b) 0%, 50% (c) 10%, 20% (d) 40%, 50%

BJT Amplifiers, Feedback and Oscillators

4

Goals and Objectives

Upon completion of this chapter, the reader is expected to

- Recall all the basic concepts of bipolar junction transistors from Chapter 3
- Understand the basic need for BJT biasing and importance of *Q*-point
- Define the terms *amplifier*, *gain* and *decibel* and compute the gain of an amplifier
- Understand the basic principles and need of an amplifier
- Understand the parameters used for various classification of amplifiers
- Understand the applications of audio-frequency amplifiers and radio-frequency amplifiers
- Differentiate between single-stage and multistage amplifiers
- Understand the importance and need of multistage amplifiers
- Calculate the cascaded gain of multistage amplifiers
- Understand amplifier classification based on location of *Q*-point on load line
- Understand different Class-A amplifiers, their performance and efficiency calculations
- Understand Class-B amplifiers operation, their performance and efficiency calculations
- Understand crossover distortion, Class-AB and Class-C amplifiers operation
- Understand the need for complementary-symmetry operation
- Understand the frequency response of an amplifier and significance of 3 dB bandwidth
- Understand different cascading methods available for multistage amplifiers
- Understand advantages and drawbacks of transformer coupling in multistage amplifiers
- Understand advantages and drawbacks of direct coupling in multistage amplifiers
- Understand the need of *RC* coupling in multistage amplifiers
- Understand the frequency response of *RC* coupled amplifiers
- Compare the performance of different coupling methods in multistage amplifiers
- Understand the concept of feedback and its need in amplifiers
- Understand the different feedback methods available and their performance
- Perform the analysis of different feedback methods on amplifier parameters like input impedance, output impedance, voltage gain and current gain
- Understand the advantage of negative feedback on the amplifier performance
- Understand the concept of positive feedback and its use in signal generation
- Understand different methods available for amplifier analysis and particularly importance of *H*-parameters in amplifier analysis
- Understand the concept, components and principle of sinusoidal oscillators
- Arrive at Barkhausen criteria for oscillators
- Understand the classification of oscillators based on various parameters
- Understand the concept, components and principle of low-frequency *RC* oscillators
- Understand the concept, components and principle of high-frequency sinusoidal oscillators
- Understand the concept, need and principle of crystal oscillators
- Feel confident in selecting amplifiers and oscillators for any application

4.1 INTRODUCTION

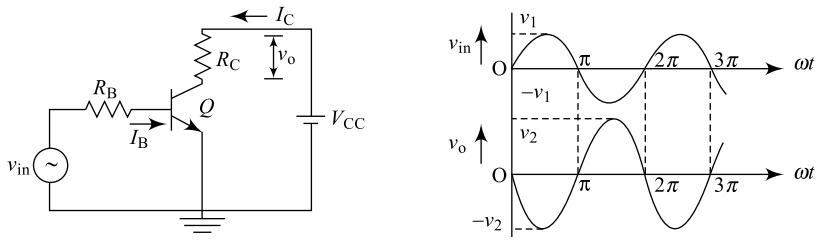
In Chapter 3, one of the most exiting and important devices in electronics, the BJT, was introduced. Unlike the diode, this is a three-terminal device with two junctions. The construction, principles of operation, characteristics and biasing methods are completely presented there. In this chapter, the most important applications of the transistor such as amplifiers and oscillators are presented. Feedback in transistors is also an important concept and is presented in this chapter.

Amplifiers are circuits used to increase the strength of weak signals. **BJT amplifiers** are widely used in the electronic industry and they offer many advantages. In order to achieve required strength for the input signal, many amplifier stages can be connected in series and these multistage amplifiers are very popular.

Feedback is a process to enhance the performance of circuits wherein a part of the output is connected back to the input. This feedback signal may be inphase with the input signal or in phase opposition to the input signal. Based on this, an amplifier can function as an oscillator. An oscillator is a circuit that can generate signals of the desired shape and frequency. Different oscillators are presented and discussed in this chapter.

4.2 AMPLIFIER BASICS

A BJT, when properly biased to fix the operation point on the load line, amplifies the input signal. In order to obtain fair and faithful output, it is necessary to choose the correct components for the amplifier. In Section 3.4 of Chapter 3, transistor amplifier basics are presented; here, the weak input signal is amplified to the required level using a BJT. Figure 4.1 shows a simple basic amplifier; here the transistor is connected in CE configuration. Resistors R_B, R_C along with the supply voltage V_{CC} decide the operating point on the load line. As discussed in Section 3.6 of Chapter 3, the operating point should give faithful amplification. R_B here limits the base drive to the transistor and R_C acts as lead. The weak input signal is transformed into a large amplified signal across R_C as indicated in Fig. 4.1(b). The dc supply V_{CC} maintains a forward bias on the base-emitter junction and reverse bias on the collector-base junction, always irrespective of the polarity of the input signal. Because of the CE configuration, there will be a phase shift of 180° between input and output signals as indicated in Fig. 4.1(b).



(a) Transistor amplifier (b) Input and output waveforms

Fig. 4.1 BJT amplifier

4.3 AMPLIFIER CLASSIFICATION

All amplifiers are basically intended to strengthen the weak signal and parameters such as current or voltage or power may be amplified. Based on various parameters, amplifiers can be classified into several classes.

Table 4.1 Amplifier classification

Sl. No.	Basis of Classification	Types available
1	Type of configuration	(a) CE amplifier (b) CB amplifier (c) CC amplifier
2	Type of signal	(a) Current amplifier (b) Voltage amplifier (c) Power amplifier
3	Frequency range	(a) Audio-Frequency amplifier (AFA) (b) Radio-Frequency amplifier (RFA)
4	Coupling stage	(a) Transformer-coupled amplifier (b) *RC* coupled amplifier (c) Direct coupled amplifier
5	Number of stages	(a) Single-stage amplifier (b) Multistage amplifier
6	Location of *Q*-point on load line	(a) Class-A amplifier (b) Class-B amplifier (c) Class-C amplifier (d) Class-AB amplifier (e) Class-D amplifier

Table 4.1 indicates various classifications for amplifiers.

Based on the frequency of operation, amplifiers can be classified into two major types:

1. Audio-frequency Amplifiers

These are designed to work in the audio-frequency range of 20 Hz to 20 kHz. The audio signals from public-address systems and other sources may be amplified using this class.

2. Radio-frequency Amplifiers

These are designed to work in the high frequency ranges (few 100s MHz) well above the audio range. Applications like radio communication, television system, mobile communications, etc. make use of these amplifiers.

Based on the signal parameter amplified, the amplifiers can be classified into three types:

1. Voltage Amplifiers

These amplifiers are designed to increase the voltage level of the input signal to the required level at the output.

The circuit performance is measured in terms of voltage gain (A_v). The voltage gain is defined as the ratio of output voltage to input voltage (Eq. 4.3)

2. Current Amplifiers

These amplifiers are designed to increase the current level of the input signal to the required level at the output.

The circuit performance is measured in terms of the current gain (A_I). The current gain is defined as the ratio of output current to input current (Eq. 4.3)

3. Power Amplifiers

These amplifiers are designed to increase both the current and the voltage levels (i.e. power level) of the input signal to the required level at the output.

The circuit performance is measured in terms of the power gain (A_p). The power gain defined as the ratio of output power to the input power (Eq. 4.1)

Based on the number of stages connected, amplifiers can be classified into two types:

1. Single-stage Amplifier

Here, only one stage will be connected and the gain obtained is limited. As indicated in Fig. 4.2, v_{in} is the input voltage to the single-stage amplifier and v_o is the output voltage.

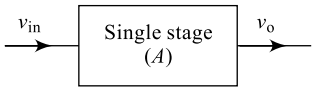


Fig. 4.2 Single-stage amplifier

The stage power gain of the amplifier is given by Eq. (4.1)

$$A_P = \frac{\text{Output power}}{\text{Input power}} \tag{4.1}$$

$$A_P = \frac{P_o}{P_{in}} = \frac{I_o^2 R}{I_{in}^2 R} = \frac{V_o^2/R}{V_{in}^2/R} \tag{4.2}$$

Similarly, the voltage gain and current gains are given by

$$A_V = \frac{V_o}{V_{in}}$$

$$A_L = \frac{I_o}{I_{in}} \tag{4.3}$$

This being a ratio of voltages or currents has no units; however, it is expressed as **'Neper' gain**. But the more conventional way of expressing the gain is in decibels (dB) and is given by Eq. (4.4).

$$\text{Gain in dB} = A_{dB} = 10 \log\left(\frac{P_o}{P_{in}}\right) \tag{4.4}$$

For ratio of currents, $A_I = 10 \log\left[\frac{I_o^2}{I_{in}^2}\right] \text{dB}$ (4.5a)

$$A_P = 20 \log\left[\frac{I_o}{I_{in}}\right] \text{dB}.$$

Similarly, for ratio of voltages, the gain is

$$A_V = 10 \log\left[\frac{V_o^2/R}{V_{in}^2/R}\right] \text{dB}$$

$$= 20 \log\left[\frac{V_o}{V_{in}}\right] \tag{4.5b}$$

Equations (4.3), (4.4) and (4.5) are all very popularly used during amplifier designs.

2. Multistage Amplifier

Here, a number of stages are cascaded (connected in series) together to obtain the required gain. Output of Stage-1 is connected as input to Stage-2, output of Stage-2 is connected as input to Stage-3,

and so on as shown in Fig. 4.3. Cascading of stages increases the overall gain of the multistage amplifier and the number of stages depends on the overall gain 'A' required. If $A_1, A_2, \ldots A_N$ are the individual stage gains then the overall gain of the multistage amplifier is given by Eq. (4.6). It is important to notice here that individual stage gains are in 'Nepers'.

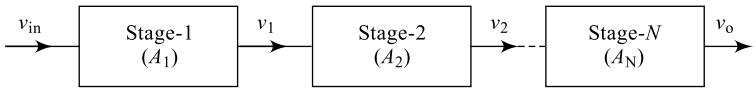


Fig. 4.3 Multistage amplifier

$$A = A_1 \times A_2 \times \cdots \times A_N \tag{4.6}$$

$$A = \frac{v_i}{v_{in}} \times \frac{v_2}{v_1} \times \cdots \times \frac{v_o}{v_{N-1}} \tag{4.7}$$

$$A = \frac{v_o}{v_{in}} \tag{4.8}$$

If it is required to express the overall gain in dB, then Eq. (4.7) can be re-written as in Eq. (4.9)

$$\begin{aligned} A_{dB} &= 20 \log \left[\frac{v_1}{v_{in}} \times \frac{v_2}{v_1} \times \cdots \times \frac{v_o}{v_{N-1}} \right] \\ &= 20 \left[\log\left(\frac{v_1}{v_{in}}\right) + \log\left(\frac{v_2}{v_1}\right) + \cdots + \log\left(\frac{v_o}{v_{N-1}}\right) \right] \\ &= 20 \log\left(\frac{v_1}{v_{in}}\right) + 20 \log\left(\frac{v_2}{v_1}\right) + \cdots + 20 \log\left(\frac{v_o}{v_{N-1}}\right) \end{aligned} \tag{4.9}$$

$$A_{dB} = (A_{1dB} + A_{2dB} + \cdots + A_{NdB})\,dB \tag{4.10}$$

Hence, it is clear from Eq. (4.10) that if individual stage gains are in dBs then the overall gain is obtained by adding each stage gain as indicated in Table 4.2.

Table 4.2 Amplifier basics

Sl. No.	Parameter	Expression
1	Current gain	$A_I = \frac{I_o}{I_{in}} = 20 \log \frac{I_o}{I_{in}} dB$
2	Voltage gain	$A_V = \frac{V_o}{V_{in}} = 20 \log \frac{V_o}{V_{in}} dB$
3	Power gain	$A_P = \frac{P_o}{P_{in}} = 10 \log \frac{P_o}{P_{in}} dB$
4	Two-stage gain	$A_P = A_1 \times A_2 = (A_{1dB} + A_{2dB})\,dB$

Example 4.1

A single-stage CE amplifier capable of doubling the input signal is supplied with an input of 2 sin t (ωt). Plot its output signal with respect to input signal.

Solution Referring to Fig. 4.1(b), there will be a phase shift of 180° between input and output signals. Also, the amplifier offers a gain of 2 and hence, the resulting waveform is shown in Fig. 4.4.

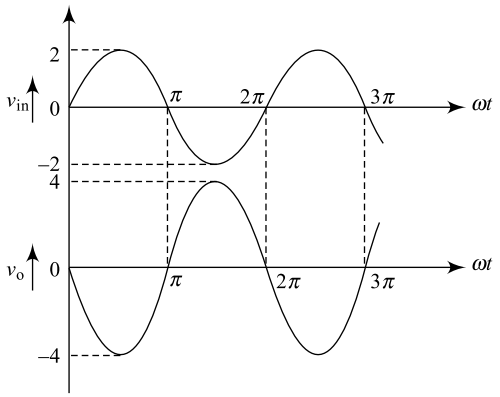


Fig. 4.4 Amplifier input-output waveforms

Example 4.2

A single-stage amplifier with an input of 250 mV produces an output of 1.5 V. What is the gain?

Solution Given $v_{in} = 250$ mV and $v_o = 1.5$ V
From Eq. 4.2(a), the voltage gain is

$$A_v = \frac{v_o}{v_{in}}$$

$$= \frac{1.5}{250 \times 10^{-3}} = 6$$

Example 4.3

A single-stage amplifier offering a stage gain of 7.5 dB produces an output of 0.5 V. What is the input voltage needed?

Solution Given $A_V = 7.5$ dB and $v_o = 500$ mV

From Eq. (4.5) $A_V = 20 \log \left(\frac{v_o}{v_{in}} \right)$ dB

i.e. $$7.5 = 20 \log \left[\frac{v_o}{v_{in}} \right]$$

i.e. $$\log \left(\frac{v_o}{v_{in}} \right) = \frac{7.5}{20} = 0.375$$

Taking antilog on both sides, we get

$$\left(\frac{v_o}{v_{in}}\right) = 2.3714$$

$$v_{in} = \frac{v_o}{2.3714} = \frac{500 \times 10^{-3}}{2.3714}$$

i.e. $$\boxed{v_{in} = 210.85 \text{ mV}}$$

Example 4.4

What is the dB gain of Example 4.2? If the output is increased by three fold, what is the gain?

Solution From Example 4.2 gain is 6 and its dB gain is

$$A_{dB} = 20 \log (6)$$

$$\boxed{A_{dB} = 15.563 \text{ dB}}$$

Output is increased by threefold; i.e. $v_o = 6$ V and then the gain is

$$A_{dB} = 20 \log \left(\frac{v_o}{v_{in}}\right)$$

$$= 20 \log \left(\frac{6.0}{250 \times 10^{-3}}\right)$$

$$\boxed{A_{dB} = 29.328 \text{ dB}}$$

Example 4.5

A two-stage amplifier has individual stage gains of 5 and 7.5. Find the overall gain.

Solution Given Stage-1 gain $A_1 = 5$

Stage-2 gain $A_2 = 7.5$

From Eq. (4.6), we have

$$A = A_1 \times A_2$$

i.e. $$A = 5 \times 7.5$$

$$\boxed{A = 37.5}$$

Example 4.6

A two-stage amplifier has individual stage gains of 10 dB and 10. What is the overall gain?

Solution Given Stage-1 gain $A_1 = 10$ dB

$$10 = 20 \log \left(\frac{V_1}{V_{in}}\right)$$

i.e. $$\log \left(\frac{V_1}{V_{in}}\right) = 0.5$$

Taking antilog on both sides, we get

i.e. $$A_1 = \frac{v_1}{v_{in}} = 3.1623$$

Stage-2 gain $A_2 = 10$

Overall gain as given by Eq. (4.6)

$$A = A_1 \times A_2$$
$$= 3.1623 \times 10$$
$$\boxed{A = 31.623}$$

Example 4.7

What is the dB gain of individual stages in Example 4.5?

Solution Given Stage-1 gain

$$A_1 = 5$$

i.e. $$A_{1dB} = 20 \log (5)$$

$$\boxed{A_{1\,dB} = 13.98\ dB}$$

Stage-2 gain

$$A_2 = 7.5$$

i.e. $$A_{2dB} = 20 \log(7.5)$$

$$\boxed{A_{2\,dB} = 17.5\ dB}$$

NOTE: Overall gain

$$A_{dB} = A_{1dB} + A_{2dB}$$
$$= (13.98 + 17.5)\ dB$$

$$\boxed{A = 31.5\ dB}$$

Example 4.8

Calculate the dB gain of stage-2 and overall dB gain in Example 4.6.

Solution Given Stage-2 gain

$$A_2 = 10$$
$$A_{2dB} = 20 \log(10)$$
$$= 20\ dB$$

Overall gain in dB is

$$A_{dB} = A_{1dB} + A_{2dB}$$
$$= (10 + 20) = 30\ dB$$

$$\boxed{A_{dB} = 30\ dB}$$

Example 4.9

It is required to increase the gain of the multistage amplifier in Example 4.6 to 95. Suggest a third stage for the purpose and calculate its dB gain.

Solution Resulting 3-stage amplifier is shown in Fig. 4.5.

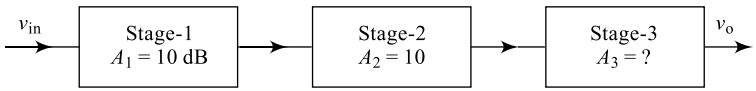


Fig. 4.5 A 3-stage amplifier

Given Stage-1 gain $A_{1dB} = 10$ dB

i.e. $A_1 = 3.1623$

Stage-2 gain $A_2 = 10$

Overall gain of Fig. 4.5 is

$$A = A_1 \times A_2 \times A_3$$

i.e. $$95 = 3.1623 \times 10 \times A_3$$

$$\boxed{A_3 = 3.004}$$

$$A_{3dB} = 20 \log(3.004)$$

$$\boxed{A_{3dB} = 9.554}\ \text{dB}$$

A third stage with a gain of 9.554 dB cascaded to the amplifier in Example 4.6 results in an overall gain of 95 (or 39.554 dB)

Example 4.10

A cascaded 3-stage amplifier has an output voltage 8 mV. Calculate the input voltage needed to obtain an overall gain of 8000 for the cascaded amplifier.

Solution Given overall gain = 8000 and output $V_o = 8$ mV.
Overall gain of the amplifier is given by Eq. (4.8)

$$A = \frac{v_o}{v_{in}}$$

i.e. $$8000 = \frac{8\ \text{mV}}{v_{in}}$$

$$\boxed{v_{in} = 1\ \mu\text{V}}$$

Example 4.11

In Example 4.10, the first two stages are identical and the last stage offers a gain of 2. Calculate the gain in dB for the first two stages.

Solution Gain of stage-3 is $A_3 = 2$

i.e. *i/p* to stage-3 is $V_{in\,3} = \frac{v_o}{A_3}$

$$V_{in\,3} = \frac{8\ \text{mV}}{2} = 4\ \text{mV}.$$

$V_{in\,3}$ is the output of stage-2; the combined gain of stage-1 and stage-2 is, therefore,

$$A' = A_1 \times A_2 = \frac{V_{in\,3}}{V_{in}}$$

$$= \frac{4\text{ mV}}{1\text{ mV}} = 4000$$

i.e. $$A' = (20 \log 4000)\text{ dB} = 72.041\text{ dB}.$$

Since stage-1 and stage-2 are identical, the gain in dB for each of them is

$$A_{dB} = A_{1dB} = A_{2dB}$$

$$= \frac{72.041}{2} = 36.02\text{ dB}$$

Based on the location of Q-point on the transistor load line, amplifiers can be classified into the following four types and are generally called **power amplifiers**.

As discussed in Chapter 3 (Table 3) a **CB (Common Base) amplifier** is characterised by very small current gain ($\propto \leq 1$) and moderate voltage gain; hence, its power gain is less. A **CC (Common Collector) amplifier** is characterised by very high current ($\gamma = \beta + 1$) and unity voltage gain ($A_V \leq 1$); thus, it has small power gain. However, a **CE (Common Emitter) amplifier** has reasonably good A_V and A_I and hence, is suitable for "power amplifiers".

Based on the location of operating point on the load line, these power amplifiers can be classified into the following categories:

(i) Class-A power amplifier
(ii) Class-B power amplifier
(iii) Class-C power amplifier
(iv) Class-AB power amplifier.

In Fig. 4.6, a single-stage common emitter BJT amplifier is shown. Resistors R_1, R_2, R_C, R_E, capacitors C_C, C_E along with supply voltage V_{CC} decide the dc operating conditions for the amplifier.

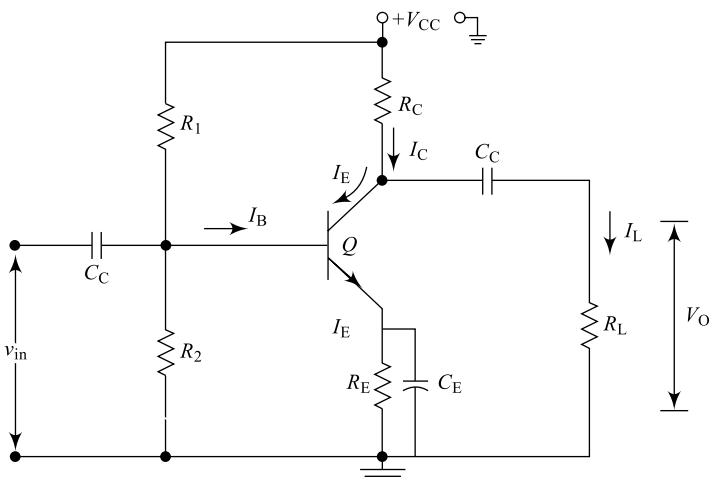


Fig. 4.6 Single-stage BJT amplifier

Selection of proper R_1, R_2, R_C, R_E and V_{CC} along with β for transistor results in a Q-point which allows the collector current I_C to flow for a desired time w.r.t *i/p*. The collector current may flow for the entire *i/p* cycle may flow for only half the *i/p* cycle, etc. Accordingly, the classifications are mentioned above.

1. Class-A Power Amplifier

A Class-A power amplifier is one in which the operating point on the load line is so located that the collector current flows for the entire *i/p* cycle, i.e. for 360°.

As indicated in Fig. 4.7, the Q-point is located midway on the load line and results in a collector current that flows for the entire input period.

For Class-A operation, the Q-point is located exactly midway on the dc load line. As indicated graphically, the collector current and, hence, the *o/p* voltage exist for the entire 360°.

There are two types of Class-A amplifiers depending on the way the *o/p* is fed to the load or coupled to the load: series-fed Class-A amplifier and transformer-coupled Class-A amplifier.

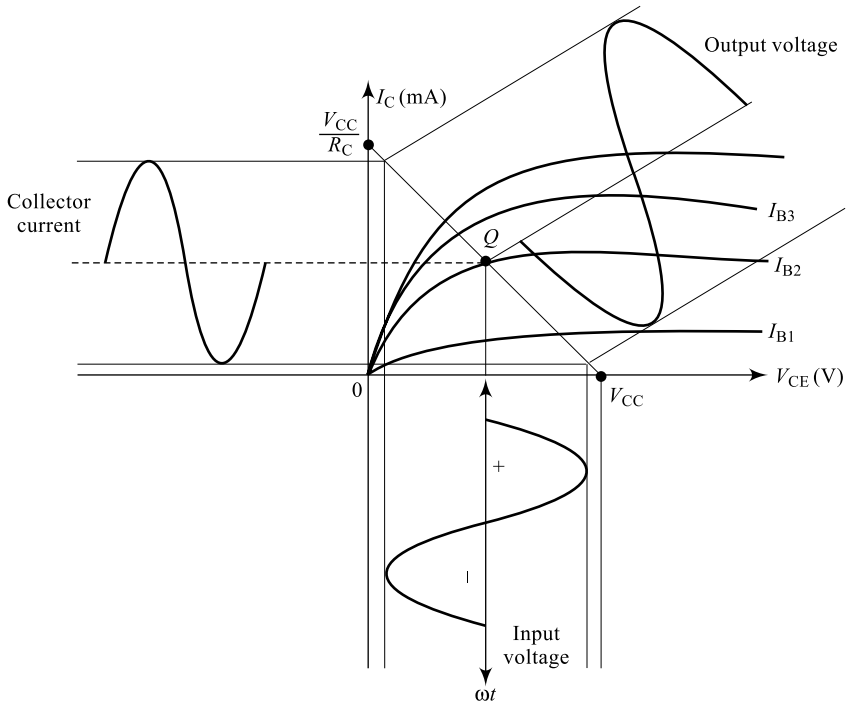


Fig. 4.7 Amplifier load line and *Q*-point.

(a) Series-fed Class-A Power Amplifier Generally, a Class-A amplifier uses more dc power to maintain the Q-point at midway on the load line. Thus, the efficiency of a Class-A power amplifier is low. The power handled by this circuit is usually high and the transistor used (power transistor) will have beta less than 100.

The diagram of a series-fed Class-A amplifier is as shown in Fig. 4.8; here, R_1, R_2, R_C, R_E and V_{CC} form the biasing circuit. The operating point is located midway on the load line and graphical analysis of *i/p* and *o/p* signals is as shown in Fig. 4.7. The operating conditions for this amplifier can be estimated through the following analysis.

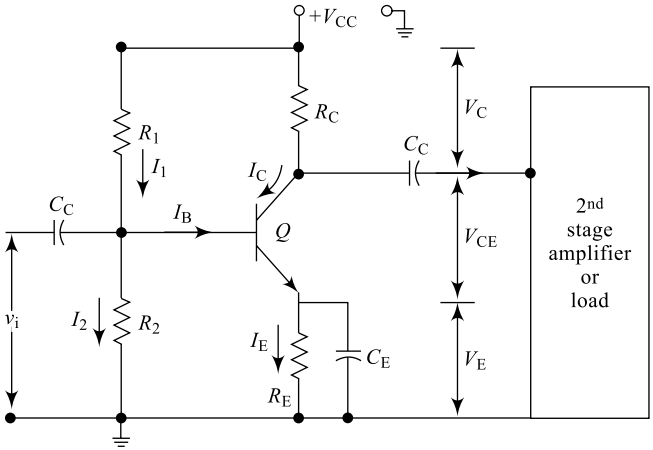


Fig. 4.8 Series-fed Class-A amplifier

dc bias Applying KVL to the output loop, we can write

$$V_{CE} = V_{CC} - I_C R_C - V_E; \tag{4.11}$$

Here, drop across R_E is V_E given by

$$V_E = (I_B + I_C)R_C \tag{4.12}$$

Neglecting the saturation currents, we can write

$$I_C = \beta I_B \tag{4.13}$$

Generally, base current I_B is only a small percentage of current R_1 and is given by

$$I_B = 0.1 I_1 \tag{4.14}$$

$$= 0.1 \times \left(\frac{V_{CC} - V_B}{R_1} \right); \tag{4.15}$$

where

$$V_B = V_{BE} + V_E \tag{4.16}$$

Normally, $I_1 \simeq I_2$ so that effect of β changes on I_C are minimised.

i.e.

$$I_2 = 0.9 I_1 \tag{4.17}$$

So, I_B the base current, is almost negligible.

(b) Transformer-coupled Class-A Power Amplifier If *o/p* of the amplifier is directly (series) fed to R_L as indicated in Fig. 4.8, the quiscent current passes through this resistor and hence *o/p* efficiency reduces. Hence, a transformer coupling can be used as shown in Fig. 4.9. Use of a transformer for coupling *o/p* to load, increases efficiency, (reduces waste of power), provides proper impedance matching. Hence, performance improves as compared to that of circuit in Fig. 4.8. The resulting load line for class-A amplifier is shown in Fig. 4.10.

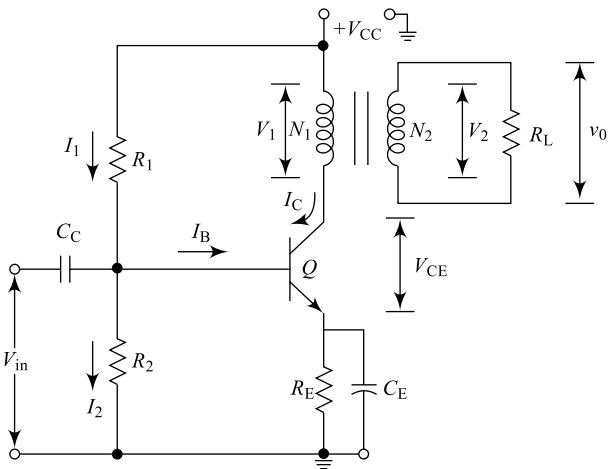


Fig. 4.9 Transformer coupled Class-A amplifier

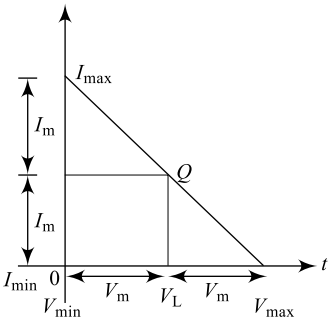


Fig. 4.10 Class-A amplifier load line

V_1 = Primary voltage of transformer

V_2 = Secondary voltage of transformer

N_1 = Number of primary turns in the transformer

N_2 = Number of secondary turns in the transformer

I_1 = Primary current

and I_2 = Secondary current

From the basics of transformer, one can write

$$\frac{V_1}{V_2} = \frac{N_1}{N_2} = \frac{I_2}{I_1} \tag{4.18}$$

i.e. $$V_1 = \frac{N_1}{N_2} V_2 \quad \text{and} \quad I_1 = \frac{N_2}{N_1} i_2$$

If $\frac{N_2}{N_1} = n$, then

$$\frac{V_1}{V_2} = n = \frac{I_1}{I_2}$$

i.e. $$\frac{V_1}{I_1} = \frac{1}{n^2} \frac{V_2}{I_2} \tag{4.19}$$

$$\frac{V_1}{I_1} \rightarrow \text{Effective } i/p \text{ impedance } R_L'$$

$$\frac{V_2}{I_2} \rightarrow o/p \text{ impedance } R_L$$

$\therefore$ $$\boxed{R_L' = \frac{1}{n^2} \cdot R_L} \tag{4.20}$$

Efficiency The ability of an amplifier to convert the dc power from supply into ac power delivered to the load is called **conversion efficiency** or **theoretical efficiency** or **collector-circuit efficiency** or **figure of merit**. η for the amplifier.

$$\eta = \frac{\text{ac power delivered to load}}{\text{dc power supplied to circuit}} \times 100\% \tag{4.21}$$

$$\eta = \frac{P_{ac}}{V_{CC}\,(I_C + B_o)} \times 100\% \qquad \text{(Neglecting the higher order distortion)}$$

$$\eta = \frac{B_1^2\, R_L'/2}{V_{CC}\,(I_C + B_o)} \times 100\%$$

Neglecting all distortion components, we get

$$\eta = \frac{1/2 \cdot V_m\, I_m}{V_{CC}\, I_C} \times 100\%$$

Here, $I_m = I_C$ and $= V_m = \dfrac{V_{max} - V_{min}}{2}$

$\therefore$ $$\eta = \frac{\frac{1}{2} \cdot \left(\frac{V_{max} - V_{min}}{2}\right) \cdot I_s}{V_{CC} \times V_i} \times 100\%$$

$$= 25 \cdot \frac{V_{max} - V_{min}}{V_{CC}}\% = 25 \qquad \frac{V_{max} - V_{min}}{V_{max}}; \because V_{max} = V_{CC}$$

$$\eta = 25 \cdot \frac{V_{max} - V_{min}}{V_{max}}\% \tag{4.22}$$

For a series-fed Class-A power amplifier, maximum conversion efficiency is therefore given by

$$\eta_{max} = 25\% \tag{4.22}$$

However, if transformer coupling is used then this efficiency can be doubled. For a transformer-coupled power amplifier efficiency 'η' can be estimated as given below. Here, collector circuit resistance is almost zero and hence

$$V_{CC} = V_C = \frac{V_{max} + V_{min}}{2} \tag{4.23}$$

$\therefore$ $$\eta = 25 \cdot \frac{V_{max} - V_{min}}{\frac{V_{max} + V_{min}}{2}}\%$$

$$\boxed{\eta_{max} = 50 \cdot \frac{V_{max} - V_{min}}{V_{max} + V_{min}}\%} \tag{4.24}$$

This clearly indicates the maximum efficiency of a transformer-coupled Class-A amplifier is 50%.

2. Class-B Power Amplifier

Here, in a Class-B operation, the *Q*-point is so located that the collector current flows only for 180° (half-cycle of *i/p*) as indicated in Fig. 4.11. In order to achieve this, push-pull operation may be used. In a push-pull amplifier, both the transistors work in Class-B mode. Each transistor conducts for only 180°, resulting in a full cycle *o/p*. However, at the end of one half cycle of *i/p*, conduction switches from one transistor to another. The time-log in a transition of switching from Q_1 to Q_2 or Q_2 to Q_1 results in a distortion of major concern called **crossover distortion**, which is as indicated in Fig. 4.12.

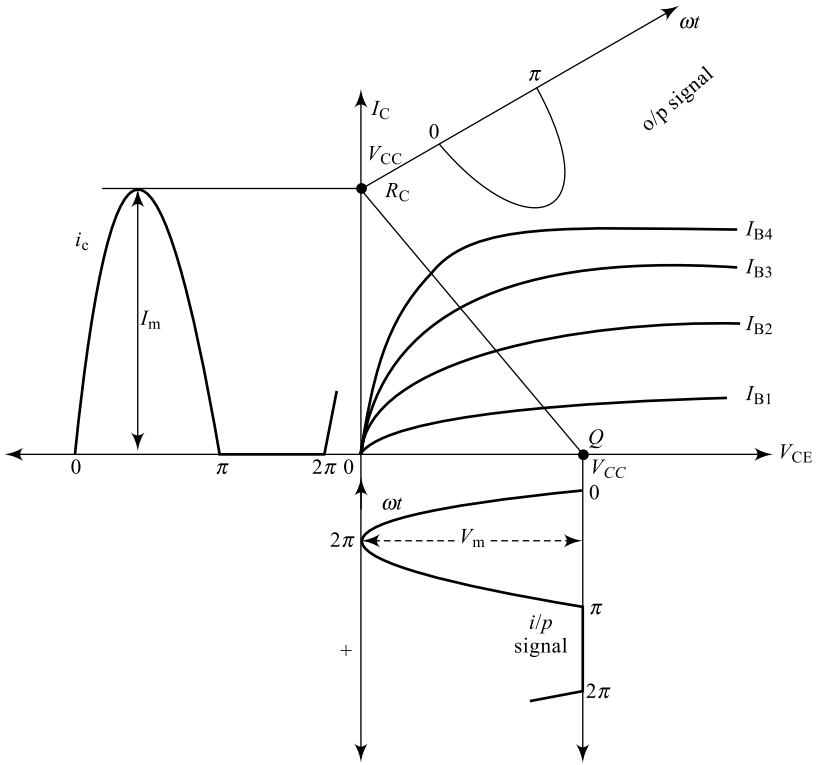


Fig. 4.11 Class-B amplifier load line

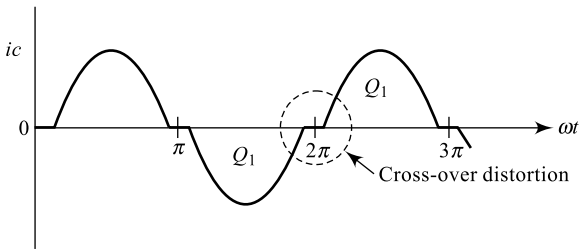


Fig. 4.12 Crossover distortion in Class-B amplifiers

This crossover distortion can be eliminated by using Class-*AB* operation.

Efficiency The conversion efficiency of a power amplifier is in general given by

$$\eta = \frac{\text{ac power delivered to load}}{\text{dc power drawn from supply}} \times 100\%$$

$$P_{dc} = V_{CC} \cdot I_{dc}/\text{transistor} \tag{4.25}$$

where $I_{dc} = I_{m/k}$ which is the average value of half-sine loop.

$$\therefore \quad P_{dc} = 2 \cdot V_{CC} \cdot \frac{I_m}{\pi} \tag{4.26}$$

2 for both Q_1 and Q_2

o/p power delivered to load is given by

$$P_{ac} = \frac{I_m \cdot V_m}{2} \tag{4.27}$$

$$= \frac{I_m}{2}(V_{CC} - V_{min})$$

$$\therefore \quad \eta = \frac{I_{m/2}\,(V_{CC} - V_{min})}{2\,V_{CC} \cdot \dfrac{I_m}{\pi}} \times 100\% \tag{4.28}$$

$$= \frac{\pi}{4}\left(\frac{V_{CC} - V_{min}}{V_{CC}}\right) \times 100\%$$

$$= \frac{\pi}{4}\left(1 - \frac{V_{min}}{V_{CC}}\right) \times 100\% \tag{4.29}$$

$$\therefore \quad \boxed{\eta_{max} = 78.5\%}$$

efficiency close to 78.5% can be achieved.

Push-Pull Amplifiers The effect of distortion produced by the non-linearity of the device can be eliminated by push-pull operation. Here, the two transistors Q_1 and Q_2 are driven by two out-of-phase signals i_{b_1} and $-i_{b_1}$, (i_{b_2}). A push-pull operation reduces distortion in the output and improves the efficiency of the amplifier. A push-pull amplifier arrangement is shown in Fig. 4.13.

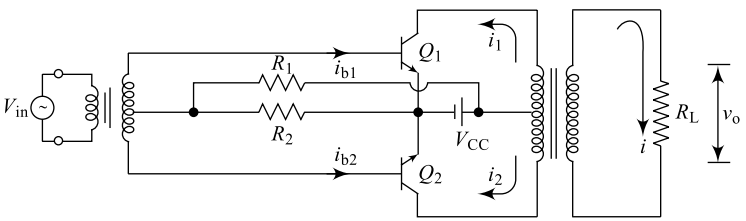


Fig. 4.13 Class-B push-pull amplifier

If $i_{b_1} = I_{b_m} \cos \omega t$, (4.30)

then $i_{b_2} = -i_{b_1} = I_{b_m} \cos(\omega t + \pi)$. (4.31)

The respective *o/p* currents are given by

$$i_1 = I_C + B_0 + B_1 \cos \omega t + B_2 \cos 2\,\omega t + B_3 \cos 3\omega t + \ldots \tag{4.32}$$

$$i_2 = I_C + B_0 - B_1 \cos \omega t + B_2 \cos 2\,\omega t - B_3 \cos 3\omega t + \ldots \tag{4.33}$$

As indicated in the circuit, i_1 and i_2 are in opposite direction. Hence, the resulting output current i is given by

$$i = kC(i_1 - i_2); \text{ where } k \text{ is a constant} \tag{4.34}$$

$$= k[(I_C + B_0 + B_1 \cos \omega t + \ldots) - (I_C + B_0 - B_1 \cos \omega t + \ldots)]$$

$$= 2k(B_1 \cos \omega t + B_3 \cos 3\omega t + B_5 \cos 5\omega t + \ldots) \tag{4.35}$$

$$\boxed{i = 2\,k\,(B_1 \cos \omega t + B_2 \cos 3\,\omega t + \ldots)} \tag{4.36}$$

This expression clearly indicates that a push-pull operation eliminates all even harmonics in the *o/p* and leaves third harmonic as the principal source of distortion. It is also evident that the two transistors work in Class-B mode.

3. Class-C Power Amplifier

A Class-C operation is one in which the *Q*-point is so located that the *o/p* current I_C flows for less than 180° in the form of pulses.

4. Class-AB power Amplifier

In a class-AB operation, the *Q*-point is so located that the *o/p* current flows for more than 180° (half-cycle) but less than 360° (full cycle); this is indicated in Fig. 4.14.

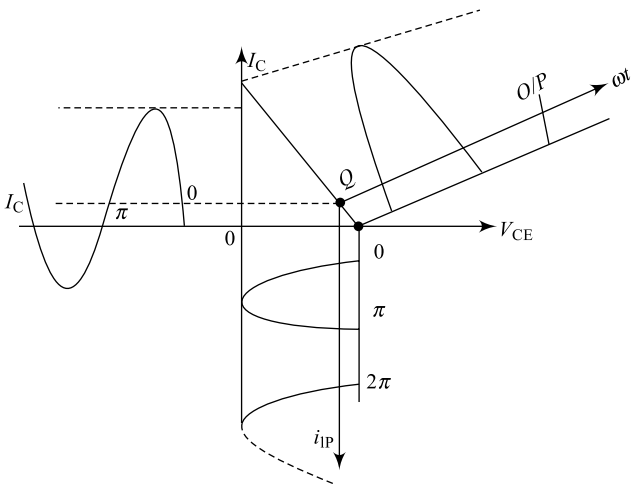


Fig. 4.14 Class-AB amplifier load line

Complementary-Symmetry Amplifier Use of complementary symmetry push-pull transistors eliminates the need for *i/p* and *o/p* transformers as indicated in Fig. 4.15. The resistor '*R*' results in Class-AB operation. Class-AB operation minimises crossover distortion.

The efficiency of Class-AB amplifier is more than 50% but less than 78.5%. If the conduction period of transistors is close to 180°, efficiency of the amplifier will be close to 78.5%.

The efficiency of a Class-C amplifier is greater than 78.5%. If the conduction period is too less, the efficiency will be close to 100% (η of the order of 90%).

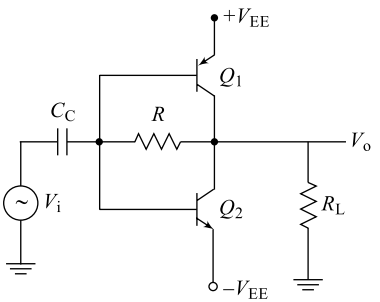


Fig. 4.15 Complementary-symmetry amplifier

4.4 AMPLIFIER FREQUENCY RESPONSE

As presented in Section 4.3, gain of an amplifier is the ratio of output to input. This gain varies if there is change in input signal frequency. In order to study the change of amplifier gain with respect to input signal frequency, a plot of gain as a function of frequency is plotted and is known as the frequency response of the amplifier. As indicated in Fig. 4.16, at low frequencies, gain of the amplifier is low and it increases with increase in the frequency. This lower gain is because of the coupling elements like capacitors C_{CC} in amplifier circuits like Fig. 4.6. The reactance offered by these capacitors at low frequencies will be very high, and hence the amplifier gain reduce in the low-frequency range as indicated in Fig. 4.16. However, increasing frequency reduces this reactance and the amplifier gain goes on increasing till input frequency reaches f_L, the lower cut-off. In the 'mid-frequency range', from 'f_L' to 'f_H' the higher cut-off, the gain becomes independent of reactance, will be constant and is maximum at 'A_{max}'. For frequencies beyond 'f_H', the effect of inter-electrode capacitances (between the terminals of the BJT) comes into picture and again the amplifier gain starts decreasing. The range of frequencies beyond 'f_H' is called **higher frequency range**. Depending on the response of the human ear, a range of frequencies between f_1 and f_2 is selected for amplifier designs and is called bandwidth of the amplifier. These frequencies f_1 and f_2 are selected at a gain which is 0.707 A_{max} or $A_{max}\left|A_{max}\right|\sqrt{2}$ or 3 dB down the maximum gain and are called **half-power frequencies** or 3 dB frequencies.

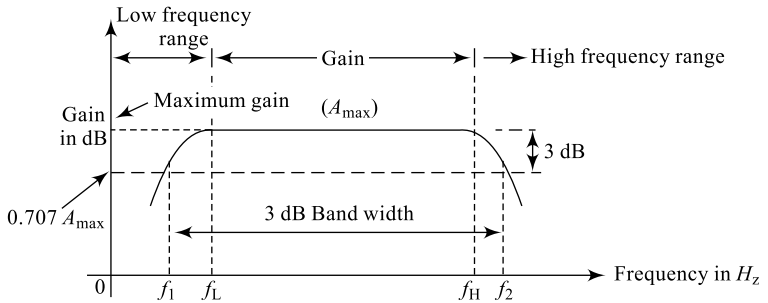


Fig. 4.16 Amplifier frequency response

$$\text{Bandwidth} = (f_2 - f_1)\ \text{Hz} \tag{4.37}$$

Using the bandwidth and the maximum gain of the amplifier, a **figure of merit** called **Gaint Bandwidth Product** (GBW) for any amplifier is defined. This figure of merit is one of the important measuring parameters for an amplifier.

4.5 MULTISTAGE AMPLIFIERS AND COUPLING

As already discussed in Section 4.3, multistage amplifiers are cascading of two or more transistor amplifiers through coupling. As indicated in Fig. 4.17 two different stages are cascaded through a coupling arrangement and there are three popular coupling methods available. They are *RC* coupling, transformer coupling and direct coupling. **RC coupling** and *RC* coupled amplifiers are dealt in Section 4.6 to follow, while transformer coupling and direct coupling are briefly discussed here.

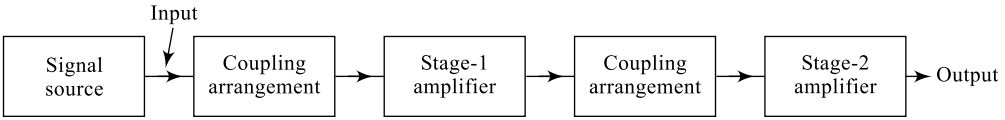


Fig. 4.17 Multistage amplifier and coupling

A **transformer-coupled amplifier** was introduced in Section 4.3 along with some of its advantages, Further, for demonstration, a two-stage transformer-coupled amplifier is shown in Fig. 4.18. It is clear from the figure that the collector circuit is connected with a transformer and use of this transformer offers a variety of advantages. Components R_1, R_2, R_E, C_C and C_E along with V_{CC}, fix/up the dc conditions (Q-point) for the circuit. Output of stage one is coupled to input of stage two; similarly, the output of stage two is connected to the load using the transformers and hence, the name transformer-coupled amplifier. As indicated in Fig. 4.18(b), the frequency response of the amplifier reflects the effect of using a transformer in the collector circuit. At low frequencies (up to f_1), the gain of the amplifier is low due to C_C and slowly increases with frequency. After the lower cut-off frequency f_1, the gain becomes independent of reactances over a range of frequencies and is constant. But, later the transformer coil, along with a virtual capacitance 'C' across the transformer secondary forms a resonant circuit and hence, gain peak resulting in a hump or kink in the response.

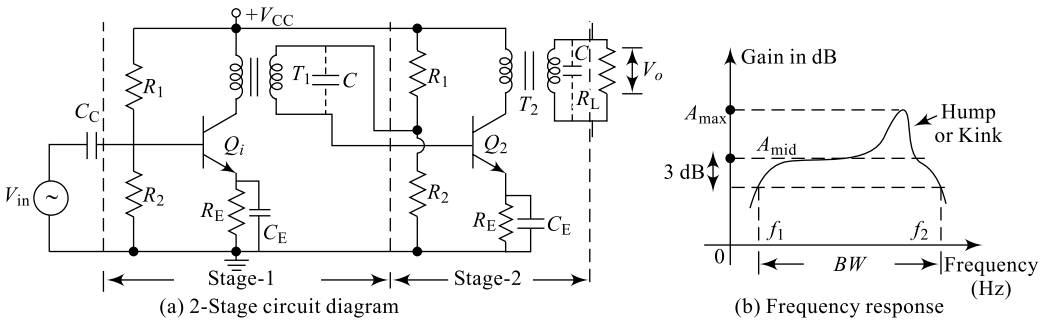


Fig. 4.18 Transformer-coupled amplifier

Then, at high frequencies, gain decreases due to the inter-electrode capacitances of the device. The bandwidth of the circuit is the range of frequencies between f_2 and f_1.

A transformer-coupled amplifier has reasonably fair frequency response, but due to the hump in the response, it is suitable for middle stages of any multistage amplifier. A transformer in the collector circuit reduces loss of power and increases the circuit efficiency. Also, use of a transformer helps in better impedance matching between stages, by adjusting the turns ratio. This feature makes a transformer-coupled amplifier best suited for final stages of amplification.

A **direct-coupled amplifier,** on the other hand, uses no coupling elements and the output of one stage is directly coupled to the input of the next stage, hence the name direct-coupled amplifier. A two-stage direct-coupled amplifier and its frequency response are shown in Fig. 4.19. It can be observed here that the two stages are cascaded together without any elements (like transformer in TC amplifier and resistor (R) capacitor (C) in an RC coupled amplifier). Due to this, there are some advantages: (i) Performance of the amplifier will not deteriorate as it happens in an RC coupled amplifier due to ageing of components. (ii) At low frequency ranges, gain reduction will not happen, because there is no coupling capacitor. (iii) Bandwidth and Gain Band Width (GBW) product will improve. However,

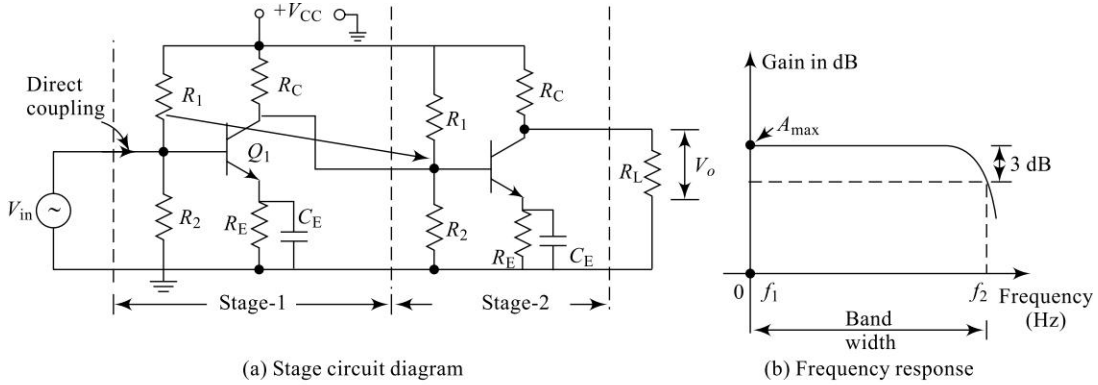


Fig. 4.19 Direct-coupled amplifier

a direct coupled amplifier suffers from a major problem that there will be a drift in the operating point and the stability of the amplifier is affected. This is because there is no 'C_C' to block dc components from one stage to another.

The *RC* coupled amplifier is another popular multistage amplifier in use and is presented in Section 4.6.

4.6 RC COUPLED AMPLIFIER

As discussed in Section 4.5, both transformer-coupled amplifiers and direct-coupled amplifiers offer some advantages, but together they bring strong disadvantages. Poor frequency response of a transformer-coupled amplifier and *Q*-point drift of a direct-coupled amplifier make them unsuitable for initial stages of a multistage amplifier in any public-address system. The *RC* coupled amplifier answers these problems and hence, is popular in all public-address systems. The circuit diagram and the frequency response of a two-stage *RC* coupled amplifier is shown in Fig. 4.20. Components R_1, R_2, R_E, R_C, C_E and C_C, along with supply voltage V_{CC} help fixing the *Q*-point and proper operating dc conditions for the circuit. Potential divider biasing is used, because it offers a good number of advantages (discussed in Chapter 3). The circuit offers good *Q*-point stability against all variations including "β" of the transistor. As explained in Section 4.4, at low frequencies gain is less because of C_C, at high frequen-

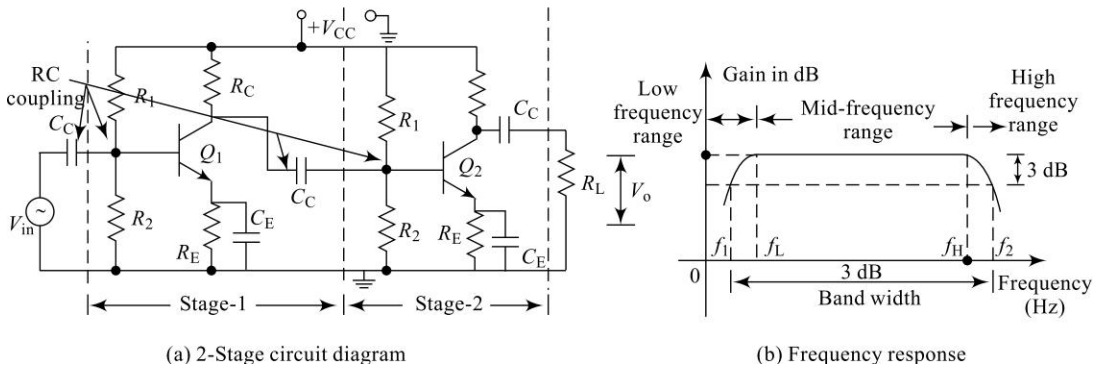


Fig. 4.20 *RC* coupled amplifier

cies gain again reduces because of device inter-electrode capacitances and in the mid-frequency range, gain is constant. The current gain at low frequency ranges is given by Eq. (4.38)

$$A_{IL} = \frac{A_{Im}}{1 - j\dfrac{fc_1}{f}} \tag{4.38}$$

Similarly, the current gain of the high-frequency range is given by Eq. (4.39)

$$A_{IH} = \frac{A_{Im}}{1 - j\dfrac{f}{fc_2}} \tag{4.39}$$

Current gain in the mid-frequency range is given by Eq. (4.40)

$$A_{in} = -h_{fe}\frac{R_o'}{R_o' + R_i'} \tag{4.40}$$

It is evident from Eq. (4.40) that in the mid-band range, gain of the amplifier is independent of any frequency terms and hence is constant. Also, Eq. (4.38) and Eq. (4.39) indicate that gain in the low- and high-frequency ranges is dependent in the operating frequency f and is hence varying.

The value of frequency 'f_L' at which gain becomes almost (independent of reactances) constant can be obtained using the equivalent circuit in Fig. 4.21 and is given by Eq. (4.41)

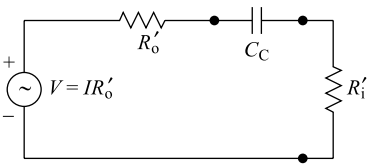


Fig. 4.21 Low-frequency input equivalent circuit

$$f_L = \frac{1}{2\pi(R_o' + R_i')C_C} \tag{4.41}$$

Here,

$$R_o' = (R_c \| R_o) \tag{4.42}$$

$$R_i' = (R_b \| R_i) \tag{4.43}$$

$$R_b = R_1 \| R_2 \tag{4.44a}$$

R_o is the output impedance of amplifier and R_i is the input impedance of the amplifier. Similarly, the voltage gain of a single stage amplifier is given by

$$A_v = \beta \times \frac{R_c}{R_i} \tag{4.44b}$$

Example 4.12

A two-stage *RC* coupled amplifier uses a collector resistors of 1 kΩ, R_1 = 20 kΩ, R_2 = 80 kΩ and transistors with R_i = 1 kΩ and R_o = 40 *k*. Find the value of the coupling capacitor such that it has low 3 dB frequency of 50 Hz.

Solution We have from Eq. (4.41),

$$f_L = \frac{1}{2\pi(R_o' + R_i')C_C}$$

From Eq. (4.42), $R_o' = (R_C \| R_o)$

$= (1\ k \| 40\ k) \simeq 1$ kΩ

From Eq. (4.43), $R_i' = (R_b \| R_i)$

$= [(R_1 \| R_2) \| R_i] = [(20k \| 80k) \| 1\ k]$

$= 1$ kΩ

Now $$f_L = \frac{1}{2\pi[1k + 1k]C_C} = 50$$

i.e. $$C_C = \frac{1}{2\pi(2k)(50)} = 1.591\,\mu F$$

From Fig. 4.20(b) the following points may be noted

(i) The frequency response may be divided into three regions the low-frequency region (0 to f_L), the mid-frequency region (f_L to f_H) and the high-frequency region (from f_H onwards).
(ii) The gain in the mid-frequency region is A_{mid} and the range of frequencies $f_L - f_H$ is band width.
(iii) Frequencies f_1 and f_2 are called 3-dB frequencies or half-power frequencies; the range of frequencies $f_1 - f_2$ is called 3 dB bandwidth (3 dB BW).
(iv) The product of A_{mid} and 3 dB bandwidth is the "figure of merit" for the amplifier.
i.e. $\text{GBW} = A_{mid} \times 3$ dB BW (4.44c)

Table 4.3 Coupled amplifiers comparison

Sl. No.	Parameter	TC amplifier	RC coupled amplifier	Direct coupled Amplifier
1	Coupling element	Transformer	Resistors-capacitors	No elements
2	Cost of amplifier	More	Less	Least
3	Frequency response	Poor, contains hump or kink	Good	Best
4	Bandwidth	Medium	Good	Best
5	Impedance matching	Very good	Poor	Good
6	Application	Power amplifiers	Voltage amplifiers	Low-frequency amplification

4.7 FEEDBACK IN AMPLIFIERS

Feedback is a process of connecting a part of output signal back to input. This feedback signal can either add to the input signal or oppose the input signal; accordingly, there are two types of feedback:

(a) Positive Feedback Here, the feedback signal and the input signal are both in phase with each other, resulting in increased input. This increases the output of the amplifier, but distortion increases and leads to instability.

(b) Negative Feedback Here, the feedback signal and the input signal are out of phase with each other resulting in decreased input. This decreases the output of the amplifier.

A feedback arrangement contains the amplifier (A), a feedback circuit, an adder to add suitably the input signal and the feedback signal; this is indicated in Fig. 4.22. A fraction of the output signal is connected back to the input of the amplifier with gain A, using a feedback network with a feedback factor 'β'. An adder circuit combines the input v_{in} suitably with the feedback signal.

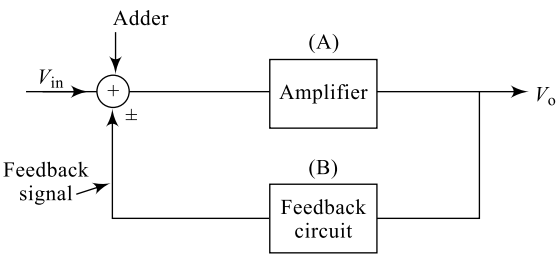
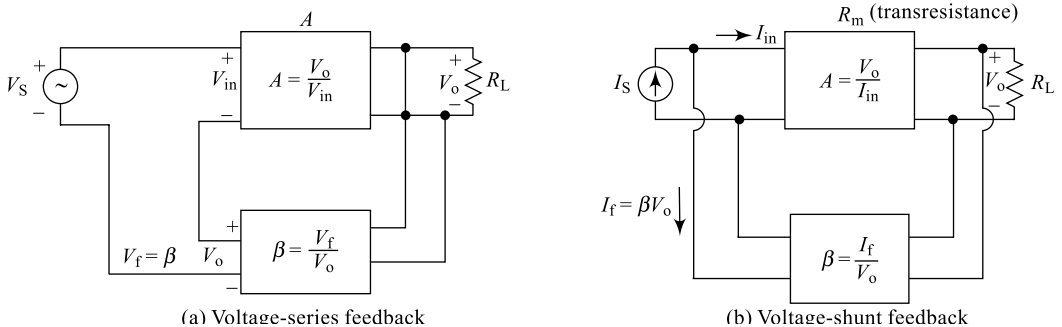
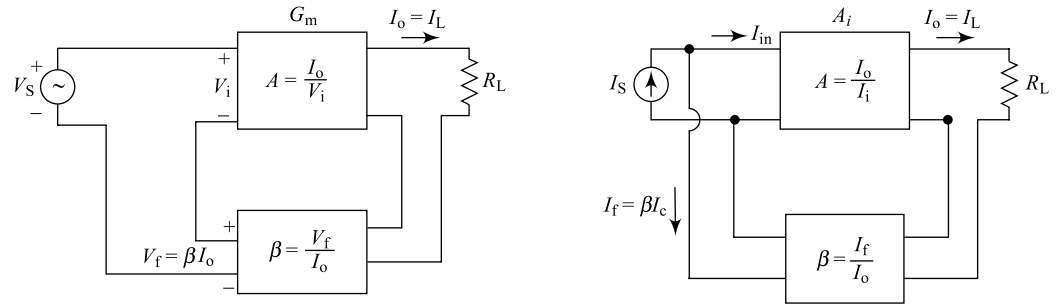


Fig. 4.22 Feedback principle



(a) Voltage-series feedback (b) Voltage-shunt feedback

Fig. 4.23 Voltage feedback



(a) Current-series feed back (b) Voltage-shund feedback

Fig. 4.24 Current feedback

A positive feedback offers the advantage of increased gain, but the disadvantages are more. Hence, it is rarely used in applications except construction of oscillators. A negative feedback reduces gain (disadvantages) of the amplifier, but offers a bunch of advantages and hence is popularly used. The advantages of negative feedback are listed in Section 4.8.

Feedback can be classified based on phase of the feedback signal with respect to that of the input signal. Positive feedback and negative feedback. Feedback can also be classified based on the signal that is feedback to the input as voltage feedback and current feedback.

As indicated in Fig. 4.23, a voltage feedback includes sampling of output voltage signal (shunt connection). This feedback signal is connected as either V_f or I_f at the input resulting in a voltage-series or voltage-shunt feedback.

As indicated in Fig. 4.23, a current feedback includes sampling of output current signal (series connection). This feedback signal is connected as either V_f or I_f at the input resulting in a current-series or current-shunt feedback.

In order to understand the effect of feedback on the performance of an amplifier the following discussion may be made use of:

1. Current Gain and Voltage Gains with Feedback

(a) Voltage-series Feedback Here, AV_f is voltage gain with feedback, A is voltage gain without feedback and B is the feedback factor.

$$AV_f = \frac{V_o}{V_s} \tag{4.45}$$

$$A = \frac{V_o}{V_{in}} \tag{4.46}$$

But $V_{in} = (V_S + V_f)$

From Eq. (4.46), we may write

$$V_o = AV_{in} = A(V_s + V_f) = AV_S + AV_f;\ V_o = AV_s + A(\beta V_o) \tag{4.47}$$

$$(1 - A\beta)V_o = AV_S \quad \text{i.e.} \quad AV_f = \frac{V_o}{V_s} = \frac{A}{(1 - A\beta)} \Rightarrow \tag{4.48}$$

Gain is reduced by a factor $(1 + A\beta)$ for negative feedbacks where β is –ve; gain average increases for positive feedbacks where β is +ve.

(b) Voltage-shunt Feedback Here, in this circuit, a transresistance is considered and is the ratio of output voltage to input source current.

$$A_f = \frac{V_o}{I_s} \tag{4.49}$$

$$= \frac{A \cdot I_{in}}{(I_{in} + I_f)} = \frac{AI_{in}}{(I_{in} + \beta V_o)} = \frac{AI_{in}}{(I_{in} + \beta AI_{in})} \tag{4.50}$$

$$\boxed{A_f = \frac{A}{(1 + A\beta)}}$$

Transfer current gain also reduces by a factor $(1 + A\beta)$ for –ve feedback.

2. Input Impedance with Feedback

(a) Voltage-series Feedback Consider the diagram given below in Fig. 4.25. Here I_{in} is input current and Z_{in} is input impedance.

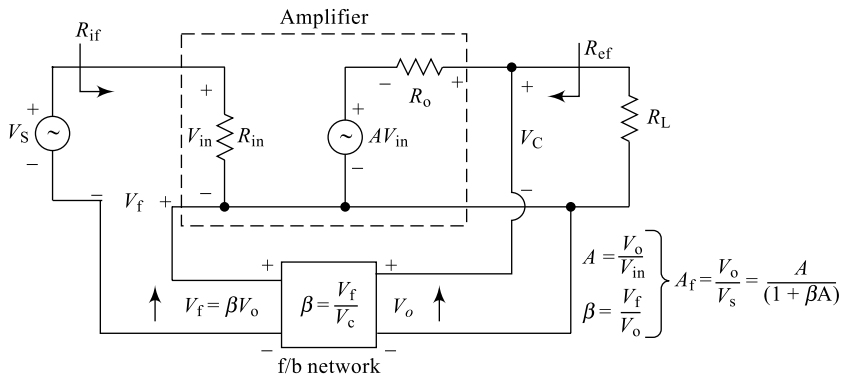


Fig. 4.25 (a) Input impedance estimation

$$I_{in} = \frac{V_{in}}{Z_{in}} \tag{4.51}$$

$$= \frac{(V_s + V_f)}{Z_{in}} = \frac{(V_s + \beta V_o)}{Z_{in}} = \frac{V_s + \beta AV_{in}}{Z_{in}} \tag{4.52}$$

$$I_{in}Z_{in} = V_S + \beta AV_{in}); \quad V_S = (I_{in}Z_{in} + \beta AV_{in})\ (I_{in}Z_{in} + \beta AI_{in}Z_{in}) \tag{4.53}$$

$$Z_{if} = \frac{V_s}{I_{in}} = Z_{in} + (\beta A)Z_{in} = Z_{in}(1 + \beta A) \tag{4.54}$$

$$\boxed{Z_{if} = Z_{in}\ (1 + A\beta)}$$

I/p impedance increases for negative feedbacks.

(b) Voltage-shunt Feedback Consider Fig. 4.25(b) to estimate the input impedance.

$$Z_{if} = \frac{V_{in}}{I_s} = \frac{V_{in}}{I_{in} + I_f} = \frac{V_{in}}{I_{in} + \beta V_o} \tag{4.55}$$
$$= \frac{(V_{in}/I_{in})}{(I_{in}/I_{in} + \beta V_o/I_{in})}$$

$$\boxed{Z_{if} = \frac{Z_{in}}{(1 + \beta A)}} \Rightarrow \text{Input impedance reduces in voltage shunt f/b.} \tag{4.56}$$

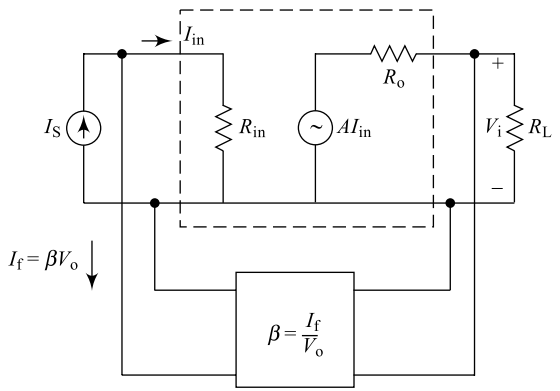


Fig. 4.25 (b) Input impedance estimation

3. Output Impedance with Feedback

(a) Voltage-series Feedback Consider the circuit of Fig. 4.24(a) and the following equations can be written:

$$V_o = (IZ_o + AV_{in}) \tag{4.57}$$

For $V_S = 0$, $V_{in} = -V_f$ so that

$$V_o = (IZ_o - AV_f) = (IZ_o - A(\beta V_o)), \text{ i.e. } IZ_o = (V_o + \beta AV_o) = V_o(1 + A\beta)$$

$$\Rightarrow \quad \boxed{\frac{V_o}{I} = \left(\frac{Z_o}{1 + A\beta}\right) = Z_{of}} \tag{4.58}$$

$\Rightarrow$ Z_o reduces with negative feedback

(b) Current-series Feedback Consider Fig. 4.26 to estimate output impedance of a current series $V_{in} = V_f$

$$I = \left(\frac{V}{Z_o} - AV_{in}\right) = \left(\frac{V}{Z_o} - AV_f\right) \tag{4.59}$$

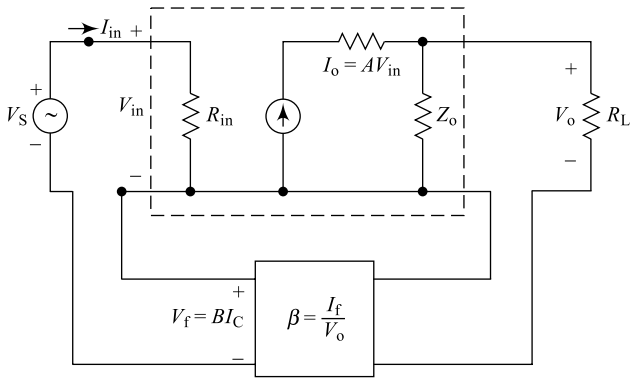


Fig. 4.26 Output impedance estimation

$$= \left(\frac{V}{Z_o} - A\beta I\right), \text{ i.e. } (I + IA\beta) = \frac{V}{Z_o}$$

i.e. $Z_o(1 + A\beta)I = V$

$\therefore$ $$\boxed{\frac{V}{I} = Z_{of} = Z_o/(1 + A\beta)} \tag{4.60}$$

Table 4.4 Z_o increases with positive feedback.

Sl. No.	Parameter	Voltage-series	Voltage-shunt	Current Series	Current Shunt
1	*I/p* impedance	$Z_{if} = Z_i(1 + A\beta)$	$Z_{if} = \frac{Z_i}{(1 + A\beta)}$	$Z_{if} = Z_i(1 + A\beta)$	$Z_{if} = \frac{Z_i}{(1 + A\beta)}$
2	*o/p* impedance	$Z_{if} = \frac{Z_o}{(1 + A\beta)}$	$Z_{of} = \frac{Z_o}{(1 + A\beta)}$	$Z_f = Z_o(1 + A\beta)$	$Z_f = Z_o(1 + A\beta)$
3	Voltage gain	$AV_f = \frac{A}{(1 + A\beta)}$	$AV_f = \frac{A}{(1 + A\beta)}$	—	—

4.8 ADVANTAGES OF NEGATIVE FEEDBACK

A negative feedback in an amplifier offers the following advantages.

(i) Input impedance of the amplifier increases
(ii) Output impedance of the amplifier decreases
(iii) Frequency response of the amplifier improves
(iv) Bandwidth of the amplifier increases
(v) Noise of the amplifier reduces

(vi) Linear range of operation for amplifier increases
(vii) Stability of operation increases
(viii) GBW of amplifier remains unchanged

Table 4.5 Summary of feedback in amplifiers

Sl. No.	Parameter	Negative Feedback	Positive Feedback
1	Input impedance	$Z_{if} = Z_{in}(1 + A\beta)$	$Z_{if} = Z_{in}/(1 + A\beta)$
2	Output impedance	$Z_{of} = Z_o/(1 + A\beta)$	$Z_{of} = Z_o(1 + A\beta)$
3	Voltage gain	$A_{Vf} = \frac{A}{(1 + A\beta)}$	$A_{Vf} = \frac{A}{(1 - A\beta)}$
4	Current gain	$A_{If} = \frac{A}{(1 + A\beta)}$	$A_{If} = \frac{A}{(1 - A\beta)}$

There is a disadvantage in negative feedback that the amplifier gain reduces. Because of all these advantages, negative feedback is widely used in amplifiers. In contrast, positive feedback offers more gain; continuously increasing gain leads to a situation where the feedback signal can completely replace the input source. This situation produces an output signal even in the absence of an input signal and the resulting application is called oscillator (discussed in sections 4.9 to 4.13).

Example 4.13

An amplifier has a gain of 5000 without any feedback. In order to improve the amplifier performance, a negative feedback is introduced into the circuit with a feedback factor of 2%. Find the gain.

Solution Given $A = 5000$, $\beta = 2\% = \frac{2}{100} = 0.02$, $A_f = ?$

From Eq. (4.48), gain with feedback is

$$A_f = \frac{A}{1 - A\beta}\ ;\ \beta = -0.02$$

i.e.
$$A_f = \frac{5000}{1 - 5000\,(-0.02)} = 49.51$$

Example 4.14

An amplifier has a given of 10^3 and this gain drops to 10^2 when a feedback is connected. Find the feedback factor and the type of feedback.

Solution Given $A = 10^3$ and $A_f = 10^3$, $\beta = ?$

Since there is a drop in gain, it is a negative feedback.

From Eq. (4.48), gain is

$$A_f = \frac{A}{1 - A\beta}$$

i.e.
$$100 = \frac{1000}{1 - 1000\,\beta}$$

i.e.
$$\boxed{\beta = -0.090}$$

Example 4.15

A two-stage amplifier uses two identical stages with a gain of 10^2. If the circuit uses a negative feedback of 0.5%. What is the gain with feedback?

Solution Given stage gain = $A_1 = A_2 = 10^2$.
From Eq. (4.61); cascaded gain $A = A_1 \times A_2 = 10^2 \times 10^2 = 10^4$
From Eq. (4.48), feedback gain is

$$A_f = \frac{A}{1 - A\beta}$$

$$= \frac{10^4}{1 - 10^4\left(\frac{-0.5}{100}\right)} = 196.08$$

Example 4.16

A BJT amplifier with a gain of 10000 and input impedance of 5 kΩ has a feedback factor of 1%. Calculate the new values of gain and input impedance.

Solution Given $A = 10000$, $Z_{in} = 5\ k\Omega$ and $\beta = 0.01$
From Eq. (4.48), feedback gain is

$$A_f = \frac{A}{1 - A\beta} = \frac{10000}{1 + 10000(0.01)} = 99.$$

From Eq. (4.54)

$$Z_{if} = Z_{in}\,(1 + A\beta)$$

$$= 5 \times 10^3\,(1 + 10000 \times 0.01)$$

$$Z_{if} = 505\ k\Omega.$$

4.9 ANALYSIS OF AMPLIFIERS

Performance of any circuit or system depends mainly on its design; it applies to amplifier circuits also. A better design procedure will always result in a better circuit performance. A better design can be obtained through a better and proper analysis. Analysis of an amplifier includes estimating important values such as the input impedance (Z_{in}), output impedance (Z_o), Current gain (A_I) and the voltage gain (A_V) for the amplifier. This can be done using several methods and each method uses a set of transistor parameters derived from an equivalent circuit. Some of the important parameters include hybrid parameters (*H*-parameters), impedance parameters (*Z*-parameters), admittance parameters (*y*-parameters), resistance parameters (*r*-parameters), etc. Of these, *H*-parameters are very popular and provide very accurate analysis. Considering a transistor two-port network shown in Fig. 4.27, different *H*-parameters can be defined based on the two important governing equations, (4.61) and (4.62).

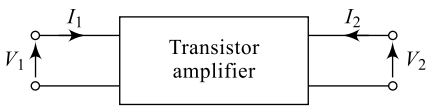


Fig. 4.27 Two-port network for *H*-parameters

$$V_1 = h_{11}I_1 + h_{12}V_2 \tag{4.61}$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \tag{4.62}$$

Here, V_1 and I_1 are port-1 parameters and V_2 and I_2 are port-2 parameters. The four amplifier parameters are hence given by

Input impedance of amplifier

$$h_i = h_{11} = \frac{V_1}{I_1}\,\Omega\Big|_{V_2=0} \tag{4.63}$$

Output impedance of amplifier

$$h_o = h_{22} = \frac{I_2}{V_2}\,\mho\Big|_{P_1=0} \tag{4.64}$$

Forward current gain of amplifier

$$h_f = h_{21} = \frac{I_2}{I_1}\Big|_{V_2=0} \tag{4.65}$$

Reverse voltage gain of amplifier

$$h_r = h_{12} = \frac{V_1}{V_2}\Big|_{I_1=0} \tag{4.66}$$

4.10 PRINCIPLE OF SINUSOIDAL OSCILLATORS

An oscillator is an electronic circuit that generates signals of the desired shape and frequency. Generating high-frequency signals using conventional electric generators is not wise because of the wear and tear associated; hence, noiseless, compact and power-efficient electronic circuits are used. An oscillator circuit generates both sinusoidal and non-sinusoidal signals with frequencies ranging from a very small value to as high values as multiples of giga hertz. As discussed in Section 4.8, positive feedback in an amplifier increases the gain continuously and a stage is reached where the feedback signal can eliminate completely the input. Therefore, an oscillator can be defined as a positive feedback amplifier with infinite gain.

Oscillators can be classified based on various parameters into different types. Based on the range of frequencies they generate, oscillators can be classified into two types.

(a) **Audio-frequency oscillators** which generate less frequencies in the audio range of 20 Hz to 20 kHz.
(b) **Radio-frequency oscillators** which generate high frequencies above audio range.

Based on the type of output signal they generate, oscillators can be classified into two types.

(a) **Sinusoidal oscillators** which generate sinusoidal signals.
(b) **Non-sinusoidal oscillators** which generate non-sinusoidal signals such as square wave, triangular wave, ramp signals, etc.

Based on the type of feedback used, oscillators can be classified into two types

(a) **Positive feedback oscillators** which use positive feedback.
(b) **Negative resistance oscillators** which use no feedback but negative resistance devices.

Basic Components of Oscillator

The basic components required to construct an oscillator are shown in Fig. 4.28(a). It consists of a positive feedback amplifier, a tank circuit (containing R, L, C components) in the feedback path. A is the amplifier gain and β is the feedback factor. Figure 4.28(b) is the LC tank circuit which is responsible for generating sinusoidal signals. Consider ideal L and C components. With 'C' fully charged. When switch 'I_s' is closed, the electrostat energy on capacitor is completely discharged into 'L' as electromagnetic

energy. This electromagnetic energy from inductor again charges C in the opposite direction resulting in a sine wave of frequency given by Eq. (4.67). This process repeats

$$f = \frac{1}{2\pi\sqrt{LC}} \text{ Hz} \tag{4.67}$$

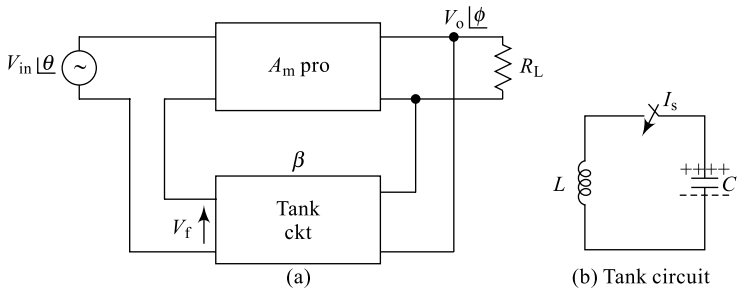


Fig. 4.28 Oscillator components

resulting in continuous sine wave. But, in a practical situation, the resistive components in L and C cause a loss in the generated signal resulting in a dying down sine wave called **damped oscillations** as indicated in Fig. 4.29(a). If the losses in the tank circuit are adjusted, then the generated signals last long, resulting in continuous **undamped oscillations** as indicated in Fig. 4.29(b). The amplifier used in the circuit compensates for the tank circuit losses.

$$V_f = \beta V_o \angle \phi \tag{4.68}$$

i.e.
$$V_f = \beta \angle \phi \, (A V_{in} \angle \phi)$$

$$V_f = A\beta \angle \theta + \phi \, (v_{in}) \tag{4.69}$$

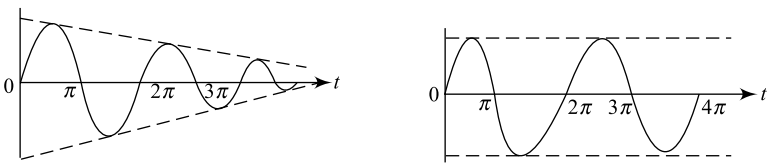


Fig. 4.29 Oscillators output signal

The output of the feedback circuit V_f is given by Eq. (4.68). The phase angle of this signal is the total phase shift around the loop given by $\angle \theta + \phi$ and the loop gain is '$A\beta$' as indicated in Eq. (4.69). Because of the positive feedback, a stage will be reached where the loop gain

$$A\beta = 1 \tag{4.70}$$

and the total phase shift around the closed loop will be $\angle \theta + \phi = 0°$ or $n(2\pi)$ (4.71)

At this stage,

$$V_f = V_{in} \tag{4.72}$$

and this indicates that the feedback signal V_f can completely replace V_{in} resulting in infinite gain (output without input) for the amplifier Equations (4.70) and (4.71) are called **Barkhausen's conditions** for oscillations. Also, for commencement of oscillations, it is required that the initial loop gain should be greater than 1,

i.e.
$$A\beta > 1 \tag{4.73}$$

4.11 RC PHASE-SHIFT OSCILLATOR

Sections 4.11 and 4.12 present two popular and widely used low-frequency oscillators. The *RC* phase-shift oscillator is one of the commonly used audio-frequency oscillators and is shown in Fig. 4.30. It consists of a BJT amplifier; here R_1, R_2, R_C, R_E, along with V_{CC} decide the dc operating conditions for the amplifier. The three *RC* sections shown form the tank circuit and also the feedback circuit. The last *RC* section contains a variable R' so that input impedance of the amplifier R_i in series with R' forms R, i.e.

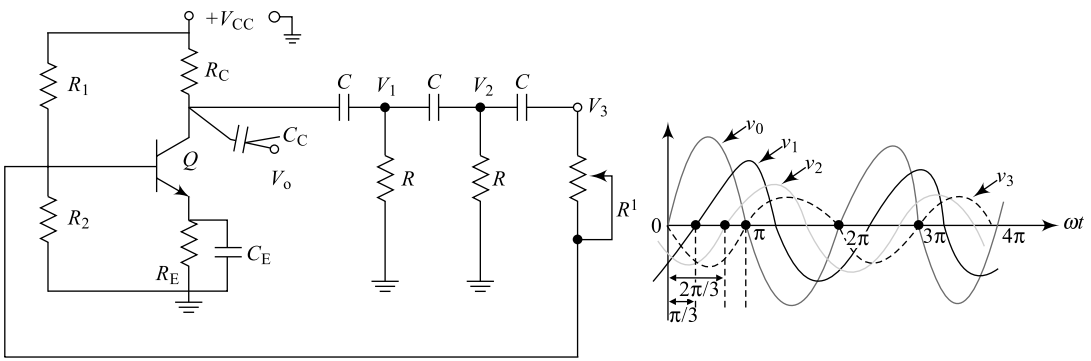
$$R' = (R - R_i) \tag{4.74}$$

The amplifier in CE configuration produces a phase shift of 180° and the three *RC* sections produce a phase shift of 180° (each section offers 60° phase shift) so that the total phase shift is 360°. This results in a positive feedback and phase condition given by Eq. (4.71) is satisfied. Now when Eq. (4.70) is satisfied, the circuit works as oscillator generating sinusoidal signal as shown in Fig. 4.29(a) and the frequency of this signal is given by Eq. (4.75).

$$f = \frac{1}{2\pi RC\sqrt{6 + 4\left(\frac{R_C}{R}\right)}} \text{Hz} \tag{4.75}$$

In order that the amplifier satisfies the gain condition given by Eq. (4.70), the BJT used should have a current gain given by Eq. (4.76)

$$h_{fe} \geq \left(23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}\right) \tag{4.76}$$



(a) Circuit diagram (b) Waveforms

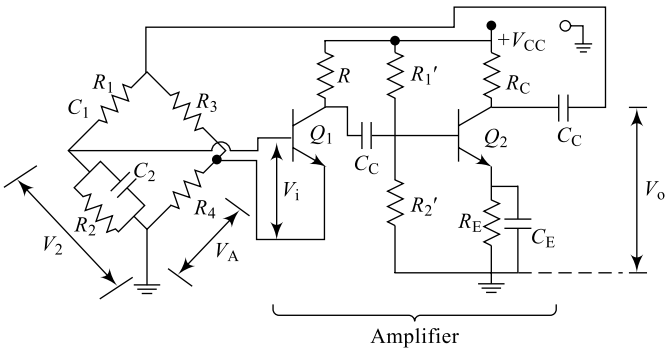
Fig. 4.30 *RC* phase-shift oscillator

4.12 WEIN BRIDGE OSCILLATOR

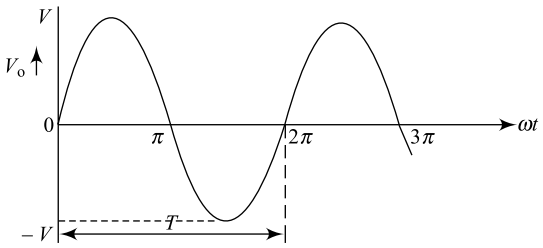
Another popular low-frequency oscillator in use is the wein bridge oscillator and its circuit diagram is shown in Fig. 4.31(a). The tank circuit consists of a bridge formed using resistors R_1, R_2, R_3, R_4 and capacitors C_1 and C_2. The sinusoidal signal generated by the circuit is shown in Fig. 4.31(b) and the reciprocal of the time period T gives the generated frequency 'f'.

Output of the oscillator 'V_o' is *i/p* to bridge.

Bridge will be balanced if $v_i = 0$ and it needs



(a) Circuit diagram



(b) Output waveforms

Fig. 4.31 Wein bridge oscillator

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \tag{4.77}$$

If $R_1 = R_2$ and $C_1 = C_2$, then

$$\frac{R_3}{R_4} = 2, \text{ i.e. } \boxed{R_3 = 2R_4} \tag{4.78}$$

Under balanced condition of bridge ($v_i = 0$)

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \tag{4.79}$$

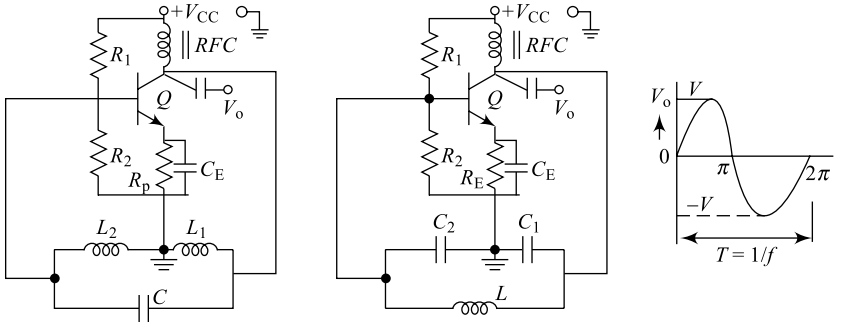
$$= \frac{1}{\sqrt{R^2 C^2}}$$

since $R_1 = R_2$ & $C_1 = C_2$

i.e. $$\boxed{f = \frac{1}{2\pi RC} \text{Hz}} \tag{4.80}$$

4.13 HARTLEY OSCILLATOR AND COLPITTS OSCILLATOR

Generation of high frequencies generally in the ratio frequency range is achieved using three popular oscillator circuits, namely Hartley oscillator, Colpitts oscillator and the crystal oscillator. The crystal oscillator is presented in Section 4.14, while the other two are discussed in this section.



(a) Hartley oscillator (b) Colpitts oscillator (c) Output waveform

Fig. 4.32 Hartley and Colpitts oscillators

Components R_1, R_2, R_E, C_E along with V_{CC} sets the dc conditions for the amplifier that works in CE mode. *RFC* is the radio frequency coil that is mainly used to avoid mixing of generated ac signals at the collector with the dc source V_{CC}. The CE amplifier provides a phase shift of 180° to the signal at output, while another 180° is provided by the tank circuit, so that the total phase shift around the closed loop is 360° satisfying phase condition given by Eq. (4.71).

For the Hartley oscillator, the tank circuit contains two inductors L_1, L_2 and a capacitor C as shown in Fig. 4.32(a). In order that there is a proper feedback, it is required that $L_1 > L_2$. Also, to satisfy the gain condition given by Eq. (4.70), the transistor should have a current gain given by Eq. (4.81)

$$h_{fe} \geq \Delta h \left(\frac{L_1}{L_2} \right) \tag{4.81}$$

Here, Δh is the determinant of h-parameters of the transistor and is given by

$$\Delta h = \begin{vmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{vmatrix} = (h_{11} h_{22} - h_{12} h_{21}) = (h_{ie} h_{oe} - h_{re} h_{fe}) \tag{4.82}$$

Similarly, for a Colpitts oscillator, the tank circuit contains two capacitors C_1, C_2 and an inductor L as shown in Fig. 4.32(b). In order that there is a proper feedback, it is required that $C_1 < C_2$. Also, to satisfy the gain condition given by Eq. (4.70), the transistor should have a current gain given by Eq. (4.83)

$$h_{fe} \geq \Delta h \left(\frac{C_2}{C_1} \right) \tag{4.83}$$

Here, Δh is given by Eq. (4.82) and the generated output for both oscillators (shown in Fig. 4.32(c) has a frequency given by (Eq. (4.84).

$$f = \frac{1}{2\pi\sqrt{LC}} \text{Hz} \tag{4.84}$$

For a Hartley oscillator,

$$L = L_1 + L_2 \tag{4.85}$$

For Colpitts oscillator,

$$C = \frac{C_1 C_2}{C_1 + C_2} \tag{4.86}$$

4.14 CRYSTAL OSCILLATOR

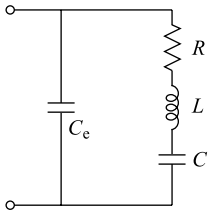


Fig. 4.33 Equivalent circuit of a crystal

As discussed in Section 4.13, Hartley, Colpitts and crystal oscillators are all used for high frequency generation. However, when very high frequencies are to be generated, stability of the output signal is very important. A crystal oscillator offers very good stability to output, even at very high frequencies. A crystal is a piezoelectric material such as crystalline, quartz etc. and its equivalent circuit indicated in Fig. 4.33 contains a series R, L, C elements with an equivalent mounting capacitance 'C_e' across them.

A crystal oscillator is simply, an alternate form of either a Hartley or a Colpitts oscillator. Different forms of crystal oscillators can be realised and two possible forms are shown in Fig. 4.33. In both cases, R_1, R_2, R_E, C_E along with V_{CC} set the dc conditions for the amplifier. The amplifier offers a phase shift of 180° in CE mode and another phase shift of 180° is offered by the tank circuit. The frequency of oscillation is given by Eq. (4.87) and the crystal is expected to have a high quality factor given by Eq. (4.88).

$$f = \frac{1}{2\pi\sqrt{LC}} \text{Hz} \tag{4.87}$$

For crystal quality factor

$$Q = \frac{\omega L}{R} \geq 20{,}000 \tag{4.88}$$

Example 4.17

A BJT amplifier has an input impedance of 4 kΩ and gain of 10^3. What is the new value of input impedance of a negative feedback of 0.005 is used?

Solution Given $Z_{in} = 4$ kΩ and $\beta = 0.005$
From Eq. (4.54),

$$Z_{if} = Z_{in}(1 + A\beta)$$
$$= 4 \times 10^3 (1 + 1000 \times 0.005)$$
$$Z_{if} = 24 \text{ k}\Omega$$

Example 4.18

A BJT *RC* phase-shift oscillator is designed to produce an audio-frequency sine wave. If tank circuit resistance is 2 kΩ and capacitance is 470/nF, what is the output frequency generated with a collector circuit resistance of 4 kΩ.

Solution Given $R = 2$ kΩ, $C = 470$ nF (47 nanofarads), $R_C = 4$ kΩ.
From Eq. (4.75), the output frequency

$$f = \frac{1}{2\pi \times 2 \times 10^3 \times 47 \times 10^{-4} \sqrt{6 + 4\left(\frac{4 \times 10^3}{2 \times 10^3}\right)}}$$
$$= 452.5 \simeq 453 \text{ Hz}$$

Example 4.19

Two transistors Q_1 and Q_2 with current gains respectively 25 and 50 are available; which among them is suitable for Example 4.18 oscillator?

Solution Given $h_{fe}(Q_1) = 25$, $h_{fe}(Q_2) = 50$
From Eq. (4.76), $h_{fe(min)}$ for Example 4.18 is

$$h_{fe} \geq \left(23 + 29\frac{2\times10^3}{4\times10^3} + 4\frac{4\times10^3}{2\times10^3} \right)$$

$$\boxed{h_{fe} \geq 45.5}$$

So, only Q_2 is suitable.

Example 4.20

A Wein bridge oscillator uses tank circuit values $R_1 = R_2 = 1000\ \Omega$ and $C_1 = C_2 = 0.1\ \mu F$. What is the frequency of the generated signal?

Solution From Eq. (4.80),

$$f = \frac{1}{2\pi(1000)(0.1\times10^{-6})} = 1591.55$$

$$\simeq 1592 \text{ Hz.}$$

Example 4.21

A Hartley oscillator is designed to generate a high-frequency signal. If $L_1 = 1$ mH, $L_2 = 0.1$ mH and $C = 200$ pF find the value of f generated.

Solution Given $L = 1$ mH, $L_2 = 0.1$ mH and $C = 200$ pF, $f = ?$
From Eq. (4.85)

$$L = (1 \times 10^3 + 0.1 \times 10^{-3}) = 1.1 \text{ mH}$$

From Eq. (4.84)

$$f = \frac{1}{2\pi\sqrt{1.1\times10^{-3}\times200\times10^{-12}}} \text{Hz}$$

$$f = 339.32 \text{ kHz.}$$

Example 4.22

A colpitts oscillator uses $C_1 = 100$ pF, $C_2 = 200$ pF and a coil of 100 μH. Find the frequency generated.

Solution Given $C_1 = 100$ pF, $C_2 = 200$ pF and $L = 100\ \mu H$
From Eq. (4.86)

$$C = \frac{C_1C_2}{C_1 + C_2} = \frac{100\times10^{-12}\times200\times10^{-12}}{(100+200)10^{-12}}$$

$$= 66.667 \text{ pF}$$

From Eq. (4.84)

$$f = \frac{1}{2\pi\sqrt{100\times10^{-6}\times66.667\times10^{-12}}}$$

$$\boxed{f = 1.95\ \text{mHz}}$$

Example 4.23

If L_2 is increased by fourfold in Example 4.21. What is the new-frequency value?

Solution Given $L_2' = 4(L_2)$

$= 4(0.1\ \text{mH}) = 0.4\ \text{mH}$

From Eq. (4.84),

$$f = \frac{1}{2\pi\sqrt{1.4\times10^{-3}\times200\times10^{-12}}}$$

$= 30.77\text{k} \simeq 301\ \text{kHz}.$

$$\boxed{f = 301\ \text{kHz}}$$

Example 4.24

If C_2 is halved in Example 4.22. What is the new frequency generated?

Solution Given $C_2' = C_2/2$

$= 100\ \text{pF}$

From Eq. (4.86),

$$C = \frac{C_1C_2}{C_1+C_2} = \frac{(100\times100)10^{-24}}{(100+100)10^{-12}}$$

$$= 50\times10^{-12}\ \text{F}$$

From Eq. (4.84),

$$f = \frac{1}{2\pi\sqrt{100\times10^{-6}\times50\times10^{-12}}}$$

$$\boxed{f = 2.251\ \text{mHz}}$$

A Wein bridge oscillator offers the following advantages compared to a Phase-shift oscillator:

(i) A wide range of frequencies can be generated because of R_1, R_2, C_1 and C_2 variations.
(ii) The circuit used both positive and negative feedback and hence is moe stable compared to phase-shift oscillator.

Because of these reasons, a Wein bridge oscillator is widely used in laboratory-purpose audio frequency (AF) signal generators.

Summary

- A BJT when supply biased on the middle of the load line, amplifies the weak input signal and the gain of amplifier may be suitably controlled.
- Audio-Frequency amplifiers (AF amplifiers) are used to amplify signals in the range of 20 Hz to 20 kHz and are widely used in public-address systems.
- Radio-Frequency amplifiers (RF amplifiers) are used to amplify audio-frequency signals in the range of a few MHz to few hundreds of MHz and are widely used in applications such as radio communication, television systems, mobile communications, etc.
- Whenever the gain required is more and if a single-stage amplifier cannot provide this gain then more stages can be connected in series to achieve the gain.
- When a number of amplifier stages are cascaded (connected in series) together, the overall gain of the multistage amplifier is a product of individual stage gains or summation of individual stage dB gains.
- Whenever the gain required is more and if a single-stage amplifier cannot provide this gain then more stages can be connected in series to achieve the gain.
- A CE amplifier offers good voltage gain and current gain, and hence is suitable for power amplification. (A CC amplifier is a current amplifier, a CB amplifier is a voltage amplifier and both of them are not suitable for power amplification.)
- A power amplifier can be put under one of the following classes depending upon the collector current flow (*Q*-point on load line): Class-*A*, Class-*B*, Class-*AB* and Class-*C*.
- A Class-A amplifier can be a series-fed type or transformer-coupled type offering a maximum conversion efficiency of 25% or 50% respectively.
- A Class-B amplifier can be a push-pull type or a complementary-type offering a maximum conversion efficiency of 78.5%.
- A Class-B amplifier eliminates all even harmonics (noise components); the output contains only odd-numbered noise components and results in reduced noise in the output.
- In a Class-B push-pull amplifier, switching between the two transistors results in a zero collector current for a short duration called the crossover distortion and this can be eliminated by Class-*AB* operation.
- A complementary-symmetry amplifier eliminates the need for input and output transformers of a Class-B amplifier.
- Frequency response of an amplifier is the gain variation of the amplifier with respect to frequency changes of the input signal and it is one of the important characteristics of an amplifier one needs to study before designing any amplifier.
- Frequency response of an amplifier gives information on the lower cut-off, upper cut-off, 3 dB bandwidth, maximum gain of the amplifier.
- The cascading of multistage amplifiers can be without use of any components and is called direct coupled amplifier.
- The frequency response of a direct-coupled amplifier is very fair compared to other coupling methods because; there is no coupling capacitor and hence there is no gain variation at low frequencies. This increases the amplifier bandwidth.
- A direct-coupled amplifier is badly affected by the drift in the *Q*-point; this is because of the dc components entering next stage due to the absence of the blocking capacitor.
- The cascading of multistage amplifiers can also be with the use of a coupling transformer and is called transformer-coupled amplifier.

- ➢ The frequency response of a transformer-coupled amplifier is not fair and contains a hump. A transformer-coupled amplifier is best suited for final stages in multistage because its turns ratio can be adjusted suitably for impedance matching.
- ➢ The cascading of multistage amplifiers can also be with the use of *RC* coupling and is called *RC* coupled amplifier.
- ➢ The frequency response of an *RC* coupled amplifier is fair enough and contains a broad and wide bandwidth. An *RC* coupled amplifier is best suited for all initial stages in multistage and is very popular in public-address systems.
- ➢ Feedback in an amplifier is the process of connecting a part of the output back to the input; if the feedback signal is in-phase with the input signal, it is called positive feedback and if the feedback signal is in-phase opposition to the input signal, it is called negative feedback.
- ➢ A negative feedback always improves the performance of an amplifier and hence is widely used. But, a positive feedback has mainly disadvantages and is rarely used.
- ➢ If a negative feedback is used in an amplifier then the frequency response, input impedance, gain and output impedance of the amplifier will improve.
- ➢ In the construction of an oscillator, a positive feedback is used and the tank circuit will be responsible for generating signals of required frequency.
- ➢ Low-frequency oscillators use *RC* circuits for signal generation and high-frequency oscillators use *LC* circuits.
- ➢ An amplifier to work as an oscillator has to satisfy magnitude condition $A\beta = 1$, phase condition closed-loop angle $(\theta + \Theta) = 0°$ or $n2\pi$ and $A\beta > 1$; these conditions are called Barkhausen's conditions for oscillators.
- ➢ Crystal oscillators are known for stable output and are a very popular class of oscillators.
- ➢ Analysis of an amplifier is better performed using *H*-parameters.

Review Questions

1. What is an amplifier? Explain in your own words.
2. From previous knowledge, explain the extent up to which the CC, CE and CB configurations work as amplifiers.
3. Sketch the basic input and output waveforms of an amplifier considering either a current or a voltage signal.
4. Explain in your own words the terms amplification, gain and dB gain.
5. Explain why the multiplication factor is 10 for power gain and 20 for either voltage or current gains when decibel (dB) gain is calculated.
6. Show that the overall gain in a multistage amplifier is the product of individual stage gains.
7. Show that the overall dB gain in a multistage amplifier is the sum of individual stage dB gains.
8. Explain in your own words the terms Class-A, Class-B and Class-C operations.
9. Explain how Class-AB operation is useful in minimising the amplifier distortion.
10. Explain in your own words, how a push-pull amplifier reduces output distortion.
11. What is crossover distortion? Explain.
12. How does a Class-AB operation eliminate cross over distortion? Explain.
13. What are the advantages of a complementary-symmetry amplifier?
14. What are the uses of frequency response in designing an amplifier?
15. Explain the following terms: bandwidth, upper cut-off, lower cut-off.

16. Explain the significance of 3 dB bandwidth for an amplifier.
17. Explain why f_1 and f_2 are called half-power frequencies?
18. What is cascading of amplifier stages? Explain
19. What are the different coupling methods available for multistage amplifier? Explain.
20. What are the advantages offered by transformer coupling? Explain.
21. Why is a transformer coupled amplifier generally not used in the initial stages of a multistage amplifier? Explain.
22. What are the disadvantages of transformer-coupled amplifier? Explain.
23. What are the advantages offered by direct coupling? Explain.
24. Why is a direct-coupled amplifier seldom used in a multistage amplifier? Explain.
25. What are the disadvantages of a direct-coupled amplifier? Explain.
26. What are the advantages offered by *RC* coupling? Explain.
27. Why is an *RC* coupled amplifier is generally preferred in the construction of a multistage amplifier?
28. What are the disadvantages of an *RC* coupled amplifier? Explain.
29. Give reasons for gain decay at low and high frequencies in an amplifier.
30. Why is the mid-band in a *RC* coupled amplifier fairly constant? Explain.
31. What are the disadvantages of an *RC* coupled amplifier? Explain.
32. What is feedback in an amplifier? Explain positive and negative feedbacks.
33. What are the disadvantages of a positive feedback? Explain.
34. What are the advantages of a negative feedback on the performance of an amplifier? Explain.
35. Why is *H*-parameter analysis widely used in BJT circuit analysis? Explain.
36. How can an amplifier be converted to work as an oscillator? Explain.
37. What are Barkhausen's conditions in an oscillator? Explain.
38. Name the low-frequency oscillators and high-frequency oscillators you know.
39. What do you mean by damped and undamped oscillations? Explain.
40. What is the gain condition that a BJT in *RC* phase shift oscillator has to satisfy?
41. What are the advantages of a Wein-bridge oscillator over an *RC* phase-shift oscillator? Explain.
42. Write the frequency expression in Hartley and Colpitts oscillators. Comment on the component values.
43. A crystal oscillator is preferred over its counterparts for high-frequency generation, Why?

Exercise Problems

1. The maximum achievable absolute gain of a single-stage BJT amplifier is 50. If the achievable undistorted output is 5 V then find the maximum input that can be applied. Also, find the decibel in gain.
2. The input power to an amplifier is 10 mW while the output power is 1.5 W. Find the maximum achievable absolute power gain of a single-stage amplifier.
3. A multistage amplifier employs 4 stages with each individual-stage power gain of 20. What is the total dB gain of the amplifier?
4. A multistage amplifier employs 3 stages with each individual-stage power gain of 30. What is the total dB gain of the amplifier? If another stage with a power gain of 20 is inserted between first and second stage, what is the new overall power gain?
5. A multistage amplifier consists of three stages; the voltage gain of the stages are 60, 100 and160. Calculate the overall dB gain.

6. A single-stage amplifier has collector load $RC = 10\ \text{k}\Omega$, input resistance $R_{\text{in}} = 1\ \text{k}\Omega$ and $\beta = 100$. If $R_L = 100\ \Omega$, find the voltage gain.
7. We are to match a 16 Ω speaker load to an amplifier so that the effective load resistance is 10 kΩ. What should be the transformer turns ratio?
8. We are to match a 24 Ω speaker load to an amplifier so that the effective load resistance is 12 kΩ. What should be the transformer turns ratio?
9. An amplifier has a gain of 2×10^5 without feedback. Determine the gain if negative voltage feedback is applied, given $\beta = 0.02$.
10. An amplifier has a gain of 2×10^5 without feedback. Determine the gain if negative voltage feedback is applied, given $\beta = 0.04$.
11. When negative voltage feedback is applied to an amplifier of gain 100, the overall gain falls to 50. Calculate the feedback factor.
12. The gain and distortion of an amplifier are 150 and 5% respectively, without feedback. If the stage has 10% of its output voltage applied as negative feedback, find the distortion of the amplifier with negative feedback.
13. The gain and distortion of an amplifier are150 and 10 respectively, without feedback. If the stage has 15% of its output voltage applied as negative feedback, find the distortion of the amplifier with negative feedback.
14. An amplifier has an internal gain A of 300 and its output impedance is 2 kΩ. Negative feedback with feedback factor 0.02 is introduced in the circuit. Calculate the output impedance of the feedback amplifier.
15. Determine the frequency of oscillation for an RC phase shift oscillator if RC network is made of 1 kΩ and 1 μF.
16. Design a RC phase shift oscillator to produce a sinusoidal wave of frequency 2800 H.
17. Design a Hartley oscillator to produce a sine wave of frequency 50 kHz.
18. Determine the frequency of oscillation of Hartley oscillator if the tank circuit has $L_1 = 5$ mH, $L_2 = 10$ mH and $C = 10$ μF. What should be the value of C to get oscillation twice the frequency of above case?
19. Design a Colpitts oscillator to produce a sine wave of frequency 50 kHz.
20. Determine the frequency of oscillation of Colpitts oscillator if the tank circuit has $L = 15$ mH, $C_1 = 5$ μF and $C_2 = 3$ μF. What should be the value of L to get oscillation twice the frequency of the above case?

Multiple-Choice Questions

1. A transistor is a three-layered three-terminal and _____ junction semiconductor device.
   (a) three (b) two (c) four (d) zero
2. An amplifier is a circuit that increases the level of an input _____.
   (a) voltage (b) current (c) both (a) and (b) (d) none of the above
3. A CE amplifier introduces a phase shift of _____ between the input and the output.
   (a) 180° (b) 90° (c) 0° (d) none of the above
4. AF amplifiers are designed to work in the frequency range of _____.
   (a) 20 Hz to 20 MHz (b) 20 Hz to 200 kHz
   (c) 2 kHz to 200 kHz (d) All the above
5. The stage power gain of the amplifier is given by _____.
   (a) A_P = Output power/Input power (b) A_P = Output power/Input voltage
   (c) A_P = Output Voltage /Input power (d) A_P = Input power/Output power

6. The stage voltage gain of the amplifier is given by _____.
   (a) A_V = Output power/Input power
   (b) A_V = Output Voltage/Input Voltage
   (c) A_V = Output Voltage /Input power
   (d) A_V = Input power/ Output power
7. The stage current gain of the amplifier is given by _____.
   (a) A_I = Output power/Input current
   (b) A_I = Output Voltage/Input Voltage
   (c) A_I = Output Voltage /Input power
   (d) A_I = Output Current /Input Current
8. The stage power gain of the amplifier is given by _____.
   (a) $A_P = 10 \log \left[\frac{P_o}{P_{in}} \right]$ dB
   (b) $A_P = 20 \log \left[\frac{I_o}{I_{in}} \right]$ dB
   (c) $A_P = 20 \log \left[\frac{V_o}{V_{in}} \right]$ dB
   (d) All the above
9. If $A_1, A_2, \ldots, A_N$ are the individual stage gains, for an N-stage amplifier then the overall gain A of the multistage amplifier is given by _____.
   (a) $A = A_1 \times A_2 \times \cdots \times A_N$
   (b) $A_{dB} = A_{1dB} + A_{2dB} + \cdots + A_N$ dB
   (c) Neither (a) nor (b)
   (d) Both (a) and (b)
10. A CB amplifier is not suitable for power amplifications, because it is characterized by _____ current gain and moderate voltage gain.
   (a) high (b) moderate (c) less than one (d) none of the above
11. A CC amplifier is not suitable for power amplifications, because it is characterized by _____ current gain and _____ voltage gain.
   (a) high, moderate (b) moderate, high (c) high, unity (d) none of the above
12. A CE amplifier is more suitable for power amplifications, because it is characterized by _____ current gain and _____ voltage gain.
   (a) high, moderate
   (b) moderate, high
   (c) moderate, moderate
   (d) none of the above
13. The power amplifier in which the collector current flows for full 360° period (full cycle) of the input signal is _____ power amplifier.
   (a) Class-A (b) Class-B (c) Class-C (d) none of the above
14. The power amplifier in which the collector current flows for only 180° period (half cycle) of the input signal is _____ power amplifier.
   (a) Class-A (b) Class-B (c) Class-C (d) none of the above
15. The power amplifier in which the collector current flows for less than 180° period (less than half cycle) of the input signal is _____ power amplifier.
   (a) Class-A (b) Class-B (c) Class-C (d) None of the above
16. The power amplifier in which the collector current flows for a period between 180° and 360° (more than half cycle, but less than full cycle) of the input signal is _____ power amplifier.
   (a) Class-A (b) Class-B (c) Class-C (d) Class-AB
17. The ability of an amplifier to convert the dc power supply into ac power delivered to the load is called _____ of the amplifier.
   (a) conversion efficiency
   (b) collector-circuit efficiency
   (c) theoretical efficiency
   (d) all the above

18. The collector-circuit efficiency of an amplifier is given by _____.
    (a) $\eta = \dfrac{\text{ac power delivered to load}}{\text{dc power supplied to circuit}} \times 10\%$ (b) $\eta = \dfrac{\text{dc power supplied to circuit}}{\text{ac power delivered to load}} \times 100\%$
    (c) neither (a) nor (b) (d) both (a) and (b)
19. The collector-circuit efficiency of a series-fed Class-A amplifier is _____.
    (a) 25% (b) 52% (c) 78% (d) 85%
20. The collector-circuit efficiency of a transformer coupled Class-A amplifier is _____.
    (a) 25% (b) 50% (c) 78% (d) 85%
21. The collector-circuit efficiency of a Class-B amplifier is _____.
    (a) 25% (b) 50% (c) 78% (d) 85%
22. The collector-circuit efficiency of a Class-AB amplifier _____.
    (a) increases with increase in conduction period
    (b) increases with decrease in conduction period
    (c) decreases with increase in conduction period
    (d) both (b) and (c)
23. The cross-over distortion is a severe problem observed in _____ amplifier.
    (a) Class-A (b) Class-B (c) Class-C (d) Class-AB
24. A push-pull Class-B operation reduces the distortion by eliminating the _____ in the output of the amplifier.
    (a) even harmonics (b) odd harmonics
    (c) odd and even harmonics (d) none of the above
25. In a transformer-coupled Class-A amplifier, the turns ratio is _____.
    (a) $\dfrac{N_2}{N_1} = \dfrac{I_2}{I_1} = \dfrac{V_1}{V_2}$ (b) $\dfrac{N_1}{N_2} = \dfrac{I_2}{I_1} = \dfrac{V_1}{V_2}$
    (c) $\dfrac{N_2}{N_1} = \dfrac{I_1}{I_2} = \dfrac{V_1}{V_2}$ (d) $\dfrac{N_1}{N_2} = \dfrac{I_1}{I_2} = \dfrac{V_1}{V_2}$
26. The 'figure of merit' for an amplifier is _____ and has _____ unit.
    (a) gain, dB (b) gain bandwidth difference, dB
    (c) gain bandwidth product (GBW), Hz (d) bandwidth, Hz
27. Coupled amplifiers or multistage amplifiers are used to _____.
    (a) increase the even harmonics in the output (b) increase the gain of the amplifier
    (c) increase the odd harmonics in the output (d) none of the above
28. A direct-coupled amplifier uses _____ to couple output of one stage to the input of next stage.
    (a) transformer (b) *RC* network
    (c) *LC* network (d) No coupling element
29. A positive feedback in an amplifier _____ of the amplifier.
    (a) reduces the gain
    (b) increases the gain and reduces the input impedance
    (c) increases the gain and increases the input impedance
    (d) none of the above
30. A negative feedback in an amplifier _____ of the amplifier.
    (a) increases the gain
    (b) increases the gain and reduces the input impedance

(c) increases the gain and increases the input impedance
(d) none of the above

31. A positive feedback in an amplifier _____ of the amplifier.
(a) increases the stability (b) decreases the stability
(c) has no impact on the stability (d) none of the above

32. A negative feedback in an amplifier _____ of the amplifier.
(a) increases the stability (b) decreases the stability
(c) has no impact on the stability (d) none of the above

33. A positive feedback in an amplifier _____ of the amplifier.
(a) increases the GBW (b) decreases the GBW
(c) has no impact on the GBW (d) none of the above

34. A negative feedback in an amplifier _____ of the amplifier.
(a) increases the GBW (b) decreases the GBW
(c) has no impact on the GBW (d) none of the above

35. Considering a transistor as a two-port network, the following h-parameters may be defined to analyze an amplifier;

(a) $h_i = \left.\frac{V_1}{I_1}\Omega\right|_{V_2=0}$ (b) $h_o = \left.\frac{I_2}{V_2}\mho\right|_{I_1=0}$

(c) $h_f = \left.\frac{I_2}{I_1}\right|_{V_2=0}$ (d) All the above

36. An amplifier may be converted into an oscillator by _____ to the circuit.
(a) adding a negative feedback (b) adding a positive feedback
(c) both (a) and (b) (d) none of the above

37. The Barkhausen's conditions for an amplifier to generate oscillations are _____ and _____.
(a) loop gain $A\beta = 1$, $\underline{|\theta + \phi = 0^\circ}$ (b) loop gain $A\beta = 0$, $\underline{|\theta + \phi = 0^\circ}$
(c) loop gain $A\beta = 1$, $\underline{|\theta + \phi = 90^\circ}$ (d) none of the above

38. An *RC* phase-shift oscillator is an example for _____.
(a) AF oscillator (b) RF oscillator
(c) non-sinusoidal oscillator (d) none of the above

39. A Wein bridge oscillator is an example for _____.
(a) AF oscillator (b) RF oscillator
(c) non-sinusoidal oscillator (d) none of the above

40. A Hartley oscillator is an example for _____.
(a) AF oscillator (b) RF oscillator
(c) non-sinusoidal oscillator (d) none of the above

41. A Colpitts oscillator is an example for _____.
(a) AF oscillator (b) RF oscillator
(c) non-sinusoidal oscillator (d) none of the above

42. A crystal oscillator is an example for _____.
(a) AF oscillator (b) RF oscillator
(c) non-sinusoidal oscillator (d) none of the above

43. A crystal oscillator is means for producing _____.
    (a) AF signals (b) stable RF signals
    (c) non-sinusoidal signals (d) none of the above
44. A UJT relaxation oscillator is an example for _____.
    (a) AF oscillator (b) RF oscillator
    (c) non-sinusoidal oscillator (d) none of the above
45. In a Hartley oscillator, the equivalent tank circuit inductance is L_{EQ} = _____.
    (a) $L_1 + L_2$ (b) $L_1 - L_2$
    (c) $L_1 \times L_2$ (d) none of the above
46. In a Colpitts oscillator, the equivalent tank circuit capacitance is C_{EQ} = _____.

    (a) $C_1 + C_2$ (b) $C_1 - C_2$ (c) $C_1 \times C_2$ (d) $\dfrac{C_1 C_2}{C_1 + C_2}$

Communication Systems

5

Goals and Objectives

Upon completion of this chapter, the reader is expected to

- Understand the basic need and concept of a communication system
- Understand the basic block diagram of a communication system
- Understand the differences between analog and digital communication schemes
- Understand the importance of each unit in a communication system
- Understand the process of modulation of the information signal
- Understand the process of de-modulation of the modulated signal
- Understand the different amplitude-modulation schemes
- Understand the power content in each component of an amplitude-modulated wave
- Understand the advantage of carrier suppression in an amplitude-modulated wave
- Understand the bandwidth requirement of an amplitude-modulated wave
- Understand the different frequency-modulation schemes
- Understand the bandwidth requirement of a frequency-modulated wave
- Understand the different AM and FM de-modulation schemes
- Understand the basic concepts of a radio transmitter and a receiver
- Understand the basic concepts of a TV transmitter and a receiver
- Understand the performance parameters such as power, current, bandwidth, etc. in an AM system
- Compare different types of modulation and de-modulation schemes
- Feel confident of taking up higher courses in communication

5.1 INTRODUCTION

A communication system involves processing the available information from a source, transmitting it over a channel available using a transmitter, on the receiving side receive it, further process it and finally deliver it to the destination. In communication systems, the information to be transmitted is called the **message signal** or **information signal** and will be in complex form. This signal is normally the output of a microphone or a television camera and to be transmitted to the receiver intended. If such signals are only amplified and transmitted directly, such a process is called **baseband transmission**. Baseband signals are low-frequency signals, cannot be directly transmitted over longer distances and need some special methods for transmission over longer distances; **modulation** is the process used. Different modulation techniques are available and the focus in this chapter is to discuss a few important methods of modulation. The sinusoidal signal generated from a source is shown in Fig. 5.1 and it can be represented (voltage) by the equation

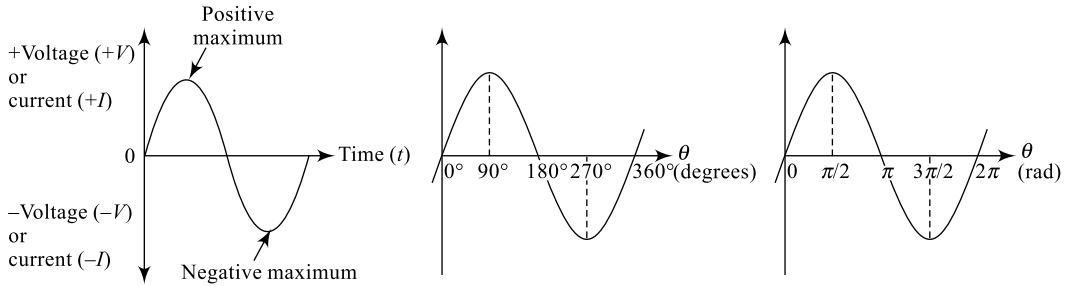


Fig. 5.1 Basic information signal representation

$$v = V_m \sin(\omega t + \Phi) \tag{5.1}$$

Here, v = Instantaneous value of voltage signal
V_m = Maximum/peak value of voltage signal
ω = Frequency in radians = $2\pi f$; f in Hertz
Φ = Signal phase difference with respect to a reference

5.2 COMMUNICATION SYSTEM

A communication process involves generation of the information to be transmitted, processing this information so that it is suitable for transmission, transmitting the processed information through a communication media and receiving it at the receiver, re-processing it so that it is recognisable and finally deliver it to the destination. The block diagram of a simple communication system is shown in Fig. 5.2 and it mainly consists of three important sections; the transmitter, the channel and the receiver.

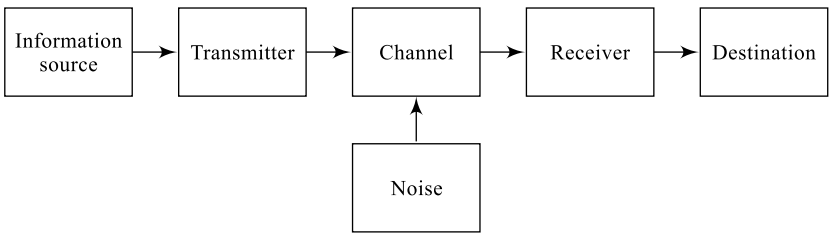


Fig. 5.2 Communication-system block diagram

1. Transmitter (Tx)

A transducer (discussed in Chapter 8) such as a microphone or a television camera generates the message signal to be transmitted. The information so generated is processed and amplified (signal conditioning) at the transmitting end. This message signal is now modulated, encoded and transmitted over a communication media by the transmitter. The transmission can be of two types: wireless communication or a wired-line communication. Hence, a transmitter section consists of a series of low-noise amplifiers, a modulator and a transmitting antenna in case of a wireless communication.

2. Receiver (Rx)

The signal transmitted through the communication media along with noise introduced by the channel is received by the receiver (Rx). The received signal, before it is reconstructed, it will be re-conditioned, amplified, noise minimised, decoded and then demodulated. The signal so detected is finally delivered to the destination. Hence, a receiver section consists of a receiving antenna (in case of a wireless communication), a series of low-noise amplifiers and a de-modulator. A de-modulator does the opposite job of a modulator to retrieve back the original signal from the modulated signal.

3. Channel

The signal from the transmitter after modulation is directed towards the receiver and this transmission can be a wired-line communication or a wireless communication. In a wired-line communication, a media such as a coaxial cable or a twisted pair is used as the transmission channel and in a wireless communication, free space or air is used as the transmission channel. Also, in wireless communication, an antenna is used for the transmission and reception of signals. A more generalised block diagram of a wireless communication system is shown in Fig. 5.3; where there is no physical transmission media connected between the transmitter and the receiver. The transmitter block consists of a transmitting antenna; the transmitter output is radiated through this antenna into free space. The receiver block also consists of an antenna; this receiver antenna collects the signals from the free space, selects the desired signal and the receiver processes this signal.

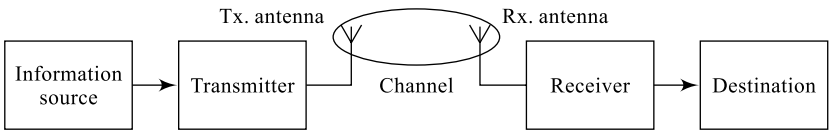


Fig. 5.3 Wireless communication system

Based on the methods adopted in the information processing at the transmitter and the receiver, the communication system can be an analog communication system or a digital communication system.

5.2.1 Analog Communication System

In an analog communication system, the signal in analog (time varying) form is modulated using analog modulation schemes and then transmitted to the receiving end. Several analog modulation schemes are in use today offering many advantages like good quality, high immunity to noise signal, less interference from other signals, lesser costs, etc. Some of the important analog modulation schemes are discussed in Section 5.3 and digital modulation schemes are not discussed here as they are beyond the scope of this text.

5.2.2 Digital Communication System

In a digital communication system, the signal in analog (time-varying) form is first converted into digital form, modulated using digital modulation schemes and then transmitted to the receiving end. A quantiser or an analog-to-digital convertor converts the analog signal to digital form. In digital modulation, the changes in the signal are chosen from a fixed list (the **modulation alphabet**), each entry of which conveys a different possible piece of information (a symbol).

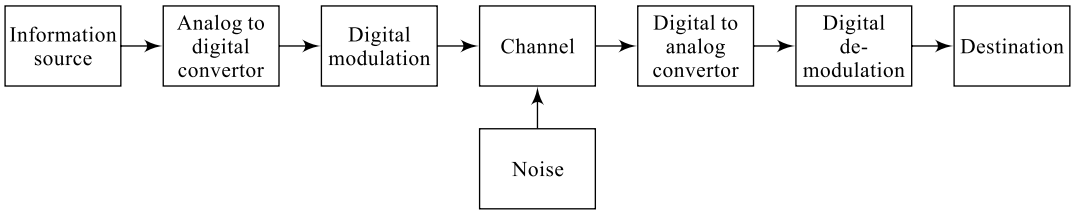


Fig. 5.4 Digital communication system

Like analog communication system, even a digital communication system can also be a wireless where the transmission media is free space and antennas are used at both the transmitter and reciever. The block diagram of a digital communication system is shown in Fig. 5.4 and it can be observed here that the analog information from the source is digitised and then modulated. A source encoder and a channel encoder at the transmitting end can be used for analog-to-digital conversion. Similarly, at the receiver end, a channel decoder and information decoder may be used.

5.2.3 Modulation and De-modulation

Modulation is a technique of modifying one or more characteristics of a carrier signal in a known way in order to transmit the information over a long distance. Any measurable property of an analog signal can be used to transmit information by changing this property in some known manner and then detecting those changes at the receiver end. The high-frequency signal that is modulated is called the **modulated signal** or the **carrier signal**, because it carries the digital information from one end of the communication channel to the other end. The low-frequency source signal that is modulating the carrier is called the **modulating signal** or the **information signal.** *Varying one of the parameters of the high-frequency carrier signal such as amplitude or frequency or phase angle with respect to the instantaneous amplitude variations of the low-frequency information signal (modulating signal) is known as* ***modulation***.

The circuit that changes the signal at the transmitting end of the communication channel is called the **modulator**. The circuit at the receiving end of the channel, which detects the actual information from the modulated signal, is called the **demodulator**.

Advantages and Need for Modulation

1. The length of the antenna required becomes small when the signal is transmitted at high-frequency ranges since $\lambda = c/f \approx$ length of antenna. For audio frequencies, the minimum length of antenna required will be

$$1 = \frac{c}{f_{\max}}$$
$$1 = \frac{3 \times 10^8}{20 \times 10^3} = 10,000 \text{ m} \tag{5.2}$$

2. When transmitted with high frequencies, the energy possessed by the signal is more and hence it can be transmitted over long distances.
3. Wireless communication is possible by increasing the frequency of the signal above the audio range(>20 kHz)
4. At high frequencies, interference or the mixing of signals is less and hence noise will be less.
5. Multiplexing of signals is possible using modulation and this helps in proper utilisation of resources available.

Basically, there are three types of modulation schemes; amplitude modulation and the angle modulation. Angle modulation can further be subdivided into frequency modulation and phase modulation.

5.3 AMPLITUDE MODULATION (AM)

Amplitude modulation is a technique most commonly used for transmitting audio or video signals in communication. It works by varying the strength of the transmitted signal in relation to the information being sent, for example, changes in the signal strength can be used to reflect the sounds being reproduced. Changing the amplitude of the carrier (modulated) signal with respect to the instantaneous changes in the amplitude of the information (modulating) signal, maintaining the carrier frequency constant is known as **Amplitude Modulation** (AM). Amplitude modulation is a form of modulation which represents information as variations in the instantaneous amplitude of a carrier wave. In AM, only the amplitude of a high-frequency carrier is changed in accordance with the instantaneous amplitude changes of a low-frequency message signal; however the frequency of carrier remains same.

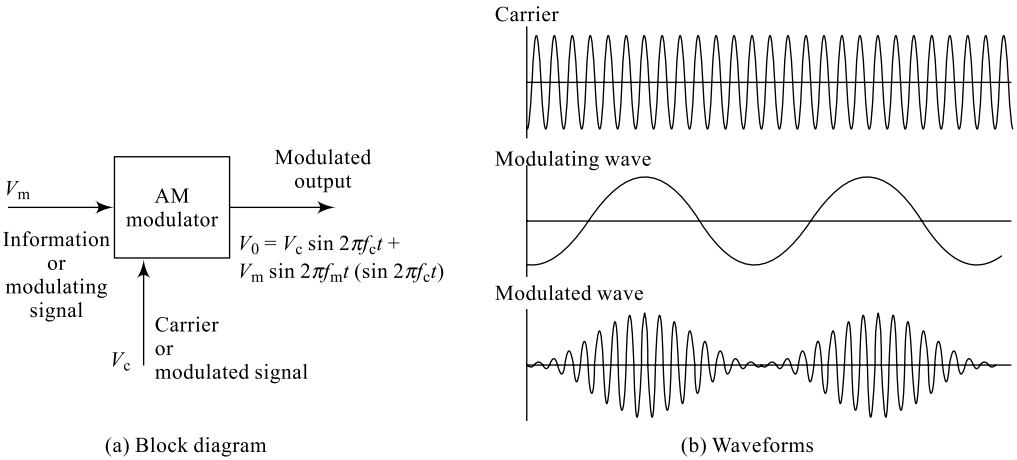


Fig. 5.5 Amplitude-modulation system

In AM, the message signal is superimposed on the carrier signal so that the amplitude of a high-frequency carrier is changed to reflect the message signal amplitude changes. The block diagram of a modulator and the corresponding waveforms are represented in Fig. 5.5. It can be observed here that the amplitude of the carrier signal is changed to reflect the instantaneous amplitude of the message signal, but the frequency of the carrier signal remains unchanged. A variety of transistor-modulation schemes and circuits are available such as an emitter modulation, base modulation, collector modulation and they are not discussed here. Sections 5.3.1 to 5.3.2 are dedicated to discuss different forms of amptitude modulation. The following 6 points provide more insight into the design details of amplitude modulation.

1. Expression for AM Output

Amplitude modulation is performed simply by adding v_m to the carrier signal v_c such that the carrier amplitude changes. Let $v_c = V_c \sin \omega_c t$ be the carrier wave and $v_m = V_m \sin \omega_m t$ be the modulating wave. As per the definition of the AM, the instantaneous amplitude of the AM wave is given by

$$A = V_c = V_m \tag{5.3}$$

$$A = V_c + V_m \sin \omega_m t$$

$$v = V_c(1 + m \sin \omega_m t$$

where $m = \dfrac{V_m}{V_c}$ = Modulation index

i.e. $A = V_c(1 + m \sin \omega_m t)$ (5.4)

The resulting instantaneous AM voltage wave, is therefore, given by

$$v = A \sin \omega_c t$$

$$v = V_1 c(1 + m \sin \omega_1 m\, t)\ [\sin \omega_1 c\, t] \tag{5.4(a)}$$

$$v = V_c \sin \omega_c t + mV_c \sin \omega_m t \sin \omega_c t$$

$$v = V_c \sin \omega_c t + \frac{mv_c}{2}[\cos(\omega_c - \omega_m)t] + \frac{mv_c}{2}[\cos(\omega_c + \omega_m)t] \tag{5.5(a)}$$

$$\text{AM} = \text{Carrier Signal} + \text{LSB} + \text{USB} \tag{5.5(b)}$$

Thus, from Eq. (5.5) it is clear that an AM output signal consists of the basic carrier signal at frequency ω_c and two sidebands, the Lower Side Band (LSB) at frequency $(\omega_c - \omega_m)$ and the Upper Side Band (USB) at frequency $(\omega_c + \omega_m)$. This is indicated in the frequency spectrum shown in Fig. 5.6.

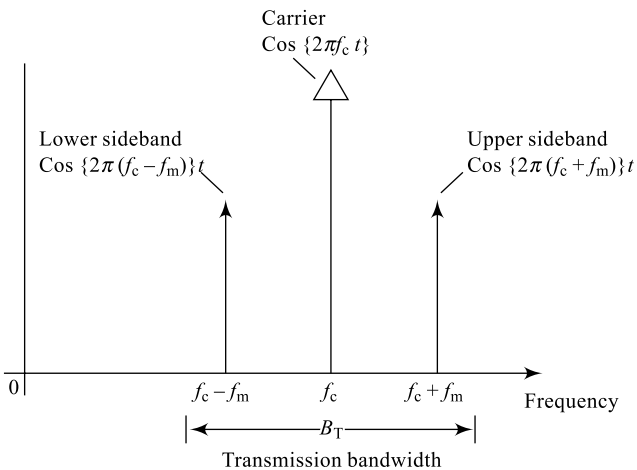


Fig. 5.6 Frequency spectrum of an AM wave

2. Expression for Modulation Index (m) of an AM Wave

Modulation index, also known as the **modulation factor**, indicates the depth of modulation in an AM wave; it is defined as the ratio of the amplitude of the modulating wave to the amplitude of the carrier wave.

$$m = \frac{V_m}{V_c} \tag{5.6}$$

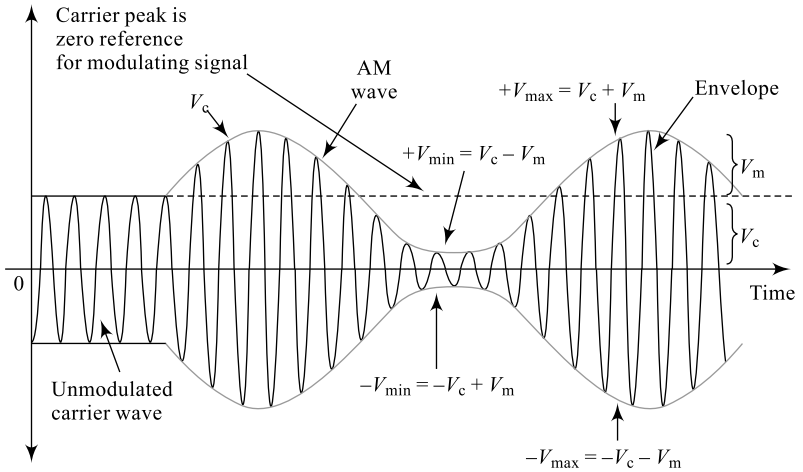


Fig. 5.7 Modulation index of an AM wave

Referring to the AM output wave shown in Fig. 5.7, we can obtain the value of V_m and V_c as

$$V_m = \frac{V_{max} - V_{min}}{2} \tag{5.7}$$

$$V_c = V_{max} - V_m \tag{5.8}$$

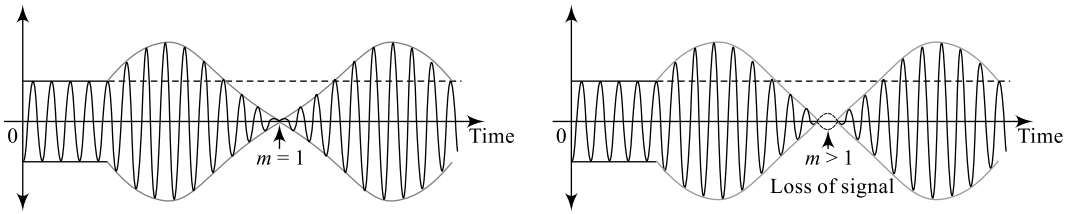
$$V_c = V_{max} - \frac{V_{max} - V_{min}}{2}$$

$$V_c = \frac{V_{max} + V_{min}}{2} \tag{5.9}$$

Now, modulation index is

$$m = \frac{V_m}{V_c} = \frac{\dfrac{V_{max} - V_{min}}{2}}{\dfrac{V_{max} + V_{min}}{2}} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \tag{5.10}$$

It can be observed from Eq. (5.10) that the depth of modulation can be a maximum of 100% when $V_{min} = 0$ and if it exceeds this value, there will be a loss of information as indicated in Fig. 5.8. Similarly, the depth of modulation can be a minimum of 0% when $V_{min} = V_{max}$ resulting in no modulation.



(a) Critical Modulation with $m = 100\ \%$ (b) Overmodulation with $m > 100\ \%$

Fig. 5.8 Limit of modulation index in amplitude-modulated wave

Hence, the range of values for the amplitude modulation index can be

$$0 < m < 1 \tag{5.11}$$

3. Power Relations in AM

The total power contained in an amplitude-modulated wave is the summation of carrier power and the side band powers:

$$P_t = (P_c + P_{LSB} + P_{USB}) \tag{5.12}$$

Now, the carrier power is estimated using the basic relationships and assuming a load of R.

$$P_c = \frac{V_{carr}^2}{R} = \frac{\left[\frac{V_c}{\sqrt{2}}\right]^2}{R}$$

$$P_c = \frac{V_c^2}{2R}\text{W} \tag{5.13}$$

Similarly, the side-band powers are estimated using the basic relationships

$$P_{SB} = \frac{V_{SB}^2}{R} = \frac{\left[\frac{mV_c}{2\sqrt{2}}\right]^2}{R} = \frac{m^2}{4}\frac{V_c^2}{2R}\text{W}$$

$$P_{SB} = \frac{m^2}{4}P_c\,\text{W} \tag{5.14}$$

Therefore, the total power contained in an amplitude-modulated wave is

$$P_t = \left(P_c + \frac{m^2}{4}P_c \text{ for LSB} + \frac{m^2}{4}P_c \text{ for USB}\right)\text{W}$$

$$P_t = P_c\left(1 + \frac{m^2}{2}\right)\text{W} \tag{5.15}$$

With $m = 1$, the total power transmitted is $1.5P_c$ and the individual side-band power contribution is $0.25P_c$.

Example 5.1

A 400-watt carrier is modulated to a depth of 75%. Calculate the total power in the modulated wave.

Solution We have from Eq. (5.15),

$$P_t = P_c\left(1+\frac{m^2}{2}\right)\text{W}$$
$$P_t = 400\left(1+\frac{0.75^2}{2}\right)\text{W}$$
$$P_t = 512.5\ \text{kW}$$

From Example 5.1, with $m = 0.75$, the total power transmitted is $1.282P_c$ and the individual sideband power contribution is $0.11P_c$.

Example 5.2

The power radiated by a transmitter is 10 kW. When the depth of modulation is 60%, calculate the carrier power.

Solution We have from Eq. (5.15),

$$P_t = P_c\left(1+\frac{m^2}{2}\right)\text{W}$$
$$P_t = \frac{P_t}{\left(1+\frac{m^2}{2}\right)}\text{W}$$
$$P_c = \frac{10\times 10^2}{\left(1+\frac{0.6^2}{2}\right)}\text{W}$$
$$P_c = 8.47\ \text{kW}$$

In a similar way, the total transmitted current in an amplitude-modulated wave can be estimated as given below; from Eq. (5.14) the total transmitted power is

$$P_t = P_c\left(1+\frac{m^2}{2}\right)\text{W}$$
$$\frac{P_t}{P_c} = \left(1+\frac{m^2}{2}\right) = \frac{I_c^2 R}{I_c^2 R}$$
$$\frac{I_t^2}{I_c^2} = \left(1+\frac{m^2}{2}\right)$$
$$\frac{I_t}{I_c} = \sqrt{\left(1+\frac{m^2}{2}\right)}$$
$$I_t = I_c\sqrt{\left(1+\frac{m^2}{2}\right)}\ \text{A} \qquad (5.16)$$

Example 5.3

An AM transmitter has an unmodulated current of 8 A and it increases to 8.95 A after modulation. Find the percentage modulation of the output wave.

Solution Given, $I_c = 8$ A and $I_t = 8.95$ A

We have from Eq. (5.16)

$$I_t = I_c \sqrt{\left(1 + \frac{m^2}{2}\right)} \text{ A}$$

Therefore,

$$8.95 = 8\sqrt{\left(1 + \frac{m^2}{2}\right)} \text{ A}$$

$$m^2 = 2\left[\left(\frac{8.95}{8}\right)^2 - 1\right]$$

$$m = \sqrt{0.5}$$

$$m = 0.707 \qquad \text{i.e. } m = 70.7\%$$

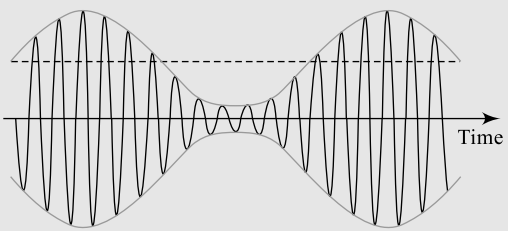
4. Bandwidth in Amplitude Modulation

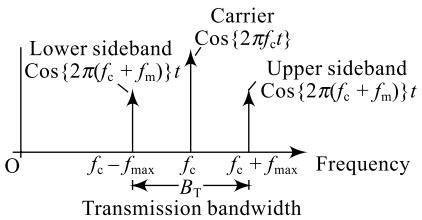
Looking at the frequency spectrum of an AM wave shown in Fig. 5.6, it is clear that the total bandwidth needed for an AM signal is twice the highest modulating frequency. The side bands are located at an equidistance of f_m around f_c and hence

$$\text{BW} = 2f_m \tag{5.17}$$

Table 5.1 presents salient features of AM scheme.

Table 5.1 Key points in AM scheme

Sl. No.	Point	Amplitude Modulation
1	Definition	Changing the amplitude of the carrier signal with respect to the instantaneous changes in the amplitude of the information signal is known as **amplitude modulation**.
2	Waveform	
3	Expression	$v = V_{\downarrow}c(1 + m \sin \omega_{\downarrow} m\, t) \sin \omega_{\downarrow} c\, t]$
4	Modulation index m	$m = \frac{V_m}{V_c} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$
5	Range of m	0 to 1 (0 to 100%)

6	Power transmitted	$Pt = P_c\left(1 + \frac{m^2}{2}\right)$W
7	Antenna Current	$I_t = I_c\sqrt{\left(1 + \frac{m^2}{2}\right)}$A
8	No. of side bands	Only two (02)
9	Frequency spectrum	
10	Total bandwidth	BW = $2f_m$
11	Side-band power	$P_{SB} = \frac{m^2}{4} P_c$ per side band

Example 5.4

An AM transmitter uses a source signal generated by an oscillator generating a sinusoidal signal of 15 sin 1250t. If the carrier signal of 500 kHz is modulated to a depth of 67%, calculate the total bandwidth required to transmit this AM output wave.

Solution Given, $v_m = 15 \sin 1250t$

We have, $\omega = 1250$

Therefore,
$$f_m = \frac{\omega}{2\pi}$$
$$f_m = \frac{1250}{2\pi} = 198.95 \approx 200 \text{ Hz}$$

Now, from Eq. (5.17), the total bandwidth can be estimated as 397.89 Hz which is approximately 400 Hz.

5. Amplitude Modulation by Multiple Signals

It is important to note that when a carrier signal is simultaneously modulated by several information signals then the total modulation index and the total transmitted power change. If V_1, V_2, V_3, etc. are the peak amplitudes and m_1, m_2, m_3, etc. are the corresponding modulation indeces of different information signals modulating simultaneously a carrier signal of amplitude V_c then the total modulation index of the modulated signal output is given by Eq. (5.18).

$$m_t = \sqrt{m_1^2 + m_2^2 + m_3^2 + \cdots} \tag{5.18}$$

Similarly, the total transmitted power is given by Eq. (5.19)

$$P_t = P_t\left(1 + \frac{m_t^2}{2}\right) \tag{5.19}$$

where the total modulation index m_t is given by Eq. (5.18).

Example 5.5

An AM transmitter uses two signal sources to modulate a carrier signal generated by an oscillator generating a sinusoidal signal $15 \sin 125 \times 10^6 t$ and the depth of modulation is 0.64. If the modulation index of the first signal is half the modulation index of the second signal, calculate the values of m_1 and m_2.

Solution Given, $m_t = 0.64$

Now, from Eq. (5.18), we can write

$$0.64 = \sqrt{m_1^2 + (2m_1)^2}$$

$$0.64 = \sqrt{5m_1^2} = 2.24\, m_1$$

$$m_1 = 0.29 \text{ and } m_2 = 0.58$$

6. Forms of Amplitude Modulation

As originally developed for the electric telephone, amplitude modulation was used to add audio information to the low-powered direct current flowing from a telephone transmitter to a receiver. As a simplified explanation, at the transmitting end, a telephone microphone was used to vary the strength of the transmitted current, according to the frequency and loudness of the sounds received. Then, at the receiving end of the telephone line, the transmitted electrical current affected an electromagnet, which strengthened and weakened in response to the strength of the current. In turn, the electromagnet produced vibrations in the receiver diaphragm, thus reproducing the frequency and loudness of the sounds originally heard at the transmitter.

In contrast to the telephone, in radio communication what is modulated is a continuous-wave radio signal (carrier wave) produced by a radio transmitter. In its basic form, amplitude modulation produces a signal with power concentrated at the carrier frequency and in two adjacent sidebands. This is referred as **Double Side-Band Full Carrier (DSB-FC)** modulation scheme. Each side band is equal in bandwidth to that of the modulating signal and is a mirror image of the other. The following sections discuss three of the forms of AM schemes.

5.3.1 DSB-FC Amplitude Modulation

In its basic form, amplitude modulation produces a signal with power concentrated at the carrier frequency and in two adjacent sidebands. This is referred as double side-band full carrier (DSB-FC) modulation scheme. Each side band is equal in bandwidth to that of the modulating signal and is a mirror image of the other. Thus, most of the power output by an AM transmitter is effectively wasted: half the power is concentrated at the carrier frequency, which carries no useful information and the remaining power is split between two identical side bands, only one of which is needed. The advantage to this method is that it greatly simplifies the receiver design and hence the cost of the system reduces. For this reason, this is the transmission method used in conventional AM radio transmissions.

The frequency spectrum shown in Fig. 5.6 suggests that the carrier signal carries no useful information, but adds to transmitted power and the side bands carry the complete information. It is evident from the power equation (5.13) and Example 5.6 that nearly 85% of the transmitted power is saved by carrier suppression.

Example 5.6

The power radiated by a transmitter is 10 kW when the depth of modulation is 60%; calculate the power to be transmitted and the percentage power saving if the carrier signal is suppressed.

Solution We have from Eq. (5.15),

$$P_t = P_c\left(1+\frac{m^2}{2}\right)\text{W}$$

And this gives $P_c = 8.47$ kW (from Example 5.2)

Now, from Eq. (5.15), the transmitted side-band power is

$$P_t' = P_{SB} = \left[P_c\left(\frac{m^2}{4}\right)\text{for LSB} + P_c\left(\frac{m^2}{4}\right)\text{for USB}\right]\text{W}$$

$$P_{SB} = P_c\left(\frac{m^2}{2}\right)\text{W}$$

$$P_{SB} = 8.47\times10^2\left(\frac{0.6^2}{2}\right)\text{W}$$

$P_t' = P_{SB} = 1.525$ kW which is only 15.25% of P_t.

Now, the percentage saving in transmitted power is 84.75%. This encourages the designers to suppress the carrier signal in order to increase the efficiency of the transmitter and reduce the cost. However, elimination of carrier at the transmitter brings in other problems such generation of carrier for synchronisation at the receiver.

5.3.2 DSB-SC Amplitude Modulation

To increase transmitter efficiency, the carrier can be removed (suppressed) from the AM signal. This produces a reduced-carrier transmission or double side-band suppressed carrier (DSB-SC) signal. DSB-SC signals need their carrier to be re-generated for it to be demodulated using conventional techniques at the receiver side.

An AM output is given by Eq. (5.5a) which is reproduced here for convenience.

$$v = V_c\sin\omega_c t + [\cos(\omega_c - \omega_m)t] + \frac{mv_c}{2[\cos(\omega_c+\omega_m)]}$$

Suppressing the carrier component results in a DSB-SC signal that is characterised by the following transmission equation:

$$v' = \frac{mv_c}{2}[\cos(\omega_c-\omega_m)t] + \frac{mv_c}{2[\cos(\omega_c+\omega_m)]} \tag{5.20}$$

It is important to notice that at the receiver side in order to extract the basic information signal, DSB-SC requires a coherent receiver, because of the absence of the carrier signal, and, therefore, the receiver needs to generate locally a carrier signal that is a replica of the carrier signal at the transmitter. DSB-SC systems are, therefore, very susceptible to frequency shifting and phase shifting on the receiving end. The carrier term in the spectrum can be eliminated by removing the dc offset from the modulating signal. DSB-SC and DSB-FC both suffer in terms of transmission bandwidth from the fact that they both send two identical (but reversed) frequency "lobes" or side bands, the upper side band and the lower side band. These bands are exactly mirror images of each other and, therefore, contain identical information. Why can't we cut one of them out and just transmit only one of them? This saves both

power and bandwidth. The resulting scheme is called **Single Side Band** (SSB) transmission. An SSB scheme transmits power given by Eq. (5.14), which is only 25% of the total power at 100% modulation. SSB has a number of problems, but also some good aspects. A compromise between AM-SSB and the two AM-DSB methods can also be thought of which is called **Vestigial Side Band** (VSB) transmission, that uses less bandwidth than the AM-DSB methods, but more than the AM-SSB.

Example 5.7

An AM transmitter suppresses the carrier signal and one of the side bands to reduce the transmitted power. Calculate the value of the transmitted power if $m = 0.64$ and DSB-FC output power is 7.5 kW.

Solution Given $m = 0.64$ and DSB-FC power = 7.5 kW.

Now, from Eq. (5.14) and (5.15), the single side-band power is calculated as below:

$$P_t = P_c\left(1+\frac{m^2}{2}\right)\text{W}$$

$$7.5\times10^3 = P_c\left(1+\frac{0.64^2}{2}\right)\text{W}$$

$$P_c = \frac{7.5\times10^3}{\left(1+\frac{0.64^2}{2}\right)} = 6.23\text{ kW}$$

$$P_{SB} = \left(\frac{m^2}{4}P_c\right)\text{W}$$

$$P_{SB} = \left(\frac{0.64^2}{4}6.23\times10^3\right) = 0.637\text{ kW}$$

This is the transmitted power.

5.3.3 SSB Amplitude Modulation

Even greater efficiency is achieved at the expense of increased transmitter and receiver complexity by completely suppressing the carrier and any one of the side bands. This is called single-side band (SSB) modulation and is widely used in amateur radio due to its efficient use of both power and bandwidth. An AM output is given by Eq. (5.5a) which is reproduced here for convenience

$$v = V_c \sin\omega_c t + \frac{mv_c}{2}[\cos(\omega_c - \omega_m)t] + \frac{mv_c}{2[\cos(\omega_c + \omega_m)]}$$

Suppressing the carrier component and any one of the side bands results in an SSB signal that is characterised by the following transmission equation:

$$v' = \frac{mv_c}{2}[\cos(\omega_c - \omega_m)t] \text{ or } v' = \frac{mv_c}{2[\cos(\omega_c + \omega_m)]} \tag{5.21}$$

It is important to notice that at the receiver side in order to extract the basic information signal, like a DSB-SC system, an SSB system also requires a coherent receiver, because of the absence of the carrier signal. Therefore, the receiver needs to generate locally a carrier signal that is a replica of the carrier signal at the transmitter. DSB-SC systems are, therefore, very susceptible to frequency shifting

and phase shifting on the receiving end. In order to generate an SSB signal, we need to remove one of the side bands from an AM-DSB signal. This means that we need to pass the AM-DSB signal through a filter, to remove one of the side bands. The filter, however, needs to be a very high-order filter, because we need to have a very aggressive roll-off. One side band needs to pass through the filter completely unchanged and the other side band needs to be stopped completely.

AM-SSB is most efficient in terms of bandwidth and transmission power, but there is a significant increased cost in terms of more complicated transmitter and receiver designs. For this reason, AM-SSB is rarely seen as being cost-effective. Table 5.2 presents a brief comparison of different AM schemes.

Table 5.2 Comparison of different AM techniques

Sl. No.	AM Type	Expression	Bandwidth	Application
1	DSB-FC	$v = v_c \sin \omega_c t + \frac{mv_c}{2}[\cos(\omega_c - \omega_m)t] + \frac{mv_c}{2[\cos(\omega_c + \omega_m)]}$	BW = $2f_m$	Radio transmission
2	DSB-SC	$v' = \frac{mv_c}{2}[\cos(\omega_c - \omega_m)t] + \frac{mv_c}{2[\cos(\omega_c + \omega_m)]}$	BW = $2f_m$	Radio transmission
3	SSB	$v' = \frac{mv_c}{2}[\cos(\omega_c - \omega_m)t]$ or $v' = \frac{mv_c}{2[\cos(\omega_c + \omega_m)]}$	BW ≈ f_m	Bandlimited applications; TV systems, telephony, etc.

There a numerous variations of SSB:

- SSB—Single Side Band used in amateur radio
- SSSC—Single Side Band Suppressed Carrier where a small pilot carrier is transmitted
- ISB—Independent Side Band where two separate side bands with a suppressed carrier are transmitted; used in radio telephony
- VSB—Vestigial Side Band, a partial sideband; used in broadcast TV
- ACSSB—Amplitude Companded SSB

There are several advantages of using SSB:

- More efficient bandwidth utilisation
- Less subject to selective signal fading
- More power can be placed in the intelligence signal

5.4 ANGLE MODULATION

As indicated in Eq. (5.1), a signal is characterised by amplitude and angle information. Angular information includes both frequency (f) and phase angle of the signal (φ) with respect to a reference. Amplitude modulation involves varying carrier amplitude, and angle modulation involves varying either the

frequency or the phase angle of the carrier signal with respect to information amplitude. Accordingly, there are two types of angle modulation: frequency modulation and phase modulation.

5.4.1 Frequency Modulation (FM)

In frequency modulation, as indicated in Fig. 5.9, the frequency of the carrier signal is changed and these frequency changes carry the information signal to the receiver end. Changing the frequency of the carrier (modulated) signal with respect to the instantaneous changes in the amplitude of the information (modulating) signal maintaining the carrier amplitude constant is known **Frequency Modulation** (FM). Frequency modulation is a form of modulation which represents information as variations in the instantaneous frequency of a carrier wave. The FM transmitter sends different sets of frequencies for a positive peak and negative peak of the information signal. (This technique is also called FSK—frequency shift keying in digital schemes). Its disadvantages are that the rate of frequency changes is limited by the bandwidth of the line and that distortion caused by the lines makes the detection even harder than amplitude modulation. In analog applications, the carrier frequency is varied in direct proportion to changes in the amplitude of an input signal. Digital data can be represented by shifting the carrier frequency among a set of discrete values, a technique known as frequency-shift keying.

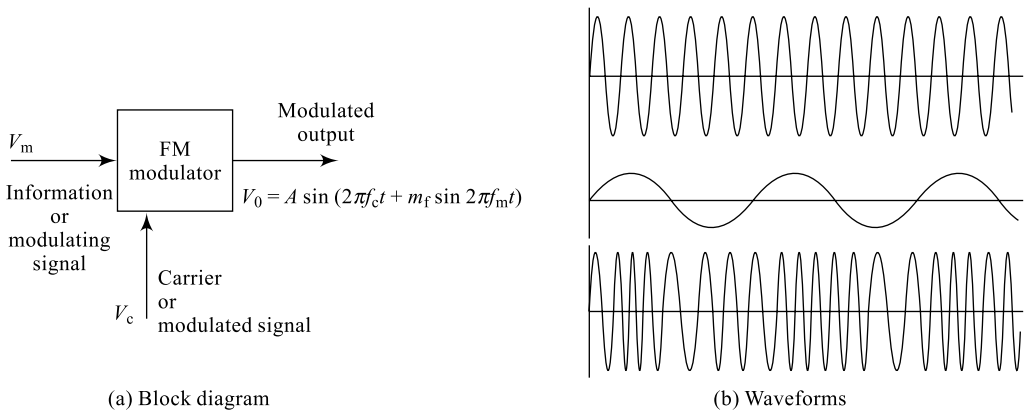


Fig. 5.9 Frequency-modulation System

1. Expression for FM Output

Frequency modulation is performed simply by adding v_m to the carrier signal v_c such that the carrier frequency changes. Let $v_c = V_c \sin \omega_c t$ be the carrier wave and $v_m = V_m \cos \omega_m t$ be the modulating wave. As per the definition of the FM, the instantaneous frequency of the FM wave is given by

$$f = f_c(1 + kV_m \cos \omega_m t) \tag{5.22a}$$

Equation (5.22a) can be rewritten in terms of ω as in Eq. (5.22b):

$$\omega = \omega_c(1 + kV_m \cos \omega_m t) \tag{5.22b}$$

where $k \rightarrow$ proportionality constant

The resulting instantaneous f can take values depending on the cos term in Eq. (5.22); the maximum value of the cos term being ±1. Under these conditions, the f value is, therefore, given by

$$f = f_c(1 \pm kV_m) \tag{5.23}$$

And hence the maximum frequency deviation on either side of f_C could be

$$\delta = kV_m f_c \tag{5.24}$$

Now, based on Eq. (5.23), the carrier signal can be expressed as a function of ω_m and ω_C as in Eq. (5.25) below:

$$v = A \sin(\omega_c, \omega_c)t = A \sin \theta \tag{5.25}$$
$$v = V_1 c(1 + m \sin \theta_1 m\, t) \sin \omega_1 c\, t]$$

Here, θ can be obtained by integrating Eq. (5.22b) with respect to time;

$$\theta = \int \omega dt = \int \omega_c (1 + kV_m \cos \omega_m t) dt$$
$$\theta = \omega_c \int (1 + kV_m \cos \omega_m t) dt$$
$$\theta = \omega_c t + \frac{kV_m \omega_c \sin \omega_m t}{\omega_m}$$
$$\theta = \omega_c t + \frac{\delta}{f_m} \sin \omega_m t \tag{5.26}$$

Now, based on equations (5.25) and (5.26), the FM output expression can be written as in Eq. (5.27):

$$v = A \sin\left(\omega_c t + \frac{\delta}{f_m} \sin \omega_m t\right) \qquad [5.27(a)]$$
$$v = A \sin(\omega_c t + \beta \sin \omega_m t) \qquad [5.27(b)]$$

where $\beta \rightarrow$ modulation index.

2. Modulation Index

Modulation index of an FM system is defined as the ratio of maximum frequency deviation and the modulating frequency f_m.

$$\beta = m_f + \frac{kV_m f_c}{f_m} = \frac{\delta}{f_m} \tag{5.28}$$

Also, $\omega_c = 2\pi f_c$ = Frequency of carrier signal
$\omega_m = 2\pi f_m$ = Frequency of modulating signal
δ = Maximum frequency deviation = $kV_m f_c$
k = Proportionality constant

Frequency of modulated output, hence, can be finally rewritten as in Eq. (5.27b). It can be observed here that the amplitude of the FM wave A remains constant at all times and that is one of the advantages of FM. The frequency spectrum of an FM wave shows that it has an *infinite number* of pair of side bands, since it is a sine function of sine wave. In order to obtain these side bands, Bessel's functions are used (not discussed here). Also, the experimental works by Carson show that most of the FM power (≈98%) is concentrated within a bandwidth of $2(\delta + f_m)$ Hz and hence as a rule of thumb, the bandwidth of the FM signal is estimated using Carson's rule. According to Carson's rule, the bandwidth required to pass an FM wave is "twice the sum of deviation and the highest modulating frequency",

i.e. Bandwidth = $2(\delta + f_m)$ Hz (5.29)

Table 5.3 specifies key points of FM scheme.

Example 5.8

Find the carrier frequency, modulating frequency m_f and maximum deviation of the FM wave represented by $v = 20 \sin(6 \times 10^8 t + 10 \sin 1250t)$

Solution We have an FM wave represented by Eq. (5.27) and hence,

$$\omega_c = 6 \times 10^8 = 2\pi f_c$$

i.e. $f_c = 6 \times 10^8/2\pi$

$$f_c = 95.5 \text{ MHz}$$

Also, $\omega_m = 1250 = 2\pi f_m$

$$f_m = 1250/2\pi$$

Modulating frequency, $f_m = 199$ Hz

Modulation index, $\beta = m_f = \delta/f_m = 10$

Maximum deviation, $\delta = (m_f \times f_m)$ Hz

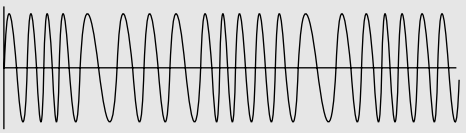
$$= 10 \times 199$$

$$\delta = 1990 \text{ Hz}$$

FM is commonly used at VHF radio frequencies for high-fidelity broadcasts of music and speech. Normally, in analog TV systems, sound signals are broadcasted using FM method. A narrowband form is used for voice communications in commercial and amateur radio settings. The type of FM used in broadcast is generally called wide-FM, or W-FM. In two-way radio, narrowband narrow-FM (N-FM) is used to conserve bandwidth. FM is also used at intermediate frequencies by most analog VCR systems. FM is the most feasible method of recording and retrieving video in magnetic tapes without extreme distortion, as video signals have a very large range of frequency components from a few hertz to several megahertz. FM is also used at audio frequencies to synthesise sound.

FM receivers inherently exhibit a phenomenon called **capture**, where the tuner is able to clearly receive the stronger of two stations being broadcast on the same frequency. Problematically, however, frequency drift or lack of selectivity may cause one station or signal to be suddenly overtaken by another on an adjacent channel. Frequency drift typically constituted a problem on very old or inexpensive

Table 5.3 Key points in an FM scheme

Sl. No.	Point	Frequency Modulation
1	Definition	Changing the frequency of the carrier signal with respect to the instantaneous changes in the amplitude of the information signal is known as **frequency modulation**.
2	Waveform	
3	Expression	$v = A \sin(\omega_c t + \beta \sin \omega_m t)$
4	Modulation Index $\boldsymbol{\beta}$	$\beta = m_f = \dfrac{kV_m f_c}{f_m} = \dfrac{\delta}{f_m}$
5	Range of $\boldsymbol{\beta}$	>1 (>100%)
6	No. of side bands	Infinite (∞)
7	Approximate bandwidth	BW = $2(\delta + f_m)$

receivers, while inadequate selectivity may plague any tuner. An FM signal can also be used to carry a stereo signal. However, this is done by using multiplexing and de-multiplexing before and after the FM process.

Example 5.9

Find the bandwidth required to transmit the FM output in Example 5.8.

Solution We have an FM wave from Eq. (5.29), the bandwidth for an FM system

$$\text{BW} = 2(\delta + f_m)\ \text{Hz}$$

$$\text{BW} = 2(1990 + 199)\ \text{Hz}.$$

$$\text{BW} = 4378\ \text{Hz}$$

5.4.2 Phase Modulation

Phase Modulation (PM) is a form of angle modulation which represents instantaneous amplitude changes in the information as variations in the phase changes of a carrier wave. Changing the phase angle of the carrier signal with respect to the instantaneous changes in the amplitude of the information signal is known as **phase modulation**. In frequency modulation, as the modulating frequency decreases and the modulating voltage amplitude remains constant, the modulation index of the FM increases. Unlike its more popular counterpart, frequency modulation, PM is not very widely used (for musical instruments, introduced by Yamaha around 1982 uses PM). This is because of the more complex and costly receiver (there can be ambiguity problems with determining whether, for example, the signal has 0° phase or 180° phase).The block diagram and the modulated output waveforms for a PM system are shown in Fig. 5.10.

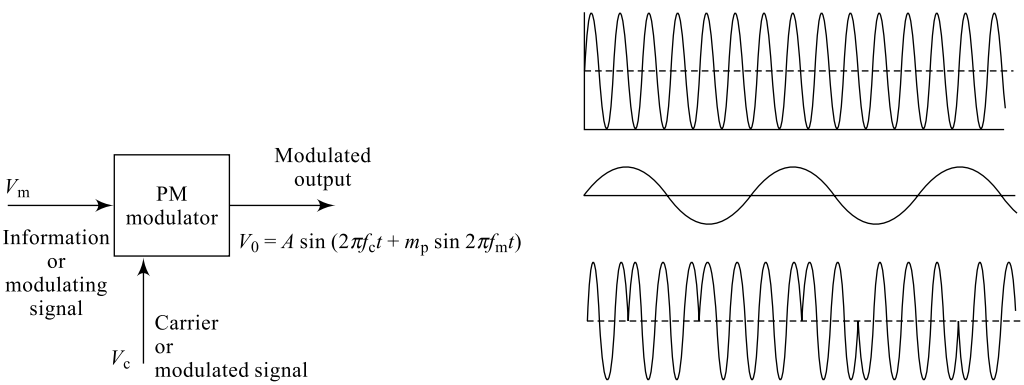


Fig. 5.10 Phase-modulation system

The phase angle φ of the carrier signal is changed according to the instantaneous amplitude of the modulating signal and the resulting phase-modulated wave is given by Eq. (5.30).

$$v = A \sin (\omega_c t + \phi_m \sin \omega_m t) \tag{5.30}$$

where φ_m = Modulation index

The spectral behaviour of PM is difficult to derive, but the mathematics reveals that there are two regions of particular interest:

- For small amplitude signals, PM is similar to amplitude modulation (AM) and exhibits its unfortunate doubling of baseband bandwidth and poor efficiency.

For a single large sinusoidal signal, PM is similar to FM, and its bandwidth is approximately

$$2(1 + \varphi_m) f_m \text{ Hz} \tag{5.31}$$

where $f_M = \omega_m/2\pi$ and φ_m is the modulation index. This is also known as **Carson's rule for PM.**

Example 5.10

A carrier signal generated from frequency source with an LC tank circuit with $L = 25$ μh and $C = 10$ pF is frequency modulated by an audio signal of 1000 Hz; write the FM output expression if the carrier amplitude is 12 V and the maximum deviation is 10×10^3.

Solution Given maximum deviation $\delta = 10 \times 10^3$, $A = 12$, $f_m = 1000$ Hz.

Carrier frequency

$$f_c = \frac{1}{2\pi\sqrt{LC}} \text{Hz}$$

$$f_c = \frac{1}{2\pi\sqrt{25^{-6}} \times 10^{-12}} = 10 \times 10^6 \text{ Hz}$$

$$\beta = \frac{\delta}{f_m} = \frac{10 \times 10^3}{1 \times 10^3} = 10$$

We have an FM wave represented by Eq. (5.27).

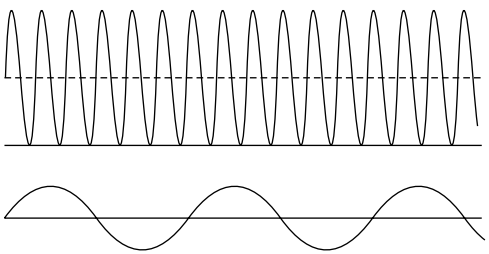
$$v = A \sin (\omega_c t + \beta \sin \omega_m t)$$

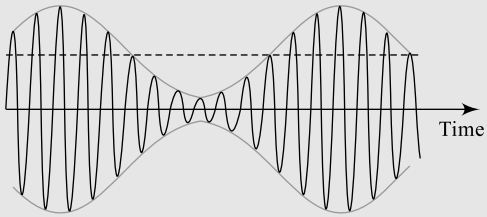
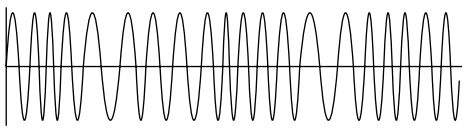
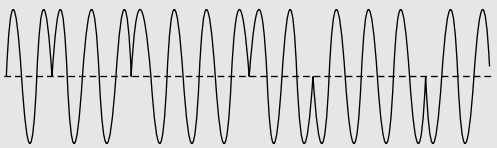
Now, the required FM expression is

$$v = 12 \sin (2\pi \times 10 \times 10^6 t + 10 \sin 2\pi \times 10^3 t)$$

Table 5.4 provides key information for various modulation schemes.

Table 5.4 Various modulated outputs for an information signal

Sl. No.	Modulation Scheme	Modulation Waveform	Output Expression
1	Basic information signal and the carrier signal		$v_m = V_m \sin \omega_m t$ $v_c = V_c \sin \omega_c t$

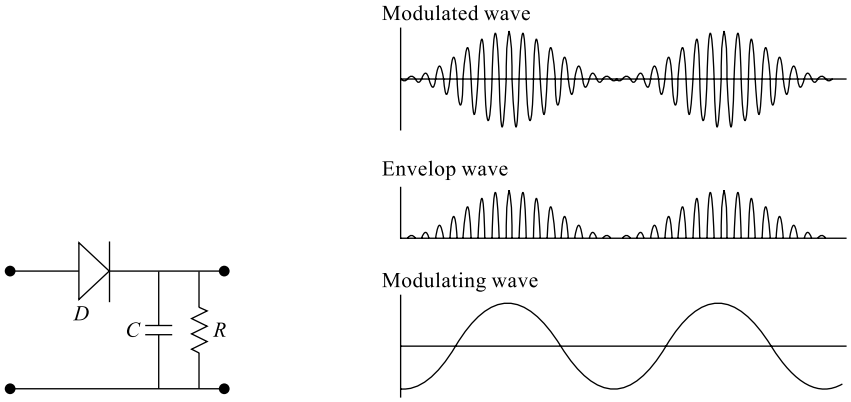
2	Amplitude modulation		$v = V_c \sin \omega_c t + \frac{mv_c}{2}[\cos(\omega_c - \omega_m t) + \frac{mv_c}{2[\cos(\omega_c + \omega_m)]}$
3	Frequency modulation		$v = A \sin(\omega_c t + \beta \sin \omega_m t)$
4	Phase modulation		$v = A \sin(\omega_c t + \phi_m \sin \omega_m t)$

5.5 DEMODULATION TECHNIQUES

The modulated signal output from the transmitter reaches the receiver via the communication channel. It is now required to recover the message signal from this signal so that it is delivered to the destination. The process of reconstructing the information signal at the receiver from the modulated wave is known as **demodulation** or **detection**. Input to the demodulator is the received modulated signal and its output is the required information signal. Detecting an AM signal is very simple and cheap as compared to FM signal or PM signal detection. For this reason, FM and PM communication systems are costlier than AM systems; however, they are characterised by quality and good performances.

5.5.1 AM Detection

In the simplest form, a junction diode can be used as an AM demodulator. From the waveforms shown in Fig. 5.5, it is clear that the message in an AM signal appears in the form of envelopes on either side of the carrier. The required complete message can be extracted from one side of the modulated carrier signal. The circuit diagram and waveforms of such an 'envelope detector' are as shown in Fig. 5.11. Here, the semiconductor diode *D* acts as a simple Half-Wave Rectifier (HWR), giving out only one side of the envelope. The capacitor acts as a filter, recording the traces of the message signal resulting in an output which resembles the information signal. The time constant (time constant of an *RC* circuit $\tau = RC$ is defined as the time taken by the capacitor to charge up to 90% from 10% of its maximum value) of the network. *RC* should be so selected that there will be minimum error in output.



(a) Envelop detector (b) Waveforms

Fig. 5.11 AM detection system

An envelope detector is simply a half-wave rectifier followed by a low-pass filter. In the case of commercial AM radio receivers (refer Section 5.7), the detector is placed after the IF section. The carrier at this point is 455 kHz while the maximum envelope frequency is only 5 kHz. The ripple component is nearly 100 times the frequency of the highest baseband signal and does not pass through any subsequent audio amplifiers. An AM signal where the carrier frequency is only 10 times the envelope frequency would have considerable ripple.

5.5.2 FM Detection

FM output cannot be directly demodulated; instead, it is converted into an AM signal using a parallel resonance circuit and then detected using a simple AM detector such as a diode detector or envelope detector.

There are two basic types of FM detection, coherent and noncoherent. Of these two, the noncoherent one is the simpler method.

- Noncoherent detection does not rely on regenerating the carrier signal. The information or modulation envelope can be removed or detected by a diode followed by an audio filter.
- Coherent detection relies on regenerating the carrier and mixing it with the AM signal. This creates sum and difference frequencies. The difference frequency corresponds to the original modulation signal.

Both detection techniques have certain drawbacks. Consequently, most radio receivers use a combination of both.

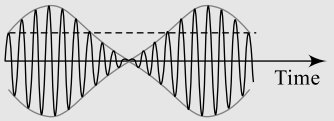
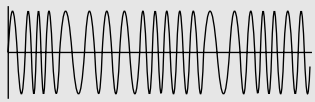
5.5.3 Comparison between AM and FM

From the different sections studied so far, it is evident that modulation is a necessary process for message transmission. Different modulation techniques are available and have some advantages and disadvantages. AM systems offer simplicity in their design and are relatively cheaper; FM systems are costly to design, but offer very good-quality signal transmission. FM systems are highly immune to noise compared to AM systems. Additionally, FM systems have other advantages:

- Noise limiters can be used (to limit amplitude at A) to eliminate noise. Hence there is more clarity.
- Noise can be further reduced by increasing β, the modulation index.

Table 5.5 elaborates further the comparison between the two systems; the AM and FM schemes.

Table 5.5 Comparison between AM and FM technique

Sl. No.	Comparison	Amplitude Modulation	Frequency Modulation
1	Definition	Amplitude of carrier is changed according to instantaneous amplitude changes in message signal, maintaining frequency constant.	Frequency of carrier is changed according to instantaneous amplitude changes in message signal, maintaining amplitude constant.
2	Output wave		
3	Output expression	$v = V_c \sin \omega_c t + \frac{mv_c}{2}[\cos(\omega_c - \omega_m)\tau] + \frac{mv_c}{2[\cos(\omega_c + \omega_m)]}$	$v = A \sin(\omega_c^c t + \beta \sin \omega_m t)$
4	Modulation index (modulation depth)	$m = \frac{V_m}{V_c} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$ Value lies between 0 and 1	$\beta = m_f = \frac{kV_m f_c}{f_m} = \frac{\delta}{f_m}$ Could be more than 1 (β independent of amplitude)
5	Number of side bands	Only two: USB and LSB	Infinite number if side bands
6	Bandwidth	BW = $2f_m$; $f_m \rightarrow$ maximum frequency of modulating signal	BW = $2(f_m + \delta)$; δ-max. frequency deviation
7	Cost of receiver	Comparatively less	More costly
8	Quality of reception	Quite acceptable	Very good
9	No. of channels/ given band of frequency	More (at least 10 times FM)	Less; because of more bandwidth required
10	Reception area [Coverage area]	More compared to FM	Less, since reception is limited to line of sight
11	Application area	TV system video transmission.	TV system audio transmission

5.6 RADIO TRANSMITTER

A radio communication involves sending radio signals from a source to the end user through a channel and a receiver. The radio transmitter is responsible for processing the actual information so that it is suitable for transmission and the radio receiver is responsible for processing the received information so that it is back in its original form before delivering it to the destination. The radio-transmitter block diagram shown in Fig. 5.12 uses amplitude-modulation scheme.

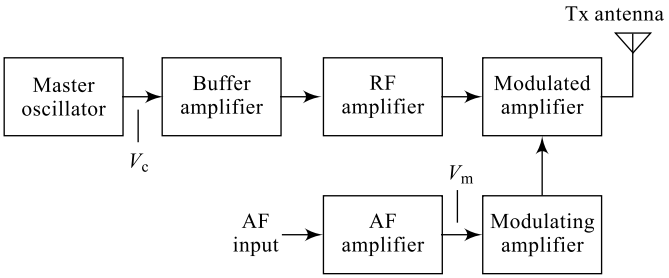


Fig. 5.12 Radio transmitter

The AM transmitter shown consists of a high-frequency carrier signal generator called **master oscillator** which normally uses a crystal oscillator for high-frequency stability. Buffer amplifier is to avoid loading on master oscillator. A series of RF amplifiers are used to increase the strength of the carrier. The low-frequency information signal is amplified using an AF amplifier. Then it is amplified in a push-pull amplifier to reduce distortion. Both the carrier and the information signals are then applied to the modulated amplifier. The output of this amplifier, which is a modulated signal, is then radiated into free space using a transmitting antenna. Thus, the AM transmitter modulates the carrier using information and transmits the signal into free space. The transmitting (Tx) antenna is responsible for radiating the modulated signal in electromagnetic form into the free space. In the arrangement, the process of modulation takes place at a high signal power and is, therefore, referred as **high-level modulation.** On the other hand, if the modulation is done at first and then a series of RF amplifiers are used to increase the power level of the signal, the scheme is referred to as a **low-level modulation**.

5.7 RADIO RECEIVER

In a radio communication, the radio receiver is responsible for processing the received information so that it is back in its original form before delivering it to the destination. A receiver is responsible for selecting the desired information signal from a bunch of such signals. It then processes the signal such that it is noise limited and suitable to be delivered to the destiny. The receiver should sense even low-strength signals and offer good response over a wide range of frequencies. Hence, a radio receiver is characterised by three important characteristics, namely sensitivity, selectivity and fidelity. **Sensitivity** is the ability of a receiver to sense and receive weak signals from the free space. **Selectivity** is the ability of a receiver to distinguish the desired signal from a group of signals available in free space. **Fidelity** is the ability of a receiver to provide a steady and fair frequency response for the received signal over a wide range of frequencies. The receiving (Rx) antenna is responsible for receiving the modulated signal in electromagnetic form from free space. Based on the principle of operation, radio receivers can be broadly classified into two types: the Tuned Radio Frequency (TRF) receiver and the Superheterodyne (superhet) receiver.

5.7.1 TRF Receiver

The block diagram of a TRF receiver is shown in Fig. 5.13. In a TRF receiver, the receiving antenna picks up the signal and this signal is passed through a series of RF amplifiers. Now, the information is reconstructed using a detector. All RF amplifiers are tuned amplifiers that are tuned to signal frequency through ganged tuning. After detection, the signal is further amplified in an AF amplifier so as to drive

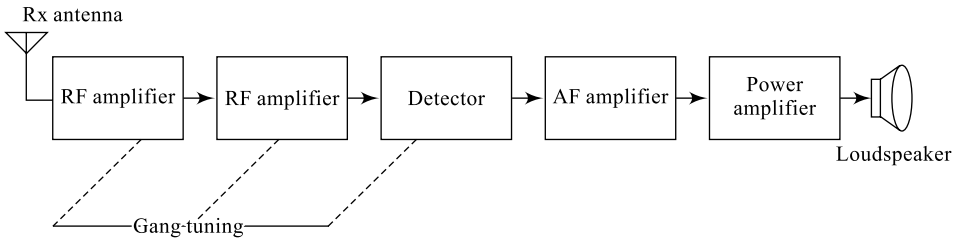


Fig. 5.13 TRF radio receiver

the loudspeaker. It is important to note here that the received signal is processed at the station (carrier) frequency and hence design of various amplifiers and other circuits will be critical. However, the system implementation cost for a TRF receiver will be relatively less compared to a superheterodyne receiver.

Disadvantages

1. Since the signal is amplified at signal frequency, design of RF amplifiers is critical.
2. Frequency response of RF stages is not uniform.
3. Receiver sensitivity reduces because of wide variation of incoming frequency.
4. Needs ganged tuning.
5. Signal-to-noise ratio is less.
6. If sensitivity and selectivity are increased, fidelity reduces.

5.7.2 Superheterodyne Radio Receiver

In a superheterodyne receiver, the receiving antenna picks up the signal and this signal is converted into an intermediate value called IF (Intermediate Frequency), irrespective of the station frequency. Then, this IF signal is passed through a series of RF amplifiers. Now, the information is reconstructed using a detector. All RF amplifiers are tuned amplifiers that are tuned to a single frequency IF through ganged tuning. After detection, the signal is further amplified in an AF amplifier so as to drive the loudspeaker. It is important to note here that the received signal is down converted into a single frequency IF and then processed and hence, the design of various amplifiers and other circuits will be relatively easier unlike in a TRF receiver. Also, response of these circuits will be better than those in TRF receiver because of single frequency. However, the system implementation cost for a TRF receiver will be relatively more compared to a TRF receiver.

The block diagram of a superheterodyne receiver is shown in Fig. 5.14. The RF amplifier boosts the RF signal into the mixer. A frequency mixer is simply a circuit that produces the output signal containing the sum and difference frequency components of the two inputs. The other mixer input is a high-frequency sine wave created by a local oscillator. In AM receivers, it is always 455 kHz above the desired station carrier frequency. An ideal mixer will combine the incoming carrier with the local oscillator to create sum and difference frequencies. Since the RF amplifier passes several radio stations at once, the mixer output can be very complex. However, the only signal of real interest is the difference between the desired station carrier frequency and the local oscillator frequency. This difference frequency, also called the IF (intermediate frequency), will always be 455 kHz. By passing this through a 10 kHz BPF (Band Pass Filter) centred at 455 kHz, the bulk of the unwanted signals can be eliminated.

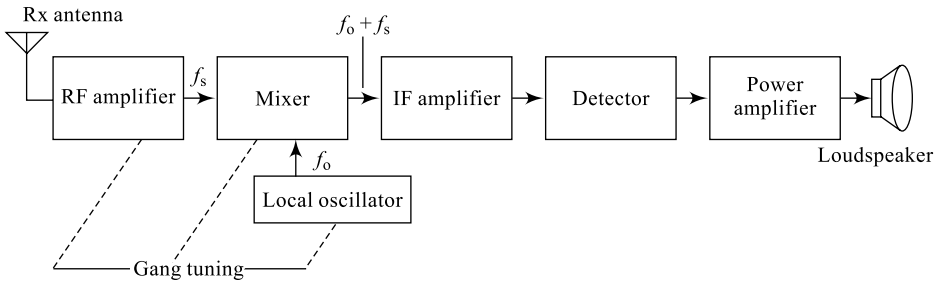


Fig. 5.14 Superheterodyne radio receiver

5.7.2 Local Oscillator Frequency

Since the mixer generates sum and difference frequencies, it is possible to generate the 455 kHz IF signal if the local oscillator is either above or below the IF. Keeping the range of capacitance to be varied in mind, the IF value is selected below the local oscillator frequency. This is elaborated taking AM station range of frequencies.

Case I

The IF value below the local oscillator frequency; this would require the oscillator to tune from (500 + 455) kHz to (1600 + 455) kHz or approximately 1 MHz to 2 MHz. Normally, here the capacitor is varied to adjust the centre frequency while the inductor value is fixed. The centre frequency is given by

$$f_c = \frac{1}{2\pi\sqrt{LC}}\text{Hz} \tag{5.32}$$

From this, the range of capacitor variation can be estimated as given by Eq. (5.33):

$$C = \frac{1}{L(2\pi f_c)^2}\text{Hz} \tag{5.33}$$

When the tuning frequency is a maximum, the tuning capacitor is a minimum and vice versa. Since we know the range of frequencies to be created for an AM station with 500 kHz to 1600 kHz, we can obtain the range of capacitance required using Eq. (5.34).

$$\frac{C_{\min}}{C_{\max}} = \frac{L(2\pi f_{\max})^2}{L(2\pi f_{\min})^2} \tag{5.34}$$

$$\frac{C_{\min}}{C_{\max}} = \frac{(2\times10^6)^2}{(1\times10^6)^2} = 4$$

Making a capacitor with a 4:1 value change is well within the realm of possibility.

Case II

The IF value above the local oscillator frequency; this would require the oscillator to tune from (500–455) kHz to (1600–455) kHz or approximately 45 kHz to 1145 kHz. When the tuning frequency is a maximum, the tuning capacitor is a minimum and vice versa. Since we know the range of frequencies to be created for an AM station with 500 kHz to 1600 kHz, we can obtain the range of capacitance required using Eq. (5.34).

$$\frac{C_{\min}}{C_{\max}} = \frac{L(2\pi f_{\max})^2}{L(2\pi f_{\min})^2}$$

$$\frac{C_{\min}}{C_{\max}} = \frac{(1145 \times 10^3)^2}{(45 \times 10^3)^2} = 648$$

It is not practical to make a tunable capacitor with this wide range of variations. Therefore, the IF value in a standard AM receiver is selected below the local oscillator frequency.

5.7.3 Image Frequency

Just as there are two oscillator frequencies, which can create the same IF, two different station frequencies can create the IF. The undesired station frequency is known as the image frequency.

If any circuit in the radio front end exhibits nonlinearity, there is a possibility that other combinations may create the intermediate frequency. Once the image frequency is in the mixer, there is no way to remove it since it is now heterodyned into the same IF band as the desired station.

A superheterodyne receiver offers the following advantages:

1. Sensitivity is good because of frequency conversion.
2. Receiver fidelity will be good as the bandwidth of IF amplifier is of required value.
3. Frequency response of all amplifiers after the mixer will be good because of single-frequency IF.

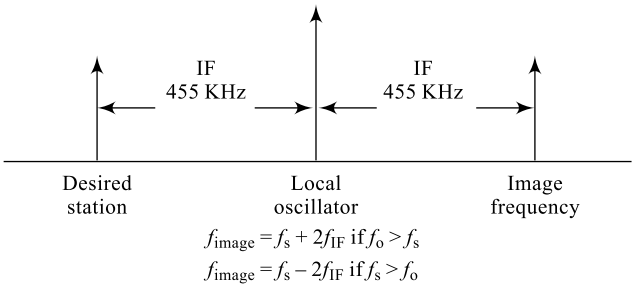


Fig. 5.15 Image frequency in a superheterodyne receiver

5.8 TELEVISION SYSTEM

A Television (TV) communication system, like a radio communication, involves sending both sound (audio) and picture (video) signals from the source to the end user through a channel and a receiver. Similar to a radio transmitter, a TV transmitter is responsible for processing the actual information so that it is suitable for transmission; but it should accommodate both audio and video signals. Similar to a radio receiver, a TV receiver is responsible for processing the received information (both audio and video) so that it is back in its original form before delivering it to the destination. It is very important to maintain a very good synchronisation between the sound and picture signals. Commercially, TV signal transmission can be in either monochrome (black and white) or a colour form. For simplicity, a monochrome system is presented here. Worldwide different regions follow different standards for transmission of TV signals; for example, we have the **American system** followed by most of the American countries, Japan and Philippines. Similarly, the European system is followed by almost the

rest of the world. These systems differ in their standards such as number of frames per second, operating frequency, etc. Table 5.6 summarises some of such differences between these two systems.

Table 5.6 Comparison between European system and American system

Sl. No.	Comparison	European System	American System
1	Operating frequency	50 Hz	60 Hz
2	Channel bandwidth	7 MHz	6 MHz
3	Number of stations	Relatively less	Relatively more
4	Sound signals	Frequency modulated	Frequency modulated
5	Picture signals	Amplitude modulated (VSB system)	Amplitude modulated (VSB system)
6	Frame frequency	25 frames/second	30 frames/second
7	Number of lines	625 lines/frame	525 lines/Frame
8	Inter-carrier frequency	5.5 MHz	4.5 MHz

5.8.1 Television Transmitter

The TV transmitter block diagram shown in Fig. 5.16 uses amplitude-modulation scheme for picture signals and frequency-modulation scheme for sound signals.

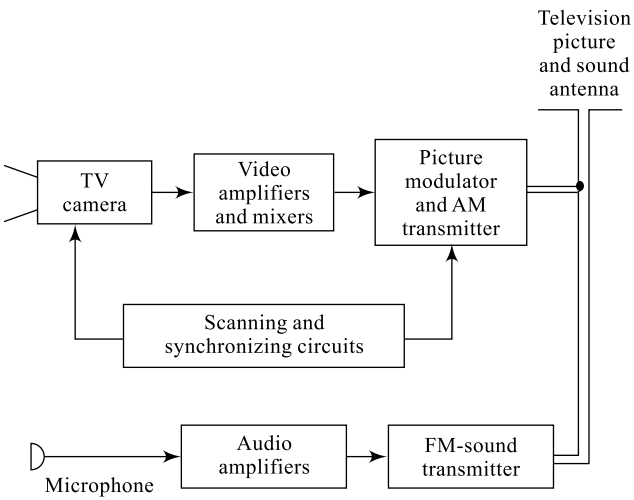


Fig. 5.16 Block diagram of a TV transmitter

The TV camera shown produces the picture information and the microphone produces the sound information. The picture signals are produced by a process called **scanning**; the TV camera scans the object and the corresponding sound signals are recorded using a microphone. In order that a picture motion effect is created for the naked eye, a minimum of 18 frames per second are to be produced. In the above-mentioned systems, 25 or 30 frames per second are produced which is sufficient enough. To avoid flickering motion of the frames, a method called **interlaced scanning** is used; where out of 525

lines, 262½ alternate lines are scanned into odd frames and the other 262½ lines are scanned into even frames. The series of amplifiers used increase the signal level, the modulator modulates the carrier signal, and the synchronising circuits produce necessary synchronisation between audio and video signals. The composite video signal produced is then transmitted into free space by the transmitting antenna.

5.8.2 Television Receiver

In a TV communication system, the TV receiver is responsible for processing the received information back in its original form before delivering it to the destination. A TV receiver is responsible for selecting the desired information signal from a bunch of such signals, then process the signal such that it is noise limited and suitable to be delivered to the destination. The block diagram of TV receiver is shown in Fig. 5.17. The tuner in the receiver selects the desired station frequency and the selected signal is heterodyned in a mixer into an IF value.

The series of amplifiers increase the signal level and the detector circuits reconstruct the information (both audio and video) signal which is then observed on the picture tube. The synchronising circuits are again responsible for maintaining proper synchronisation between the audio and video signals.

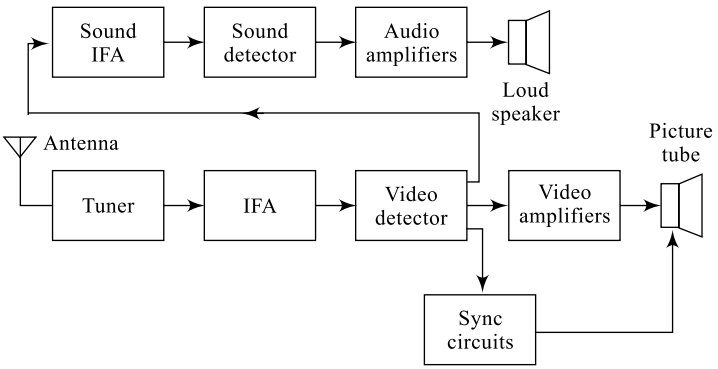


Fig. 5.17 Block diagram of a TV receiver

Summary

- A communication system involves processing the source information, transmitting it over a channel using a transmitter, and on the receiving side receiving, processing and finally delivering it to the destination.
- A signal is mainly characterised by amplitude (A), frequency (f) and phase (φ).
- A communication system includes a source, a transmitter, a channel, a receiver and a destination.
- The length of the antenna required to transmit an unmodulated signal is very large and most of the times, not practically possible.
- The media of transmission between a Tx and Rx can be a twisted pair, a co-axial cable in a wireline communication or free space (air) in a wireless communication.
- A Tx is responsible for processing the information from the source, modulating it and then sending it over the channel to the receiver.
- An Rx is responsible for processing the information received from the Tx, de-modulating it and then delivering it to the destination.
- A digital communication system, in contrast to an analog communication system, includes encoding and decoding the analog signal offering all the advantages of digital systems.

- ➢ Modulation is a process of changing one of the characteristics of the information signal in accordance with the instantaneous amplitude changes of the information signal.
- ➢ Amplitude modulation is a process of changing the amplitude (A) of the information signal in accordance with the instantaneous amplitude changes of the information signal.
- ➢ Frequency modulation is a process of changing the frequency (f) of the information signal in accordance with the instantaneous amplitude changes of the information signal.
- ➢ Phase modulation is a process of changing the phase (φ) of the information signal in accordance with the instantaneous amplitude changes of the information signal.
- ➢ De-modulation is a process of recovering the information signal from the received modulated signal.
- ➢ An envelope detector uses a simple diode to detect an AM signal.
- ➢ To detect an FM signal, first the frequency variations are converted into amplitude variations and then an AM detector is used to recover the information signal.
- ➢ In AM output, the carrier signal can be eliminated forming DSB-SC output and this saves power to be transmitted.
- ➢ In AM output, the carrier signal and one side band can be eliminated forming SSB output and this further saves power to be transmitted.
- ➢ A radio transmitter can employ either a low-level modulation or a high-level modulation.
- ➢ A radio receiver can be either a TRF type or a superheterodyne type.
- ➢ A superheterodyne radio receiver converts the entire range of incoming signal frequencies into IF value.
- ➢ In a superheterodyne radio receiver, the IF value is selected below local oscillator frequency.
- ➢ A radio receiver is characterised by sensitivity, selectivity and fidelity.
- ➢ A TV transmitter uses AM for video and FM for audio signal transmission.
- ➢ A TV receiver also uses the superheterodyning principle offering all the advantages.

Review Questions

1. Comment on the length of the antenna required to transmit an audio signal.
2. Can we transmit a speech signal using an antenna without modulation? Comment.
3. What is the side-band power variation when the signal is (i) unmodulated? (ii) 50% modulated? (iii) 100% modulated?
4. What is the role of a carrier signal in a modulation scheme?
5. A carrier signal $V_c = 25 \sin 2\pi 10^5 t$ is amplitude modulated by an information signal $V_m = 12 \sin 2\pi 10^3 t$. Draw the output waveform and comment.
6. What are the advantages of amplitude modulation?
7. Draw the frequency spectrum of an AM wave and comment on the bandwidth requirement.
8. What are the advantages of frequency modulation?
9. A carrier signal $V_c = 25 \sin 2\pi 10^5 t$ is frequency modulated by an information signal $V_m = 12 \sin 2\pi 10^3 t$. Draw the output waveform and comment.
10. In your own words, explain the role of the channel as a communication media.
11. What are the main advantages of a superheterodyne receiver?
12. Why is the IF value less than the local oscillator frequency?
13. What is image frequency?

14. What is gang tuning? Explain in your own words.
15. In a TV system, what type of modulation is used for audio and video signals? Explain.

Exercise Problems

1. A signal source produces information at 50 kHz. Is it practically possible to transmit this signal using an antenna without modulation?
2. It is required to transmit the speech signal of a VIP using an antenna, but without modulation. Is this possible? Give reasons.
3. The total power in an amplitude-modulated wave is 500 watts. If the carrier is modulated to a depth of 75%, calculate the carrier power.
4. The power radiated by an AM transmitter is 125 percent of the carrier power; calculate the depth of modulation for the carrier wave ($m = 0.707$).
5. An AM transmitter has an unmodulated current of 8 A and it increases by 1.4 A after modulation. Find the percentage modulation of the output wave ($m = 0.87$).
6. A 400-watt carrier is modulated by an audio signal. Calculate the side-band power when $m = 0.5$ and $m = 1.0$.
7. An audio signal of 5 kHz is modulating by a 400-watt, 500 kHz carrier wave. Calculate the side-band frequencies.
8. An AM transmitter has an unmodulated current of 8 A. Find the increase in antenna current when this signal is modulated with $m = 0.5$ and $m = 0.6$
9. An AM wave is represented by the equation below; find all the frequency components contained in it. $v = 150(1 + 0.25\cos 6280t)\cos 2\pi \times 10^6\, t$
10. An AM transmitter has a side-band power 45 watts at 70% modulation. Calculate the total power contained in the AM output wave.
11. A carrier signal $V_c = 25 \sin 2\pi 10^5 t$ is amplitude modulated by an information signal $V_m = 12 \sin 2\pi 10^3 t$. Calculate the modulation index, side-band frequencies and total transmitted power through an antenna of 300 Ω.
12. A carrier signal $V_c = 25 \sin 2\pi 10^5 t$ is frequency modulated by an information signal $V_m = 12 \sin 2\pi 10^3 t$. Calculate the modulation index and bandwidth if the maximum deviation is 75 kHz.
13. A carrier signal $V_c = 50 \sin 2\pi 10^5 t$ is amplitude modulated by an information signal $V_m = 15 \sin 2\pi 10^2 t$. Calculate the modulation index, side-band frequencies and the bandwidth.
14. A FM output is represented by the equation $V_c = 50 \sin (2 \times 10^5 t + 20 \sin 1200t)$. Calculate the modulation index, carrier and information frequencies and the frequency deviation (0.702 kHz, 722 kHz and 20 kHz)
15. A 712 kHz sine wave is amplitude modulated by an information signal of 10 kHz. Calculate the side-band frequencies and the bandwidth. (0.702 kHz, 722 kHz and 20 kHz)
16. A 712 kHz, 9 kW sine wave is amplitude-modulated by an information signal of 10 kHz; the resulting $P_t = 10.125$ kW. This signal is simultaneously modulated by another sinusoidal signal increasing the transmitted power to 10.84 kW; calculate the individual modulation indices and the total modulation index. (0.5, 0.4 and 0.64)

Multiple-Choice Questions

1. In order to transmit information signal over longer distances, the process used is
   (a) modulation (b) de-modulation (c) suppression (d) amplification
2. The transmission of the information signal directly without any modification is called
   (a) modulation (b) baseband transmission
   (c) de-modulation (d) all the above
3. The information signal in a modulation process is called
   (a) modulated signal (b) modulating signal (c) noise signal (d) detected signal
4. The low-frequency signal in a modulation process is called
   (a) modulated signal (b) detected signal (c) noise signal (d) modulating signal
5. The high-frequency signal in a modulation process is called
   (a) modulated signal (b) detected signal (c) noise signal (d) modulating signal
6. The carrier signal in a modulation process is also called
   (a) noise signal (b) modulating signal (c) modulated signal (d) detected signal
7. The length of the transmitting antenna will be very large if the information signal is _____ before transmission.
   (a) directly sent without any modification (b) modulated
   (c) demodulated (d) amplified
8. _____ is the process of modifying one or more characteristics of a carrier signal in a known way in order to transmit the information over a long distance.
   (a) De-modulation (b) Modulation (c) Suppression (d) Amplification
9. _____ is the process of extracting the information signal from the received signal.
   (a) De-modulation (b) Modulation (c) Suppression (d) Amplification
10. Changing the amplitude of the carrier signal with respect to the instantaneous changes in the amplitude of the information signal is known as _____.
    (a) frequency modulation (b) amplification
    (c) rectification (d) amplitude modulation
11. The modulation process for an information signal offers
    (a) small antenna sise (b) reduced noise
    (c) transmission over long distances (d) all the above
12. The transmitter section of the communication system does not contain the
    (a) modulator (b) de-modulator (c) information source (d) all the above
13. The receiver section of the communication system does not contain
    (a) modulator (b) de-modulator (c) destination (d) all the above
14. The transmitter section and the receiver section of the communication system exchange information through a
    (a) modulator (b) demodulator (c) channel (d) noise source
15. The channel in a communication system can be
    (a) air or free space (b) twisted pair (c) co-axial cable (d) all the above
16. The quantisation of analog signal is done in _____ the communication system.
    (a) analog (b) digital (c) both (a) and (b) (d) all the above
17. In an AM system, the carrier signal _____ varies and _____ remains constant.
    (a) frequency, amplitude (b) amplitude, frequency
    (c) noise, amplitude (d) frequency, noise

18. In an AM system, the amplitude of the carrier signal varies according to the instantaneous amplitude of the message signal.
    (a) True (b) False
19. In an AM system, the frequency of the carrier signal varies according to the instantaneous amplitude of the message signal.
    (a) True (b) False
20. In an AM system, the amplitude of the carrier signal varies according to the instantaneous frequency changes in the message signal.
    (a) True (b) False
21. In an AM system, the depth of modulation is given by the equation
    (a) $m = \frac{V_{max} + V_{min}}{V_{max} + V_{min}}$ (b) $m = \frac{V_{max} - V_{min}}{V_{max} - V_{min}}$ (c) $m = \frac{V_{min} - V_{max}}{V_{max} + V_{min}}$ (d) $m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$
22. In an AM system, the depth of modulation can vary from 0 to 100%.
    (a) True (b) False
23. In an AM system, if the depth of modulation exceeds 100% then
    (a) there is no loss of signal (b) there is a loss of signal
    (c) there is no modulation of signal (d) there is no de-modulation of signal
24. In an AM system, if the depth of modulation exceeds 0% then
    (a) there is no loss of signal (b) there is a loss of signal
    (c) there is no modulation of signal (d) there is no de-modulation of signal
25. In an AM system, the total power transmitted is given by
    (a) $P_t = P_C(1 + m^2/4)$ (b) $P_t = P_C/(1 + m^2/4)$ (c) $P_t = P_C(1 - m^2/4)$ (d) $P_t = P_C/(1 - m^2/4)$
26. In an AM system, the total current transmitted is given by
    (a) $I_t = I_c/\sqrt{(1 + m^2/2)}$ (b) $I_t = I_c\sqrt{(1 - m^2/2)}$ (c) $I_t = I_c/\sqrt{(1 - m^2/2)}$ (d) $I_t = I_c\sqrt{(1 + m^2/2)}$
27. In an AM system, the single side-band power transmitted is given by
    (a) $P_{SB} = \frac{m^4}{4} P_c$ W (b) $P_{SB} = \frac{m^2}{2} P_c$ W (c) $P_{SB} = \frac{m^2}{3} P_c$ W (d) $P_{SB} = \frac{m^2}{4} P_c$ W
28. In an AM system, the total side-band power transmitted is given by
    (a) $P_{SB} = \frac{m^4}{4} P_c$ W (b) $P_{SB} = \frac{m^2}{2} P_c$ W (c) $P_{SB} = \frac{m^2}{3} P_c$ W (d) $P_{SB} = \frac{m^2}{4} P_c$ W
29. In an AM system, the total bandwidth needed for transmission is
    (a) $2f_m$ (b) $2(f_m + f_m)$ (c) $2f_c$ (d) infinity
30. In an AM system, if the carrier signal is eliminated then
    (a) there is no transmission of signal (b) there is no power for transmission
    (c) transmitted power is unchanged (d) transmitted power is reduced
31. In an AM system, if the carrier signal is eliminated then
    (a) there is no transmission of signal (b) there is no power for transmission
    (c) transmitted power is unchanged (d) transmitted power is reduced
32. In an AM system with $m = 1$, if the carrier signal is eliminated then ____% of the transmitted power is saved.
    (a) 66.67 (b) 33.33 (c) 55.25 (d) 16.67
33. In an AM system, if only one side band is transmitted then
    (a) there is no transmission of signal (b) there is no power for transmission
    (c) transmitted power is unchanged (d) transmitted power is reduced

34. In an AM system with $m = 1$, if only one side band is transmitted then ____% of the transmitted power is saved.
    (a) 33.33 (b) 66.67 (c) 55.25 (d) 16.67
35. Changing the frequency of the carrier signal with respect to the instantaneous changes in the amplitude of the information signal is known as _____.
    (a) frequency modulation (b) amplification
    (c) rectification (d) amplitude modulation
36. In an FM system, the carrier signal _____ varies and _____ remains constant.
    (a) frequency, amplitude (b) amplitude, frequency
    (c) noise, amplitude (d) frequency, noise
37. In an FM system, the amplitude of the carrier signal varies according to the instantaneous amplitude of the message signal.
    (a) True (b) False
38. In an FM system, the frequency of the carrier signal varies according to the instantaneous amplitude of the message signal.
    (a) True (b) False
39. In an FM system, the amplitude of the carrier signal varies according to the instantaneous frequency changes in the message signal.
    (a) True (b) False
40. In an FM system, the depth of modulation is given by the equation
    (a) $m_f = \beta = \frac{\delta}{f_m}$ (b) $m_f = \beta = \frac{1}{\delta \times f_m}$ (c) $m_f = \beta = \delta \times f_m$ (d) $m_f = \beta = \frac{\delta \times f_m}{2}$
41. In an FM system, the depth of modulation can vary from 0 to >100%
    (a) True (b) False
42. In an FM system, the approximate bandwidth needed for transmission is
    (a) $2(\Delta f - f_m) = 2(1 - \beta) f_m$ (b) $2(\Delta f + f_m) = 2(1 - \beta) f_m$
    (c) $2(\Delta f - f_m) = 2(1 + \beta) f_m$ (d) $2(\Delta f + f_m) = 2(1 + \beta)\ f_m$
43. In an AM system, the number of side bands available for transmission is
    (a) two (b) ten (c) zero (d) infinity
44. In an FM system, the number of side bands available for transmission is
    (a) two (b) ten (c) zero (d) Infinity
45. An angle modulation includes
    (a) AM and FM (b) AM and PM (c) FM and PM (d) AM, FM and PM.
46. In an AM detector a ____ serves as an envelope detector.
    (a) diode (b) transistor (c) UJT (d) FET
47. In an FM detector, frequency changes are first converted into amplitude changes and then an AM detector is used.
    (a) False (b) True
48. The expression for an AM wave is
    (a) $v = V_{\downarrow}c \sin \omega_{\downarrow}c\ t + mV_{\downarrow}c/2[\cos(\omega_{\downarrow}ct - \omega_{\downarrow}m\ t) - \cos(\omega_{\downarrow}c\ t + \omega_{\downarrow}m\ t)$
    (b) $v = V_{\downarrow}c \sin \omega_{\downarrow}c\ t + \mathrm{mV}_{\downarrow}c/2[\cos(\omega_{\downarrow}c\ t - \omega_{\downarrow}m\ t) + \cos(\omega_{\downarrow}c\ t + \omega_{\downarrow}m\ t)$
    (c) $v = A \sin((\omega)_c t + m_f \sin(\omega_m t))$
    (d) none of the above

49. The expression for an FM wave is
    (a) $v = V_{\downarrow}c \sin \omega_{\downarrow}c\, t + \mathrm{mV}_{\downarrow}c/2\, [\cos(\omega_{\downarrow}c\, t - \omega_{\downarrow}m\, t) - \cos(\omega_{\downarrow}c\, t + \omega_{\downarrow}m\, t)$
    (b) $v = A \sin(\omega_c t + m_f \sin(\omega_m t + \omega_c t))$
    (c) $v = A \sin(\omega_c t + m_f \sin(\omega_m t))$
    (d) none of the above
50. Carson's rule is related to
    (a) AM system (b) FM system (c) both (a) and (b) (d) PM system
51. The master oscillator in a radio transmitter is to generate
    (a) carrier signal (b) information signal (c) both (a) and (b) (d) Noise
52. Series of RF amplifiers used in a TRF radio receiver to
    (a) select and amplify the desired signal (b) de-modulate the received signal
    (c) both (a) and (b) (d) none of the above
53. In a TRF radio receiver, design of RF amplifiers is very difficult because their design changes according to the received signal frequency.
    (a) False (b) True
54. In a superheterodyne radio receiver, design of RF amplifiers is very difficult because their design changes according to the received signal frequency.
    (a) False (b) True
55. In a superheterodyne radio receiver, all the received signal frequencies are converted into one common value.
    (a) False (b) True
56. In a superheterodyne radio receiver, all the received signal frequencies are converted into one common value called _____.
    (a) carrier frequency (b) signal frequency
    (c) intermediate frequency (d) none of the above
57. In a superheterodyne radio receiver, the local oscillator frequency is selected above the IF value.
    (a) False (b) True
58. A superheterodyne radio receiver compared to TRF receiver offers good
    (a) selectivity (b) sensitivity (c) fidelity (d) none of the above
59. In a television system, _____ is used for audio signal and ____ is used for video signal.
    (a) AM scheme, FM scheme (b) AM scheme, PM scheme
    (c) FM scheme, AM scheme (d) FM scheme, PM scheme
60. In a TV receiver, a mixer is used to mix local oscillator and signal frequencies; the output of a mixer contains the sum and difference of the two.
    (a) False (b) True

Linear Integrated Circuits

6

Goals and Objectives

Upon completion of this chapter, the reader is expected to

- Recall all the basic concepts of transistors, biasing and operating point from Chapter 3
- Understand the basic block diagram of an op-amp
- Understand the role and importance of each unit of an op-amp
- Understand the analysis of a basic differential amplifier
- Understand the performance of a basic differential amplifier
- Understand the op-amp performance parameters like CMMR, gain, input/output impedances, slew rate, etc.
- Understand the various performance parameters of an op-amp
- Understand the working and design of op-amp applications like inverter, non-inverter, buffer, adder, subtractor, etc.
- Understand the working and design of op-amp applications like integrator, differentiator, instrumentation amplifier, comparator, etc.
- Understand the working and design of op-amp applications like Schmitt trigger, multivibrators, waveform generator, etc.
- Understand the advantages and working of different forms of active filters
- Compare different types of filters and choose the best suitable for an application
- Feel confident of taking up the next course in linear ICs

6.1 INTRODUCTION

Solid-state devices replacing vacuum-tube devices revolutionised the electronics industry offering innumerable advantages. One such advantage is that these devices and circuits being very compact occupy very less space. Later, these circuits are fabricated on a single silicon wafer resulting in very compact Integrated Circuits (ICs). Integrated Circuits can be broadly classified into two types: linear ICs and digital ICs. Digital ICs generally respond to two types of signals, logic low and 'logic high'. This class of ICs are discussed in Chapter 7. On the other hand, linear ICs respond to linear or analog or time-varying signals. An operational amplifier (op-amp), timer, phase-locked loop (PLL) are some examples of linear ICs. An op-amp is a direct-coupled, very high-gain differential amplifier with high input impedance and low output impedance. This chapter deals mainly with op-amp characteristics, important applications, timer IC-555 working, its useful applications and PLL IC-565 block diagram and some of its applications. Typical applications of the op-amp are amplitude scale changers (voltage amplitude and polarity), comparators, instrumentation amplifier, oscillators, filter circuits and many types of instrumentation circuits. An op-amp contains a number of differential amplifier (DA) stages to achieve a very high voltage gain.

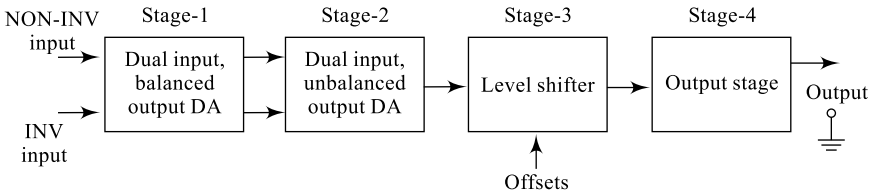


Fig. 6.1 Block diagram of op-amp

An op-amp is a direct-coupled, high-gain difference amplifier containing four stages as shown in Fig. 6.1. Stage-1 is a low-gain double-ended differential amplifier (Section 6.2) that controls a large number of op-amp parameters (Section 6.3) such as CMMR, input impedance, bandwidth, etc. Stage-2 is a high-gain single-ended differential amplifier (Section 6.2) that controls a number of op-amp parameters (Section 6.3) such as drift, stability, offset voltages and currents, etc. The output of Stage-1 is directly coupled to Stage-2 and this results in loss of signal reference (normal problem in direct-coupled amplifiers); hence, Stage-3 is a level translator that re-introduces dc level into the signal. An emitter follower with a constant-current source is used to clamp the signal to the required level. Most op-amps even use offset corrections at this stage. Stage-4 is an output stage used as a driver stage; this stage will be responsible for providing sufficient driving capability and low output impedance to the op-amp. The IC-555 timer is a highly versatile linear IC offering varieties of applications such as multivibrators, capacitance meters, ramp generators, etc. It consists of two comparators, a 3R network and a flip-flop (to be introduced in Chapter 7). Similarly, IC-565 is another important linear IC called Phase-Locked Loop (PLL), used for varieties of applications such as frequency multiplication, frequency division, different de-modulation circuits, etc. It consists of a phase detector, a Voltage Controlled Oscillator (VCO) and a Low-Pass Filter (LPF).

6.2 DIFFERENTIAL AMPLIFIER CIRCUIT

A differential amplifier (DA) is the basic building block of an op-amp and decides the major performance of the op-amp. It consists of two emitter-coupled transistors as shown in Fig. 6.2; the

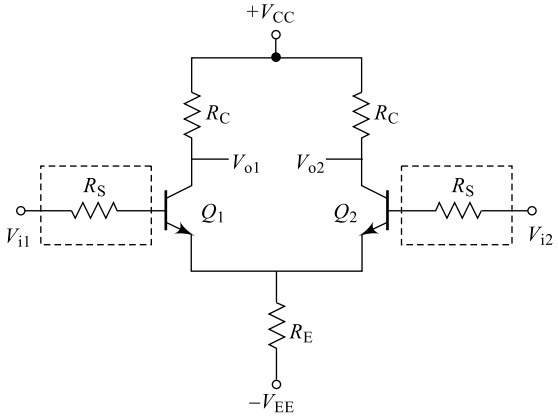


Fig. 6.2 Differential amplifier

transistors necessarily need to be identical and even a small difference in the transistors affects the performance of the op-amp to a greater extent. Use of Field Effect Transistors (FETs, to be discussed in Chapter 10) instead of BJT improves the device performance greatly. Commercially, both forms of op-amps are available and FET input op-amps are more popular. The differential amplifier uses two dc supply sources V_{CC} and V_{EE} in order to establish the operating point for the BJTs. R_S represents the supply source resistance. The emitter resistor R_E, when replaced by a current source, improves the performance of the device greatly. The circuit consists of two inputs V_{i1} and V_{i2} and the difference between these two inputs will be amplified at the output; hence, the name *difference amplifier*. Any common-mode signal between the two input sources will be completely rejected by the op-amp and a measure of this ability is an important parameter for the op-amp. The difference amplifiers can have single-ended input or double-ended input; similarly, the output can be either single-ended or double-ended.

6.2.1 Single-Ended Input

Single-ended input operation results when one of the input signals is connected to one input (either V_{i1} or V_{i2}) with the other input connected to ground. Figure 6.3(a) shows the signal connected for a single-ended input operation; here, the input is applied to the base of Q_1 while the other input (the base of Q_2 to ground). The resulting output has an opposite polarity as the applied input signal; hence, V_{i1} is termed **inverting input** represented by a minus (–) sign. Similarly, the input is applied to the base of Q_2 while on the other input (the base of Q_1 to ground), the resulting output has a polarity that is same as the applied input signal; hence V_{i2} is termed **non-inverting input**, represented by a plus (+) sign.

6.2.2 Double-Ended (Differential) Input

In contrary to a single-ended input, if the input is applied to both the input terminals V_{i1} and V_{i2}, this results in a double-ended operation. Figure 6.3 (b) shows the arrangement where two inputs are applied separately to the two input terminals and this forms a differential double-ended input operation. Also, a common input source can be connected between the two input terminals resulting in a common-mode double-ended input operation as shown in Fig. 6.3(b). But it is important to note that a good DA should offer zero gain to common-mode input signals.

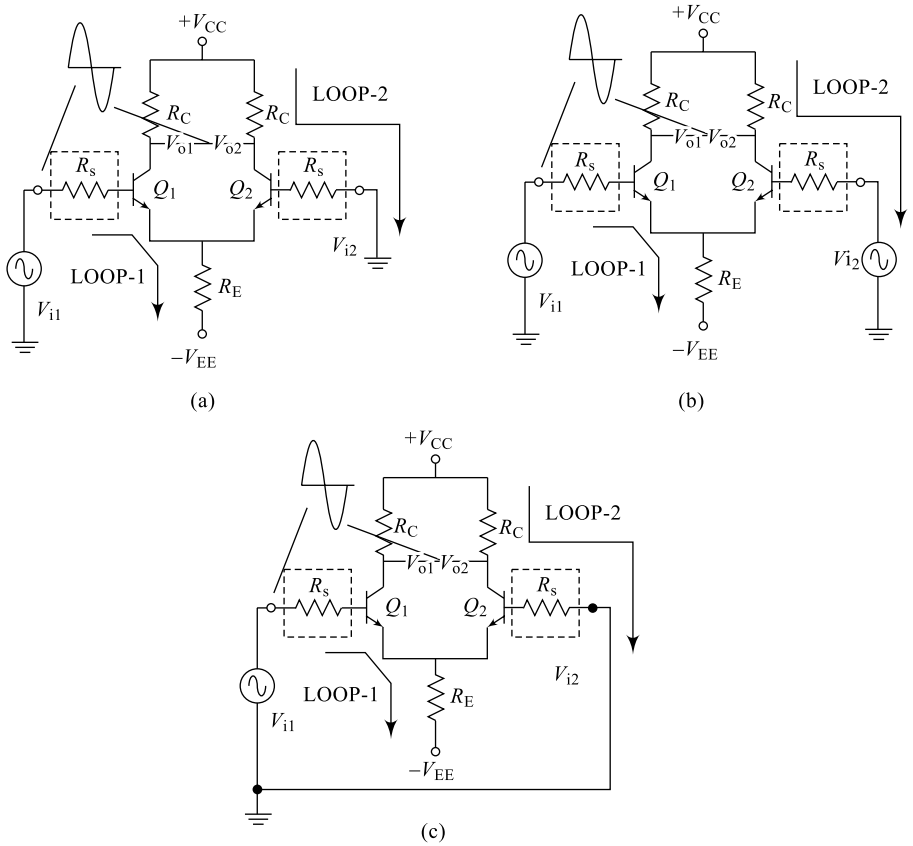


Fig. 6.3 (a) Single-ended DA (b) Double-ended (differential) DA (c) Double-ended (common) DA

6.2.3 Double-Ended Output

Whereas the operation discussed so far has a single output, the op-amp can also be operated with opposite outputs. An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Figure 6.4(a) shows a single-ended input with a double-ended output, where output is measured between one output terminal and the ground. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Figure 6.4(b) shows the same operation with a single output measured between output terminals (not with respect to ground). This difference output signal is also referred to as a floating signal since neither output terminal is the ground (reference) terminal. Notice that the difference output is twice as large as either or because they are of opposite polarity and subtracting them results in twice their amplitude [e.g. Figure 10.7 shows a differential input, differential output operation. The input is applied between the two input terminals and the output taken from between the two output terminals. This is fully differential operation.

6.2.4 Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 6.3(c). Ideally, the two inputs are equally amplified, and since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0 V output. Practically, a small output signal will

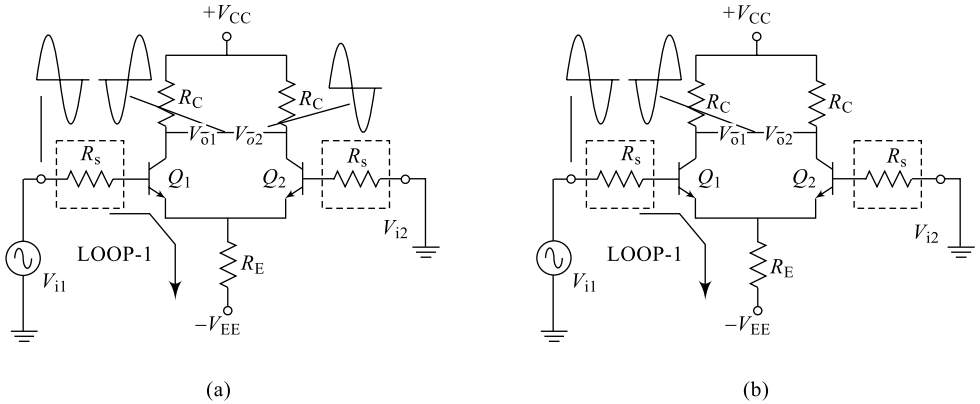


Fig. 6.4 (a) Single-ended i/p, double-ended o/p DA (b) Single-ended i/p, single-ended o/p DA

be present resulting in a nonzero common-mode gain and this is mainly because of a small mismatch between the transistors.

Table 6.1 Popular linear ICs at a glance

Sl. No.	IC	Manufacturer	Applications
1	μA-741	Fairchild Corporation	Rectification, Filtering, Regulation, Amplification, Signal generation, etc.
2	NE/SE-555	National Semiconductors/Signetics Corporation	Timing applications, Multivibrators, Ramp generator, Capacitance meters, etc
3	NE/SE565	National Semiconductors/Signetics Corporation	Frequency synthesis, FSK modulation and demodulation, etc.

6.2.5 Common-Mode Rejection

A significant feature of a differential connection is that the signals that are opposite at the inputs are highly amplified, whereas those that are common to the two inputs are only slightly amplified—the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide attenuation of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature is referred to as common-mode rejection.

One of the most important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs while only slightly amplifying signals that are common to both inputs. An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs. Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common-mode rejection as described by a numerical value called the **Common-Mode Rejection Ratio (CMRR)**.

It should be clear that the desired operation will have very large differential gain and very small common-mode gain. That is, the signal components of opposite polarity will appear greatly amplified at the output, whereas the signal components that are in phase will mostly cancel out so that the common-mode gain is very small. Ideally, the value of the CMRR is infinite. Practically, the larger the value of CMRR, the better the circuit operation. CMRR is expressed in dB and is one of the most important characterising parameters of the op-amp.

6.2.6 Differential Amplifier DC Analysis

The dc equivalent circuit of Fig. 6.2 can be drawn as in Fig. 6.5 where the ac sources are shorted and replaced by their internal source impedances R_S which is small enough. Also, it is essential that transistors be identical; any mismatch leads to variations in op-amp parameters.

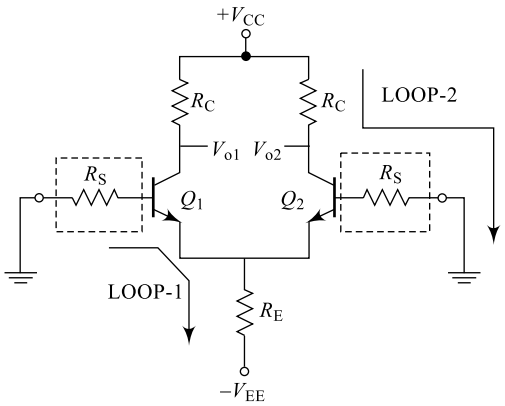


Fig. 6.5 The dc equivalent circuit of a double-ended DA

Applying KVL to the input loop-1, we can write

$$-R_S I_B - V_{BE} - R_E(2I_E) + V_{EE} = 0 \tag{6.1}$$

but $I_B \cong I_E/\beta$, this is $\because I_C \cong I_E$

Substituting and re-arranging the terms, we get

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \dfrac{R_S}{\beta}} = \frac{V_{EE} - V_{BE}}{2R_E} \tag{6.2}$$

$$I_{EQ} = \frac{V_{EE} - V_{BE}}{2R_E}; \quad \because \frac{R}{\beta} << 2R_E \tag{6.3}$$

Equation (6.3) clearly indicates that selection of I_E is dependent on R_E and V_{EE}; it is independent of R_C, the collector resistor.

Similarly, applying KVL to the output loop-2, we can write

$$-R_C I_C - I_C R_C - R_S I_B + V_{CC} = 0 \tag{6.4}$$

$$-R_C I_C - V_C - R_S I_B + V_{CC} = 0;$$

Neglecting $R_S I_B$, drop across R_S, we can write

$$V_C = V_{CC} - I_C R_C. \tag{6.5}$$

Neglecting drop across R_S, we can write $V_E = -V_{BE}$

Now, $V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (-V_{BE})$

$$\therefore \quad V_{CEQ} = V_{CC} + V_{BE} - I_C R_C \tag{6.6}$$

Equations (6.3) and (6.6) represent the operating point for the DA.

6.2.7 Differential Amplifier AC Analysis

The ac analysis and the ac equivalent circuit of a DA are beyond the scope of this text; hence, only the relevant equations are produced here for reference purpose.

The **voltage gain** (A_d) is defined as the ratio of output voltage to the input differential voltage;

$$A_d = \frac{V_o}{V_{id}} \tag{6.7}$$

$$V_o = \frac{R_C}{r_e (V_{i1} - V_{i2})} \tag{6.7(a)}$$

$A_d = \dfrac{R_C}{r_e}$ where r_e is the ac emitter resistance. (6.8)

1. Differential Input Resistance (R_{i1})

It is defined as the equivalent resistance measured between one input terminal and the ground (other input terminal will be grounded).

$$R_{i1} = 2 r_e \beta_{ac} \tag{6.9(a)}$$

Similarly, $$R_{i2} = 2 r_e \beta_{ac} \tag{6.9(b)}$$

Output resistance (R_{O1}): $R_{O1} = R_{O2} = R_C$ (6.10)

Common-mode Rejection Ratio (CMRR): $\text{CMRR} = \dfrac{A_d}{A_C}$ (6.11)

where A_d is the differential mode gain and A_C is the common-mode gain.

2. Use of Constant-Current Source

A good differential amplifier has a very large difference gain which is much larger than the common-mode gain. The common-mode rejection ability of the circuit can be considerably improved by making the common-mode gain as small as possible (ideally, 0). This can be done by using a constant-current source in place of emitter resistor R_E as indicated in Fig. 6.6. This provides a large value of resistance from the common emitter to ac ground. The major improvement of this circuit is that use of constant-current source offers much larger ac impedance. Transistor Q_3 along with resistances R_1, R_2 and R_3 forms the constant-current source offering all the advantages.

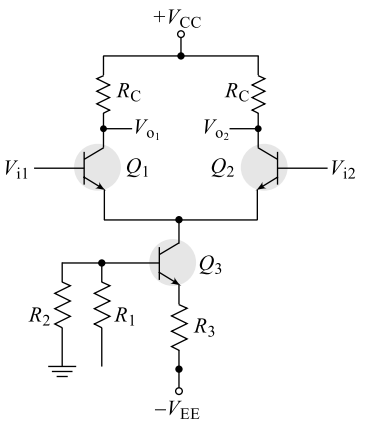
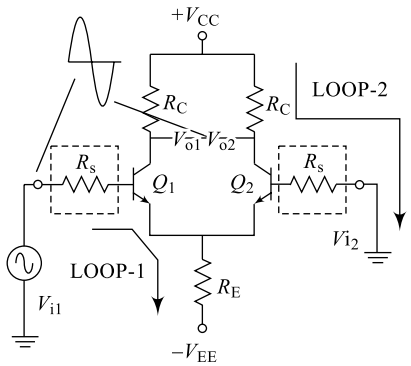
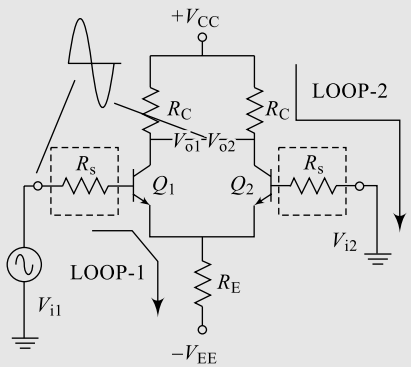
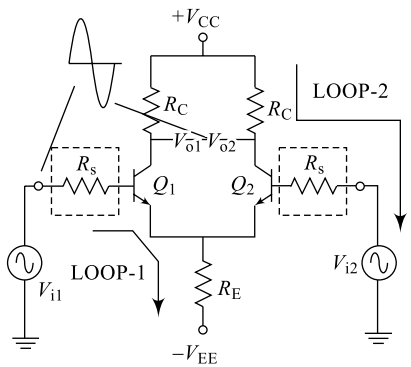
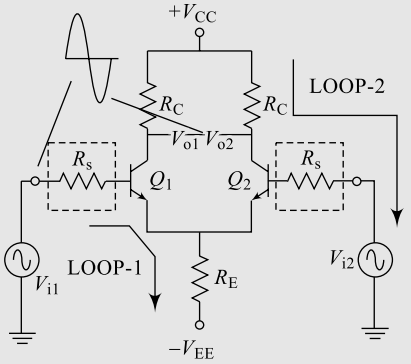


Fig. 6.6 DA with a constant-current source

Table 6.2 Different forms of differential amplifiers (DAs)

Sl. No.	DA	Circuit Diagram	ac Governing Equations
1	Single-input balanced-output DA ***[input to either V_{i1} or V_{i2} and Output between two collectors]***		**1.** $A_d = \dfrac{R_C}{r_e}$ **2.** $R_{i1} = R_{i2} = 2\beta_{ac} r_e$ **3.** $R_{o1} = R_{o2} = R_C$
2	Single-input un-balanced-output DA ***[input to either V_{i1} or V_{i2} and output between one collector and ground]***		**1.** $A_d = \dfrac{R_C}{2r_e}$ **2.** $R_{i1} = R_{i2} = 2\beta_{ac} r_e$ **3.** $R_o = R_C$
3	Dual-input balanced-output DA ***[input to both V_{i1} and V_{i2} and output between two collectors]***		**1.** $A_d = \dfrac{R_C}{r_e}$ **2.** $R_i = 2\beta_{ac} r_e$ **3.** $R_{o1} = R_{o2} = R_C$

4	Dual-input un-balanced-output DA ***[input to both V_{i1} and V_{i2} and Output between one collector and ground]***		1. $A_d = \frac{R_C}{2r_e}$ 2. $R_i = 2\beta_{ac} r_e$ 3. $R_o = R_C$

All the above circuits have the same set of dc analysis governing equations given by

$$I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2_{RE} + \frac{R_{in}}{\beta_{dc}}} \quad \textbf{and } V_{CE} = V_{CEQ} = V_{CC} + V_{BE} - R_C I_{CQ}$$

3. Basic Op-Amp

An operational amplifier (op-amp) is a very-high-gain amplifier having very high input impedance typically of the order of a few mega-ohms and low output impedance. The basic circuit is made using a difference amplifier having two inputs named INV and NON-INV inputs and at least one output. The basic block diagram of an op-amp is shown in Fig. 6.1 where the first two blocks are the differential amplifiers; the first stage is a double-ended differential amplifier while the second stage is a single-ended differential amplifier. The third stage is a level translator which is responsible for dc restoring; the lost reference due to direct coupling is re-inserted in this stage by using circuits like clampers. Offset corrections are also part of this stage. The fourth (output) stage is a buffer stage, which is responsible for increasing the driving capacity of the device.

Figure 6.7 shows a basic op-amp symbol and an example of commercially available IC package unit µA-741. µA-714 is another commercially available package with FETs in the first DA stage and this offers still better performance as compared to BJT input DA; this can be seen with the typical values provided for each op-amp parameter. As discussed earlier, the plus input produces an output that is in phase with the signal applied, whereas an input to the minus input results in an opposite-polarity output. Pin2—Inverting input, Pin3—Non-Inverting input, Pin4—Negative power supply, Pin5—Positive power supply, Pin6—Output, and Pins 1 and 5—Offset adjustment pins.

6.3 OP-AMP CHARACTERISTICS

It is very important to become familiar with the performance parameters of the op-amp before taking up any of its practical applications. Some of the important performance parameters are listed in this section alongwith their typical values for µA-741 and µA-714 op-amps.

1. Input Bias Current (i_b)

Under balanced conditions (when $V_{i1} = V_{i2}$, the resulting $V_O = 0$), the current drawn by the input terminals should be ideally zero. But in practice, a small input base current (i_{b1} and i_{b2}) always flows

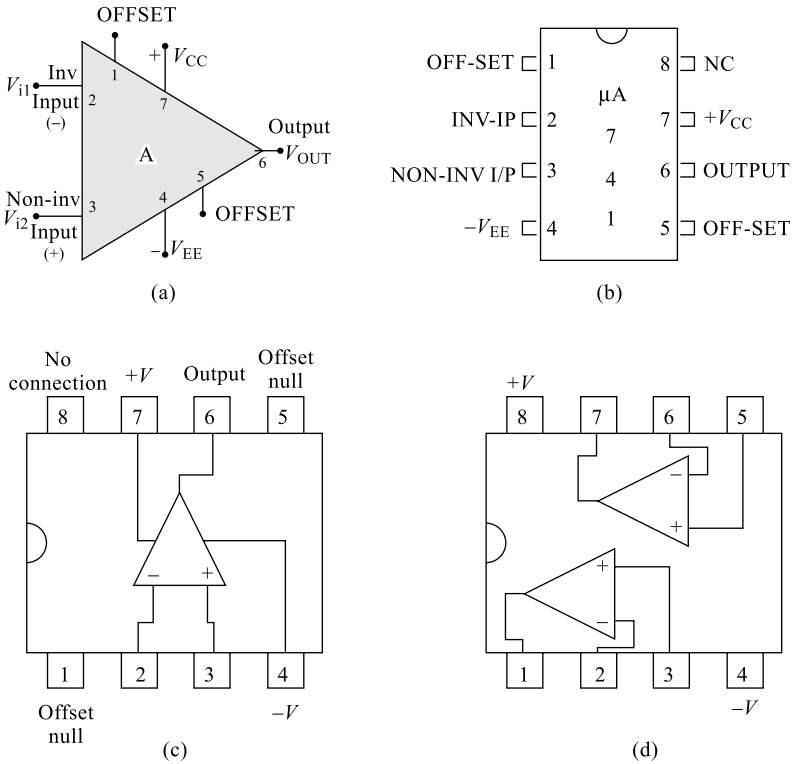


Fig. 6.7 (a) Op-amp symbol (b) Op-amp pin diagram (c) 8-pin DIP op-amp IC (d) 8-pin DIP dual op-amp IC

through each input terminal as indicated in Fig. 6.8(a) and the average of these two currents is called the input bias current.

$$i_b = \frac{i_{b1} + i_{b2}}{2} \tag{6.12}$$

For an ideal op-amp, this value should be zero since both $i_{b1} = i_{b2} = 0$ because of high input impedance, but typically for μA-741, $i_b = 500$ nA and for μA-714, its value is $i_b = 7$nA.

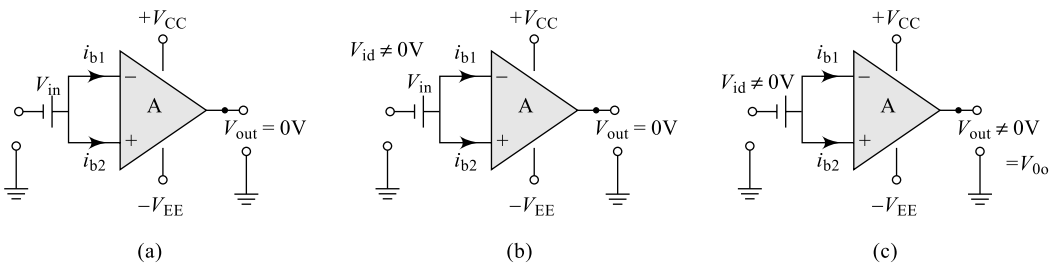


Fig. 6.8 (a) Input-bias current (b) Input offset voltage (c) Output offset voltage

2. *Input Offset Current (I_{iO})*

It is the difference between the two base currents under balanced condition.

$$I_{iO} = i_{b1} \sim i_{b2} \tag{6.13}$$

For an ideal op-amp, this value should be zero since both $i_{b1} = i_{b2} = 0$, but typically for μA-741, i_b = 200 nA and for μA-714, its value is $i_b = 6$ nA.

3. Input Offset Current Drift (dI_{iO}/dT)

It is the defined as the rate of change of input offset current with respect to device temperature T. For an ideal op-amp, this value should be zero since ideal $I_{iO} = 0$.

4. Input Offset Voltage (Vi_O)

In an ideal op-amp, when the two input terminals are at the same potential ($V_{id} = 0$), the output V_O should be zero as indicated in Fig. 6.8(b); but in practice, it is not true. In order to make $V_O = 0$, a small amount of non-zero V_{id} should be applied at the input terminals and it is called the input offset voltage.

$$V_{iO} = V_{i1} \sim V_{i2} \tag{6.14}$$

For an ideal op-amp, this value should be zero since both $V_{i1} = V_{i2} = 0$, but typically for μA-741, V_{iO} = 6 mV and for μA-714, its value is V_{Io} = 150 μV.

5. Input Offset Voltage Drift (dVi_O/dT)

It is the defined as the rate of change of input offset voltage with respect to device temperature T. For an ideal op-amp, this value should be zero since ideal $V_{iO} = 0$.

6. Output Offset Voltage (V_{Oo})

In an ideal op-amp, when the two input terminals are at the same potential ($V_{id} = 0$), the output V_O should be zero as indicated in Fig. 6.8(c); but in practice it is not true. The small amount of nonzero output V_O when $V_{id} = 0$ at the input terminals is called the output offset voltage. An output offset voltage will also result due to any difference in dc bias currents at both inputs. Since the two input transistors are never exactly matched, each will operate at a slightly different current. For an ideal op-amp, this value should be zero since both common-mode gains for an op-amp should be zero.

7. Input Resistance (R_i)

Two input resistances can be defined for an op-amp:

(a) Differential Input Resistance (R_{id}) It is the resistance measured between one of the input terminals and the ground with the other terminal being grounded.

(b) Common-Mode Input Resistance (R_{iC}) It is the resistance measured between the two input terminals directly. R_i will be very high in the order of a few 100s of kΩ and approaches even 10^{12}Ω for op-amps with FET input DAs.

For an ideal op-amp, this value should be infinity, but typically for μA-741, R_i = 2 MΩ and for μA-714, its value is R_i = 100 MΩ.

8. Input Voltage Swing

It is the maximum common-mode voltage that can be applied at the input of op-amp with the device working in the linear region. Generally, this value is dependent on the supply voltages and is around 30% of supply voltages.

9. Output Voltage Swing

It is the maximum value of output voltage that is available with the device working in the linear region. Even this value is also dependent on the supply voltages and is around 90-95% of supply voltages.

10. Open Loop Voltage Gain (A_{VO})

It is the ratio of change in output voltage to a corresponding change in differential input voltage defined for dc conditions.

$$A_{Vo} = \frac{\Delta V_o}{\Delta V_{id}} \tag{6.15}$$

For an ideal op-amp, this value should be infinity, but typically for μA-741, $A_{VO} = 10^5$ or more and for μA-714, its value is even more. A_{VO} is a function of frequency; at $f = 0$, it is maximum and falls off with frequency.

11. Virtual Ground Concept

In an op-amp, the input voltage and the output voltage are limited by the supply voltages. Also, for an op-amp, the ideal open-loop voltage gain should be infinity. Considering Eq. (6.15), for $A_{VO} \simeq \infty$, it can be written that $V_{id} = 0$ and this implies that $V_{i1} = V_{i2}$. If one of these inputs is physically connected to zero, then the potential at other input will be zero; and this is called virtual-ground concept.

Compared to input and output voltages, the value of V_{id} is very small and may be considered as approximately 0 V. Note that although it is not exactly 0 V, at the amplifier input there exists a virtual short-circuit or virtual ground. The concept of a virtual short implies that, there is no current through the amplifier input terminal to ground. This is supported by the fact that the device input impedance is very high and no current flows through the *i/p* terminals.

12. Common-Mode Rejection Ratio (CMRR)

An ideal op-amp should offer infinite gain for differential input signals ($A_d = \infty$ and $A_c = 0$) and zero gain for common-mode signals. But, in practice, neither $A_d = \infty$ nor $A_c = 0$ and hence, a figure of merit called CMRR is defined that speaks about the ability of an op-amp to reject all common-mode signals, amplifying all differential-mode signals to maximum extent. Thus, CMRR is defined as the ratio of differential-mode gain to common-mode gain; expressed in dB.

$$\text{CMRR} = \frac{A_d}{A_c} \tag{6.16}$$

For an ideal op-amp, this value should be infinity, but typically for μA-741, CMRR = 90 dB and for μA-714, its value is CMRR = 120 dB.

13. Power Supply Rejection Ratio (PSRR)

An ideal op-amp should offer zero input offset voltage V_{io}, but in practice, it is always nonzero and this V_{io} is sensitive to supply voltage changes. The rate of change of input offset voltage with respect to changes in supply voltages V_{CC} or V_{EE} is called PSRR. It is also termed Supply Voltage Rejection Ratio (SVRR) or Power Supply Sensitivity (PSS) and expressed in μV/V or dB.

$$\text{PSRR} = \text{SVRR} = \text{PSS} = \frac{\Delta V_{io}}{\Delta V_{CC}} \mu \frac{V}{V} \tag{6.17}$$

For an ideal op-amp, this value should be zero since V_{io} ideally is zero, but typically for μA-741, PSRR = 150 μV/V and for μA-714, its value is PSRR = 6.31 μV/V.

14. Bandwidth

Two bandwidths can be defined here for an op-amp:

(a) f_U, the Unity Gain Bandwidth This bandwidth corresponds to a frequency at which the open-loop gain of the system crossesover the unity gain (0 dB line). We know A_{VO} is a function of frequency and falls off with increasing frequency as indicated in Fig. 6.9. The unity gain bandwidth f_U corresponds to a single frequency value.

(b) f_P, Full Power Bandwidth This bandwidth corresponds to a frequency at which the open-loop gain of the system equals $0.707A_{VO}$ (corresponds to 3 dB frequency) and is as indicated in Fig. 6.9. The unity gain bandwidth f_U corresponds to a single frequency value.

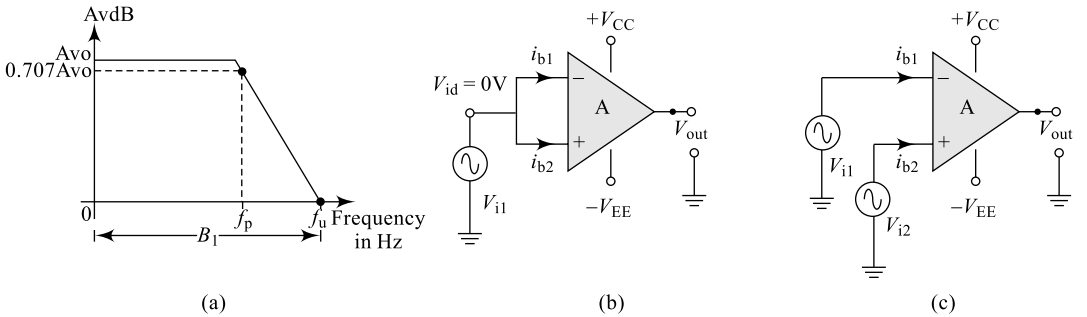


Fig. 6.9 (a) Bandwidth (b) Common-mode gain (c) Differential-mode gain

15. Slew Rate (SR)

Another very important parameter of the op-amp is its slew rate which speaks about the ability of the device to respond to high-frequency input signals. It is defined as the maximum rate of change of output voltage per unit time and expressed in V/μS.

$$\text{SR} = \left.\frac{dV_o}{dt}\right/_{\text{max}} \text{V/μS} \tag{6.18}$$

SR changes with change in voltage gain and is normally specified for unity gain and it is an indication of full power bandwidth. The SR provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal. If the input changes at a rate greater than the slew rate then the output would not be able to change fast enough and would not vary over the full range expected, resulting in signal clipping or distortion. For an ideal op-amp, this value should be infinity, but typically for μA-741, SR = 0.5 V/μS and for μA-714, its value is SR = 12 V/μS. Practical op-amps with SRs from 0.1 V/μS to well above 1000 V/μS are available; for example, for μA-771, SR = 13 V/μS; LF-751, SR = 13 V/μS; MC-34001, SR = 13 V/μS; LM-318, SR = 70 V/μS and LH-0063C, SR = 6000 V/μS. SR is caused by current limiting and the saturation of internal stages of op-amp. In other words, at high frequencies the internal capacitor charging rate prevents output from changing simultaneously with the input.

Slew Rate (SR) Equation

SR is very important frequency related parameter of the op-amp which speaks about the ability of the device to respond to high frequency input signals. For example, a SR of 1 V/μS means that the output rises or falls at no faster than 1 V every μS time. Since SR is specified for unity gain, let us consider a voltage follower:

$$V_i = V_O = V_P \sin \omega t$$

The rate of change of output voltage is

$$\frac{dV_o}{dt} = V_p\, \omega \cos \omega t \tag{6.19}$$

The maximum rate of change of output occurs at cos $\omega t = 1$ and hence,

$$\text{SR} = \frac{dV_o}{dt}\Big/\text{max} \text{ at } \cos \omega t = 1$$

$$\text{SR} = V_P\ x\omega = V_P(2\pi f)$$

$$\text{SR} = \frac{V_P(2\pi f)}{10^6}\text{V/}\mu\text{S} \tag{6.20}$$

Equation (6.20) clearly indicates that SR is dependent on the peak value of the signal and the full power bandwidth f_P. The maximum frequency at which an op-amp may operate depends on both the bandwidth (BW) and slew rate (SR) parameters of the op-amp.

16. Characteristics of an Ideal Op-Amp

An ideal op-amp has the following characteristics:

- Infinite common-mode Rejection Ratio (CMRR = ∞)
- Infinite slew rate (SR = ∞)
- Infinite input impedance ($Z_i = \infty$)
- Infinite bandwidth (f_P or $f_U = \infty$)
- Infinite open loop-gain ($A_{VO} = \infty$)
- Zero output impedance ($Z_O = 0$)
- Zero offsets (both *V* and *I*)
- Zero power-supply rejection ratio (PSRR = 0)

6.4 OP-AMP SPECIFICATIONS

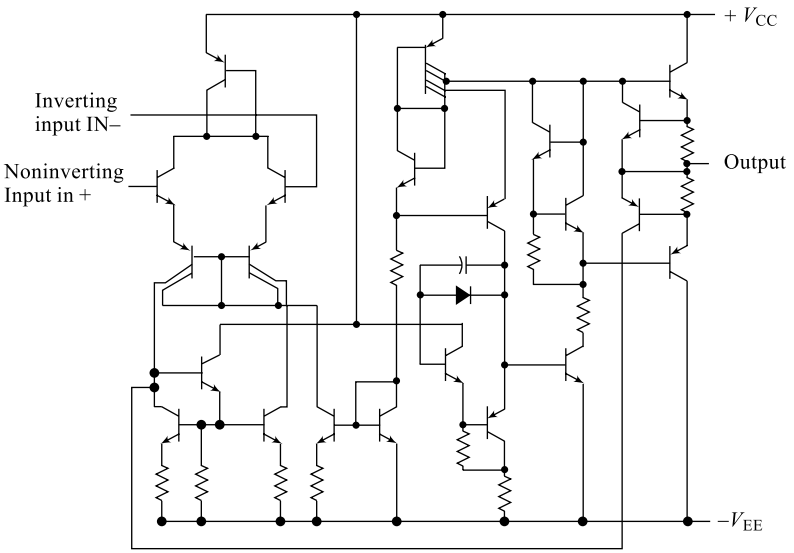


Fig. 6.10 Internal circuit of op-amp μA-741

Table 6.3 Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	uA741M	uA741C	Unit
Supply voltage V_{CC+} (See Note 1)	22	18	V
Supply voltage V_{CC-} (See Note 1)	–22	–18	V
Differential input voltage (see Note 2)	± 30	± 30	V
Input voltage any input (see Notes 1 and 3)	± 15	± 15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}	± 0.5	± 0.5	V
Duration of output short-circuit (see Note 4)	unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)	500	500	mW
Operating free-air temperature range	–55 to 125	0 to 70	°C
Storage temperature range	–65 to 150	–65 to 150	°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds FH, FK, J, JG, or U package	300	300	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds D, N, or P package		260	°C

Notes:

1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA741M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J and JG package, uA741M chips are alloy mounted, uA741C chips are glass mounted.

6.5 OP-AMP EQUIVALENT CIRCUIT

Figure 6.10 represents a simplified, internal circuit of a typical MA 741 op-amp. The equivalent circuit of an op-amp can be very useful in analysing any application built around the op-amp. Also, in analszing the basic operating principles, effect of feedback, etc. the equivalent circuit is very useful. As shown in Fig. 6.11, it consists of Thevenin's equivalent voltage source AV_{id} in series with the Thevenin's equivalent output impedance. Z_{in} is the equivalent input impedance seen between the input terminals.

Op-Amp Applications

An op-amp can be used in varieties of applications such as signal inversion, signal amplification, buffering, signals summing, signal integration, differentiation, signal multiplication, signal generation, signal conversion and many more. The op-amp can be connected in a large number of circuits to provide various operating characteristics and mainly in two different forms: the open-loop (no feedback) configuration and the closed-loop (with feedback) configuration. However, the concept of feedback is discussed in Chapter 4. In the following sections, a few of the most commonly used applications of the op-amp will be discussed.

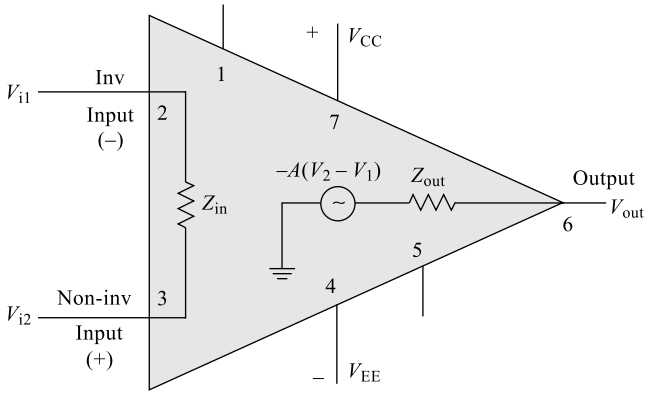


Fig. 6.11 Op-amp equivalent circuit

6.6 OP-AMP INVERTER

6.6.1 Open-Loop Op-Amp Inverter

The inverter, or the inverting amplifier, is one of the most widely used constant-gain amplifier op-amp circuit and is as shown in Fig. 6.12. In the inverter without the feedback shown in Fig. 6.12 (a), R_S represents the source resistance; V_{id} is the differential mode input signal and A is the amplifier open loop gain. Single-ended input is applied to the circuit; V_1 is connected with input through R_S and V_2 is connected to ground.

We have $$A = \frac{V_o}{V_{id}} = \frac{V_o}{V_2 - V_1}$$

i.e. $$V_O = A(V_2 - V_1) = A(0 - V_1) = -AV_1 \tag{6.21}$$

The negative sign in Eq. (6.21) indicates here that output is phase inverted from input and it is also indicated in the input–output waveforms of Fig. 6.12(c).

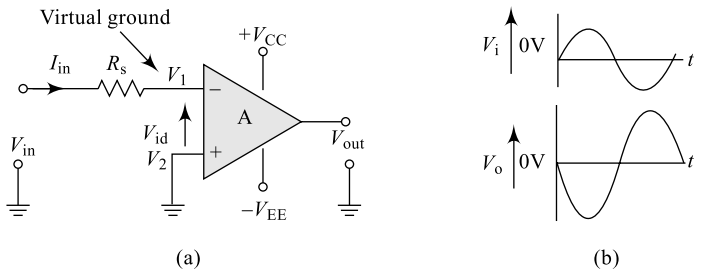


Fig. 6.12 (a) Op-amp inverter (open loop) (b) I/O Waveforms

Example 6.1

For the op-amp inverting amplifier shown in Fig. 6.13, find the output voltage if the input is a sinusoidal signal of 10 mV peak.

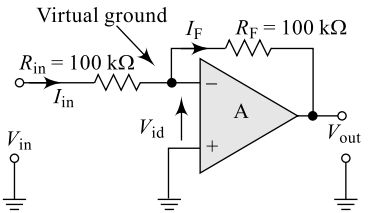


Fig. 6.13 Op-amp inverting amplifier for Example 6.1

Solution We have gain for an inverting amplifier given by Eq. (6.26) as

$$A_F = -\frac{V_o}{V_{in}} = -\frac{R_F}{R_{in}}$$

$$A_F = -\frac{100\,K}{10\,K} = 10$$

Hence, $V_O = -V_{in} \times A_F$

$$V_O = -10\ mV \times 10 = 100\ mV$$

6.6.2 Closed-Loop Op-Amp Inverter

An open-loop inverter can be converted in to a closed-loop one by adding a feedback resistor R_F as shown in Fig. 6.14 (a) and this offers very good stability to the circuit and minimises the output noise level. Once again, a single-ended input is applied to the circuit; input is applied to V_1 through R_{in}, V_2 is connected to ground and R_S, the source resistance, is neglected for simplicity (in comparison with other resistances). The negative feedback offers many advantages such as increased bandwidth, input impedance, reduced output impedance, etc.

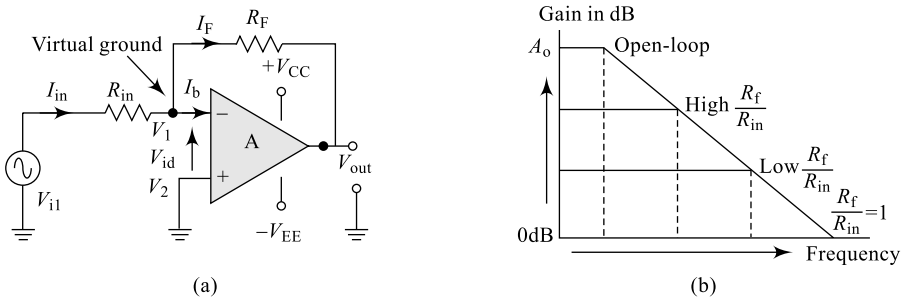


Fig. 6.14 (a) Op-amp inverter (closed loop) (b) Inverter frequency response

Applying Kirchhoff's Current Law (KCL) to the input node V_1, we can write

$$I_{in} = I_F + I_b \tag{6.22}$$

But, the bias current I_b will be very small, of the order of a few nano-amps or even less, and is neglected in comparison with the other two currents which are in the order of a few milli-amps. Hence, Eq. (6.22) can be rewritten as

$$I_{in} \approx I_F$$

$$\frac{V_{in} - V_1}{R_{in}} = \frac{V_1 - V_o}{R_F} \tag{6.23}$$

But, the open-loop gain of the amplifier is given by

$$A = \frac{V_o}{V_{id}} = \frac{V_o}{V_2 - V_1} \tag{6.24}$$

i.e.

$$(V_2 - V_1) = \frac{V_o}{A}$$

$$V_1 = -\frac{V_o}{A} \tag{6.24(a))}$$

Substituting Eq. (6.24) into Eq. (6.23), we can write

$$\frac{V_{in} - \left(-\frac{V_o}{A}\right)}{R_{in}} = \frac{\left(-\frac{V_o}{A}\right) - V_o}{R_F}$$

Re-arranging the terms, we get

$$V_o = -V_{in} \frac{AR_F}{R_{in} + AR_{in} + R_F} \tag{6.25}$$

$$A_F = -\frac{V_o}{V_{in}} = -\frac{AR_F}{AR_{in} + (R_{in} + R_F)} \tag{6.26}$$

The negative sign in Eq. (6.26) indicates here that the output is phase inverted from input and it is also indicated in the input–output waveforms of Fig. 6.12(b). Normally, the open-loop gain of op-amp A is very high and hence $AR_{in} >> (R_{in} + R_F)$; therefore Eq. (6.26) can be rewritten as

$$A_F = -\frac{R_F}{R_{in}} \tag{6.27}$$

The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor R_{in} and feedback resistor R_F, this output also being inverted from the input. Thus, the term on the right-hand side of Eq. (6.27) is called the **scale factor**.

Further, Eq. (6.26) can be re-arranged as below:

$$A_F = -\frac{AR_F}{AR_{in} + (R_{in} + R_F)} \times \frac{(R_{in} + R_F)}{(R_{in} + R_F)}$$

$$A_F = -\frac{\frac{AR_F}{R_{in} + R_F}}{1 + \frac{AR_{in}}{R_{in} + R_F}} = -\frac{Ak}{1 + A\beta} \tag{6.28}$$

where $k = \frac{R_F}{(R_{in} + R_F)}$ is the voltage attenuation factor and $\beta = \frac{R_1}{(R_{in} + R_F)}$ is gain of the feedback circuit.

Example 6.2

For the op-amp inverting amplifier shown in Fig. 6.15, find the scale factor. Plot the output voltage if the input is a sinusoidal signal of 5 mV peak.

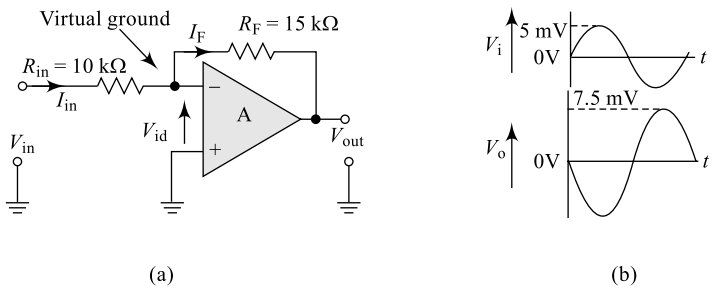


Fig. 6.15 (a) Inverting amplifier for Example 6.2 (b) Input/Output waveforms

Solution We have scale factor for an inverting amplifier given by Eq. (6.27) as

$$A_F = -\frac{R_F}{R_{in}}$$

$$A_F = -\frac{15\,K}{10\,K} = 1.5$$

With a scale factor of 1.5 and an input of 5 mV peak, we get an inverted output of 7.5 mV peak and is plotted as in Fig. 6.15(b).

6.7 OP-AMP NON-INVERTER

Another important application of an op-amp is the non-inverting amplifier, the circuit connection of which is shown in Fig. 6.16. The inverting amplifier connection is more widely used as compared to a non-inverting amplifier because it has better frequency stability. R_F is the feedback resistor, R_{in} is the input resistor, A is the open-loop gain of the op-amp and input signal is connected to non-inverting terminal; once again R_S is the source resistance neglected for simplicity (in comparison with other

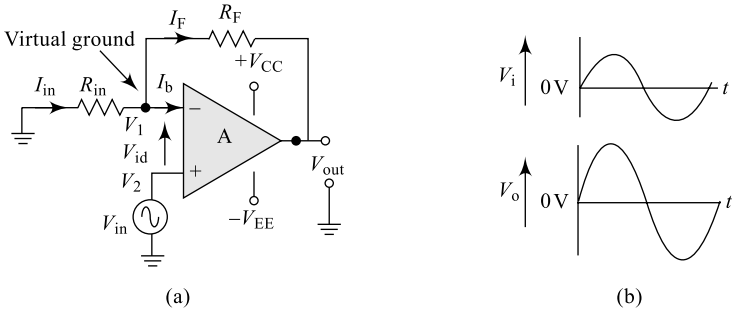


Fig. 6.16 (a) Op-amp non-inverting amplifier (b) Input/Output waveforms

resistances). To determine the voltage gain of the circuit, we first find V_f, the voltage at the inverting terminal using the potential divider rule; since input impedance is very high, zero current flows into the inverting terminal of op-amp and, therefore, we can write

$$V_f = V_2 = V_o \frac{R_{in}}{R_{in} + R_F} \tag{6.29}$$

But, the open-loop gain of the amplifier is given by

$$A = \frac{V_o}{V_{id}} = \frac{V_o}{V_2 - V_1}$$

i.e. $$(V_2 - V_1) = V_{id} = \frac{V_o}{A} \approx 0$$

This is because A is very large.

i.e. $$(V_2 - V_1) = 0$$

This implies that $V_2 = V_1$ and, therefore, we can write

$$V_f = V_2 = V_{in} = V_o \frac{R_{in}}{R_{in} + R_F} \tag{6.30}$$

i.e. $$V_o = V_{in} \frac{R_{in} + R_F}{R_{in}} = V_{in}\left(1 + \frac{R_F}{R_{in}}\right) \tag{6.31}$$

The positive sign in Eq. (6.31) indicates here that output is in-phase with the input; it is non-inverted and it is also indicated in the input–output waveforms of Fig. 6.16(b). The circuit gain can be controlled by the ratio $\frac{R_F}{R_{in}}$ and if $R_F = R_{in}$ then $V_O = 2V_{in.}$

The gain with feedback is given by

$$A_F = \frac{V_o}{V_i}$$

But, $V_o = [A(V]_2 - V_1)$ where $V_2 = V_{in}$ and $V_1 = V_f = V_o \frac{R_{in}}{R_{in} + R_F}$

Therefore, $$V_o = [A(V]_{in} - V_o \frac{R_{in}}{R_{in} + R_F}\Big)$$

Re-arranging gives $$V_o = A\frac{[(R]_{in} + R_F)V_{in} - R_{in}V_o}{R_{in} + R_F} \tag{6.32}$$

i.e. $$V_o = A\frac{[(R]_{in} + R_F)V_{in}}{R_{in} + AR_{in} + R_F}$$

i.e. $$A_F = \frac{V_o}{V_{in}} = A\frac{[(R]_{in} + R_F)}{AR_{in} + (R_{in} + R_F)}.$$ But, $AR_{in} >> (R_{in} + R_F)$

Hence,
$$A_F = A\frac{[(R]_{in} + R_F)}{AR_{in}} = A\left[1 + \frac{R_F}{R_{in}}\right] \tag{6.33}$$

Also, we can write
$$A_F = \frac{A[(R]_{in} + R_F)}{AR_{in} + (R_{in} + R_F)}$$

$$A_F = \frac{\dfrac{[A(R]_{in} + R_F)}{R_{in} + R_F}}{\dfrac{1 + AR_{in}}{R_{in} + R_F}}$$

$$A_F = \frac{A}{1 + A\beta} \tag{6.34}$$

where, $\beta = \dfrac{R_{in}}{[(R]_{in} + R_F)}$ is the feedback factor and $A\beta$ is the loop gain.

Example 6.3

For the op-amp non-inverting amplifier shown in Fig. 6.17, find and plot the output voltage if the input is a sinusoidal signal of 12 mV peak.

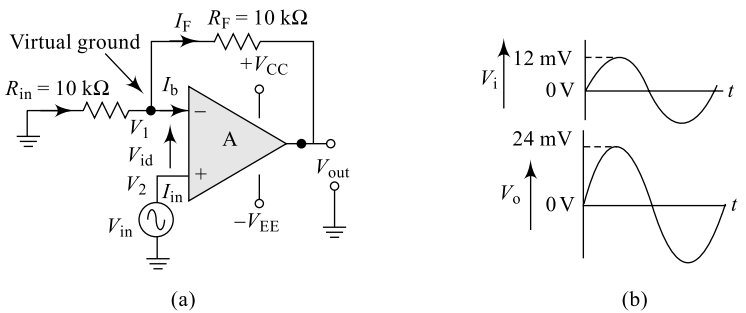


Fig. 6.17 (a) Non-Inverting amplifier for Example 6.3 (b) Input/Output waveforms

Solution We have for a non-inverting amplifier, the gain given by Eq. (6.33)

$$A_F = \frac{V_o}{V_{in}} = \left[1 + \frac{R_F}{R_{in}}\right]$$

$$A_F = \frac{V_o}{V_{in}} = \left[1 + \frac{10\,K}{10\,K}\right] = 2$$

With a gain of 2 and an input of 12 mV peak, we get a non-inverted output of 24 mV peak plotted as in Fig. 6.17(b).

6.8 OP-AMP BUFFER OR VOLTAGE FOLLOWER

In Eq. (6.33), the gain of the non-inverting amplifier will be 1 if $R_F = 0$ or if $R_{in} = \infty$; which implies that by short circuiting the feedback path and/or open circuiting the R_{in}, a no-inverting amplifier works as

a unity gain amplifier. The unity gain amplifier, also called buffer or voltage follower circuit shown in Fig. 6.18(a), produces a gain of unity (1) with no polarity or phase reversal as indicated in Fig. 6.18(b). From the waveforms, it is clear that and that the output has the same polarity and magnitude as the input.

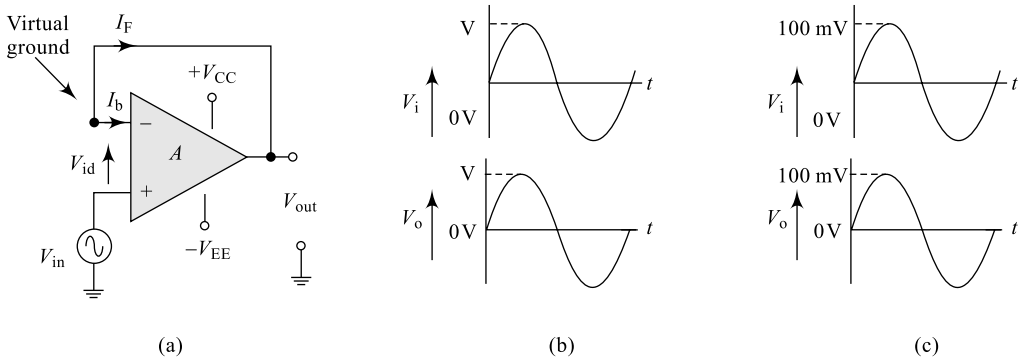


Fig. 6.18 (a) Op-amp voltage follower (b) Input/Output waveforms (c) I/O waveforms for Ex. 6.4

$$A_F = \frac{V_o}{V_{in}} = \left[1 + \frac{0}{\infty}\right] = 1 \tag{6.35}$$

This implies that the output is the exact replica of the input; i.e. $V_O = V_{in}$.

Example 6.4

For the op-amp non-inverting amplifier shown in Fig. 6.18(a), draw to scale the output voltage if the input is a sinusoidal signal of 100 mV peak.

Solution We have for a buffer amplifier, the gain given by Eq. (6.35) as

$$A_F = \frac{V_o}{V_{in}} = 1$$

With a gain of 1 and an input of 100 mV peak, we get a non-inverted output of 100 mV peak plotted as in Fig. 6.18(c).

6.9 OP-AMP SUMMER OR SUMMING AMPLIFIER

Another important application of op-amp is an adder or a summing amplifier; there are two types of summing amplifiers—inverting type and non-inverting type.

6.9.1 Inverting-Type Op-Amp Summer

The circuit connection of an inverting type of summer is shown in Fig. 6.19. A two-input inverting summer circuit connection is shown in Fig. 6.19(a) and a three-input inverting summer circuit connection is shown in Fig. 6.19(b).

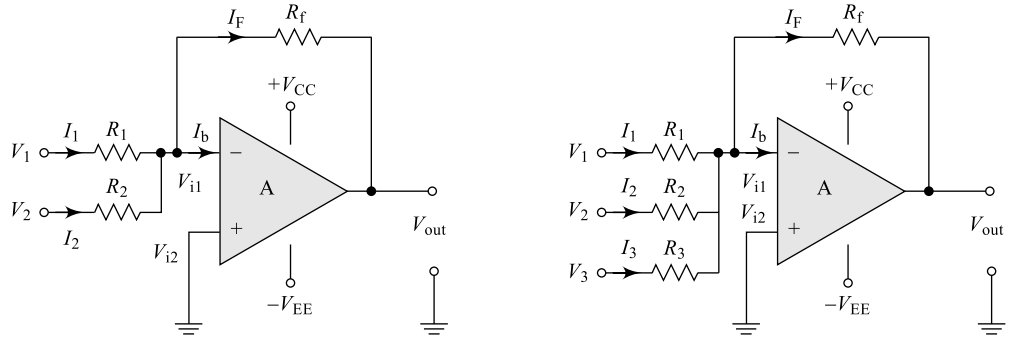


Fig. 6.19 Inverting op-amp summing amplifier: (a) Two inputs (b) Three inputs

Applying Kirchhoff's Current Law (KCL) to the input node V_{i1} of Fig. 6.19(a), we can write

$$I_1 + I_2 = I_F + I_b \qquad [6.36\,(a)]$$

But, the bias current I_b will be very small which is in the order of a few nano-amps or even less. This current is neglected in comparison with the other three currents which are in the order of few milli-amps. Hence, Eq. (6.35) can be rewritten as

$$I_1 + I_2 \approx I_F$$

$$\frac{V_1 - V_{i1}}{R_1} + \frac{V_2 - V_{i1}}{R_2} = \frac{V_{i1} - V_o}{R_F} \qquad [6.36\,(b)]$$

But, the open-loop gain of the amplifier is given by

$$A = \frac{V_o}{V_{id}} = \frac{V_o}{V_{i2} \sim V_{i1}}$$

i.e. $$(V_{i2} \sim V_{i1}) = \frac{V_o}{A} \approx 0 \qquad \because A \text{ is a very large value.}$$

$\therefore$ $$V_{i1} = V_{i2} = 0; \quad \textit{Concept of virtual ground.} \qquad (6.37)$$

Therefore, Eq. (6.36) can be be re-written as

$$\frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} = \frac{0 - V_o}{R_F}$$

On re-arranging, we get

$$V_o = -R_F\left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right] \qquad [6.38\,(a)]$$

Equation [6.38(a)] indicates clearly that the output is proportionally equal to the summation of the two input signals V_1 and V_2. Also, it is important to note that the output signal is phase inverted by 180° from the input signals. In Eq. (6.38), as a special case if $R_1 = R_2 = R_F$ then we have

$$V_O = -[\,V_1 + V_2] \qquad [6.38\,(b)]$$

In Fig. 6.19(b), an inverting type of summer with three inputs is shown and a similar analysis can be done to arrive at the output expression

$$V_o = R_F\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right] \qquad [6.39\,(a)]$$

and $$V_O = -[\,V_1 + V_2 + V_3] \qquad [6.39\,(b)]$$

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.

Example 6.5

Calculate the output voltage of an op-amp summing amplifier shown in Fig. 6.19(b) for the following set of input voltages and resistors:

$V_1 = 200$ mV, $V_2 = 400$ mV, $V_3 = 800$ mV, $R_1 = 20$ kΩ, $R_2 = 40$ kΩ, $R_3 = 80$ kΩ and $R_F = 20$ kΩ.

Solution We have from Eq. [6.39(a)], the output given by

$$V_o = -R_F\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

$$V_o = -20k\left[\frac{200m}{20k} + \frac{400m}{40k} + \frac{800m}{80k}\right] = 600 \text{ mV}$$

6.9.2 Non-Inverting Type Op-Amp Summer

Unlike in the case of inverting summing amplifiers, in a non-inverting type, all the input signals to be summed are applied to the non-inverting terminal; the circuit of Fig. 6.20 shows a three-input non-inverting summing amplifier, which provides a means of algebraically summing (adding) three voltages; each multiplied by a constant-gain factor. Using the superposition theorem, we can express the effective voltage at node V_{i2} in terms of all the inputs as

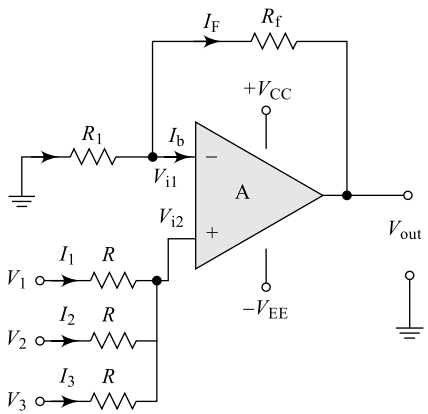


Fig. 6.20 Non-inverting op-amp summing amplifier

$$V_{i2} = \left[\frac{V_1}{\left(R + \frac{R}{2}\right)} \times \frac{R}{2}\right] + \left[\frac{V_2}{\left(R + \frac{R}{2}\right)} \times \frac{R}{2}\right] + \left[\frac{V_3}{\left(R + \frac{R}{2}\right)} \times \frac{R}{2}\right]$$

$$= \left[\frac{R/2}{R + \frac{R}{2}}\right][V_1 + V_2 + V_3] \qquad [6.40\,(a)]$$

$$V_{i2} = \frac{2R/2}{3R}[V_1 + V_2 + V_3] \qquad [6.40\,(b)]$$

Now, this V_{i2} acts as input to the non-inverting amplifier and hence the output expression can be written following Eq. (6.31) as

$$V_o = V_{i2}\left(1 + \frac{R_F}{R_1}\right) \tag{6.41}$$

6.10 OP-AMP INTEGRATOR

Another very useful application of an op-amp is the integrator that finds a wide range of applications in analog computations. The circuit diagram of an integrator and output waveform for a square-wave input are shown in Fig. 6.21. The input source is connected to an inverting terminal through a resistor R_1 and the output is measured across a capacitor connected in the feedback path. An integrator allows only low-frequency components below a designed value f_L to pass to the output and eliminates all high-frequency components above f_L; hence, it is also referred to as a high-frequency discriminator or a low-pass filter (filters are discussed in Section 6.18).

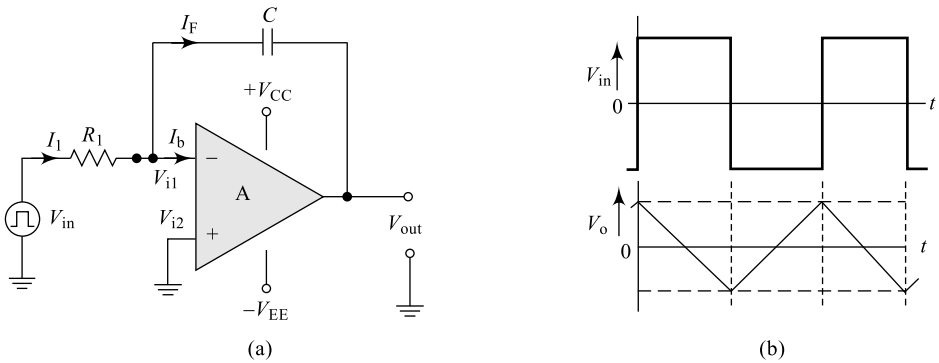


Fig. 6.21 (a) Op-amp integrator (b) Input/Output waveforms

Applying Kirchhoff's Current Law to node V_{i1}, we get

$$I_1 = I_F + I_b \tag{6.42}$$

But, the bias current I_b will be very small in the order of a few nano-amps or even less and is neglected in comparison with the other two currents which are in the order of few milli-amps. Hence, Eq. (6.42) can be rewritten as

$I_1 \approx I_F$; here I_F is the capacitor current.

$$\frac{V_{in} - V_{i1}}{R_1} = C\frac{d(V_{i1} - V_o)}{dt} \tag{6.43}$$

But, the open-loop gain of the amplifier is given by

$$A = \frac{V_o}{V_{id}} = \frac{V_o}{V_{i2} \sim V_{i1}}$$

i.e. $$(V_{i2} \sim V_{i1}) = \frac{V_o}{A} \approx 0$$

$$V_{i1} = V_{i2} = 0 \qquad \textit{Concept of virtual ground}$$

Therefore, Eq. (6.43) can be be rewritten as

$$\frac{V_{in} - 0}{R_1} = C\frac{d}{dt(0 - V_o)}$$

$$V_{in} = -R_1 C\frac{d}{dt(V_o)} \tag{6.44}$$

Integrating Eq. (6.44) on both sides, we get

$$V_o = \frac{1}{R_1 C}\int V_{in}\, dt + k \tag{6.45}$$

Equation (6.45) clearly indicates that the output is an integral function of the input signal V_{in}. The integration constant k in Eq. (6.45) represents the initial charge on the capacitor.

When V_{in} changes abruptly, the capacitor C acts as an open circuit and the circuit works as an open-loop amplifier. Now, the input offset voltage and a part of the input current produce an error voltage at the output; therefore, in a practical integrator, a large resistor R_2 across C will be connected to reduce this error voltage as shown in Fig. 6.22. This R_2 reduces the gain of the amplifier and hence, a very large value of $R_2 >> 10R_1$ will be selected. Figure 6.22(b) indicates the frequency response of the basic integrator circuit.

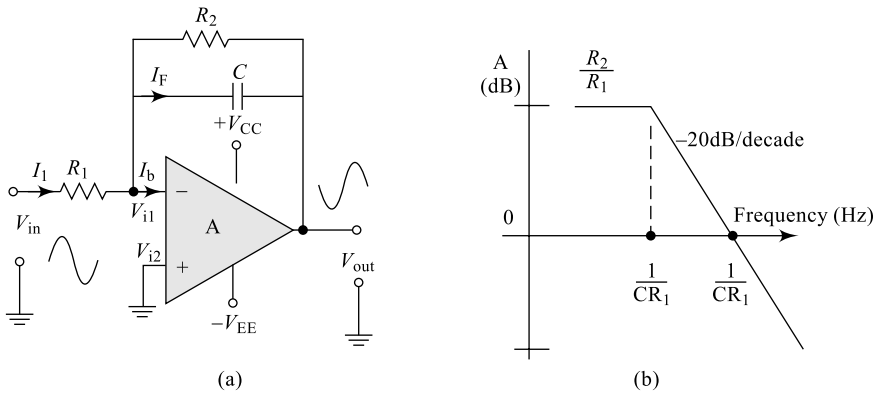


Fig. 6.22 Op-amp integrator (a) Practical circuit (b) Integrator frequency response

For low-frequency signal components, the capacitor offers a very high reactance and hence, maximum signal appears at the output; but for high-frequency components, the reactance is very low and almost no signal appears at the output. This is because, for a capacitor, the reactance is inversly proportional to frequency; thus an integrator acts as a low-pass filter or a high-frequency discriminator.

6.11 OP-AMP DIFFERENTIATOR

Another very useful application of an op-amp is the differentiator which finds a wide range of applications in analog computations. The circuit diagram of a differentiator and the output waveform for a triangular-wave input are shown in Fig. 6.23. The input source is connected to an inverting terminal through the capacitor and the output is measured across the resistor R_1 connected in the feedback path. A differentiator allows all the frequency components above a designed value f_H to pass to the output

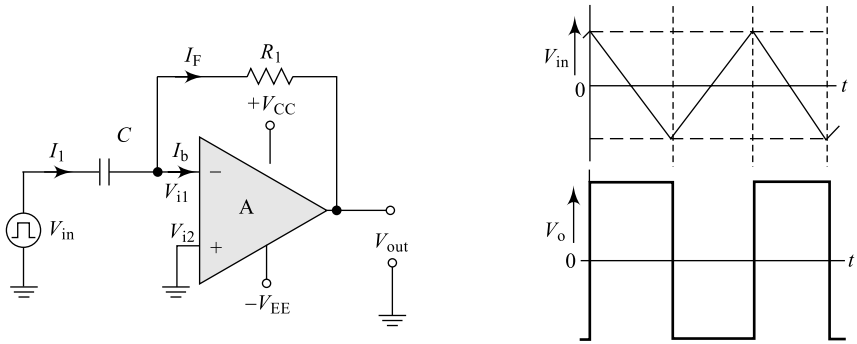


Fig. 6.23 (a) Op-amp differentiator (b) Input/Output waveforms

and eliminates all low-frequency components below f_H; hence, it is also referred to as a low-frequency discriminator or a high-pass filter.

Applying Kirchhoff's Current Law to the node V_{i1}, we get

$$I_1 = I_F + I_b \tag{6.46}$$

But, the bias current I_b will be very small, of the order of a few nano-amps or even less, and is neglected in comparison with the other two currents which are of the order of a few milli-amps. Hence, Eq. (6.46) can be rewritten as

$I_1 \approx I_F$; here, I_1 is the capacitor current.

$$C\frac{d}{dt(V_{in} - V_{i1})} = \frac{V_{i1} - V_o}{R_1} \tag{6.47}$$

But, the open-loop gain of the amplifier is given by

$$A = \frac{V_o}{V_{id}} = \frac{V_o}{V_{i2} \sim V_{i1}}$$

i.e. $$(V_{i2} \sim V_{i1}) = \frac{V_o}{A} \approx 0$$

$$V_{i1} = V_{i2} = 0; \qquad \textit{Concept of virtual ground}$$

Therefore, Eq. (6.47) can be be rewritten as

$$C\frac{d}{dt(V_{in} - 0)} = \frac{0 - V_o}{R_1}$$

$$V_o = -R_1 C\frac{d}{dt(V_{in})} \tag{6.48}$$

Equation (6.48) clearly indicates that output is proportional to a differential function of the input signal V_{in}. For low-frequency signal components, the capacitor offers a very high reactance and hence, a very minimum signal appears at the output; but for high-frequency components, the reactance is very low and almost the complete signal appears at the output. This is once again because, for a capacitor, the reactance is inversely proportional to frequency; thus an integrator acts as a high-pass filter or a low frequency discriminator.

6.12 OP-AMP SUBTRACTOR OR DIFFERENCE AMPLIFIER

Another very useful application of an op-amp is the difference amplifier; a difference amplifier is widely used in instrumentation and industrial applications for amplifying very sensitive and small signals such as weather forecasting, output of a Wheatstone bridge, etc. A difference amplifier is certainly a good choice over other inverting or non-inverting types of amplifiers as these are better able to reject the common-mode signals (noise) offering high-degree CMRR and present a balanced input impedance. The circuit arrangement for a difference amplifier is shown in Fig. 6.24; here the two inputs whose difference is to be estimated and amplified are applied to the two input terminals. It is clear from the diagram that a difference amplifier is a combination of an inverting and a non-inverting amplifier; hence, applying the superposition principle, we can obtain the output of the circuit.

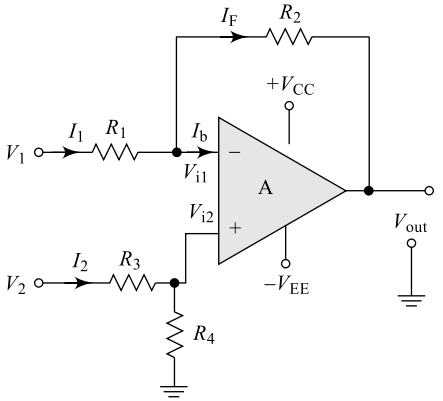


Fig. 6.24 Difference amplifier

Considering only the source V_1, with the source V_2 grounded, the circuit forms an inverting amplifier and the resulting output due to the source V_1 alone is given by

$$V_{o1} = -\frac{R_2}{R_1} V_1 \tag{6.49}$$

Similarly, considering only the source V_2, with the source V_1 grounded, the circuit forms a non-inverting amplifier and the resulting output due to the source V_2 alone is given by

$$V_{o2} = +\left(1 + \frac{R_2}{R_1}\right) V_{i2} \tag{6.50}$$

where V_{i2} is the effective voltage at the non-inverting terminal due to the source V_2 and is given by the potential divider rule applied for R_3 and R_4.

$$V_{i2} = \left(\frac{R_4}{R_4 + R_3}\right) V_2 \tag{6.51}$$

Now, we can obtain the output of the circuit by combining equations (6.49), (6.50) and (6.51) using the superposition principle as

$$\begin{aligned} V_o &= V_{o1} + V_{o2} \\ V_o &= -\frac{R_2}{R_1} V_1 + \left(1 + \frac{R_2}{R_1}\right) V_{i2} \\ V_o &= -\frac{R_2}{R_1} V_1 + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_4 + R_3}\right) V_2 \end{aligned} \tag{6.52}$$

As a special case, if $R_3 = R_1$ and $R_4 = R_2$ then Eq. (6.52) can be rewritten as

$$V_o = -\frac{R_2}{R_1}(V_1 - V_2) = -\frac{R_2}{R_1}(V_{12}) \tag{6.53}$$

$$V_o = \frac{V_o}{V_{12}} = -\frac{R_2}{R_1} \tag{6.54}$$

6.13 INSTRUMENTATION AMPLIFIER

One of the most popular areas of op-amp application is in instrumentation and control circuits such as weather forecasting, dc or ac current and voltage meters, etc. A circuit providing an output proportional to the difference between two inputs is shown in Fig. 6.24; a difference amplifier with either one op-amp or two op-amps (not shown) offers different input impedances to the two input sources which is the biggest problem in such sensitive applications. A three op-amp difference amplifier circuit is shown in Fig. 6.25 which forms the basic instrumentation amplifier, the circuit offers equal input impedance to both the sources and hence it is an ideal instrumentation amplifier.

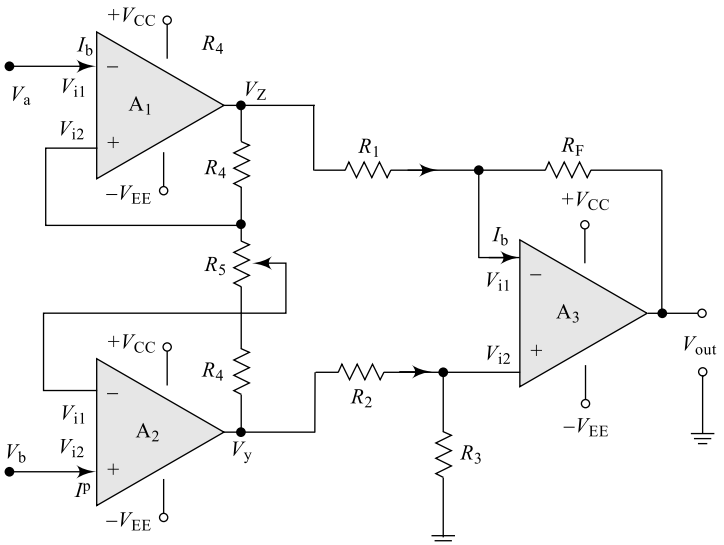


Fig. 6.25 (a) Op-amp instrumentation amplifier

In order to find the output voltage of each stage, we have to use the superposition principle. The equivalent circuits to find the output voltages of each stage are shown in Fig. 6.26. Applying the superposition principle to Fig. 6.26(b), we can write

$$V_Z = -\frac{R_4}{R_4 + R_5} V_Y + \left(1 + \frac{R_4}{R_4 - R_5}\right) V_a \tag{6.55}$$

$$V_Z = \left(\frac{2R_4 + R_5}{R_4 + R_5}\right) V_a - \frac{R_4}{R_4 + R_5} V_Y \tag{6.56}$$

Similarly, applying the superposition principle to Fig. 6.26(c), we can write

$$V_Y = -\frac{R_4}{R_4 + R_5} V_Z + \left(1 + \frac{R_4}{R_4 + R_5}\right) V_b \qquad [6.57(a)]$$

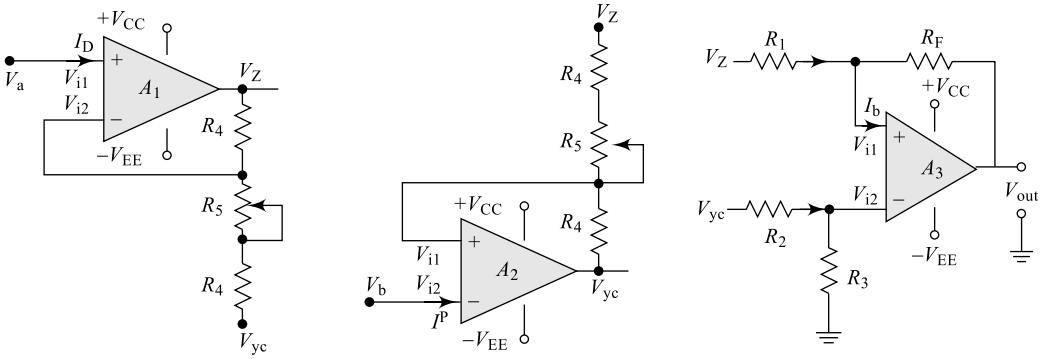


Fig. 6.26 IA Equivalent circuits: (a) To find V_Z (b) To find V_Y (c) To find V_{OUT}

$$V_y = \left(\frac{2R_4 + R_5}{R_4 + R_5}\right)V_b - \frac{R_4}{R_4 + R_5}V_Z \qquad [6.57(b)]$$

The output of Stage-1 is V_{o1}, given by

$$V_{o1} = V_{ZY} = V_Z - V_y$$

$$V_{ZY} = \left[\left(\frac{2R_4 + R_5}{R_4 + R_5}\right)V_a - \frac{R_4}{R_4 + R_5}V_y\right] - \left[\left(\frac{2R_4 + R_5}{R_4 + R_5}\right)V_b - \frac{R_4}{R_4 + R_5}V_Z\right] \qquad (6.58)$$

$$V_{ZY} = \left[\left(\frac{2R_4 + R_5}{R_4 + R_5}(V_a - V_b)\right)\right] + \left[\frac{R_4}{R_4 + R_5}(V_z - V_y)\right]$$

$$V_{ZY} = \left[\left(\frac{2R_4 + R_5}{R_4 + R_5}V_{ab}\right)\right] + \left[\frac{R_4}{R_4 + R_5}V_{zy}\right] \qquad (6.59)$$

The gain of Stage-1 is $\dfrac{V_{ZY}}{V_{ab}} = \dfrac{2R_4 + R_5}{R_5}$ (6.60)

The gain of Stage-2 is $\dfrac{V_o}{V_{ZY}} = -\dfrac{R_F}{R_1}$ as per Eq. (6.54). (6.61)

Then, the overall gain of the amplifier can be estimated using Fig. 6.25(d) and is given by

$$A_d = \frac{V_{ZY}}{V_{ab}} \times \frac{V_o}{V_{ZY}} = \frac{2R_4 + R_5}{R_5} \times \left(-\frac{R_F}{R_1}\right)$$

$$A_d = -\left(1 + \frac{2R_4}{R_5}\right) \times \left(\frac{R_F}{R_1}\right) \qquad (6.62)$$

Thus, the overall gain of the amplifier can be controlled by controlling R_5.

6.14 OP-AMP COMPARATOR

A comparator compares an analog signal on one input terminal with another input signal or a reference signal and provides a digital output; hence, it can be called a one-bit analog-to-digital converter (ADC). The output may be of either positive or negative saturation value, when the circuit operates in open-loop mode. Comparators find vast applications in digital interfacing, Schmitt triggers, discriminators, voltage-level detectors, oscillators, etc. Comparators can be realised in any of the following eight different forms:

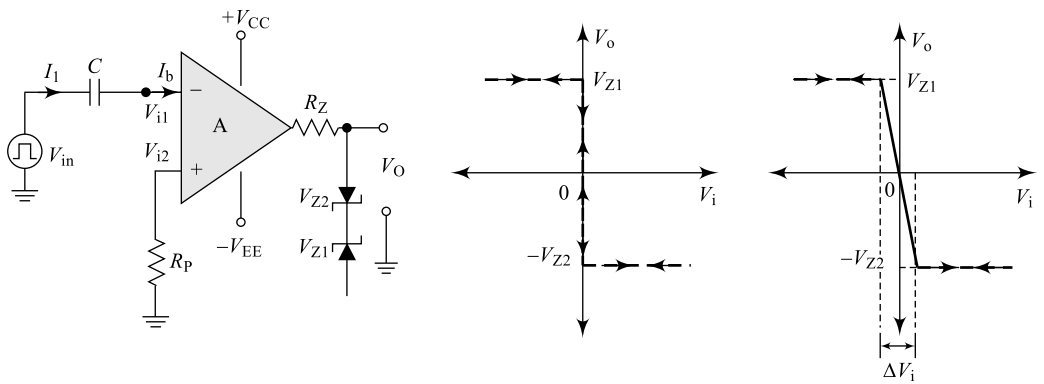
(i) Inverting zero-crossing comparator
(ii) Non-inverting zero-crossing comparator
(iii) Inverting zero-crossing comparator with hysteresis
(iv) Non-inverting zero-crossing comparator with hysteresis
(v) Inverting level detector
(vi) Non-inverting level detector
(vii) Inverting level detector with hysteresis
(viii) Non-inverting level detector with hysteresis

Cases (i), (ii), (v) and (vi) operate in open-loop configuration without any reference source, while cases (iii), (iv), (vii) and (viii) operate in closed-loop configuration with a reference source connected.

6.14.1 Inverting Zero-Crossing Comparator

In the open-loop mode, output of the amplifier will be at its saturation in either direction; V_{sat} on the positive side and $-V_{sat}$ on the negative side. But, use of limiting Zener diodes clamps this voltage to V_Z in either direction. R_Z is the Zener current limiter and R_P is the temperature compensation resistor for the op-amp.

When $V_{in} < V_{ref}$ (= 0), i.e. when V_{in} is negative, the output of the op-amp is $+V_{sat}$ and will be limited to $+V_{Z1}$ due to the Zener diode Z_1. Similarly, When $V_{in} > V_{ref}$ (= 0), i.e. when V_{in} is positive, output of op-amp is $-V_{sat}$ and will be limited to $-V_{Z2}$ due to Zener diode Z_2. It is clear from the transfer characteristics shown in Fig. 6.27(b) that a comparator can be used as a linear signal like a sine wave or a triangular wave to a square-wave output. Also, the analog input is converted into a digital output; hence,



(a) Circuit (b) Ideal transfer curve (c) Practical transfer curve

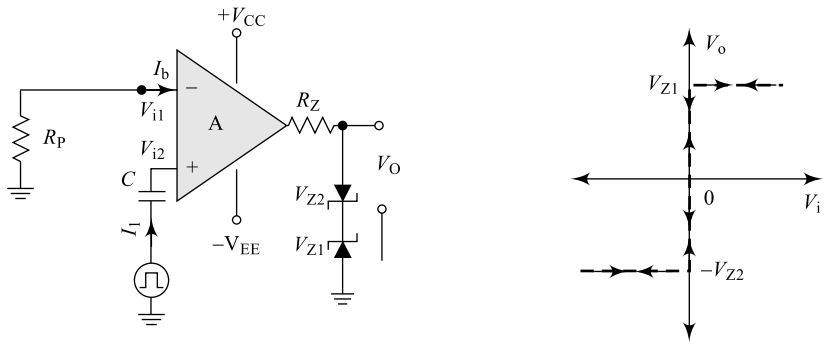
Fig. 6.27 Inverting zero-crossing comparator

it can be considered as a one-bit analog-to-digital convertor. In a practical op-amp, the output signal transition will not be as steep as indicated in Fig. 6.27(b) since the open-loop gain of the op-amp is not infinity. Because of the finite open-loop gain, there always exists a region of uncertainty ΔV_i where V_O can be anywhere between $+V$ and $-V$ and this is indicated in Fig. 6.27(c).

6.14.2 Non-Inverting Zero-Crossing Comparator

In this case, the input signal is applied to the non-inverting terminal and hence, the transfer curve takes an inverted shape in comparison to the case in section 6.15.1 and is indicated in Fig. 6.28(b). In the circuit diagram, the capacitor C is used to block the possible dc components from the input source, so as to maintain the stable operating conditions.

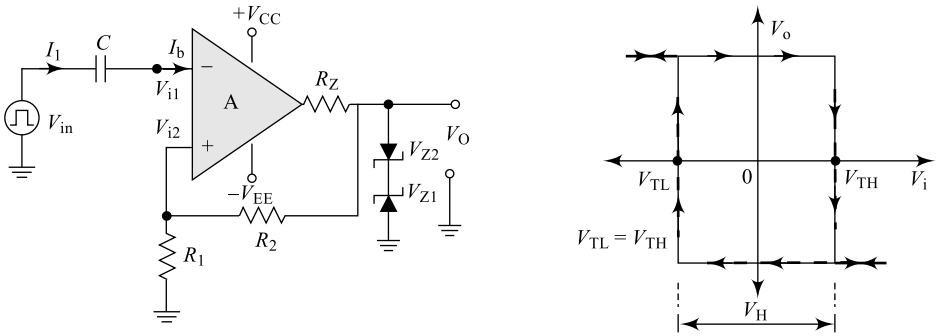
When $V_{in} < V_{ref}$ (= 0), i.e. when V_{in} is negative, the output of the op-amp is $-V_{sat}$ and will be limited to $-V_{Z_2}$ due to the Zener diode Z_2. Similarly, When $V_{in} > V_{ref}$ (= 0), i.e. when V_{in} is positive, the output of the op-amp is $+V_{sat}$ and will be limited to $+V_{Z_1}$ due to the Zener diode Z_1. This is indicated as ideal characteristics in Fig. 6.28(b) and a similar explanation as in Fig. 6.28(c) holds good for practical cases.



(a) Circuit (b) Transfer characteristics

Fig. 6.28 Non-inverting zero-crossing comparator

6.14.3 Inverting Zero-crossing Comparator with Hysteresis



(a) Circuit (b) Transfer characteristics

Fig. 6.29 Inverting zero-crossing comparator with V_H

In the open-loop mode, the output of the amplifier will be at its saturation in either direction; and in order to reduce the effect of noise, hysteresis is introduced into the circuit. In Fig. 6.29(a), resistors R_1 and R_2 form a positive feedback and every time the input signal makes a transition, a new reference at the non-inverting terminal is introduced by this arrangement. This results in **hysteresis** or **backlash property** as indicated in Fig. 6.29(b). Use of limiting Zener diodes clamps the output voltage to V_Z in either direction. R_Z is the Zener current limiter and R_P is the temperature compensation resistor for op-amp. Unlike in the previous two cases, a nonzero reference voltage is now available at the non-inverting terminal and is given by the expression

$$V_{i2} = V_o \frac{R_1}{R_1 + R_2} = V_Z \frac{R_1}{R_1 + R_2} \tag{6.63}$$

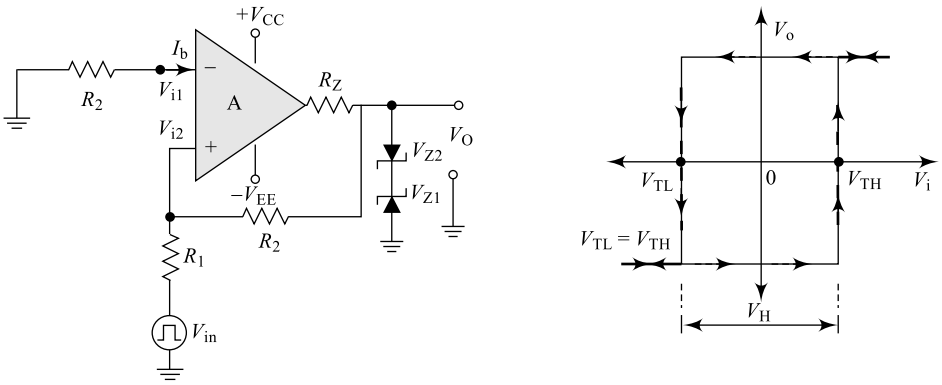
Now, depending on output polarity, the two reference voltages can be defined and are given by equations [6.63(a)] and [6.63(b)].

$$V_{TH} = V_{Z1} \frac{R_1}{R_1 + R_2} \tag{6.63(a)}$$

$$V_{TL} = -V_{Z2} \frac{R_1}{R_1 + R_2} \tag{6.63(b)}$$

When $V_{in} < +V_{ref}$ ($= V_{TH}$), the output of the op-amp is $+V_{sat}$ and will be limited to $+V_{Z1}$ due to the Zener diode Z_1. Similarly, when $V_{in} > -V_{ref}$ ($= V_{TL}$), the output of the op-amp is $-V_{sat}$ and will be limited to $+V_{Z2}$ due to the Zener diode Z_2. It is clear from the transfer characteristics shown in Fig. 6.28(b) that due to changing references, a backlash appears given by $V_H = (V_{TH} - V_{TL})$.

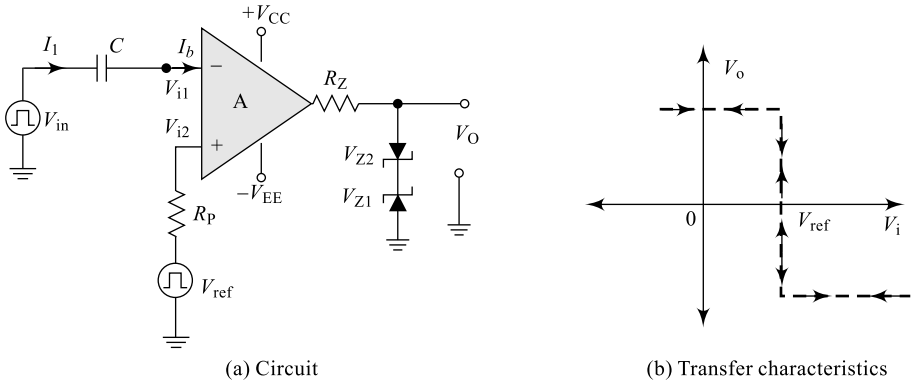
6.14.4 Non-Inverting Zero-Crossing Comparator with Hysteresis



(a) Circuit (b) Transfer characteristics

Fig. 6.30 Non-inverting zero-crossing comparator with V_H

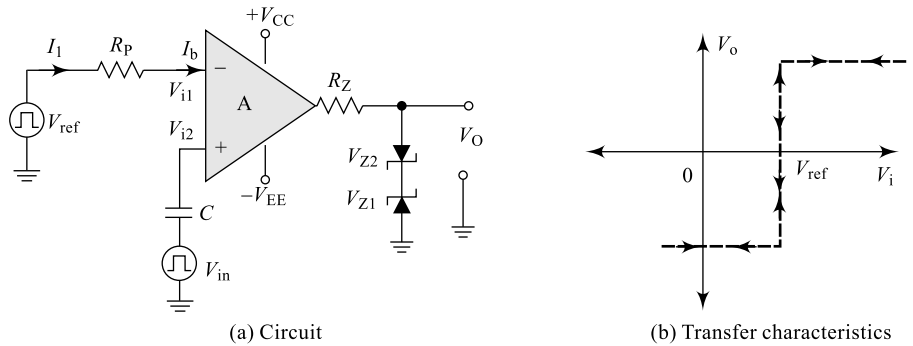
6.14.5 Inverting Level Detector



(a) Circuit (b) Transfer characteristics

Fig. 6.31 Inverting level detector

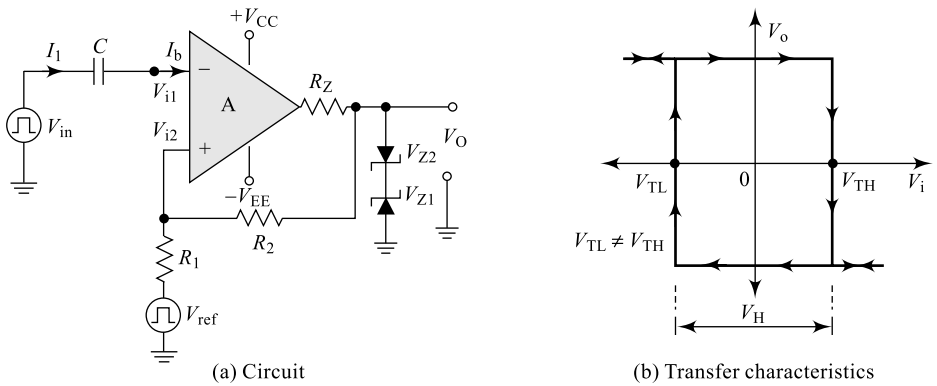
6.14.6 Non-Inverting Level Detector



(a) Circuit (b) Transfer characteristics

Fig. 6.32 Non-inverting level detector

6.14.7 Inverting Level Detector with Hysteresis



(a) Circuit (b) Transfer characteristics

Fig. 6.33 Inverting level detector with V_H

6.14.8 Non-Inverting Level Detector with Hysteresis

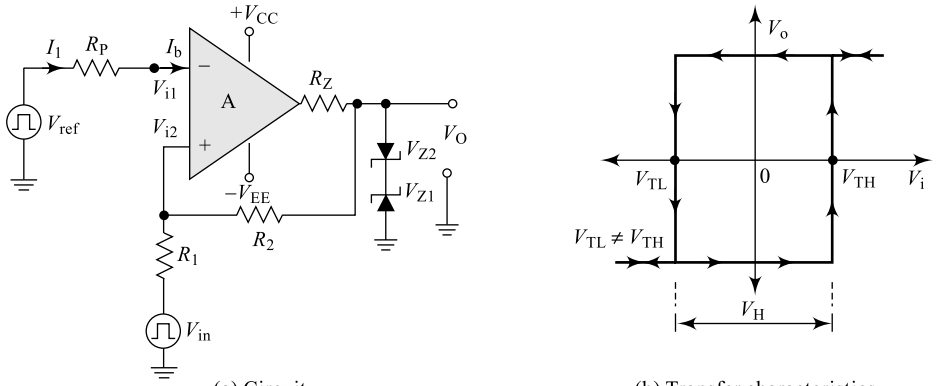


Fig. 6.34 Non-inverting level detector with V_H

6.15 OP-AMP SCHMITT TRIGGER

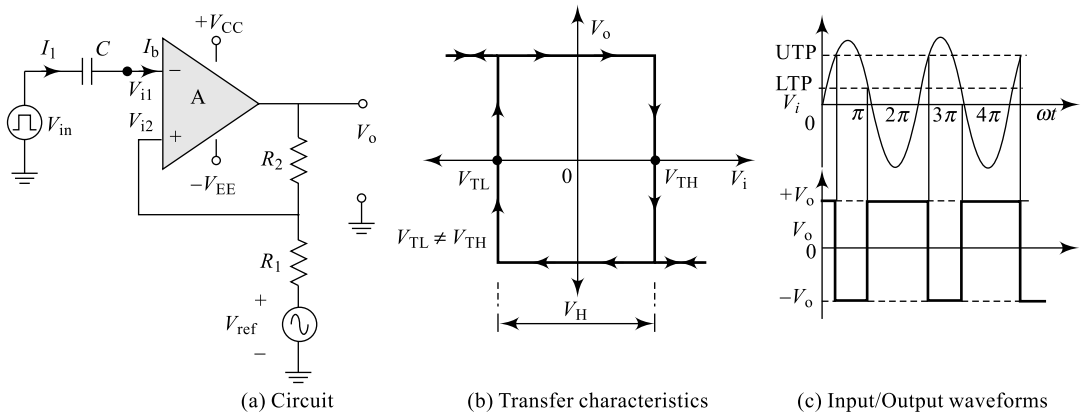


Fig. 6.35 Op-amp Schmitt trigger

The region of uncertainty in an open-loop comparator can be eliminated by using a positive feedback; the resulting circuit known as Schmitt trigger is shown in Fig. 6.35(a) along with its transfer curve in Fig. 6.35(b). Resistors R_1 and R_2 form the positive feedback circuit, introduce the hysteresis and offer changing thresholds called as lower threshold potential (LTP) and Upper Threshold Potential (UTP).

The potential at the non-inverting terminal $V_T = V_{i2}$ depends on the output voltage V_o and the reference voltage V_{ref} will be obtained using the superposition principle. The magnitude and polarity of V_T depends on both V_o and V_{ref}; they will be positive when V_o is positive and negative when V_o is negative assuming V_{ref} is small in magnitude. A Schmitt Trigger converts an input periodic signal into a square wave; this is indicated in Fig. 6.34(c). When the input signal is negative, the output will be at $+V_o$ and the threshold at the non-inverting terminal is obtained by using the superposition principle, given by

$$V_{T(+)} = V_o \frac{R_1}{R_1 + R_2} \pm V_{ref} \frac{R_2}{R_1 + R_2} = \text{UTP} \quad [6.64(a)]$$

$$\text{UTP} = V_o \beta \pm V_{ref} (1 - \beta) \quad [6.64(b)]$$

where $\beta = \frac{R_1}{R_1 + R_2}$ and $(1 - \beta) = \frac{R_1}{R_1 + R_2}$ represents the feedback factor. [6.64(c)]

When input signal rises just above this threshold potential, because of the comparator action, the output makes a transition to $-V_{sat}$ and any further increase in the input signal amplitude has no effect on the output. This value of threshold potential is called the Upper Threshold Potential (UTP). Now, the new value of V_T is obtained once again by using the superposition principle and is given by

$$V_{T(-)} = -V_o \frac{R_1}{R_1 + R_2} \pm V_{ref} \frac{R_2}{R_1 + R_2} = \text{LTP} \quad [6.65(a)]$$

$$\text{LTP} = -V_o \beta \pm V_{ref} (1 - \beta) \quad [6.65(b)]$$

When the input signal falls just below this threshold potential, because of the comparator action, the output makes a transition to $+V_{sat}$ and any further decrease in the input signal amplitude has no effect on output. This value of threshold potential is called the Lower Threshold Potential (LTP). It can be observed that every time the input crosses the threshold potential values defined by equations (6.64) and (6.65), the output makes a transition and sets a new threshold value; this results in hysteresis V_H. The value of hysteresis can be obtained by the expression

$$V_H = \text{UTP} - \text{LTP} \quad [6.66(a)]$$

$$V_H = V_o \frac{R_1}{R_1 + R_2} \pm V_{ref} \frac{R_2}{R_1 + R_2} \left[-[-V]_o \frac{R_1}{R_1 + R_2} \pm V_{ref} \frac{R_2}{R_1 + R_2} \right] \quad [6.66(b)]$$

$$V_H = 2V_o \frac{R_1}{R_1 + R_2} \quad [6.66(c)]$$

Example 6.6

Design an op-amp Schmitt trigger circuit to meet the following specifications: LTP = 2 V, UTP = 4 V and $V_{CC} = \pm 12$ V.

Solution Referring to Fig. 6.34(a), we have from Eq. [6.64 (b)],

$$\text{UTP} = \beta V_O + (1 - \beta)\, V_R$$

and from Eq. [6.65 (b)], $\text{LTP} = -\beta V_O + (1 - \beta)\, V_R$

The feedback factor β is given by Eq. [6.64(c)].

Now, Eq. [6.64(b)] – Eq. [6.65 (c)] = $2\beta V_O$

But, from Eq. [6.64(c)], $\beta = 2/2(12) = 0.0833$

Similarly, Eq. [6.64(b)] + Eq. [6.65 (c)] = $2((1 - \beta)\, V_R)$

Hence, $V_R = 6/2(1 - 0.0833) = 3.273$ V

Now, $\beta = R_2/(R_1 + R_2) = 0.0833$

Solving the above equation, we get $(R_1/R_2) = 11$;

Choose $R_2 = 2$ kΩ; then $R_1 = 22$ kΩ

6.16 ACTIVE FILTERS

One of the popular applications of op-amps is active filters. A filter can be constructed using passive components such as resistors, inductors and capacitors and is called a **passive filter**. An **active filter** additionally uses an amplifier like an op-amp to provide voltage amplification and signal isolation or buffering. A filter is an electric circuit that allows a certain band of frequencies to reach output and eliminates all other frequencies. Hence, the frequency response of a filter can be said to have a **pass band** where input signals are passed with minimum or zero attenuation and a **stop band** where signals are completely eliminated with maximum or infinite attenuation. The frequency at which these two bands are separated is called the **cut-off frequency** (f_C). A filter can be

(i) analog or digital, depending on the application and construction,
(ii) passive or active, depending on the components used, and
(iii) Audio Frequency (AF) or Radio Frequency (RF), depending on the frequency.

A passive filter provides no gain to the input signal and has a poor frequency response, but an active filter with the use of an op-amp offers the following advantages:

(i) Introduces gain to the input signal
(ii) Provides high input impedance and low output impedance
(iii) Offers very good separation between pass band and stop band
(iv) Operates over wide frequency range for given R and C values
(v) Offers better frequency response and slew rate

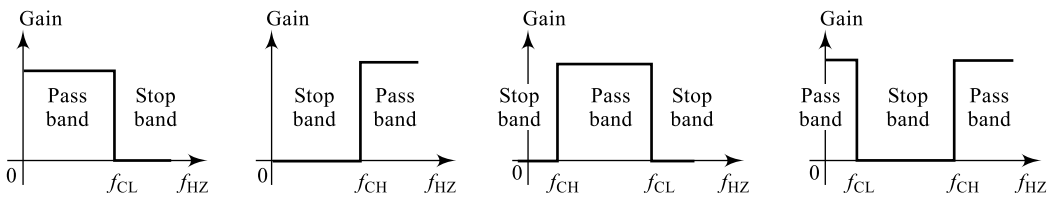
However, an active filter with the use of an op-amp suffers from the following disadvantages:

(i) Needs two power supplies for op-amp
(ii) Cost of filter will be more
(iii) Op-amp should have high bandwidth and slew rate

Based on the selection of the pass band and the stop band, filters can be classified into the following four types:

(i) Low-Pass Filter (LPF)
(ii) High-Pass Filter (HPF)
(iii) Band-Pass Filter (BPF)
(iv) Band Elimination Pass Filter (BEF)

A filter that provides a constant output from dc up to a cut-off frequency f_C and then passes no signal above that frequency is called an **ideal low-pass filter**. A filter that passes no signal below a cut-off frequency f_C and provides a constant output from that frequency is called an **ideal high-pass filter**. A filter that passes signals between a range of frequencies f_{C1} and f_{C2} providing a constant output and passes no signal beyond these two cut-off frequencies is called an **ideal band-pass filter**. A filter that eliminates signals between a range of frequencies f_{C1} and f_{C2} providing no output and passes the complete signal beyond these two cut-off frequencies providing a constant output is called an **ideal band-elimination filter**. The ideal frequency responses of all these filters are shown in Fig. 6.36.



(a) Low-pass filter (b) High-pass filter (c) Band-pass filter (d) Band elimination filter

Fig. 6.36 Ideal filter responses

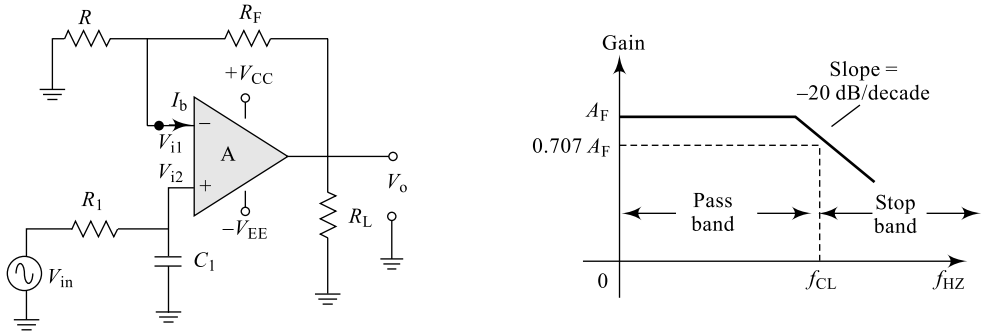
6.16.1 Low-Pass Active Filters (LPF)

A filter that allows or passes signals below a cut-off frequency f_{CL} is a low-pass filter and its ideal frequency response is shown in Fig. 6.35(a). A first-order (order of the filter means number of *RC* sections used) low-pass filter using a single resistor and capacitor is shown in Fig. 6.36(a) and its frequency response has a practical slope of –20 dB per decade, as shown in Fig. 6.36(b) [rather than the ideal response of Fig. 6.35(a)]. The voltage gain below the cut-off frequency is constant at A_F and decays at a slope of –20 dB/decade above the cut-off frequency.

1. First-Order Low-Pass Active Filters

A first-order (first order means one *RC* section) low-pass filter using one resistor and one capacitor is shown in Fig. 6.37(a) and its frequency response has a practical slope of –20 dB per decade, as shown in Fig. 6.37(b). The separation between the pass band and stop band is not very steep and the region of uncertainty between pass band and stop band is not minimised; however, the gain of the system is given by the equation

$$A_f = 1 + \frac{R_f}{R_1} \qquad [6.67(a)]$$



(a) Low pass filter circuit (b) Frequency response

Fig. 6.37 First-order low-pass filter

The expression for the cut-off frequency is given by

$$f_{CL} = \frac{1}{2\pi R_1 C_1} \text{Hz} \qquad [6.67(b)]$$

The gain of the system is given by the expression

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left[\frac{f}{f_c}\right]^2}} \quad \text{where } A_F = 1 + \frac{R_F}{R} \qquad (6.68)$$

Now, the filter operation can be summarised using the gain equation as below:

(i) At very low frequencies, i.e. $f << f_{cL}$,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+0}} \cong A_F$$

(ii) At frequencies that are comparable with $f_{cL,}$ i.e. $f = f_{cL}$,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+1}} \cong 0.707 A_F$$

(iii) At frequencies that are above f_{cL}, i.e. $f >> f_{cL}$,

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

Thus, an LPF has a constant gain of A_F from 0 to f_{CL} Hz, at cut-off frequency, the gain is 0.707 A_F and for frequencies above f_{CL}, the gain decreases with a constant decay rate of –20 dB/decade. The cut-off frequency is also called the **corner frequency** or **break frequency** or **–3 dB frequency**.

Example 6.7

Calculate the cut-off frequency of a first-order low-pass filter whose $R = 2$ kΩ and $C = 0.1$ μF.

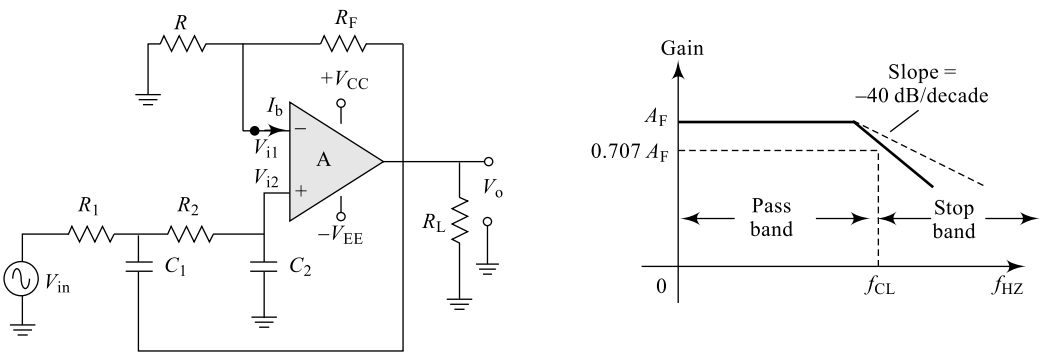
Solution We have for a first-order LPF from Eq. (6.67),

$$f_{CL} = \frac{1}{2\pi R_1 C_1} \text{Hz}$$

$$f_{CL} = \frac{1}{2\pi \times 2 \times 10^3\ 0.1 \times 10^{-6}} = 795.8 \cong 796 \text{ Hz}$$

2. Second-Order Low-Pass Active Filters

A second-order (second order order means two *RC* sections) low-pass filter using two resistors and two capacitors is shown in Fig. 6.38(a) and its frequency response has a practical slope of –40 dB per decade, as shown in Fig. 6.38(b). Use of two *RC* sections improves the frequency response as shown. The separation between the pass band and stop band is very steep and the region of uncertainty between pass band and stop band is minimised; however, the gain of the system is limited to 1.586.



(a) Low-pass filter circuit (b) Frequency response

Fig. 6.38 Second-order low-pass filter

The expression for the cut-off frequency is given by

$$f_{CL} = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}} \text{Hz} \tag{6.69}$$

The gain of the system is given by the expression

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left[\frac{f}{f_c}\right]^4}} \quad \text{where } A_F = 1+\frac{R_F}{R} \tag{6.70}$$

Example 6.8

Calculate the cut-off frequency of a second-order low-pass filter whose $R = 2\ \text{k}\Omega$ and $C = 0.1\ \mu\text{F}$.

Solution We have for a second-order LPF from Eq. (6.69),

$$f_{CL} = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}\ \text{Hz}$$

$$f_{CL} = \frac{1}{2\pi \times \sqrt{(2\times 10^3\ 0.1\times 10^{-6})^2}} = 795.8 \cong 796\ \text{Hz}$$

6.16.2 High-Pass Active Filters (HPF)

A filter that allows or passes signals above a cut-off frequency f_{CH} is a high-pass filter and its ideal frequency response is shown in Fig. 6.35(b). A first-order high-pass filter uses one *RC* section consisting of a single resistor and capacitor is shown in Fig. 6.38(a) and its frequency response has a practical slope of 20 dB per decade, as shown in Fig. 6.38(b) [rather than the ideal response of Fig. 6.35(b)]. The voltage gain has a slope of 20 dB/decade up to the cut-off frequency and is constant at A_F above the cut-off frequency.

1. First-Order High Pass Active Filters

A first-order (first order means one *RC* section) high-pass filter using one resistor and one capacitor is shown in Fig. 6.38(a) and its frequency response has a practical slope of +20 dB per decade, as shown in Fig. 6.38(b). The separation between the pass band and stop band is not very steep and the region of uncertainty between pass band and stop band is not minimised; however, the gain of the system is given by the equation

$$A_f = 1+\frac{R_f}{R_1} \qquad [6.67(a)]$$

The expression for the cut-off frequency is given by

$$f_{CH} = \frac{1}{2\pi R_1 C_1}\ \text{Hz} \tag{6.71}$$

The gain of the system is given by the expression

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F\frac{f}{f_c}}{\sqrt{1+\left[\frac{f}{f_c}\right]^2}} \quad \text{where } A_F = 1+\frac{R_F}{R} \tag{6.72}$$

Now, the filter operation can be summarised using the gain equation as below:

(i) At very low frequencies, i.e. $f << f_{cH}$,

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

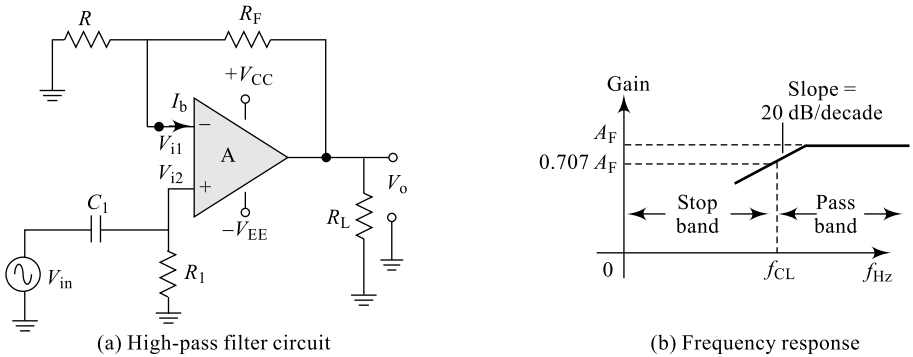
(ii) At frequencies that are comparable with f_{cH}, i.e. $f = f_{cH}$,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+1}} \cong 0.707 A_F$$

(iii) At frequencies that are above f_{cH}, i.e. $f >> f_{cH}$,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+0}} \cong A_F$$

Thus, an HPF has a constant gain of A_F from f_{CH} Hz to ∞, at cut-off frequency, the gain is 0.707 A_F and for frequencies below f_{CH}, the gain increases with a constant growth rate of 20 dB/decade.



(a) High-pass filter circuit (b) Frequency response

Fig. 6.39 First-order high-pass filter

Example 6.9

Calculate the cut-off frequency of a first-order high-pass filter whose R = 2 kΩ and C = 0.1 μF.

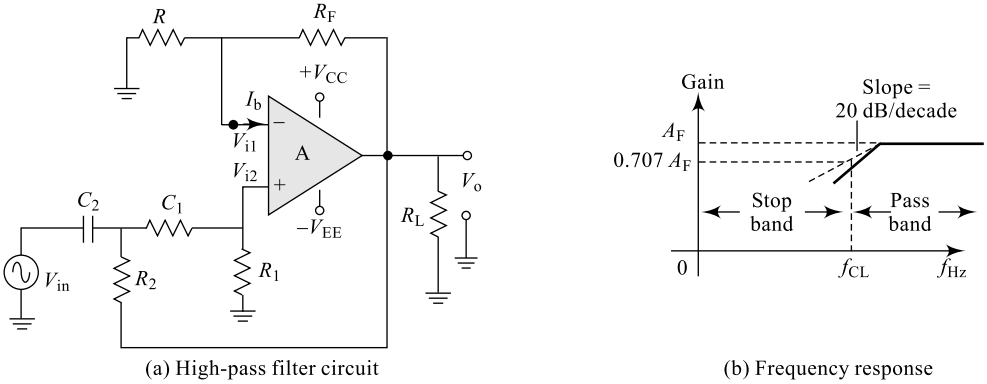
Solution We have for a first-order HPF from Eq. (6.71),

$$f_{CH} = \frac{1}{2\pi R_1 C_1} \text{ Hz}$$

$$f_{CH} = \frac{1}{2\pi \times 2 \times 10^3\ 0.1 \times 10^{-6}} = 795.8 \cong 796 \text{ Hz}$$

2. Second-Order High-Pass Active Filters

A second-order (second order means two *RC* sections) high-pass filter using two resistors and two capacitors is shown in Fig. 6.40(a) and its frequency response has a practical slope of –40 dB per decade, as shown in Fig. 6.40(b). Use of two *RC* sections improves the frequency response as shown. The separation between the pass band and stop band is very steep and the region of uncertainty between pass band and stop band is minimised; however, the gain of the system is limited to 1.586.



(a) High-pass filter circuit (b) Frequency response

Fig. 6.40 Second-order high-pass filter

The expression for the cut-off frequency is given by

$$f_{CL} = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}} \text{ Hz} \tag{6.73}$$

The gain of the system is given by the expression

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F\left[\frac{f}{f_c}\right]}{\sqrt{1+\left[\frac{f}{f_c}\right]^4}} \text{ where } A_F = 1 + \frac{R_F}{R} \tag{6.74}$$

Example 6.10

Calculate the cut-off frequency of a second-order high-pass filter whose $R = 2\ \text{k}\Omega$ and $C = 0.1\ \mu\text{F}$.

Solution We have for a second-order HPF from Eq. (6.73),

$$f_{CL} = \frac{1}{2\pi\sqrt{R_1 C_2 R_2 C_2}} \text{ Hz}$$

$$f_{CL} = \frac{1}{2\pi \times \sqrt{(2\times10^3\ 0.1\times10^{-6})^2}} = 795.8 \cong 796 \text{ Hz}$$

6.16.3 Band Pass Active Filters (BPF)

When the filter circuit allows or passes signals that are above one ideal cut-off frequency and below a second cut-off frequency, it is called a band-pass filter; its ideal frequency response is shown in Fig. 6.35(c). A first-order band-pass filter can, therefore, be a series cascading of a LPF and a HPF as shown in Fig. 6.41(a) with a condition that $f_{CL} > f_{CH}$. The HPF uses one *RC* section consisting of an R_1 and C_1 and the LPF uses one *RC* section consisting of an R_2 and C_2 as shown in Fig. 6.41(a). The frequency response has a practical slope of 20 dB per decade, as shown in Fig. 6.41(c). The voltage gain has a slope of 20 dB/decade up to the cut-off frequency f_{CH}, is constant at A_F between the cut-off frequencies and has a slope of –20 dB/decade after the cut-off frequency f_{CL}.

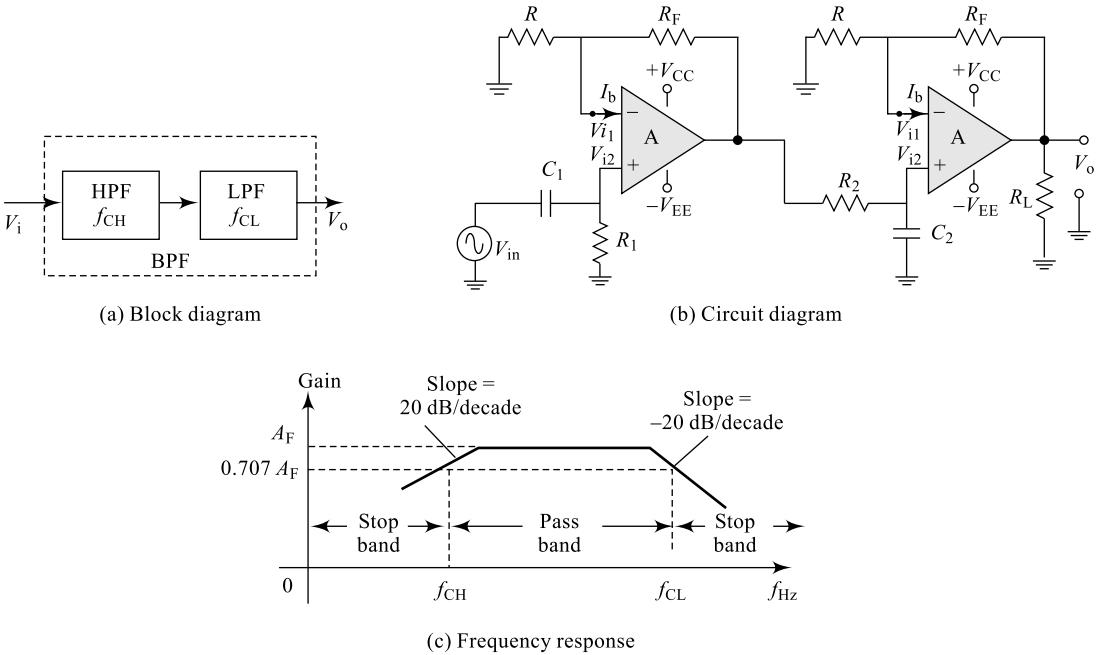


Fig. 6.41 Band-pass filter

The expression for the cut-off frequencies is given by equations (6.67) and (6.71) which are reproduced here for convenience and minor corrections:

$$f_{CH} = \frac{1}{2\pi R_1 C_1}\text{Hz} \quad \text{and} \quad f_{CL} = \frac{1}{2\pi R_2 C_2}\text{Hz} \tag{6.75}$$

The BPF can be classified as a narrow band-pass filter or a wide band-pass filter depending on the value of a measuring factor called the ***Q*-factor** or **quality factor**. *Q*-factor is defined as the ratio of centre frequency to the bandwidth and for a BPF, it is given by

$$Q = \frac{f_C}{f_{CL} - f_{CH}} \text{ where } f_C = \sqrt{f_{CL} \times f_{CH}} \tag{6.76(a)}$$

Q-factor

*Q*uality or *Q*-factor is a figure of merit for a filter which is a measure of its selectivity; where selectivity of a filter is the ability of the filter to choose any bandlimited signal. It can be defined as the ratio of the centre frequency to the filter bandwidth:

$$Q = \frac{f_C}{f_{CL} - f_{CH}} \tag{6.76(b)}$$

Higher the value of Q, more selective will be the filter circuit. A bandlimited filter can be a narrowband filter if $Q > 10$ or a wide band filter if $Q < 10$.

Example 6.11

Design a band-pass filter with component values of R_1 = 2 kΩ, R_2 = 2 kΩ and C_1 = 0.05 μF, C_1 = 0.05 μF. Group these components so that circuits works as proper BPF (condition $f_{CL} > f_{CH}$ is satisfied)

Solution We have for a second-order HPF from Eq. (6.75)

$$f_{CH} = \frac{1}{2\pi R_1 C_1} \text{Hz}$$

$$f_{CH} = \frac{1}{2\pi \times 2 \times 10^3 \times 0.05 \times 10^{-6}} \text{Hz} = 1591.6 \cong 1592 \text{ Hz}$$

and

$$f_{CL} = \frac{1}{2\pi R_2 C_2} \text{Hz}$$

$$f_{CL} = \frac{1}{2\pi \times 2 \times 10^3 \times 0.01 \times 10^{-6}} \text{Hz} = 7957.75 \cong 7958 \text{ Hz}$$

R_1, C_1 form the HPF components and R_2, C_2 form the LPF components.

6.16.4 Band Elimination Active Filters (BEF)

When the filter circuit allows or passes signals that are below one ideal cut-off frequency and above a second cut-off frequency, in other words, a band of signals is rejected, it is called a band-elimination filter; its ideal frequency response is shown in Fig. 6.35(d). A first-order band-elimination filter can, therefore, be a parallel connection of a LPF and a HPF as shown in Fig. 6.42(a) with a summing amplifier to combine the outputs of LPF and HPF. The HPF uses one *RC* section consisting of an R_1 and C_1 and the LPF uses one *RC* section consisting of an R_2 and C_2 as shown in Fig. 6.42(b). The frequency response has a practical slope of 20 dB per decade, as shown in Fig. 6.42(c). The voltage gain has a slope of 20 dB/decade between cut-off frequencies f_{CL} and f_{CH}, is constant at A_F beyond these cut-off frequencies.

The expression for the cut-off frequencies is given by equations (6.67) and (6.71) which are reproduced in Eq. (6.75).

Example 6.12

Design a band-elimination filter with component values of R_1 = 2 kΩ, R_2 = 2 kΩ and C_1 = 0.01 μF, C_2 = 0.05 μF. Group these components so that circuits works as proper BEF (condition $f_{CL} < f_{CH}$ is satisfied)

Solution We have for a second-order HPF from Eq. (6.75),

$$f_{CL} = \frac{1}{2\pi R_1 C_1} \text{Hz}$$

$$f_{CL} = \frac{1}{2\pi \times 2 \times 10^3 \times 0.05 \times 10^{-6}} \text{Hz} = 1591.6 \cong 1592 \text{ Hz}$$

and

$$f_{CH} = \frac{1}{2\pi R_2 C_2} \text{Hz}$$

$$f_{CH} = \frac{1}{2\pi \times 2 \times 10^3 \times 0.01 \times 10^{-6}} \text{Hz} = 7957.75 \cong 7958 \text{ Hz}$$

R_1, C_1 form the LPF components and R_2, C_2 form the HPF components.

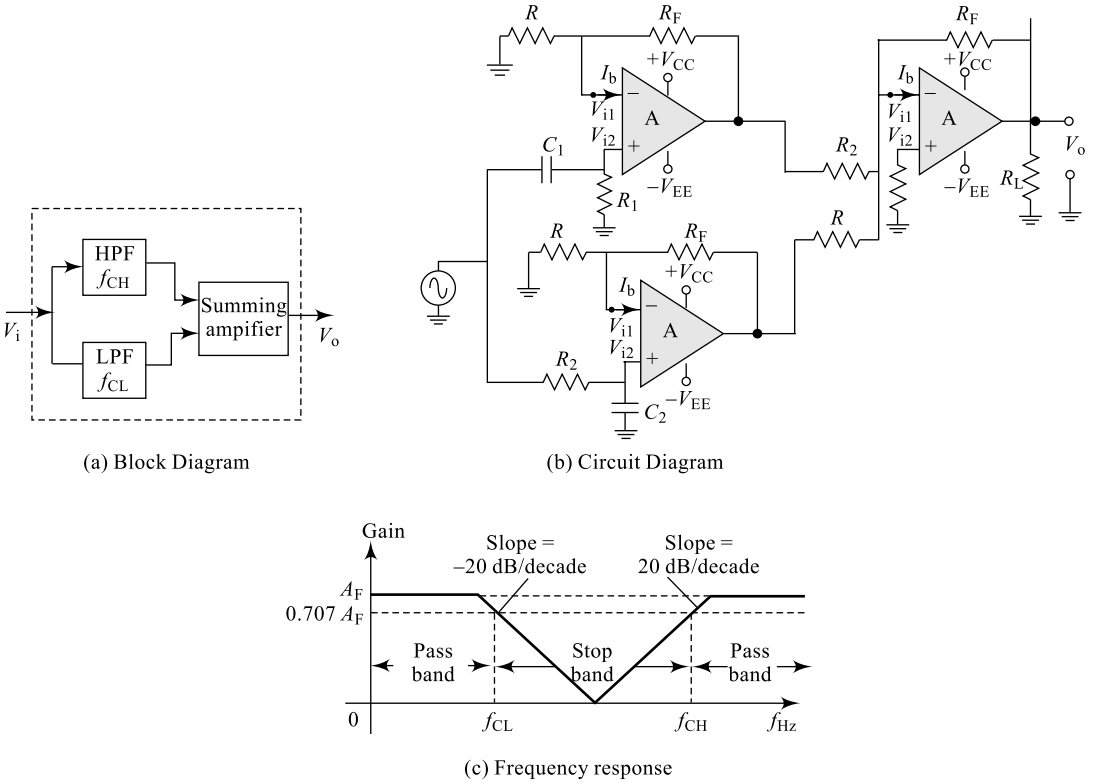
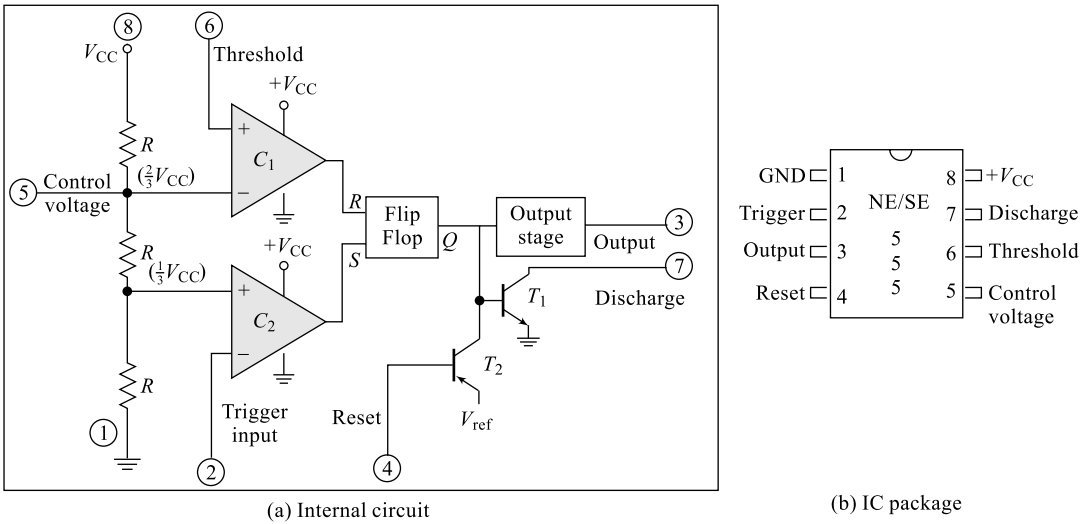


Fig. 6.42 Band elimination filter

The BEF can be called a **notch filter** (narrowband reject) or a wideband reject filter depending on the value of the *Q*-factor.

6.17 TIMER-555

Another important and very popular analog–digital integrated circuit is the most versatile 555 timer from Signetics Corporation. The IC is made up of a combination of linear components such as comparators, buffers, BJTs and digital components such as flip-flops and inverters as indicated in Fig. 6.43(a). This timer has a varieties of applications like Mono-stable Multi-Vibrator (MMV), Astable Multi-Vibrator (AMV), ramp generator, capacitance meter, etc. The entire circuit is housed in an 8-pin dual-in-line package (DIP) as shown in Fig. 6.43(b). Some of the important characteristics of this IC, which contribute to its versatility, are operating temperature range of –55°C to +125°C (for SE-555 and 0 to 70°C for NE-555), operating supply voltage range of +5 V to +18 V, wide timing range from microseconds to hours and a current sourcing of 200 mA. The internal schematic of the timer IC shown consists of a series connection of three equal resistors *R* that sets the reference voltage levels to the two comparators C_1 and C_2 at $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$ respectively. The output of these comparators either sets or resets the flip-flop unit and the output of the flip-flop is then brought out through an output inverter stage. The flip-flop unit also operates a transistor inside the IC, the transistor collector usually being driven low to discharge a timing capacitor.



(a) Internal circuit

(b) IC package

Fig. 6.43 IC-555 timer

When the voltage at the threshold terminal (Pin-6) exceeds $2V_{CC}/3$, output of comparator C_1 goes high and resets the FF, which in turn switches timer output low. This drives T_1, the discharge transistor into saturation and any source connected to discharge terminal (Pin-7) can easily discharge into T_1. Similarly, if the voltage at the trigger input (Pin-2) falls below $V_{CC}/3$, the output of the comparator C_2 goes high and sets the FF, which in turn switches the timer output high. This drives T_1, the discharge transistor, the out of saturation and the discharge terminal becomes inactive. RESET terminal (Pin-4) helps in forcing the output to zero unconditionally; when the potential at this terminal is brought sufficiently down driving T_2 into saturation, timer output will be zero. Under normal working conditions this terminal is tied to V_{CC}. The control voltage terminal (Pin-5) is used in special applications such as modulation, de-modulation (discussed in Chapter 5), ramp generation, etc. otherwise this pin is connected to grounded through a 0.01 μF capacitor. Some of the important applications are discussed in the following sections.

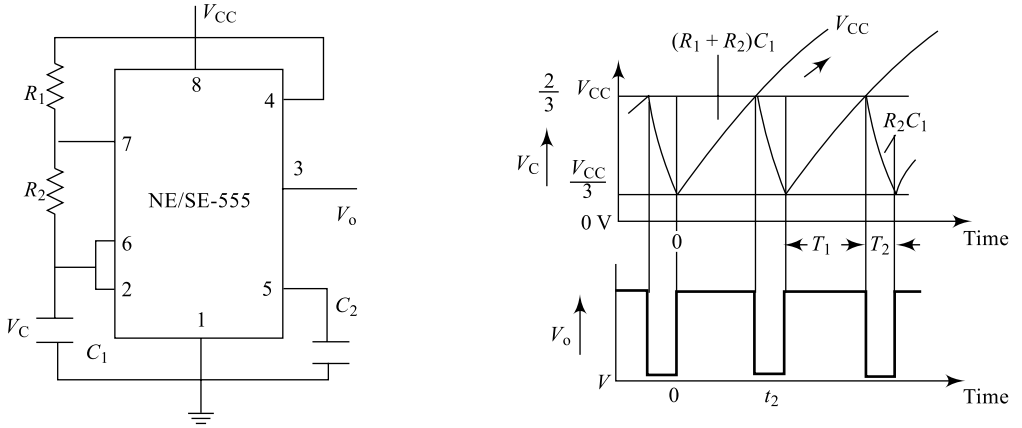
6.17.1 Astable Multivibrator Operation

One popular application of the 555 timer IC is an astable multivibrator or a clock circuit or a square-wave generator. Figure 6.44(a) shows an astable multivibrator circuit built using IC-555; an external capacitor C_1, resistors R_1 and R_2 set the timing interval of the output signal. The trigger input Pin-2 and threshold Pin-6 are shorted together and receive their reference potential from the capacitor voltage V_C. The control voltage Pin-5 is grounded through a 0.01 μF capacitor and the RESET Pin-4 is connected to V_{CC}.

1. Working

Assuming a zero initial charge, the voltage on the capacitor will be zero and when V_{CC} is applied to the circuit, the capacitor starts charging in an exponential fashion towards V_{CC}. The charging path has a resistance $(R_1 + R_2)$ and hence, the charging time constant is

$$\tau_1 = (R_1 + R_2)C \tag{6.77}$$



(a) Circuit diagram (b) Waveforms

Fig. 6.44 Timer IC-555 astable multivibrator

With $V_C = 0$ V, the output of the comparator C_2 will be high that sets the FF and hence the timer output; this drives T_1 into cut-off, the discharge terminal is inactive and the capacitor accumulates voltage. At time interval t_1, the rising capacitor voltage reaches and just exceeds $2V_{CC}/3$; output of the comparator C_1 goes high that resets the FF and hence, the timer output; this drives T_1 into saturation, the discharge terminal becomes active and the capacitor discharges into T_1; this is indicated in the waveforms shown in Fig. 6.43(b). The discharging path has a resistance R_2 and hence the discharging time constant is

$$\tau_2 = R_2C \tag{6.78}$$

Again, at time interval t_2, the decreasing capacitor voltage reaches and just falls below $V_{CC}/3$; output of the comparator C_2 goes high that sets the FF and hence the timer output; this drives T_1 into cut-off, the discharge terminal is inactive and the capacitor accumulates voltage. The process repeats every time the capacitor voltage v_C crosses $2V_{CC}/3$ and $V_{CC}/3$, resulting in an output voltage signal that oscillates between 0 V and $+V_{CC}$ at a frequency f Hz. The expression for this output frequency can be obtained as

$$f = \frac{1}{T_1 + T_2} \tag{6.79}$$

T_1 and T_2 values can be approximated starting from the instantaneous capacitor voltage equation

$$\vartheta C = V_F - (V_F - V_{int})\, e^{\frac{t}{RC}} \tag{6.80}$$

Here, V_F = Final voltage on capacitor (towards which the capacitor is aiming at) = V_{CC}

V_{int} = Initial voltage on capacitor (from which the capacitor begins charging) = $V_{CC}/3$

RC associated time constant = $(R_1 + R_2)C$

$$\therefore \qquad \vartheta C = V_{CC} - \left(V_{CC} - \frac{V_{CC}}{3}\right) e^{-\frac{t}{(R_1 + R_2)C}}$$

But at the end of the time interval $t_1 = T_1$, the capacitor voltage will be $\vartheta C = \frac{2V_{CC}}{3}$ and hence,

$$\frac{2V_{CC}}{3} = V_{CC} - \left(V_{CC} - \frac{V_{CC}}{3}\right) e^{-\frac{T_1}{(R_1 + R_2)C}}$$

$$\frac{2}{3} = 1 - \left(1 - \frac{1}{3}\right) e^{-\frac{T_1}{(R_1 + R_2)C}}$$

which on simplification results in an expression for T_1

$$T_1 = 0.693(R_1 + R_2)C \tag{6.81}$$

Similarly, an expression for time period T_2 can obtained; here

V_F = Final voltage on capacitor towards which the capacitor is aiming at = 0 V

V_{int} = Initial voltage on capacitor from which the capacitor begins charging = $2V_{CC}/3$

RC associated time constant = R_2C

$T_2 = 0.693R_2C$ (6.82)

Now, Eq. (6.66) can be rewritten as

$$f = \frac{1}{T_1 + T_2} = \frac{1}{0.693(R_1 + R_2 + R_2)C} \tag{6.83}$$

$$f = \frac{1.4}{(R_1 + 2R_2)C}\text{Hz} \tag{6.84}$$

2. Duty Cycle

Duty cycle of a signal is defined as the ratio of ON period to the total period. For the output square wave generated, the period is T_1 and the total period is $(T_1 + T_2)$ and hence, the duty cycle is expressed as

$$\Delta = \frac{T_1}{T_1 + T_2} \tag{6.85}$$

Duty cycle of a signal can also be defined as the product of ON period and the signal frequency, i.e.

$\Delta = T_1 \times f$ (6.86)

Example 6.13

Calculate the ON and OFF periods for the output clock generated by an AMV using IC-555; the timing resistors are R_1 = 10 kΩ, R_2 = 10 kΩ and the capacitor is 1 μF.

Solution We have from Eq. (6.81)

$$T_1 = 0.693(R_1 + R_2)C$$
$$= 0.693(10k + 10k) \times 1\ \mu F$$
$$\boldsymbol{T_1 = 13.86\ mS}$$

Similarly, we have from Eq. (6.82)

$$T_2 = 0.693R_2C$$
$$= 0.693 \times 10k \times 1\ \mu F$$
$$\boldsymbol{T_2 = 6.93\ mS}$$

Example 6.14

Calculate the frequency of the output and the duty cycle for the clock generated by the AMV using IC-555 in Example 6.20.

Solution We have from Eq. (6.83)

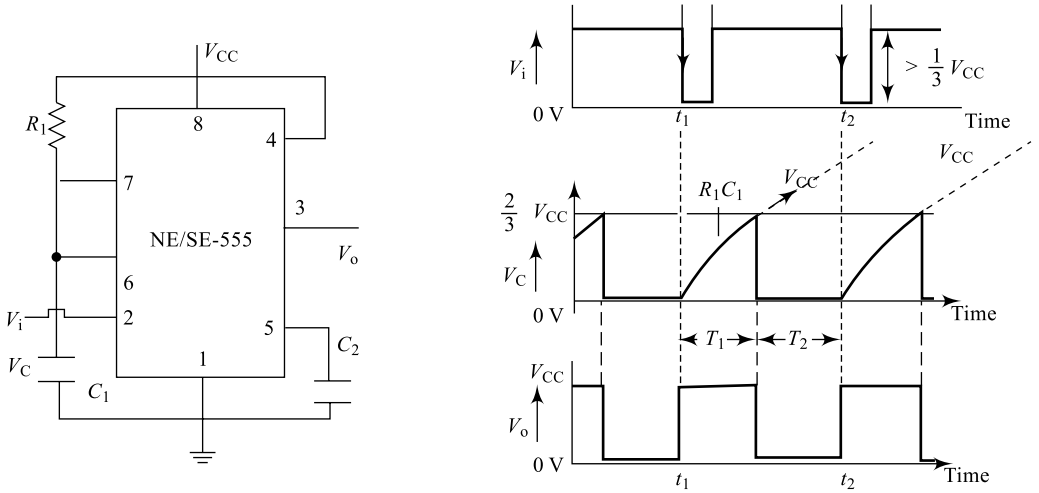
$$f = \frac{1}{T_1 + T_2} = \frac{1}{13.86\ \text{mS} + 6.93\ \text{mS}} = 48.1 \cong 48\ \text{Hz}$$

or,
$$f = \frac{1.4}{(R_1 + 2R_2)C}\text{Hz}$$
$$f = \frac{1.4}{(10\text{K} + 2 \times 10\text{K})1\,\mu\text{F}} = 46.667 \cong 47\ \text{Hz}$$

Similarly, We have from Eq. (6.85), duty cycle
$$\Delta = \frac{T_1}{T_1 + T_2} = \frac{13.86\ \text{mS}}{13.86\ \text{mS} + 6.93\ \text{mS}} = 0.667$$

6.17.2 Monostable Multivibrator Operation

Another popular application of the 555 timer IC is as a monostable multivibrator. Figure 6.44(a) shows a monostable multivibrator circuit built using IC-555; an external capacitor C_1, resistor R_1 sets the width of the pulse output signal. Pin-2 is connected with the trigger input signal V_i, the magnitude of which should be a minimum of $V_{CC}/3$. Discharge Pin-7 and threshold Pin-6 are shorted together and receive their reference potential from the capacitor voltage V_C. The control voltage Pin-5 is grounded through a 0.01 μF capacitor and the RESET Pin-4 is connected to V_{CC}.



(a) Circuit diagram (b) Waveforms

Fig. 6.45 Timer IC-555 monostable multivibrator

Working

Assuming a zero initial charge, the voltage on capacitor will be zero and with $V_C = 0$ V, the output will be at high (stable) state. When a negative-going triggering signal V_i is applied to Pin-2 at $t = 0$, the output of the comparator C_2 goes high that sets the FF and hence the timer output; this drives T_1 into cut-off, the discharge terminal is inactive. Now, the capacitor starts charging in an exponential fashion towards V_{CC} with a charging path resistance of R_1 and hence, the charging time constant is

$$\tau_1 = R_1 C \tag{6.87}$$

The capacitor starts accumulating voltage and at the time interval t_1, the rising capacitor voltage reaches and just exceeds $2V_{CC}/3$; output of comparator C_1 goes high that resets the FF and hence, the

timer output; this drives T_1 into saturation, the discharge terminal becomes active and the capacitor discharges into T_1; this is indicated in the waveforms shown in Fig. 6.44(b). The discharging path has only negligible saturation resistance of transistor T_1 and hence, the discharging time constant is almost zero.

Again, at time interval t_2, if another triggering input is applied, the process repeats resulting in another pulse, the width of which can be estimated using the instantaneous capacitor voltage equation

$$\vartheta c = V_F - (V_F - V_{int})e^{-\frac{t}{RC}} \tag{6.88}$$

Here, V_F = Final voltage on capacitor (towards which the capacitor is aiming at) = V_{CC}

V_{int} = Initial voltage on capacitor (from which the capacitor begins charging) = 0 V

RC associated time constant = R_1C

$$\therefore \quad \vartheta c = V_{CC} - (V_{CC} - 0)e^{-\frac{t}{R_1C}}$$

But at the end of the time interval $t_1 = T_1$, the capacitor voltage will be $\vartheta C = \frac{2V_{CC}}{3}$ and hence,

$$\frac{2V_{CC}}{3} = V_{CC} - (V_{CC} - 0)e^{-\frac{T_1}{R_1C}}$$

$$\frac{2}{3} = \left(1 - e^{-\frac{T_1}{(R_1 + R_2)C}}\right)$$

which on simplification results in an expression for T_P;

$$T_P = 1.099R_1C \tag{6.89}$$

Example 6.15

Calculate the pulse period for the output generated by a MMV using IC-555; the timing resistor R_1 = 10 kΩ and the capacitor is 1 μF.

Solution We have from Eq. (6.89)

$$T_P = 1.099\ R_1C$$

$$= 1.099 \times 10k \times 1\ \mu F$$

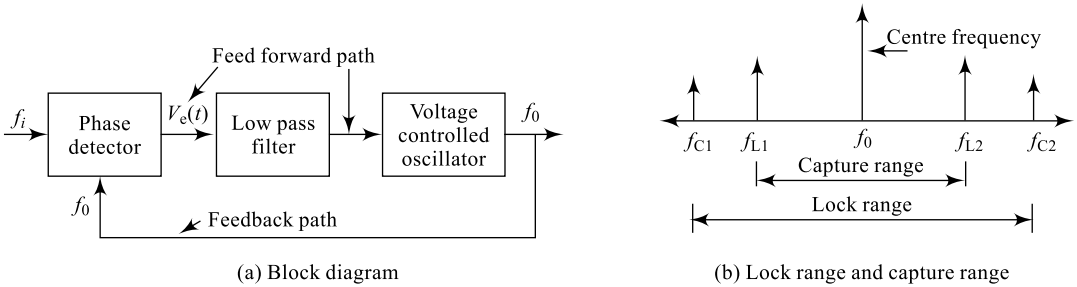
$$\mathbf{T_P = 10.99\ mS}$$

6.18 PLL-565

A Phase-Locked Loop (PLL) is one of the important linear ICs that finds varieties of system-building applications such as frequency multiplier, frequency synthesiser, FM stereo detector, motor speed controller, etc. A PLL is essentially a frequency feedback system and the basic block diagram of a PLL consists of a phase detector, a low-pass filter and a voltage-controlled oscillator (VCO) as indicated in Fig. 6.46 on next page. It can be observed here that the system consists of a feed-forward path and a feedback path.

6.18.1 PLL Block Diagram and Basic Definitions

The **phase comparator** compares the input signal frequency (phase) f_i with the output signal frequency (phase) f_O and produces an error voltage $V_{e(t)}$ that is proportional to the frequency (phase) difference between the two. The output of the phase detector $V_{e(t)}$ is then applied to a **Low-Pass Filter** (LPF) to



(a) Block diagram (b) Lock range and capture range

Fig. 6.46 Block diagram of a PLL

remove the high-frequency noise and produce a dc signal. This dc signal is now used to drive a **Voltage-Controlled Oscillator** (VCO) which is essentially a voltage-to-frequency convertor. The output frequency of VCO is proportional to the dc signal which is the difference between f_i and f_O; f_O is adjusted until it equals f_i. In order to achieve this, a PLL goes through three different states to produce a constant and stable output frequency f_O; a free running state, a capture state and a phase-lock state.

Before an input signal is applied, the PLL is generating an output signal f_O which is compared with itself producing a known error voltage. This frequency is called the **free running frequency** or **centre frequency** and this state of PLL is called a free running state. Once the input f_I is applied, the phase comparator starts producing an error signal that is proportional to the phase or frequency difference between the two signals. This error voltage forming the input to LPF, produces an output dc signal to drive VCO. Now, VCO output starts changing continuously until f_i equals f_O and this state of PLL is called **capture state**. The VCO output continues to change till the phase or frequency difference between the input signal and the feedback signal becomes zero and this state of PLL is called the **phase-lock state**. When phase locked, the closed-loop tracks any small change in f_i within certain limits and produces an output which is highly stable.

In the free running state, without any applied input signal, the PLL will be producing a free running frequency f_O. Now, if the signal of frequency f_i is applied to the input, the PLL starts synchronising with the input signal and in the process enters into the two important states called capture state and lock state. The following two important definitions can be given for the PLL:

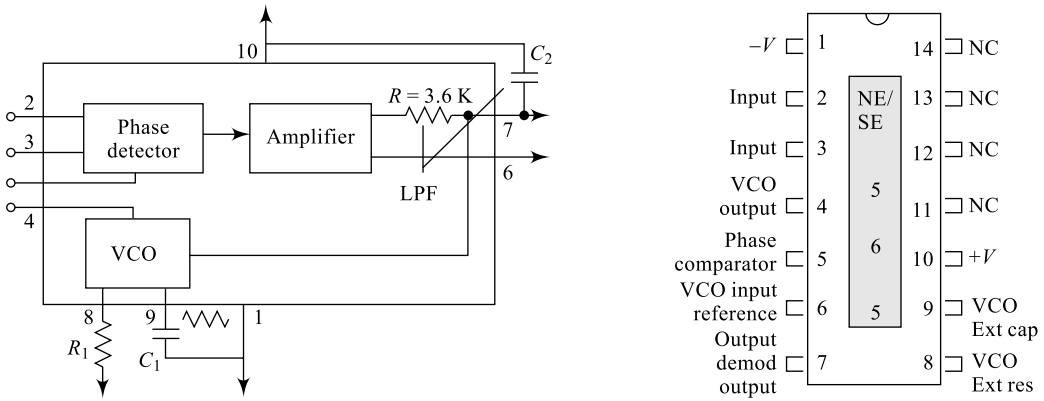
1. Capture Range

Once f_i is applied to the PLL, the phase detector produces an error voltage that is proportional to the phase (frequency) difference between f_i and f_O. This error voltage is applied as input to the VCO; the VCO produces a voltage that changes continuously till the phase (frequency) difference between f_i and f_O becomes zero. This process is called capture process, and the range of frequencies about f_O over which the PLL *establishes synchronisation* between f_i and f_O is called capture range.

2. Lock Range

Once f_i is synchronised with the f_O, the phase detector produces a zero error voltage (that means the phase (frequency) difference between f_i and f_O is zero) and this will continue over a range of input frequencies. This process is called lock process, and the range of frequencies about f_O over which the PLL *maintains synchronisation* between f_i and f_O is called the lock range.

This is clearly indicated in Fig. 6.45(b). The design equations for capture and lock range can be given based on the block diagram of a commercially available PLL IC-565 from Signetics Corporation or National semiconductors shown in Fig. 6.46(a) and the corresponding pin-out diagram is shown in Fig. 6.46(b).



(a) IC-565 block diagram

(b) IC-565 Pin-out

Fig. 6.47 Commercial PLL IC-565

The design equations for f_O, f_C and f_L are given as below:

(i) $$f_o \cong \frac{1.2}{4R_1C_1}\text{Hz} \tag{6.90}$$

(ii) $$f_L \cong \pm\frac{8f_o}{V}\text{Hz} \tag{6.91}$$

(iii) $$f_C \cong \pm\left[\frac{f_L}{2\pi(3.6\times10^3)C_2}\right]^{\frac{1}{2}}\text{Hz} \tag{6.92}$$

6.18.2 PLL Applications

PLL is a most versatile linear IC that can be used as one of the most important building blocks in linear system designs. These applications are not discussed in detail in this text as this is a basic course textbook; however, these applications are listed for all needed reference. The most important PLL applications include

(i) Frequency Multiplication Input frequency is going to be multiplied by an integer value N so that $f_O = Nf_{in}$.

(ii) Frequency Translation Input frequency is going to be mixed with a reference signal f_R so that $f_O = f_R \pm f_{in}$.

(iii) AM Detection PLL is used to demodulate an Amplitude modulated signal (modulation/demodulation schemes are discussed in Chapter 5).

(iv) FM Detection PLL is used to demodulate a frequency-modulated signal.

(v) FSK detection PLL is used to demodulate a Frequency Shift Key (FSK, type of modulation/demodulation) modulated signal.

Summary

- ➢ Linear ICs respond to linear analog inputs which are time varying.
- ➢ Digital ICs respond to digital signal levels "TRUE" or "FALSE".
- ➢ An operational amplifier uses a differential amplifier as the building block.
- ➢ A differential amplifier amplifies difference in the two input signals.
- ➢ Differential operation involves the use of opposite-polarity inputs.
- ➢ Common-mode operation involves the use of the same-polarity inputs.
- ➢ Common-mode rejection compares the gain for differential inputs to that for common inputs.
- ➢ Common-mode rejection ratio speaks about the ability of op-amp to reject common mode inputs.
- ➢ The basic features of an op-amp are:
  - Very high input impedance (typically Mega Ohms),
  - Very high voltage gain (typically a few hundred thousands),
  - Low output impedance (typically less than few 100 Ohms),
  - Very high bandwidth (typically few hundred thousand Hertz),
  - Very high slew rate(typically few tens of V/μs),
  - Very high common mode rejection ratio(typically few hundreds of dBs).
- ➢ Virtual ground is a concept based on the practical fact that the differential input voltage between plus and minus inputs is nearly (virtually) zero volts (very high voltage gain).
- ➢ Basic op-amp applications include:
  - Inverting amplifier
  - Non-inverting amplifier
  - Unity-gain amplifier
  - Summing amplifier
  - Difference amplifier
  - Integrator amplifier
  - Differentiator amplifier
  - Instrumentation amplifier
  - Comparators and Schmitt triggers
- ➢ Important op-amp specifications include:
  - Offset voltages and currents
  - Frequency parameters
  - Gain–bandwidth
  - Slew rate
  - Common Mode rejection ratio
  - Input and output impedances
- ➢ Active filters offer a good number of advantages over passive filters such as good input impedance and output impedance, good gain, good frequency response, good noise rejection and many more.
- ➢ The IC-555 timer is another most versatile linear IC that finds good number of applications in electronic system building.
- ➢ Typical IC-555 timer applications include multivibrators, ramp generators, capacitance meters, etc.
- ➢ PLL is another powerful linear IC that finds a good number of communication applications.
- ➢ Typical PLL applications include frequency multiplication, frequency translation, AM/FM generation, detection, FSK detection, etc.

Review Questions

1. Sketch the output waveform for the circuit of Fig. P6.1 for a sinusoidal input of $2V_{(peak)}$.
2. Sketch the output waveform for the circuit of Fig. P6.1 for a sinusoidal input of $2V_{(peak)}$ when R_{in} is increased tenfold.
3. Sketch the output waveform for the circuit of Fig. P6.1 for a sinusoidal input of $2V_{(peak)}$ when R_f is decreased tenfold.
4. For the circuit of Fig. P6.1, what is the maximum input signal that results in an undistorted output?
5. What is the role of level shifter in an op-amp? Explain.
6. What is the meaning of virtual ground? On what assumption do we arrive at this concept?
7. Sketch the output waveform for the circuit of Fig. P6.7 for a sinusoidal input of $2V_{(peak)}$.
8. Sketch the output waveform for the circuit Fig. P6.7 for a sinusoidal input of $2V_{(peak)}$ when R_{in} is increased tenfold.
9. Sketch the output waveform for the circuit of Fig. P6.7 for a sinusoidal input of $2V_{(peak)}$ when R_f is decreased tenfold.
10. For the circuit of Fig. P6.7, what is the maximum input signal that results in an undistorted output?
11. List the major functions of each block in an op-amp.
12. Obtain the operating point for a dual input, balanced output DA.
13. What is the significance of off sets in an op-amp?
14. What is the significance of input impedance in an op-amp?
15. What is the significance of output impedance in an op-amp?
16. What is the significance of slew rate in an op-amp?
17. What is the significance of CMRR in an op-amp?
18. What is the significance of PSRR an op-amp?
19. What is the significance of unity gain bandwidth 'f_U' in an op-amp?
20. What is the significance of full power bandwidth 'f_P' in an op-amp?
21. Draw the transfer characteristics for an op-amp and comment on region of uncertainty.
22. What is the role of a buffer in system design using op-amps?
23. Explain how a buffer is different from a non-inverter.
24. An even number of buffers are cascaded together. What is the output expected for a sine-wave input?
25. An integrator with a square-wave input is driving a differentiator. What is the expected output of this cascaded combination?
26. Comment whether designing an Inverting type Op-Amp Summer is complex or a Non-Inverting type Op-Amp Summer?
27. An integrator with a sine wave input is driving a differentiator. What is the expected output of this cascaded combination?
28. A single op-amp difference amplifier fails to offer equal loading to the two input sources; explain why.
29. A two-op-amp difference amplifier also fails to offer equal loading to the two input sources; explain why.
30. An instrumentation amplifier or a three-op-amp difference amplifier offers equal loading to the two input sources; explain how.

31. An instrumentation amplifier or a three-op-amp difference amplifier offers equal loading to the two input sources; explain how.
32. An instrumentation amplifier or a three-op-amp difference amplifier offers equal loading to the two input sources; explain how.
33. An instrumentation amplifier or a three-op-amp difference amplifier offers equal loading to the two input sources; explain how.
34. An instrumentation amplifier or a three-op-amp difference amplifier offers equal loading to the two input sources; explain how.
35. An instrumentation amplifier or a three-op-amp difference amplifier offers equal loading to the two input sources; explain how.

Exercise Problems

1. The input to the circuit of Fig. P6.1 is a sinusoidal input of $2V_{(rms)}$. Calculate the peak value of voltage and plot the output wave form.
2. What input voltage results in an output of $2V_{(P\text{-}P)}$ in the circuit of Fig. P6.1?
3. What is the range of the output voltage in the circuit of Fig. P6.1 if the input varies from 0.1 to 0.5 V and R_{in} is raised by 50%?
4. What is the range of the output voltage in the circuit of Fig. P6.1 if the input resistance is a potentiometer that varies from $10k$ to $20k$ and V_{in} is 1V?
5. What input voltage results in an output of $V_{out} = -1.5V$ in the circuit of Fig. P6.1?
6. What output voltage is resulted if the R_{in} and R_F are interchanged in the Fig. 6.1 with an input of 10 V?
7. The input to the circuit of Fig. P6.7 is a sinusoidal input of $2V_{(rms)}$, Calculate the peak value of voltage and plot the output waveform.
8. What input voltage results in an output of $2V_{(P\text{-}P)}$ in the circuit of Fig. P6.7?
9. What is the range of the output voltage in the circuit of Fig. P6.7 if the input varies from 0.1 to 0.5 V and R_{in} is raised by 50%?

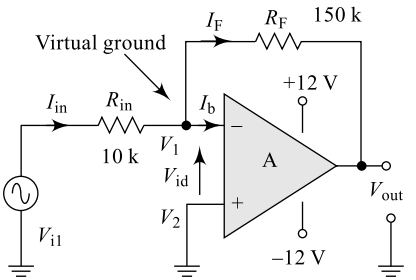


Fig. P6.1

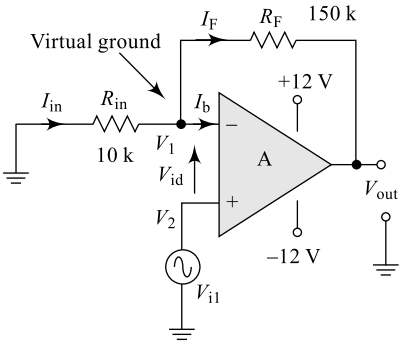


Fig. P6.7

11. What is the range of the output voltage in the circuit of Fig. P6.7 if the input resistance is a potentiometer that varies from $10k$ to $20k$ and V_{in} is 1 V?
12. What input voltage results in an output of $V_{out} = +1.5$ V in the circuit of Fig. P6.7?
13. What output voltage is resulted if the R_{in} and R_F are interchanged in Fig. 6.7 with an input of 10 V?
14. **a.** Calculate the output voltage V_O in the circuit of Fig. P6.14 given $V_{in} = 5 \text{ Sin } \omega t$.
    b. Plot the output voltage, V_O with respect to V_{in}.

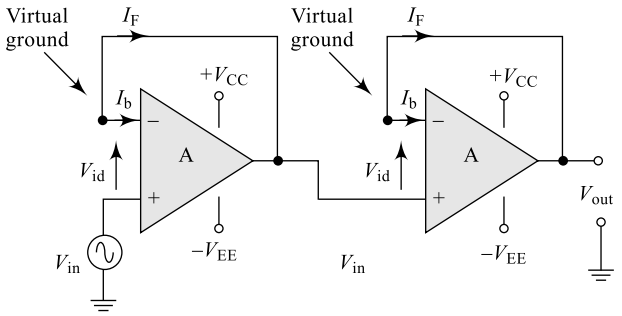


Fig. P6.14

15. **(a)** Calculate the output voltage V_O in the circuit of Fig. 6.14 given V_{in} =15 Sin ωt.
(b) Plot the output voltage, V_O with respect to V_{in}.

16. Calculate the total output voltage for the circuit of Fig. P6.16 given V_1 = 200 mV, V_2 = 400 mV and V_3 = 800 mV.

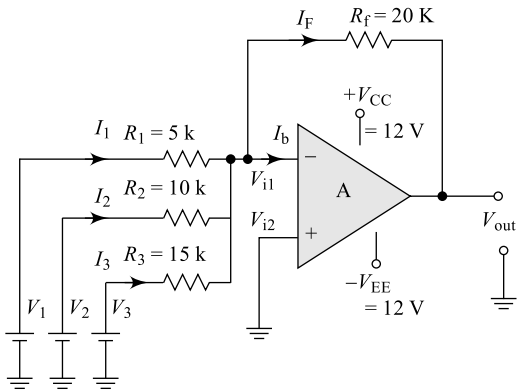


Fig. P6.16

17. Calculate the total output voltage for the circuit of Fig. P6.16 if all the inputs are tied together and supplied with a voltage source of V_{in} = 200 mV.

18. Calculate and plot to scale the total output voltage for the circuit of Fig. P6.16 if all the inputs are tied together and supplied with a voltage source of $V_{in} = 0.2 \sin \omega t$.

19. In problem 17, calculate the maximum value of input voltage that results in an undistorted output.

20. Calculate the total output voltage for the circuit of Fig. P6.20 if all the inputs are tied together and supplied with a voltage source of V_{in} = 200 mV.

21. Calculate and plot to scale the total output voltage for the circuit of Fig. P6.20 if all the inputs are tied together and supplied with a voltage source of $V_{in} = 0.2 \sin \omega t$.

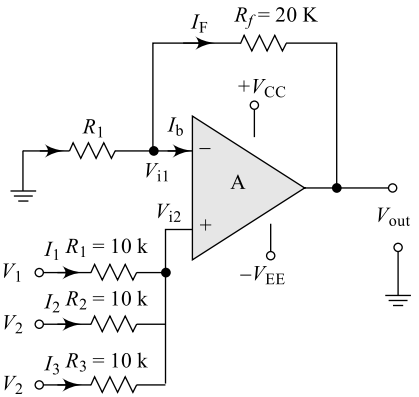


Fig. P6.20

22. In problem 20, calculate the maximum value of input voltage that results in an undistorted output.

23. Determine the output voltage for the circuit of Fig. P6.23 if V_1 = 4000 mV and V_2 = 2000 mV given the supply voltages are 12 V.

24. For the circuit of Fig. P6.20, calculate the output voltage if V_1 and V_2 are same.

25. Calculate time constant τ for the circuit of Fig. 6.25 and plot output if V_{in} is a square wave of $10V_{P\text{-}P}$ amplitude for (i) $\tau << T$, (ii) $\tau >> T$, and (iii) $\tau \cong T$

26. Calculate time constant τ for the circuit of Fig. 6.26 and plot output if V_{in} is a square wave of $10V_{P\text{-}P}$ amplitude for (i) $\tau << T$, (ii) $\tau >> T$, and (iii) $\tau \cong T$

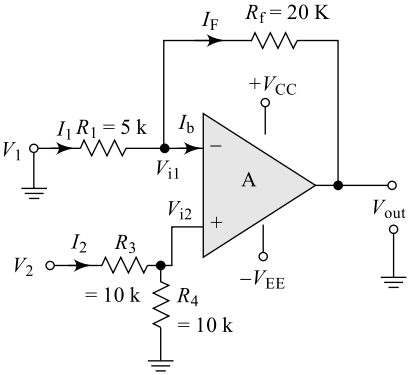


Fig. P6.23

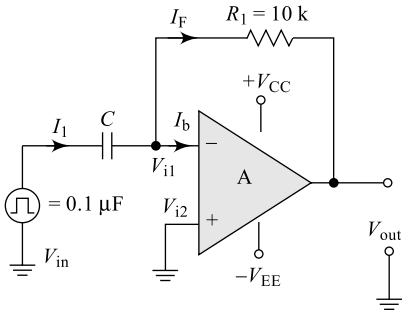


Fig. P6.25

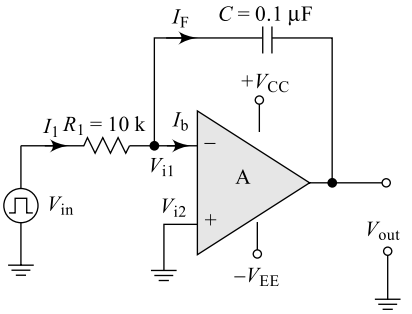


Fig. P6.26

27. Plot output V_O if V_{in} is a square wave of $10V_{P\text{-}P}$ amplitude in the circuit of Fig. P6.27.

28. Design an op-amp Schmitt trigger circuit to meet the following specifications: LTP = 2V, UTP = 4V and supply voltages $V_{CC} = \pm 12$ V.

29. Calculate the values of LTP and UTP in the op-amp Schmitt trigger circuit of Fig. P6.29, given supply voltages are $V_{CC} = \pm 12$V.

30. Design a low-pass filter for a cut-off frequency of 1KHz with a pass-band gain of 2.

31. Plot the frequency response for the low-pass filter of problem 29.

32. Design a high-pass filter for a cut-off frequency of 2KHz with a pass-band gain of 2.

33. Plot the frequency response for the low pass filter of Problem 33.

34. Design a band-pass filter for cut-off frequencies of 2 KHz and 5 KHz with a pass-band gain of 2.

35. Calculate the Q-factor for the circuit of problem 34 and Draw the designed circuit.

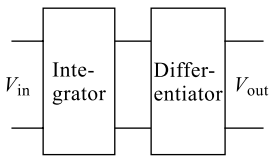


Fig. P6.27

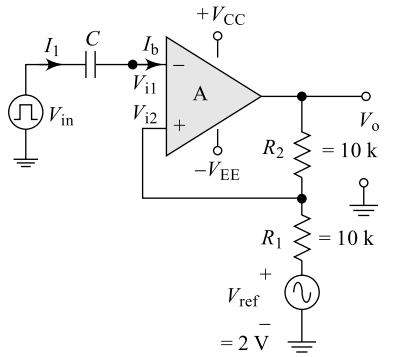


Fig. P6.29

36. Design a band-elimination filter for cut-off frequencies of 2 KHz and 5 KHz with a pass band gain of 2

37. Calculate the Q-factor for the circuit of problem 36 and Draw the designed circuit.

38. Calculate the output frequency of an astable multivibrator using IC-555 having $R_1 = R_2 = 10\ \text{k}\Omega$ and $C_1 = 0.1\ \mu\text{F}$.

39. **(a)** Calculate the on period T_{ON} for a Monostable multivibrator using IC-555 having $R_1 = 10\ \text{k}\Omega$ and $C_1 = 0.1\ \mu\text{F}$.

(b) What should be the value of supply voltage to produce a pulse amplitude of ~10V?

Multiple-Choice Questions

1. Which of the following devices is very compact and require very less space in systems?
   (a) integrated circuits (b) solid state devices
   (c) vacuum tube devices (d) all the above
2. An integrated circuits is characterised by and requires very less space in systems of
   (a) very compact size (b) low power consumption
   (c) high speed (d) all the above
3. A Linear Integrated circuit responds to
   (a) analog signal (b) digital signal
   (c) neither (a) nor (b) (d) both (a) and (b)
4. An op-amp is a Linear integrated circuit that is
   (a) an *RC* coupled high-gain amplifier (b) a direct-coupled medium-gain amplifier
   (c) a direct-coupled high-gain amplifier (d) an *RC* coupled medium-gain amplifier
5. The basic building block of an op-amp is
   (a) an *RC* coupled amplifier (b) a differential amplifier
   (c) an oscillator (d) all the above
6. An op-amp can amplify
   (a) only ac signals (b) only dc signals
   (c) neither (a) nor (b) (d) both (a) and (b)
7. The first stage of an op-amp is
   (a) level shifter (b) single ended DA (c) double ended DA (d) driver amplifier
8. The second stage of an op-amp is
   (a) double ended DA (b) single ended DA (c) level shifter (d) driver amplifier
9. The third stage of an op-amp is
   (a) level shifter (b) single ended DA (c) double-ended DA (d) driver amplifier
10. The fourth stage of an op-amp is
    (a) driver amplifier (b) single ended DA (c) level shifter (d) double-ended DA
11. The first stage of an op-amp is mainly responsible for
    (a) input impedance (b) bandwidth (c) CMMR (d) all the above
12. The second stage of an op-amp is mainly responsible for
    (a) drift (b) stability
    (c) offset voltages and currents (d) all the above
13. The fourth stage of an op-amp is mainly responsible for
    (a) driving capability (b) output impedance
    (c) both (a) and (b) (d) neither (a) nor (b)

14. The ability of an op-amp to reject the common mode signals is termed as its
    (a) common-mode gain (b) differential mode gain
    (c) offset voltages (d) CMRR
15. The ability of an op-amp to respond to high frequency input signals is termed as its
    (a) drift (b) stability (c) slew rate (d) CMRR
16. The CMRR for an op-amp is usually expressed in
    (a) volts (b) decibels (dB) (c) Volts/S (d) Volts/μS
17. The Slew rate for an op-amp is usually expressed in
    (a) volts (b) decibels (dB) (c) Volts/S (d) Volts/μS
18. The open loop gain A_V of an op-amp is usually very high, of the order of
    (a) 10^{15} (b) 10^{25} (c) 10^{5} (d) 10^{50}
19. The input impedance of an op-amp is usually very high, of the order of
    (a) mega Ohms (b) kilo Ohms (c) micro-ohms (d) terra-ohms
20. The input impedance of an op-amp can be further improved by the use of
    (a) emitter follower (b) FET input stages
    (c) both (a) and (b) (d) neither (a) nor (b)
21. The stability of an op-amp can be further improved by the use of
    (a) constant-current source (b) large R_E
    (c) small R_E (d) emitter follower
22. The scale factor of an op-amp Inverter is the ratio of
    (a) Z_{in} to Z_O (b) Z_O to Z_{in} (c) R_{in} to R_F (d) R_F to R_{in}
23. The phase difference between input and output signal of an op-amp inverter is
    (a) Zero (b) 120° (c) 360° (d) 180°
24. The gain of an op-amp inverter with input R_1 and feedback R_F is given by
    (a) $A = 1 + \frac{R_F}{R_1}$ (b) $A = 1 + \frac{R_1}{R_F}$ (c) $A = +\frac{R_F}{R_1}$ (d) $A = -\frac{R_F}{R_1}$
25. The gain of an op-amp circuit with supply voltages of ±12 V is limited to
    (a) around 11V (b) around 1V (c) around 11mV (d) around 11mV
26. The gain of an op-amp Non-Inverter with input R_1 and feedback R_F is given by
    (a) $A = 1 + \frac{R_F}{R_1}$ (b) $A = 1 + \frac{R_1}{R_F}$ (c) $A = +\frac{R_F}{R_1}$ (d) $A = -\frac{R_F}{R_1}$
27. The phase difference between input and output signal of an op-amp non-inverter is
    (a) Zero (b) 120° (c) 270° (d) 180°
28. The gain of an op-amp non-inverter with input R_1 equal to feedback R_F is given by
    (a) Zero (b) 2 (c) 5 (d) 10
29. The input impedance of an op-amp non-inverter with feedback is given by
    (a) $R_{iF} = \frac{R_{in}}{(1 + A\beta)}$ (b) $R_{iF} = \frac{R_{in}}{(1 - A\beta)}$ (c) $R_{iF} = R_{in}(1 + A\beta)$ (d) none of the above
30. The output impedance of an op-amp non-inverter with feedback is given by
    (a) $R_{OF} = \frac{R_O}{(1 + A\beta)}$ (b) $R_{OF} = \frac{R_O}{(1 - A\beta)}$
    (c) $R_{OF} = R_O(1 + A\beta)$ (d) none of the above

31. The phase difference between input and output signals of an op-amp buffer is
(a) Zero (b) 120° (c) 270° (d) 180°
32. The gain of an op-amp of buffer is
(a) zero (b) 1 (c) 2 (d) infinity
33. The circuit of an op-amp non-inverter can be converted in to a buffer by
(a) making R_F Zero (b) making R_1 infinity (c) both (a) and (b) (d) neither (a) nor (b)
34. An op-amp voltage follower is generally used for
(a) impedance matching (b) increasing the driving
(c) both (a) and (b) (d) neither (a) nor (b)
35. An op-amp comparator produces an output that is proportional to
(a) zero (b) sum of the two inputs
(c) difference of the two inputs (d) infinity
36. An op-amp comparator produces a non-zero output, if the two input signals are
(a) different (b) same (c) zero (d) infinity
37. An op-amp Schmitt trigger produces a rectangular output, if the input signal is
(a) a sine wave (b) a triangular wave
(c) both (a) and (b) (d) neither (a) nor (b)
38. The UTP for an op-amp Schmitt trigger is given by
(a) $\text{UTP} = V_o\beta \pm V_{ref}(1-\beta)$ (b) $\text{UTP} = -V_o\beta \pm V_{ref}(1-\beta)$
(c) $\text{UTP} = V_o(1-\beta) \pm V_{ref}(1-\beta)$ (d) $\text{UTP} = -V_o(1-\beta) \pm V_{ref}(1-\beta)$
39. The LTP for an op-amp Schmitt trigger is given by
(a) $\text{UTP} = V_o\beta \pm V_{ref}(1-\beta)$ (b) $\text{UTP} = -V_o\beta \pm V_{ref}(1-\beta)$
(c) $\text{UTP} = V_o(1-\beta) \pm V_{ref}(1-\beta)$ (d) $\text{UTP} = -V_o(1-\beta) \pm V_{ref}(1-\beta)$
40. The hysteresis V_H for an op-amp Schmitt trigger is given by
(a) $V_H = \text{UTP} \times \text{LTP}$ (b) $V_H = \text{UTP} / \text{LTP}$
(c) $V_H = \text{UTP} - \text{LTP}$ (d) $V_H = \text{UTP} + \text{LTP}$
41. The magnitude of LTP and UTP for an op-amp Schmitt trigger with hysteresis $V_H = 0$ are
(a) both Zero (b) both equal
(c) both positive (d) both negative
42. An active filter using op-amp as compared to a passive filter offers good
(a) gain (b) input impedance
(c) frequency response (d) all the above
43. As the order of the active filter increases, the separation between pass and stop band
(a) becomes zero (b) steepens (c) not affected (d) none of the above
44. The selectivity of an active filter using op-amp depends on the
(a) upper cut-off frequency (b) lower cut-off frequency
(c) quality factor (d) all the above
45. The supply voltage for the IC-555 timer varies from
(a) 0 to 10 V (b) 3 to 5 V (c) 3 to 9 V (d) 3 to 18 V
46. The reference signals for the comparators in a IC-555 timer are obtained from
(a) separate sources (b) a 3*R* network
(c) both (a) and (b) (d) neither (a) nor (b)

47. An astable multivibrator using IC-555 is a square wave generator since it uses
    (a) no input to generate a square wave
    (b) square-wave input to generate a square wave
    (c) sine-wave input to generate a square wave
    (d) none of the above
48. A monostable multivibrator using IC-555 produces a pulse whose period is
    (a) $T_P = 0.693RC$ (b) $T_P = 1.099RC$
    (c) both (a) and (b) (d) neither (a) nor (b)
49. The basic building block/s of a PLL is/are
    (a) a phase comparator (b) an active LPF
    (c) a VCO (d) all the above
50. The VCO in a PLL is driven by the
    (a) the error signal generated by Phase comparator
    (b) input signal
    (c) the error signal generated by LPF
    (d) none of the above

Digital Electronics

7

Goals and Objectives

Upon completion of this chapter, the reader is expected to

- Understand the differences between analog and digital signals
- Understand the differences between positive and negative logic
- Understand the basics of different number systems and their inter-conversions
- Understand the basics of Boolean algebra and Boolean postulates
- Become familiar with De Morgan's theorems and their use
- Become familiar with the basic gates, their function tables and symbols
- Become familiar with the universal gates, their function table and symbols
- Understand the realisation of basic gates using universal gates
- Understand the need for simplification of switching functions before realisation
- Understand the process of simplification of switching functions using Boolean theorems
- Understand the basics of Karnaugh-map simplification of switching functions
- Realise some of the basic arithmetic circuits like half adders, full adders, etc.
- Understand the basic concepts of latches, flip-flops and their applications
- Understand the basic concepts of counters and their uses in system design
- Understand the basic concepts of shift registers and their uses in system design
- Feel confident of taking up the next courses in digital system design

7.1 INTRODUCTION

Digital computers are widely used for various control and process applications in industry. Many scientific applications such as space research, where satellite launching and monitoring is to be done, and industrial applications such as automobile electronic automation are achieved using digital computers. These digital computers accept strings of 1s and 0s as data and control inputs, process these strings and again produce strings of 1s and 0s as outputs. These data streams are obtained by converting continuous analog signals into a finite number of discrete states using a process called **digitisation** or **quantisation**. The conversion of an analog signal to digital form can be done using circuits such as an Analog-to-Digital Convertor (ADC). This information is digital in nature, so it is natural to process and manipulate it using purely digital techniques. The drawback of digitisation is that a single analog signal needs many discrete states or *bits*, in order to give a satisfactory reproduction. For example, it requires a minimum of 10 bits to determine a voltage at any given time to an accuracy of close to 0.1% and for transmission of this signal, we require 10 separate lines instead of the one original analog line. The explosion in digital techniques and technology has been made possible by the incredible increase in the density of digital circuitry, its robust performance, its relatively low cost and its speed. The basic circuitry used is a transistor switch, which can be operated with two states and hence, the digital information is intrinsically **binary**. Finally, the external world needs an analog signal and hence, the processed digital information needs a re-conversion back to analog form. This is done by using a circuit called a Digital-to-Analog Convertor (DAC).

1. Positive Logic

In this case, logical 'TRUE' refers to logical 'HIGH' and represents + 5 V; logical 'FALSE' refers to logical 'LOW' and represents 0 V. Positive logic is hence also called a **positive true logic** or **high true logic**.

FALSE or Logic-0 = LOW = 0 V
TRUE or Logic-1 = HIGH = 5 V

2. Negative Logic

In this case, logical 'TRUE' refers to logical 'LOW' and represents + 5 V; logical 'FALSE' refers to logical 'HI*G*H' and represents 0 V. Negative logic is hence also called a **negative true logic** or **low true logic**.

FALSE or Logic-0 = HIGH = 0 V
TRUE or Logic-1 = LOW = 5 V

Table 7.1 shown below indicates conventions for defining binary logic states: the low-voltage state (L) is generally 0 to 0.8 volts and the high-voltage state (H) is roughly 2.5 to 5 volts.

Table 7.1 Logic levels

Digital Logic	Boolean Algebra	Voltage State		Voltage levels in both Logics
		Positive logic	Negative logic	
TRUE(T)	1	High (H)	Low (L)	5 V
FALSE(F)	0	Low (L)	High (H)	0 V

The convention for naming these states is illustrated in Fig. 7.1 and the 'positive logic' case is illustrated. In the figure, when the switch is open, the stated function is True (T) and this corresponds to a high voltage (+ 5 V) at the labeled output point. Similarly, when the switch is closed, the stated function is False (F) and this corresponds to a low voltage (0 V) at the labeled output point.

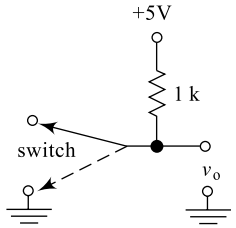


Fig. 7.1 Logic levels

With a closed switch, the labeled point is connected to ground, with a 5-volt drop across the resistor and a current of $I = V/R = 5$ mA through it.

There are basically two ways of representing the numerical value of quantities: **analog representation** and **digital representation**.

7.1.1 Analog Representation

In analog representation, a voltage or a current is represented as a continuous function of time, i.e. variation in amplitude over a continuous range of time values. At different time intervals, instantaneous amplitude of the signal is represented as a function of time. Figure 7.2(a) indicates variation of an *analog voltage vs time*.

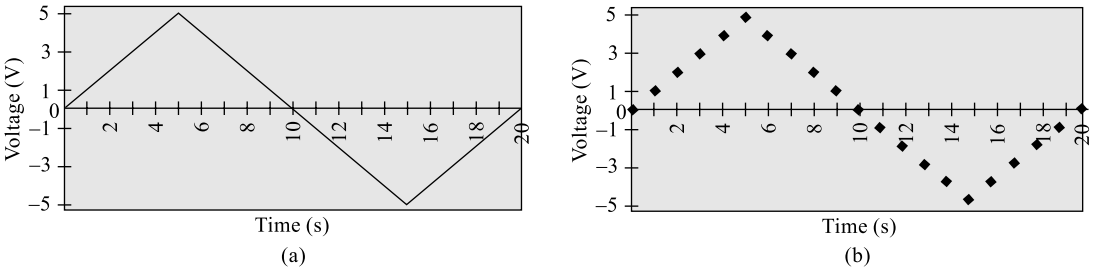


Fig. 7.2 (a) Analog signal (b) Digital signal

7.1.2 Digital Representation

In digital representation, a voltage or a current is represented as a discrete (noncontinuous) function of time. In digital representation, the signal quantities are represented by symbols called **digits**. As an example, consider the digital watch, which provides the time of day in the form of decimal digits which represent hours, minutes and seconds. At different time intervals, the digital representation of the time of day changes in discrete steps. Figure 7.2(b) indicates variation of an *analog voltage vs time*.

7.1.3 Analog Representation Vs Digital Representation

Data processing and control in the present scenario is almost digital and digital computers are, therefore, used everywhere. These digital processors require the input data to be in digital form and produce digital data output. The performance of any digital system in comparison with an analog system can therefore be understood by making a study of advantages and disadvantages of a digital representation.

Advantages of Digital Representation over Analog Representation

1. Exact digital values of voltage or current are not important, but only the range (HIGH or LOW) in which they fall is important.
2. Information processing and storage is very easy.

3. Higher accuracy and precision can be achieved in digital systems.
4. Effect of noise on digital circuits is less as long as the noise is not large enough to prevent us from distinguishing a HIGH from a LOW.
5. More digital circuitry can be fabricated on a unit area of silicon IC chips.

Disadvantages of Digital Representation

1. Analog systems are more reliable than digital systems.
2. The real world is mainly analog in nature. Most physical quantities are analog in nature and it is these quantities that are often the inputs and outputs that are being monitored, operated on and controlled by a system.

To take advantage of digital techniques when dealing with analog inputs and outputs, the following three steps are followed:

1. Convert the real-world analog inputs to digital form using an analog-to-digital converter.
2. Process (operate on) the digital information.
3. Convert the digital outputs back to analog form using a digital-to-analog converter.

7.2 NUMBER SYSTEMS

Digital computers are now part and parcel of everyday life; here, we find a computer embedded into every application we use. These computers use digital numbers for all their process-and-control operations. In everyday life, we use the decimal number system which is very convenient; however, there are different number systems available in addition to the decimal number system, such as binary number system, octal number system, hexadecimal number system, etc. In this section, we will understand the basics of all these number systems and conversion from one number system to another.

7.2.1 Decimal Number System

The most commonly used number system worldwide is the decimal number system. The decimal number system, also called the **base-10** system, has the base or radix of 10 and the system is composed of 10 numerals or symbols or digits used for representation: they are 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9. Using these symbols any number can be easily represented, for example, we can represent 'nine thousand eight hundred and seventy-six' as 9876 as in Eq. (7.1). This is basically a shorthand notation for 'nine thousands plus eight hundreds plus seven tens plus six',

i.e. $$9876 = 9 \times 10^3 + 8 \times 10^2 + 7 \times 10^1 + 6 \times 10^0 \quad (7.1)$$

All of us are completely familiar with the decimal number system and decimal arithmetic such as decimal addition, decimal subtraction, etc. Therefore, it is not necessary to consider decimal arithmetic once again. However, representation of decimal numbers is depicted in Table 7.2. Here representation of both integer and fractional numbers is given.

Table 7.2 Decimal number system

10^4	10^3	10^2	10^1	10^0		10^{-1}	10^{-2}	10^{-3}	10^{-4}
= 10000	= 1000	= 100	= 10	= 1	.	= 0.1	= 0.01	= 0.001	= 0.0001
Most significant digit					Decimal point				Least significant digit

7.2.2 Binary Number System

All digital systems make use of the binary number system extensively. The binary number system, also called the **base-2** system, has the base or radix of 2 and the system is composed of only 2 numerals or symbols or digits used for representation: they are 0 and 1. Each digit in binary is a '0' or a '1' and is called a **bit**, which is an abbreviation of **binary digit**. This base-2 system can be used to represent any quantity that can be represented in decimal or any other number system. Using these symbols, any number can be easily represented; for example, we can represent the decimal 'two hundred and fifty-five' in binary as indicated in Eq. (7.2) in Example 7.1. This is basically a shorthand notation for 'two hundreds plus five tens plus five.' It is based on the representation available in Table 7.3 and is clearly depicted in Example 7.1. However, the complete conversion procedure required is provided in Section 7.3.2.

Example 7.1

Represent 11111111_2 in its equivalent decimal form.

Solution

$$\begin{aligned} 11111111_2 &= 1\times 2^7 + 1\times 2^6 + 1\times 2^5 + 1\times 2^4 + 1\times 2^3 + 1\times 2^2 + 1\times 2^1 + 1\times 2^0 \\ &= 1\times 128 + 1\times 64 + 1\times 32 + 1\times 16 + 1\times 8 + 1\times 4 + 1\times 2 + 1\times 1 \\ &= 128 + 64 + 32 + 16 + 8 + 4 + 2 + 1 = 255_{10} \end{aligned} \tag{7.2}$$

$$\therefore \quad 255_{10} = 11111111_2$$

The subscripts used in the above representation indicate the **radix** of the number system. Representation of binary numbers is depicted in Table 7.3; here representation of both integer and fractional numbers is given.

Table 7.3 Binary number system

2^4	2^3	2^2	2^1	2^0		2^{-1}	2^{-2}	2^{-3}	2^{-4}
= 16	= 8	= 4	= 2	= 1	.	= 0.5	= 0.25	= 0.125	= 0.0625
Most Significant Bit (MSB)					Binary point				Least Significant Bit (LSB)

Example 7.2

Represent $\mathbf{101101_2}$ in its equivalent decimal form.

Solution

$$\begin{aligned} \mathbf{101101_2} &= 1\times 2^5 + 0\times 2^4 + 1\times 2^3 + 1\times 2^2 + 0\times 2^1 + 1\times 2^0 \\ &= 1\times 32 + 0\times 16 + 1\times 8 + 1\times 4 + 0\times 2 + 1\times 1 \\ &= 32 + 8 + 4 + 1 = \mathbf{45_{10}} \end{aligned}$$

$$\therefore \quad \mathbf{45_{10} = 101101_2}$$

The binary counting sequence is shown in Table 7.4 where the representation can be further extended by adding additional columns.

Table 7.4 Binary counting table

Binary Weights				Decimal Equivalents	Remarks
2^3	2^2	2^1	2^0		
—	—	—	0	0	—
—	—	—	1	1	First column is completed
—	—	1	0	2	Reset first column and add 1 to second column
—	—	1	1	3	First two columns are completed
—	1	0	0	4	Reset first two columns and add 1 to third column
—	1	0	1	5	—
—	1	1	0	6	—
—	1	1	1	7	First three columns are completed
1	0	0	0	8	Reset first three columns and add 1 to fourth column
1	0	0	1	9	—
1	0	1	0	10	—
1	0	1	1	11	—
1	1	0	0	12	—
1	1	0	1	13	—
1	1	1	0	14	—
1	1	1	1	15	—

There are several common conventions for representation of numbers in binary: the most familiar is **unsigned binary**. Another example of an 8-bit number in this case is

$$01001111_2 = 0 \times 2^7 + 1 \times 2^6 + \cdots + 1 \times 2^0 = 0 + 64 + 0 + 0 + 8 + 4 + 2 + 1 = 79_{10} \quad (7.3)$$

The subscripts are used to indicate the radix of the system and will not be considered while finding the equivalent values.

7.2.3 Representation of Signed Numbers

To represent signed numbers, there are three commonly used forms are indicated below. Representation of positive numbers is same in all the three cases, but representation of negative numbers is different in all the three cases. When a positive number is to be represented, the sign is represented by a 0 and the magnitude is represented by a positive binary number. When a negative number is to be represented, the sign is represented by a 1 and the magnitude part is represented by any of the following forms.

(i) Sign magnitude representation
(ii) One's complement representation
(iii) Two's complement representation

Sign Magnitude Representation

In **sign magnitude** representation, the sign of the number is represented by the MSB and the magnitude is represented by a positive binary number. For example, the number 12_{10} can be represented as an 8-bit number in sign magnitude form as shown in Eq. (7.4) below:

$$\mathbf{+ 12_{10} = 0\ 000\ 1100 \text{ and } - 12_{10} = 1\ 000\ 1100} \quad (7.4)$$

It can be observed that only the sign bit changes and the magnitude bits are same in both the cases.

Sign 1's Complement Representation

In **sign 1's complement** representation, the sign of the number is represented by the MSB and the magnitude is represented by 1's complement of the binary number. For example, the same number 12_{10} can be represented as an 8-bit number in sign 1's complement form as shown in Eq. (7.5) below:

$$\mathbf{+ 12_{10} = 0\ 000\ 1100 \text{ and } -12_{10} = 1\ 111\ 0011} \tag{7.5}$$

It can be observed that both the sign bit and the magnitude bits are changing here. The magnitude bits are in 1's complement form.

Sign 2's Complement Representation

In **sign 2's complement** representation, the sign of the number is represented by the MSB and the magnitude is represented by 2's complement of the binary number. For example, the same number 12_{10} can be represented as an 8-bit number in sign 1's complement form as shown in Eq. (7.6) below:

$$\mathbf{+ 12_{10} = 0\ 000\ 1100 \text{ and } - 12_{10} = 1\ 111\ 0100} \tag{7.6}$$

It can be observed that both the sign bit and the magnitude bits are changing here. The magnitude bits are in 2's complement form.

Example 7.3

Represent $\mathbf{+0_{10}}$ and $\mathbf{-0_{10}}$ in 8-bit sign-magnitude, sign 1's complement and sign 2's complement forms.

Solution The three representations for a positive and negative representation are shown in Table 7.5. It can be observed here that the first two types have two different representations, while the 2's complement form has a single representation for both the zeros.

Of the three representations, sign 2's complement form has the advantage of one extra representation: because in the first two cases, we have a separate representation for positive and negative zeros. In 2's complement form, both zeros have only one representation and hence, this representation is preferred in most computers.

Table 7.6 presents the representation of both positive and negative numbers using sign magnitude, sign 1's complement and sign 2's complement forms. It can be observed here that a positive number has same representation in all three types as indicated in the last three rows. A negative number has sign bit '1' and different magnitude part in all three forms; this is indicated in the table.

Table 7.5 Positive and negative zero representations

	Sign Magnitude	Sign 1's Complement	Sign 2's Complement
+ 0	0 000 0000	0 000 0000	0 000 0000
– 0	1 000 0000	1 111 1111	0 000 0000

Table 7.6 Positive and negative number representation

	Sign Magnitude	Sign 1's Complement	Sign 2's Complement
–12	1 000 1100	1 111 0011	1 111 0100
–9	1 000 1001	1 111 0110	1 111 0111
–1	1 000 0001	1 111 1110	1 111 1111
+0	0 000 0000	0 000 0000	0 000 0000
–0	1 000 0000	1 111 1111	0 000 0000
+1	0 000 0001	0 000 0001	0 000 0001
+9	0 000 1001	0 000 1001	0 000 1001
+12	0 000 1100	0 000 1100	0 000 1100

7.2.4 Octal Number System

Some digital systems make use of another important number system known as the octal number system. The octal number system, also called the **base-8** system, has the base or radix of 8 and the system is composed of 8 numerals or symbols or digits used for representation: they are 0, 1, 2, 3, 4, 5, 6 and 7. This base-8 system can be used to represent any quantity that can be represented in decimal or any other number system. Using these symbols, any number can be easily represented; for example, we can represent the decimal 'three hundred and seventeen' as 475 in octal. This is basically a shorthand notation for 'three hundreds plus one ten plus seven', it is based on the representation available in Table 7.5 and is clearly depicted in Eq. (7.7) in Example 7.4.

Example 7.4

Represent $\mathbf{475_8}$ in its equivalent decimal form.

Solution

$$475_8 = 4 \times 8^2 + 7 \times 8^1 + 5 \times 8^0 \tag{7.7}$$
$$= 4 \times 64 + 7 \times 8 + 5 \times 1 = 256 + 56 + 5 = 317_{10}$$
$$\therefore \quad 475_8 = 317_{10}$$

Representation of octal numbers is depicted in Table 7.7. Here, representation of both integer and fractional numbers is given.

Table 7.7 Octal number system

8^4	8^3	8^2	8^1	8^0		8^{-1}	8^{-2}	8^{-3}	8^{-4}
= 4096	= 512	= 64	= 8	= 1	.	= 0.125	= 0.0625	= 0.00778	= 0.00097
Most significant digit					Octal point				Least significant digit

The octal counting sequence is shown in Table 7.8 where the representation can be further extended by adding additional columns.

Table 7.8 Octal number counting sequence

Octal Weights				Decimal Equivalents	Remarks
8^3	8^2	8^1	8^0		
—	—	—	0	0	—
—	—	—	1	1	—
—	—	—	2	2	—
—	—	—	3	3	—
—	—	—	4	4	—
—	—	—	5	5	—
—	—	—	6	6	—
—	—	—	7	7	First column is completed
—	—	1	0	8	Reset first column and add 1 to second column
—	—	1	1	9	—
—	—	1	2	10	—
—	—	1	3	11	—
—	—	1	4	12	—
—	—	1	5	13	—
—	—	1	6	14	—
—	—	1	7	15	First column is completed
—	—	2	0	16	Reset first column and add 1 to second column

7.2.5 Hexadecimal Number System

Most digital systems make use of another very important number system known as the hexadecimal number system. The hexadecimal number system, also called the base-16 system, has the base or radix of 16 and the system is composed of 16 numerals or symbols or digits used for representation: they are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 and *A, B*, *C*, *D*, *E* and *F*. This base-16 system can be used to represent any quantity that can be represented in decimal or any other number system. Using these symbols, any number can be easily represented; for example, we can represent decimal 'forty-three thousand, nine hundred and eighty-one' as *ABCD* in hexadecimal. This is basically a shorthand notation for 'forty-three thousands plus nine hundreds plus eight ten plus one.' It is based on the representation available in Table 7.7 and is clearly depicted in Eq. (7.8) in Example 7.5.

Example 7.5

Represent $\boldsymbol{ABCD_{16}}$ in its equivalent decimal form.

Solution

$$\begin{aligned} \boldsymbol{ABCD_{16}} &= A \times 16^3 + B \times 16^2 + C \times 16^1 + D \times 16^0 \\ &= 10 \times 4096 + 11 \times 256 + 12 \times 16 + 13 \times 1 \\ &= 40960 + 2816 + 192 + 13 = 43981_{10} \end{aligned} \tag{7.8}$$

Table 7.9 Hexadecimal number system

16^4	16^3	16^2	16^1	16^0		16^{-1}	16^{-2}	16^{-3}	16^{-4}
= 65536	= 4096	= 256	= 16	= 1	.	= 0.0625	= 0.003906	= 0.000244	= 0.0000153
Most significant digit					Hexa-decimal point				Least significant digit

Representation of hexadecimal numbers is depicted in Table 7.9. Here, representation of both integer and fractional numbers is given.

The hexadecimal counting sequence is shown in Table 7.10 where the representation can be further extended by adding additional columns.

Table 7.10 Hexadecimal number counting sequence

Hexadecimal Weights				Decimal Equivalents	Remarks
16^3	16^2	16^1	16^0		
—	—	—	0	0	—
—	—	—	1	1	—
—	—	—	2	2	—
—	—	—	3	3	—
—	—	—	4	4	—
—	—	—	5	5	—
—	—	—	6	6	—
—	—	—	7	7	—
—	—	—	8	8	—
—	—	—	9	9	—
—	—	—	A	10	—
—	—	—	B	11	—
—	—	—	C	12	—
—	—	—	D	13	—
—	—	—	E	14	—
—	—	—	F	15	First column is completed
—	—	1	0	16	Reset first column and add 1 to second column
—	—	1	1	17	—

7.3 NUMBER BASE CONVERSIONS

On a number of occasions, conversion from one number system to another number system becomes essential; this allows the use of different number systems. Generally, digital computers use binary or hexadecimal number systems and other number systems if used need a conversion. The following sections

illustrate the conversion from one number system to another number system and the examples used help the reader in understanding these conversions further.

7.3.1 Binary-to-Decimal Conversion

The given binary number can be converted to its equivalent decimal number by multiplying each bit in the given number by its positional weight as given in Table 7.3 and adding all these values or products. To convert from base-2, that is binary, to base-10, that is decimal, one can make use of Table 7.3. Example 7.6 clearly depicts the conversion procedure:

Example 7.6

Convert $\mathbf{101101_2}$ to its equivalent decimal number.

Solution

$$\begin{aligned}\mathbf{101101_2} &= 1\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0\\ &= 1\times32 + 0\times16 + 1\times8 + 1\times4 + 0\times2 + 1\times1\\ &= 32 + 8 + 4 + 1 = \mathbf{45_{10}}\end{aligned}$$

$$\therefore \quad \mathbf{101101_2 = 45_{10}}$$

Example 7.7

Convert $\mathbf{11111111_2}$ to its equivalent decimal number.

Solution

$$\begin{aligned}\mathbf{11111111_2} &= 1\times2^7 + 1\times2^6 + 1\times2^5 + 1\times2^4 + 1\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0\\ &= 1\times128 + 1\times64 + 1\times32 + 1\times16 + 1\times8 + 1\times4 + 1\times2 + 1\times1\\ &= 128 + 64 + 32 + 16 + 8 + 4 + 2 + 1 = \mathbf{255_{10}}\end{aligned}$$

$$\therefore \quad \mathbf{11111111_2 = 255_{10}}$$

Fractions Conversion

In order to convert a binary fraction into its equivalent decimal number, each bit in the fractional part is multiplied by its positional weight after the decimal point as given in Table 7.3 and adding all these values or products. This is illustrated in Eqs. (7.9) and (7.10) in Example 7.8

Example 7.8

Convert $\mathbf{110101.1011_2}$ to its equivalent decimal number.

Solution *Integer Part:*

$$\begin{aligned}\mathbf{110101_2} &= 1\times2^5 + 1\times2^4 + 0\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0 \qquad (7.9)\\ &= 1\times32 + 1\times16 + 0\times8 + 1\times4 + 0\times2 + 1\times1\\ &= 32 + 16 + 4 + 1 = \mathbf{53_{10}}\end{aligned}$$

Fractional Part:

$$\begin{aligned}\mathbf{0.1011_2} &= 1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} + 1\times2^{-4} \qquad (7.10)\\ &= 1\times1/2 + 0\times¼ + 1\times1/8 + 1\times1/16\\ &= 1\times0.5 + 0\times0.25 + 1\times0.125 + 1\times0.0625\\ &= 0.5 + 0.125 + 0.0625 = \mathbf{0.6875_{10}}\end{aligned}$$

$$\therefore \quad \mathbf{110101.1011_2 = 53.6875_{10}}$$

7.3.2 Decimal-to-Binary Conversions

The given decimal number, i.e. integer part, is repeatedly divided by two, which is the base of the binary number system until the remainder becomes less than the radix of the binary number system, i.e. either a 0 or a 1. Then, these remainders are arranged from bottom to top to get the binary equivalent of the decimal integer. This is clearly illustrated in Example 7.9.

Example 7.9

Convert $\mathbf{255_{10}}$ to its equivalent binary number.

Solution

$$
\begin{array}{rl}
2 \mid 255 & \\
2 \mid 127 & \rightarrow 1 \\
2 \mid 63 & \rightarrow 1 \\
2 \mid 31 & \rightarrow 1 \\
2 \mid 15 & \rightarrow 1 \\
2 \mid 7 & \rightarrow 1 \\
2 \mid 3 & \rightarrow 1 \\
1 & \rightarrow 1
\end{array}
\qquad \therefore \quad \mathbf{255_{10} = 11111111_2}
$$

Fraction Conversion

In order to convert a fractional part in the decimal system into its binary equivalent, the fractional part is repeatedly multiplied by 2 until the fraction becomes zero or until the desired number of places after the binary point is reached. The integer bits are then arranged from top to bottom to get the equivalent fractional binary equivalent.

Example 7.10

Convert $\mathbf{255.65_{10}}$ to its equivalent binary number.

Solution

$$
\begin{array}{rl}
2 \mid 255 & \\
2 \mid 127 & \rightarrow 1 \\
2 \mid 63 & \rightarrow 1 \\
2 \mid 31 & \rightarrow 1 \\
2 \mid 15 & \rightarrow 1 \\
2 \mid 7 & \rightarrow 1 \\
2 \mid 3 & \rightarrow 1 \\
1 & \rightarrow 1
\end{array}
\qquad 255_{10} = 11111111_2
$$

$$
\begin{array}{rl}
0.65 \times 2 & \\
1.30 \times 2 & \rightarrow 1 \\
0.60 \times 2 & \rightarrow 0 \\
1.20 \times 2 & \rightarrow 1 \\
0.40 \times 2 & \rightarrow 1
\end{array}
\qquad 0.65_{10} = 1011_2
$$

$\therefore$ $\mathbf{255.65_{10} = 11111111\ .1011_2}$

7.3.3 Binary-to-Octal Conversion

The given binary number can be converted to its equivalent octal number by using the following procedure:

1. Group the binary digits into groups of three bits each, starting from the binary point to the left for the integer part and to the right for the fractional part. Preceding zeros may be appended for the integer part and following zeros may be appended for the fractional part to complete the group.
2. Multiply each bit in the given group by its positional weight as given in Table 7.3 and add all these values or products to get the octal digits.
3. Retain the binary point in the same position as the octal point; the resulting number is the equivalent octal number.

Example 7.11 Clearly depicts the conversion procedure for a binary number into its equivalent octal number.

Example 7.11

Convert $\mathbf{1011010_2}$ to its equivalent octal number.

Solution *Step 1:* Group binary digits into groups of 3 bits from the right.

i.e. **1** **011** **010** = **001** **011** **010**

Append zeros to complete the group.

Step 2: Now using Table 7.3, find the decimal equivalent of each group.

$0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 1$ $\quad 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 3$ $\quad 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 2$

$= \mathbf{132_8}$

$\therefore \quad \mathbf{1011010_2 = 132_8}$

Example 7.12

Convert $\mathbf{10110101.0111011_2}$ to its equivalent octal number.

Solution: *Step 1:* Group binary digits into groups of 3 bits from the right.

i.e. **010** **110** **101** . **011** **101** **100**

Append zeros to complete the group.

Step 2: Now using Table 7.3, find decimal equivalent of each group.

$0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 2$ $\quad 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 6$ $\quad 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 5$

$0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 3$ $\quad 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 5$ $\quad 1 \times 2^2 + 0 \times 2^1 + 0 \times 2^0 = 4$

$\therefore \quad \mathbf{10110101_2 = 265.354_8}$

7.3.4 Octal-to-Binary Conversion

The given octal number can be converted to its equivalent binary number by using the following procedure:

1. Map the individual octal digits into groups of three binary bits, each starting from the octal point to the left for the integer part and to the right for the fractional part.
2. Retain the octal point in the same position as the binary point; the resulting number is the equivalent binary number.

Example 7.13 clearly depicts the conversion procedure for an octal number into its equivalent binary number.

Example 7.13

Convert $\mathbf{132_8}$ to its equivalent binary number.

Solution Map the individual octal digits into 3-bit binary numbers,

i.e. $\boxed{1}\ \boxed{3}\ \boxed{2}$ (each ↓)

$= \mathbf{001}\ \ \mathbf{011}\ \ \mathbf{010}$

$\therefore \quad \mathbf{132_8 = 1011010_2}$

Example 7.14

Convert 265.354_8 to its equivalent binary number.

Solution Map the individual octal digits into 3-bit binary numbers from the octal point,

i.e. $\boxed{2}\ \boxed{6}\ \boxed{5\ \cdot}\ \boxed{3}\ \boxed{5}\ \boxed{4}$ (each ↓)

$= 010\ \ 110\ \ 101\ \cdot\ \ 011\ \ 101\ \ 100$

$\therefore \quad 265.354_8 = 010110101.011101100_2$

7.3.5 Binary-to-Hexadecimal Conversion

The given binary number can be converted to its equivalent hexadecimal number by using following procedure:

1. Group the binary digits into groups of four bits each, starting from the binary point to the left for the integer part and to the right for the fractional part. Preceding zeros may be appended for the integer part and following zeros may be appended for the fractional part to complete the group.
2. Multiply each bit in the given group by its positional weight as given in Table 7.3 and add all these values or products to get the hexadecimal digits.
3. Retain the binary point in the same position as the hexadecimal point; the resulting number is the equivalent hexadecimal number.

Example 7.15 clearly depicts the conversion procedure for a binary number into its equivalent hexadecimal number.

Example 7.15

Convert $\mathbf{1011010_2}$ to its equivalent hexadecimal number.

Solution *Step 1:* Group binary digits into groups of 4 bits from the right,

i.e. $\boxed{\mathbf{101}}\ \boxed{\mathbf{1010}} = \boxed{\mathbf{0101}}\ \boxed{\mathbf{1010}}$

Append zeros to complete the group.

Step 2: Now using Table 7.3, find the decimal equivalent of each group.

$0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$ $\qquad$ $1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$

$= 5_{10} = 5_{16}$ $\qquad$ $= 10_{10} = A_{16}$

$= \mathbf{132_8}$

$\therefore \quad \mathbf{1011010_2 = 5A_{16}}$

Example 7.16

Convert $\mathbf{10110101.0111011_2}$ to its equivalent hexadecimal number.

Solution *Step* 1: Group binary digits into groups of 4 bits from the binary point,

i.e. $\boxed{\mathbf{1011}}\ \boxed{\mathbf{0101}} \cdot \boxed{\mathbf{0111}}\ \boxed{\mathbf{0110}}$

Append zeros to complete the group.

Step 2: Now using Table 7.3, find the decimal equivalent of each group and using Table 7.5, obtain its hexadecimal equivalent.

$1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$ $\qquad$ $0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$

$= 11_{10} = B_{16}$ $\qquad$ $= 5_{10} = 5_{16}$

$0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$ $\qquad$ $0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$

$= 7_{10} = 7_{16}$ $\qquad$ $= 6_{10} = 6_{16}$

$\therefore \quad \mathbf{10110101.0111011_2 = \mathit{B}5.76_{16}}$

7.3.6 Hexadecimal-to-Binary Conversion

The given hexadecimal number can be converted to its equivalent binary number by using the following procedure:

1. Map the individual hexadecimal digits into groups of four binary bits, starting from the hexadecimal point to left for the integer part and to the right for the fractional part.
2. Retain the hexadecimal point in the same position as the binary point; the resulting number is the equivalent binary number.

Example 7.17 clearly depicts the conversion procedure for a hexadecimal number into its equivalent binary number.

Example 7.17

Convert $\mathbf{1A2B_{16}}$ to its equivalent binary number.

Solution Map the individual hexadecimal digits into 4-bit binary numbers.

i.e. $\boxed{\mathbf{1}}\ \boxed{\mathbf{A}}\ \boxed{\mathbf{2}}\ \boxed{\mathbf{B}}$

$= \mathbf{0001}\ \ \mathbf{1010}\ \ \mathbf{0010}\ \ \mathbf{1011}$

$\therefore\ \mathbf{1A2B_{16} = 1101000101011_2}$

Example 7.18

Convert $\mathbf{2468.3F5E_{16}}$ to its equivalent binary number.

Solution Map the individual hexadecimal digits into 4-bit binary numbers from the hexadecimal point,

i.e. $\boxed{2}\ \boxed{4}\ \boxed{6}\ \boxed{8}\ .\ \boxed{3}\ \boxed{F}\ \boxed{5}\ \boxed{E}$

$= 0010\ \ 0100\ \ 0110\ \ 1000\ .\ \ 0011\ \ 1111\ \ 0101\ \ 1110$

$\therefore\ 2468.3F5E_{16} = 10010001101000.0011111101011110_2$

7.4 ADDITION AND SUBTRACTION

Just like the decimal number system, even in binary number system, arithmetic operations such as addition, subtraction, etc. can be performed.

1. Binary Addition

Addition of two binary numbers is carried out in a very similar manner to any other number system such as a decimal number system. Consider addition of the two decimal numbers shown in Example 7.19; here, the two decimal numbers are represented in binary form and then added. Any carry generated is carried over to the next column.

Example 7.19

Perform the addition of 1011_2 and 1110_2.

Solution The basic binary addition can be depicted as in Table 7.11.

Table 7.11 Single-bit binary addition

A + *B*	*S* (Sum)	*C* (Carry)
0 + 0	0	0
0 + 1	1	0
1 + 0	1	0
1 + 1	0	1

$$\begin{array}{rcl} 1011_2 & \rightarrow & 11_{10} \\ 1110_2 & \rightarrow & 14_{10} \\ \hline 11001_2 & \rightarrow & 25_{10} \end{array}$$

Example 7.20

Perform the addition of 101.10_2 and 111.11_2.

Solution

$$\begin{array}{rcl} 101.10_2 & \rightarrow & 5.5_{10} \\ 111.11_2 & \rightarrow & 7.75_{10} \\ \hline 1101.01_2 & \rightarrow & 13.25_{10} \end{array}$$

2. Binary Subtraction

Subtraction of two binary numbers is carried out in a very similar manner to any other number system such as the decimal number system. Consider subtraction of the two decimal numbers shown in Example 7.21; here, the two decimal numbers are represented in binary form and then subtracted. Any borrows is to be taken from the previous column.

Example 7.21

Perform the subtraction of 1011_2 from 1110_2.

Solution The basic binary subtraction can be depicted as in Table 7.12.

Table 7.12 Single-bit binary subtraction

$A - B$	D (difference)	β (Borrow)
0 – 0	0	0
0 – 1	1	1
1 – 0	1	0
1 – 1	0	0

$$\begin{array}{rcl} 1110_2 & \rightarrow & 14_{10} \\ 1011_2 & \rightarrow & 11_{10} \\ \hline 11001_2 & \rightarrow & 03_{10} \end{array}$$

Example 7.22

Perform the following arithmetic using 1's complement method.

(i) $+6$ $+9$

(ii) -6 $+9$

(iii) $+6$ -9

Solution Taking the 1's complement for the negative numbers, we have

(i) $+6$ 0 000 0110
$+9$ 0 000 1001
+ 15 0 000 1111

(ii) -6 1 111 1001
$+9$ 0 000 1001
+ 3 10 000 0010

(iii) $+6$ 0 000 0110
-9 1 111 0110
–3 1111 1100

0 000 0011

Note: Steps to be followed in 1's complement arithmetic:

1. Find the 1's complement of the negative number.
2. Add this 1's complement to the positive number.
3. In subtraction we may have to subtract the following:
   (a) Smaller number form a larger one if there is a carry generated; then add that carry to LSB. The process is called **end-around carry** [Example 7.22(ii)].
   (b) Larger number from a smaller one results in no carry. Again take 1's compliment of result obtained in Step 2 to get the correct answer [Example 7.22(iii)].

Example 7.23

Perform the following arithmetic using 2's complement method:

(i)	(ii)	(iii)
+ 6	– 6	+ 6
+ 9	+ 9	– 9

Solution Taking the 2's complement for the negative numbers, we have

(i)	(ii)	(iii)
+ 6 0 000 0110	– 6 1 111 1010	+ 6 0 000 0110
+ 9 0 000 1001	+ 9 0 000 1001	– 9 1 111 0111
+ 15 0 000 1111	**+ 3 10 000 0011**	**– 3 1 111 1101**

Note: Steps to be followed in 2's complement arithmetic:

1. Find the 2's compliment of the negative number.
2. Add this 2's compliment to the positive number.
3. In subtraction we may have to subtract the following:
   (a) Smaller number form a larger one if there is a carry generated; then discard that carry to get correct answer [Example 7.23(ii)].
   (b) Larger number from a smaller one results in no carry; then take 2's complement of result obtained in Step 2 to get the correct answer [Example 7.23(iii)].

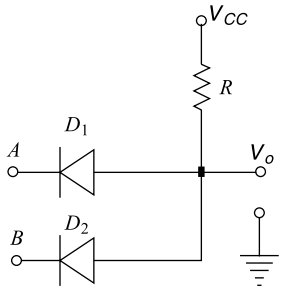
7.5 BASIC LOGIC GATES

The basic logic gates are AND gate, OR gate and NOT gate. The basic circuit, symbol and their corresponding Boolean expressions for these gates are given in this section. The other logic gates that are useful in realising a digital system include NAND gate, NOR gate, EX-OR gate and EX-NOR gate. NAND and NOR gates are termed **universal gates**, since it is possible to realise any logic gate using these gates. Universal gates are presented in Section 7.6. EX-OR and EX-NOR gates are presented in this section itself.

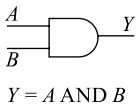
7.5.1 AND Gate

The circuit diagram of AND gate using diodes is shown in Fig. 7.3(a) and the logic symbol is shown in Fig. 7.3(b). The two diodes D_1 and D_2 are the switches for the two inputs A and B. The resistor R is used to limit the circuit current.

Let us assume positive logic and the diodes used are ideal with $\boldsymbol{V_y} = 0$ and $\boldsymbol{R_f} = 0\ \Omega$. The working of this circuit can be understood by considering all the possible input combinations. Let the input level low correspond to a 0 V and the input level high correspond to a +5 V. Note that logic variables A, B and Y can assume voltage values 0 V or 5 V corresponding to logic levels 0 or 1.



(a) AND gate circuit



(b) AND gate symbol

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(c) AND gate function table

Fig. 7.3 AND logic gate

Case 1

When input variables $A = 0$ and $B = 0$, both diodes D_1 and D_2 are forward biased resulting in a short circuit across output and hence, $Y = 0$. This is depicted in the first row of the function table (truth table) shown in Fig. 7.3 (c).

Case 2

When input variables $A = 0$ and $B = 1$, the diode D_1 is forward biased and D_2 is reverse biased resulting in a short circuit across output and hence, $Y = 0$. This is depicted in the second row of the function table.

Case 3

When input variables $A = 1$ and $B = 0$, the diode D_1 is reverse biased and D_2 is forward biased resulting in a short circuit across output and hence, $Y = 0$. This is depicted in the third row of the function table.

Case 4

When input variables $A = 1$ and $B = 1$, both diodes D_1 and D_2 are reverse biased resulting in an open circuit across output and hence, $Y = 1$. This is depicted in the fourth row of the function table.

The output function for an AND gate is represented therefore in Eq. (7.11).

$$Y = A \cdot B = AB = A \wedge B = A \cap B \tag{7.11}$$

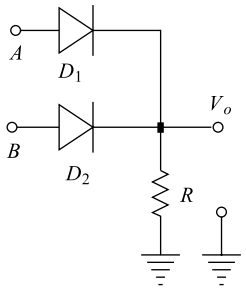
7.5.2 OR Gate

The circuit diagram of an OR gate using diodes is shown in Fig. 7.4 (a) and the logic symbol is shown in Fig. 7.4 (b). The two diodes D_1 and D_2 are the switches for the two inputs A and B. The resistor R is used to limit the circuit current.

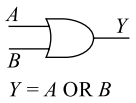
Let us assume positive logic and the diodes used are ideal with $\boldsymbol{V_y} = 0$ and $\boldsymbol{R_f} = 0\ \Omega$. The working of this circuit can be understood by considering all the possible input combinations. Let the input level low correspond to a 0 V and the input level high correspond to a +5 V. Note that logic variables A, B and Y can assume voltage values 0 V or 5 V corresponding to logic levels 0 or 1.

Case 1

When input variables $A = 0$ and $B = 0$, both diodes D_1 and D_2 are reverse biased resulting in no circuit current and no output; hence, $Y = 0$. This is depicted in the first row of the function table (truth table) shown in Fig. 7.4 (c).



(a) OR gate circuit



(a) OR gate symbol

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(a) OR gate truth table

Fig. 7.4 OR logic gate

Case 2

When input variables $A = 0$ and $B = 1$, the diode D_1 is reverse biased and D_2 is forward biased resulting in a circuit current and an output; hence, $Y = 1$. This is depicted in the second row of the function table.

Case 3

When input variables $A = 1$ and $B = 0$, the diode D_1 is forward biased and D_2 is reverse biased resulting in a circuit current and an output; hence, $Y = 1$. This is depicted in the third row of the function table.

Case 4

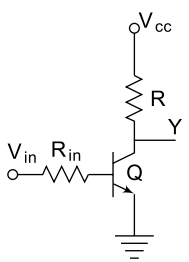
When input variables $A = 1$ and $B = 1$, both diodes D_1 and D_2 are forward biased resulting in a circuit current and an output; hence, $Y = 1$. This is depicted in the fourth row of the function table.

The output function for an OR gate is represented, therefore, as in Eq. (7.12).

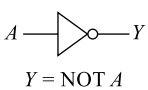
$$\boldsymbol{Y = A + B = A \; V \; B = A \cup B} \tag{7.12}$$

7.5.3 NOT Gate

The circuit diagram of a NOT gate using a transistor is shown in Fig. 7.5. The transistor is biased to work in the cut-off and saturation region. The resistors *R* are used to limit the circuit current. The transistor here works as a switch and offers a complemented output *Y.*



(a) NOT gate circuit



(b) NOT gate symbol

A	Y
0	1
1	0

(c) NOT gate truth table

Fig. 7.5 NOT logic gate

The working of this circuit can be understood by considering the two possible input combinations. Let the input level low correspond to a 0 V and the input level high correspond to a +5 V. Note that logic variables A, B and Y can assume voltage values 0 V or 5 V corresponding to logic levels 0 or 1.

Case 1

When the input variable $A = 1$, it means when V_{in} is at 5 V, the transistor is driven into saturation and the collector-to-emitter voltage $V_0 = V_{CE} = 0$ V, meaning $Y = 0$. This is depicted in the first row of the function table (truth table) shown in Fig. 7.5 (c).

Case 2

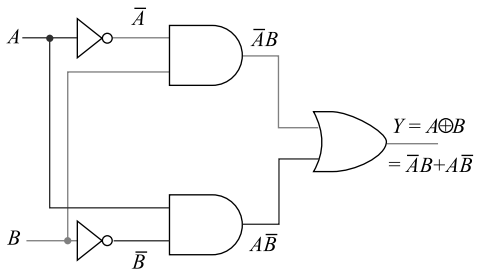
When the input variable $A = 0$, it means when V_{in} is at 0 V, the transistor is driven into cut-off and the collector-to-emitter voltage $V_0 = V_{CE} = V_{CC} = 5$ V, meaning $Y = 1$. This is depicted in the first row of the function table (truth table) shown.

The output function for a NOT gate is represented, therefore, in Eq. (7.13).

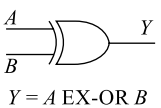
$$\boldsymbol{Y = \text{NOT}\, A = A' = \overline{A}} \tag{7.13}$$

7.5.4 EX-OR Gate

The logic diagram of an EX-OR gate using basic gates, its symbol and the function table are shown in Fig. 7.6. Assuming a positive logic, the working of this logic gate can be understood by considering all the possible input combinations. Let the input level low correspond to a 0 V and the input level high correspond to a +5 V. Note that logic variables A, B and Y can assume voltage values 0 V or 5 V corresponding to logic levels 0 or 1.



(a) EX-OR gate using basic gates



(b) EX-OR gate symbol

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(b) EX-OR gate truth table

Fig. 7.6 EX-OR logic gate

Case 1

When input variables $A = 0$ and $B = 0$, both the NOT gates offer inverted A and B to the AND gates and both the AND gate outputs are zero as indicated; hence, $Y = 0$. This is depicted in the first row of the function table (truth table) shown in Fig. 7.6 (c).

Case 2

When input variables $A = 0$ and $B = 1$, the output of the top AND gate is 1 and that of the bottom AND gate is 0; hence, $Y = 1$. This is depicted in the second row of the function table.

Case 3

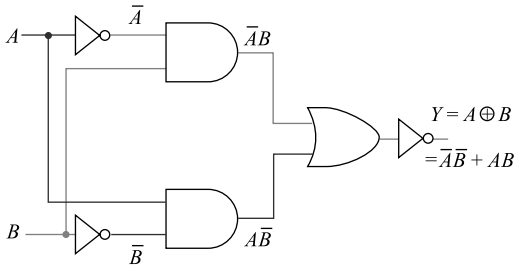
When input variables $A = 1$ and $B = 0$, the output of the top AND gate is 0 and that of the bottom AND gate is 1; hence, $Y = 1$. This is depicted in the third row of the function table.

Case 4

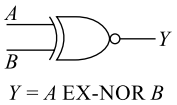
When input variables $A = 1$ and $B = 1$, both the NOT gates offer inverted A and B to the AND gates and both the AND gate outputs are zero as indicated; hence, $Y = 1$. This is depicted in the fourth row of the function table. The output logic function is represented in Fig. 7.6(a).

7.5.5 EX-NOR Gate

The logic diagram of an EX-NOR gate using basic gates, its symbol and the function table are shown in Fig. 7.7. Assuming a positive logic, the working of this logic gate can be understood by considering all the possible input combinations. Let the input level low correspond to a 0 V and the input level high correspond to a +5 V. Note that logic variables A, B and Y can assume voltage values 0 V or 5 V corresponding to logic levels 0 or 1.



(a) EX-NOR gate using basic gates



(a) EX-NOR gate symbol

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(a) EX-NOR gate truth table

Fig. 7.7 EX-NOR logic gate

Case 1

When input variables $A = 0$ and $B = 0$, both the NOT gates offer inverted A and B to the AND gates and both the AND gate outputs are zero as indicated; hence output of the OR gate is 0, however final output $Y = 1$. This is depicted in the first row of the function table (truth table) shown in Fig. 7.7(c).

Case 2

When input variables $A = 0$ and $B = 1$, the output of the top AND gate is 1 and that of the bottom AND gate is 0; hence output of the OR gate is 1. However, final output $Y = 0$. This is depicted in the second row of the function table.

Case 3

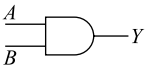
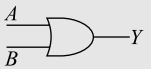
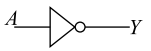
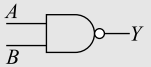
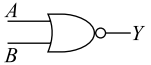
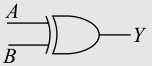
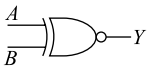
When input variables $A = 1$ and $B = 0$, the output of the top AND gate is 0 and that of the bottom AND gate is 1; hence output of the OR gate is 1. However, final output $Y = 0$. This is depicted in the third row of the function table.

Case 4

When input variables $A = 1$ and $B = 1$, both the NO*T* gates offer inverted A and B to the AND gates and both the AND gate outputs are zero as indicated; hence output of the OR gate is 0. However, final output $Y = 1$. This is depicted in the fourth row of the function table. The output logic function is represented in Fig. 7.7(a).

Table 7.13 contains all the logic gates, their symbols and the Boolean functions. For simplicity, only two inputs are shown (except for NOT gate), but more than two input gates are also commercially available.

Table 7.13 Logic gates symbols and functions

Sl. No.	Gate	Logic Symbol	Function	Commercial IC
1	AND		$Y = A \cdot B$	74LS08: Quad, 2-input AND gate.
2	OR		$Y = A + B$	74LS32: Quad, 2-input OR gate.
3	NOT		$Y = \overline{A}$	74LS04: Hex, 1-input NOT gate.
4	NAND		$Y = \overline{A \cdot B}$	74LS00: Quad, 2-input NAND gate.
5	NOR		$Y = \overline{A + B}$	74LS02: Quad, 2-input NOR gate.
6	EX-OR		$Y = A \oplus B$	74LS86: Quad, 2-input EX-OR gate.
7	EX-NOR		$Y = \overline{A \oplus B}$	—

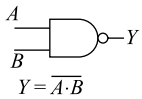
7.6 UNIVERSAL LOGIC GATES

As a simple example, consider realization of an INV gate, using a 2-input NOR gate or a 2-input NAND gate.

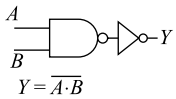
Simply connect the two inputs of the NOR gate together. Algebraically, if the two original NOR gate inputs are labeled B and C, and they are combined to form A, then we have the NOR gate output.

$Y = \overline{B + C} = \overline{A + A} = \overline{A}$, which is the INV operation. In a similar fashion, NAND and NOR gates may be used to realize any other function. This is illustrated in Figures 7.9 through 7.19.

7.6.1 NAND as Universal Gate



(a) NAND gate symbol



(b) NAND equivalent

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(c) Truth table

Fig. 7.8 NAND logic gate

Figure 7.8 presents NAND gate and its function table. Figure 7.9 through 7.13 illustrate various realizations using NAND gates.

1. NAND Gate Working as a NOT Gate

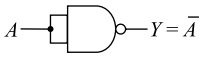


Fig. 7.9 Realisation of NOT function using NAND gate

We know that when the same input is applied to NAND then it becomes $\overline{AA} = \overline{A}$

2. NAND Gate Working as an AND Gate

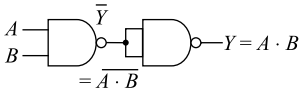


Fig. 7.10 Realisation of AND function using NAND gate

The above arrangement results in an AND gate function realisation. This can be understood by considering the Boolean simplification shown below:

$$Y = \overline{\overline{Y}}$$
$$Y = \overline{\overline{A \cdot B}}$$
$$Y = \overline{\overline{A} + \overline{B}}$$
$$Y = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

The simplification procedure needs the use of Boolean postulates and De Morgan's theorems.

3. NAND Gate Working as an OR Gate

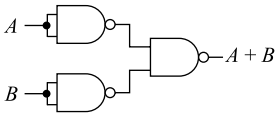


Fig. 7.11 Realisation of OR function using NAND gate

The above arrangement results in an OR gate function realisation. This can be understood by considering the Boolean simplification shown below:

$$Y = \overline{\overline{A \cdot A}\ \overline{B \cdot B}}$$
$$Y = \overline{\overline{A} \cdot \overline{B}}$$
$$Y = \overline{\overline{A}} + \overline{\overline{B}} = A + B$$

The simplification procedure needs the use of Boolean postulates and De Morgan's theorems.

4. NAND Gate Working as an EX-OR Gate

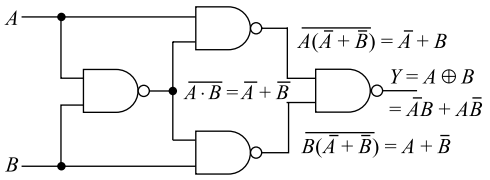


Fig. 7.12 Realisation of EX-OR function using NAND gate

The above arrangement results in an EX-OR gate function realisation. This can be understood by considering the Boolean simplifications shown at each gate output. The simplification procedure needs the use of Boolean postulates and De Morgan's theorems. The final expression indicates the output Y is EX-OR of inputs A and B.

5. NAND Gate Working as an EX-NOR Gate

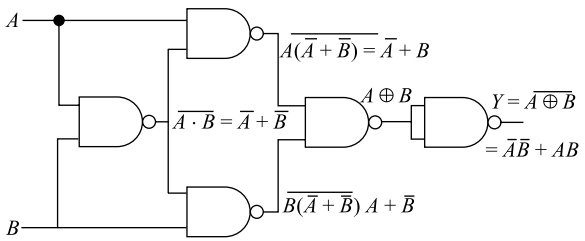
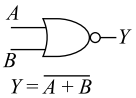


Fig. 7.13 Realisation of EX-NOR function using NAND gate

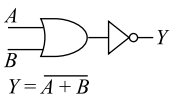
The EX-NOR function can be realised simply by adding an additional NAND as the last stage which is functioning as an inverter and this is indicated in Fig. 7.13.

7.6.2 NOR as Universal Gate

Figure 7.14 presents a NOR gate and its function table. Figures 7.15 through 7.19 illustrate various realizations using NOR gates.



(a) NOR gate symbol



(b) NOR equivalent

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(c) Truth table

Fig. 7.14 NOR logic gate

1. NOR Gate Working as a NOT Gate

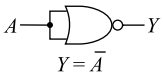


Fig. 7.15 Realisation of NOT function using NOR gate

We know that when the same input is applied to NOR gate, it becomes $\overline{AA} = \overline{A}$

2. NOR Gate Working as an OR Gate

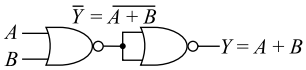


Fig. 7.16 Realisation of OR function using NOR gate

The above arrangement results in an OR gate function realisation. This can be understood by considering the Boolean simplification shown below:

$$Y = \overline{\overline{Y}}$$
$$Y = \overline{\overline{\overline{A + B}}}$$
$$Y = \overline{\overline{A} \cdot \overline{B}}$$
$$Y = \overline{\overline{A}} + \overline{\overline{B}}$$
$$Y = A + B$$

The simplification procedure needs the use of Boolean postulates and De Morgan's theorems. The final expression indicates the output Y is OR of inputs A and B.

3. NOR Gate Working as an AND Gate

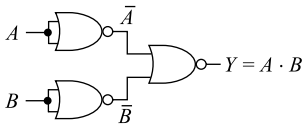


Fig. 7.17 Realisation of AND function using NOR gate

The above arrangement results in an AND gate function realisation. This can be understood by considering the Boolean simplification shown below:

$$Y = \overline{\overline{A} + \overline{B}}$$
$$Y = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

The simplification procedure needs the use of Boolean postulates and De Morgan's theorems. The final expression indicates the output Y is AND of inputs A and B.

4. NOR Gate Working as an EX-OR Gate

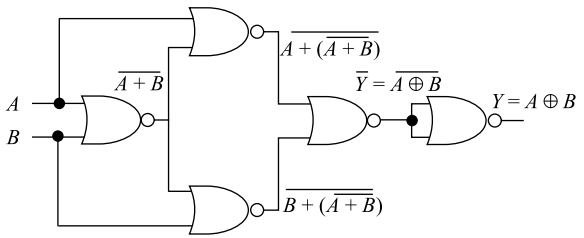


Fig. 7.18 Realisation of EX-OR function using NOR gate

The above arrangement results in an EX-OR gate function realisation. This can be understood by considering the Boolean simplifications shown at each gate output. The simplification procedure needs the use of Boolean postulates and De Morgan's theorems. The final expression indicates the output Y is EX-OR of inputs A and B.

5. NOR Gate Working as an EX-NOR Gate

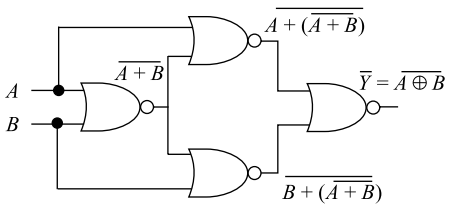


Fig. 7.19 Realisation of EX-NOR function using NOR gate

The EX-NOR function can be realised simply by eliminating the last-stage NOR gate which is functioning as an inverter and this is indicated in Fig. 7.19.

7.7 BOOLEAN POSTULATES

A switching function containing input variables represents a digital system. The logic realisation of these functions directly may not be economical and efficient on many occasions. These functions can be simplified to an extent still maintaining the desired output and then implemented which results in a lot of cost, area and power optimisation. For the process of optimisation, several popular methods such as Venn diagrams, Boolean algebra, Karnaugh maps, etc. are available. George Boole (1815–1864) developed an algebra known as **Boolean algebra** to evaluate the truth or false of a set of propositions either singly or joined together by basic logical connections. The use of symbols to represent propositions, conditions, truth and false conditions lead to the name **symbolic logic**. In 1938, *C*laude Shannon described the method of using Boolean algebra to represent two-state circuits (or binary circuits). This principle is used in all switching networks (computers). Boolean algebra can be used to formalise the combinations of binary logic states. The fundamental relations are given in Table 7.14 of the text. In these relations, A and B are binary quantities, that is, they can be either logical true (T or 1) or logical false (F or 0). Most of these relations are obvious and some of them can be proved using simple steps.

Example 7.24

Prove the following Boolean theorems.

(i) $A + AB = A$ (ii) $A + \overline{A}B = A + B$

Solution The above theorems can be proved in two ways: one is the truth-table method and the second one is by using Boolean theorems.

(i) $\boldsymbol{A + AB = A}$

(a) *Using truth-table method (also called* ***perfect induction method****)*

It can be observed here that the columns 1 and 4 are same and hence $A + A \cdot B = A$.

A	B	$A \cdot B$	$A + A \cdot B$
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

Table 7.14 Boolean postulates

Sl. No.	Boolean Postulate	Remarks
1	$A \cdot A = A$	**AND theorems**
2	$A \cdot \overline{A} = 0$	
3	$A \cdot 1 = A$	
4	$A \cdot 0 = 0$	
5	$A + \overline{A} = 1$	**OR theorems**
6	$A + A = A$	
7	$A + 1 = 1$	
8	$A + 0 = A$	
9	$A + AB = A$	
10	$A + \overline{A}B = A + B$	
11	$\overline{A} + AB = \overline{A} + B$	
12	$(A + B)(A + C) = A + BC$	
13	$A + B = B + A$	**Commutative law**
14	$A \cdot B = B \cdot A$	
15	$A + A \cdot B = A$	**Absorption law**
16	$A \cdot (A + B) = A$	
17	$A + (B + C) = (A + B) + C$	**Associative law**
18	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$	
19	$A + B \cdot C = (A + B) \cdot (A + C)$	**Distributive law**
20	$A \cdot (B + C) = A \cdot B + A \cdot C$	

(b) *Using Boolean postulates*

$A + AB = A\ (1 + B)$: taking A as common factor

$= A \cdot 1$: we know that $1 + B = 1$

Hence, the law is proved.

(ii) $\boldsymbol{A + \overline{A}B = A + B}$

(a) *Using truth-table method*

A	B	$\overline{A}B$	$A + \overline{A}B$	$A + B$
0	0	0	0	0
0	1	1	1	1
1	0	0	1	1
1	1	0	1	1

It can be observed here that the columns 4 and 5 are same and hence $A + \overline{A} \cdot B = A + B$.

(b) *Using Boolean postulates*

$$A + \overline{A}B = A\,(1 + B) + \overline{A}B\text{: multiplying } A \text{ by } (1 + B) = 1$$
$$= A + AB + \overline{A}B$$
$$= A + AB + \overline{A}B = A + B\,(\mathrm{A} + \overline{A})\text{: taking } B \text{ as common factor}$$
$$= A + B$$

Hence, the law is proved.

7.8 DE MORGAN'S THEOREMS

In addition to the powerful set of Boolean postulates, there are two De Morgan theorems that can be used to simplify digital switching functions. These laws combined with Boolean postulates form a very powerful tool and are widely used in the process of simplification. The two De Morgan's theorems turn out to be quite useful and we shall use them often. The two laws can be stated, proved and represented symbolically by the diagrams shown in Fig. 7.20.

(a) First law (a) Second law

Fig. 7.20 De Morgan's laws

Theorem 1

De Morgan's first law states that the complement of the sum of all input variables is equivalent to the product of all individual complement of input variables.

$$\overline{A + B + C + \cdots} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \cdots \tag{7.14}$$

Proof: Using truth-table method and considering only two input variables:

A	B	$\overline{A+B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

It can be observed here that columns 3 and 4 are same and hence, the statement.

Theorem 2

De Morgan's second law states that the complement of the product of all input variables is equivalent to the sum of all individual complement of input variables.

$$\overline{A \cdot B \cdot C \cdot \cdots} = \overline{A} + \overline{B} + \overline{C} + \cdots \tag{7.15}$$

Proof: Using truth-table method and considering only two input variables:

A	B	$\overline{A \cdot B}$	$\overline{A} + \overline{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

It can be observed here that columns 3 and 4 are same and hence, the statement.

7.9 SIMPLIFICATION OF BOOLEAN SWITCHING FUNCTIONS

A digital system can be represented either using a function table or a switching function. The switching function is nothing but an expression containing a set of product terms called **minterms** or a set of sum terms called **maxterms**. The switching function containing a set of minterms is called **SOP (Sum Of Product)** expression and that containing a set of maxterms is called **POS (Product Of Sum)** expression. This switching function is then realised using logic gates discussed in Section 7.6; however, before realisation, the switching function can be simplified to reduce the number of minterms or maxterms still maintaining the functionality of the system. Simplification of switching functions offers the following advantages:

(i) The number of terms and hence the hardware for implementation is reduced.
(ii) Reduced hardware reduces the cost of system implementation.
(iii) Reduced hardware reduces area of implementation.

Several methods are in use for simplification of switching functions. Some of them are Boolean-postulate simplification, K-map simplification, VEM (Variable Entered Mapping) simplification, Quine Mc Clusky simplification, Venn-diagram simplification, etc. Here, only the first two methods are discussed.

7.9.1 Simplification Using Boolean Postulates

We observed that a switching function in the form of a truth table representing any system can be realised directly by using a set of basic or universal gates. However, such a procedure could produce very lengthy and needlessly inefficient systems. There are several methods for simplification of Boolean logic expressions also called **logic minimisation** and the goal is to form a result which is highly optimised and efficient. Examples 7.25 and 7.26 illustrate logic minimisation using Boolean postulates and De Morgan's laws.

Example 7.25

Find minimal SOP expression for the switching function

$$f(A, B, C, D) = A(C + D)'\,(B' + D') + C(B + C' + A'D).$$

Solution Given

$$\begin{aligned} f(A, B, C, D) &= A(C + D)'(B' + D') + C(B + C' + A'D) && (7.16)\\ &= A(C'D')(B' + D') + BC + CC' + A'CD; && \text{using De Morgan's first law}\\ &= AB'C'D' + AC'D'D' + BC + CC' + A'CD; && \text{use of distributive law}\\ &= AB'C'D' + AC'D' + BC + A'CD; && \text{because } D'D' = D' \text{ and } CC' = 0. \end{aligned}$$

$= AC'D'(B' + 1) + BC + A'CD$: taking common factor between the first two
$= AC'D' + BC + A'CD$: because $(B' + 1) = 1$ (7.17)

Looking at the simplified expression, it is clear that Eq. (7.16) and Eq. (7.17) produce the same output, but Eq. (7.17) is more optimised and less expensive to implement.

Example 7.26

Simplify the switching function in Eq. (7.18) using Boolean postulates and implement the logic diagram for the simplified expression.

$$F_{(A, B, C, D)} = (A \cdot B + C)(A \cdot B + D) \tag{7.18}$$

Solution Given $F_{(A, B, C, D)} = (A \cdot B + C)(A \cdot B + D)$
We know that $(P + Q)(P + R) = P + QR$.
Substitute P for $A \cdot B$, Q for C and R for D; then we get

$$\begin{aligned} F_{(A, B, C, D)} &= (P + Q)(P + R) \\ &= (PP + PR + PQ + QR) \\ &= P + P(R + Q) + QR \\ &= P(1 + R + Q) + QR = P + QR \\ F_{(A, B, C, D)} &= A \cdot B + C \cdot D \end{aligned} \tag{7.19}$$

Looking at the simplified expression, it is clear that Eq. (7.18) and Eq. (7.19) produce the same output, but Eq. (7.19) is more optimised and less expensive to implement. Equation (7.19) can be implemented either using the basic gates or the universal gates; the implemented logic diagram is as shown in Fig. 7.21. It is recommended to use universal NAND gates to implement a SOP expression and universal NOR gates to implement a POS expression.

(a) Using basic gates (b) Using NAND gates

Fig. 7.21 Logic realisation of Eq. (7.19)

7.9.2 Simplification using Karnaugh Maps

On a number of occasions, Boolean simplification may not be ideal and may not result in an optimised expression. Therefore, one can use Karnaugh maps popularly called **K-maps**, to simplify a given switching function. K-maps give the best solution to simplification problems and are ideal for up to 5 input variables. If the number of input variables is more than 5, this method becomes slightly cumbersome. K-map is an abstract form of Venn diagram and is a graphical (map) representation of the given switching function organised as a matrix of cubes, where each cube represents a minterm (SOP) or a maxterm (POS) and adjacent cubes always differ by just one literal. Consider a digital system with two input variables A and B: the K-map for any expression containing these two variables can be drawn and the variables can be entered into the map as indicated in Fig. 7.22. The map can be drawn in the following two forms: in each form the representation of the input variable differs and hence the weightage for each cube differs. As indicated inside the parenthesis in the bottom corners, the weightage for box-2 in form-1 is 1 and in form-2, it is 2. This is because of the representation of the variables.

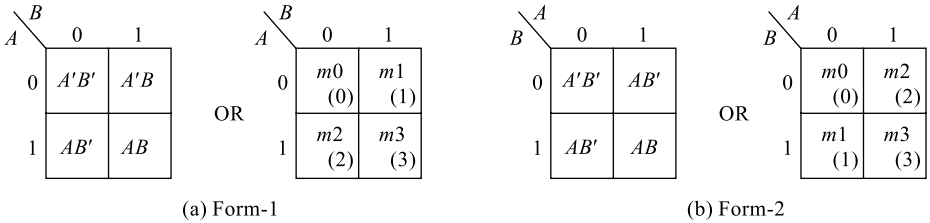


Fig. 7.22 *A two-variable K-map*

The K-map simplification procedure for any switching function is as indicated below and let us consider a switching function $f_{(A, B)} = \Sigma_m(0, 1, 2)$

(i) Prepare a map as indicated in Fig. 7.22(a) above, the number of cubes N in the map and the number of input variables n are related by Eq. (7.20).

$$N = 2^n \tag{7.20}$$

(ii) Assign variables to each square box, obtain the weightage for each box and enter each minterm/maxterm into the respective box.

(iii) Form groups of adjacent 1s (adjacent 0s for POS); the group should contain a maximum number of such adjacent cubes in multiples of powers of 2; for example, $2^0 = 1$, $2^1 = 2$, $2^2 = 4$, etc. The groups can overlap, and a cube can be used by any number of groups.

(iv) Write the expression for each group in terms of the input variables by reading the group first rowwise and then columnwise. Eliminate the complemented variable from the output expression and retain only the common variable from each cube.

(v) OR together these expressions in case of SOP simplification and AND these expressions in the case of POS simplification.

(vi) The simplified expression so obtained can be implemented then using the required hardware.

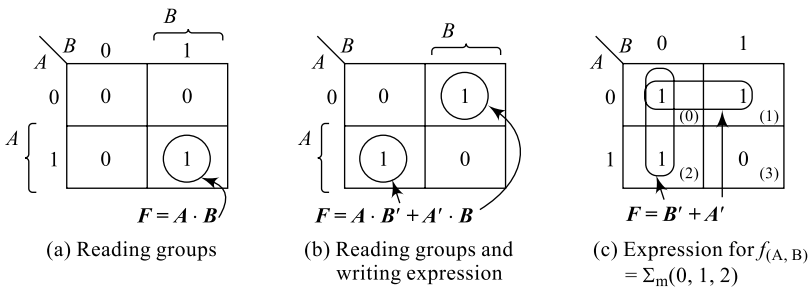


Fig. 7.23 *A two-variable K-map grouping and reading*

The grouping and writing the expressions for such groups is indicated in Fig. 7.23(a) and 7.23(b). For the given example $f_{(A, B)} = \Sigma_m(0, 1, 2)$, the simplified expression is obtained from Fig. 7.23(c) and is given by Eq. (7.21). The grouping results in two pairs: vertical group containing cubes 0 and 2 is one pair and the horizontal group containing cubes 0 and 1 is another. Reading group-1 results in B' and reading group-2 results in A' and the final SOP expression is

$$F = A' + B' \tag{7.21}$$

Three- and Four-Variable K-maps

A three-variable K-map contains $2^3 = 8$ cubes in it and is represented in Fig. 7.24. *A* four-variable K-map contains $2^4 = 16$ cubes in it and is represented in Fig. 7.25. The procedure for entering, grouping and reading is same as explained for a two-variable map. This is made more understandable in examples 7.27 to 7.30.

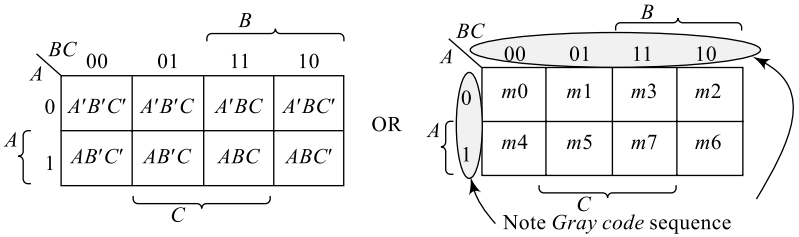


Fig. 7.24 *A three-variable K-map*

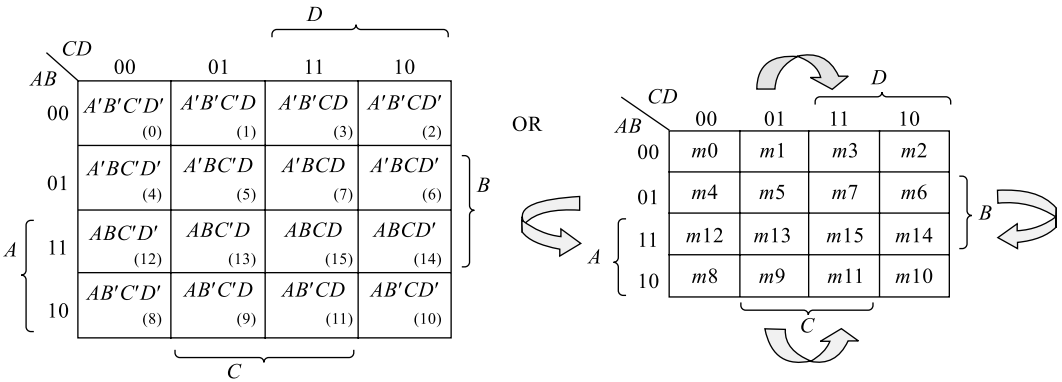


Fig. 7.25 *A four-variable K-map*

In the process of simplification, the following groups can be formed and each group contributes in a way to the simplification process. While forming groups, maximum number of cubes have to be included in a group and this number is an integer power of 2: for example in a 4-variable map, a group of all 16 cells have to be tried, if that is not possible, then an Octet may be tried. Higher the number of cells in a group, lower will be the number of variables in the output expression and hence lower will be the cost of implementation.

Important Terms in K-map Simplification

Min Term Each fundamental product term that occupies a single cell in K-map is called 'minterm' for sop expression.

Max Term Each fundamental sum term that occupies a single cell in K-map is called 'maxterm' for pos expression. Both minterm and maxterm are called implicants.

Prime Implicant (PI) A PI is a product term or sum term obtained by combining the maximum possible number of miniterms or maxterms from adjascent squores in the map.

Essential Prime Implicants (EPI) An EPI is a prime implicants that contains at least one implicant that is not covered by any other prime implicant.

Pair A pair is a group of two adjacent 1s/0s and a pair eliminates one variable ($2^1 = 2$) in the corresponding SOP term in the output expression.

Quad A quad is a group of four adjacent 1s/0s and a quad eliminates two variables ($2^2 = 4$) in the corresponding SOP term in the output expression. *A* pair and a quad are indicated in Example 7.29.

Octet An octet is a group of eight adjacent 1s/0s and an octet eliminates three-variables ($2^3 = 8$) in the corresponding SOP term in the output expression. An octet is indicated in Example 7.27.

Redundant Group A redundant group is one in which all the elements of this group are covered by the neighbouring groups. A redundant group is indicated in Example 7.28.

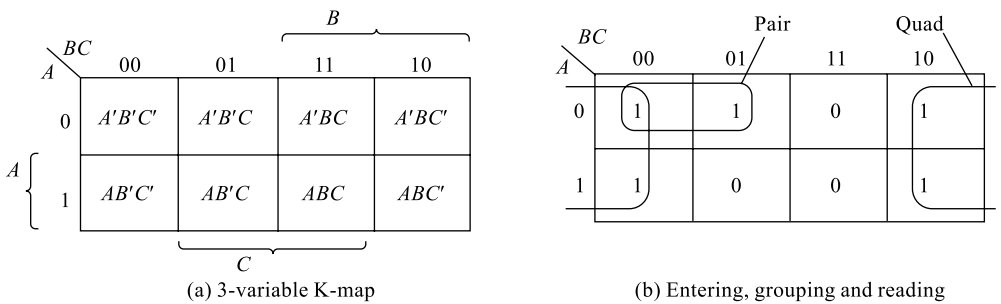
Don't-care Condition *A* don't care condition in a K-map is a situation on inputs where the output can be anything like a logic high or a logic low. It has no influence on the performance of the system. Don't care conditions are represented using '**x**' or '**d**' or '**Φ**' in the expression and in the K-map. This don't care condition can be used to simplification advantage that while grouping is needed, it can be treated as a logic-1 (logic-0 for POS). This is demonstrated in Example 7.29.

Example 7.27

Simplify the switching function $f_{(A, B, C)} = A'B'C' + A'B'C + A'BC' + AB'C' + ABC'$ using a K-map.

Solution The 3-variable K-map is prepared as indicated in Fig. 7.26(a) and switching function is entered and grouped as indicated in Fig. 7.26(b). Reading the pair results in $A'B'$ and reading the quad results in C'; hence the final simplified expression for the given switching function is

$$f_{(A, B, C)} = A'B' + C' \tag{7.22}$$



(a) 3-variable K-map (b) Entering, grouping and reading

Fig. 7.26 K-map for Example 7.27

Comparing Eq. (7.22) with the original switching function, it is clear that the simplification process resulted in a considerable amount of hardware reduction.

Example 7.28

Simplify the switching function $f_{(A, B, C, D)} = A'BC'D' + A'BC'D + ABC'D + AB'C'D + ABCD' + A'B'CD + A'BCD + ABCD$ using a K-map.

Solution The 4-variable K-map is prepared as indicated in Fig. 7.28 and switching function is entered. Grouping is done starting with a quad followed by four pairs. It can be observed that all the ele-

ments of the quad are covered by the neighbouring pairs. Hence, the quad becomes a redundant group. Reading the pair-1 results in $A'BC'$, reading the pair-2 results in $A'CD$, reading the pair-3 results in ABC and reading the pair-4 results in $AC'D$; hence the final simplified expression for the given switching function is

$$f_{(A, B, C)} = A'BC' + A'CD + ABC + AC'D \quad (7.23)$$

Comparing Eq. (7.23) with the original switching function, it is clear that the simplification process resulted in a considerable amount of hardware reduction.

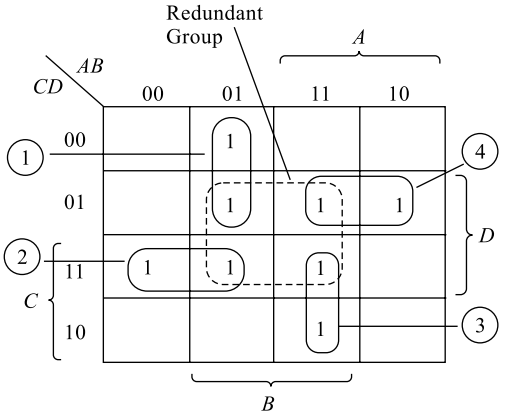


Fig. 7.27 K-map for Example 7.28

Example 7.29

Simplify the switching function $f_{(A, B, C, D)} = \Sigma_m (4, 5, 6, 7, 12, 13, 14) + \Sigma_d (11, 15)$ using a K-map.

Solution The 4-variable K-map is prepared as indicated in Fig. 7.28 and the switching function is entered. Grouping is done considering don't care condition of minterm m15 as logic 1 and minterm m14 as logic 0. The octet is formed using the don't care at cube-m15 and reading the octet results in the SOP term *B*. This itself is the simplified expression,

i.e. $$f_{(A, B, C, D)} = B \quad (7.24)$$

Comparing Eq. (7.24) with the original switching function, it is clear that the simplification process resulted in a considerable amount of hardware reduction.

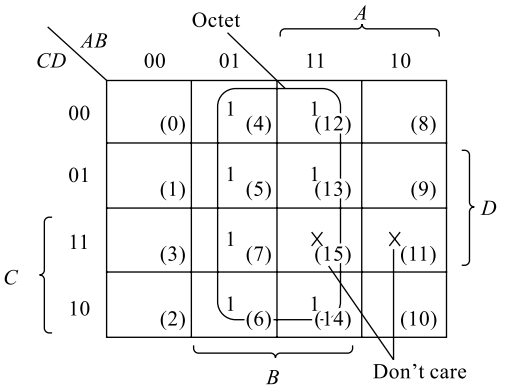


Fig. 7.28 K-map for Example 7.29

7.10 COMBINATIONAL AND SEQUENTIAL CIRCUITS

Digital circuits can be broadly classified into two categories based on their ability to store the information, namely combinational circuits and sequential circuits.

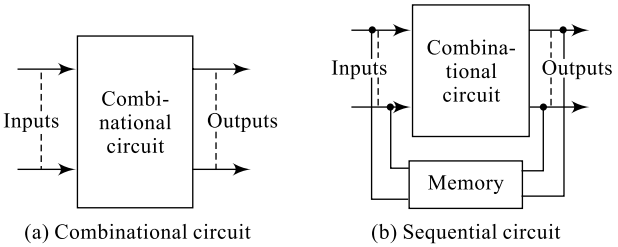
1. Combinational Circuit

A combinational circuit is one whose present state output depends only on the present state of inputs; no information about the previous output or input will be available in order to determine the present output state. Hence, it is obvious that a combinational circuit does not have memory in it and hence cannot store. Arithmetic circuits like adders, subtractors, multiplexers, de-multiplexers, encoders, decoders, gates, etc. are all some examples of combinational circuits. The block diagram of a combinational circuit is shown in Fig. 7.29(a) and some examples of combinational circuits are introduced in Section 7.11.

2. Sequential Circuit

A sequential circuit is one whose present state output depends not only on the present state of inputs, but also on the previous output; hence information about the previous output should be made available

in order to determine the present output state. Hence, it is obvious that a sequential circuit does have memory in it and hence can store. Latches, flip-flops, counters, registers, etc. are some examples of sequential circuits. The block diagram of a sequential circuit is shown in Fig. 7.29(b) and some examples of combinational circuits are introduced in Section 7.12.



(a) Combinational circuit (b) Sequential circuit

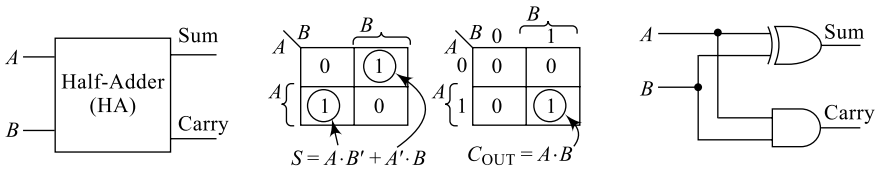
Fig. 7.29 Combinational and sequential circuit

7.11 ARITHMETIC CIRCUITS

Arithmetic circuits are used to implement basic arithmetic operations such as addition, subtraction, multiplication, etc. Multiple bits of binary numbers can be added sequentially using a serial adder or simultaneously using a parallel adder. Subtraction of binary numbers can be performed using an adder circuit with inputs controlled; in fact, any arithmetic or logic operation can be done using a parallel adder and an associated combinational circuit.

7.11.1 Half Adder

A **half adder** is an arithmetic circuit that performs an addition operation on two binary digits A and B; the carry generated from earlier stages will not be taken into consideration. The half adder produces a sum and carry bits as outputs and this is indicated in the form of a block diagram in Fig. 7.30(a). The functional description of a half adder is given in Table 7.15. The simplified expressions for sum and carry outputs are given in Fig. 7.30(b) and the logic diagram implementation is given in Fig. 7.30(c).



(a) Block diagram (b) K-map simplifications (c) Logic diagram

Fig. 7.30 Half adder

Table 7.15 Half-adder truth table

A	B	S	C_{OUT}
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The SOP expressions for sum and carry output of a half adder are given in Eq. (7.25).

$$S = A \oplus B \qquad [7.25(a)]$$

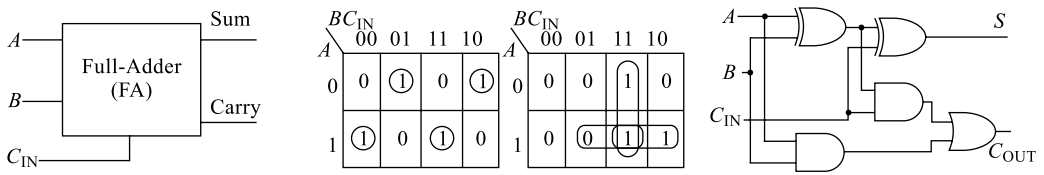
And

$$C_{OUT} = AB \qquad [7.25(b)]$$

A **half adder** has two inputs, generally labelled *A* and *B*; and two outputs, the sum *S* and carry C_{OUT}. The K-map simplification of *S* results in the XOR of *A* and *B*, and *C* results in the AND of *A* and *B*. The drawback of this circuit is that in the case of a multi-bit addition, the present stage cannot include the carry output from its previous stage for addition.

7.11.2 Full Adder

A **full adder** is an arithmetic circuit that performs an addition operation on three binary digits *A, B* and C_{IN}: the carry generated from earlier stages is also taken into consideration. The full adder produces a sum and a carry bits as outputs and this is indicated in the form of a block diagram in Fig. 7.31(a). The functional description of a full adder is given in Table 7.16, the simplified expressions for sum and carry outputs are given in Fig. 7.31(b) and the logic diagram implementation, in Fig. 7.31(c).



(a) Block diagram (b) K-map simplifications (c) Logic diagram

Fig. 7.31 Full adder

Table 7.16 Full-adder truth table

A	*B*	C_{IN}	*S*	C_{0UT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A **full adder** has three inputs, generally labelled *A*, *B* and C_{IN}, and two outputs, the sum *S* and carry C_{OUT}. The K-map simplification of *S* results in the XOR of *A*, *B* and C_{IN}, and C_{OUT} results in the expression $C_{OUT} = AB + BC_{IN} + AC_{IN}$. The advantage of a full-adder realisation is that even by using two HAs, a FA can be realised and this circuit is suitable for a multi-bit addition because the present-stage carry input is the carry output from its previous stage.

Alternatively, the simplified SOP forms of sum and carry expressions can be obtained using basic Boolean postulates. The SOP expression for sum *S* can be obtained starting from the basic expression written by reading the sum column in Table 7.16.

$$\begin{aligned} S &= A'B'C_{IN} + A'BC'_{IN} + AB'C'_{IN} + ABC_{IN} \\ &= A'(B'C_{IN} + BC'_{IN}) + A(B'C'_{IN} + BC_{IN}) \\ &= A'(B \oplus C_{IN}) + A(B \oplus C_{IN})' \end{aligned} \tag{7.26}$$

Let $(B \oplus C_{IN}) = P$ and hence $(B \oplus C_{IN})' = P'$

Now the expression becomes

$$S = A'P + AP' = A \oplus P$$

$$S = A \oplus (B \oplus C_{IN}) \tag{7.27}$$

Similarly, the SOP expression for carry C_{OUT} can be obtained starting from the basic expression written by reading the carry column in Table 7.16.

$$C_{OUT} = A'BC_{IN} + AB'C_{IN} + ABC'_{IN} + ABC_{IN} \tag{7.28}$$

$$= A'\,BC_{IN} + AB'C_{IN} + AB\,(C'_{IN} + C_{IN})$$

$$= (A \oplus B)C_{IN} + AB$$

$$= A'BC_{IN} + AB'C_{IN} + AB$$

$$= A'BC_{IN} + A\,(B'C_{IN} + B)$$

$$= A'BC_{IN} + A\,(C_{IN} + B)$$

$$= A'BC_{IN} + AC_{IN} + AB$$

$$= C_{IN}\,(A'B + A) + AB = C_{IN}\,(B + A) + AB = AB + BC_{IN} + AC_{IN} \tag{7.29}$$

Note that the final OR gate before the carry-out output may be replaced by an XOR gate without altering the resulting logic. This is because the only discrepancy between OR and XOR gates occurs when both inputs are 1; for the adder shown here, this is never possible. Using only two types of gates is convenient when it is to implement the adder directly using common IC chips.

7.11.3 Full Adder Using Two-Half Adders

A full adder can be constructed and realised using two half adders; this is indicated in Fig. 7.32. By connecting A and B to the input of the first half adder, we obtain the partial sum $A \oplus B$ and the partial carry AB as outputs. Now, connecting the partial sum from the first half adder and the carry input C_{IN} as inputs to the second half adder, we obtain the final sum and carry outputs. The intermediate carries from HA-1 and HA-2 are ORed together to get the final C_{OUT}. It can be shown that the final sum and carry for the arrangement are as represented in Eq. (7.27) and Eq. (7.29).

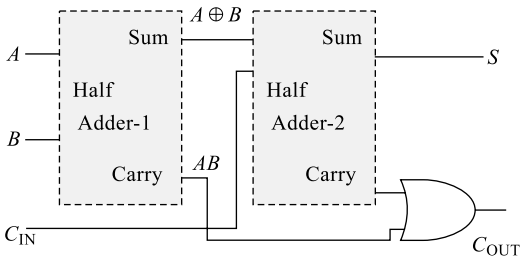


Fig. 7.32 Full adder using two half adders

7.11.4 A 4-bit Parallel Adder

A **full adder** has three inputs, A, B and C_{IN}, and two outputs, S and C_{OUT}, such that multiple full adders can be connected in parallel to add multi-bit numbers; this results in a parallel adder. The arrangement of a 4-bit parallel adder is shown in Fig. 7.33 and it can be extended to add more number of bits. Each

stage shown is a FA: however, the first stage can be a half adder, since there is no need of C_{IN} for this stage. Each *F*A receives three inputs and produces two outputs. The carry output from each stage forms the carry input to the next stage (as in conventional multi-bit addition). This circuit produces the sum output after a total delay of approximately 4-stage delay, where each stage delay is the propagation delay for the input to propagate to the output. This circuit is faster than a serial adder (not discussed here) that can be used alternatively to add multiple bits.

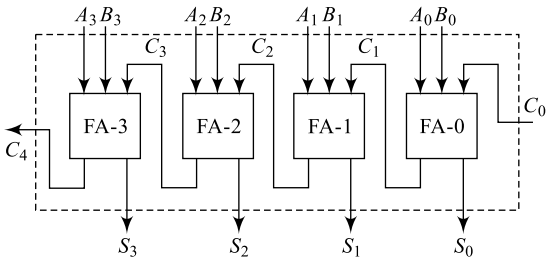


Fig. 7.33 Four-bit parallel adder using full adders

7.11.5 Adder/Subtractor using Parallel Adder

A parallel adder can be used to realise even the subtraction of two multi-bit numbers. The fact is that a parallel adder forms the basic building block of any arithmetic or logic operations. The arrangement of a 4-bit adder/subtractor is shown in Fig. 7.34; here, a 4-bit parallel adder performs both addition and subtraction operations. The subtraction operation uses an additional combinational unit called **controlled inverter** and follows 2's complement addition procedure.

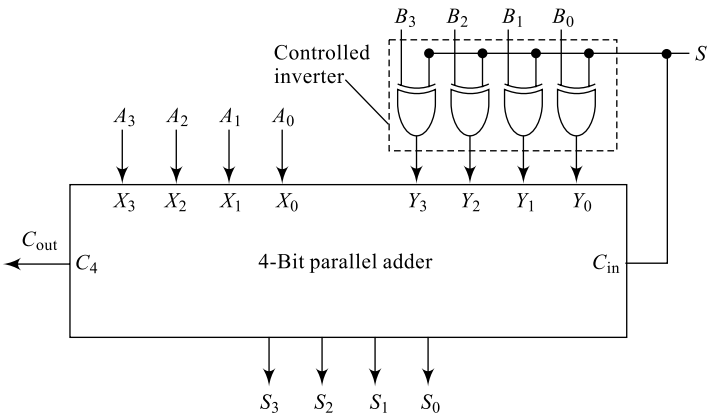


Fig. 7.34 Adder/Subtractor using parallel adders

The control input S decides the addition or subtraction to be performed: $S = 0$ for addition and $S = 1$ for subtraction. During addition, with $S = 0$, the output of the controlled inverter will be directly B_i, $C_{IN} = 0$ and hence addition of A_i and B_i is carried out. During subtraction, with $S = 1$, the output of the controlled inverter will be 1s complement of B_i, $C_{IN} = 1$ resulting in a 2s complement number at Y_i and hence addition of A_i and 2s complement of B_i is carried out which is nothing but the subtraction. Example 7.30 clearly depicts the addition and subtraction procedure using the above circuit.

Example 7.30

Perform the following binary arithmetic operations using the circuit of Fig. 7.34.

(i) 9 + 6 (ii) 9 – 6

Solution

(i) The binary form of the given numbers and addition is as below:

$$\begin{array}{rcr} 09_{10} & \rightarrow & 1001_2 \\ +\,06_{10} & \rightarrow & 0110_2 \\ \hline 15_{10} & & 1111_2 \end{array}$$

(ii) The binary form of +9 is 1001_2 and the 1's complement of –6 is 1001_2 produced by the controlled inverter and its 2's complement is $(1001 + 1)_2 = 1010_2$

Now, addition of these two is as below:

$$\begin{array}{rcr} 09_{10} & \rightarrow & 1001_2 \\ -\,06_{10} & \rightarrow & 1010_2 \\ \hline 03_{10} & & \mathbf{1}\,0011_2 \end{array}$$

Ignore the carry generated.

7.12 LATCHES AND FLIP-FLOPS

We now turn our attention to sequential digital circuits that have states which change in time, usually according to an external clock: latches and flip-flops. These circuits form important elements of digital system building. The sequential circuits have the interesting property of storing information, i.e. memory, and these can be set to a state which is retained until explicitly reset or changed by an external signal. Latches are the storing elements without an external clock signal for controlling and flip-flops are the latches with clock signals for external control and synchronisation.

7.12.1 *SR* Flip-Flop

The simplest type of storage device is the Set-Reset flip-flop (*SR*-FF) and can be constructed using two NAND or NOR gates. Figure 7.35 illustrates the *SR*-FF using NAND, its function table and the logic symbol. It has two inputs named *S* and *R* and two outputs *Q* and *Q′* that are complements of each other: here, *Q* is called TRUE output and *Q′* is called the COMPLEMENT output. The output Q_{n+1} indicates the next-state output while Q_n indicates the present-state output. The working of each latch can be understood by using the respective function table. Consider the latch in Fig. 7.35(a):

Case 1

When $R = 0$ and $S = 0$

Assuming that the present true output *Q* is at logical-1 and the two inputs are low: both the outputs will be at logical-1. This violates the condition on outputs that they should be complements of each other and hence is an '**invalid**' condition as indicated in the first row of the function table.

Case 2

When $R = 0$ and $S = 1$

Assuming that the present true output *Q* is at logical-1 and the inputs $R = 0$ and $S = 1$: the output of *G*2 becomes logical-0. This maintains a logical-1 at the output of *G*1. Thus, with $S = 1$, the output is

set and hence this terminal is called **set (*S*) terminal**. This is indicated as the **SET** state in the second row of the function table.

Case 3

When $R = 1$ and $S = 0$

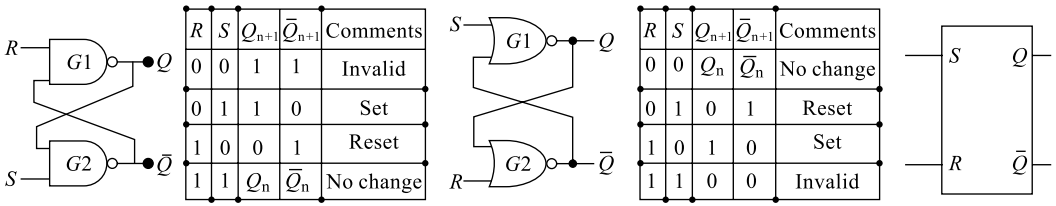
Assuming that the present true output Q is at logical-1 and the inputs $R = 1$ and $S = 0$: the output of $G2$ becomes logical-1. This changes the output of $G1$ to a logical-0. Thus, with $R = 1$, the output is reset and hence this terminal is called **reset (R) terminal**. This is indicated as the **RESET** state in the third row of the function table.

Case 4

When $R = 1$ and $S = 1$

Assuming that the present true output Q is at logical-1 and the two inputs are high, the output of $G2$ will be at logical-0. This will maintain a logical-1 on Q. Similarly, if the true output Q is assumed to be at logical-0 then the output of $G2$ will be at logical-1. This will maintain a logical-0 on Q. Hence, $Q_{n+1} = Q_n$ and this condition is indicated as **No change** in the fourth row of the function table.

It is evident from the function table that the latch contents are stable and change only when there is a change in the applied inputs; thus, a latch is capable of storing one bit of information, a 0 or a 1. It can also be used as a '**switch de-bouncer**' to provide bounce-free switch contacts.



R	S	Q_{n+1}	$\bar{Q}_{n+1}$	Comments
0	0	1	1	Invalid
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q_n	$\bar{Q}_n$	No change

(a) Using NAND gates

R	S	Q_{n+1}	$\bar{Q}_{n+1}$	Comments
0	0	Q_n	$\bar{Q}_n$	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Invalid

(b) Using NOR gates

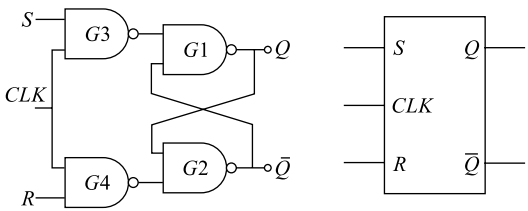
(c) Logic symbol

Fig. 7.35 *SR* latches

The working of an *SR* latch using NOR gates can be explained in a similar way and the circuit functions in a similar manner. The logic diagram and the truth table are shown in Fig. 7.35(b). The logic symbol of an *SR* latch is shown in Fig. 7.35(c).

7.12.2 Clocked *SR* Flip-Flop

A basic *SR* latch can be converted into a flip-flop by adding gates $G3$ and $G4$ at the input: one input from both $G3$ and $G4$ tied together to receive a common clock. The flip-flop can then be made to respond to input levels only during the occurrence of a clock pulse. The logic diagram and the logic symbol of a clocked *SR* flip-flop are shown in Fig. 7.36. The working of this clocked *SR*-FF can be understood by using its function table shown in Table 7.17.



(a) Using NAND gates

(b) Logic symbol

Fig. 7.36 *SR* flip-flop

Table 7.17 SR-FF (clocked) truth table

CLK	*S*	*R*	Q_{n+1}	$\overline{Q}_{n+1}$	Remarks
0	x	x	Q_n	Q_n	No change
1	0	0	1	0	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	1	1	Invalid

The outputs from the two NAND gates *G*3 and *G*4 remain unchanged as long as the clock pulse is '0' regardless of the *S* and *R* inputs. When the clock pulse goes to 1, informations on the *S* and *R* inputs are allowed to reach the basic latch formed of gates *G*1 and *G*2. This is indicated in the first row of the function table.

Case 1

When $R = 0$ and $S = 0$

Assuming that the present true output *Q* is at logical-1 and the two inputs are low; outputs of both *G*3 and *G*4 will be at logical-1, once again resulting in no change in the output. This is indicated in the second row of the function table.

Case 2

When $R = 0$ and $S = 1$

Assuming that the present true output *Q* is at logical-1 and the inputs $R = 0$ and $S = 1$; the output of *G*4 will at logical-1 and that of *G*3 will be at logical-0. This results in the second condition of the simple latch where Q_{n+1} will be at logical-1. Thus, with $S = 1$, the output is set and hence this terminal is called **set (*S*) terminal**. This is indicated as the '**SET**' state in the third row of the function table.

Case 3

When $R = 1$ and $S = 0$

Assuming that the present true output *Q* is at logical-1 and the inputs $R = 1$ and $S = 0$; the output of *G*3 will at logical-1 and that of *G*4 will be at logical-0. This results in the third condition of the simple latch where Q_{n+1} will be at logical-0. Thus, with $R = 1$, the output is reset and hence this terminal is called **reset (*R*) terminal**. This is indicated as the '**RESET**' state in the fourth row of the function table.

Case 4

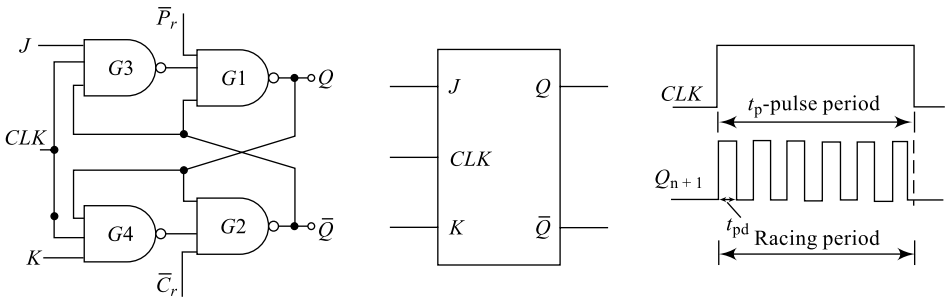
When $R = 1$ and $S = 1$

Assuming that the present true output *Q* is at logical-1 and the inputs $R = 1$ and $S = 1$; the output of both *G*3 and *G*4 will be at logical-0. This results in the first condition of the simple latch where Q_{n+1} and Q'_{n+1} will be at logical-1. This violates the condition on outputs that they should be complement of each other; and hence is an **invalid** condition as indicated in the last row of the function table.

The clock signal added to the basic latch helps synchronising the circuit with other circuits and the circuit responds to the clock signal changes. However, the problem of invalid condition continues to exist and in order to solve this problem, the circuit is included with the feedbacks. Inclusion of the feedback to the clocked *SR*-FF results in a *JK* flip-flop.

7.12.3 *JK* Flip-Flop

A *JK* flip-flop can be considered as a clocked *SR*-FF with feedback arrangements as shown in Fig. 7.37. The invalid condition in the *SR*-FF is a concern in using it for any application; hence, feedback is added to the circuit as shown. The true output Q is fed back to $G2$ and $G4$; similarly the complement output Q' is fed back to $G1$ and $G3$. J and K, along with CLK, form other inputs to $G1$ and $G2$. P'_r and C'_r are the two asynchronous inputs used to preset or clear the circuit output. In order to make it possible to start the circuit analysis with a pre-defined state (instead of assuming an output condition as in the case of *SR*-FF), P'_r and C'_r control terminals are added to the circuit. These are called **asynchronous** inputs because they can change the circuit output irrespective of clock and the inputs J and K. The first three rows of the function table indicate the asynchronous operation of these preset and clear inputs. When $P'_r = C'_r = 0$, the output of both $G1$ and $G2$ will be high. This violates the condition on outputs that they should be complements of each other and hence is an 'invalid' condition as indicated in the first row of the function table. When $P'_r = 0$ and $C'_r = 1$, the output of $G1$ will be high and that of $G2$ will be low irrespective of other inputs and clock. This preset condition is indicated in the second row of the function table. When $P'_r = 1$ and $C'_r = 0$, the output of $G1$ will be low and that of $G2$ will be high irrespective of other inputs and clock. This clear condition is indicated in the third row of the function table. For normal working of the circuit, both these control inputs should be inactive, i.e. $P'_r = C'_r = 1$.



(a) Using NAND gates (b) Logic symbol (c) Race-around problem

Fig. 7.37 *JK* flip-flop

The working of this *JK*-FF can be understood by using its function table shown in Table 7.18. As indicated in the truth table, using P'_r and C'_r inputs, the circuit output is initially pre-defined. Let initially $Q = 0$ and $Q = 1$ by making $C'_r = 0$; in normal working conditions $P'_r = C'_r = 1$ and with $CLK = 0$, the output of $G3$ and $G4$ will be high, forcing the latch ($G1$ and $G2$) output to remain unchanged.

Case 1

$J = 0 = K$ and $CLK = 1$

Under this condition, output of $G3$ is at logical-1 (because $J = 0$) and output of $G4$ is 1 (because $K = 0$ and $Q = 0$ is fed back to $G4$). Hence, the final output remains unchanged; this is indicated in fifth row of the function table.

Table 7.18 JK-FF truth table

P'_r	C'_r	CLK	J	K	Q_{n+1}	Q'_{n+1}	Remarks
0	0	×	×	×	1	1	Invalid
0	1	×	×	×	1	0	Preset
1	0	×	×	×	0	1	clear
1	1	0	×	×	0	1	No change
1	1	1	0	0	0	1	No change
1	1	1	0	1	0	1	Reset
1	1	1	1	0	1	0	Set
1	1	1	1	1	0/1	1/0	Race around

Case 2

$J = 0$, $K = 1$ and $CLK = 1$

Under this condition, output of $G3$ is at logical-1 (because $J = 0$) and output of $G4$ is 1 (because $Q_n = 0$). Hence, the final output is still in **reset** condition. Also, even if the $Q_n = 1$, the output will be reset after the application of clock pulse. This is indicated in the sixth row of the function table.

Case 3

$J = 1$, $K = 0$ and $CLK = 1$

Under this condition, output of $G4$ is 1(because $K = 0$ and also $Q = 0$ is fed back to $G4$). However, $G3$ inputs are $J = 1$, $Ck = 1$ and $Q' = 1$ (feedback from $G2$) and hence, output of $G3$ is 0 forcing the true output of $G1$ Q_{n+1} to logical-1. This $Q_{n+1} = 1$ and output of $G4$ also at logical-1 form the input to $G2$ and force $Q' = 0$. Hence, with $J = 1$ and $K = 0$, $Q_{n+1} = 1$ and $Q'_{n+1} = 0$, the flip-flop will be **set**. Also, even if the $Q_n = 1$, the output will be set after the application of clock pulse and this is indicated in the seventh row of the function table.

Case 4

$J = K = 1$ and $CLK = 1$

Under this condition, the inputs to $G3$ are $J = 1$, $CLK = 1$ and $Q'_n = 1$; hence, its output is at logical-0: the inputs to $G4$ are $K = 1$, $Ck = 1$ and $Q_n = 0$; hence, its output is logical-0. This forces output of $G2$ to logical-1 (Q'_{n+1}) and hence output of $G1$ will be a logical-1. Thus output changes from logical-0 to logical-1. Now, if Ck is still high, because of immediate feedback, outputs of $G3$ and $G4$ will change to logical-1 and logical-0 respectively: forcing the final output of $G1$ to logical-0 and that of $G2$ to logical-1. Hence, again outputs change: Q_{n+1} changes continuously as long as the clock pulse is high and thus, because of immediate feedback, output keeps on changing between high and low states. This is known as '**race around condition**' and is clearly indicated in Fig. 7.37(c). At the end of CLK pulse period, the output cannot be predicted precisely.

The race-around problem can be eliminated by

1. narrowing t_p, the clock pulse period to less than the propagation delay t_{pd} of the flip-flop. But, normally t_{pd} will be of a few nanoseconds and designing such a clock pulse is very difficult and the circuit is then expected to work at very high speeds.
2. converting JK into a master-slave arrangement (JK-MS) and hence delaying the feedback signal beyond the clock duration t_p.
3. making the FF sensitive only to the edges of the clock pulse (using edge triggering).

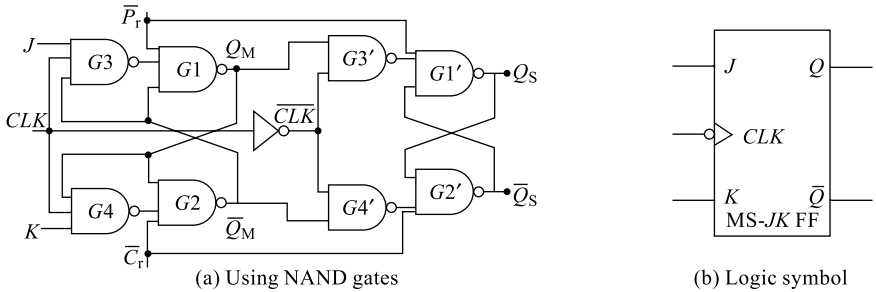


Fig. 7.38 MS *JK* flip-flop

In an MS-*JK* flip-flop, the outputs are not immediately connected to input: instead one more stage called 'slave' is added to delay the feedback. Also, the slave stage will be active only when $CLK = 0$ or the master stage is inactive and hence race-around problem will be eliminated. The arrangement of a Master-Slave *JK* (MS-*JK*) flip-flop is shown in Fig. 7.38.

7.12.4 *JK* Master-Slave Flip-Flop

An MS-*JK* flip-flop can be considered as a combination of a *JK* flip-flop and a clocked *SR* flip-flop. Here, *G*3 and *G*4 receive the feedback after another stage delay (slave stage). P'_r and C'_r are asynchronous inputs, which control the output irrespective of clock, and *J* and *K*.

The working of this MS *JK*-FF can be understood by using its function table shown in Table 7.19. As indicated in the truth table, using P'_r and C'_r inputs, the circuit output is initially pre-defined. Let initially $Q = 0$ and $Q = 1$ by making $C'_r = 0$. In normal working conditions $P'_r = C'_r = 1$ and with $Ck = 0$, output of *G*3 and *G*4 will be high forcing the latch (*G*1 and *G*2) output to remain unchanged. Q_M and Q'_M are the outputs of master stage and Q_S and Q'_S are the outputs of the slave stage and are the final outputs. With $Ck = 0$, outputs of *G*3 and *G*4 will be at logical-1 and hence Q_M and Q'_M remain unchanged, thus the final output Q_S and Q'_S is unchanged. In order to change the outputs, the clock signal should be changed to logical-1. Let initially the outputs be $Q_S = 0$ and $Q'_S = 1$. This is done by making $C'_r = 0$.

Table 7.19 MS-*JK* FF truth table

P'_r	C'_r	*CLK*	*J*	*K*	Q_{n+1}	Q'_{n+1}	Remarks
0	0	×	×	×	1	1	Invalid
0	1	×	×	×	1	0	Preset
1	0	×	×	×	0	1	Clear
1	1	0	×	×	0	1	No change
1	1	1	0	0	0	1	No change
1	1	1	0	1	0	1	Reset
1	1	1	1	0	1	0	Set
1	1	1	1	1	0/1	1/0	Toggle

Case 1

$J = 0 = K$ and $CLK = 1$

Under this condition, the output of $G3$ is at logical-1 and output of $G4$ is also at logical-1. Hence, outputs of master stage Q_M and Q'_M remain unchanged. When CLK changes from 0 to1, CLK' changes from 1 to 0: with $CLK = 1$, the final output remains in its previous state only. This is indicated in the fifth row of the function table.

Case 2

$J = 0$, $K = 1$ and $CLK = 1$

Under this condition, the output of $G3$ is at logical-1 and output of $G4$ is also at logical-1. Hence, outputs of master stage Q_M and Q'_M remain unchanged. When CLK changes from 0 to1, CLK' changes from 1 to 0: with $CLK = 1$, the final output remains in its previous state only. Even if the previous output is at logical-1 then the output of $G4$ will be at logical-0, forcing $Q_M = 0$ and $Q'_M = 1$. When $CLK = 0$, these values on Q_M and Q'_M are propagated to output of $G3'$ and $G4'$ as 1 and 0 respectively and hence final output $Q_S = 0$ and $Q'_S = 1$. This is the RESET condition and is indicated in the sixth row of the function table.

Case 3

$J = 1$ and $K = 0$ with $CLK = 1$

Under this condition, output of $G3$ is at logical-0 and output of $G4$ is at logical-1. Hence, outputs of master stage Q_M and Q'_M will be 1 and 0 respectively. When CLK changes from 0 to 1, CLK' changes from 1 to 0: with $CLK = 1$, the final output remains in its previous state only. When the clock changes to 0, the CLK' changes to 1 and now these values of Q_M and Q'_M are propagated to the output of $G3'$ and $G4'$ as 0 and 1 respectively. This in turn changes the final output $Q_S = 1$ and $Q'_S = 0$. This is the SET condition and is indicated in the seventh row of the function table.

Case 4

$J = 1 = k$ with $CLK = 1$

Under this condition, unlike in the case of *JK*-FF, here output changes only once at every clock falling edge. This is because, we know that in a *JK*-FF, with $J = 1 = K$ output toggles, but since slave is inactive as long as master is active, there will be no change in feedback, hence no racing problem. But once CLK goes low, CLK' goes high changing the final output. Hence, the output toggles. This is indicated in the eighth row of the function table.

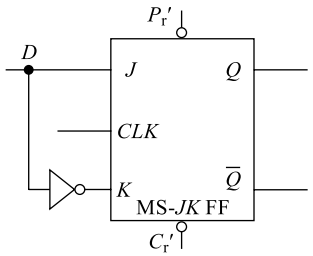
MS-*JK* FF is the ideal flip-flop that can be used widely for all our digital system designs. For convenience, the function table can be presented in the simplified form as shown in Table 7.20. Looking at the middle two rows, it is clear that for $K = J'$, the input on J terminal is transferred as data input

Table 7.20 MS-*JK* FF simplified truth table

J	K	Q_{n+1}	Q'_{n+1}	Remarks
0	0	Q_n	Q'_n	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	Q'_n	Q_n	Toggle

with one clock pulse delay and this results in an application called *D*-FF that can be used to store an information bit. Similarly, looking at the last row, it is clear that for $J = K = 1$, the output changes for every clock pulse applied resulting in another application called a *T*-FF that can be used to construct counters. These two applications of FFs are discussed in sections 7.12.5 and 7.12.6.

7.12.5 *D* Flip-Flop



(a) D flip-flop

CLK	*D*	Q_{n+1}	Q'_{n+1}	Remarks
0	0	Q_n	Q'_n	No change
1	0	0	0	D
1	1	1	1	D

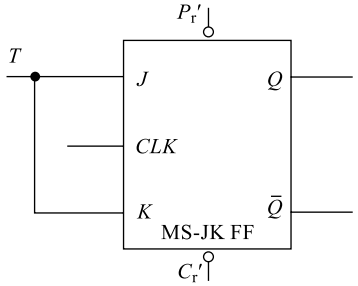
(b) Truth table

Fig. 7.39 *D* flip-flop using MS-*JK* flip-flop

A *D* flip-flop can be realised by modifying an MS-*JK* FF: it can also be realised by modifying a clocked *RS* flip-flop. The *D*-FF obtained by modifying an MS-*JK* FF is shown in Fig. 7.39(a) and its function table in Fig. 7.39(b). The *D* input goes directly to the *J* input and its complement is applied to the *K* input. The asynchronous inputs P'_r and C'_r are to pre-define the output as already discussed in Section 7.12.3. When the clock pulse is 0, the outputs of *D*-FF are at their previous values (Q_n and Q'_n) regardless of the *D* input: this is indicated in first row of the function table. If the *D* input is 0 and the clock pulse is applied, the true output of *D*-FF changes to 0, switching the flip-flop to the reset state; this is indicated in the second row of the function table. Similarly, if the *D* input is 1 and the clock pulse is applied, the true output of *D*-FF changes to 1, switching the flip-flop to the set state; this is indicated in third row of the function table. Because of its ability to transfer 'data' into a flip-flop and deliver it with one clock pulse delay, it receives the name data/delay flip-flop. *D*-FFs are employed in constructing registers and memory units because each *D*-FF can store one bit of binary information.

7.12.6 *T*-Flip-Flop

A *T* flip-flop can be realised by modifying a MS-*JK FF*: it can also be realised by modifying a clocked *RS* flip-flop. The *T*-FF obtained by modifying a MS-*JK* FF is shown in Fig. 7.40(a) and its function table in Fig. 7.40(b). The *T* input goes directly to the *J* input and *K* input. The asynchronous inputs P'_r and C'_r are to pre-define the output as already discussed in Section 7.12.3. When the clock pulse is 0, the outputs of the *T*-FF are at their previous values (Q_n and Q'_n) regardless of the *T* input; this is indicated in first row of the function table. If the *T* input is 0 and the clock pulse is applied, again the outputs of *T*-FF remain unchanged; this is indicated in the second row of the function table. *B*ut, if the *T* input is 1 and the clock pulse is applied then the true output of *T*-FF changes to Q'_n, and the complement output changes to Q_n resulting in the flip-flop toggling; this is indicated in the third row of the function table. Because of its ability to toggle the output of the flip-flop, it receives the name *T* flip-flop. *T*-FFs are employed in constructing counters and timers, because each *T*-FF can count to a base of two (mod-2 counter).



(a) *T* flip-flop

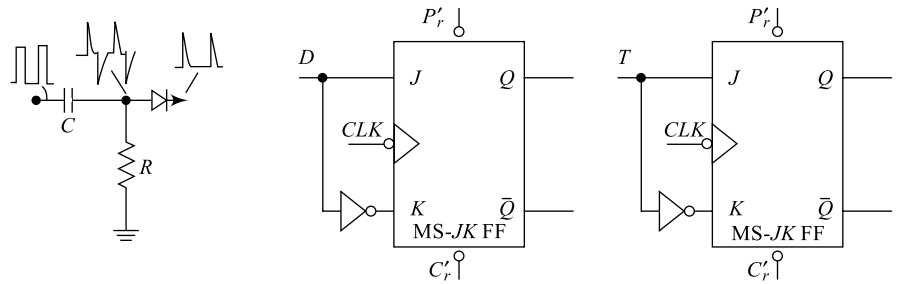
CLK	*T*	Q_{n+1}	Q'_{n+1}	Remarks
0	0	Q_n	Q'_n	No Change
1	0	Q_n	Q'_n	No Change
1	0	Q'_n	Q_n	No Change

(b) Truth table

Fig. 7.40 *T* flip-flop using MS-*JK* flip-flop

7.12.7 Edge-triggered Flip-Flops

In order to solve the problems such as race-around in a *JK-FF*, the FFs can be converted into edge-triggered flip-flops and are basically sensitive to edges of the clock pulses. On a number of occasions, it is very difficult to design narrow clock pulses. Under such circumstances, the clock pulse can be converted into only edges using a simple *RC* differentiator circuit. Figure 7.41 contains various edge-triggered FFs; the working of these circuits is exactly similar to the conventional FFs except that these circuits change their outputs at either the rising (leading) edge of the clock or the falling (trailing) edge of the clock. Accordingly, the logic symbols of these circuits will change.



(a) *RC* network for clock edges (b) *D* flip-flop (c) *T* flip-flop

Fig. 7.41 Edge-triggered flip-flops

Example 7.31

Draw the timing waveforms for the function table of *SR* latch shown in Fig. 7.32.

Solution The timing waveforms for *SR* latch are drawn as per the function table given in Fig. 7.35(a). It is clear from the waveforms given in Fig. 7.42 that when $S = 1$ and $R = 0$, the latch output becomes 1. When $S = 0$ and $R = 1$, the latch output becomes 0. When $S = 1$ and $R = 1$, the latch output remains unchanged and when $S = 0$ and $R = 0$, both the latch outputs become 1 (invalid condition).

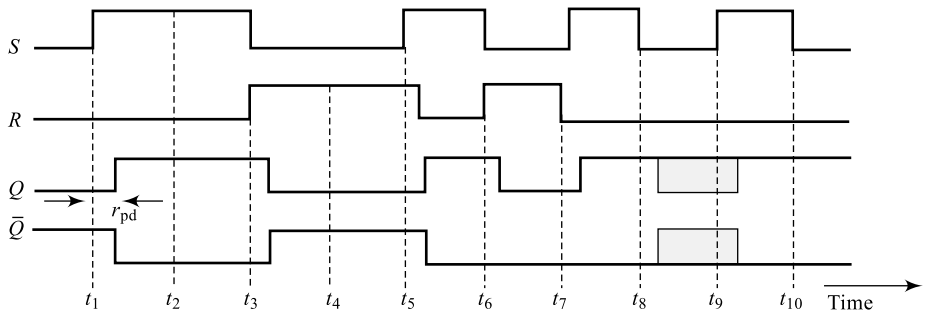


Fig. 7.42 Timing waveforms of an *SR* latch

Example 7.32

Draw the timing waveforms for the function table of a *D* flip-flop shown in Fig. 7.39.

Solution The timing waveforms for a *D*-latch are drawn as per the function table given in Fig. 7.39(b). It is clear from the waveforms given in Fig. 7.43 that when $C = 0$, the output remains unchanged irrespective of *D* input. With $CLK = 1$, when $D = 1$, the latch output becomes 1; when $D = 0$, the latch output becomes 0.

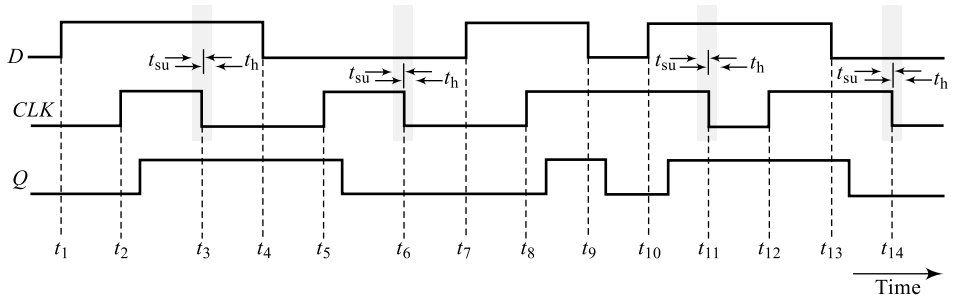


Fig. 7.43 Timing waveforms of a *D*-flip-flop

7.13 COUNTERS

A counter is a logic circuit that is used to count the sequence of operations. Normally, a *T*-FF is the basic building block of a counter. A counter is one of the most useful and versatile subsystems in a digital system. A counter driven by a clock can be used to count the number of external events. Since the clock pulses occur at known intervals of time, a counter can be used as an instrument for measuring time and, therefore, period or frequency. Based on the way the clock pulses are connected to individual *T*-FF, counters can be classified into two types: asynchronous or ripple counters and synchronous counters. A basic *T*-FF can count two clock pulses and each clock pulse applied drives this *T*-FF through two different stages '0' and '1': these stages or states through which a counter passes is called **modulus** (**Mod**) of a counter. The modulus of a counter *M* is related to the number of FFs *N* in the counter through the relation

$$M = 2^N \tag{7.30}$$

7.13.1 Asynchronous Counters

In an asynchronous counter, the clock-pulse source is connected to the first stage only, while each stage output *Q* serves as the clock input signal to its next stage and all the stages do not change states in exact synchronisation with the main clock pulse. It is also commonly referred to as a **ripple counter** and the logic diagram of a 3-bit asynchronous counter is shown in Fig. 7.44. The arrangement consists of three cascaded *JK* FFs (in *T*-FF form): the clock pulse input is connected to FF-1, its output 'A' changes for every **one clock pulse** and is therefore referred as Least Significant Bit (LSB) output. Output 'A' forms the clock input to FF-2 whose output '*B*' changes for every **two clock pulses**. Similarly, output '*B*' is connected as clock input to FF-3 and its output changes for every **four clock pulses**. The asynchronous input *Cr*′ from each FF is used to reset (*ABC* = 000) the counter. The FFs are assumed to be negative edge-triggered which means the output of the FF changes only when its clock input falls from 1 to 0.

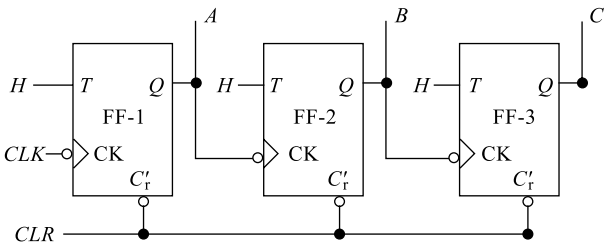


Fig. 7.44 *A* 3-bit asynchronous counter

Figure 7.45 is a 3-bit asynchronous counter using a commercially available *JK FF* IC: (circuits of Fig. 7.45 and 7.46 can be used in the laboratory to verify the counter working). Initially, let the counter be reset using the clear terminal available; hence, the counter output *ABC* = 000. With the first clock pulse, the output of FF-1 changes to 1 at the trailing clock edge, this being the clock input to FF-2, its output and FF-3 output will not change; the counter reads *ABC* = 001. With the second clock pulse, again the output of FF-1 changes to 0 at the trailing clock edge, this being the clock input to FF-2,

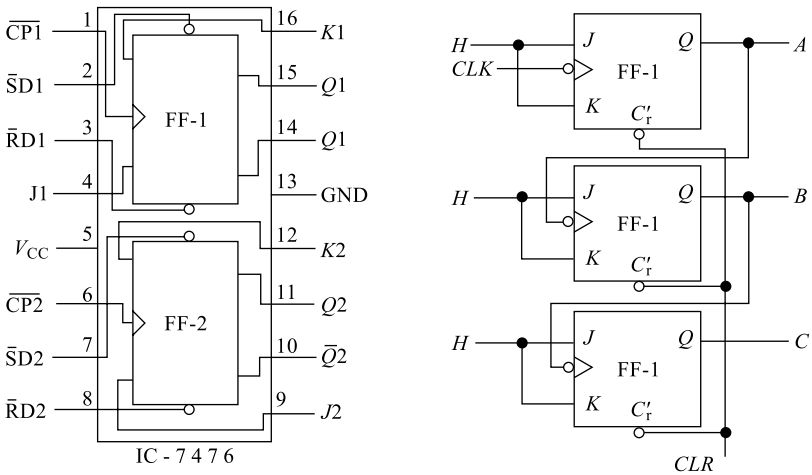


Fig. 7.45 A 3-bit asynchronous counter using *JK* FF

its output changes to 1 and FF-3 output will not change; the counter reads $ABC = 010$. This continues for each clock pulse till seventh clock pulse where counter reads $ABC = 111$. With the eighth clock pulse, the output of FF-1 changes to 0 at the trailing clock edge, this being the clock input to FF-2, its output also changes to 0 and FF-3 output will also change to 0 because of falling clock edge; the counter reads $ABC = 000$.

The working of a 3-bit ripple counter is illustrated through a function table given in Table 7.21 and the corresponding timing waveforms are shown in Fig. 7.46. The clock pulse column C_P represents the falling or trailing edge and the FFs are negative edge sensitive.

Table 7.21 Truth table of a 3-bit asynchronous counter

C_P	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

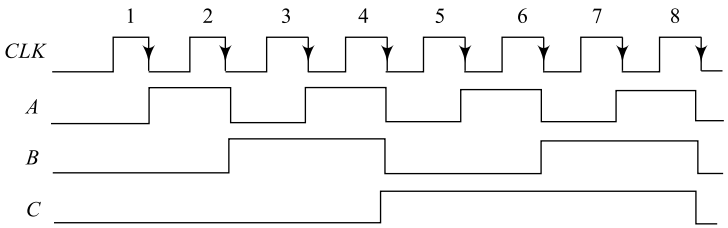
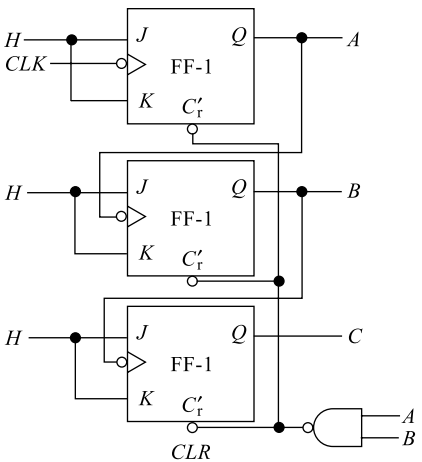


Fig. 7.46 Timing waveforms for a 3-bit counter

Example 7.33

Draw the circuit of a Mod-7 counter using *T*-FFs and prepare its function table.

Solution The circuit of a Mod-7 counter using *T*-FFs and its function table are shown in Fig. 7.47.



(a) Logic diagram

C_p	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	0	0	0

(b) Function Table

Fig. 7.47 Mod-7 counter using *JK* (T) FF

Up/Down Counter

The circuit diagram for 3-bit asynchronous up/down counter using *JK* FFs (IC-7476), AND gates (IC-7408) and OR gates (IC-7432) is shown in Fig. 7.48; the *J* and *K* inputs from all FFs are tied to logic HIGH (*T*-mode). The asynchronous inputs P_r' are all connected together to form the master preset terminal that is used to set the counter outputs. Similarly, other asynchronous inputs C_r'' are all connected together to form the master clear terminal that is used to reset the counter outputs. The main clock source is connected to the first FF and all other FFs get their clock input from the previous stage output through AND-OR gate arrangements. For up counting, the true output is connected and for down counting, the complemented output is connected as clock to next stage.

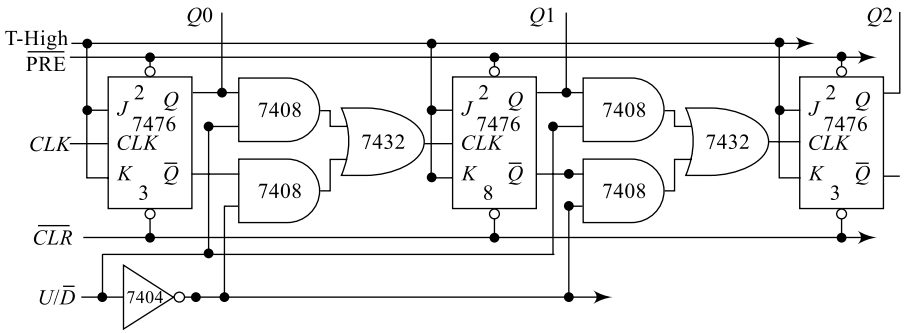


Fig. 7.48 A 3-bit asynchronous up/down counter

The working of the circuit is similar to the circuit of Fig. 7.45 and the function table is given in Table 7.22. The control input U/D' decides the counting direction: if $U/D' = 1$, the upper AND gate is enabled and applies Q as clock input to next stage; the counter works as an up-counter. If $U/D' = 0$, the lower AND gate is enabled and applies Q' as clock input to next stage; the counter works as a down-counter. Figure 7.49 represents timing waveforms for the circuit when $U/D' = 1$, the up-counter. It can be observed here that the circuit responds to leading clock edges. When the circuit control when $U/D' = 0$, the down-counter, the waveforms can be drawn in a way similar to Fig. 7.49.

Table 7.22 Truth Table of a 3-bit asynchronous counter

	$U/D' = 1$			$U/D' = 0$		
CLK	***Q2***	***Q1***	***Q0***	***Q2***	***Q1***	***Q0***
—	0	0	0	0	0	0
1	0	0	1	1	1	1
2	0	1	0	1	1	0
3	0	1	1	1	0	1
4	1	0	0	1	0	0
5	1	0	1	0	1	1
6	1	1	0	0	1	0
7	1	1	1	0	0	1
8	0	0	0	0	0	0

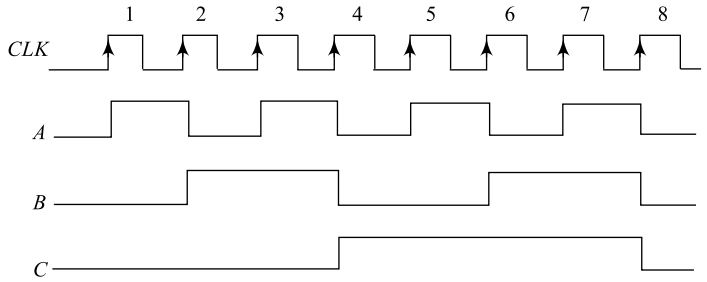


Fig. 7.49 Timing waveforms for a 3-bit up-counter

7.13.2 Synchronous Counters

In a synchronous counter, a common clock pulse source is connected to all stages of FFs in the counter and each stage inputs *J* and *K* are separately controlled. The logic diagram of a 3-bit synchronous counter is shown in Fig. 7.50. The arrangement consists of three cascaded *JK* FFs: the clock pulse input is connected to FF-1, its output '*A*' changes for every **one clock pulse** and is, therefore, referred as Least Significant Bit (LSB) output. Output '*A*' forms the clock input to FF-2 whose output '*B*' changes for every **two clock pulses**. Similarly, previous outputs *A* and *B* are ANDed together to supply clock input to FF-3 and its output changes for every **four clock pulses**. The asynchronous input C_r' from each FF is used to reset (*ABC* = 000) the counter. The FFs are assumed to be negative edge-triggered which means the output of the FF changes only when its clock input falls from 1 to 0. In this type of counter, since all the stages are triggered simultaneously (in parallel) by the clock input pulses, this counter is also called **parallel counter**.

The working of the circuit is similar to the circuit of Fig. 7.45 except that each FF receives the same clock pulse and the function table is same as given in Table 7.21.

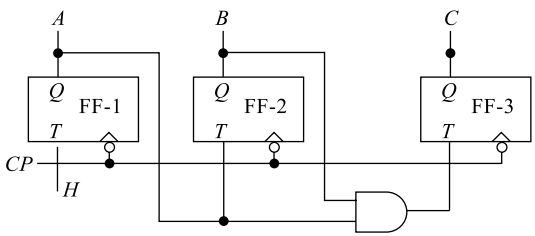


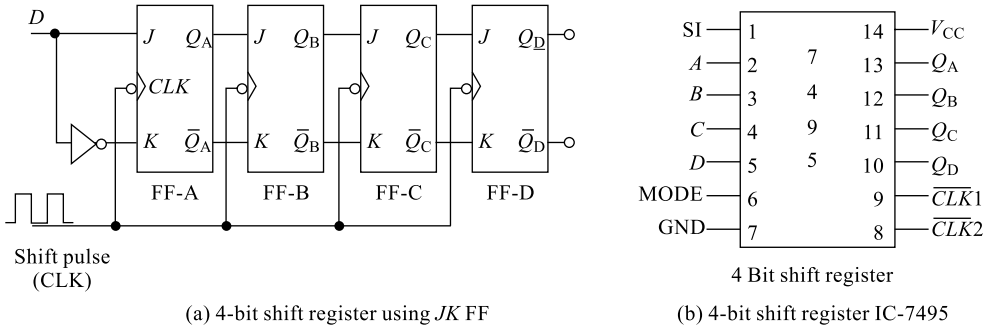
Fig. 7.50 A 3-bit synchronous counter

7.14 SHIFT REGISTERS

A register is a group of flip-flops arranged so that the binary numbers stored in the flip-flop are shifted from one flip-flop to the next for every clock pulse. Figure 7.51(a) shows a 4-bit shift register using *JK* flip-flops working as *D*-FF. The flip-flops are arranged such that the output of FF-A is transferred into FF-*B*, the output of FF-*B* is transferred into FF-C and the output of FF-C is transferred into FF-D when a clock pulse is applied. There are a number of commercial shift registers available and IC-7495 is one of them. It is a 4-bit shift register with facilities for right shift, serial shift, parallel shift, etc. The left shift can also be implemented with external connections. The pin diagram of the IC-7495 shift register is shown in Fig. 7.51(b): it is a 14-pin IC with a mode-selection option for serial and parallel operations. With MODE = 0 (Pin 6), the serial mode is selected and the string of data on the serial input pin SI (Pin 1) is entered into the register with the application of four-clock pulses on *CLK*1 (Pin 9). Similarly, with MODE = 1 (Pin 6), the parallel mode is selected and the string of data on the parallel serial input pins *A*, *B*, *C*, and *D* (Pins 2 to 5) is entered into the register with the application of a falling edge on *CLK*2

(Pin 8). Parallel outputs are available on Q_A, Q_B, Q_C and Q_D (Pins 10 to 13), the serial output on Q_D (Pin 10) and the IC operates on +5 V supply.

7.14.1 Basic Operations



(a) 4-bit shift register using *JK* FF

(b) 4-bit shift register IC-7495

Fig. 7.51 A 4-bit shift register

There are four basic types of operations that can be performed using a shift register depending on the manner in which data is entered into and retrieved out of the register. They are

1. Serial-In-Serial-Out (SISO) operation
2. Serial-In-Parallel-Out (SIPO) operation
3. Parallel-In-Serial-out (PISO) operation
4. Parallel-In-Parallel-out (PIPO) operation

1. Serial-In-Serial-Out (SISO) and Serial-In-Parallel-Out (SIPO)

In order to enter a stream of data serially into the register (IC-7495) and later retrieving it either serially or parallelly, the following procedure may be followed:

(a) Serial-In-Parallel-Out: [SIPO]

(i) The circuit is rigged up using IC-7495.
(ii) Serial mode selection is made with MODE = 0.
(iii) Serial data is applied at the serial input pin SI (Pin 1).
(iv) Four clock pulses are applied to *CLK*1 (Pin 9), data enters in serially.
(v) Now, parallel data output is available on pins 10 to 13.

(b) Serial-In-Serial-Out: [SISO]

(i) Serial mode selection is made with MODE = 0.
(ii) Serial data is applied at the serial input pin SI (Pin 1).
(iii) Four clock pulses are applied to *CLK*1 (Pin 9), data enters in serially.
(iv) For the next four clock pulses, the data output is shifted at Q_D pin in serial fashion.

The procedure given above is depicted with a sample data in the form of a function table in Table 7.23.

Table 7.23 Truth table of a 4-bit in SISO and SIPO modes

Clock Pluse	Serial Data Input	Out puts			
		Q_A	Q_B	Q_C	Q_D
0	1	×	×	×	×
1	0	1	×	×	×
2	1	0	1	×	×
3	0	1	0	1	×
4	×	0	1	0	1
5	×	×	0	1	0
6	×	×	×	0	1
7	×	×	×	×	0

Parallel data output after 4th clock pluse

Serial data out put observed during 4th, 5th, 6th, 7th clockpulse

2. Parallel-In-Serial-Out (PISO) and Parallel-In-Parallel-Out (PIPO)

In order to enter a stream of data parallelly into the register (IC-7495) and later retrieving it either serially or parallelly, the following procedure may be followed:

(c) Parallel-In-Parallel-Out: [PIPO]

(i) The circuit is rigged up using IC-7495.
(ii) Parallel mode selection is made with MODE = 1.
(iii) Parallel data is applied at the parallel input pins *A*, *B*, *C* and *D* (Pins 2 to 5).
(iv) A falling edge on *CLK*2 (Pin 8), enters data in parallel.
(v) Now, parallel data output is available on pins 10 to 13.

(d) Parallel-In-Serial-Out: [PISO]

(i) Parallel mode selection is made with MODE = 1.
(ii) Parallel data is applied at the parallel input pins *A*, *B*, *C* and *D* (Pins 2 to 5).
(iii) A falling edge on *CLK*2 (Pin 8), enters data in parallel.
(iv) Serial mode selection is made with MODE = 0.
(v) For the next four clock pulses, the data output is shifted at Q_D pin in serial fashion.

The procedure given above is depicted with a sample data in the form of a function table in Table 7.24. A bi-directional shift register can also be constructed using I*C*-7495 and in this case the data can be shifted to either left or right.

3. Shift Register Counters

A shift register counter is basically a shift register with the serial output connected back to the serial input through a decoder in order to produce special sequences which are very useful in many communication applications. These circuits are often classified as counters because they exhibit a specified sequence of states.

7.14.2 Ring Counter

A ring counter is constructed using a serial shift register and in this case, the final serial output Q_D is feedback to the serial input line SI directly without any decoder. The circuit arrangement for a 4-bit ring

Table 7.24 Truth table of a 4-bit shift register in PISO and PIPO modes

Clock Pulse	Mode	Clock Input To	Out Puts			
			QA	QB	QC	QD
0	1	Clock 2	×	×	×	×
1			1	0	1	0
2	0	Clock 1	×	1	0	1
3			×	×	1	0
4			×	×	×	1
5			×	×	×	×

Parallel data output after 1st clock pulse

Serial data outputs observed during 1st, 2nd, 3rd, & 4th clock pulses

counter is shown in Fig. 7.52 and is operated in serial mode. Initially, let the contents in the counter be $Q_A\ Q_B\ Q_C\ Q_D = 1\ 0\ 0\ 0$ (loaded either in serial or parallel fashion). The Q_D output from the last stage is connected to the serial input SI (Pin 1) of the first stage.

In order to realise a ring counter using IC-7495, the following procedure can be followed:

(i) The circuit is rigged up using IC-7495 as in Fig. 7.52.
(ii) Parallel mode selection is made with MODE = 1.
(iii) Parallel data is applied at the parallel input pins *A*, *B*, *C* and *D* (Pins 2 to 5).
(iv) A falling edge on *CLK*2 (Pin 8), enters data in parallel.
(v) The mode control *M* = 0 and clock is given to clock 1 (Pin 9).
(vi) The clock pulses are applied to *CLK*1 and the output is observed as in Table 7.25.

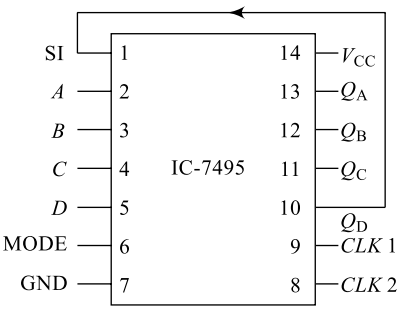


Fig. 7.52 Ring counter using IC-7495

Table 7.25 Truth table of a 4-bit ring counter

Ck	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

7.14.3 Johnson Counter or Twisted Ring Counter

In a Johnson counter (also called **Moebi counter**), the complement of the output of the last flip-flop is connected back to the serial input of the IC-7495. The feedback arrangement produces a unique sequence of states. Four-bit sequence has a total of eight states. In general an *n*-stage Johnson counter will produce a module of 2*n*, where *n* is the number of stages connected to the *D* input of each stage. The single exception is that the Q^- output of the last stage is connecting back to the *D* input of the first stage. One advantage of this type of sequence is that it is readily decoded with two-input AND gate.

In order to realise a twisted ring counter using IC-7495, the following procedure can be followed:

(i) The circuit is rigged up using IC-7495 as in Fig. 7.53.
(ii) Parallel mode selection is made with MODE = 1.
(iii) Parallel data is applied at the parallel input pins *A*, *B*, *C* and *D* (Pins 2 to 5).
(iv) A falling edge on *CLK*2 (Pin 8), enters data in parallel.
(v) The mode control *M* = 0 and clock is given to clock-1 (Pin 9).
(vi) The clock pulses are applied to *CLK*1 and the output is observed as in Table 7.26.

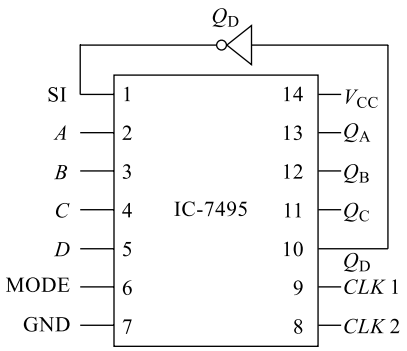


Fig. 7.53 Twisted ring (Johnson) counter using IC-7495

Table 7.26 Truth table of a 4-bit twisted ring counter

CLK	Q_0	Q_1	Q_2	Q_3
0	0	0	0	1
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1

Summary

- An analog signal has time-varying amplitude, but a digital signal has only two representations: logic-HIGH and logic-LOW.
- Digital computers are used to process digital signals. Hence, digital processing is fast and accurate. Analog processing is more reliable.
- A binary number system is one of the convenient methods for representing, processing and controlling a digital system.
- Octal and hexadecimal number systems are the other methods available for conveniently representing, processing and controlling a digital system.
- Sign magnitude representation has separate representation for positive zero and negative zero.
- Sign 1's complement representation also has separate representation for positive zero and negative zero. This representation can be conveniently used to perform binary arithmetic.
- Sign 2's complement representation has only one representation for both positive zero and negative zero. This representation can be conveniently used to perform binary arithmetic.
- Sign 2's complement representation has one extra representation on the negative side and is the most preferred representations in modern-day computing.
- Hexadecimal number system is used in modern-day computing to represent addresses, data, control, etc.
- Conversion from one number system to another provides a convenient way to use different forms of data for processing.
- A binary parallel adder can be used for both addition and subtraction (a parallel adder is the basic building block for an Arithmetic Logic Unit-ALU).

- ➢ AND, OR and NOT gates are the basic logic gates. Using these functions, any digital system can be realised logically (including EX-OR function).
- ➢ NAND gate and NOR gate are the universal gates. Using these functions, any other basic function or any digital system can be realised logically (including EX-OR function).
- ➢ Simplifying any digital system and then implementing simplified expression results in a considerable amount of hardware reduction.
- ➢ Boolean postulates and De Morgan's theorems are helpful in simplifying a digital switching function.
- ➢ A K-map is another tool for simplification of switching functions; it is a graphical representation and simplification can be done in SOP or POS forms.
- ➢ The output of a combinational circuit depends only on the present input; not on the previous output, hence there is no memory in a combinational circuit.
- ➢ The output of a sequential circuit depends not only on the present input, but also on the previous output, hence there is a memory in a sequential circuit.
- ➢ The arithmetic circuits such as adders and subtractors are combinational circuits.
- ➢ Latches and flip-flops are some examples of sequential circuits and these are mainly used to store binary information.
- ➢ An *SR* FF is simple to construct, but it has a disadvantage of an invalid output when both inputs are at high.
- ➢ A *JK*-FF overcomes the problem of *SR*-FF, but has a disadvantage of a racing output when both input are at high.
- ➢ An MS-*JK* FF overcomes the problem of *SR*-FF and *JK*-FF and offers an advantage of toggle output when both inputs are at high.
- ➢ An MS-*JK* FF can be modified into a *D*-FF that can be used to construct registers.
- ➢ An MS-*JK* FF can be modified into a *T*-FF that can be used to construct counters.
- ➢ Modulus of a counter is the number of discrete stages through which the counter progresses; the modulus of a counter *M* is related to the number of FFs *N* in the counter through the relation $M = 2^N$.
- ➢ A shift register is used for applications such as to store binary information, to shift the data in either directions, to convert serial data stream into parallel and vice versa, etc.

Review Questions

1. What do you mean by 'positive logic' and 'negative logic'? Explain
2. Most of the real world requires analog signals, but still digital systems are popular, why?
3. Why are NAND and NOR gates called universal gates?
4. Realise EX-OR function using basic gates.
5. Realise EX-OR function using NAND gates.
6. Realise EX-OR function using NOR gates.
7. Realise EX-NOR function using NAND gates.
8. Realise EX-NOR function using NAND gates.
9. State and prove the 'commutative law' in Boolean algebra.
10. State and prove the 'associative law' in Boolean algebra.
11. State and prove the 'distributive law' in Boolean algebra.
12. State and prove the De Morgan's theorems in Boolean algebra.
13. What are the advantages of 2's complement representation?

14. Show that 2's complementation representation has only one zero representation.
15. What is race-around condition? Explain how it can be eliminated.
16. What is 'Toggle condition'? Explain. What are its advantages?
17. Draw the timing waveforms for *SR* flip-flop.
18. Draw the timing waveforms for *JK* flip-flop
19. Draw the timing waveforms for MS-*JK* flip-flop
20. Draw the timing waveforms for *D*-flip-flop
21. Draw the timing waveforms for *T*-flip-flop
22. Explain SIPO operation in a shift register. How it is useful in serial communication?
23. Explain PISO operation in a shift register. How it is useful in serial communication?
24. What is modulus of a counter? Explain.
25. What is a ripple counter? Explain.
26. Draw the block diagram of a 3-bit ripple counter using *JK*-FF and explain its working with a function table.
27. How many FFs are needed to realise a Mod-125 counter? Explain.
28. Draw a logic circuit for the switching function $f_{(A, B, C, D)} = BD + BE + D'F$
29. Draw a logic circuit for the switching function $f_{(A, B, C)} = A'BC + B'CD + BC'D + ABD'$

Exercise Problems

1. If $43_{10} = X_2$, find the value of X.
2. Convert 111101101110.10111101_2 into its octal equivalent.
3. Convert 3146.52_8 into its binary equivalent.
4. Add 101101_2 and 110101_2 and convert the result into its equivalent decimal value.
5. Convert 47_{10} into an equivalent octal number
6. If $332_{10} = X_8$ then find the value of X.
7. Convert the decimal number 4429.625_{10} into its equivalent octal number.
8. If $632.97_{10} = X_8$, find the value of X.
9. Convert the octal number 15 into its decimal equivalent.
10. Convert octal number 72 into its decimal equivalent.
11. Convert 15.6_8 into its decimal equivalent.
12. Convert 11011110_2 into its octal equivalent.
13. Convert 11011110_2 into its hexadecimal equivalent.
14. Convert 11101_2 plus 111.11_2 into its hexadecimal equivalent.
15. Convert $AA \cdot 1A_{16}$ into its binary equivalent.
16. Convert 15_{16} into its equivalent decimal number.
17. Convert $B8_{16}$ into its equivalent decimal number.
18. If $AB4_{16} = X_{10}$, find the value of X.
19. If $9.1A_{16} = X_{10}$, find the value of X.
20. What is the hexadecimal equivalent of 24_{10}?
21. If $513_{10} = X_{16}$, find the value of X.
22. If $26.21_{10} = X_{16}$, find the value of X.
23. Perform the following conversions:
    (i) 63.25_{10} to equivalent binary
    (ii) 43.8125_{10} to equivalent binary
    (iii) 485_{10} to base-16

24. Perform the following conversions:
    (i) 1001011.011_2 to equivalent decimal
    (ii) 110101.1011_2 to equivalent decimal
    (iii) 11001.1_2 to base-8
25. Perform the following conversions:
    (i) 25.68 to equivalent binary
    (ii) 35.18 to base-16
    (iii) 39.A16 to base-8
26. Perform the following conversions:
    (i) $01010011_2 =$ ____$_8$
    (ii) $2BE_{16} =$ ____ 8
    (iii) $11011.01_2 =$ ____$_8$
    (iv) $1000_{10} =$ ____$_{16}$
    (v) 2's complement of $(1110101)_2$ is _____
27. Simplify the switching function $F_{(ABC)} = A'B'C' + A'B'C + AB'C' + ABC$ using Boolean postulates. Realise the simplified expression using basic gates.
28. Simplify the switching function $F_{(ABC)} = A'B'C' + A'B'C + A'BC + AB'C' + ABC$ using Boolean postulates. Realise the simplified expression using NAND gates.
29. Simplify the switching function $F_{(ABCD)} = A'B'C'D' + A'B'C'D + A'BCD + AB'C'D' + ABCD$ using a K-map and realise the simplified expression using NAND gates.
30. Simplify the switching function $F_{(ABCD)} = A'B'C' + B'C + A'BCD + AC' + ABD$ using a K-map after converting it into canonical SOP form. Realise the simplified expression using NAND gates.
31. Convert the switching function $F_{(ABC)} = A'B' + A'B'C + AB +$ AC into canonical SOP form.
32. Simplify the switching function $F_{(ABCD)} = \Sigma_m$ (0, 1, 4, 8, 9, 12) using a K-map and realise the simplified expression using NAND gates.
33. Simplify the switching function $F_{(ABCD)} = \Sigma_m$ (0, 1, 4, 8, 9, 12) + Σ_d (13, 14, 15) using a K-map and realise the simplified expression using NAND gates.
34. Write the function table for a full adder. Simplify the switching functions for sum and carry using a K-map and realise the simplified expression using EX-OR and AND gates.
35. Write the function table for a full adder. Simplify the switching functions for sum and carry using a K-map and realise the simplified expression using NAND gates.
36. For the circuit shown in Fig. P7.36, write the output expression.

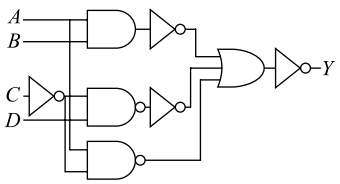


Fig. P7.36

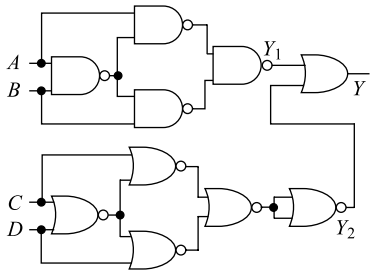


Fig. P7.37

37. For the circuit shown in Fig. P7.37, write the output expressions Y, Y_1 and Y_2.

38. The K-map of a three-variable function F is shown in Fig. P7.38. What is the sum-of-minterms expression of F?

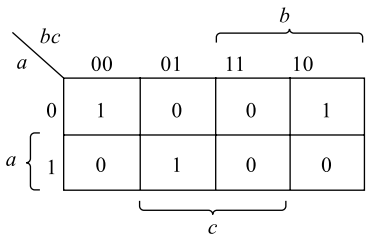


Fig. P7.38

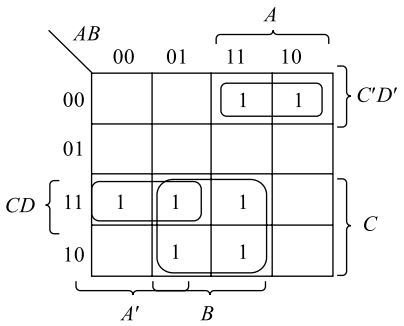


Fig. P7.39

39. For the K-map shown in Fig. P7.39, write the simplified output expression F.
40. Realise the expression obtained in Problem 39 using basic gates.
41. For the K-map shown in Fig. P7.41, write the simplified output expression F.
42. Realise the expression obtained in Problem 41 using basic gates.
43. Simplify the switching function $f(A, B, C, D) = \Sigma_m (2, 3, 4, 5, 7, 8, 10, 13, 15) + \Sigma_d (2, 3, 4)$ using a K-map.
44. Realise the expression obtained in Problem 41 using universal NAND gates.

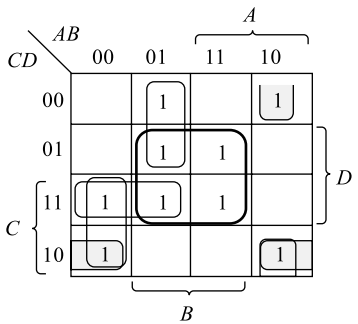
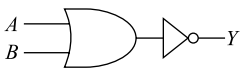


Fig. P7.41

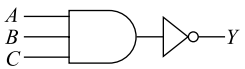
Multiple-Choice Questions

1. The radix of a number system represents
   (a) number of repeated digits in that number system
   (b) number of zeros in that number system
   (c) number of digits in that number system
   (d) none of the above
2. In an analog representation, the signal amplitude is represented as a
   (a) continuous function of time (b) discrete function of time
   (c) both (a) and (b) (d) neither (a) nor (b)
3. In a digital representation, the signal amplitude is represented as a
   (a) continuous function of time (b) discrete function of time
   (c) both (a) and (b) (d) neither (a) nor (b)
4. Conversion of an analog signal into a digital form is done by using a
   (a) digital-to-analog convertor (b) analog-to-digital convertor
   (c) both (a) and (b) (d) neither (a) nor (b)

5. Conversion of a digital signal into an analog form is done by using a
   (a) digital-to-analog convertor (b) analog-to-digital convertor
   (c) both (a) and (b) (d) neither (a) nor (b)
6. Analog systems offer the following advantage/s as compared to digital systems:
   (a) More reliable (b) Less noisy
   (c) Both (a) and (b) (d) Neither (a) nor (b)
7. Digital systems offer the following advantage/s as compared to analog systems:
   (a) Easy processing (b) Easy storage
   (c) Both (a) and (b) (d) Neither (a) nor (b)
8. A decimal number system is characterised by the following:
   (a) Radix of the system is 10 (b) Contains 10 digits for representation
   (c) Neither (a) nor (b) (d) Both (a) and (b)
9. A binary number system is characterised by the following:
   (a) Radix of the system is 2 (b) Contains 2 digits for representation
   (c) Neither (a) nor (b) (d) Both (a) and (b)
10. An octal number system is characterised by the following:
   (a) Radix of the system is 8 (b) Contains 8 digits for representation
   (c) Neither (a) nor (b) (d) Both (a) and (b)
11. A hexadecimal number system is characterised by the following:
   (a) Radix of the system is 16 (b) Contains 16 digits for representation
   (c) Neither (a) nor (b) (d) Both (a) and (b)
12. For a binary number system, the following statement is not correct:
   (a) Radix of the system is 2 (b) Contains 2 digits for representation
   (c) 2 is a valid digit (d) All the above
13. For an octal number system, the following statement is not correct:
   (a) Radix of the system is 8 (b) Contains 7 digits for representation
   (c) 8 is a valid digit (d) All the above
14. For a hexadecimal number system, the following statement is not correct:
   (a) Radix of the system is 16 (b) Contains 16 digits for representation
   (c) 9 is a valid digit (d) None of the above
15. 123_{10} is equal to
   (a) 1111011_2 (b) 173_8 (c) $07b_{16}$ (d) all the above
16. 2468_{10} is equal to
   (a) 1111011_2 (b) 173_8 (c) $09a4_{16}$ (d) all the above
17. What is the output Y if both inputs A and B in the figure below are 0?

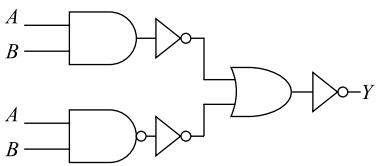


   (a) $Y = 0$ (b) $Y = 1$ (c) Y is unknown (d) None of the above
18. A certain logic gate with two inputs produces a low output only when both inputs are same; then it is
   (a) an EX-OR gate (b) an OR gate (c) a NAND gate (d) an AND gate
19. What is the output Y if input $A = 1$, $B = 0$ and $C = 1$ in the figure below?



   (a) $Y = 0$ (b) $Y = 1$ (c) Y is unknown (d) None of the above

20. In Question 19, what changes in the inputs are needed for the output Y to be '0'?
    (a) Invert all inputs (b) $A = 0, B = 1, C = 0$
    (c) $A = 1, B = 1, C = 1$ (d) No change
21. A certain logic gate with two inputs produces a high output only when both inputs are same; then it is
    (a) an EX-OR gate (b) an OR gate
    (c) an EX-NOR gate (d) an AND gate
22. A certain logic gate with n inputs produces a high output only when odd numbers of inputs are at logic high; then it is
    (a) an EX-OR gate (b) an OR gate (c) an EX-NOR gate (d) an AND gate
23. A certain logic gate with n inputs produces a low output only when odd numbers of inputs are at logic high; then it is
    (a) an EX-OR gate (b) an OR gate (c) an EX-NOR gate (d) an AND gate
24. In the figure shown below if the inputs are both '1', what is the output?



    (a) $Y = 0$ (b) $Y = 1$ (c) Unknown (d) None of the above
25. In Question 24, what are the values of the inputs if output needs to be'1'?
    (a) $A = 0$ and $B = 0$ (b) $A = 0$ and $B = 1$ (c) $A = 1$ and $B = 0$ (d) None of the above
26. A certain logic gate produces an output as in the truth table shown below. What type of logic gate is it?

A	*B*	*C*	*X*
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

    (a) 3-input OR gate (b) 3-input NAND gate
    (c) 3-input NOR gate (d) 3-input AND gate
27. Similar to decimal number system, the binary number system also is/has
    (a) a positional number system (b) basic digits 0 and 1
    (c) a base-2 system (d) all of the above
28. The previous and next numbers of the hexadecimal number $1C00_{16}$ are respectively
    (a) $1B99_{16}$ and $1C01_{16}$ (b) $1BFF_{16}$ and $1C01_{16}$
    (c) $1B00_{16}$ and $1D00_{16}$ (d) $0C00_{16}$ and $1C01_{16}$

29. In the list given below, _____ is not an octal number.
    (a) 1234_8 (b) 5678_8 (c) 4567_8 (d) 1010_8
30. In the list given below, _____ is not an hexadecimal number.
    (a) 1234_{16} (b) 5678_{16} (c) $FFGF_{16}$ (d) $FFFF_{16}$
31. *A* and *B* are two binary numbers and $A > B$. When the operation $(A - B)$ using 1's complement method is done, 1's complement of *B* is added to *A*. In this case,
    (a) carry certainly will be present after addition and it has to be added to the partial result to obtain the true result
    (b) carry will not be present after addition
    (c) carry will be present but it is to be discarded to obtain the true result
    (d) none of the above
32. *A* and *B* are two binary numbers and $A < B$. When the operation $(A - B)$ using 1's complement method is done, 1's complement of (B) is added to (A). In this case,
    (a) carry certainly will be present after partial addition, and it has to be added to the partial added result to obtain the true result
    (b) carry will not be present after addition but the partial added result will be in complement form; L's complement of the partial added result is to be obtained to get the true result
    (c) carry will be present but it is to be discarded to obtain the true result
    (d) none of the above
33. *A* and *B* are two binary numbers and $A > B$. When the operation $(A - B)$ using 2's complement method is done, 1's complement of (B) is added to (A). In this case,
    (a) carry certainly will be present after addition, and it has to added to the partial added result to obtain the true result
    (b) carry will not be present after partial addition
    (c) carry certainly will be but it is to be discarded to obtain the true result
    (d) none of the above
34. *A* and *B* are two binary numbers and $A < B$. When the operation $(A - B)$ using 2's complement method is done, 1's complement of (B) is added to (A). In this case,
    (a) carry certainly will be present after partial addition, and it has to added to the partial result to obtain the true result
    (b) carry will not be present after addition hut the partial added result will be in 2's complement form; 2's complement of the partial added result is to be obtained to get the true result
    (c) carry will be present but it is to he discarded to obtain the true result
    (d) none of the above
35. In sign magnitude representation of a positive and a negative number, the following statement/s is correct:
    (a) MSB bit represents the sign (b) Magnitude bits are same
    (c) Both (a) and (b) (d) Neither (a) nor (b)
36. In sign 1's complement representation of a positive and a negative number, the following statement/s is correct:
    (a) MSB bit represents the sign
    (b) Magnitude bits are complement of each other
    (c) There are two representations for zero
    (d) All the above

37. In sign 2's complement representation of a positive and a negative number, the following statement/s is correct:
    (a) LSB bit represents the sign
    (b) There is only one representation for zero
    (c) Magnitude bits are same
    (d) All the above
38. $123_8 + 45O_8 =$ _____ $_8$
    (a) 567_8 (b) 579_8 (c) 523_8 (d) 573_8
39. $09FF_{16} + 0001_{16} =$ ____ $_{16}$
    (a) 1010_{16} (b) 1110_{16} (c) 1000_{16} (d) $0A00_{16}$
40. $123_8 + 45O_{16} =$ ____ $_8$
    (a) 567_8 (b) 579_8 (c) 573_8 (d) 2243_8
41. $123_8 + 45O_{16} =$ _____ $_{16}$
    (a) 567_{16} (b) 579_{16} (c) 573_{16} (d) $4A3_{16}$
42. Pick the odd one out:
    (a) $EFGA_{16}$ (b) $ABCD_{16}$ (c) 1234_8 (d) 1000_2
43. A logic gate has multiple inputs and one output. The output of this gate is at logic '1'. When one or more inputs are at logic '1' then that gate is _____
    (a) AND gate (b) OR gate (c) NOR gate (d) EX-OR gate
44. A logic gate has multiple inputs and one output. The output of this gate is at logic '1' only when all the inputs are at logic '1'. Then that gate is _____
    (a) AND gate (b) OR gate (c) NOR gate (d) EX-OR gate
45. A logic gate has multiple inputs and one output. The output of this gate is at logic '0' when all the inputs are at logic '1'. Then that gate is called as,
    (a) NAND gate (b) OR gate (c) NOR gate (d) EX-OR gate
46. A logic gate has multiple inputs and one output. The output of this gate is at logic '1' when all the inputs are at logic '0'. Then that gate is called as,
    (a) AND gate (b) OR gate (c) NOR gate (d) EX-OR gate
47. As per De Morgan's theorem,
    (a) $\overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$
    (b) $\overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$
    (c) both (a) and (b)
    (d) Neither (a) nor (b)
48. One of the following Boolean postulates is wrong and that is
    (a) $A + A = A$ (b) $A + A' = A$ (c) $A + A' = 1$ (d) $A * A' = 0$
49. In a K-map simplification, one of the incorrect statements is
    (a) an octet eliminates 3 variables
    (b) A quad eliminates 2 variables
    (c) redundant group appears in final simplified expression
    (d) A pair eliminates 1 variable
50. In a K-map simplification, one of the incorrect statements is
    (a) an octet contains 3-logical adjacent 1s
    (b) a pair contains 2-logical adjacent 1s
    (c) a quad contains 4-logical adjacent 1s
    (d) an octet contains 8-logical adjacent 1s
51. The Boolean expression $A' * A\ [(B + A' + C') + A'BC] =$
    (a) $A + (B + C)$ (b) $A * (B + C)$ (c) 0 (d) A
52. The SUM expression for a half adder represents _____
    (a) AND gate (b) EX-OR gate (c) NAND gate (d) NOR gate
53. The CARRY expression for a half adder represents _____
    (a) NAND gate (b) EX-OR gate (c) AND gate (d) NOR gate

54. The SUM expression for a full adder represents a 3-input _____
(a) AND gate (b) EX-OR gate (c) NAND gate (d) NOR gate

55. Out of the truth tables of a half-adder, only one is correct with A and B as inputs. S is a sum output and C is a carry output. The correct truth table is,

(a)

A	*B*	*S*	*C*
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

(b)

A	*B*	*S*	*C*
0	0	1	0
0	1	0	1
1	0	1	0
1	1	1	1

(c)

A	*B*	*S*	*C*
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

(d)

A	*B*	*S*	*C*
0	0	0	1
0	1	0	0
1	0	1	0
1	1	1	1

56. The full adder can be realised using
(a) only two half adders (b) two half adders and one 'OR' gate
(c) two half adders and one 'AND' gate (d) only two 'EX-OR' gates

57. Out of the truth tables of a full adder, only one is correct. A, B and C_{IN} are inputs, S is a sum output and C_o is a carry output. The correct truth table is

(a)

A	B	C_{IN}	S_O	C_O
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	0	1
1	1	1	1	1

(b)

A	B	C_{IN}	S_O	C_O
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(c)

A	B	C_{IN}	S_O	C_O
0	0	0	1	0
0	0	1	1	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	0	1
1	1	1	1	1

(d)

A	B	C_{IN}	S_O	C_O
0	0	0	0	1
0	0	1	1	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	0	1
1	1	1	1	1

58. A simple *SR* latch can be used as a
    (a) storage element (b) switch de-bouncer
    (c) both (a) and (b) (d) neither (a) nor (b)
59. Race around is the problem existing in a/an
    (a) MS-*JK* flip-flop (b) *JK* flip-flop (c) *SR* flip-flop (d) none of the above
60. A MS-*JK* flip-flop can be modified into a
    (a) a *D* flip-flop (b) a *T* flip-flop (c) both (a) and (b) (d) Neither (a) nor (b)
61. Toggle condition exists in a
    (a) MS-*JK* flip-flop (b) *JK* flip-flop (c) *SR* flip-flop (d) none of the above
62. A register can be constructed using a
    (a) *D* flip-flop (b) *T* flip-flop (c) both (a) and (b) (d) neither (a) nor (b)
63. A counter can be constructed using a
    (a) *D* flip-flops (b) *T* flip-flops (c) both (a) and (b) (d) neither (a) nor (b)
64. A series of *N* cascaded *D* flip-flops can be used to
    (a) store *N*-bit data (b) count *N* states (c) both (a) and (b) (d) neither (a) nor (b)
65. A series of *N* cascaded *T* flip-flops can be used to
    (a) store *N*-bit data (b) count 2^N states (c) both (a) and (b) (d) neither (a) nor (b)

Measuring Instruments

8

Goals and Objectives

After successfully completing the study of this chapter, the reader is expected to

- Understand the importance of signal quantities measurement in electronics
- Understand the basic relationship between voltage, current and power
- Understand the basic differences between ac quantity and dc quantity measurements
- Understand the basic similarities in the construction of ammeter and voltmeter
- Understand the basic working principle of the basic meters such as a PMMC meter
- Understand the effect of signal quantity measurement.
- Understand the principle of a voltmeter, its working and range extension in multirange voltmeter
- Understand the principle of an ammeter, its working and range extension in multirange ammeter
- Understand the principle of a rectifier-type voltmeter
- Understand the need, construction of multimeters, analog multimeters and digital multimeters
- Understand the importance of waveform display in signal measurements
- Understand the construction, working principle and uses of CRO
- Understand the principle of electron-beam formation, its focussing and speeding to display the signals
- Understand the role of time-base generator in displaying the signal on a CRO
- Understand the controls available and their association with the internal block in a CRO
- Understand various applications of CRO such as signal display, amplitude, time, frequency and phase-angle measurements
- Gain knowledge of lissajous-pattern generation, its use in measurement of phase difference and frequency
- Feel confident in using electronic measuring in all display instruments practical applications.

8.1 INTRODUCTION

Measurement of circuit parameters such as current, voltage and power is an important part in any system design. An **ammeter** is used to measure the circuit current. A **voltmeter** is used to measure the voltage and a **wattmeter** is used to measure the power in the circuit. Measurement may involve ac quantity measurement or dc quantity measurement. In order to measure current, an ammeter will be connected in series with the load; similarly, a voltmeter is connected in parallel for voltage measurement. DC power measurement can be done using Eq. (8.1).

$$P_{dc} = I^2R \text{ watts} \quad [8.1(b)]$$

$$= V \cdot I \text{ watts} \quad [8.1(a)]$$

$$= V^2/R \text{ watts} \quad [8.1(c)]$$

The ac power measurement can be done using Eq. (8.2).

$$P_{ac} = VI \cos \phi \text{ watts} \quad (8.2)$$

Here, cos ϕ is the power factor of the circuit and ϕ indicates the phase difference between circuit voltage (V) and current (I). The operating principle, and the working of both ammeters and voltmeters is almost similar. In an ammeter, a deflecting torque is produced by the current under measurement and in a voltmeter, this deflecting torque is produced by a current proportional to the voltage under measurement. It is essential that the power consumption of these measuring instruments should be ideally zero or practically very minimum. Also, when these instruments are connected in the circuit for a parameter measurement, the circuit conditions should not be altered and hence, a proper case is needed in designing these instruments.

The ammeters should have very negligible internal resistance, because they are connected in series in the circuit and the power consumption in the meter is given by Eq. (8.3).

$$P_{am} = I^2R_{am} \quad (8.3)$$

Here, I is the current to be measured and R_{am} is the resistance of the ammeter. For P_{am} to be minimum, R_{am} should be as minimum as possible.

The voltmeters should have very high internal resistance, because they are connected in parallel in the circuit and the power consumption in the meter is given by Eq. (8.4)

$$P_{vm} = V^2/R_{vm} \quad (8.4)$$

Here, V is the voltage to be measured and R_{vm} is the resistance of the voltmeter. For P_{vm} to be minimum, R_{vm} should be as high as possible.

Both ammeters and voltmeters can be built using different types such as Permanent Magnet Moving Coil (PMMC) type, moving-iron type, electrostatic type, rectifier type, etc. A PMMC type meter is useful for dc quantities; an induction-type meter is useful for ac quantities and an electrodynamometer type is suitable for measurement of both ac and dc quantities. The scope of this text is limited to dc measurement using a PMMC instrument and ac measurement using a rectifier-type instrument. A PMMC instrument is shown in Fig. 8.1 which forms the basis of an ammeter and a voltmeter.

It consists of a permanent magnet, a moving coil, a pivotal arrangement with a pointer, a bearing with a jewel and a spring with balancing weight. The signal (current or voltage) under measurement produces a magnetic field in the coil which suitably interacts with the magnetic field produced by the permanent magnet. This results in the pointer movement proportional to signal magnitude. The torque produced due to the field moves the pointer on a scale that is calibrated in terms of either voltage or current (depending on the meter). The restoring of meter pointer is done by the spring action and the

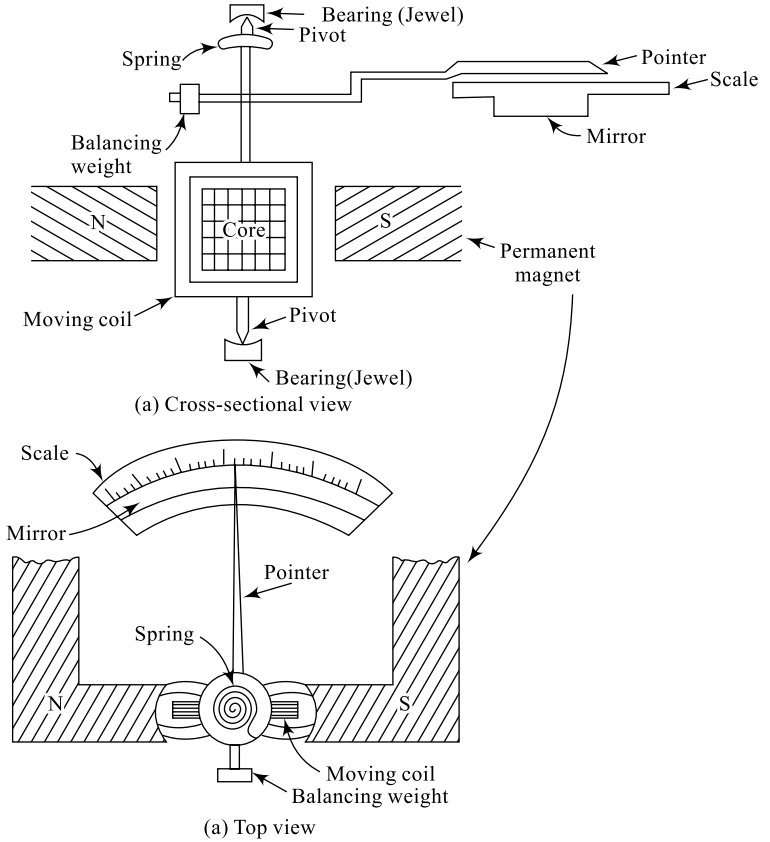


Fig. 8.1 A PMMC meter

balancing weight. A mirror is provided beneath the scale to avoid an error called "Parallox" and this results in more accuracy. Parallox is an error in meter reading that is resulted when the pointer, the value marking on the scale and the human eye are not in line. Even a small angle deviation in these three reduces the reading accuracy.

8.2 VOLTAGE MEASUREMENT

Based on the PMMC instrument principle in Section 8.1, a voltmeter can be constructed for measurement of dc voltages. A simple arrangement of a dc voltmeter is shown in Figure 8.2; the series resistance R_S is called the **multiplier** and the combination of meter and R_S together forms the voltmeter.

Here, terminals *AB* represent the voltage measuring points, I_m is the maximum meter current, R_{vm} is the meter resistance and R_S is the series resistor used to safeguard the meter from excess current flow. The value of R_S is calculated as given by Eq. (8.7).

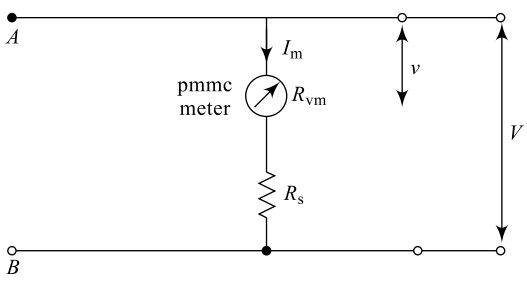


Fig. 8.2 PMMC voltmeter

Voltage across meter

$$v = I_m R_{vm} \tag{8.5}$$

Voltage across terminals AB

$$V = I_m(R_{vm} + R_S) \tag{8.6}$$

Hence, the series resistance

$$R_S = \left(\frac{V - I_m R_{vm}}{I_m} \right)$$

$$R_S = \left(\frac{V}{I_m} - R_{vm} \right) \tag{8.7}$$

This meter can be range extended to read multiple voltage ranges as shown in Fig. 8.3. Here, R_{S_1}, R_{S_2}, etc. are all series resistances that decide the range of V_1, V_2, etc. and are calculated using Eq. 8.7. Selection of the switch position depends on the range of voltage to be measured.

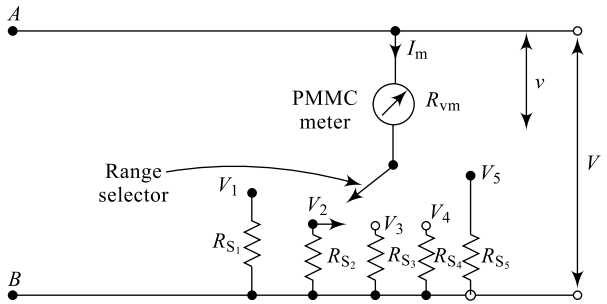


Fig. 8.3 Multirange voltmeter

Example 8.1

A dc ammeter has a resistance of 10 Ω and a power dissipation of 100 mW. What is the current flowing through the meter?

Solution Given $R_{am} = 10\ \Omega$, $P_{am} = 100$ mW, $I = ?$
From Eq. (8.3),

$$I^2 = \frac{P_{am}}{R_{am}}$$

$$= \frac{100 \times 10^{-3}}{10} = 0.01$$

i.e. $$I = 0.1 \text{ A}$$

Example 8.2

A dc voltmeter has a resistance 10,000 Ω and a measured voltage of 50 volts. What is the power dissipated?

Solution Given $R_{vm} = 10{,}000\ \Omega$, $V = 50$ V

From Eq. (8.4),

$$P_{vm} = V^2/R_{vm}$$
$$= (50)^2/10{,}000$$
$$= 250 \text{ mW}$$

Example 8.3

A moving coil meter has a potential difference of 100 mV and a meter current of $I_m = 10$ mA. Calculate the series resistance for a terminal voltage of 1000 V.

Solution Given $I_m = 10$ mA, $v = 100$ mV, $V = 1000$ V, $R_S = ?$
From Eq. (8.5),

$$R_{vm} = \frac{V}{I_m}$$
$$= \frac{100 \text{ mV}}{10 \text{ mA}} = 10\ \Omega$$

Now from Eq. (8.7),

$$R_S = \left(\frac{V}{I_m} - R_{vm}\right)$$
$$= \left(\frac{1000}{10 \text{ mA}} - 10\right) \cong 100{,}000\ \Omega$$

8.3 CURRENT MEASUREMENT

Based on the PMMC instrument given in Section 8.1, an ammeter can be constructed for the measurement of dc current. A simple arrangement of a dc ammeter is shown in Fig. 8.4; the shunt resistance R_{sh} along with the meter from the ammeter.

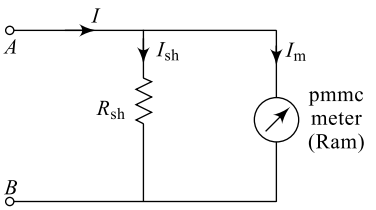


Fig. 8.4 PMMC ammeter

Here, the terminals *AB* forms the arm through which the current is to be measured. I_m is the current through the meter, R_{am} is the resistance of the meter, R_{sh} is the shunt resistance and I is the current under measurement. The value of R_{sh} is calculated using Eq. (8.10).

Since the R_{sh} and meter are in shunt the voltage across them will be same and is given by

$$I_{sh} \times R_{sh} = I_m R_{am} \tag{8.8}$$

i.e.
$$R_{sh} = \frac{I_m R_{am}}{I_{sh}} \tag{8.9}$$

But $I_{sh} = (I - I_m)$ and, therefore,

$$R_{sh} = \frac{I_m R_{am}}{(I - I_m)} \tag{8.10}$$

This meter can be range extended to read multiple currents as shown in Fig. 8.5. Here R_{sh_1}, R_{sh_2}, etc. are all shunt resistances that decide the range of current that can be measured and all these values are estimated using Eq. (8.10).

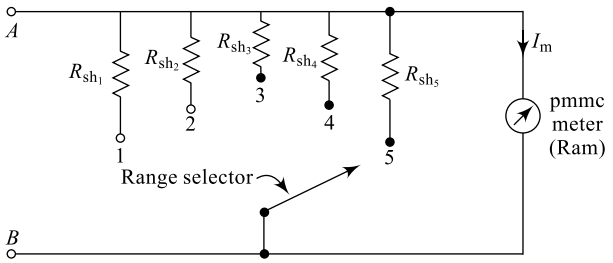


Fig. 8.5 Multirange ammeter

Example 8.4

In example 8.3, calculate the shunt resistance for a current of 100 A.

Solution Given $I_m = 10$ mA, $v = 100$ mV, $I = 100$ A, $R_{sh} = ?$

From Eq. (8.5), $$R_{am} = \frac{V}{I_m} = \frac{100 \text{ mV}}{10 \text{ mA}} = 10\ \Omega$$

From Eq. (8.10), $$R_{sh} = \frac{I_m \times R_{am}}{(I - I_m)}$$

$$= \frac{10 \times 10^{-3} \times 10}{(100 - 10 \text{ mA})} = 0.001\ \Omega$$

Example 8.5

A 1 mA pmmc meter with a 100 Ω resistance is to handle a maximum current of 100 mA, calculate R_{sh}.

Solution Given $I = 100$ mA, $R_{am} = 100\ \Omega$, $R_{sh} = ?$, $I_m = 1$ mA

From Eq. (8.10),

$$R_{sh} = \frac{I_m \times R_{am}}{(I - I_m)}$$

$$= \frac{1 \times 100}{(100 \times 10^{-3} - 1 \times 10^{-3})} = \frac{100}{99 \times 10^{-3}}$$

$$R_{sh} = 1.01\ \Omega$$

Example 8.6

A moving-coil ammeter has a shunt of 0.02 Ω. Find current through the shunt if the potential difference across coil is 500 mV. Also, find the coil resistance if the current of 0.5 mA flows corresponding to a full-scale deflection.

Solution Given $R_{sh} = 0.02\ \Omega$, $V = 500$ mV, $I_{sh} = ?$

$$R = ?\ \text{if}\ I = 0.5\ \text{mA}$$

Now
$$I_{sh} = \frac{V}{R_{sh}} = \frac{500 \times 10^{-3}}{0.02} = 25\ \text{A}$$

Also,
$$R = \frac{V}{I}$$
$$= \frac{500 \times 10^{-3}}{0.5 \times 10^{-3}} = 1000\ \Omega$$

8.4 RECTIFIER-TYPE VOLTMETER

The current and voltage meters can be built using rectifier element and are useful in ac quantity measurement. These instruments can be built both using a half-wave rectifier and full-wave rectifier. They offer many good advantages in ac quantity (V or I) measurement such as wide frequency range, very low power dissipation, good accuracy (around ±5%), good sensitivity, etc. Figure 8.6 shows an ac voltmeter using a full-wave rectifier circuit. A conventional PMMC meter is used for indication and is preceded by a bridge-type of full-wave rectifier. The PMMC meter forms the load for the bridge rectifier formed using diodes D_1, D_2, D_3 and D_4. The series multiplier resistance R_S is selected corresponding to a full-scale deflection. When a dc voltage V is applied to the meter, the current through the meter is given by

$$I = \frac{V}{(R_m + R_s)} \tag{8.11}$$

and it causes a full-scale deflection.

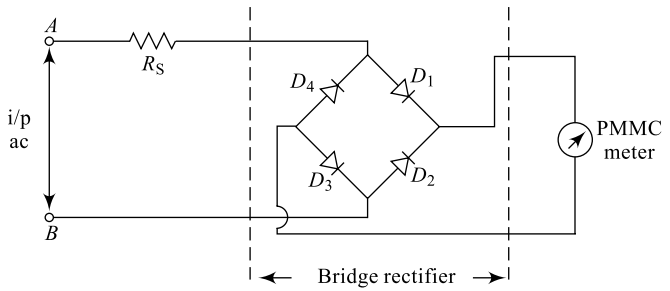


Fig. 8.6 Rectifier-type voltmeter

If an ac signal v given by Eq. (8.12) is applied, the

$$v = V_m \sin \omega t \tag{8.12(a)}$$

$$= \sqrt{2}\ V \sin \omega t \tag{8.12(b)}$$

then the average voltage across the meter is a given by Eq. (8.13)

$$V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t\, d\omega t \tag{8.13}$$

$$= \frac{2V_m}{\pi} \tag{8.14(a)}$$

i.e. $$V_{dc} = 0.636\ V_m \qquad [8.14(b)]$$

i.e. $$V_{dc} = 0.9\ V \qquad [8.14(c)]$$

The corresponding average current in the meter is given by Eq. (8.15); this equation indicates that the sensitivity of an FWR type instruments with ac *i/ps* is 90% of that of dc voltage of same magnitude.

$$I_{aw} = \frac{0.9\,V}{(R_m + R_S)} \tag{8.15}$$

However, the ac sensitivity of the rectifier-type instrument with a sinusoidal input is given by Eq. (8.16); here S_{dc} is the

$$S_{ac} = 0.9\ S_{dc} \tag{8.16}$$

dc sensitivity of the instrument is given by Eq. (8.17)

$$S_{dc} = \frac{1}{If_s} v/\Omega \tag{8.17}$$

I_{fs} is the current required to produce full-scale deflection.

8.5 MULTIMETERS

A multimeter may be implemented with a galvanometer's meter movement. The meters for analog measurement of current, voltage and resistance are constructed using the basic d'Arsonval movement used in galvanometers (a galvanometer is an instrument used to detect presence of very small magnitude currents or voltages in a circuit). Hence, it is possible to construct a common meter for measuring all these quantities both in ac and dc forms and is called a multimeter. Analog multimeters are common, although a quality analog instrument will be about the same cost as a digital multimeter.

8.5.1 Analog Multimeters (AMMs)

Analog multimeters have the precision and reading accuracy limitations and so are not built to provide the same accuracy as digital instruments. Analog meters are sometimes considered better for detecting the rate of change of a reading; some digital multimeters include a fast-responding bar-graph display for this purpose. A typical example is a simple "good/no good" test of a filter capacitor, which is quicker and easier to read on an analog meter (though somewhat less accurate than with a digital meter).

In Fig. 8.7 an analog multimeter is shown; it contains a mirror in the meter to avoid parallox error during reading. The meter movement in a moving-pointer analog multimeter is practically always a moving-coil galvanometer of the d'Arsonval type, using either jeweled pivots or taut bands to support the moving coil. In a basic analog multimeter, the current to deflect the coil and pointer is drawn from the circuit being measured; it is usually an advantage to minimise the current drawn from the circuit. The sensitivity of an analog multimeter is given in units of ohms per volt. For example, an inexpensive multimeter would have a sensitivity of 1000 ohms per volt and would draw 1 milliampere from a circuit at the full-scale measured voltage. More expensive (and more delicate) multimeters would have sensitivities of 20,000 ohms per volt or higher, with a 50,000 ohms per voltmeter (drawing 20 microamperes at full scale) being about the upper limit for a portable, general-purpose, non-amplified analog multimeter. To avoid the loading of the measured circuit by the current drawn by the meter movement, some analog multimeters use an amplifier inserted between the measured circuit and the meter movement. While this increases the expense and complexity of the meter and requires a power supply to operate

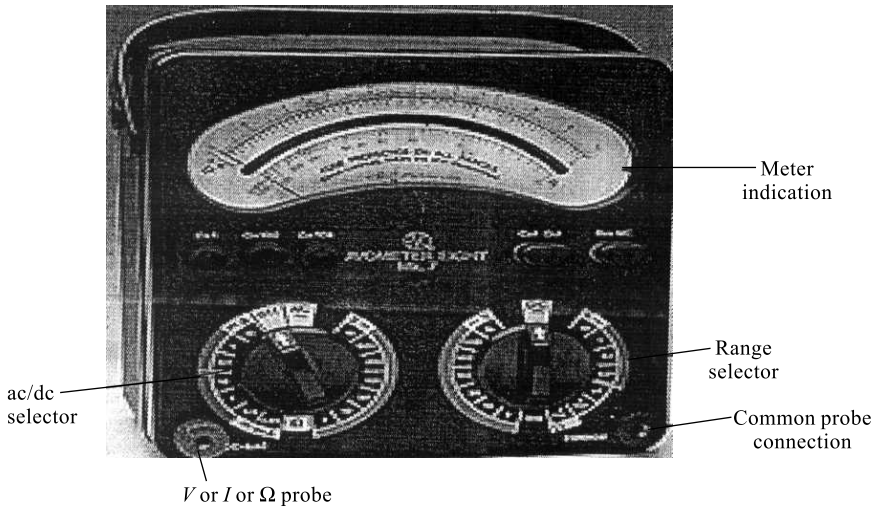


Fig. 8.7 Analog multimeter

the amplifier, by use of vacuum tubes or field effect transistors the input resistance can be made very high and independent of the current required to operate the meter movement coil. Such amplified multimeters are called VTVMs (Vacuum Tube VoltMeters), TVMs (Transistor VoltMeters), Fet-VOMs, and similar names.

8.5.2 Digital MultiMeters (DMMs)

Digital Multimeters (DMMs) are often (inaccurately) referred to as digital voltmeters or DVMs at their heart is an analog-to-digital converter (ADC). A block diagram of a DMM is shown in Fig. 8.8; here, the display may be LED or LCD type.

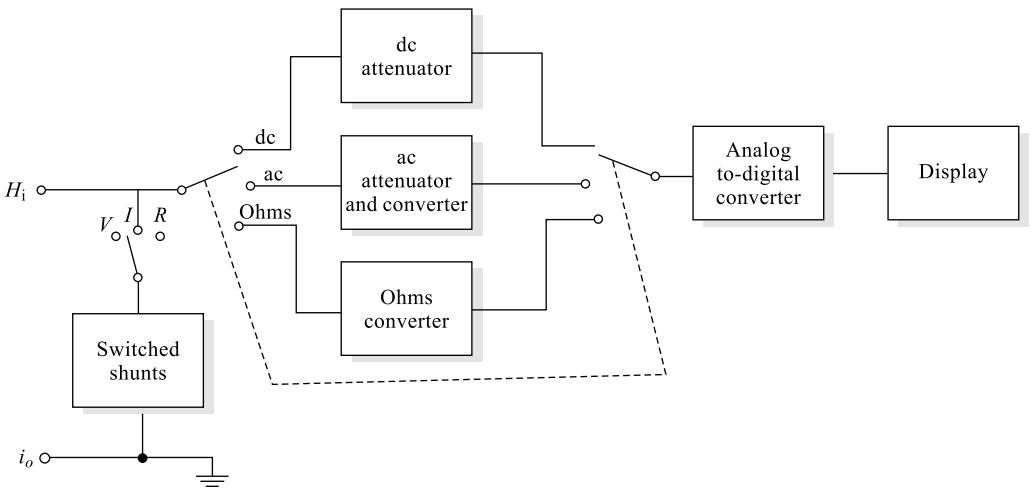


Fig. 8.8 Block diagram of a digital multimeter

An *Analog-to-Digital Converter (ADC)* receives an analog input signal and produces an approximate digital output. Similarly a digital-to-analog converter (DAC) receives digital input and produces an approximate analogue output. Thus ADC and DAC form an important part of any data acquisition system. Measurement of voltage, current and resistance is achieved using appropriate circuits to produce a voltage that is proportional to the quantity under measurement. In simple DMMs, alternating signals are rectified to give the average value which is multiplied by 1.11 to directly give the rms value of the sine wave.

An alternator is a circuit used to reduce the signal amplitude without changing the shape and other characteristics of the signal. Other characteristics importantly include frequency and phase of the signal. Attenuators are constructed using high-precision resistors and hence are passive circuits.

In Fig. 8.9, some typical multimeters are shown; Fig. 8.9(a) is a digital multimeter and 8.9(b) is an analog multimeter. DMMs offer a very high accuracy and AMMs are very rugged in construction. To avoid error parallox during reading, a mirror is provided beneath the needle.

(a) Digital multimeters (b) Analog multimeter

Fig. 8.9 Multimeters

Example 8.7

A full-wave rectifier type of voltmeter has an *i/p* whose peak voltage is 15 V and a series multiplier of 750 Ω. What is the average voltage indicated by the meter?

Solution From Eq. [8.14(b)], the average value of voltage

$$V_{dc} = 0.636\ (V_m)$$
$$= 0.636 \times 15 = 9.54\ \text{V}$$

Example 8.8

In the example 8.7, if the average current is 12 mA. What is the meter resistance?

Solution From Eq. [8.14(c)] and (8.15),

$$(R_m + R_s) = \frac{V_{dc}}{I_{am}}$$

$$= \frac{9.54}{12 \times 10^{-3}}$$

$$= 795\ \Omega$$

Given $R_s = 750\ \Omega$ and hence

$$R_m = (795 - 750)$$

$$\boxed{R_m = 45\ \Omega}$$

1. Battery

Hand-held meters use a battery or batteries for continuity and resistance readings at the very least, and the battery may also power a digital multimeter or an amplifier in a FET-VOM. This allows the meter to test a device that is disconnected from a mains power source, by supplying its own low voltage for the test. It is one of the most important safety features of the multimeter. A 1.5 volt AA battery is typical; more sophisticated meters with added capabilities will also commonly use a 9-volt battery in addition for some types of readings, or higher-voltage batteries for higher resistance testing. Meters intended for testing hazardous locations or for use on blasting circuits may require use of a manufacturer-specified battery to maintain their safety rating.

2. Probes

A multimeter can utilise a variety of test probes to connect to the circuit or device under test. Crocodile clips, retractable hook clips and pointed probes are the three most common attachments. The connectors are attached to flexible, thickly insulated leads that are terminated with connectors appropriate for the meter. Handheld meters typically use shrouded or recessed banana jacks, while bench-top meters may use banana jacks or BNC connectors, 2 mm plugs and binding posts have also been used at times, but are not so common today. Meters which measure high voltages or current may use noncontact attachment mechanism to trade accuracy for safety. Clamp meters provide a coil that clamps around a conductor in order to measure the current flowing through it.

3. Safety

All but the most inexpensive multimeters include a fuse, or two fuses, which will sometimes prevent damage to the multimeter if it is overloaded. However, the fuse often only protects the highest current range on the multimeter. A common error when operating a multimeter is to set the meter to measure resistance or current and then connect it directly to a low-impedance voltage source; meters without protection are quickly damaged by such errors, and can sometimes explode causing injury to the operator. Fuses used in meters will carry the maximum measuring current of the instrument, but are intended to clear if operator error exposes the meter to a low-impedance fault.

8.6 CATHODE RAY OSCILLOSCOPE (CRO)

A cathode ray oscilloscope, popularly called CRO is a most versatile and useful laboratory measuring instrument. It is used for many useful applications such as signal display, amplitude measurement and analysis of waveforms.

It is a very fast *X-Y* recorder which can be used to measure voltage, current, frequency, phase angle, etc. of an input or output waveform and for these reasons a CRO is affectionately called the **Eye** of an Electronics engineer. The block diagram of a CRO is shown in Fig. 8.10; it contains a Cathode Ray Tube (CRT) and a big set of associated circuitry.

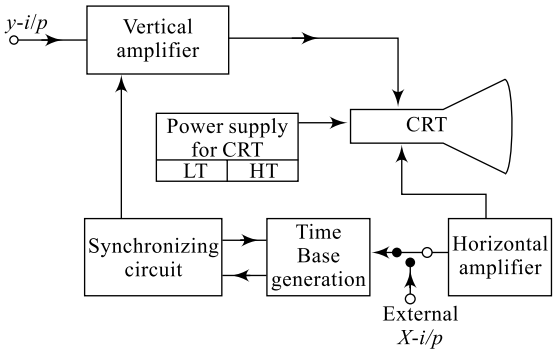


Fig. 8.10 CRO block diagram

A Cathode Ray Tube (CRT) is the heart of any CRO. As shown in the block diagram, the associated circuitry along with CRT helps in displaying a waveform under measurement. A CRO can be better understood through the following main parts.

1. Cathode Ray Tube (CRT)

The main parts of a CRT are electron-gun assembly (that contains electron-beam generator, focussing & accelerating anodes), deflection plates (vertical and horizontal) and fluorescent screen. The electron-gun assembly generates controls the electron beam. This electron beam creates a bright spot on hitting the fluorescent screen. The electron beam is modulated by (*y*-axis control) the *i/p* signal and its horizontal movement is controlled by a sweep signal generated by horizontal amplifier. Thus, it creates both *x* and *y* movements for the signal and hence, is a very fast *x*-*y* recorder.

2. Power Supply

In order to operate a CRO, the power supply needed consists of two-parts, the LT and the HT. The Low-Tension (LT) supply is for filament heating. The cathode is indirectly heated by this filament. The High-Tension (HT) supply is for focussing and accelerating anodes to control the electron beam.

3. Vertical Amplifier

It receives signal to be displayed as its *i/p* (*y* – *i/p*). This section in turn is connected to vertical deflection plates which will modulate the electron beam vertically.

4. Horizontal Amplifier

This forms the *x*-*i/p* and the sweep causes the *x*-axis movement of the signal to be displayed. A time-base generator (sweep) supplies the horizontal amplifier whose *o/p* is connected to horizontal deflection plates. The horizontal deflection plates cause the electron beam to move horizontally.

An external *i/p* as trigger can also be connected (if necessary) instead of internal triggering.

Both horizontal *i/p* and vertical *i/p*s are synchronised through a synchronising circuit in order to have proper display of the signal.

8.6.1 Cathode Ray Tube

The block diagram of a CRT is shown in Fig. 8.11. It consists of a large number of components that are responsible for producing a visible display of the signal under measurement.

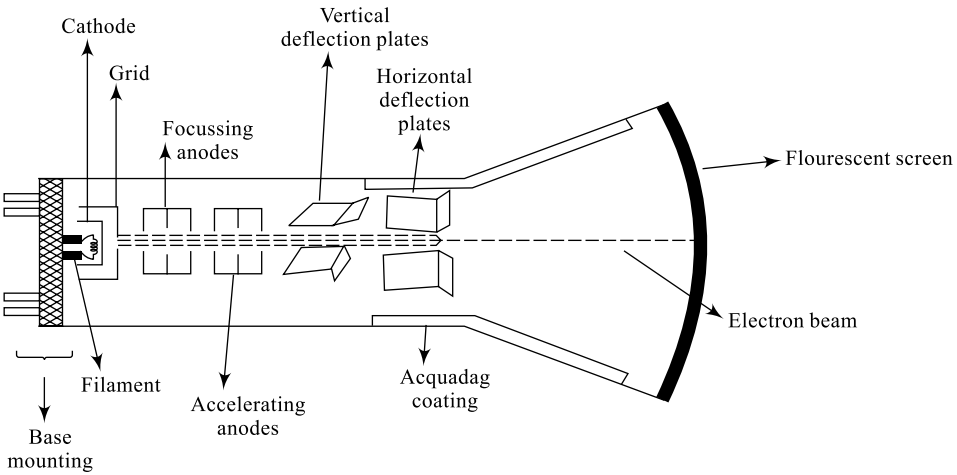


Fig. 8.11 CRT block diagram

Indirectly heated cathode produces a beam of electrons which is sharply focused by the focussing anodes. Electrostatic focussing or magnetic focussing is used. The beam is then accelerated to a high velocity by accelerating anodes. The deflection of electron beam will be of two types electrostatic deflection and magnetic deflection. This focussed and accelerated electron beam strikes the fluorescent screen with sufficient energy to cause a luminous spot on the flourescent screen. The *vertical & horizontal* movement of the beam is controlled by deflection plates. The acquadag coating collects the free electrons (if any) back to the gun assembly for focussing and acceleration making it possible to reuse them. Electrostatic deflection is preferred compared to electromagnetic deflection for the electron beam since magnetic deflection requires large currents for deflection. This results in loss of power, but an electrostatic deflection requires very little power. Also a magnetic deflection at high frequencies is very difficult and troublesome to handle; therefore an electrostatic deflection is used.

The displacement of the electron beam produced on the screen is dependent on important parameters such as length of the deflection plates (l), separation (d) between these plates, voltage applied to these plates (V_d), the accelerating anode voltage (V_a) and distance between the screen and the deflection plates centre (L). The displacement (D) produced is given by Eq. (8.18):

$$D = \frac{L \times l \times V_d}{2 \times V_a \times d} \tag{8.18}$$

The deflection sensitivity of the electrostatic deflection system depends on parameters such as length of deflection plates (l), distance between screen and deflection plates (L), the accelerating anode voltage (V_a), separation between plates (d) and is given by Eq. (8.19):

$$S = \frac{L \times l}{2 \times V_a \times d} \tag{8.19}$$

This is indicated in Fig. 8.12; here the screen is shown as a vertical line only for convenience, but in practice, the screen will be a (concave) bulged shape. Sensitivity and displacement are related through Eq. (8.20); here, V_d is the deflecting plate voltage.

$$S = \frac{D}{V_d} \tag{8.20}$$

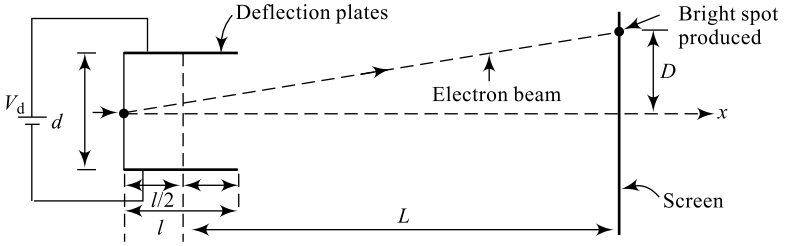


Fig. 8.12 Electron-beam

Example 8.9

A cathode-ray tube uses electrostatic deflection with deflection plates 2 cm long and placed 4 mm apart. The screen is 25 cm away from the centre of the plate. Calculate the sensitivity of the tube if the final anode has a potential of 1000 V.

Solution Given $l = 2$ cm, $L = 25$ cm, $d = 5$ mm, $V_a = 1000$ V, $S = ?$

From Eq. (8.19), $$S = \frac{25 \times 10^{-2} \times 2 \times 10^{-2}}{2 \times 1000 \times 4 \times 10^{-3}}$$

$$S = 0.625 \text{ mm/V}.$$

Example 8.10

In example 8.10, what is the value of anode potential that should be applied to the final anode so that the sensitivity is 0.5 mm/V.

Solution From Eq. (8.18), $$V_a = \frac{L \times l}{2 \times d \times S}$$

i.e. $$V = \frac{25 \times 10^{-2} \times 2 \times 10^{-2}}{2 \times 4 \times 10^{-3} \times 0.5 \times 10^{-3}}$$

i.e. $$V = 1250 \text{ V}$$

Example 8.11

Find the deflection produced in Example 8.10, if a voltage of 200 V is applied to the deflection plates.

Solution Given $V_d = 20$ V and $S = 0.625 \times 10^{-3}$ m/V.
From Eq. (8.20),

$$S = \frac{D}{V_d}$$

i.e. $$D = S \times V_d = 0.625 \times 10^{-3} \times 20$$

$$D = 12.5 \text{ mm}$$

Example 8.12

Find the deflection of electron beam produced in Example 8.11 if the deflection voltage is 20 V.

Solution Given $V_d = 20$ V and $S = 0.5$ mm/V

Table 8.1 Flourescent phosphor and their colours.

Phosphor	Flourescent colour	Application
P-1	Green	General-purpose CROs
P-4	White	Television display
P-7	Yellow	Radar display
P-12	Orange	Radar display
P-19	Orange	Radar display

From Eq. (8.19),

$$D = S \times V_d$$
$$= 0.5 \times 10^{-3} \times 20$$
$$D = 10 \text{ mm}$$

On the walls of the cathode ray tube, a layer of suitable phosphor material is coated, so that the electron beam hitting the screen produces a visible light. Table 8.1 presents different phosphor materials and the colour of the light produced along with application.

The front panel of a practical oscilloscope contains a series of controls and settings that are useful for signal display and measurement. Figure 8.13 indicates the front panel of a typical laboratory CRO. Different controls adjustments and settings, the internal block to which they belong and their functions and indicated in Table 8.2.

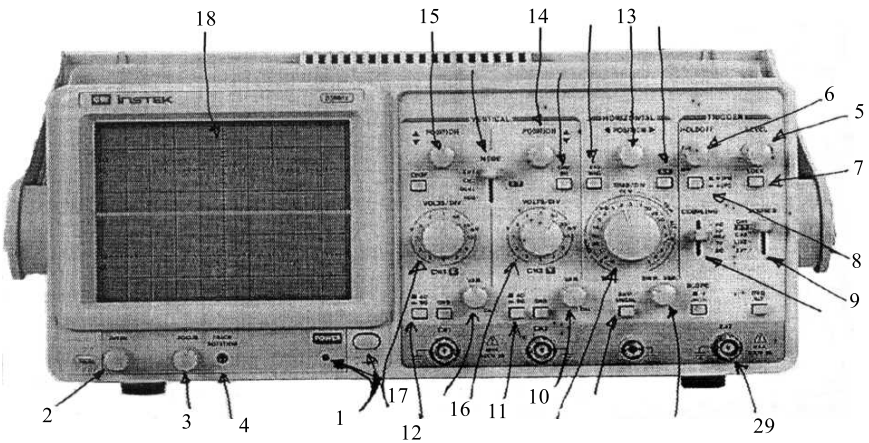


Fig. 8.13 A Typical CRO used in laboratories

Table 8.2 CRO controls and settings

Sl. No.	Control	Block	Function
1	ON/OFF power	Power supply	Switching ON and OFF the CRO
2	Intensity	Accelerating Anodes	The illumination of the display produced is controlled.
3	Focus	Focussing Anodes	The size of the electron beam is controlled.

(*Contd.*)

(*Contd.*)

4	Trace Rotation	Deflection unit	The *X*-axis tilt adjustment
5	Level	Trigger	Waveform stabilizing
6	Hold	Trigger	Waveform stabilizing
7	Lock	Trigger	Waveform stabilizing
8	Magnitude	Attenuator	Scale selector for magnitude measurement (along with 16 & 17)
9	Time multiplier	Time base generator	Multiplier for time axis (along with 10)
10	Time/division	Sweep generator (Horizontal)	Varying *X*-axis measurement
11 & 12	Function select ac/dc	—	Choosing between ac and dc measurements
13	Horizontal position	Horizontal section	Horizontal movement of signals on channel-*x* and channel-*y*.
14	Vertical position for channel-*x*	Vertical section	Vertical movement of signals on channel-*x*.
15	Vertical position for channel-*y*	Vertical section	Vertical movement of signal on channel-*y*
16	Voltage/or for channel-*y*	Attenuator	Amplitude control for signal on channel-*y*
17	Voltage/Div for channel-*x*	Attenuator	Amplitude control for signal on channel-*x*
18	Screen	CRT	Display signals

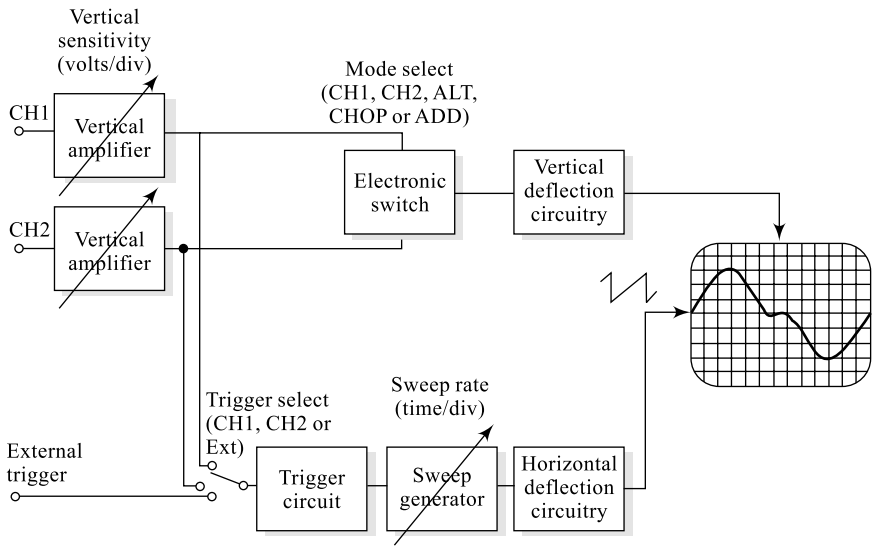


Fig. 8.14 CRO Front panel controls connected to internal blocks

Figure 8.14 indicates the typical connectivity of the front panel controls with the internal blocks of a CRO. Second column of Table 8.2 represents this and is completely mapped in the diagram. The verti-

cal amplifier (volts/div) modulates the amplitude of the signal being displayed and the vertical deflection circuitry is responsible for *y*-axis movement (21 and 27) of the signal. The sweep generator (time/div) modulates the width of the signal and the horizontal deflection circuitry is responsible for *x*-axis movement (13) of the signal. As indicated in the diagram, the trigger for horizontal movement may be selected either from input or from an external source.

8.6.2 Applications of CRO

CRO is a most versatile, visual and accurate electronic laboratory equipment that can be used to display and measure various parameters of signals. The following are some of the most important applications of a CRO:

(i) Display waveforms
(ii) Measure the amplitudes of signals
(iii) Measure the time period of a signal
(iv) Measure the frequency of a signal
(v) Measure the phase angle of a signal
(vi) Measure the phase difference between two signals

The signal whose parameters are to be measured is applied to one of the channels and from the display, various parameters are measured. In Fig. 8.15, two signals are displayed on two channels: '*T*'-represents the time period of the signal and its value is obtained by multiplying number of divisions in one full cycle with time/div value. In the example, one full cycle of waveform has 8 divisions and if the value of time/div is 5 μS then the time period of the signal is $(8 \times 5\ \mu s) = 40\ \mu s$. Similarly, '*V*' represents the peak-to-peak amplitude of the signal and its value is obtained by multiplying number of divisions with volts/div value. In the example '*V*' contains 3.6 divisions and if the value of volts/div is 2 then peak-to-peak amplitude of the signal is $(3.6 \times 2) = 7.2$ V; hence its peak amplitude $V' = V/2$. The phase angle of the signal is given by Eq. (8.21) and frequency of the signal is given by Eq. (8.22a) and corresponding T is given by Eq. (8.22b). Frequency and phase angle of the signal can also be measured using Lissajous figures and is presented in Section 8.7.

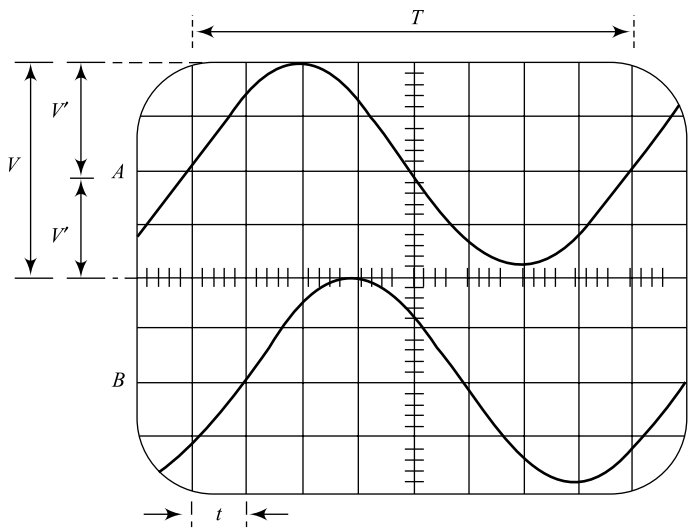


Fig. 8.15 CRO measurements

$$\text{Phase angle } \theta = \frac{t}{T} \times 360^\circ$$

$$= \frac{t}{T} \times 2\pi \text{ radians} \tag{8.21}$$

Here, 'T' in units of number of divisions
Frequency of signal

$$f = \frac{1}{I}\text{Hz} \tag{8.22a}$$

Here 'I' in units of seconds and it is given by

$$T = \text{Number of divisions} \times (\text{time/div}) \tag{8.22b}$$

Example 8.13

A CRO measurement has 2.3 divisions measured for peak-to-peak amplitude of a signal; what is the rms value of the signal, if volts/div is set on 5?

Solution No. of divisions for peak-to-peak signal = 2.3

volts/div = 5

$\therefore$ $V_{(PP)} = 2.3 \times 5 = 11.5$ V

i.e. $V_P = \dfrac{V_{(PP)}}{2} = \dfrac{11.5}{2} = 5.75$ V

rms value of signal is

$$V = \frac{V_P}{\sqrt{2}} = \frac{5.75 \text{ V}}{\sqrt{2}} =$$

Example 8.14

A CRO measurement has 5.6 divisions measure for total time period T of the signal; what is the time period and frequency of the signal if time/div is set on 5 μs?

Solution Number of divisions = 5.6

Time/div = 5 μs

$\therefore$ $T = 5.6 \times 5$ ms = 28 μs

From Eq. (8.22a), frequency of signal

$$f = \frac{1}{28 \times 10^{-6}} = 35714.3 \text{ Hz} \simeq 35.714 \text{ kHz}$$

Example 8.15

In Fig. 8.15, the signal A has a total period of 8 full divisions; if the frequency of this signal is 6250 Hz. What might be the setting on time/div knob?

Solution No. of divisions = 8
Frequency of signal = 6250 Hz
From Eq. (8.22a),

$$T = \frac{1}{f}$$

$$= \frac{1}{6250} = 1.6 \times 10^{-4}$$

Here, T = No. of divisions × (time/div)

$$\therefore \quad \text{time/div} = \frac{I}{\text{No. of div}} = \frac{1.6 \times 10^{-4}}{8} = 20\ \mu\text{s}$$

Example 8.16

In Fig. 8.15, the signal A has a total peak-to-peak amplitude of 3.8 divisions; if the volts/div is set at 10 V. What is the rms value of the signal?

Solution Peak-to-peak amplitude $= 3.8 \times 10$
$= 38$ V

$$\therefore \quad \text{peak voltage } V_m = \frac{38}{2} = 19 \text{ V}$$

rms value of signal is

$$V = \frac{V_m}{\sqrt{2}} = \frac{19}{\sqrt{2}} = 13.44 \text{ V}$$

8.7 LISSAJOUS FIGURES

Measurement of phase and frequency of a signal can be done as illustrated in Section 8.6.2. Another fastest, accurate and familiar method is to use a pattern of display on CRO known as Lissajous pattern. A Lissajous figure is obtained on a CRO, by using two signals, one reference and the other unknown signal. One of the signals (reference) is applied to channel-1 or the horizontal deflection plates and the other signal is applied to channel-2 or the vertical deflection plates; for a lissajous pattern to be displayed, the time/div (13) knob should be in x-y mode. Then the resultant pattern is an ellipse, the exact shape of which depends on the signal characteristics such as amplitude, phase difference, frequency, etc. of the two signals. Lissajous figures are mainly used to measure the phase difference and frequency of an unknown signal with respect to known signal values.

8.7.1 Measurement of Phase Difference

Two signals $v_1 = v_m \sin \omega t$ and $v_2 = v_m \sin (\omega t + \theta)$ which are of same frequency when applied to vertical (channel-1) and horizontal inputs (channel-2) with time/div knob set to x-y mode, the pattern of signal on oscilloscope shown in Fig. 8.16 is displayed and is called Lissajous figure.

$$\sin \theta = \pm \frac{x_1}{y_1} \tag{8.23}$$

Now, the phase difference 'θ' between the two signals is given by Eq. (8.24); here 'y_1' is the ordinate when x-input is zero and 'y_2' is the maximum deflection of the spot.

$$\theta = \sin^{-1}\left(\frac{y_1}{y_2}\right) \tag{8.24}$$

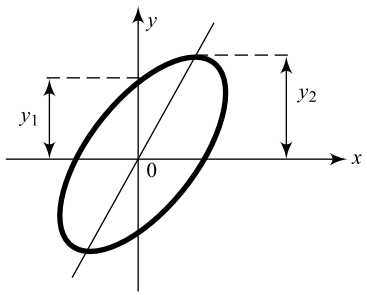
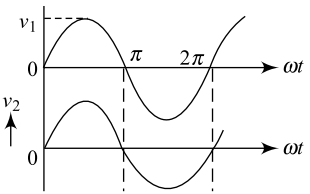
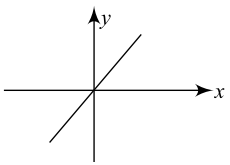
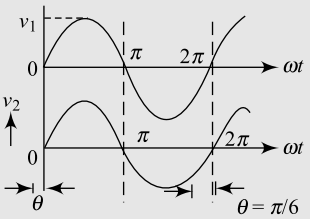
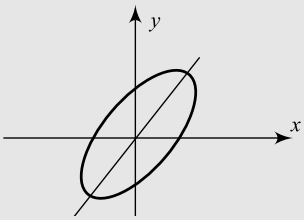
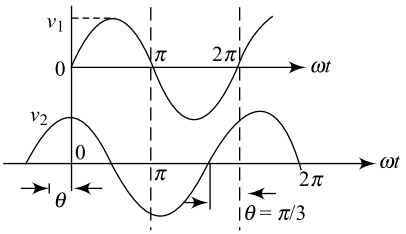
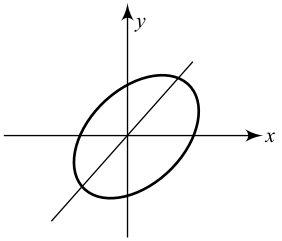
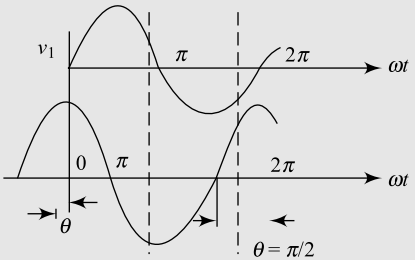
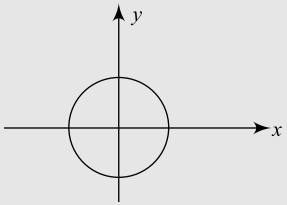
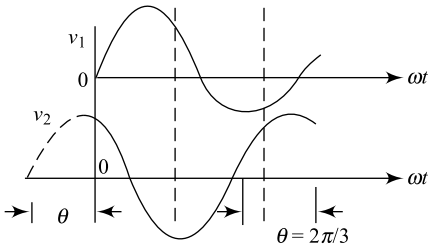
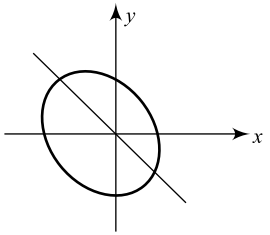


Fig. 8.16 Measurement of phase

The shape of the lissajous pattern produced depends on the phase difference 'θ' between the two signals; the shape varies from a simple diagonal line for $\theta = 0°$ to a circle for $\theta = 90°$ or an ellipse. This is indicated in Table 8.3; v_1 is the reference signal and v_2 varies in phase.

Table 8.3 Lissajous figures and phase difference 'θ'

Sl. No.	Signals v_1 and v_2	Lissajous Figures	Phase difference "θ"
1			$\theta = 0°$
2			θ 30° or = 330°
3			$\theta = 66°$ or = 300°
4			$\theta = 90°$ or = 270°
5			$\theta = 120°$ or = 240°

(*Contd.*)

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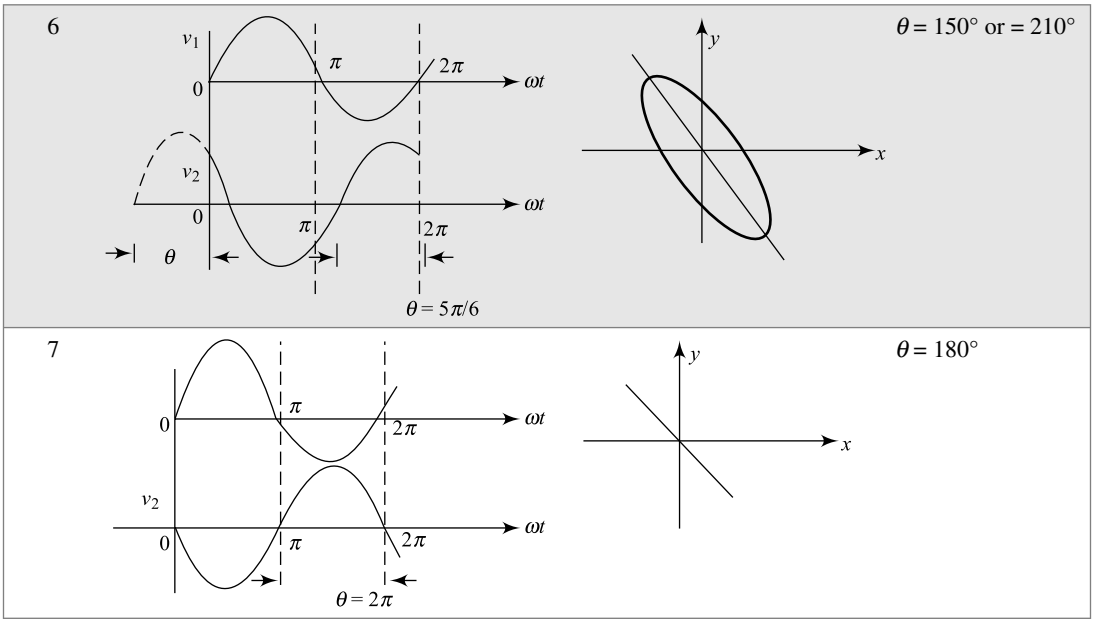
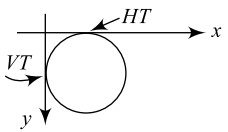
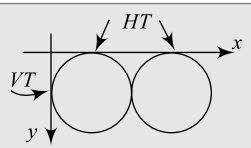


8.7.2 Measurement of Frequency

To measure the unknown frequency of a signal using Lissajous pattern, the signal of known frequency f_1, is applied to horizontal deflection plates or *y*-plates and the signal whose frequency f_2, is to be measured is applied to the vertical deflection plates or *x*-plates. With time/div knob in *x*-*y* position, the lissajous pattern is displayed; the shape of which depends on the ratio of two frequencies. The ratio of these two frequencies is given by Eq. (8.25) and the lissajous pattern for different ratios is provided in Table 8.4.

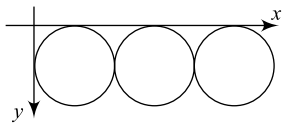
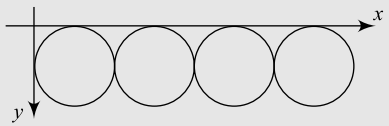
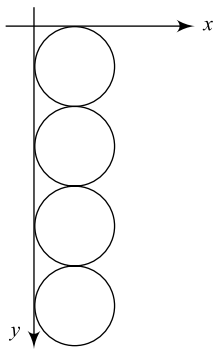
$$\frac{f_1}{f_2} = \frac{\text{Number of horizontal tangencies}}{\text{Number of vertical tangencies}} = \frac{N_{HT}}{N_{VT}} \tag{8.25}$$

Table 8.4 Lissajous figures for frequency measurement

Sl. No.	Pattern	N_{HT}	N_{VT}	Value of unknown frequency
1		1	1	$f_2 = f_1$
2		2	1	$f_2 = 2f_1$

(*Contd.*)

(*Contd.*)

3		3	1	$f_2 = 3f_1$
4		4	1	$f_2 = 4f_1$
5		1	4	$f_2 = \frac{f_1}{4}$

Example 8.17

In Fig. 8.15, what is the phase angle between signal-A and signal-B?

Solution Considering signal-A as reference; signal-B starts with a delay of 1 full division. For both signal-A and signal-B

1 full cycle = 8 div = 360°

$\therefore$ each division $= \frac{360}{8} = 45°$

$\therefore$ Signal-B has a lagging phase angle

$$\phi = 45°$$

Example 8.18

Signals displayed in Fig. 8.15 result in a Lissajous pattern; what is the ratio of y_1 to y_2?

Solution From Example 8.17 and Fig. 8.15,

$$\theta = 45°$$

From Eq. (8.23),

$$\sin\theta = \frac{y_1}{y_2}$$

i.e. $$\frac{y_1}{y_2} = \sin 45°$$

$$= 0.701$$

i.e. $$y_1 = 0.707 y_2$$

Example 8.19

In Fig. 8.15, in order to make the ratio y_1/y_2 equal to 1, what should be the change in signal-B display with respect to signal-A?

Solution For $y_1/y_2 = 1$, from Eq. (8.25).

$$\theta = \sin^{-1}(1) = 90°$$

In Fig. 8.15, each division = 45°; hence signal-B should start after 2 divisions from signal-A.

Example 8.20

In a frequency measurement using CRO, a signal of frequency, 5 kHz is fed to y plates and another signal of frequency 'f_x' is fed to x-plates. The resulting Lissajous pattern is as in row-3 of Table 8.4. What is 'f_x' value?

Solution From Eq. (8.25),

$$\frac{f_x}{f} = \frac{N_{HT}}{N_{VT}} = \frac{3}{1}$$

i.e. $$f_x = 3f = 3(5 \text{ kHz})$$

$$f_x = 15 \text{ kHz}$$

8.8 DUAL TRACE OSCILLOSCOPE

A dual-trace oscilloscope consists of two separate vertical input channels, namely channel-x and channel-y. Each of these channels have separate controls starting from the attenuator, pre-amplifier and hence the amplitude of the two signals can be independently controlled. Figure 8.17 indicates a block diagram of a dual-trace oscilloscope. The vertical section of the oscilloscope includes two inputs via channel-x and channel-y. The electronic switch 'S' can be operated either in 'alternate mode' or 'chop-mode' which can be selected by the front panel control.

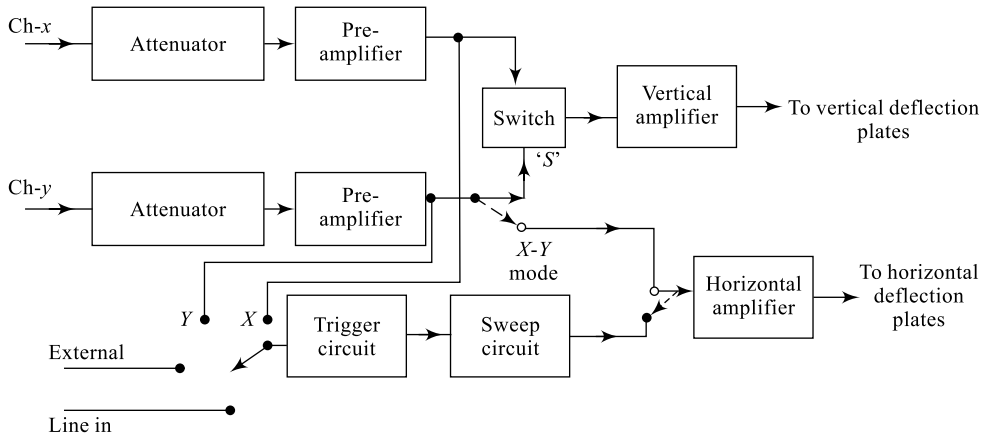


Fig. 8.17 Block diagram of a dual trace CRO

In alternate mode, the electronic switch selects channel-x and channel-y input signals alternative for one cycle of horizontal sweep signal. In order to avoid discontinuity in display, the display is blanked during fly-back period. Further, the display can be improved by inserting a delay line between switch 'S' and the vertical amplifier. However, alternate mode is not suitable for low frequency signal display.

In chopped mode, the switch is operated at a higher speed (few 100 kHz) choosing small portions of the two sigma from ch-x and ch-y. This chopped mode is suitable even for low-frequency signals. To display two fast switching signals, **dual-beam oscilloscope** may be used. In a dual-beam oscilloscope there are two separate vertical channels with or without separate time base generators. But this increases cost of the oscilloscope.

Summary

- Measurement of circuit parameters such as current, voltage, power, power factor, phase angle, etc. is very important in any system design.
- The dc power in a circuit is $P_{dc} = V \cdot I$ (Eq. 8.1) and ac power is $P_{ac} = VI \cos \phi$ (Eq. 8.2)
- A pmmc meter is the basis for ammeter and a voltmeter.
- A voltmeter is connected in parallel and an ammeter is connected in series for measurement.
- A series resistance R_s is always connected in series with a basic pmms meter for meter safety in a voltmeter.
- A shunt resistance R_{sh} is always connected in parallel with the basic pmmc meter for meter safety in ammeter.
- A rectifier type instrument uses a rectifier (HWR or FWR) along with a basic pmmc meter.
- A multimeter is an instrument used to measure current voltage and resistance. It can also be used to test continuity in a circuit, testing devices like diode, transistor.
- A multimeter may be an analog type (Amm) or a digital type (Dmm).
- A CRO is the most versatile electronic measuring instrument that can display signals.
- A CRO can be used to measure voltage, current, time, frequency, phase difference of signals.
- Lissajous figures are very useful in accurate measurement of frequency and phase angle of a signal.

Review Questions

1. Explain in your own words, the significance of circuit parameters in any design.
2. Relate power voltage and current in any system.
3. What is the impact of load on the parameters in Question 2.
4. Draw a phasor diagram relating voltage and current in an ac circuit (use the knowledge of impedance triangle).
5. Explain how to avoid parallox error in measurement?
6. Explain in your own words the importance of R_s in a voltmeter.
7. How do you change the value of R_c in a multimeter, voltmeter? Explain.
8. Explain in your own words, the importance of R_{sh} in an ammeter.
9. How do you choose the value of R_{sh} in a multirange ammeter? Explain.
10. Explain in your own words, the advantage of rectifier type of instruments.
11. Explain in your own words why multimeters are very popular in measurements.
12. "Analog multimeters are a better option than a DMM". Comment in your own words.
13. Explain in your own words the significance of waveform display in a measurement.

14. How can a galvanometer be used as detector in ac measurements?
15. Comment in your words the selection of R_s or R_{sh} in any meter.
16. Using your basic knowledge on half-wave rectifier, can you estimate average dc voltage in a voltmeter using half-wave rectifier. (Hint: refer Fig. 8.6 and Eq. (8.1).
17. On a similar grounds in Question. 16, estimate ac sensitivity.
18. What are the qualities expected for an attenuator?
19. Explain the role of battery in a multimeter.
20. Explain how the trajectory of an electron beam is controlled in the CRO.
21. Draw the basic structure of a cathode ray tube an identify different components.
22. Draw the functional block diagram of the CRO and explain the functions of each block.
23. Explain how a CRO is used in a phase measurement.
24. Given a single-beam oscilloscope, how do you measure the amplitude and frequency of a signal waveform?
25. What is a sweep generator, what are its requirements?
26. What is the trace time and fly-back time in a CRO?
27. List importance of Lissajous patterns.

Exercise Problems

1. A certain current measurement across a resistor of 1000 ohms is 1.25 mA; what is the power consumed by the circuit?
2. If a voltmeter is connected across '*R*' in Problem 1, what is its reading?
3. An ac circuit of unity power factor has a measured power of 250 mW. If the current measured is 100 mA what is the reading on the voltmeter?
4. If the power factor of the circuit is halved in Problem 3, what is the new power?
5. If the resistance of the meter in Example 8.1 is doubled, what is the new power dissipation?
6. If the resistance of the meter in Example 8.2 is halved, what is the new power dissipation?
7. If the series resistance in Example 8.3 is reduced by 20%. What is the new terminal voltage?
8. Design a multirange ammeter with ranges of 10 mA, 20 mA and 500 mA given the meter resistance of 20 Ω and the maximum current of 1 mA.
9. Design a multirange voltmeter with ranges of 10 V, 20 V and 50 V given the meter resistance of 100 Ω and a maximum current of 1 mA.
10. Calculate the value of the multiplier required in series with a full-wave rectifier-type voltmeter given the basic pmmc meter of 100 μA and 1000 Ω. Diodes used are ideal and the meters.
11. Find the meter sensitivity in Problem 10.
12. Find the unknown frequency 'f_H' from the lissajous pattern shown in Fig. P12 in terms of reference frequency 'f'.

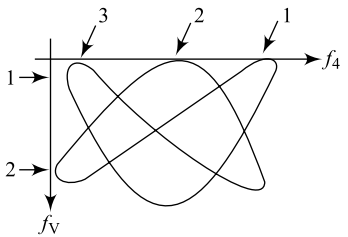


Fig. P.12

13. If the 'f_V' value in Problem 12 is 10 KHz. Find 'f_H'.
14. The lissajous shown in Fig. P.14 refers to two frequencies 'f_V' and 'f_H'; find the value of 'f_y' in terms of 'f_V'.

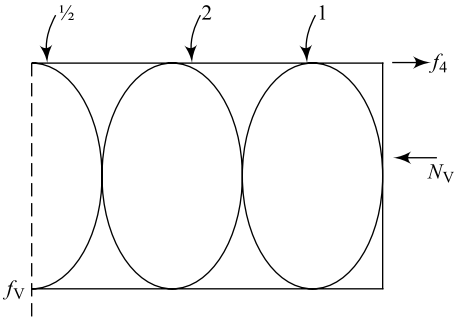


Fig. P.14

15. If 'f_V' is the maximum audio range value in Problem 14, what is the value of 'f_H'?
16. Find the ratio of frequencies of reference and unknown signals in Figure P16.

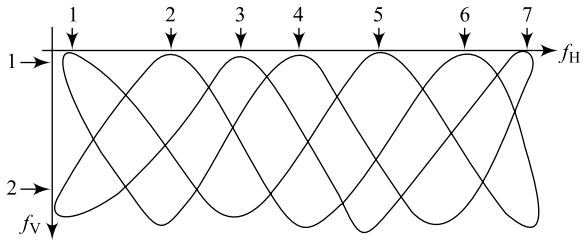


Fig. P.16

17. If the reference frequency in Problem 16 is its times the lower range of audio frequency, what is the value of unknown frequency?

Multiple-Choice Questions

1. The circuit parameters that designers wish to measure.
   (a) Voltage (b) Power (c) Frequency (d) All the above.
2. Power in dc circuit is estimated using equation
   (a) $P_{dc} = VI \cos \phi$ (b) $P_{dc} = VI \sin \phi$ (c) $P_{dc} = VI$ (d) $P_{dc} = I^2V$
3. Power in an ac circuit is measured using equation
   (a) $P_{ac} = VI \cos \phi$ (b) $P_{ac} = VI \sin \phi$ (c) $P_{ac} = P_{dc} \times f$ (d) $P_{ac} = V^2I^2f$
4. In a circuit, a multimeter is used to measure
   (a) current (b) voltage (c) resistance (d) all the above
5. In a circuit, a digital multimeter (DMM) is used to measure
   (a) ac components (b) dc components
   (c) neither (a) nor (b) (d) both (a) and (b)

6. In a circuit, a wattmeter is used to measure
   (a) current (b) power (c) voltage (d) frequency
7. Circuit current is measured using
   (a) ammeter (b) multimeter
   (c) both (a) and (b) (d) neither (a) nor (b)
8. Circuit voltage is measured using
   (a) multimeter (b) voltmeter (c) ammeter (d) both (a) and (b)
9. For circuit measurements using an ammeter and voltmeter,
   (a) the ammeter is connected in series and the voltmeter in parallel.
   (b) the ammeter is connected in parallel and the voltmeter in series
   (c) both are connected in series.
   (d) both are connected in parallel.
10. A PMMC meter contains
    (a) a permanent magnet (b) a moving coil
    (c) a pivotal measurement (d) all the above
11. In order to avoid error parallax, the meter is provided with a _____ beneath the scale.
    (a) mirror (b) LED (c) beeper (d) all the above
12. For meter protection, a voltmeter is provided with
    (a) series resistance R_s (b) shunt resistance R_{sh}
    (c) neither (a) nor (b) (d) both (a) and (b)
13. For meter protection, an ammeter is provided with
    (a) series resistance R_s (b) shunt resistance R_{sh}
    (c) both (a) and (b) (d) neither (a) nor (b)
14. A rectifier type of meter is suitable for measuring
    (a) ac quantity (b) dc quantity
    (c) both (a) and (b) (d) none of the above
15. A DMM contains
    (a) attenuator (b) converter
    (c) analog-to-digital converter (d) all the above
16. Which of the following is a display instrument?
    (a) Ammeter (b) Cathode ray oscilloscope (CRO)
    (c) Voltmeter (d) Wattmeter
17. In a CRO, the _____ is referred to as the heart of the instrument.
    (a) cathode ray tube (CRT) (b) synchronising circuit
    (c) power supply (d) horizontal amplifier
18. In a CRO, the CRT contains
    (a) no filament (b) indirectly heated filament
    (c) directly heated filament (d) indirectly heated cathode
19. In a CRO, the sweep circuit is responsible for
    (a) blanking the display (b) horizontal or *x*-movement of the display
    (c) vertical or *y*-movement of display (d) none

20. In a CRO, the aquadog coating
    (a) provides display colour (b) repels electron beam
    (c) collects and reuses unfocussed electrons (d) none
21. In a CRO, the displacement 'D' of the electron beam produced is
    (a) directly proportional to distance between plates and screen
    (b) directly proportional to length of deflection plates
    (c) indirectly proportional to accelerating anode voltage.
    (d) all the above.
22. In a CRO, the deflection sensitivity 'S' is
    (a) directly proportional to distance between plates and screens
    (b) directly proportional to length of deflection plates
    (c) indirectly proportional to accelerating anode voltage
    (d) all the above.
23. In a CRO, the sensitivity 'S' and displacement 'D' are related through the equation
    (a) $S = D \times V_d$ (b) $S = D \times V_a$ (c) $S = D/V_d$ (d) $S = D/V_a$
24. A CRO may be used to
    (a) display waveforms (b) measure frequency
    (c) measure amplitude (d) all the above
25. In a CRO, the phase difference between two signals can be measured
    (a) using time difference (b) using Lissajous figures
    (c) neither (a) nor (b) (d) both (a) and (b)
26. In a CRO, the input signal frequency can be measured using
    (a) time measurement (b) Lissajous measurements
    (c) both (a) and (b) (d) none of the above
27. In a dual-trace oscilloscope, the control for horizontal signal movement is
    (a) common for both channels (b) separate for both channels
    (c) not present (d) none of the above
28. A CRO is a graphical display instrument that can measure electrical quantities like voltage and frequency of the signal.
    (a) TRUE (b) FALSE
29. A CRO is a graphical display instrument that can measure electrical quantities like phase angle and time period of the signal.
    (a) TRUE (b) FALSE
30. In a CRO, a waveform is moved up or down on the screen by using the _____ control.
    (a) vertical (b) horizontal (c) both (a) and (b) (d) neither (a) nor (b)
31. In a CRO, a waveform is moved left or right on the screen by using the _____ control.
    (a) vertical (b) horizontal (c) both (a) and (b) (d) neither (a) nor (b)

Transducers

9

Goals and Objectives

Upon completion of the chapter, the reader is expected to

- Understand the importance of energy conversion for various electronic applications in everyday life
- Understand the basic objectives of transducers in electronics and instrumentation
- Understand the differences between the two types of transducers (sensors and actuators)
- Gain adequate knowledge on sensors and transducers
- Understand the basics of transducers and gain knowledge about working principle, construction and analysis of transducers
- To give a clear insight about transducer effects in silicon and other materials
- Emphasise on characteristics and response of transducers
- To classify transducers based on different parameters
- To impart basic knowledge about different types of errors and error-reducing techniques of transducers
- To have an adequate knowledge in resistance transducers
- Basic knowledge in inductance, capacitance and piezoelectric transducers
- Understand a realistic model of electrical strain gauges
- Understand the main operating principles of temperature-measurement devices such as thermistors and thermocouples
- To understand and describe the Hall effect
- To give a brief overview of multidisciplinary applications of transducers
- Be able to give an engineering description and dimension to transducers
- Feel confident in selecting a right transducer for any practical application

9.1 INTRODUCTION

Science and technological developments have resulted in sophisticated, high-precision instruments and systems that are very useful in various engineering fields such as medicine, aerospace, oceanography, geology, astronomy, space engineering, etc. A *transducer* is one such device for transforming wave, motion, signal, excitation, oscillation or, in general, one form of energy into another form. This energy conversion may be to or from electrical, electromechanical, electromagnetic, photonic, photovoltaic, or any other form of energy. The word **transducer** is derived from a combination of two words: *trans* means *lead* and *ducer* means *across.* There are two different kinds of transducers: a sensor and an actuator. A **sensor** is used to detect a parameter in one form and report it in another form of energy (usually an electrical or digital signal), for example a tachometer might detect speed or a pressure sensor might detect pressure (a mechanical form of energy) and convert that into an electrical signal. These devices which perform an input function are commonly called sensors because they "sense" a physical change in some characteristic, for example heat or force or pressure or any such quantity and convert that into another form such as an electrical signal.

Figure 9.1 shows process of sensing and actuating during energy conversion. The form of the output signal will often be a voltage analogous to the input signal, though sometimes it may be a waveform whose frequency is proportional to the input or a pulse train containing the information in some other form.

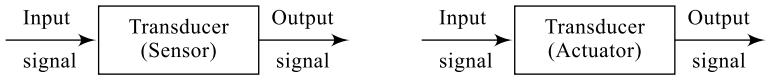


Fig. 9.1 (a) Sensing process (b) Actuating process

An **actuator** is used for the transformation of energy or in other words, an actuator is the one which gets actuated or stands responsible for the output action, in that it converts electrical signal into generally non-electrical energy. An example of an actuator is a loudspeaker which converts an electrical signal into a variable magnetic field and, subsequently, into acoustic waves. These devices which perform an output function are generally called actuators and are used to control some external devices. An actuator accepts energy and produces movement (action). The energy supplied to an actuator might be electrical or mechanical (pneumatic, hydraulic, etc.).

An electric motor and a loudspeaker are both transducers, converting electrical energy into motion for different purposes. Both sensors and actuators are collectively known as transducers because they are used to convert energy of one kind into energy of another kind; for example, a microphone (input device) converts sound waves into electrical signals for the amplifier to amplify, and a loudspeaker (output device) converts the electrical signals back into sound waves. Similarly, an ultrasonic transducer switches back and forth many times a second between acting as an actuator to produce ultrasonic waves, and acting as a sensor to detect ultrasonic waves. There are many different types of transducers commercially available in the market, and the choice of transducers for any application depends upon the quantity being measured or controlled. Table 9.1 gives some of the more commonly used types of transducers as sensors and actuators.

Figure 9.2 shows the complete transduction (sensing and actuating) process in terms of energy conversion. The input stage consists of a system whose energy needs to be converted, a transducer in the form of a sensor. Similarly, the output stage consists of a transducer in the form of an actuator and a system whose input energy needs to be converted. $F_1, F_2, \ldots F_k$ are the signal-conditioning stages that suppress noise signals and help improve the system efficiency by improving signal-to-noise ratio (SNR).

Table 9.1 Types of transducers

Quantity being Measured	Input Devices (Sensors)	Output Devices (Actuators)
Light intensity or level	Light-Dependent Resistor (LDR); Photodiode; Phototransistor; Solar cell	Lights and lamps; LEDs and displays; Fiber optics; Solar lamps; Water heaters, etc.
Temperature level	Thermocouple; Thermistor; Thermostat; Resistive Temperature Detectors (RTD)	Heater; Fan
Force/Pressure level	Strain gauge; Pressure switch; Load cells	Lifts and jacks; Electromagnetic vibration
Position	Potentiometer; Encoders; Reflective/ Slotted ppto-switch; LVDT	Motor; Solenoid; Panel meters
Speed	Tacho-generator; Reflective/Slotted opto-coupler; Doppler effect sensors	ac and dc motors; Stepper motor brake
Sound level	Carbon microphone; Piezoelectric crystal	Bell; Buzzer; Loudspeaker

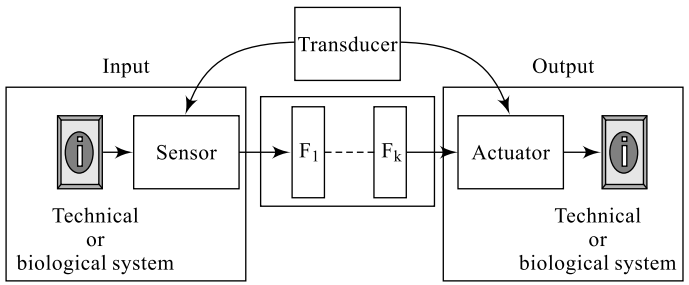


Fig. 9.2 Transduction process

Figure 9.3 shows different possible sources of energy for the complete transduction (sensing and actuating) process in terms of energy conversion. The source of energy may be from different domains such as mechanical, electrical, chemical, magnetic, etc. The modifying unit consists of data acquisition systems such as Analog-to-Digital Convertor (ADC), Digital-to-Analog Convertor (DAC), etc.

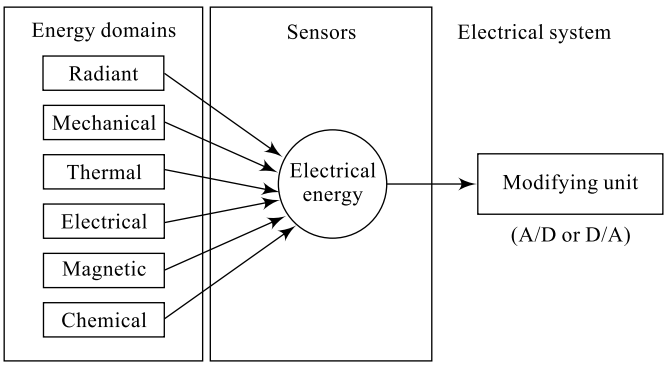
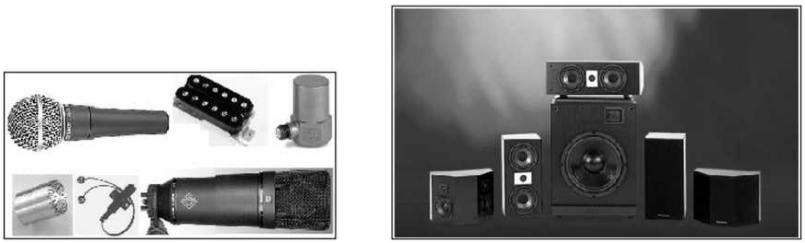


Fig. 9.3 Sources of energy for transduction

Transducers work on the fact that piezoelectric substances create an electric current when struck. This was discovered when certain types of quartz rocks, when struck, generated current. They actually warp slightly as current passes through them. According to the size and shape of the substance, a pulse of sound is emitted. If the substance is small then the sound is in the frequency range (>20,000 Hz) and considered "ultrasound"; if the substance is large enough then the sound will be in the hearing range of humans and we would call it a speaker. This is the basis of all ultrasound transducers. They are extremely high-tech speaker/microphones and because of the small size of the crystals and the brittleness of the materials, they are very fragile. A typical transducer has many crystals. There are many different ways to configure the crystal placement. The important thing to remember is that in each transducer cable there may be one or two wires per crystal. The crystal count per transducer can be very high (as high as 512 in many cases) with which one can imagine how small and fragile these connecting wires become. To give a small idea, in a cable of about 7 cm diameter, 100 wires as small as a lead pencil refill (0.7 mm) may be accommodated. These wires have to be extremely small and still have a coating of insulation. Earlier, a transducer with 128 crystals was about as thick as an average thumb and quite stiff and sturdy; but now transducers with 512 crystals routinely have cables as small as the little finger and are quiet flexible. Transducer crystals are cut from a block of piezoelectric material with a saw blade so fine that it can cut a human hair end (split ends) four to seven times. The electrical connections are generally hand-soldered (up to over 1000 times in a transducer) and these are the reasons that transducers are somewhat expensive. Simple standalone electronic circuits can be made to repeatedly flash a light or play a musical note, but in order for an electronic circuit or system to perform any useful task or function, it needs to be able to communicate with the "real world" whether this is by reading an input signal from an "ON/OFF" switch or by activating some form of output device to illuminate a single light. The type of input or output device used really depends upon the type of signal or process being "sensed" or "controlled". Transducers can be used to sense a wide range of different energy forms such as movement, electrical signals, radiant energy, thermal or magnetic energy, etc. and there are many different types of both analogue and digital input and output devices available to choose from. Some are transducers (loudspeakers, microphones, pickups, accelerometer).

Figure 9.4 shows different commercially available transducers both in the form of sensors and actuators, wherein the main concern is with electro-*mechano*-acoustic transduction. Transducer signals can be captured directly by USB, parallel or serial computer ports or by sound cards. Data acquisition can also be done with DAQ cards made especially for that purpose. Some signals are also transmitted to the computer wirelessly. Scientists and engineers often write their own programs in languages such as BASIC or C++ to capture and manipulate transducer signals. Other options include commercial software such as LabView or Matlab, or freeware such as Glove or Visual Analyser.



(a) Practical actuators (b) Practical sensors

Fig. 9.4 Commercial transducers

9.2 CLASSIFICATION OF TRANSDUCERS

Transducers may be classified into a variety of classes based on different parameters such as form of input-output energy used, kind of function they perform, whether self-generating or not, primary or secondary type, etc.

Based on the input/output energy sources used, transducers may be classified into the following types:

1. Electromagnetic transducers
2. Electromechanical transducers
3. Electro-acoustic transducers
4. Photoelectric transducers
5. Electrostatic transducers
6. Thermoelectric transducers

Based on the location they are placed and the function they are performing in a system, transducers may be classified into the following types;

1. Input transducers, e.g. microphones
2. Output transducers, e.g. speakers

Based on the location they are placed and the function they are performing in a system, transducers may also be classified into the following types:

1. Sensing transducers (sensor), e.g. microphones
2. Actuating transducers (actuator), e.g. speakers

Based on the power generated for their operation, transducers may be classified into the following types:

1. Active Transducers e.g. solar cells, thermocouples, piezoelectric elements. Active transducers are also called self-generating transducers.

2. Passive Transducers e.g. speakers, strain gauges, thermal resistors, liquid-crystal displays. Passive transducers are also called **modulating transducers**.

Based on the type of output signal they generate, transducers may be classified into the following types:

1. Analog transducers, e.g. thermocouple
2. Digital transducers, e.g. light sensors

It is important to choose transducers that have the desired frequency, bandwidth, and focusing to optimise inspection capability. Most often, the transducer is chosen either to enhance the sensitivity or resolution of the system. Based on the type of application, transducers may be classified into the following types:

1. Contact Transducers Establish firm contact with I/O devices

2. Immersion Transducers Immersion transducers are typically used inside a water tank (thermocouples) in scanning applications.

3. Delay-line Transducers They are designed for use in applications such as high-precision thickness gauging of thin materials and de-lamination checks in composite materials.

4. Paintbrush Transducers They are useful for collecting data for industrial or scientific purposes. Additional tasks include signal processing and manipulation, and instrument and process control.

Transducers that detect or transmit information include common items such as microphones, Geiger meters, potentiometers, pressure sensors, thermometers and antennas. A microphone, for example, converts sound waves that strike its diaphragm into an analogous electrical signal that can be transmitted over wires. A pressure sensor turns the physical force being exerted on the sensing apparatus into an analog reading that can be easily represented. While many people think of transducers as being some sort of technical device, once you start looking for them, you will find transducers everywhere in your everyday life. Most transducers have an inverse that allows for the energy to be returned to its original form. Audio cassettes, for example, are created by using a transducer to turn the electrical signal from the microphone pick-up—which in turn went through a transducer to convert the sound waves into electrical signal—into magnetic fluctuations on the tape head. These magnetic fluctuations are then read and converted by another transducer—in this case a stereo system—to be turned back into an electrical signal, which is then fed by a wire to speakers, which act as yet another transducer to turn the electrical signal back into audio waves. Other transducers turn one type of energy into another form, not for the purpose of measuring something in the external environment or to communicate information, but rather to make use of that energy in a more productive manner. A light bulb, for example, one of the many transducers around us in our day-to-day lives, converts electrical energy into visible light. Electric motors are another common form of electromechanical transducer, converting electrical energy into kinetic energy to perform a mechanical task. The inverse of an electric motor, a generator, is also a transducer, turning kinetic energy into electrical energy that can then be used by other devices. Some important transducer types are discussed in the following sections.

9.3 CAPACITIVE TRANSDUCERS

A capacitive transducer employs a diaphragm positioned between two fixed metal plates as indicated in Fig. 9.5(a). The principle of operation of a capacitive transducer is directly derived from the basic capacitance equation represented in Eq. (9.1) which is represented based on Fig. 9.5(b). The capacitance of a parallel-plate capacitor is dependent on the plates' dimensions and characteristics of the dielectric material and the media between the plates.

In some designs, the metal plates are fixed to either side of the diaphragm; deflection of the diaphragm changes the capacitive coupling between the diaphragm and the metal plates. In other designs,

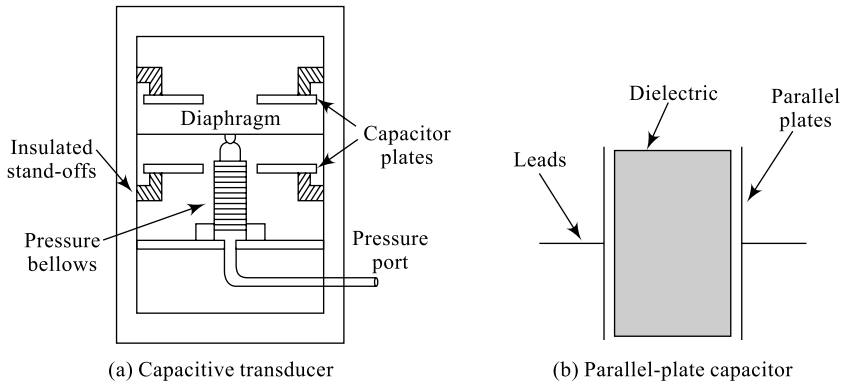


Fig. 9.5 Capacitive transducer

the metal plates are isolated from the moving diaphragm; deflection of the diaphragm causes a change in the capacitive coupling between the two metal plates. An alternating current (ac) signal across the plates can be used to sense the change in capacitance.

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \text{ farads} \tag{9.1}$$

The capacitance value C may be changed by changing A, the plate area or d, the plate separation or ε_r, the relative permittivity of the dielectric material. Capacitances are constructed using any of these principles; the sensitivity S of such a transducer is then given by Eq. (9.2). Here, δx is the displacement in metres and δC is the incremental change of the capacitance value in farads.

$$S = \frac{\delta C \ F}{\delta x \ m} \tag{9.2}$$

Similarly, capacitive transducers may be constructed using cylindrical capacitors, cantilevers, quartz diaphragms, etc. Capacitive transducers offer system designers a good number of advantages—they are very sensitive, have high input impedance, good frequency response, and are very useful in small system designs. Due to these advantages, capacitive transducers find applications in force, pressure, displacement (both linear and angular), humidity, liquid-level measurements, etc. However, capacitive transducers are hampered by some major disadvantages; smaller values of C results in larger impedances, loading effect is more at low operating frequencies, and frequency response is nonlinear and affected by the edge effects, metallic plates and parts of the capacitor.

9.4 INDUCTIVE TRANSDUCERS

An inductive transducer is mainly used for the measurement of displacement. An inductive transducer is an active transducer and operates on the principle that the relative motion between a conductor and a magnetic field induces a voltage in the conductor. This voltage is due to the self-inductance or mutual inductance of the coil as indicated in Fig. 9.6. In an inductive transducer, pressure-induced displacements of a diaphragm cause a change in the self-inductance of a single coil. If the displacements occur in the magnetic coupling between a pair of coils, it is called a reluctive transducer. Because the pressure-induced electrical output signal requires relative motion, the inductive design is limited to dynamic measurements. In a reluctive transducer, displacements occur in the magnetic coupling between a pair of coils.

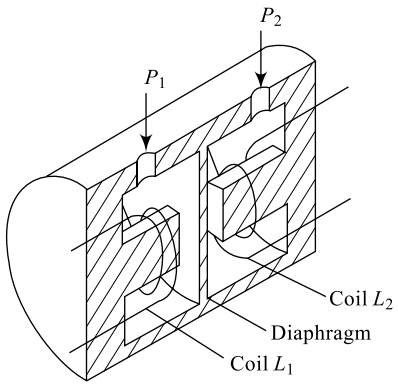


Fig. 9.6 Inductive or active transducer

The principle of operation of an inductive transducer is given by Eq. (9.3) which is dependent on the coil characteristics like number of turns, cross-sectional area, length, etc.

$$L = \frac{N^2}{R} = \frac{N^2 \mu A}{l} \text{ henries} \tag{9.3}$$

It is clear from the equation that L may be varied by varying the length of the coil l, number of turns N, cross-sectional area A or the permeability of the medium μ. An inductive transducer can also be

constructed based on the mutual inductance principle and the mutual inductance between two coils is given by Eq. (9.4); where L_1 and L_2 are the self-inductances of two coils and K is the coupling coefficient between them.

$$L_M = K\sqrt{L_1 L_2} \text{ henries} \tag{9.4}$$

Reluctive Transducer

A reluctive transducer is a passive transducer and requires external ac excitation of a pair of coils. It operates on the principle that the magnetic coupling between the two coils is affected by the displacement of a pressure-driven conductor located in the magnetic field between the two coils. As indicated in Fig. 9.7, the conductor is either connected to a force-summing device or is itself a force-summing device.

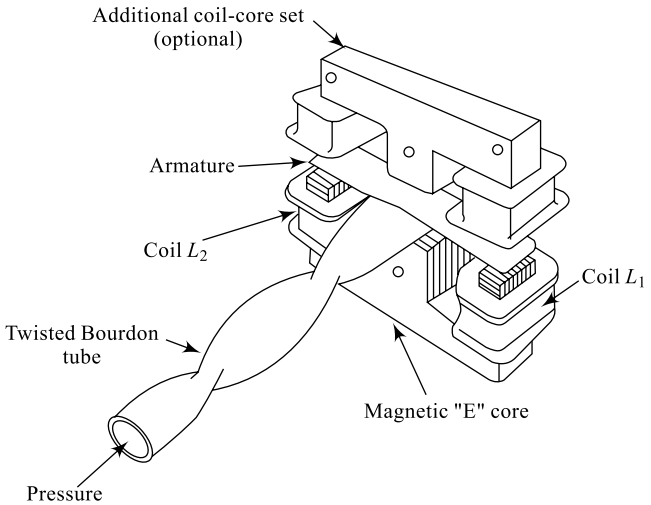
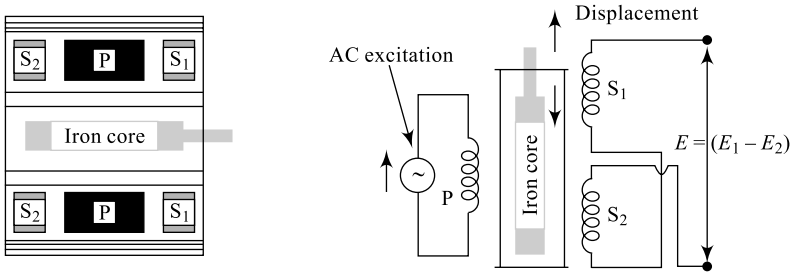


Fig. 9.7 Reluctive or passive transducer

The most commonly used type of variable inductance transducer is the linearly variable differential transducer presented in Section 9.5.

9.5 LINEARLY VARIABLE DIFFERENTIAL TRANSDUCER (LVDT)

A linearly variable differential transducer, popularly called LVDT, is the most commonly used type of variable inductance transducer and is primarily used to convert a linear displacement into an electrical signal. A linearly variable differential transducer consists of a transformer with one primary winding and two secondary windings as indicated in Fig. 9.8. The primary winding P is supplied with an ac source in the audio range (up to 20 kHz) and the two secondary windings with equal number of turns on them are placed on either side of P. The secondary windings are wound on a cylindrical tube inside which a soft-iron core with high permeability is mounted; the displacement under measurement is applied to this iron core. The entire set-up is placed in a steel box containing shielded leads.



(a) LVDT (b) LVDT circuit

Fig. 9.8 Linearly Variable Differential Transducer (LVDT)

The alternating magnetic field produced due to the ac source applied to the primary winding induces secondary voltage in the two coils S_1 and S_2; the magnitude of this voltage depends on the amount of primary excitation. The two output voltages E_1 and E_2 are suitably combined (series connection) to give a single output voltage E, given by Eq. (9.5). When the iron core is in its normal (zero) position, the magnitudes of E_1 and E_2 are equal and hence $E = 0$. With a displacement applied to the arm of the iron core, the position of the arm results in

$$\boldsymbol{E = E_1 - E_2} \tag{9.5}$$

a voltage E dependent on magnitudes of E_1 and E_2; $E_1 > E_2$ if the arm moves up and $E_1 < E_2$ if the arm is moved down. Thus, the output voltage produced is proportional to the displacement, or in other words the linear motion. The sensitivity of LVDT is given by

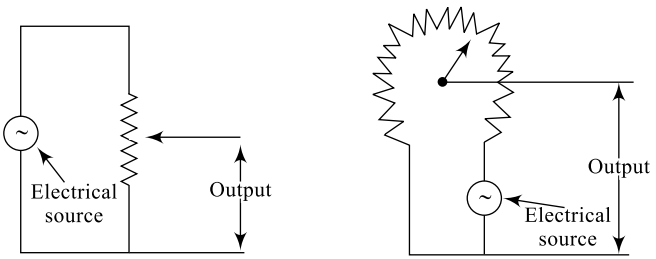
$$S = \frac{\text{Output voltage}}{\text{Displacement}} \tag{9.5a}$$

9.6 POTENTIOMETRIC TRANSDUCER

A potentiometric transducer is a passive type of transducer wherein a resistive potentiometer or a variable resistance component or a POT with sliding contact forms the main block. A POT needs an external power source for its operation and is available in different forms such as linear translational, rotational, helical, etc. Of them, translational and rotational are very popular and are shown in Fig. 9.9.

$$\Delta R = \frac{\rho l}{A}\Omega \tag{9.6}$$

These transducers for their operation depend on the incremental change in the resistance ΔR given by Eq. (9.6): l is the length of resistive wire in metres, A is its area in metre-square and ρ is the resistivity



(a) Linear translational transducer (b) Rotational transducer

Fig. 9.9 Potentiometric transducer

in ohm-metre. Potentiometric transducers are generally preferred because of the reason that a resistor is equally sensitive to both ac and dc excitations. The sensitivity of a potentiometric transducer is given by Eq. (9.7).

$$S = \frac{\text{Output}}{\text{Input}} = \frac{V_o}{V_i} \tag{9.7}$$

9.7 PIEZOELECTRIC TRANSDUCER

Piezoelectric devices contain special crystals and these crystals produce a voltage if a pressure is applied to them in one direction. This potential is a result of displacement of charges. As an inverse operation, if a potential is applied across the crystal, the shape of the crystal can be changed. This property of the materials is called piezoelectric property and the materials exhibiting this property are called **piezoelectric** *or* **electro-resistive materials,** indicated in Fig. 9.10. A common use of piezoelectric devices is in buzzers, which produce a buzzing noise when a voltage is applied.

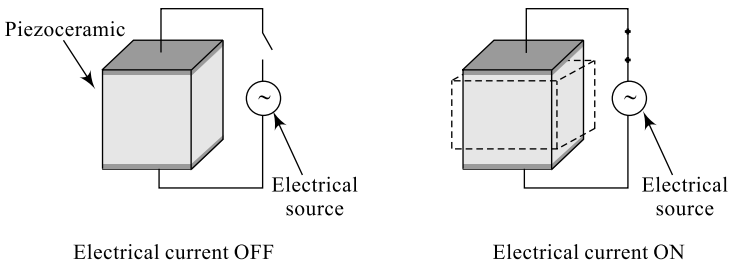
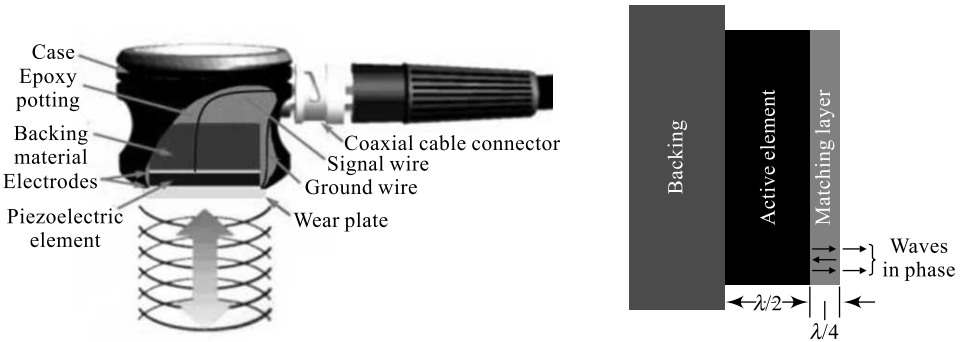


Fig. 9.10 Piezoelectric material

The active element is the heart of the transducer as it converts the electrical energy to acoustic energy, and vice versa. The active element is basically a piece of polarised material (i.e. some parts of the molecule are positively charged, while other parts of the molecule are negatively charged) with electrodes attached to two of its opposite faces. When an electric field is applied across the material, the polarised molecules will align themselves with the electric field, resulting in induced dipoles within the molecular or crystal structure of the material. This alignment of molecules will cause the material to change dimensions. This phenomenon is known as **electrostriction**. In addition, a permanently polarised material such as quartz (SiO_2) or barium titanate ($BaTiO_3$) will produce an electric field when the material changes dimensions as a result of an imposed mechanical force. This phenomenon is known as the **piezoelectric effect**. The active element of most acoustic transducers used today is a piezoelectric ceramic, which can be cut in various ways to produce different wave modes. A large piezoelectric ceramic element can be seen in the image of a sectioned low-frequency transducer. Preceding the advent of piezoelectric ceramics in the early 1950's, piezoelectric crystals made from quartz crystals and magnetostrictive materials were primarily used. When piezoelectric ceramics were introduced, they soon became the dominant material for transducers due to their good piezoelectric properties and their ease of manufacture into a variety of shapes and sizes. They also operate at low voltage and are usable up to about 300°C. The first piezoceramic in general use was barium titanate, and that was followed during the 1960's by lead zirconate titanate compositions, which are now the most commonly employed ceramic for making transducers. New materials such as piezopolymers and composites are also being used in some applications. The thickness of the active element is determined by the desired frequency of the transducer. A thin wafer element vibrates with a wavelength that is twice its thickness. Therefore, piezoelectric crystals are cut to a thickness that is 1/2 the desired radiated wavelength. The higher the

frequency of the transducer, the thinner the active element. The primary reason that high-frequency contact transducers are not produced is because the element is very thin and too fragile. The transducer is a very important part of the ultrasonic instrumentation system and it incorporates a piezoelectric element, which converts electrical signals into mechanical vibrations (transmit mode) and mechanical vibrations into electrical signals (receive mode). Many factors, including material, mechanical and electrical construction, and the external mechanical and electrical load conditions, influence the behaviour of a transducer. Mechanical construction includes parameters such as the radiation surface area, mechanical damping, housing, connector type and other variables of physical construction.



(a) Piezoelectric transducer (a) Piezoelectric transducer

Fig. 9.11 Piezoelectric transducer

A cut-away of a typical piezoelectric contact transducer is shown in Fig. 9.11. To get as much energy out of the transducer as possible, an impedance matching is placed between the active element and the face of the transducer. Optimal impedance matching is achieved by sizing the matching layer so that its thickness is 1/4 of the desired wavelength. This keeps waves that were reflected within the matching layer in phase when they exit the layer. For contact transducers, the matching layer is made from a material that has an acoustical impedance between the active element and steel. Immersion transducers have a matching layer with an acoustical impedance between the active element and water. Contact transducers also incorporate a wear plate to protect the matching layer and active element from scratching. The backing material supporting the crystal has a great influence on the damping characteristics of a transducer. Using a backing material with impedance similar to that of the active element will produce the most effective damping. Such a transducer will have a wider bandwidth resulting in higher sensitivity. As the mismatch in impedance between the active element and the backing material increases, material penetration increases but transducer sensitivity is reduced.

If a pressure 'p' is applied across the crystal of thickness 't', the output voltage produced is given by

$$V_0 = \text{'}s\text{'} \times t \times p \tag{9.7a}$$

Here 's' is crystal sensitivity which is defined as the ratio of electric field to applied stress pressure.

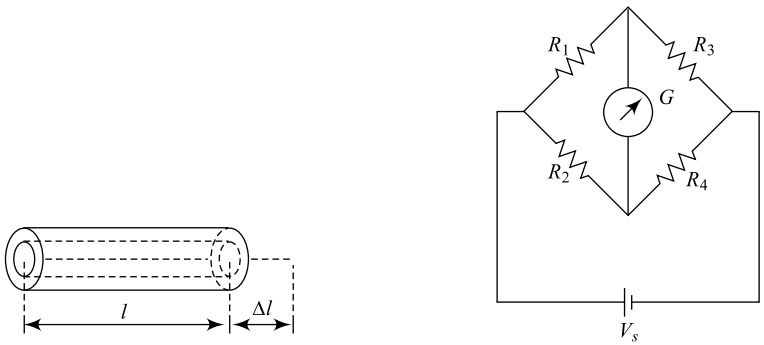
i.e.
$$\text{s} = \frac{E}{P} \tag{9.7b}$$

9.8 ELECTRICAL STRAIN GAUGES

When a metallic conductor is either stretched (elongated) or compressed by applying a longitudinal stress, the conductor will be deformed and this deformation results in change in resistance of the conductor; this is indicated in Eq. (9.6). Rewriting this equation as in Eq. (9.8)

$$R = \frac{\rho l}{A}\Omega \tag{9.8}$$

with usual notations, the resistance R of the conductor is dependent on l, the length of resistive wire in metres. A is its area in metre-square and ρ is the resistivity in ohm-metre. This is the operating principle for any resistive transducer and in particular for a strain gauge; this is indicated in Fig. 9.12(a). This change in resistance can be accurately measured using a resistance bridge such as a Wheatstone bridge as shown in Fig. 9.12(b).



(a) Strain-gauge principle (b) Wheatstone bridge

Fig. 9.12 Strain gauge

The performance of the gauge is measured using a factor called *gauge factor* G_F and is given by Eq. (9.9). Here, $\in$ is called *strain* of the device.

$$G_F = \frac{\frac{\Delta R}{R}}{\frac{\Delta L}{L}} = \frac{\frac{\Delta R}{R}}{\in} \tag{9.9}$$

The materials used for construction of strain gauges should have some specific characteristics in order that the strain gauge offers good performance; for example, the wire used should have high specific resistance, low temperature coefficient, reasonably constant gauge factor and reasonably constant strain-sensitivity over a wide range of strain ($\in$).

Table 9.2 indicates different types of materials and their characteristics such as temperature coefficient (TC), gauge factor (G_F) and resistivity.

Table 9.2 Properties of different wire materials for strain gauges

Material	TC/°C	G_F	ñ Ù-m
Platinum	$+40 \times 10^{-4}$	4.8	10×10^{-8}
Nickel	$+68 \times 10^{-4}$	–12	6.5×10^{-8}
Karma alloy	$+0.2 \times 10^{-4}$	2.1	125×10^{-8}
Nichrome alloy	1×10^{-4}	2.1 to 2.5	100×10^{-8}
Constantan Advance alloy	$\pm 0.2 \times 10^{-4}$	2.1	48×10^{-8}

Similarly, Table 9.3 indicates different types of backing materials, the adhesive/bonding cement that are useful in strain-gauge manufacturing along with their temperature ranges.

Table 9.3 Temperature ranges for different backing, adhesive and bonding materials

Material	Adhesive/Cement	Temperature Range
Paper	$+40 \times 10^{-4}$	0 to 60°C
Epoxy Paper/Phenolic	$+68 \times 10^{-4}$	–12
Phenolic fibre glass	$+0.2 \times 10^{-4}$	2.1
Transfer gauge	1×10^{-4}	2.1 to 2.5

There are various forms of strain gauges commercially available and a few of them are listed here: wire gauges, foil gauges, thin-film gauges, semiconductor strain gauges, etc.

9.9 THERMISTORS, THERMOCOUPLES AND HALL EFFECT

9.9.1 Thermistors

Thermistors are variable resistors meaning that their resistance varies with temperature. Like other resistive transducers which are sensitive to a form of energy, thermistors are sensitive to temperature. For most practical purposes, within limited temperature ranges, the resistance-temperature relationship may be written as in Eq. (9.10).

$$R_2 = R_1(1 + \alpha (t_2 - t_1)) = R_1(1 + \alpha \Delta t) \tag{9.10}$$

Here, R_1 is thermistor resistance at temperature t_1, R_2 is thermistor resistance at temperature t_2 and α is temperature coefficient. Resistivity ρ of pure metals and most alloys (some exceptions like carbon alloy) is directly related to temperature changes and hence they have positive α. Resistivity ρ of some materials is indirectly related to temperature changes and hence they have negative α. The resistance of a positive temperature coefficient (+ve α) device increases with increasing temperature and its resistance decreases with decreasing temperature. The resistance of a negative temperature coefficient (–ve α) device decreases with increasing temperature and its resistance increases with decreasing temperature. Table 9.4 indicates temperature coefficients of some popular materials that are useful as thermistors.

Table 9.4 Temperature coefficients of different materials

Material	α value/°C
Platinum	+0.00392
Nickel	+0.0041
Copper	+0.0043
Iron	+0.002 to +0.006
Thermistors	–0.02 to –0.09

Applications of Thermistors

Thermistors are very useful for measurement of temperature, control of temperature, compensation for temperature, measurement of high-frequency power and vacuum.

9.9.2 Thermocouples

1. Analogue Sensors

When two different metals produce a continuous output signal or voltage, it is generally proportional to the quantity being measured. Physical quantities such as temperature, speed, pressure, displacement, strain, etc. are all analogue quantities as they tend to be continuous in nature. For example, the temperature of a liquid can be measured using a thermometer or thermocouple which continuously responds to temperature changes as the liquid is heated up or cooled down.

Thermocouple used to Produce an Analogue Signal

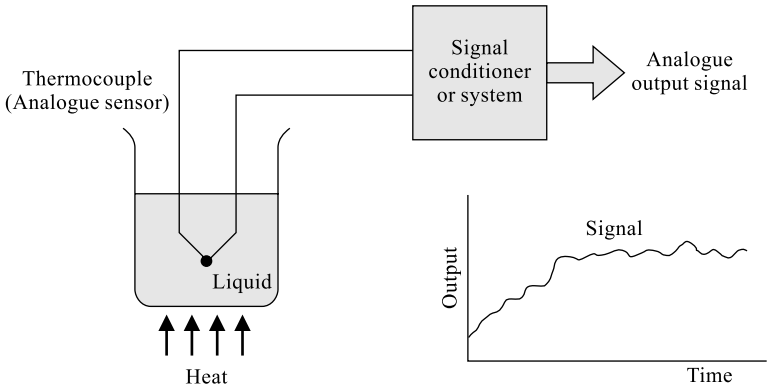


Fig. 9.13 Thermocouple as a transducer

Analogue sensors tend to produce output signals which are slow changing and very small in value. So some form of amplification is required. Also analogue signals can be easily converted into digital signals for use in microcontroller systems by the use of analogue-to-digital converters.

2. Digital Sensors

As its name implies, **digital sensors** produce a discrete output signal or voltage that is a digital representation of the quantity being measured. Digital sensors produce a *binary* output signal in the form of logic 1 or logic 0 (ON or OFF). This means then that a digital signal only produces discrete (noncontinuous) values which may be outputted as a single *bit* (serial transmission), or by combining the bits to produce a single *byte* output (parallel transmission).

Light Sensor used to Produce a Digital Signal

In our simple example above, the speed of the rotating shaft is measured by using a digital LED/Opto-detector sensor. The disc which is fixed to the shaft has a number of transparent slots within its design. As the disc rotates with the speed of the shaft, each slot passes by the sensor in turn producing an output pulse representing a logic level 1. These pulses are sent to a register or counter and finally to an output display to show the speed or revolutions of the shaft. By increasing the number of slots or *windows* within the disc, more output pulses can be produced giving a greater resolution and accuracy as fractions of a revolution can be detected. Then this type of sensor could also be used for positional control.

In most cases, sensors, and more specifically analogue sensors, generally require an external power supply and some form of additional amplification or filtering of the signal in order to produce a suitable

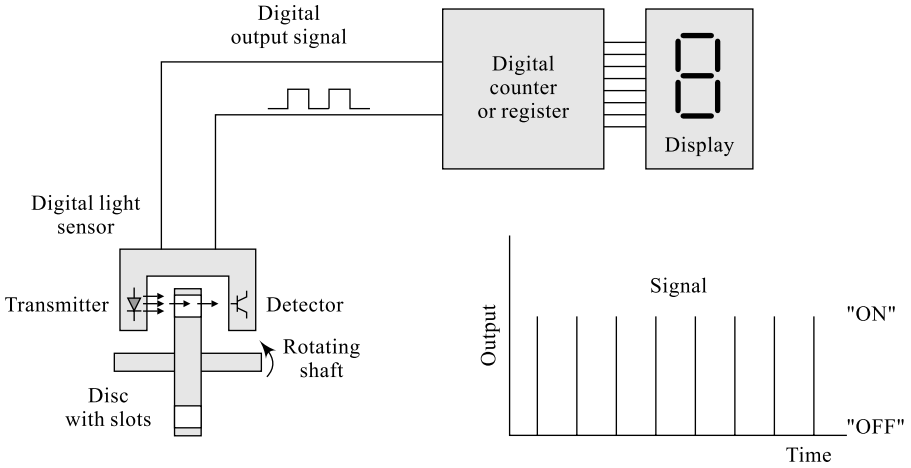


Fig. 9.14 Thermocouple as a transducer

electrical signal which is capable of being measured or used. One very good way of achieving both amplification and filtering within a single circuit is to use *operational amplifiers* as seen before.

9.9.3 Hall Effect and Hall Effect Transducers

When a strip of conductor carrying current is traversed in a magnetic field, an EMF (ElectroMagnetic Force) is generated between the ends of the conductor. The magnitude of this emf is proportional to the flux density of the magnetic field, magnitude of the current flowing through the conductor and the Hall effect coefficient $\boldsymbol{K_H}$ of the material. This property of the material is termed as the Hall effect and finds an extensive use in measuring instruments such as flux meters, ammeters, wattmeters, etc. The value of Hall effect coefficient $\boldsymbol{K_H}$ depends on the conductor properties such as charge mobility and charge density.

Figure 9.15 indicates the principle of a Hall-effect transducer; a strip of Hall-effect conductor of thickness 't' and carrying current 'I' is placed in a magnetic field. There will be no potential developed across the terminals of the Hall strip when there is no magnetic field. When a transverse magnetic field is applied, a voltage is developed across the terminals of the Hall Conductor given by Eq. (9.11).

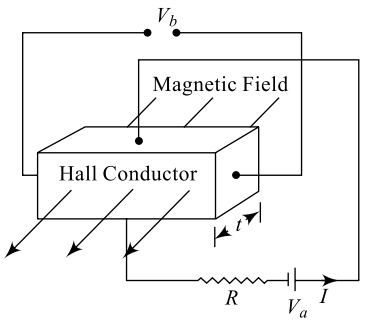


Fig. 9.15 Hall-effect transducer

$$V_b = \frac{B \times I \times K_H}{t} \tag{9.11}$$

Here, K_H is the Hall-effect coefficient, the units of which are given by Eq. (9.12).

$$K_H \text{ is in terms of } \frac{V_\alpha - m}{A - \frac{\text{Wb}}{\text{m}^2}} \tag{9.12}$$

Thus, using Eq. (9.13) the current 'I' or the magnetic field strength 'B' may be measured in terms of the output voltage 'V_b' produced; however, the magnitude of this emf is very small in most of the Hall-effect materials. Table 9.5 indicates some of the commonly used materials for Hall-effect transducers and their Hall-effect coefficient values for a given field strength in Wb/m^2 at around 20°C temperature. It can be seen from Table 9.5 that the Hall effect emf is in semiconductor materials such as Ge and Si.

Table 9.5 Applications of transducers from different Energy domains

Sl. No.	Material	Field Strength in Wb/m^2	K_H Value
1	Si	2.0	4.1×10^{-6}
2	Ge	0.8	-8×10^{-3}
3	Fe	1.7	1.1×10^{-9}
4	Cu	2.2	-52×10^{-12}
5	As	0.8	4.52×10^{-9}

Hall-Effect Transducer Applications

Hall-effect transducers find extensive applications in the following:

(i) Measurement of magnetic fields (magnetic to electric transducer)
—Produces an output voltage proportional to the magnetic field

(ii) Measurement of current (electric to magnetic transducer)
—Produces a magnetic field proportional to the current flowing

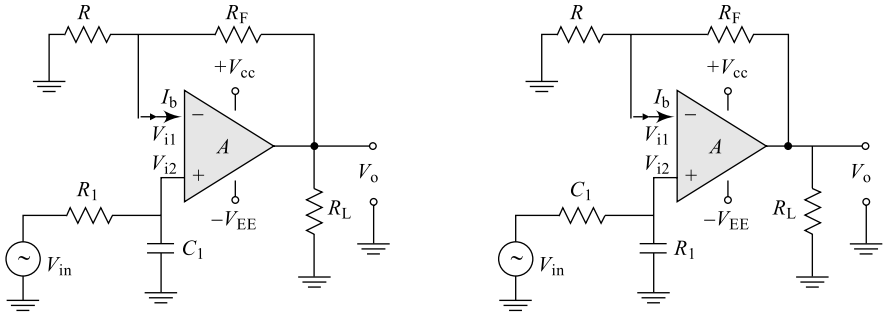
(iii) Measurement of displacement (magnetic to electric transducer)
—Produces an output voltage proportional to the magnetic field

(iv) Measurement of power (magnetic to electric transducer)
—Produces an output power proportional to the magnetic field

9.9.4 Signal Conditioning

As we saw in Chapter 6, an *operational amplifier* can be used to provide amplification of signals when connected in either inverting or non-inverting configurations. The very small analogue signal voltages produced by a sensor (few microvolts or millivolts) can be amplified many times by a simple op-amp circuit to produce a much larger voltage signal (5 V or 10 V) the amplified signal can then be used as input to a microprocessor-based system. When using sensors, generally some form of amplification (gain), impedance matching or perhaps phase shifting may be required before the signal can be used. This is conveniently performed by operational amplifiers and is called signal conditioning.

Also, when measuring very small physical changes, the output signal of a sensor can become *contaminated* with unwanted signals or voltages that prevent the actual signal required from being measured correctly. These unwanted signals are called **noise**. This noise, or interference, can be either greatly reduced or even eliminated by using signal conditioning or filtering techniques as discussed in Section 6.16, the *active filter*. Figure 9.16 indicates few such active filters. By using *low-pass*, *high-pass* or even *bandpass* filters the bandwidth of the noise can be reduced to leave just the output signal required. For example, many types of inputs from switches, keyboards or manual controls are not capable of changing state rapidly and so low-pass filters can be used. When the interference is at



(a) Low-pass filter circuit (b) High-pass filter circuit

Fig. 9.16 Active filters for signal conditioning

a particular frequency, for example mains frequency, narrowband reject or **notch filters** can be used. Where some random noise still remains after filtering, it may be necessary to take several samples and then average them to give the final value, hence increasing the Signal-to-Noise Ratio (SNR, a figure of merit to measure the quality of a signal).

Either way, both amplification and filtering play an important role in interfacing microprocessor and electronics based systems to real-world conditions.

9.9.5 Transducer Testing

Some transducer manufacturers have a lead in the development of transducer characterisation techniques and have participated in developing the methods for testing single-element pulse-echo ultrasonic transducers as well as for evaluating characteristics of ultrasonic search units. Additionally, some manufacturers perform characterisations according to many industrial and military standards. As part of the documentation process, an extensive database containing records of the waveform and spectrum of each transducer is maintained and can be accessed for comparative or statistical studies of transducer characteristics. Manufacturers often provide time-and frequency-domain plots for each transducer.

1. Transducer Efficiency

Some transducers are specially fabricated to be more efficient transmitters and others to be more efficient receivers. A transducer that performs well in one application will not always produce the desired results in a different application. For example, sensitivity to small defects is proportional to the product of the efficiency of the transducer as a transmitter and a receiver. Resolution, the ability to locate defects near the surface or in close proximity in the material, requires a highly damped transducer. As in all energy conversions, some energy is lost when transducers operate. The efficiency of a transducer is found by comparing the total energy input to the total energy coming out of the system. Some transducers are very efficient, while others are extraordinarily inefficient. A radio antenna, for example, acts as a transducer to turn radio frequency power into an electromagnetic field; when operating well, this process is upwards of 80% efficient. Most electrical motors, by contrast, are well under 50% efficient, and a common lightbulb, because of the amount of energy lost as heat, is less than 10% efficient. Transducer efficiency is measured as the ratio of output power generated in desired form to total input power. Mathematically, if Q represents the power output in desired form and P represents the total power input then the efficiency E is given by Eq. (9.13).

$$E = Q/P \tag{9.13}$$

No transducer is 100% efficient. Some power is always lost in the conversion process. Usually, this loss is manifested in the form of heat. Some antennas approach 100% efficiency. The worst transducers in case of efficiency are incandescent lamps. A 100 W lamp radiates only a few watts of visible light. Most of the power is dissipated as heat.

2. Transducer Applications

Table 9.6 indicates some of the available transducers along with their applications and type of transduction. The form of input energy and the output energy are also indicated.

Table 9.6 Transducers and applications

Sl. No.	Transducer	Energy Domain	Application
1	Antenna	Electromagnetic	Converts electromagnetic waves into electric current and vice versa
2	Cathode Ray Tube (CRT)	Electromagnetic	Converts electrical signals into visual form
3	Fluorescent lamp, lightbulb	Electromagnetic	Converts electrical power into visible light
4	Magnetic cartridge	Electromagnetic	Converts motion into electrical form
5	Photodetector or Photoresistor (LDR)	Electromagnetic	Converts changes in light levels into resistance changes
6	Cassette player; Tape head	Electromagnetic	Converts changing magnetic fields into electrical form
7	pH probes	Electrochemical	
8	Load cell	Electromechanical	Converts force to mV/V electrical signal using strain gauge
9	Galvanometer	Electromechanical	Converts electrical signal to displacement
10	Loudspeaker, earphone	Electro-acoustic	Converts electrical signals into sound
11	Human ear	Electro-acoustic	Converts sound into electrical signals
12	Microphone	Electro-acoustic	Converts sound into an electrical signal
13	Laser diode, light-emitting diode	Photoelectric	Convert electrical power into forms of light
14	Photodiode, photoresistor, phototransistor, LASCR	Photoelectric	Converts changing light levels into electrical form
15	RTD (Resistance Temperature Detector)	Thermoelectric	Converts changing heat levels into electrical (resistance) form
16	Thermocouple	Thermoelectric	Converts changing heat levels into electrical (resistance) form
17	Thermistor	Thermoelectric	Converts changing heat levels into electrical (resistance) form

3. Some Transducer Manufacturers

Temposonics™ Transducers are available from MTS System Corporation, Sensors Division, 3001 Sheldon Drive, Cary, NC 27513, 800-633-7609. Some transducer manufacturers have lead in the development of transducer characterisation techniques and have participated in developing the AIUM

Standard Methods for Testing Single-Element Pulse-Echo Ultrasonic Transducers as well as ASTM-E 1065 Standard Guide for Evaluating Characteristics of Ultrasonic Search Units. Additionally, some manufacturers perform characterisations according to AWS, ESI, and many other industrial and military standards. Often, equipment in test labs is maintained in compliance with MIL-C-45662A Calibration System Requirements.

Summary

- The process of converting one form of energy into another form of energy is transduction and the device is called transducer.
- A transducer can be in the form of a sensor or actuator.
- A transducer may use various sources of input energy such as mechanical, electrical, chemical, magnetic, etc.
- Transducers can be classified into input transducers and output transducers based on the location they are placed and the function they are performing in a system.
- Transducers can also be classified into sensor transducers and actuator transducers based on the location they are placed and the function they are performing in a system.
- Transducers can be classified into different types based on forms of input/output energy as electromagnetic transducers, electromechanical transducers, electro-acoustic transducers, photoelectric transducers, electrostatic transducers, thermoelectric transducers, etc.
- Based on the power generated for their operation, transducers may be classified into active transducers and passive transducers.
- Based on the type of output signal they generate, transducers may be classified into analog transducers and digital transducers.
- Based on the type of application, transducers may be classified into contact transducers, immersion transducers, delay-line transducers, paintbrush transducers, etc.
- The principle of operation of a capacitive transducer is based on the equation represented in Eq. (9.1) which is dependent on the plates' dimensions and characteristics of the dielectric material and the media between the plates.
- The capacitance value C of a capacitive transducer may be changed by changing A, the plate area or d, the plate separation or ε_r, the relative permittivity of the dielectric material.
- The principle of operation of an inductive transducer is given by the equation represented in Eq. (9.3) which is dependent on the coil characteristics like number of turns, cross-sectional area, length, etc.
- A linearly variable differential transducer, popularly called LVDT, is the most commonly used type of variable inductance transducer and is primarily used to convert a linear displacement into an electrical signal.
- A potentiometric transducer is a passive type of transducer wherein a linear or rotational displacement is converted into a resistance.
- Piezoelectric devices contain special crystals and these crystals produce a voltage if a pressure is applied to them in one direction. This potential is a result of displacement of charges.
- When a metallic conductor is either strained by applying a longitudinal stress, the conductor will be deformed and this deformation results in change in resistance of the conductor as indicated in Eq. (9.7). This is the operating principle for any resistive transducers and, in particular, for a strain gauge.

- ➢ Thermistors are variable resistors; their resistance varies with temperature as given in Eq. (9.11).
- ➢ The resistance of a positive temperature coefficient (+ve α) device changes directly with changes in temperature.
- ➢ The resistance of a negative temperature coefficient (–ve α) device changes inversely with changes in temperature.
- ➢ The efficiency of a transducer is found by comparing the total energy input to the total energy coming out of the system.

Review Questions

1. Define a transducer in your own words.
2. Define the following: a sensor, an actuator.
3. Differentiate between the following: (i) a transducer and inverse transducer (ii) a sensor and actuator.
4. Differentiate between the following: (i) active transducer and passive transducer (ii) analog transducer and digital transducer.
5. Differentiate between the following: (i) primary transducer and secondary transducer (ii) input transducers and output transducers.
6. Explain the principle of operation of a capacitive transducer in your own words.
7. Explain the principle of operation of a inductive transducer in your own words.
8. Explain the principle of operation of a resistive transducer in your own words.
9. Explain the principle of operation of an LVDT in your own words.
10. Explain the principle of piezoelectric transducer in your own words.
11. Differentiate between a thermocouple and a thermistor.

Exercise Problems

1. A parallel-plate capacitive transducer has plate dimensions of 20 mm × 25 mm separated by a distance of 0.3 mm. Find the diaphragm movement if the pressure applied to it produces a new capacitance of 670 pF for the transducer; the un-pressured capacitance of the transducer is 370 pF.
2. A parallel-plate capacitive transducer has plate dimensions of 20 mm × 25 mm separated by a distance of 0.3 mm. Find the diaphragm movement if the pressure applied to it produces a new capacitance of 670 pF for the transducer; the un-pressured and no dielectric capacitance of the transducer is 370 pF. The dielectric constant of the mica sheet used is 8 and that of air is 8.85×10^{-12}.
3. A quartz crystal has a force of 10 N acting on it; the charge sensitivity of the quartz crystal is 2.55 pC/N. Calculate the output voltage developed across the output terminals of the transducer given the crystal dimensions ($5 \times 5 \times 2$) mm and the permittivity is 40.6×10^{-12} F/m.
4. The length of a linear resistance potentiometer is 100 mm and the total resistance is 100 kΩ. Find the displacement corresponding to a resistance reading of 4 kΩ, if the normal position for the slider is the mid-way of potentiometer. Also find resolution for the potentiometer.
5. A piezoelectric crystal with dimensions ($l \times w \times t$) = ($8 \times 8 \times 1.5$) mm is subjected to a stress of 1.5 MN/m2. Calculate the output voltage developed across the crystal if the crystal sensitivity is 0.055 Vm/N.

6. The piezoelectric crystal with dimensions ($l \times w \times t$) = ($8 \times 8 \times 2$) mm has output voltage developed across the crystal equal to 100 V. Calculate the stress applied if the crystal sensitivity is 0.055 Vm/N.
7. A strain gauge of resistance 120 Ω is connected to a cantilever and applied with a force that causes a change in gauge resistance of 0.152 Ω. If the strain is measured to be 0.55×10^{-3}, what is the gauge factor?
8. The resistance of a Thermistor used in an application at 25°C is 10 kΩ. Find the resistances of the thermistor (i) when the temperature is halved, and (ii) when the temperature is doubled given the temperature co-efficient is -0.08/°C. Comment on the results.
9. The resistance of a thermistor used in an application at 25°C is 10 kΩ. Find the resistances of the thermistor (i) when the temperature is halved, and (ii) when the temperature is doubled given the temperature co-efficient is +0.08/°C. Comment on the results and compare with that in Problem 7.
10. Calculate the output voltage developed across a Hall-effect transducer used for the measurement of a magnetic field of 0.55 Wb/m^2 strength. The current flowing through the germanium Hall conductor of thickness 2 mm is 3000 mA and the Hall co-efficient is $-8 \times 10^{-3} \frac{V_\alpha - m}{A - \frac{\text{Wb}}{\text{m}^2}}$.
11. Find value of charge and the voltage developed for a piezoelectric transducer with dimensions of $(2 \times 2 \times 1)$ mm if the crystal is subjected to a strain of 10×10^{-6} m/m, given the charge sensitivity of the crystal 21 C/N and permittivity of 40.6×10^{-12} F/m.

Multiple-Choice Questions

1. A _____ element is that part of a transducer which responds to a physical phenomenon or change in a physical phenomenon.
   (a) sensing (b) transduction (c) resistive (d) inductive
2. Some of the functional building blocks of the transduction system are
   (a) primary sensing element (b) transduction element
   (c) output load (d) all the above
3. In order to measure and manipulate the input non-electrical quantity for an instrumentation system, the device used is
   (a) transducer (b) oscillator (c) amplifier (d) none of the above
4. A transducer is characterized by
   (a) the physical phenomenon is transformed into an electrical quantity or vice versa
   (b) the relationship between the physical parameter and its resulting electrical signal must be a linear one.
   (c) consists of two parts a sensing element and a transduction element
   (d) all the above
5. The part of the transducer that transforms the output of a sensing element to an equivalent electrical output is
   (a) sensing (b) transduction (c) resistive (d) inductive

6. The transducers can be classified as
   (a) primary and secondary transducers (b) passive and active transducers
   (c) analog and digital transducers (d) all the above
7. The transducers can be classified on the basis of principle of transduction as
   (a) resistive (b) inductive (c) capacitive (d) all the above
8. An example of passive transducer is
   (a) resistive (b) inductive (c) capacitive (d) all the above
9. An example of active transducer is
   (a) piezoelectric (b) photovoltaic (c) both (a) and (b) (d) none of the above
10. An example of analog transducer is
   (a) piezoelectric (b) photovoltaic (c) LVDT (d) none of the above
11. An example of digital transducer is
   (a) piezoelectric (b) photovoltaic (c) LVDT (d) none of the above
12. A device which converts an electrical quantity into a non-electrical quantity is
   (a) transducer (b) inverse transducer or output transducer
   (c) amplifier (d) oscillator
13. An example of inverse transducer is
   (a) indicating Instruments (b) pen recorders
   (c) oscilloscope (d) all the above
14. Potentiometer, thermistor, resistance strain gauge are examples of _____ transducer
   (a) resistive (b) inductive (c) capacitive (d) all the above
15. Photoconductive cell, hot wire meter, resistance thermometer are examples of _____ transducer
   (a) resistive (b) inductive (c) capacitive (d) all the above
16. Capacitor microphone, dielectric gauge, capacitance pressure gauge are examples of _____ transducer
   (a) resistive (b) inductive (c) capacitive (d) all the above
17. Magnetic circuit transducer, reluctance pick-up, differential transformer are examples of _____ transducer.
   (a) resistive (b) inductive (c) capacitive (d) all the above
18. Eddy current gauge, magnetostriction gauge are examples of _____ transducer.
   (a) resistive (b) inductive (c) capacitive (d) all the above
19. Photovoltaic cell, photo-emissive cell, photo-multiplier tube are examples of _____ transducer.
   (a) resistive (b) inductive (c) capacitive (d) active
20. Which of the following statements is/are correct? A transducer converts
   (i) mechanical energy into electrical energy.
   (ii) mechanical displacement into electrical signal
   (iii) one form of energy into another form
   (iv) Electrical energy into mechanical form
   (a) (i) and (iv) (b) (i) and (ii) (c) only (iii) (d) only (i)
21. Which one of the following transducers requires power supply for its operation?
   (a) Thermocouple (b) Photovoltaic cell (c) Piezoelectric (d) Thermistor

22. The pair of active transducers is
    (a) thermistor, solar cell
    (b) thermocouple, thermistor
    (c) thermocouple, solar cell
    (d) solar cell, LVDT

23. An ideal transducer should have the following characteristics:
    (a) Should maintain a good resolution throughout its operating range
    (b) Should ideally extract no force, power or energy from the quantity under measurement for more accurate measurement
    (c) Should have no loading effect on the input quantity being measured
    (d) All the above

24. An inverse-transducer is a device that converts
    (a) light energy into mechanical energy
    (b) any form of energy into electrical energy
    (c) mechanical energy into light energy
    (d) electrical energy into any form of energy

25. A microphone is an example of a/an _____ type transducer.
    (a) actuating
    (b) sensing
    (c) both actuating and sensing
    (d) neither actuating nor sensing

26. A speaker is an example of a/an _____ type transducer.
    (a) actuating
    (b) sensing
    (c) both actuating and sensing
    (d) neither actuating nor sensing

27. A solar cell is an example of a/an _____ type transducer.
    (a) active
    (b) passive
    (c) both active and passive
    (d) neither active nor passive

28. A speaker is an example of a/an _____ type transducer.
    (a) active
    (b) passive
    (c) both active and passive
    (d) neither active nor passive

29. A thermocouple is an example of a/an _____ type transducer.
    (a) active
    (b) passive
    (c) both active and passive
    (d) neither active nor passive

30. A strain gauge is an example of a/an _____ type transducer.
    (a) active
    (b) passive
    (c) both active and passive
    (d) neither active nor passive

31. A/An _____ transducer is also called a modulating transducer.
    (a) active
    (b) passive
    (c) both active and passive
    (d) neither active nor passive

32. A capacitive transducer measures _____ as a change in capacitance.
    (a) applied pressure
    (b) applied voltage
    (c) applied temperature
    (d) applied current

33. In a capacitive transducer, the applied pressure results in movement of _____.
    (a) parallel plates (b) transducer (c) leads (d) diaphragm

34. The sensitivity of a capacitive transducer is given by _____.
    (a) $S = \frac{\delta \mathrm{x} F}{\delta \mathrm{cm}}$ (b) $S = \delta C \times \delta \mathrm{x} \frac{\mathrm{F}}{\mathrm{m}}$ (c) $S = \frac{\delta C F}{\delta \mathrm{x} m}$ (d) None

35. In a capacitive transducer the applied pressure increases the effective capacitance; this implies that the separation between the plates is _____.
(a) increased (b) unchanged (c) decreased (d) none of the above

36. An inductive transducer measures _____ as a change in Inductance.
(a) applied pressure (b) applied voltage
(c) applied temperature (d) applied current

37. In an inductive transducer, the applied pressure results in movement of _____.
(a) parallel plates (b) transducer (c) coils (d) none of the above

38. In an inductive transducer, the total inductance is given by _____.

(a) $L = \frac{N^2 \mu}{Al} H$ (b) $L = \frac{N^2 \mu}{Al} H$ (c) $L = \frac{N^2 \mu A}{l} H$ (d) none of the above

39. In an inductive transducer, if L_1 and L_2 are the self-inductances then the mutual inductance is given by _____.

(a) $L_M = K\sqrt{L_1 L_2}\, H$ (b) $L_M = \frac{K}{\sqrt{L_1 L_2}} H$ (c) $L_M = \frac{\sqrt{L_1 L_2}}{K} H$ (d) none

40. The gauge factor in a strain gauge is given by _____.

(a) $G_F = \frac{\frac{\Delta L}{R}}{\frac{\Delta L}{R}}$ (b) $G_F = \frac{\frac{\Delta L}{R}}{\frac{\Delta R}{L}}$ (c) $G_F = \frac{\frac{\Delta L}{L}}{\frac{\Delta R}{R}}$ (d) none of the above

41. In an inductive transducer, the applied pressure results in movement of _____.

(a) $G_F = 1 + 2x + \frac{\Delta\rho/\rho}{\varepsilon}$ (b) $G_F = 1 - 2x + \frac{\Delta\rho/\rho}{\varepsilon}$

(c) both (a) and (b) (d) none of the above

42. The sensitivity of a potentiometric transducer is given by _____.

(a) $S = \frac{\text{Output}}{\text{Input}} = \frac{V_i}{V_o}$ (b) $S = \frac{\text{Output}}{\text{Input}} = \frac{V_o}{V_i}$

(c) $S = \frac{\text{Input}}{\text{Output}} = \frac{V_i}{V_o}$ (d) none of the above

43. The sensitivity of an LVDT is defined as the ratio of _____.

(a) $S = \frac{\text{Output Voltage}}{\text{Core displacement}}$ (b) $S = \frac{\text{Core displacement}}{\text{Output Voltage}}$

(c) $S = \frac{\text{Output Voltage}}{\text{Input Voltage}}$ (d) None of the above

44. The output voltage produced in a piezoelectric transducer is given by _____.

(a) $V_o = \frac{d}{t\, P\, \varepsilon_0 \varepsilon_r}$ (b) $V_o = \frac{d}{t\, \varepsilon_0 \varepsilon_r} P$ (c) $V_o = \frac{d}{\varepsilon_0 \varepsilon_r} t\, P$ (d) none of the above

45. The voltage sensitivity of a piezoelectric transducer is given by _____.

(a) $g = \varepsilon_0 \dfrac{d}{\varepsilon_r}$ (b) $g = \dfrac{d}{\varepsilon_0 \varepsilon_r}$ (c) $g = \dfrac{\varepsilon_0 \varepsilon_r}{d}$ (d) none of the above

46. In a potentiometric transducer, within limited temperature ranges, the resistance-temperature relationship may be written as _____.

(a) $R_2 = R_1(1 + \alpha (t_2 - t_1))$ (b) $R_2 = R_1(1 + \alpha \Delta t)$
(c) $R_2 = R_1(1 - \alpha (t_2 + t_1))$ (d) both (a) and (b)

47. The output voltage produced in a Hall-effect transducer is given by _____.

(a) $V_b = \dfrac{B \times I}{t \times K_H}$ (b) $V_b = \dfrac{I \times K_H}{B \times t}$ (c) $V_b = \dfrac{B \times I \times K_H}{t}$ (d) none of the above

48. The transfer function of a system is defined as follows:
(a) Ratio of Laplace transform of input to Laplace transform of output with initial conditions $\neq 0$.
(b) Ratio of Laplace transform of output to Laplace transform of input with initial conditions $\neq 0$.
(c) Ratio of Laplace transform of input to Laplace transform if output with all initial condition = 0.
(d) Ratio of Laplace transform of output to Laplace transform of input with initial condition = 0

Field Effect Transistors and Other Devices

10

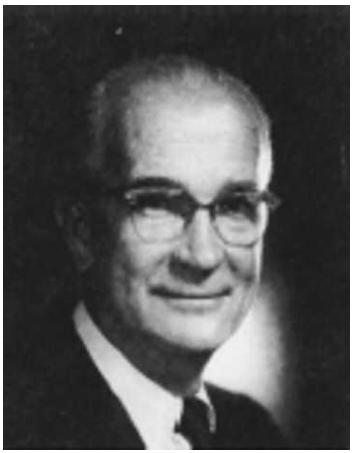
Goals and Objectives

Upon completion of this chapter, the reader is expected to;

- Understand the basic construction of a FET and compare that with a BJT
- Understand the working principle, characteristics of a FET and compare that with a BJT
- Understand and define the performance parameters of a FET
- Understand the biasing concepts of a FET and bias a FET for various applications
- Learn how to construct different amplifiers such as common-source and common-drain amplifiers
- Understand different modes of MOSFET operation (enhancement mode and depletion mode)
- Understand basics of CMOS circuits
- Know how to extract different FET characteristics for various applications
- Understand the basic construction of a MOSFET and compare that with a FET
- Understand the working principle, characteristics of a MOSFET
- Understand the biasing concepts of a MOSFET and bias a MOSFET
- Understand the basic construction of UJT and compare that with a BJT
- Understand the working principle, characteristics of a UJT
- Understand the negative resistance property of a UJT and use this property to construct an oscillator
- Understand the basic construction, working principle, characteristics and applications of special devices like SCS, DIAC and TRIAC
- Understand the basic concepts of opto-couplers and opto-devices
- Feel confident of taking up higher courses like VLSI design, power electronics, etc.

10.1 INTRODUCTION

In a conventional transistor (BJT), both electrons and holes constitute the device current and hence it is called a **bipolar device**. A BJT has some major disadvantages such as the input impedance is very small because of forward-biased input junction, small device gain, more noise, larger device sise, etc. But, a Field Effect Transistor (FET) is a **unipolar device** and the device current is only due to only one type of charge carriers, i.e. either due to electrons or holes. Almost all the disadvantages of a BJT are overcome in a FET and hence this device is used in almost all Integrated Circuit (IC) designs. Unlike a BJT, a FET offers high input impedance which is one of the important requirements in any circuit design. A FET is smaller in size compared to a BJT, has less noise and offers very good gain. The Silicon-Controlled Rectifier (SCR) is another important special device that is used in all power electronic applications such as controlled rectifiers, inverters (dc to ac converters), choppers (dc to dc converters), etc. SCRs are capable of controlling precisely the amount of power that is fed to the load. This three-terminal device plays a vital role in many power applications. The Unijunction Transistor (UJT) is another unipolar, special device that is used in applications like SCR triggering circuits. This special device possesses a very important characteristic called **negative resistance property** based on which signals can be generated. This gives rise to a special class of signal generators (oscillators) called **negative resistance oscillators**. There are many other special devices like DIAC, TRIAC, Programmable UJTs, etc. In this chapter, a focus is drawn to study the construction, working principles and applications of all these special devices.



(a) William Bradford Shockley (1910–1989), co-inventor of the first transistor and formulator of the 'field-effect' theory employed in the development of the transistor and the FET.

(b) Drs. Ian Munro Ross (front) and G. C. Dacey jointly developed an experimental procedure for measuring the characteristics of a FET in 1955.

Fig. 10.1

10.2 FIELD EFFECT TRANSISTORS (FETs)

Field Effect Transistor is a 3-terminal device similar to a BJT (discussed in Chapter 3 and Chapter 4) that can easily replace a BJT in many applications such as an amplifier, an oscillator (signal generator), a switch, a chopper (dc to dc convertor), etc. In construction, a FET contains one basic *PN* junction and can be built either as a Junction FET (JFET) or Insulated Gate FET (IGFET) or Metal Oxide Semiconductor FET (MOSFET). In Fig. 10.2, the basic construction, different terminals and the circuit symbols of field effect transistors are shown.

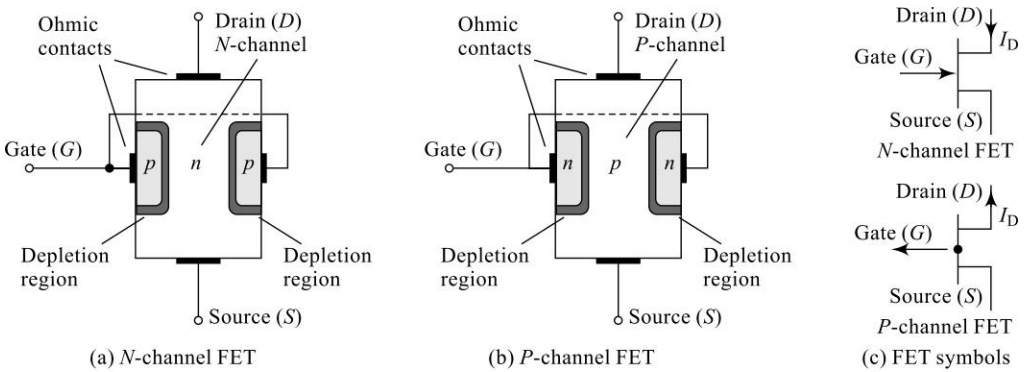


Fig. 10.2 Field Effect Transistor (FET)

The *N*-channel FET is constructed using a bar of *N*-type semiconductor material into which a pair of *P*-type region is diffused. This forms an *N*-channel and a *PN* junction. Similarly, a *P*-channel FET is constructed using a bar of *P*-type semiconductor material into which a pair of *N*-type region is diffused. This forms a *P*-channel and a *PN* junction. The circuit symbols for both these devices are shown; for a *P*-channel, the gate terminal arrowhead is shown outward and for an *N*-channel, the gate terminal arrowhead is shown inward.

Working

The principle of working of a FET is understood by considering the diagrams shown in Fig. 10.3. The input gate-source terminals are reverse biased using the supply source V_{GG} and the output drain-source terminals are supplied with a voltage source V_{DD} that provides a voltage V_{DS} between drain and source terminals; this results in the drain current I_D. This current passes through the *N*-channel surrounded by *P*-type gate.

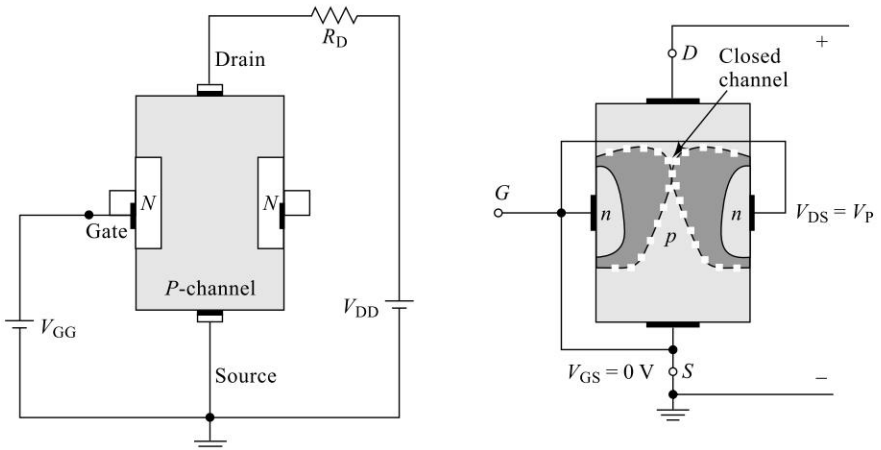


Fig. 10.3 FET working principle

A voltage V_{GS} set by V_{GG} between the gate and source reverse biases the gate source junction and results in no gate current. The effect of this gate-source voltage is to form a depletion region in the channel and to reduce the channel width resulting in less I_D.

With a reverse bias on gate-source, the depletion region is more near the drain end compared to the source end; an increase in V_{DS} causes the depletion region to grow. Further increase in V_{DS} causes the depletion region to grow and at one stage, the depletion region forms fully across the channel after which the drain current saturates and remains constant. With $V_{GS} = 0$, the drain current I_D increases until the depletion region is formed. Now the FET is said to be in ohmic region and the slope of the curve represents the channel resistance (R). This is indicated in the drain characteristics shown in Fig. 10.4. It can be observed here that the channel resistance is increasing near pinch-off.

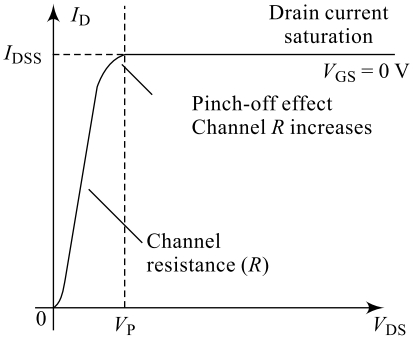


Fig. 10.4 FET characteristics

10.2.1 FET Characteristics

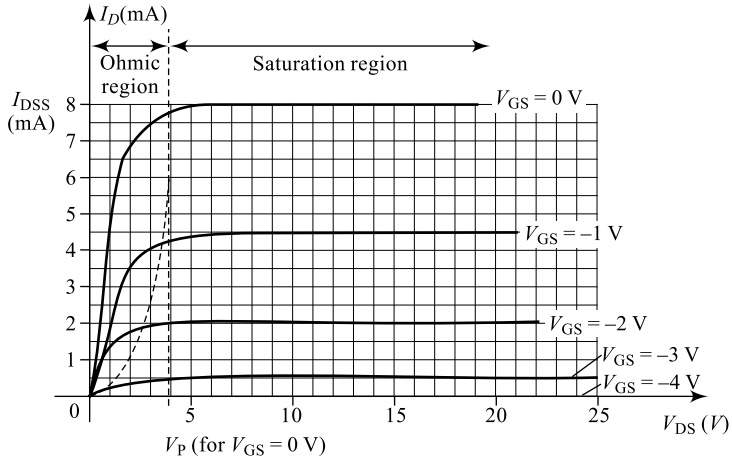
FET performance characteristics can be drawn based on the working principle and there are two sets of characteristics; the drain characteristics and the mutual characteristics. Drain characteristics is a plot of drain-current variation as a function of drain-source voltage for a given gate-source voltage. As the reverse bias on gate-source increases, the drain current reduces and for a given gate-source voltage, increasing drain-source voltage results in drain-current saturation (pinch-off). This is indicated in Fig. 10.5(a). Once the channel is completely bolted, the I_D levels off and this value of drain current is I_{DSS}, the drain-to-source current with gate source shorted. The region on drain characteristics after which I_D levels off is called **pinch-off region** and the corresponding voltage on drain-source is V_P. Mutual or transfer characteristics is a plot of drain-current variation as a function of gate-source voltage for a given drain-source voltage. As the reverse bias on gate-source increases, the drain current decreases. At one particular value, it may even become zero. The value of gate-source voltage V_{GS} at which drain current becomes zero is known as **pinch-off voltage** (V_P). At this value of V_{GS}, the channel is pinched off removing all charge carriers resulting in $I_D = 0$ and hence, this voltage is referred to as V_{GS} (OFF). As V_{GS} is increased in magnitude, I_D falls and at $V_{GS} = V_p$, I_D becomes zero. Once FET enters saturation region, the drain current I_D follows the **Shockley's equation** Eq. (10.1), and the shape of transfer characteristics is, therefore, a parabola as shown in Fig. 10.5(b).

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{10.1}$$

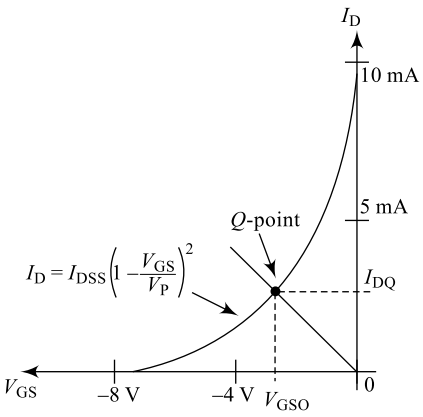
1. FET Parameters

Manufacturers specify number of parameters that describe FET device and provide data necessary for selecting FET for a particular application. Some of these more useful parameters are listed below:

(i) I_{DSS}, the drain-source saturation current
(ii) $V_P = V_{GS(OFF)}$, the pinch-off voltage
(iii) g_m, the device transconductance
(iv) $r_{d(on)}$, the drain source resistance when the device is on
(v) μ, the amplification factor.



(a) Drain characteristics



(b) Mutual characteristics

Fig. 10.5 FET characteristics

2. *Drain Resistance,* r_d

The drain resistance of a FET in its ON condition is defined as the ratio of a change in the drain-source voltage V_{DS} to a corresponding change in the drain current I_D for a given gate-source voltage $V_{GS.}$ Drain resistance is expressed in units of ohms.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Bigg/ V_{GS} \ \Omega \tag{10.2}$$

It is an indication of the JFET channel resistance and its value increases with increase in the reverse bias on the gate-source terminals. Drain resistance will be maximum at the pinch-off region, i.e. when $|V_{GS}| = V_P$. This is because the channel will be closed at pinch-off.

3. Transconductance, g_m

It is an indication of the JFET ac amplification; g_m tells how much the ac current will change due to an applied ac gate-source voltage. It is defined as the ratio of change in drain current I_D to a corresponding change in gate-source voltage V_{GS} for a given drain-source voltage V_{GS}. Transconductance is expressed in units of mhos.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big/ \Delta V_{DS} \quad \text{℧} \tag{10.3}$$

Example 10.1

Determine the amplification factor for a FET whose on-state drain resistance is 2000 Ω and the transconductance is 50×10^{-4} mhos.

Solution From Eq. (10.4a), the amplification factor is given as

$$\mu = r_d \times g_m$$
$$\mu = 2000 \times 50 \times 10^{-4}$$
$$\mu = 10$$

4. Amplification Factor, μ

It is an indication of the JFET ac amplification and it is directly the product of the drain resistance and the transconductance. It is defined as the ratio of the change in drain-source voltage V_{DS} to a corresponding change in gate-source voltage V_{GS}.

$$\mu = r_d \times g_m \qquad [(10.4(a)]$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta V_{GS}} \qquad [(10.4(b)]$$

In addition, a number of other parameters like device capacitances, noise voltage, turn-on time, turn-off times and the power-handling capacity are usually provided in the manufacturer's data sheet.

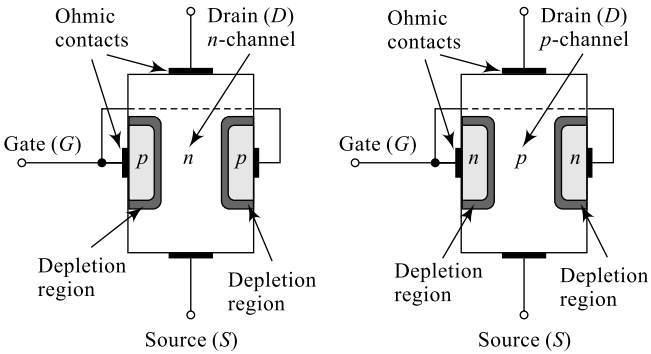
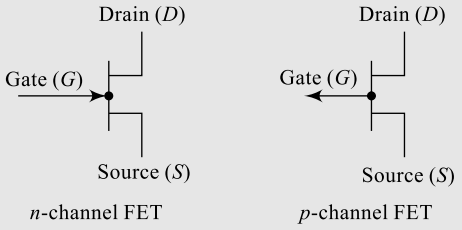
Example 10.2

In Example 10.1, determine the change in drain-source voltage to achieve the resulting amplification factor for the FET if the drain current changes by 5 mA.

Solution From Eq. (10.2), the drain resistance is given as

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Big/ V_{GS} \quad \Omega$$
$$r_d = 2000 = \frac{\Delta V_{DS}}{\Delta I_D}$$
$$\Delta V_{DS} = 2000 \times \Delta I_D = 2000 \times 5 \times 10^{-3}$$
$$\Delta V_{DS} = 10 \text{ V}$$

Table 10.1 FET basics

Sl. No.	Parameter	
1	Device construction	
2	Device symbol	
3	Pinch-off voltage	V_P, the gate-source voltage at which the channel is completely seized
4	Saturation drain current	I_{DSS}, the drain current resulted after V_P
5	Drain resistance ($\boldsymbol{r_d}$)	$r_d = \dfrac{\Delta V_{DS}}{\Delta I_D}\ \Omega$
6	Transconductance ($\boldsymbol{g_m}$)	$g_m = \dfrac{\Delta I_D}{\Delta V_{GS}}\ \mho$
7	Amplification factor ($\boldsymbol{\mu}$)	$\mu = r_d \times g_m = \dfrac{\Delta V_{DS}}{\Delta V_{GS}}$

Example 10.3

Determine the resistance offered by a FET whose drain current changes by 7 mA for a change of 5 V in gate-source voltage, given its amplification factor is 10.

Solution From Eq. (10.3), the transconductance of the device is given as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big/ \Delta V_{DS}\ \mho$$

$$g_m = \frac{7 \times 10^{-6}}{5} = 1.4 \times 10^{-3}\ \mho$$

From Eq. (10.4a), the drain resistance of the device is given as

$$\mu = r_d \times g_m$$

$$r_d = \frac{\mu}{g_m} = \frac{10}{1.4 \times 10^{-3}} = 7142.86\ \Omega$$

$$r_d = 7.143\ \text{k}\Omega$$

10.2.2 FET Biasing

To fix up an operating point (Q-point), just like a conventional BJT, even JFET requires biasing. In order that a FET functions properly, its gate-source junction needs to be reverse biased and the source-drain needs a forward bias. As discussed in sections 3.5 to 3.11, several biasing techniques can be considered even for FET biasing and only three standard FET biasing methods are discussed here; they are

(i) Fixed biasing
(ii) Self-biasing
(iii) Potential-divider biasing

1. Fixed Biasing

The arrangement shown in Fig. 10.6 is a fixed-bias circuit; the power source V_{GG} provides the required reverse bias for gate-source junction and power source V_{DD} provides a reverse bias to the drain and a forward bias to the source terminal. Use of R_D and R_G along with V_{GG} and V_{DD} fixes the values of I_D and V_{DS} with zero input signal corresponding to the Q-point and are referred as I_{DQ} and V_{DSQ}.

These values can be obtained by analysing the above circuit using the conventional analysis methods. We know from Eq. (10.1),

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where $I_{DSS} = I_D$ with $V_{GS} = 0$ and is called drain-saturation circuit.

Also, for the input circuit, using KVL, we may write

$$-V_{GG} - I_G R_G - V_{GS} = 0 \tag{10.5}$$

where V_{GS} is the gate-to-source potential and since gate-source is reverse biased, $I_G = 0$,

i.e. $$-V_{GG} - 0 - V_{GS} = 0$$

i.e. $$V_{GS} = -V_{GG} \tag{10.6}$$

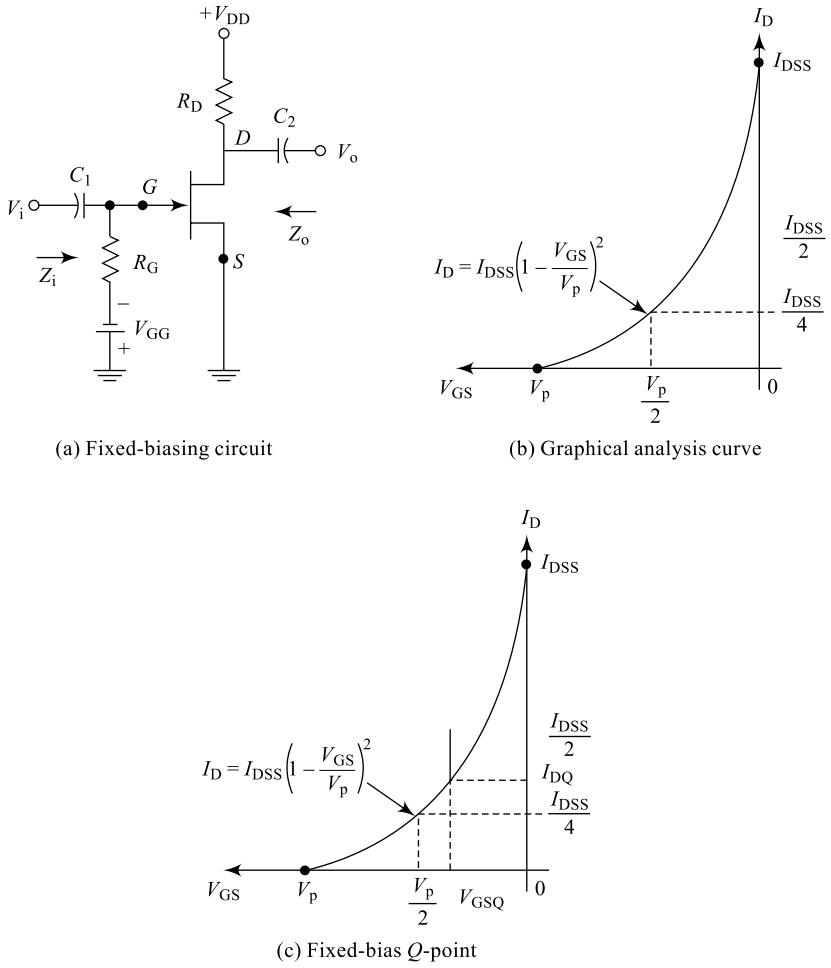
Substituting Eq. (10.6) in Eq. (10.1) results in

$$I_D = I_{DSS}\left(1 + \frac{V_{GG}}{V_P}\right)^2 \tag{10.7}$$

Analysing the output circuit using KVL, we may write the following equation:

$$V_{DS} = V_{DD} - I_D R_D \tag{10.8}$$

Equations (10.7) and (10.8) represent the operating point (Q-point) for the fixed-bias circuit and these two equations are the design equations for a fixed-bias circuit. This circuit is similar to a two-battery bias circuit for a BJT and uses two battery sources, V_{GG} and V_{DD}.



(a) Fixed-biasing circuit

(b) Graphical analysis curve

(c) Fixed-bias *Q*-point

Fig. 10.6 FET Fixed Biasing

Graphical Method The above approach is called the analytical method and this method is normally used to find the operating point for any FET biasing circuit. Alternatively, another method, referred to as graphical method, can also be used to find the operating point for any biasing circuit. From Eq. (10.1), the Shockley equation, the transfer curve can be drawn as in Fig. 10.6(b). If $V_{GS} = V_P/2$ then $I_D = I_{DSS}/4$. A vertical line corresponding to $V_P = V_{GSQ}$ intersects the transfer curve and this points gives the operating point for fixed-bias configuration. This is depicted clearly in Fig. 10.6(c) and more clarification may be obtained by referring to Example 10.5 for this method.

Example 10.4

For the fixed-bias circuit shown in Fig. 10.7, determine the operating point if I_{DSS} = 10 mA and V_P = –4 V.

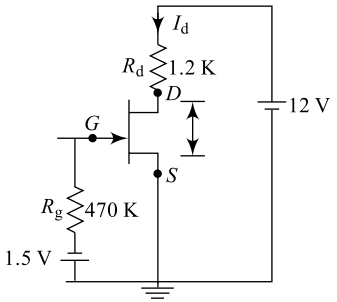


Fig. 10.7 Fixed-bias circuit

Solution From Eq. (10.5), $V_{GS} = -V_{GG} = -1.5$ V

Now, from Eq. (10.1),

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 10 \times 10^{-3}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 10 \times 10^{-3}\left(1 - \frac{-1.5}{-4}\right)^2$$

$$I_D = 3.91 \text{ mA} = I_{DQ}$$

Also, from Eq. (10.8),

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = 12 - (3.91 \times 10^{-3})(1.2 \times 10^3)$$

$$V_{DS} = 7.31 \text{ V} = V_{DSQ}$$

Thus, the operating point required is $Q\ (I_{DQ}, V_{DSQ}) = (3.91 \text{ mA}, 7.31 \text{ V})$.

Example 10.5

For the problem in Example 10.4, determine the operating point using graphical method.

Solution From Eq. (10.1), the Shockley equation, the transfer curve can be drawn as in Fig. 10.8. At $V_{GS} = -1.5$ V, the drain current $I_D = 3.9$ mA.

Now, from Eq. (10.8), we obtain the drain-source voltage.

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = 12 - (3.9 \text{ mA} \times 1.2 \text{ k}\Omega)$$

$$V_{DS} = 7.32 \text{ V}$$

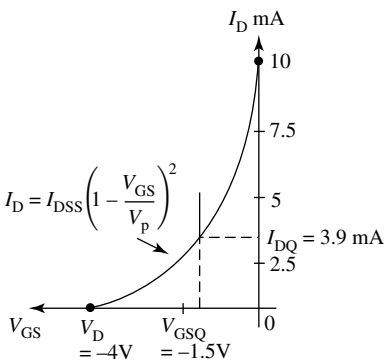


Fig. 10.8 Fixed-bias circuit transfer curve

2. Self-Biasing

The arrangement shown in Fig. 10.9 is a self-bias circuit; in this method V_{DD} provides the required bias for drain-source terminals and the required reverse bias for gate-source junction is obtained by the help of a drop across R_S, hence the name self-

bias. This circuit, unlike a fixed-bias circuit, uses only one battery source V_{DD} and hence, is a better circuit.

The zero-signal values of I_D and V_{DS} are called the **operating point (*Q*-point)** and are referred as I_{DQ} and V_{DSQ}. These values for a self-bias circuit can be obtained by analysing the above circuit using KVL and other conventional analysis methods. We know, from Eq. (10.1),

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where $I_{DSS} = I_D$ with $V_{GS} = 0$ and is called **drain-saturation current**.

Also, for the input circuit, using KVL, we may write

$$-I_G R_G - V_{GS} - (I_D + I_G) R_S = 0 \qquad (10.9)$$

where V_{GS} is the gate-to-source potential and since gate-source is reverse biased, $I_G = 0$

$$-V_{GS} = I_D R_S \qquad (10.10)$$

Or
$$V_{GS} = -I_D R_S \qquad (10.11)$$

Substituting Eq. (10.11) in Eq. (10.1) results in

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2 \qquad (10.12)$$

Equation (10.12) is a quadratic equation (QE) in I_D and the value of I_D can be obtained by solving this quadratic equation (positive value to be taken).

Note: Solving the QE $ax^2 + bx + c = 0$, the roots are given by

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

Analysing the output circuit using KVL, we may write the following equation:

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

From this, we can write $V_{DS} = V_{DD} - I_D R_D - I_D R_S$ (10.13)

Equations (10.12) and (10.13) represent the operating point (*Q*-point) for the self-bias circuit and these two equations are the design equations for a self-bias circuit. This circuit is analogous to a self-bias circuit for a BJT and uses only one battery source V_{DD}.

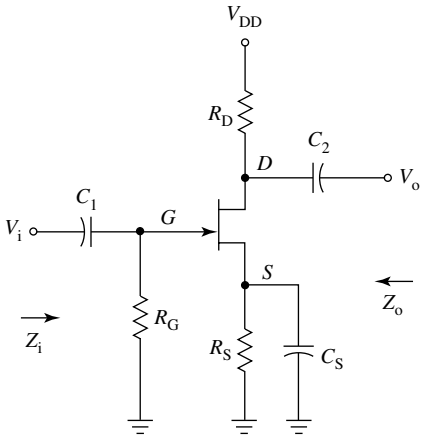


Fig. 10.9 FET self-biasing

Example 10.6

Determine the operating point (*Q*-Point) for the self-bias circuit shown in Fig. 10.10, given $V_{DD} = 16$ V, $R_D = 3.3$ kΩ, $R_G = 470$ kΩ, $R_S = 1$ kΩ, $I_{DSS} = 10$ mA and $V_P = -6$ V.

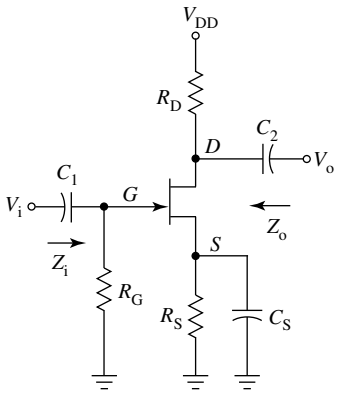


Fig. 10.10 Self-biasing

Solution Now, from Eq. (10.1), $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

From Eq. (10.11), $V_{GS} = -I_D \times R_S$

$$I_D = I_{DSS}\left(1 + \frac{V_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\{1 + (R_S/V_P)^2\ I_D^2 + 2\,(R_S/V_P)\,I_D\}$$

$$I_D\{1 - 2I_{DSS}\,(R_S/V_P)\} = I_{DSS} + I_{DSS}\,(R_S/V_P)^2\ I_D^2$$

$$I_{DSS}\,(R_S/V_P)^2\ I_D^2 - \{1 - 2I_{DSS}(R_S/V_P)\}I_D + I_{DSS} = 0$$

$$10 \times 10^3 \times (1.0 \times 10^3/-6)^2\ I_D^2 - \{1 - 2 \times 10 \times 10^{-3} \times (1.0 \times 10^3/-6)\}I_D + 10 \times 10^3 = 0$$

$$1406.25\ I_D^2 - 8.5I_D + 10 \times 10^3 = 0 \tag{10.14}$$

Equation (10.14) is a quadratic equation in I_D, whose roots are

$$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

$$= \frac{-(-8.5) \pm \sqrt{(-8.5)^2 - 4(1406.25)(10 \times 10^{-2})}}{2(1406.25)}$$

$$I_D = (8.5 \pm 4/2812.5)$$

As the drain current will be very low, $I_D = (8.5 - 4)/2812.5$ value is used.

$$I_D = (8.5 - 4)/2812.5$$

$$I_D = 1.6 \text{ mA} = I_{DQ} \tag{10.15}$$

Now, $V_{DS} = V_{DD} - I_D\,(R_D + R_S)$

$$= 16 - 1.6 \times 10^{-3}\,(3.3 + 1.0)10^3$$

$$V_{DS} = 9.12 \text{ V} = V_{DSQ} \tag{10.16}$$

The corresponding value of V_{GS} is given by

$$V_{GSQ} = -I_D R_S$$

$$= -1.6 \times 10^{-3} \times 1.0 \times 10^3$$

$$V_{GSQ} = -1.6 \text{ V} \tag{10.17}$$

Equations (10.14), (10.15), (10.16) and (10.17) represent the operating point.

Example 10.7

For the problem in Example 10.6, determine the operating point using graphical method.

Solution We have from Eq. (10.1),

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

To plot the transfer characteristics using graphical method, a table of I_D as a function V_{GS} is to be prepared. Now, the following table can be prepared and the transfer curve is plotted using these values.

$V_{GS(V)}$	$I_{D(mA)}$
0.0	10.0
–1.2	6.4
–2.4	3.6
–3.6	2.5
–4.8	0.4
–6.0	0.0

Also, we have $V_{GS} = -I_D R_S$ to plot the self-bias line:

$I_{D(\ mA)}$	$V_{GS(\ mA)}$
0	0
$(-V_P/R_S) = 6.0$	–6

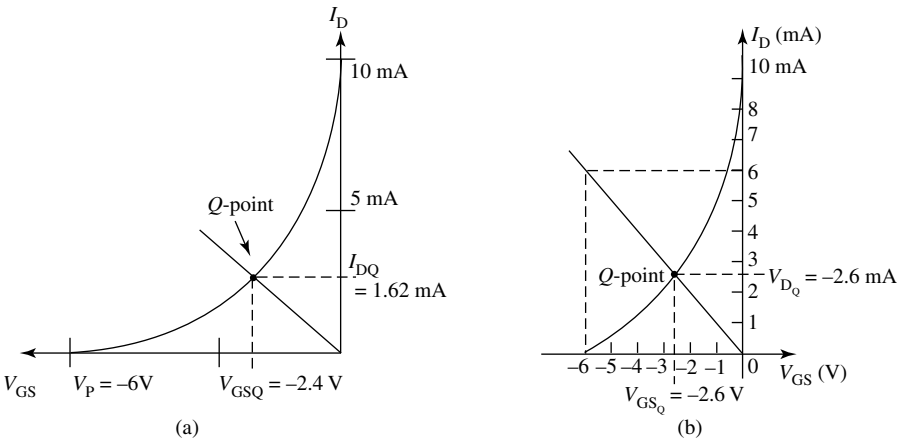


Fig. 10.11 Self-biasing

2. Voltage Divider Biasing

The circuit diagram discussed in Fig. 10.9 is a better option compared to that in Fig. 10.6, but has poor stability. Therefore, a self-bias circuit is modified by splitting R_G into R_1 and R_2 resulting in a voltage-divider biasing circuit. The arrangement for a potential-divider circuit is shown in Fig. 10.12. Supply source V_{DD} along with the combination of R_1 and R_2 provides the required reverse bias for gate-source circuit and also the bias for gate-source terminals. This circuit can be simplified as shown in Fig. 10.13 using Thevenin's theorem.

Applying Thevenin's principle across the resistor R_2, we obtain an equivalent circuit for Fig. 10.12 and it is as shown in Fig. 10.13. Here, V_G is the Thevenin's equivalent voltage and R_G is the Thevenin's equivalent impedance. The values of V_G and R_G are obtained using the basic principles.

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right) \tag{10.18}$$

$$R_G = \left(\frac{R_1 R_2}{R_1 + R_2}\right) \tag{10.19}$$

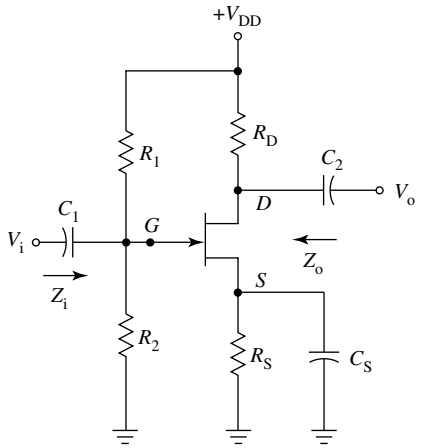


Fig. 10.12 FET potential-divider biasing

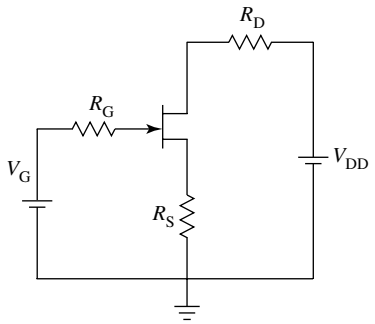


Fig. 10.13 Thevinised potential-divider biasing circuit

The operating point (Q-point) can now be obtained by analysing the circuit shown in Fig. 10.13 by using basic principles.

From Eq. (10.1), we have

$$I_D = I_{DDS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Applying KVL to the input section, we may write the following loop equation:

$$V_G - I_G R_G - V_{GS} - I_D R_S = 0 \tag{10.20}$$

Since $I_G = 0$, $V_G - 0 - V_{GS} - I_D R_S = 0$

$$V_{GS} = V_G - I_D R_S \tag{10.21}$$

Substituting Eq. (10.21) into Eq. (10.1), we get the drain current

$$I_D = I_{DSS}\left(1 - \left(\frac{V_G - I_D R_S}{V_P}\right)\right)^2 \tag{10.22}$$

Applying KVL to the output section, we may write the following loop equation:

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S) \tag{10.23}$$

Equations (10.21), (10.22) and (10.23) represent the Q-point for the voltage-divider biasing circuit. Also, Eq. (10.22) is a quadratic equation in I_D and the value of I_D can be obtained by solving this equation as in a self-bias circuit.

Table 10.2 Different FET biasing methods

Parameter	Fixed Biasing	Self-Biasing	Voltage-divider Biasing
Source resistance	No	Yes	Yes
Number of batteries	Two	One	One
Quiescent gate-source voltage	$V_{GS} = -V_{GG}$	$V_{GS} = -I_D R_S$	$V_{GS} = V_G - I_D R_S$
Quiescent drain-source voltage	$V_{DS} = V_{DD} - I_D R_D$	$V_{DS} = V_{DD} - I_D R_D - I_D R_S$	$V_{DS} = V_{DD} - I_D (R_D + R_S)$
Quiescent drain current	$I_D = I_{DSS}\left(1 + \frac{V_{GG}}{V_P}\right)^2$	$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$	$I_D = I_{DSS}\left(1 - \left(\frac{V_G - I_D R_S}{V_P}\right)\right)^2$
Stability	Moderate	Good	Better

Example 10.8

For the circuit shown in Fig. 10.14, find I_{DQ}, V_{GSQ} and V_{DSQ} using analytical method.

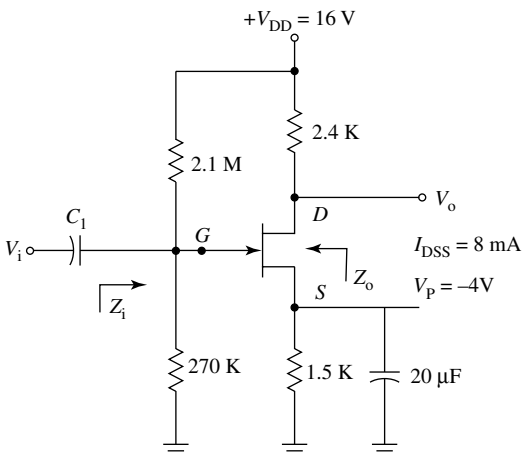


Fig. 10.14 Potential divider biasing

Solution From Eq. (10.1), the drain current is $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$$I_D = I_{DSS}\,[1 - (V_G - I_D R_S / V_P)]^2$$

Where $V_G = V_{DD} \times (R_2 / R_1 + R_2)$

$= 16 \times (270k / 2.1m + 270k)$

$= 1.82$ V

We have $R_G = (R_1 \times R_2 / R_1 + R_2)$

$= (2.1m \times 270k / 2.1m + 270k)$

$R_G = 239.24\ \text{k}\Omega$

Now
$$I_D = I_{DSS}\,[1 - (1.82/-4) + (1.5k/-4)I_D]^2$$
$$I_D = I_{DSS}\,[1.455 - 375\,I_D]^2$$
$$I_D = I_{DSS}\,[1.455^2 + (375\,I_D)^2 - 2(1.455)\,(375I_D)]$$
$$I_{DSS}\,(1.455)^2 + I_{DSS}\,(375\,I_D)^2 - I_{DSS}\,[2(1.455)\,(375I_D)] = 0 \qquad (10.24)$$
$$1125\,I_D^2 - 9.73\,I_D + 17 \times 10^{-3} = 0$$

Solving for I_D, we have

$$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$
$$= \frac{-(-9.73) \pm \sqrt{(94.673 - 4(1125 \times 17 \times 10)^{-3}}}{2(1125)}$$
$$= \frac{9.73 \pm 4.263}{2(1125)}$$
$$I_D = 2.43 \text{ mA}$$

Also, we have
$$V_{GS} = V_G - I_D R_S$$
$$= 1.8 - (2.43 \times 10^{-3} \times 1.5 \times 10^{-3})$$
$$V_{GSQ} = -1.82 \text{ V}$$
$$V_{DS} = V_{DD} - I_D\,(R_D + R_S)$$
$$= 16 - 2.4 \times 10^{-3}\,(3.9k)$$
$$V_{DS} = 6.64 \text{ V} = V_{DSQ}$$

Example 10.9

For the circuit in Example 10.8, find I_{DQ}, V_{GSQ} and V_{DSQ} using graphical method

Solution We have from Eq. (10.1), $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

To plot the transfer characteristics using graphical method, a table of I_D as a function V_{GS} is to be prepared. Now, the following table can be prepared and the transfer curve is plotted using these values.

$V_{GS(V)}$	$I_{D(\text{mA})}$
0	8
–1.2	4
–2	2
–4	0

Also, we have $V_{GS} = V_G - I_D R_S$

where $V_G = 1.82$ V

$$V_{GS} = 1.82 - I_D R_S$$

If $I_D = 0$, then $V_{GS} = 1.82$ V
$V_{GS} = 0$ then $I_D = 1.2$ Ma
$V_{GS} = -4$ then $I_D = 3.88$ Ma

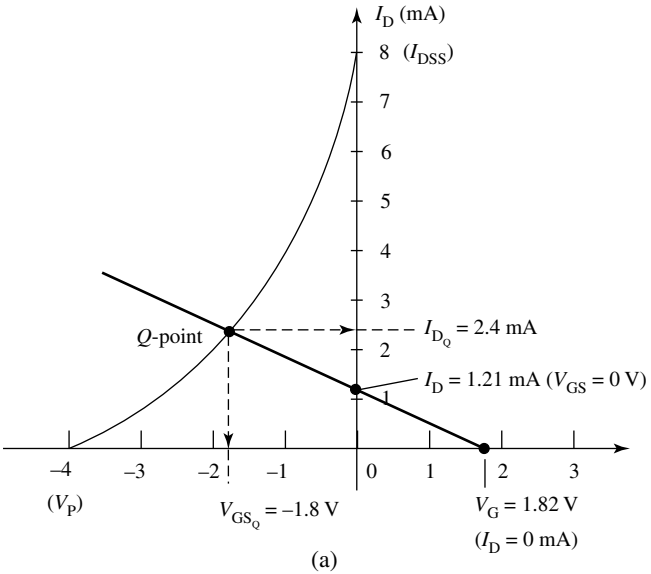


Fig. 10.15 Self-biasing

Example 10.10

Determine the operating point (Q-Point) for the potential-divider bias circuit shown in Fig. 10.16.

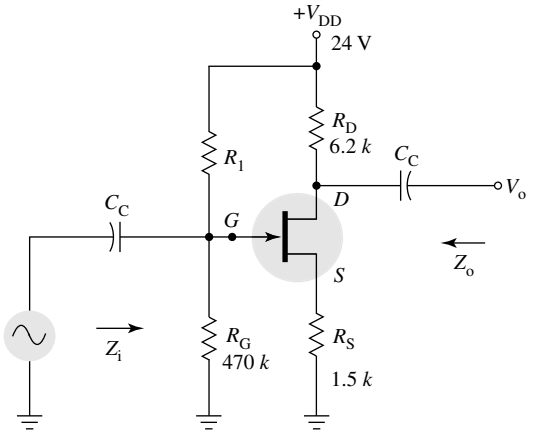


Fig. 10.16 Circuit for Example 10.10

Solution We have

$$I_D = I_{DSS}\{1 - (V_{GS}/V_P)^2\}$$

Where $I_D = I_{DSS}\{1 + (I_D R_S/V_P)\}^2$

$$I_D = I_{DSS}\{1 + (R_S/V_P)^2\ I_D^2 + 2\,(R_S/V_P)\,I_D\}$$

$$I_D\{1 - 2I_{DSS}\,(R_S/V_P)\} = I_{DSS} + I_{DSS}\,(R_S/V_P)^2\ I_D^2$$

$$I_{DSS}\,(R_S/V_P)^2\ I_D^2 - \{1 - 2I_{DSS}(R_S/V_P)\}I_D + I_{DSS} = 0$$

$$10 \times 10^3 \times (1.5 \times 10^3/-4)^2\ I_D^2 - \{1 - 2 \times 10^3 \times (1.5 \times 10^3/-4)\}\ I_D + 10 \times 10^3 = 0$$

$$1406.25\ I_D^2 - 8.5 I_D + 10 \times 10^3 = 0 \tag{10.25}$$

Equation (10.25) is a quadratic equation in I_D, whose roots are

$$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

$$= (-(-8.5) \pm \sqrt{((-8.5)2 - 4)(14.06.25)(10 \times 10\varepsilon - 3)/(2(1406.25))}$$

$$I_D = (8.5 \pm 4/2812.5)$$

As the drain current will be very low, $I_D = 8.5 - 4/2812.5$ value is used.

$$I_D = (8.5 - 4)/2812.5$$

$$I_D = 1.6 \text{ mA} = I_{DQ} \tag{10.26}$$

Now $V_{DS} = V_{DD} - I_D\,(R_D + R_S)$

$$= -1.6 \times 10^{-3}(6.2 + 1.5)10^3$$

$$V_{DS} = 11.68 \text{ V} = V_{DSQ} \tag{10.27}$$

The corresponding values of V_{GS} is given by

$$V_{GSQ} = -I_D R_S$$

$$= -1.6 \times 10^{-3} \times 1.5 \times 10^3$$

$$V_{GSQ} = -2.4 \text{ V} \tag{10.28}$$

Equations (10.26), (10.27) and (10.28) represent the required operating point.

Example 10.11

For the circuit in Example 10.10, find I_{DQ}, V_{GSQ} and V_{DSQ} using graphical method

Solution We have from Eq. (10.1), $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$

To plot the transfer characteristics using graphical method, a table of I_D as a function V_{GS} is to be prepared. Now, the following table can be prepared and the transfer curve is plotted using these values as indicated in Figure 10.17.

$V_{GS(V)}$	$I_{D(mA)}$
0.0	10.0
–0.8	6.4
–1.6	3.6
–2.0	2.5
–3.2	0.4
–4.0	0.0

Also, we have $V_{GS} = -I_D R_S$ to plot the self-bias line:

$I_{D(mA)}$	$V_{GS(mA)}$
0	0
$(-V_P/R_S)$ 2.67	–4

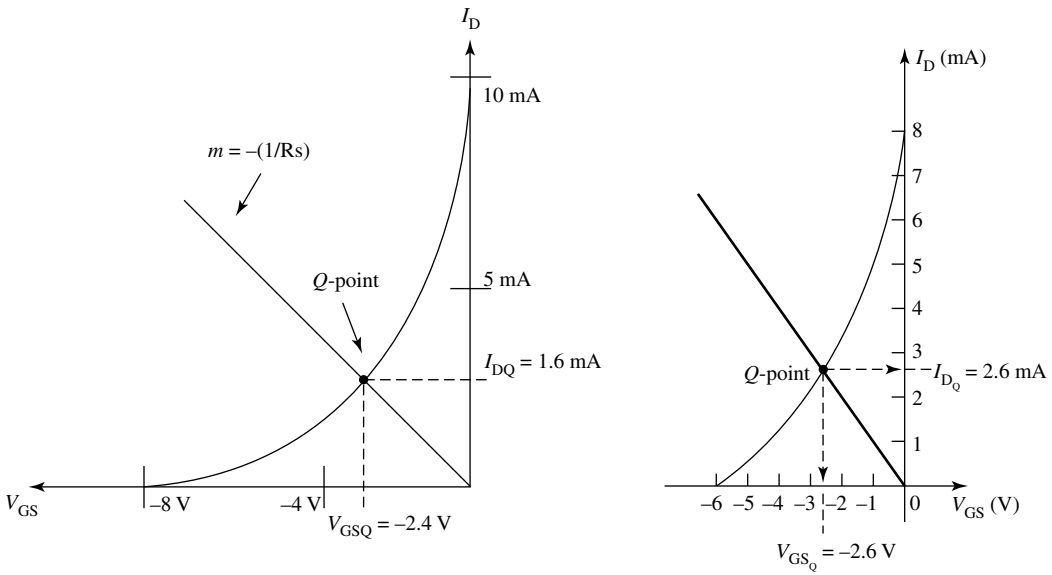


Fig. 10.17 Graphical method for Example 10.11

10.2.3 Comparison of FET and BJT

Bipolar Junction Transistors (BJTs) are referred to as conventional and Field Effect Transistors, (FETs) effectively replaced these devices in almost all areas of electronic circuit and system designs. BJTs being slightly bigger in size than FETs, in IC designs FETs are used. FETs offer very good noise immunity as compared to BJTs. A detailed comparison between FETs and BJTs is depicted in Table 10.3.

Table 10.3 Why are FETs pets to circuit designers?

Sl. No.	Factor	FET	BJT
1	Device type	Unipolar	Bipolar
2	Charge carriers	Only majority type	Both majority and minority
3	Device control	Voltage-controlled device, the conduction is controlled by gate-source voltage	Current-controlled device, the conduction is controlled by base current
4	Input impedance	High input impedance since input circuit is reverse biased (100 MΩ typical)	Low input impedance since input circuit is forward biased (2 – 4 kΩ typical)
5	Input current	Gate current is almost zero because of reverse bias	Base current is in the order of μA because of forward bias
6	Offset voltage	No	Yes
7	Noise immunity	More, noise is less as there are no junctions to cross for the charge carriers	Less, noise is more as charge carriers need to cross the junctions (BE and BC)
8	Thermal stability	More	Less
9	Device characterisation	Characterised by transconductance (g_m) and gate-source voltage controls the drain current	Characterised by current gain and base current controls collector current (α, β and γ)
10	Size	Smaller, suitable for integrated circuit designs	Bigger in size
11	GBW product	Less	More
12	Typical applications	VVR, ICs, switch, amplifiers, oscillators, etc.	Switch, amplifiers, oscillators, etc.

10.2.4 FET Applications

Like a conventional BJT, even a FET can be used for varieties of applications; some of the FET applications are switch, amplifier, oscillator, chopper (dc to dc converter), voltage variable resistor, etc. For simplicity, only two typical applications are discussed here in the following sub-sections; they are FET amplifier and FET VVR.

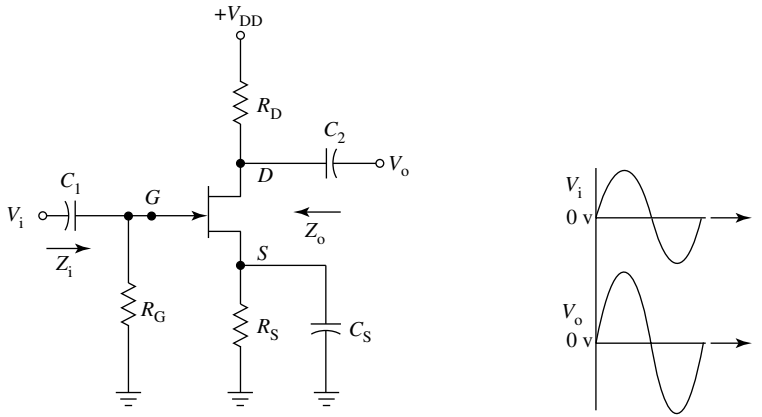
1. FET as an Amplifier

FET can be used as an amplifier to amplify an input signal. The strength of an input weak signal can be increased sufficiently to meet the requirements of any system design.

A small change in the reverse bias on the gate-source terminals causes a considerable change in the drain current and results in amplification of the input signal. During positive half cycle of the input signal, the reverse bias on the gate-source reduces increasing the drain current. This increases the output voltage and this is indicated in the waveforms shown in Fig. 10.18(b). Similarly, during the negative half cycle of the input, the reverse bias on gate-source increases, decreasing the channel width. This reduces the output, but in the opposite direction, thus providing the required amplification.

2. FET as a Voltage Variable Resistor (VVR)

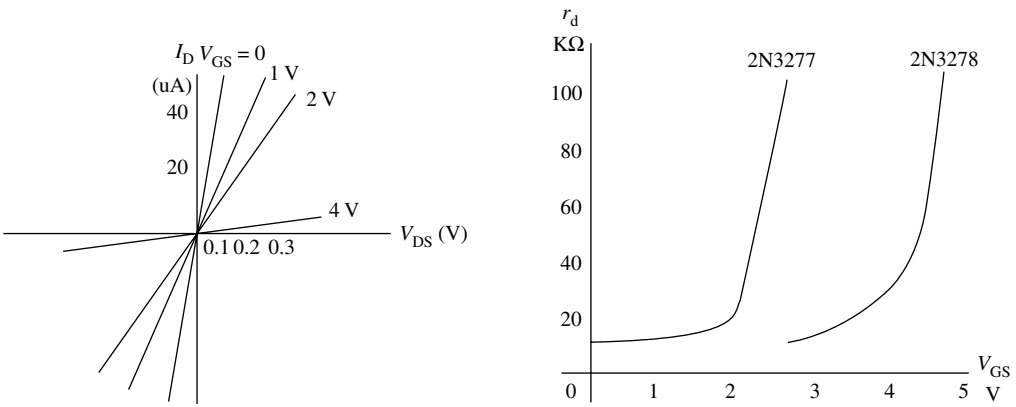
In most linear applications, FET is operated in the constant current portion of its output characteristics. When operated in the region before the pinch-off, where V_{DS} is small, the drain-to-source



(a) JFET amplifier circuit (b) Waveforms

Fig. 10.18 JFET amplifier

resistance is controlled by the bias voltage V_{GS}. Here, it is useful as voltage-controlled resistor or Voltage-Dependant Resistor (VDR). This is indicated in Fig. 10.19(a).



(a) VVR characteristics (b) VVR curves for 2N3277 and 2N3278

Fig. 10.19 JFET as a VVR

Consider the characteristic curves as shown in Fig. 10.19(b), the slope of these curves gives drain resistance $\boldsymbol{r_d}$ as a function of $\boldsymbol{V_{GS}}$ for two commercially available devices 2N3277 and 2N3278. It can be observed here that the device drain resistance varies from few tens of kΩ to few hundreds of kΩ for a small change in gate-source voltage. We have drain conductance for the device given by Eq. (10.29) and is for small values of V_{DS}.

Now,
$$g_d = g_{do}\left(1 - \frac{V_{GS}}{V_P}\right)^{\frac{1}{2}} \tag{10.29}$$

where
$$g_{do} = g_d \text{ with } V_{GS} = 0$$

Variation of r_d with V_{GS} is as shown in the graph of Fig. 10.19(a) and it can be closely approximated by the following equation:

$$r_d = \frac{r_o}{1 - kV_{GS}} \tag{10.30}$$

where $r_o = r_d$ with $V_{GS} = 0$ and k = constant dependant on FET.

FET as a VVR (V_{DR}) can be used in Automatic Gain Control (AGC). The gain of amplifier 'A' can be varied by providing a suitable feedback which changes the gate-to-source bias V_{GS}.

10.2.5 JFET Manufacturer's Specifications

Like other devices, even FET commercially comes out with a list of manufacturer's specifications. There are a large number of leading FET manufacturers and one leading name is Motorola. A few of the most important series manufactured by Motorola are BFW-10, 2N5457, etc. The specification sheets for both these devices, the 2N5457 and BFW-10, the *N*-channel JFET as provided by Motorola are provided in tables 10.4 and 10.5.

10.3 MOSFETs

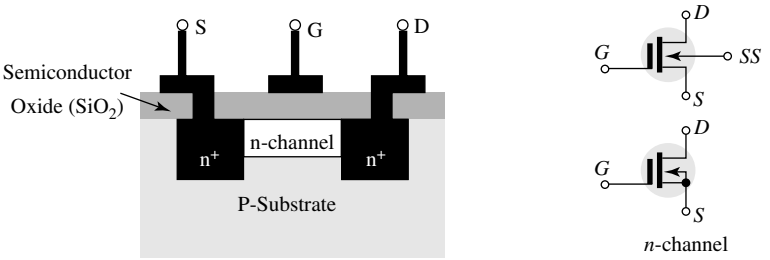
A field effect transistor can be constructed with the gate terminal insulated from the channel. A metal oxide semiconductor FET (MOSFET) or IGFET extension bits very high i/p impedance because of insulated gate terminal.

A MOSFET can be of two types:

(i) Depletion MOSFET
(ii) Enhancement MOSFET

10.3.1 Depletion MOSFET

In depletion MOSFET, a channel is physically constructed and current between drain and source results from a voltage connected between drain and source V_{DD}. Figure 10.20 shows the constructional details on a depletion-mode MOSFET. The *N*-channel depletion MOSFET is formed on a *P*-substrate (*P*-doped Si material on to which the FET structure is formed). The source and drain are connected by a metal (aluminium) to *N*-doped source and drain regions which are internally connected by *N*-doped channel. A metal layer is formed on the *N*-channel over a SiO_2 layer to form the gate terminal and the SiO_2 layer forms the insulation layer. The combination of metal gate on an oxide layer over a semiconductor substrate forms the depletion MOSFET.



(a) MOSFETS (b) Symbols

Fig. 10.20 MOSFETS

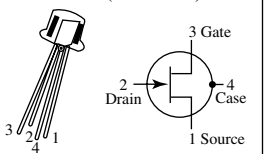
Table 10.4 Specification sheet for BFW-10

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Reverse Gate-Source Voltage	V_{GSR}	–30	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.71	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

BFW10/BFW11

CASE 20-30, STYLE 1
TO-72 (TO-206A)



JFET
VHF/UHF AMPLIFIER
N-CHANNEL–DEPLETION

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

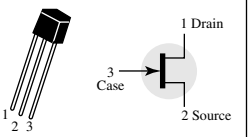
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	—	—	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 0.5 nAdc	BFW10 BFW11	$V_{GS(off)}$	—	—	8 6	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	0.1	nAdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 400 μAdc)	BFW10	V_{GS}	2	—	7.5	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 50 μAdc)	BFW11	V_{GS}	1.25	—	4	Vdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	BFW10 BFW11	I_{DSS}	8 4	— —	20 10	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)	BFW10 BFW11	γ_{fs}	3.5 3.0	— —	6.5 6.5	mmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	BFW10 BFW11	γ_{os}	— —	— —	85 50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)		C_{iss}	—	—	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)		C_{rss}	—	—	0.8	pF
Forward Transadmittance (V_{DS} = 15 Vdc, V_{DS} = 0, f = 200 MHz)		γ_{fs}	3.2	—	—	mmhos
Equivalent Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 25 Hz)		e_n	—	—	75	nV/VHz
Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0 V, see Figs 1, 2, 3)		NF	—	—	2.5	dB

Table 10.5 Specification sheet for 2N5457

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	–25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	$T_{\mu g}$	–65 to +150	°C

2N5457
CASE 29-04, STYLE 5
TO-92 (TO-226AA)



JFETs
GENERAL PURPOSE
N-CHANNEL–DEPLETION

ELECTRICAL CHARACTERISTICS (T_A = 25° C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = –10 μAdc, V_{DS} = 0)		$V_{(DR)GSS}$	–25	—	—	Vdc
Gate Reverse Current (V_{GS} = –15 Vdc, V_{DS} = 0) (V_{GS} = –15 Vdc, V_{DS} = 0, T_A = 100°C)		I_{GSS}	 — —	 — —	 –1.0 –200	nAdc
Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457	$V_{GS(off)}$	 –0.5	 —	 –6.0	Vdc
Gain Source Voltage (V_{DS} = 15 Vdc, I_D = 100 μAdc)	2N5457	V_{GS}	 —	 –2.5	 —	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current* (V_{DS} = 15 Vdc, V_{OS} = 0)	2N5457	I_{DSS}	 1.0	 3.0	 5.0	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5457	$\lvert y_{rs}\rvert$	 1000	 —	 5000	μmhos
Output Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\lvert y_{os}\rvert$	 —	 10	 50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	 —	 4.5	 7.5	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	 —	 1.5	 3.0	pF

Working

For an *N*-channel device, a negative gate-source voltage pushes electrons out of the channel region to deplete the channel and a large enough negative gate-source voltage on the other hand increases channel size, resulting in large drain current.

The device characteristics are as shown in Fig. 10.21. The device is shown to operate with either +ve or –ve gate-source voltage. The transfer characteristics is same for –ve V_s (in case of MOSFET as JFET) but it continues for +ve V_s. Since the gate is isolated from channel for both +ve and –ve V_s, the device can be operated (no gate current results in either case).

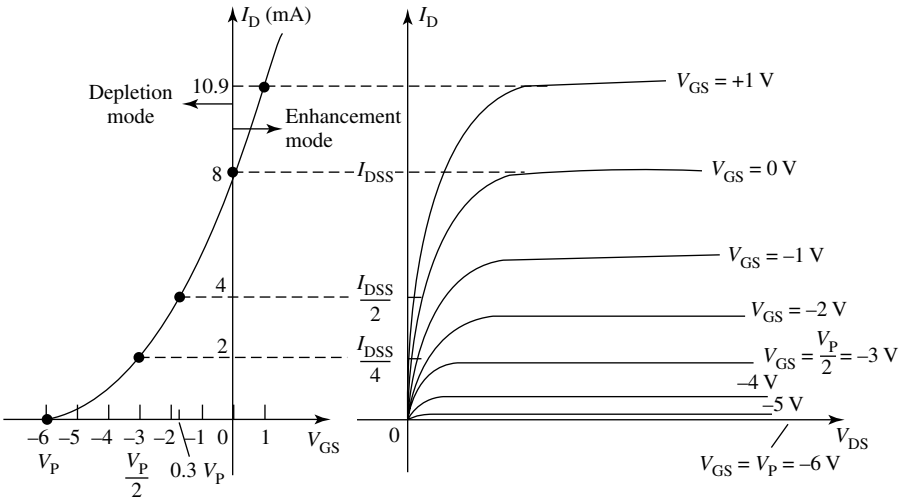


Fig. 10.21 *N*-channel MOSFET characteristics

The structure of a *P*-channel MOSFET and its symbol are shown in Fig. 10.22.

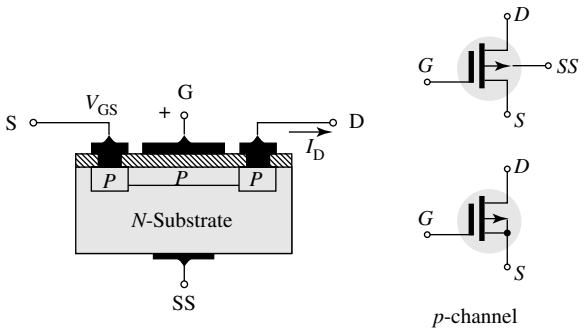


Fig. 10.22 *P*-channel MOSFET and its symbol

The *P*-channel MOSFET transfer and drain characteristics are shown in Fig. 10.23.

10.3.2 Enhancement MOSFET

In an enhancement MOSFET, no channel is formed (physically) when the device is constructed. Voltage is applied at the gate to develop a channel of charge carriers so that the current results when a voltage is applied across drain-source terminals. Figure 10.24 shows the *N*-channel, enhancement-type MOSFET with and without channel formation. It also contains its circuit symbol.

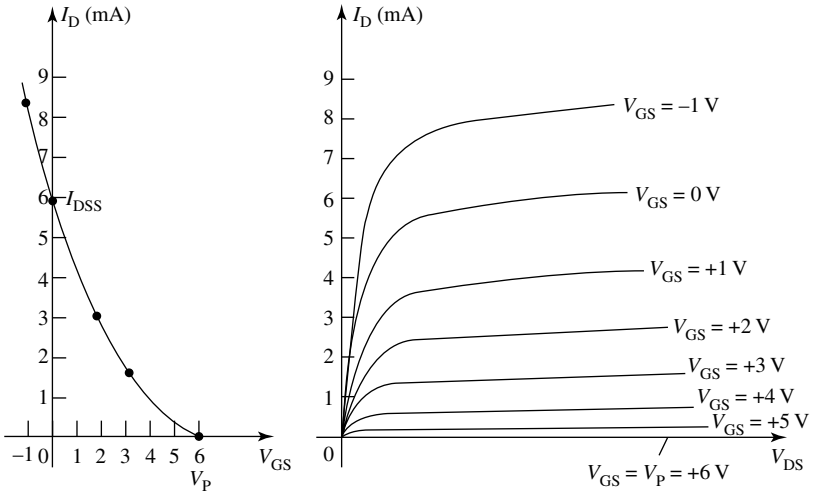
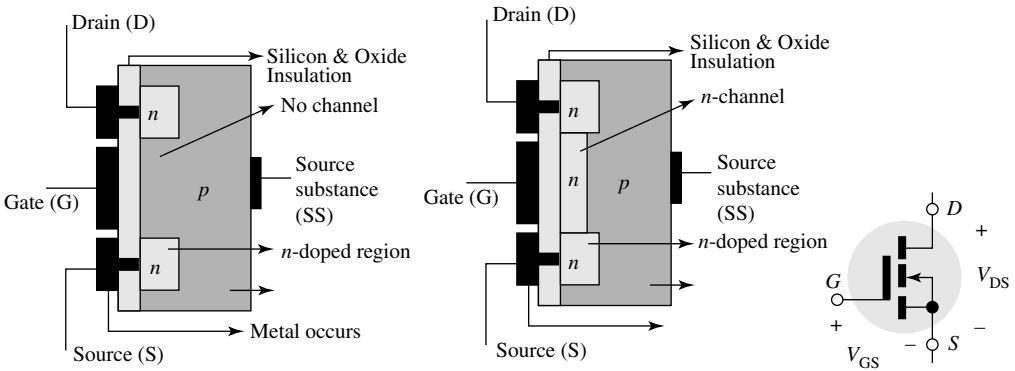


Fig. 10.23 *P*-channel MOSFET characteristics



(a) Enhancement MOSFET without channel formed (OFF state)

(b) Enhancement MOSFET with channel formed (ON state)

(c) Symbol

Fig. 10.24 Enhancement MOSFET

There is no channel as a past of the basic device construction. Application of positive gate-source voltage forms a depletion region under the gate, repelling the holes in the substrate under the gate. When gate voltage is sufficiently positive, electrons are attracted into this depletion region making it then act as an *N*-channel between drain and source. There is no drain current until gate source voltage reaches a value called V_T. Increased V_{GS} value above the V_T results in more drain current. The transfer characteristics and the drain characteristics are as shown in Fig. 10.25; the characteristics follow the equation

$$I_D = k\,(V_{GS} - V_T)^2 \qquad (10.31)$$

$$\text{for all } |V_{GS}| > |V_T|$$

where k typically is 0.3 mA/V^2 and is a property of device construction.

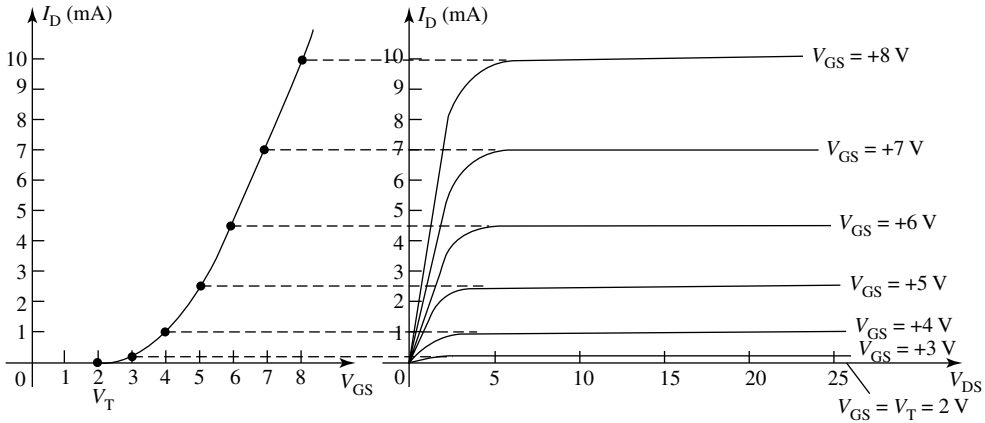


Fig. 10.25 Enhancement MOSFET characteristics

Note that no value of I_{DSS} is associated with I_D since at $V_{GS} = 0$, no I_D results, although the enhancement MOSFET is more restricted in operating range than a depletion MOSFET. It is very useful in LSI circuits as it is simpler in construction and small in size.

The symbol and characteristics of a *P*-channel enhancement MOSFET are as shown in Fig. 10.26.

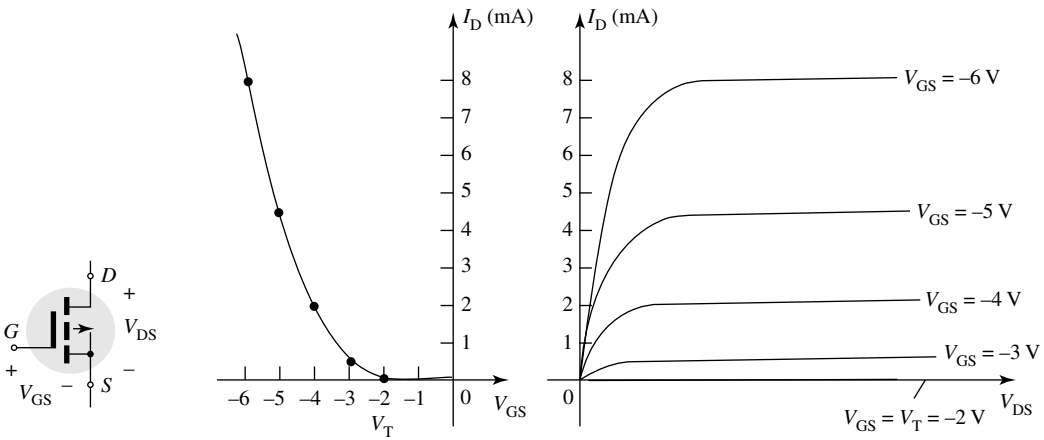


Fig. 10.26 Enhancement MOSFET symbol and characteristics

As in case of JFET and depletion MOSFET also, transconductance is defined by Eq. (10.32).

$$G_m = 2k\,(V_{GS} - V_P) \tag{10.32}$$

10.3.3 MOSFET Biasing

An enhancement MOSFET requires a gate-source voltage greater than its threshold voltage to drive the device on. The convention self-bias method cannot be used for an enhancement MOSFET. Since the drop across R_S reverse biases ($> V_T$) is required. The following two circuits shown in Fig. 10.27 can be used to bias an enhancement MOSFET.

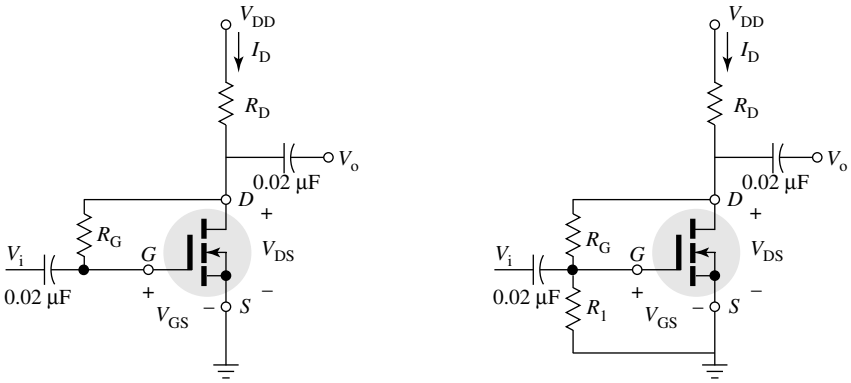


Fig. 10.27 MOSFET biasing circuits

Example 10.12

For the circuit shown using enhancement MOSFET, find I_{DQ} and V_{DSQ} values

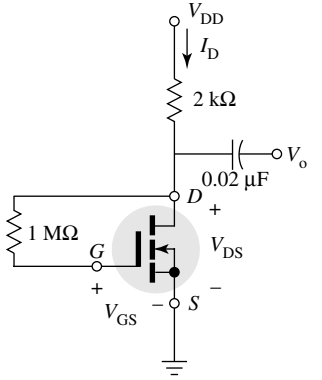


Fig. 10.28 Enhancement MOSFET for Example 10.12

Solution Assuming $k = 0.3$ mA/V^2 and using Eq. (10.31),

$$I_D = k\,(V_{GS} - V_T)^2$$
$$= 0.3 \times 10^{-3}(V_{DS} - 3)^2$$

$V_{GS(V)}$	$I_{D(\text{mA})}$
3	0
5	1.2
7	4.8
9	10.8

The load line using Eq. (10.8)

$$V_{DS} = V_{DD} - I_D R_D$$
$$= 12 - I_D\,(2 \times 10^{-3})$$

$I_{D(\text{mA})}$	$V_{DS(V)}$
0	12
6	0

Example 10.13

Draw the transfer class for the *N*-channel depletion MOSFET shown in Fig. 10.29.

Solution For depletion MOSFET, we have

$$I_D = I_{DSS}\,[1 - (V_{GS}/V_P)]^2$$
$$I_D = 6m\,[1 - (V_{GS}/-3)]^2$$

$V_{GS(V)}$	$I_{D(mA)}$
$(-0.4\ V_P) + 1.2$	12
0	6
$(0.3\ V_P) - 0.9$	3
$(0.5\ V_P) - 1.5$	1.5
$(V_P) - 3.0$	0

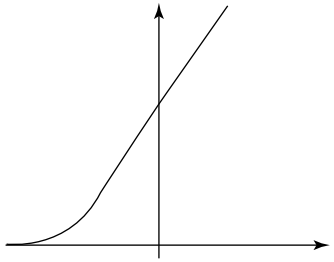


Fig. 10.29 *N*-channel depletion MOSFET for Example 10.13

Example 10.14

Design a voltage-divider bias circuit using a 2N3797 *N*-channel depletion MOSFET to operate at $I_D = 0.5I_{DSS}$, given supply voltage $V_{DD} = 15$ V.

Solution At $I_D = I_{DSS}/2 = 3$ mA. We have gate source V_g;

$$I_D = I_{DSS}\,[1 - (V_{GS}/V_P)]^2$$
$$3 \times 10^{-3} = 6 \times 10^{-3}\,[1 - (V_{GS}/-6)]^2$$
$$V_{GS} = -1.76\ \text{V}$$
$$V_{GS} \cong -1.8\ \text{V}$$

To find R_S, let us use the V_G expression

$$V_G = V_{GS} + I_D R_S$$

Let $V_G = 2$ V; then $2 = -1.8 + 3 \times 10^{-3}\ R_S$

$$\boxed{R_S = 1.3\ \text{k}\Omega}$$

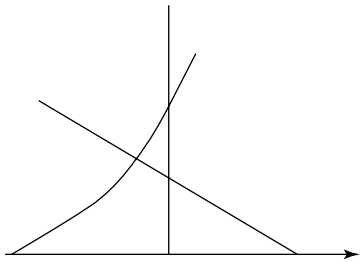


Fig. 10.30 *N*-channel depletion MOSFET for Example 10.14

Now V_D is limited between $V_{DD} = 12$ V and $V_S = 3.9$ V

Let $V_D = 8$ V

$$8 = V_{DD} - I_D R_D$$
$$R_D = 12.8/3\ \text{mA} = 1.3\ \text{k}\Omega$$

Also,

$$V_G = V_{GS} + V_S$$
$$= -1.8 + 3.9\ \text{V}$$
$$V_{DD} = R_2/(R_1 + R_2)$$
$$R_2/(R_1 + R_2) = V_G/V_{DD} = 2.1/12$$
$$(R_1 + R_2)/R_2 = 12/2.1 = 5.7$$
$$(R_1/R_2) + 1 = 5.7$$
$$(R_1/R_2) = 4.7$$

Let $R_1 = 47\ \text{m}\Omega$

i.e. $R_2 = 10\ \text{m}\Omega$

10.3.4 MOSFET Manufacturer's Specifications

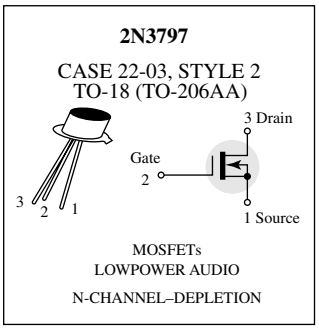
Like other devices, even MOSFET commercially comes out with a list of manufacturer's specifications. There are a large number of leading FET manufacturers and a few of the most important series

that are commercially available are 2N3797, the *N*-channel depletion type 2N4351, the *N*-channel enhancement type, etc. The specification sheets for both these devices, the 2N3797 and 2N4351, are provided in tables 10.6 and 10.7.

Table 10.6 Specification sheet for 2N3797

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drain-Source Voltage	2N3797	V_{DS}	20	Vdc
Gate-Source Voltage		V_{GS}	±10	Vdc
Drain Current		I_D	20	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C		P_D	200 1.14	mW mW/°C
Junction Temperature Range		T_1	+175	°C
Storage Channel Temperature Range		T_{stg}	–65 to +200	°C



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain Source Breakdown Voltage (V_{GS} = –7.0 V, I_D = 5.0 μA)	2N3797	$V_{(BR)DSX}$	20	25	—	Vdc
Gate Reverse Current (1) (V_{GS} = –10 V, V_{DS} = 0) (V_{GS} = –10 V, V_{DS} = 0, T_A = 150°C)		I_{GSS}	— —	— —	1.0 200	pADC
Gate Source Cutoff Voltage (I_D = 2.0 μA, V_{DS} = 10 V)	2N3797	$V_{GS(off)}$	—	–5.0	–7.0	Vdc
Drain-Gate Reverse Current (1) (V_{DG} = 10 V, I_S = 0)		I_{DGO}	—	—	1.0	pAdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0)	2N 3797	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current (V_{DS} = 10 V, V_{GS} = +3.5 V)	2N3797	$I_{D(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz) (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797 2N3797	$\lvert y_{fs}\rvert$	1500 1500	2300 —	3000 —	μmhos
Output Admittance (I_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3797	$\lvert y_{os}\rvert$	—	27	60	μmhos
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797	C_{iss}	—	6.0	8.0	pF
Reverse Transfer Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	—	0.5	0.8	pF

Table 10.7 Specification sheet for 2N4351

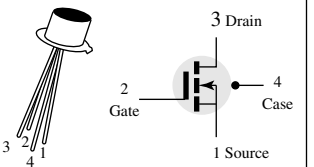
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW°C
Junction Temperature Range	T_j	175	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

*Transient potentials of ±75 Volt will not cause gate-oxide failure.

2N4351

CASE 20-03, STYLE 2
TO-72 (TO-206AF)



MOSFET SWITCHING

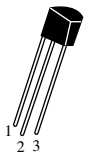
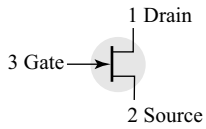
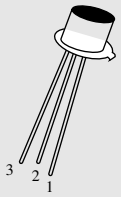
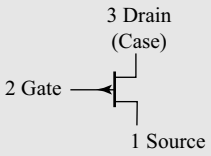
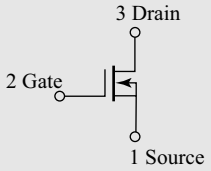
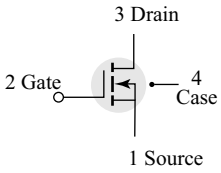
N-CHANNEL—ENHANCEMENT

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (I_D = 10 μA, V_{GS} = 0)	$V_{(BR)DSX}$	25	—	Vdc
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0) T_A = 25°C T_A = 150°C	I_{DSS}	 — —	 10 10	 nAdc μAdc
Gate Reverse Current (V_{GS} = ±15 Vdc, V_{DS} = 0)	I_{GSS}	—	±10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 μA)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage (I_D = 2.0 mA, V_{GS} = 10 V)	$V_{DS(on)}$	—	1.0	V
On-State Drain current (V_{GS} = 10 V, V_{DS} = 10 V)	$I_{D(on)}$	3.0	—	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (V_{DS} = 10 V, I_D = 2.0 mA, f = 1.0 kHz)	$\|y_{fs}\|$	1000	—	μmho
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz)	C_{iss}	—	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	C_{rss}	—	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz)	$C_{d(sub)}$	—	5.0	pF
Drain-Source Resistance (V_{GS} = 10 V, I_D = 0, f = 1.0 kHz)	$r_{ds(on)}$	—	300	ohms

Characteristic		Symbol	Min	Max	Unit
SWITCHING CHARACTERISTICS					
Turn-On Delay (Fig. 5)	I_D = 2.0 mAdc, V_{DS} = 10 Vdc, (V_{GS} = 10 Vdc) (See Fig. 9: Times Circuit Determined)	t_{d1}	—	45	ns
Rise Time (Fig. 6)		t_f	—	65	ns
Turn-Off Delay (Fig. 7)		t_{d2}	—	60	ns
Fall Time (Fig. 8)		t_f	—	100	ns

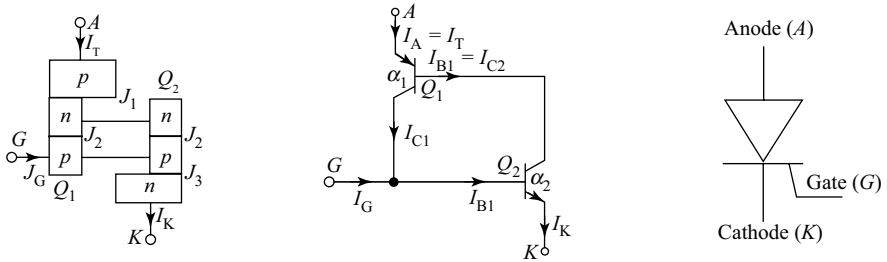
Table 10.8 Different FETs and MOSFETs

FETs	Device	Symbol
2N5457		
2N2844		
MOSFETs		
2N3797 Depletion-type *N*-channel MOSFET		
2N4351 Enhancement-type *N*-channel MOSFET		

10.4 SILICON-CONTROLLED RECTIFIER (SCR)

In Chapter 2, one of the important applications of the conventional *PN* junction diode, the rectifiers, is presented. In these conventional rectifiers, there is no control on the amount of power that is delivered to the load. In order to precisely control the load power, a silicon-controlled rectifier can be used. A Silicon-Controlled Rectifier (SCR), also called **Shockley diodes**, are curious devices, whose limited applications may be expanded by equipping them with another means of latching. An SCR is a four-layered, three-junction, three-terminal *PNPN* switching silicon device. Two transistors, a *PNP* and an *NPN*, are connected back to back to form a four-layered, three-junction device as indicated in

Fig. 10.31(a). The three terminals are Anode (A), Cathode (K) and the Gate (G); the cathode gate here forms a PN junction (J_3). An SCR can be analysed now using the transistor equivalent model shown in Fig. 10.31(b) and its circuit symbol is shown in Fig. 10.31(c). In order that an SCR works as a switch, its anode-cathode terminals are applied with a large positive voltage $\boldsymbol{V_{AK}}$. However, the gate terminal being connected directly to the base of the transistor Q_2, the SCR may be latched or turned on at relatively lower $\boldsymbol{V_{AK}}$ values.



(a) Silicon-controlled rectifier (b) Two-transistor equivalent (c) Symbol

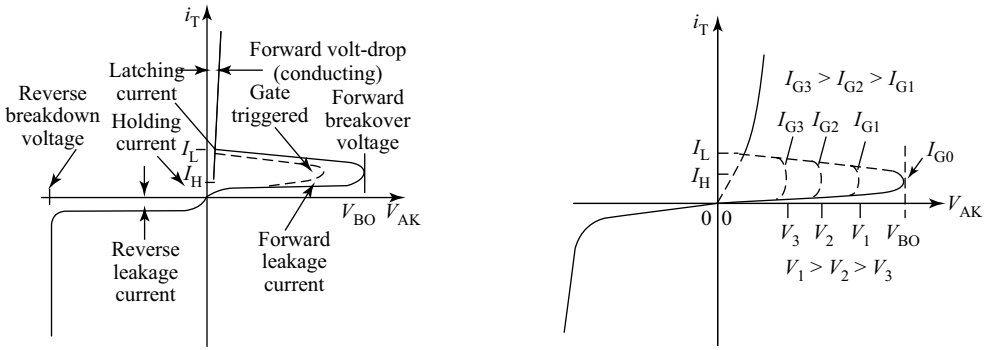
Fig. 10.31 Silicon-controlled rectifier

By applying a small voltage between the gate and cathode, the lower transistor Q_1 will be forced on by the resulting base current, which will cause the upper transistor Q_1 to conduct, which then supplies the lower transistor's base current so that it no longer needs to be activated by a gate voltage. The necessary gate current to initiate latch-up will be much lower than the current through the SCR from cathode to anode. This method of securing SCR conduction is called **triggering** and it is by far the most common way that SCRs are latched in actual practice. In fact, SCRs are usually chosen so that their breakover voltage is far beyond the greatest voltage expected to be experienced from the power source, so that it can be turned on only by an intentional voltage pulse applied to the gate.

10.4.1 SCR Characteristics

When a voltage is applied between the anode and cathode terminals, junctions J_1, J_3 are forward biased and J_2 is reverse biased. This situation continues till the anode-cathode voltage reaches a value called the **forward breakover voltage ($\boldsymbol{V_{FBO}}$)** and this state of SCR is called **forward blocking state**. This is indicated in Fig. 10.32 (a).

It should be noted that SCRs have large V_{FBO} value and need sufficient gate drive to turn on with lesser breakover voltage. Further increase in the anode-cathode voltage turns on the device and the anode current suddenly shoots up. The value of anode current once SCR starts conduction from the forward blocking state is called **latching current $\boldsymbol{I_L}$**. Increasing the gate drive steadily reduces the required anode-cathode voltage and this is indicated in Fig. 10.32(b). To turn off a conducting SCR, now the gate terminal cannot be used. Once the SCR starts conduction, the two-transistor analogy does not hold good and the gate loses its control over the conduction. In order to turn off the device, the anode-cathode voltage should be reduced such that the anode current reduces. The anode current falls sufficiently below the latching value I_L, suddenly drops to zero and the SCR fails to remain ON. The value of anode current below which the SCR fails to remain ON is called **holding current $\boldsymbol{I_H}$**. This is indicated in Fig. 10.32(a). It should be mentioned that SCRs may sometimes be turned off by directly applying a negative anode-cathode voltage so that the device is forced to turn off.



(a) *VI* characteristics (b) Effect of gate drive on SCR latching

Fig. 10.32 SCR characteristics

The SCR anode current I_A is given by an expression containing the current gains α_1 and α_2 for the transistors, the collector leakage current I_{CO} and the gate drive I_g.

$$I_A = \frac{I_{CO} + I_g}{1 - (\alpha_1 + \alpha_2)} \tag{10.33}$$

1. SCR Turn-on Methods

There are five basic methods to turn on SCRs and are listed below;

(a) Gate Triggering It is the most popular and useful method of triggering an SCR. It can be achieved by applying a small drive to the gate terminal with an anode-to-cathode forward voltage applied.

(b) $\frac{dv}{dt}$ Triggering If the rate of rise of forward voltage exceeds the critical rate of rise of voltage then the SCR gets triggered.

(c) V_{BO} (Breakdown Voltage) Triggering When the forward voltage is made very high, due to the avalanche charge multiplication at junction J_2, the device gets turned ON.

(d) Thermal Triggering When the SCR is applied with a forward voltage very near to the breakover voltage then the increase in the operating temperature turns the SCR ON as the increase in temperature decreases the width of the depletion region.

(e) Photon Triggering When the SCR is biased to the nearest value of breakdown voltage then a light focused on to it generates excess electron hole pairs result in triggering the SCR. These devices are referred as Light-Activated SCRs (LASCRs).

2. SCR Turn-off Methods

The SCR can be turned off by reducing its anode current below the holding current level. There are two turn-off methods available.

(a) Natural Turn-off or Commutation When input to the SCR is an ac signal then naturally the anode current reduces below the holding current level because of the negative input signal and hence SCR turns off automatically.

(b) Forced Turn-off or Commutation If the input applied to the SCR does not make the anode current reduce below the holding current then a reverse bias is applied to turn off and is called the forced commutation method.

3. SCR Testing

A rudimentary test of SCR functioning, or at least terminal identification, may be performed with an ohmmeter. Because the internal connection between gate and cathode is a single *PN* junction, a meter should indicate continuity between these terminals with the red test lead on the gate and the black test lead on the cathode. This is indicated in Fig. 10.33.

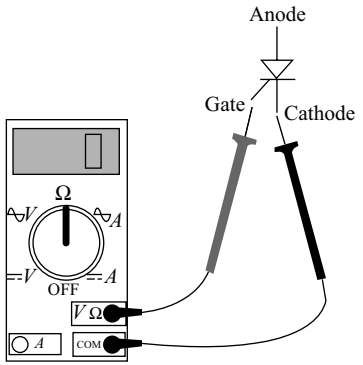


Fig. 10.33 SCR testing

All other continuity measurements performed on an SCR will show "open" ("OL" on some digital multimeter displays). It must be understood that this test is very crude and does not constitute a comprehensive assessment of the SCR. It is possible for an SCR to give good ohmmeter indications and still be defective. Ultimately, the only way to test an SCR is to subject it to a load current. If you are using a multimeter with a "diode check" function, the gate-to-cathode junction voltage indication you get may or may not correspond to what's expected of a silicon *PN* junction (approximately 0.7 volts). In some cases, you will read a much lower junction voltage: mere hundredths of a volt. This is due to an internal resistor connected between the gate and cathode incorporated within some SCRs. This resistor is added to make the SCR less susceptible to false triggering by spurious voltage spikes, from circuit "noise" or from static electric discharge. In other words, having a resistor connected across the gate-cathode junction requires that a strong triggering signal (substantial current) be applied to latch the SCR. This feature is often found in larger SCRs, but not in small SCRs. Bear in mind that an SCR with an internal resistor connected between gate and cathode will indicate continuity in both directions between those two terminals.

10.4.2 SCR Applications

A SCR finds varieties of applications in the field of electronics and a few of them are as listed below:

1. For controlled rectification, that is to control the amount of power fed to load
2. For motor-speed control
3. For temperature and illumination control
4. For ac and dc circuit breaker
5. Variable frequency inverter (dc to ac)
6. Variable voltage converter (ac to dc)
7. Variable dc to dc converter (chopper)
8. Used as cyclo-converter (up conversion of frequency) and as cyclo-converter (down conversion of frequency)

Figure 10.34 is an example of SCR applications; the SCR half-wave rectifier and the corresponding waveforms are shown. The input to the circuit is a sine wave which drives the SCR into forward blocking state during the positive half cycle.

Figure 10.35 is another example of SCR applications; the SCR heater control shown consists of a transducer (discussed in Chapter 9) in the form of an RTD, a heater element, diodes and few passive components. RTD is a temperature-dependant resistor with negative temperature coefficient (whose resistance varies inversely as the temperature).

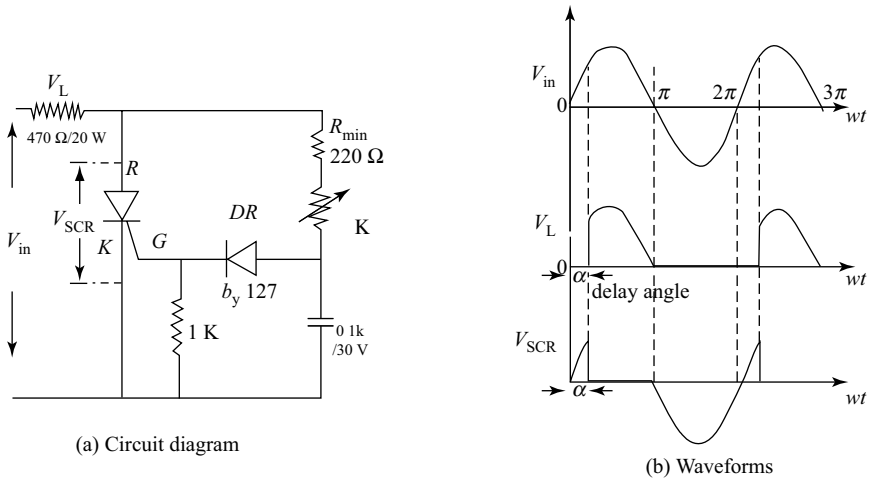


Fig. 10.34 SCR half-wave rectifier

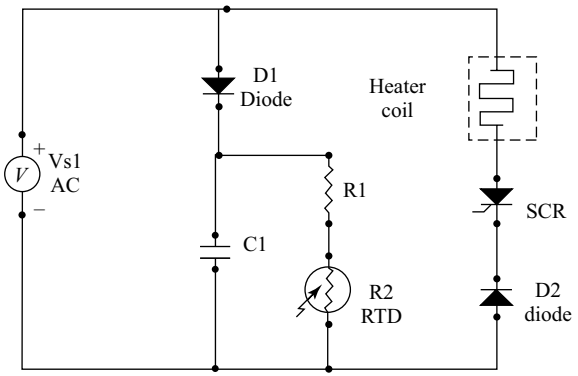


Fig. 10.35 SCR heater control

If the heater coil is radiating the required temperature then the phase control of SCR remains unaltered.

If temperature increases then the resistance of RTD decreases which makes the time constant increasing and hence triggering of SCR is delayed. This varies α, the firing angle, up thus reducing the voltage applied to the heater and hence radiated temperature is reduced. Similarly, if temperature decreases then the resistance of RTD increases which makes the time constant decreasing and hence triggering of SCR is advanced This shifts 'α', the firing angle, down thus increasing the voltage applied to the heater and hence radiated temperature is increased.

10.4.3 SCR Manufacturer's Specifications

Like other devices, even SCR commercially comes out with a list of manufacturer's specifications. There are a large number of leading SCR manufacturers and one of the most important commercially available devices is TYN612. The specification sheet for this device is provided in Table 10.9.

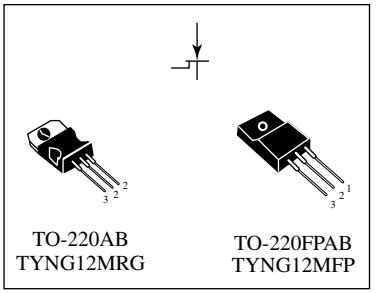
Table 10.9 Specification sheet for TYN612

TYN612M

12 A SCR

Main features

Symbol	Value	Unit
$I_{T(RMS)}$	12	A
V_{DRM}/V_{RRM}	600	V
I_{GT}(min/max)	1.5/5	mA



TO-220AB TYNG12MRG

TO-220FPAB TYNG12MFP

Description

The TYN612M SCR is suitable to fit modes of control found in applications such as voltage regulation circuits for motorbikes, overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, inrush current limiting circuits, capacitive discharge ignition.

The insulated fullpack package allows a back to back configuration.

Order codes

Part Numbers	Marketing
TYN612MRG	TYN612M
TYN612MFP	TYN612MFP

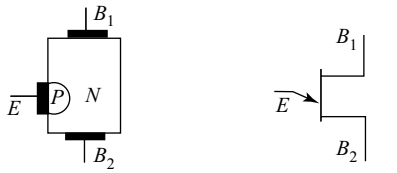
Absolute ratings (limiting values)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)	TO-220AB	T_c = 105°C	12	A
		TO-220FPAB	T_c = 70°C	12	
$I_{T(AV)}$	Average on-state current (180° conduction angle)	TO-220AB	T_c = 105°C	8	A
		TO-220FPAB	T_c = 70°C	8	
I_{TBM}	Non repetitive surge peak on-state current	t_p = 8.3 ms	T_j = 25°C	125	A
		t_p = 10 ms		120	
I^2t	I^2t Value for fusing	t_p = 10 ms	T_j = 25°C	72	A^2s
dI/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100$ ns	F = 60 Hz	T_j = 125°C	50	A/μs
I_{GM}	Peak gate current	t_p = 20 μs	T_j = 125°C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125°C	1	W
T_{stg}	Storage junction temperature range			–40 to + 150	°C
T_j	Operating junction temperature range			–40 to + 125	
V_{RGM}	Maximum peak reverse gate voltage			5	V

10.5 UNIJUNCTION TRANSISTOR (UJT)

The UJT is a three-terminal device with only one *PN* junction. A slab of lightly doped (increased resistance characteristics) *N*-type silicon material has two base contacts at both ends. It is also called **double-base diode**. The junction is formed closer to base-2. Here, the conduction is due to only one type of charge carriers, i.e. holes and thus it is a unipolar device (like FET and unlike BJT). The

arrowhead indicates the flow of conventional current. The UJT construction and the circuit symbol are shown in Fig. 10.36. There is a single *PN* junction formed and the charge carriers are only holes.

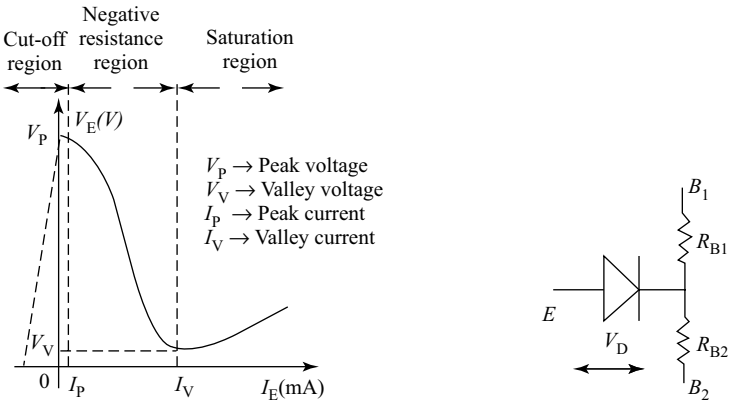


(a) Unijunction transistor (b) Symbol

Fig. 10.36 UniJunction Transistor (UJT)

The working principle of an UJT can be better understood through the *VI* characteristic curves of the device shown in Fig. 10.37(a). It is clear that in the *VI* characteristics shown, for all emitter potentials less than V_P, I_E is never greater than I_{EO} [(few μA) which corresponds to (very closely) I_{CO} of a BJT]. This region is called **cut-off region** and is indicated on the curve. Once conduction starts at $V_E = V_P$, the emitter potential V_E drops and I_E increases. The emitter current continues to increase and the emitter potential drops to lowest called **valley voltage**. The region between VV and V_P observes an increase in emitter current for reducing emitter voltages and is called **negative resistance region**. Eventually, after the valley point is reached, any further increase in I_E places the device in 'saturation region' and hereafter emitter current and emitter voltage both increase.

The decrease in resistance in the active region is due to the holes injected into *N*-type slab from the aluminum *P*-type rod when conduction is established. This increased holes increases conductivity (G).



(a) *VI* characteristics (b) Equivalent circuit

Fig. 10.37 UJT relaxation oscillator

Figure 10.38(b) represents the equivalent circuit for the UJT; R_{B1} and R_{B2} represent the base resistances for B_1 and B_2 respectively. The inter-base resistance R_{BB} is the summation of resistances of the device between B_1 and B_2 with $I_E = 0$,

i.e. $$R_{BB} = (R_{B1} + R_{B2}) \text{ at } I_E = 0 \qquad (10.34)$$

R_{BB} is typically in the range of 4 to 10 kΩ. The position of aluminum rod (forming *PN* junction) determines the relative values of R_{B1} and R_{B2} with $I_E = 0$. The magnitude of V_{RB1} is determined by the following equation:

$$V_{RB1} = V_{BB} \frac{R_{B1}}{R_{B1} + R_{B2}} \qquad [10.35(a)]$$

$$V_{RB1} = \eta V_{BB} \text{ with } I_E = 0 \qquad [10.35(b)]$$

where η is the intrinsic stand-off ratio.

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} \qquad (10.36)$$

Typical η value for a device like 2N2646 ranges from 0.6 to 0.93. Considering the equivalent circuit, we can write

$$V_E = V_{RB1} + V_D$$
$$V_E = \eta V_{BB} + V_D$$
$$V_P = nV_{BB} + V_D \tag{10.37}$$

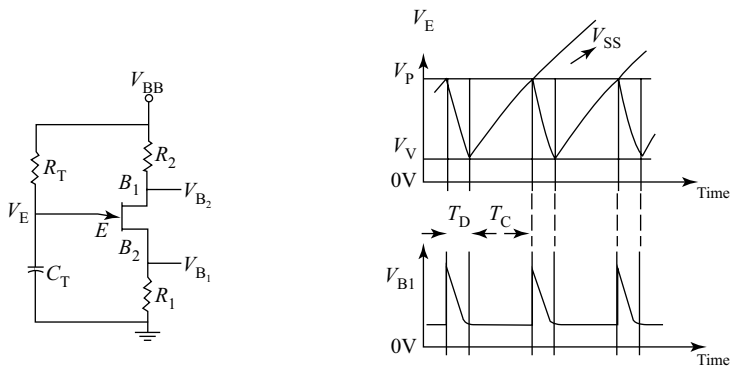
where, V_{BB} is the applied voltage between B_1 and B_2,
V_D is the diode drop, which is typically 0.5 to 0.7 V, and
η and V_D being constants, the magnitude of V_P depends on V_{BB} used.

1. Applications

A UJT can be used in a variety of applications and a few of them are listed as below:

- To construct negative resistance oscillators (without any feedback)
- To trigger SCRs (spikes generator)
- As sawtooth waveform generators
- Phase control, timing circuits, bi-stable networks, voltage or current regulated supplies, and so on

Figure 10.38 represents the circuit diagram and the corresponding waveforms of a relaxation oscillator using UJT. This oscillator incorporates no feedback and works on the principle of negative resistance property of the device. The expression for the output frequency in terms of the circuit parameters is given in Eq. (10.38).



(a) UJT relaxation oscillator circuit (b) Waveforms

Fig. 10.38 UJT relaxation oscillator

The output frequency is given by

$$f = \frac{1}{T} = \frac{1}{T_c + T_d} \tag{10.38}$$

where T_c is the capacitor charging period and T_c is the capacitor discharging period.

Now, $T = T_C + T_d$
$T \approx T_C$ because the discharge period is very small.

Using basic capacitor voltage equation, the final expression for the charging period can be derived as given by Eq. (10.39).

$$T_c = RC \log_e \frac{V_{BB} - V_V}{V_{BB} - V_P}$$

$$T_c = \text{RC} \log_e \left[\frac{V_{BB} - V_V}{V_{BB} - [\eta V_{BB} + V_D]} \right] \tag{10.39}$$

Since $V_{BB} >> V_V$ and V_D

$$T_c = \text{RC} \log_e \left[\frac{V_{BB}}{V_{BB} - \left[\eta V_{(BB]}\right)} \right]$$

$$T_c = \text{RC} \log_e \left[\frac{1}{1 - \eta} \right] \tag{10.40}$$

Example 10.15

For a certain UJT, the base-1 internal resistance is double the base-2 internal resistance. Calculate the intrinsic stand-off ratio for the device.

Solution Given $\boldsymbol{R_{B1} = 2\, R_{B2}}$ and from Eq. (10.36),

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

$$\eta = \frac{2R_{B2}}{2R_{B2} + R_{B2}}$$

$$\eta = \frac{2}{3} = 0.6$$

2. UJT Manufacturer's Specifications

Like other devices, even UJT commercially comes out with a list of manufacturer's specifications. There are a large number of leading FET manufacturers and one leading name is Philips Semiconductors. One of the most popular UJTs manufactured by them is 2N2646. The specification sheet for this device 2N2646, the silicon *PN*-UJT as provided by Philips Semiconductors is provided in Table 10.10.

Example 10.16

For a certain UJT, the base-1 internal resistance is 2.5 times the base-2 internal resistance. Calculate the peak voltage V_P if the device operates with a supply voltage of 10 V.

Solution Given $R_{B1} = 2R_{B2}$ and from Eq. (10.36),

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

$$\eta = \frac{2.5R_{B2}}{2.5R_{B2} + R_{B2}}$$

$$\eta = \frac{2.5}{3.5} = 0.7143$$

Now, from Eq. (10.36) and Eq. (10.27), the peak voltage is given by

$$V_P = nV_{BB} + V_D$$
$$= (0.7143 \times 10 + 0.6)\ \text{V}$$
$$= 7.743\ \text{V}$$

Table 10.10 Specification sheet for 2N2646

2N2646
Silicon unijunction transistor

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{EB2}	emitter-base 2 voltage		—	—	30	V
I_{EM}	emitter current	peak value	—	—	2	A
P_{tot}	total power dissipation		—	—	300	mW
T_J	junction temperature		—	—	125	°C
R_{BB}	static inter-base resistance	$V_{B2B1} = 3$ V $I_E = 0$	—	7	—	kΩ
V_{E01sat}	emitter-base 1 saturation voltage	$V_{B2B1} = 10$ V $I_E = 50$ mA	—	3.5	—	V
$I_{E(V)}$	emitter valley point current		4	6	—	mA
$I_{E(P)}$	emitter peak point current		—	1	5	μA

PINNING-TO-18
Base 2 connected to case.

Pin	Description
1	emitter
2	base 1
3	base 2

PIN CONFIGURATION

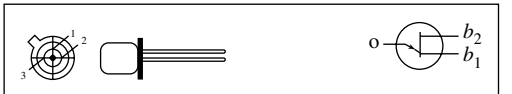


Fig. 1 Simplified outline and symbol.

LIMITING VALUES
In accordance with the Absolute Maximum System (IEC 134).

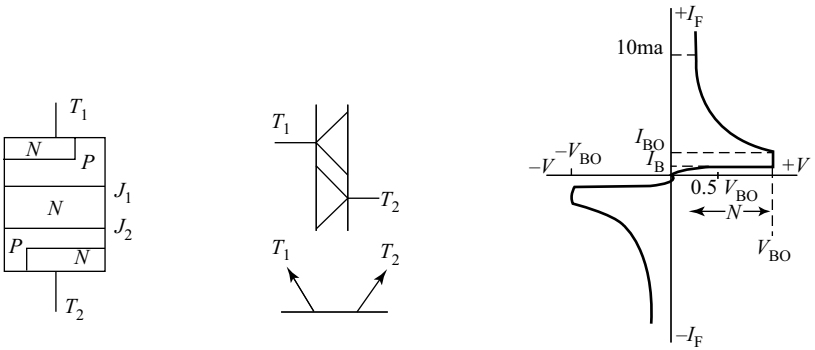
Symbol	Parameter	Conditions	Min.	Max.	Unit
$-V_{EB2}$	emitter-base 2 voltage		—	30	V
V_{B2B1}	inter-base voltage		—	35	V
I_E	emitter current	average value	—	50	mA
I_{EM}	emitter current (note 1)	peak value	—	2	A
P_{tot}	total power dissipation (note 2)	$T_{amb} \leq 25$°C	—	300	mW
T_{stg}	storage temperature range		–65	150	°C
T_J	junction temperature		—	125	°C

Notes
1. Capacitor discharge ≤ 10 μF at ≤ 30 V.
2. Must be limited by external circuit.

10.6 OTHER SPECIAL DEVICES

10.6.1 DIAC

Like all other diodes, Shockley diodes are unidirectional devices and they only conduct current in one direction. If bidirectional (ac) operation is desired, two Shockley diodes may be joined in parallel facing different directions to form a new kind of thyristor, called the DIAC. A DIAC is a five-layered, four-junction, two-terminal, bi-directional device. It is equivalent to two parallelly connected diodes and can be operated on either polarity of voltages. The constructional details, circuit symbol (two) and the *VI* characteristics of the DIAC are shown in Fig. 10.39.



(a) Construction (b) Symbols (c) *VI* characteristics

Fig. 10.39 DIAC, the bidirectional diode

As shown in the *VI* characteristics, till the applied voltage reaches the breakover voltage V_{BO} (avalanche breakover), the current through the device will be very small and negligible. Once V_{BO} is crossed, the device current increases and the voltage decreases; the device exhibits a negative resistance. A DIAC is a bilateral device and hence its *VI* characteristics are symmetrical about the *x*-axis, except the phase reversal. A DIAC operated with a dc voltage across it behaves exactly the same as a Shockley diode. With ac, however, the behaviour is different from what one might expect. Because alternating current repeatedly reverses direction, DIACs will not stay latched longer than one half cycle. If a DIAC becomes latched, it will continue to conduct current only as long as there is voltage available to push enough current in that direction. When the ac polarity reverses, as it must twice per cycle, the DIAC will drop out due to insufficient current, necessitating another breakover before it conducts again. The result is a current waveform that looks as shown in Fig. 10.40.

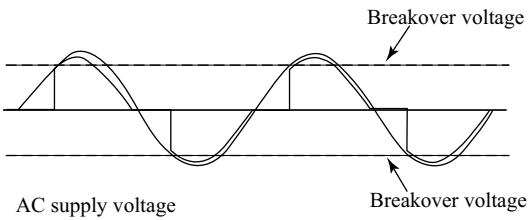


Fig. 10.40 DIAC bidirectional waveforms

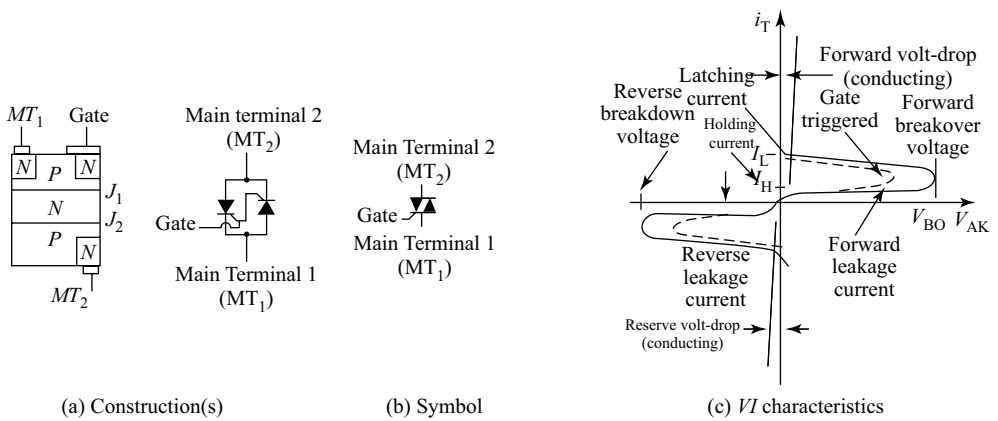
DIACs are almost never used alone, but in conjunction with other thyristor devices.

A DIAC also finds a variety of applications:

1. For TRIAC triggering
2. Speed control of universal motor, and so on

10.6.2 TRIAC

An SCR being a unidirectional current device, it is useful for controlling dc powers only and in order to achieve ac power controls, two SCRs are to be connected back to back. A TRIAC is just similar to such an operation. It is a three-terminal, bilateral device that is equivalent to two back-to-back connected SCRs with only one gate to control (converse parallel connection). The constructional details, circuit symbol and the *VI* characteristics of the TRIAC are shown in Fig. 10.41.



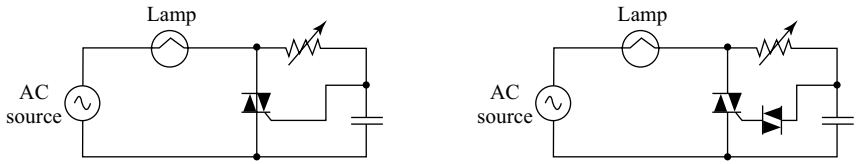
(a) Construction(s) (b) Symbol (c) *VI* characteristics

Fig. 10.41 TRIAC, the bidirectional SCR

A TRIAC can block voltages of either polarity, conduct in both the directions and hence it is very useful in ac power controls. The converse parallel connection property is the result of the junction structure shown in Fig. 10.41(a). The *N*-type emitter at MT_2 is directly located opposite to the *P*-type emitter at MT_1 and the *P*-type emitter at MT_2 is directly located opposite to *N*-type emitter at MT_1. The gate terminal makes the ohmic contact with both *P* and *N*-type materials, thus enabling the use of either positive or negative triggering pulses. The *VI* characteristics shown in Fig. 10.41(c) indicate that it is equivalent to SCR forward curves, but in I and III quadrants. A TRIAC switches on for voltages above V_{FBO} in both the directions. There are four modes of operation for a TRIAC and they are

(a) MT_2 to MT_1 voltage positive and gate to MT_1 voltage is positive (I Quadrant)
(b) MT_2 to MT_1 voltage positive and gate to MT_1 voltage is negative (I Quadrant)
(c) MT_2 to MT_1 voltage negative and gate to MT_1 voltage is negative (III Quadrant)
(d) MT_2 to MT_1 voltage negative and gate to MT_1 voltage is positive (III Quadrant)

Because individual SCRs are more flexible to use in advanced control systems, they are more commonly seen in circuits like motor drives, while TRIACs are usually seen in simple, low-power applications like household dimmer switches. A simple lamp-dimmer circuit is shown in Fig. 10.42(a), complete with the phase-shifting resistor-capacitor network necessary for triggering.



(a) Simple RC triggering (b) DIAC triggering

Fig. 10.42 TRIAC light dimmer

TRIACs are notorious for not triggering symmetrically. This means they usually won't trigger at the exact same gate voltage level for one polarity as for the other. Generally speaking, this is undesirable, because unsymmetrical triggering results in a current waveform with a greater variety of harmonic frequencies. Waveforms that are symmetrical above and below their average centrelines are comprised of only odd-numbered harmonics. Unsymmetrical waveforms, on the other hand, contain even-numbered harmonics (which may or may not be accompanied by odd-numbered harmonics as well). In the interest of reducing total harmonic content in power systems, the fewer and less diverse the harmonics, a better and alternate arrangement shown in Fig. 10.42(b) may be used. One way to make the TRIAC's current waveform more symmetrical is to use a device external to the TRIAC to time the triggering pulse. A DIAC placed in series with the gate does a fair job of this; DIAC breakover voltages tend to be much more symmetrical (the same in one polarity as the other) than TRIAC triggering voltage thresholds. Since the DIAC prevents any gate current until the triggering voltage has reached a certain, repeatable level in either direction, the triggering point of the TRIAC from one half-cycle to the next tends to be more consistent, and the waveform more symmetrical above and below its centreline. Practically, all the characteristics and ratings of SCRs apply equally to TRIACs, except that TRIACs of course are bidirectional (can handle current in both directions). Not much more needs to be said about this device except for an important caveat concerning its terminal designations.

The key to successfully triggering a TRIAC is to make sure the gate receives its triggering current from the main terminal 2 side of the circuit (the main terminal on the opposite side of the TRIAC symbol from the gate terminal). Identification of the MT_1 and MT_2 terminals must be done via the TRIAC's part number with reference to a data sheet or book.

A TRIAC being a more versatile device finds a variety of applications. Some of them are

1. For power control in ac applications
2. For speed control ac, dc and universal motors
3. In light dimmer network, and so on

10.6.3 Silicon Controlled Switch (SCS)

If we take the equivalent circuit for an SCR and add another external terminal, connected to the base of the top transistor and the collector of the bottom transistor, we have a device known as a silicon-controlled switch, or SCS, as indicated in Fig. 10.43.

This extra terminal allows more control to be exerted over the device, particularly in the mode of forced commutation, where an external signal forces it to turn on while the main current through the device has not yet fallen below the holding current value. Consider the circuit shown in Fig. 10.44, when the "on" pushbutton switch is actuated, there is a voltage applied between the cathode gate and the cathode, forward-biasing the lower transistor's base-emitter junction, and turning it on. The top transistor of the SCS is ready to conduct, having been supplied with a current path from its emitter terminal

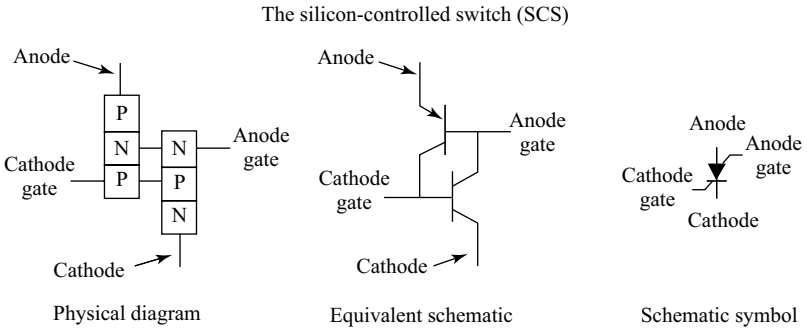


Fig. 10.43 Silicon-controlled switch

(the SCS's anode terminal) through resistor R_2 to the positive side of the power supply. As in the case of the SCR, both transistors turn on and maintain each other in the "on" mode. When the lower transistor turns on, it conducts the motor's load current, and the motor starts and runs. The motor may be stopped by interrupting the power supply, as with an SCR, and this is called **natural commutation**. However, the SCS provides us with another means of turning on: forced commutation by shorting the anode terminal to the cathode. If this is done (by actuating the "on" pushbutton switch), the upper transistor within the SCS will lose its emitter current, thus halting current through the base of the lower transistor. When the lower transistor turns on, it breaks the circuit for base current through the top transistor (securing its "o®" state), and the motor (making it stop). The SCS will remain in the o® condition until such time that the "on" pushbutton switch is re-actuated.

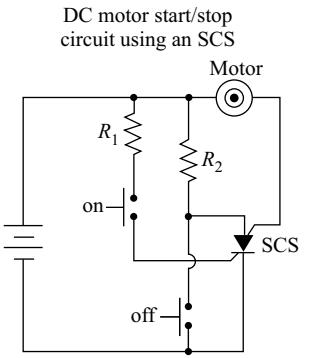


Fig. 10.44 SCS motor control

10.6.4 Programmable UJT (PUT)

A programmable UJT is a four-layered, three-terminal device (like SCR). It is also known as **complementary SCR (CSCR)** or **Silicon Unilateral Switch (SUS)**. Unlike an SCR, it has an anode gate

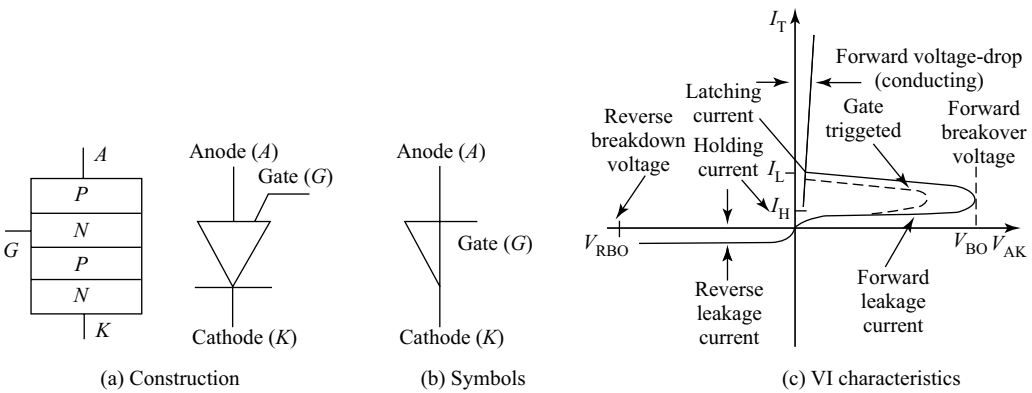


Fig. 10.45 Programmable UJT

connected to the inner *N*-region and it requires a negative hard gate drive to turn on. This is because the top *N*-layer is less doped and hence has more resistance, requiring a hard gate drive. However, it is a unilateral device and characteristics are similar to that of SCR. The construction, symbol and characteristics are indicated in Fig. 10.45.

The current through the device is almost negligible as long as $V_{AK} < V_{BO}$. Once breakover occurs, current increases rapidly.

It is used as a substitute for UJT in the construction of a relaxation oscillator. However, here using CSCR, η can be independently selected by the proper selection of external resistances R_1 and R_2. Hence, the name programmable UJT (PUT).

10.6.5 Opto-Couplers

An opto-coupler, or an opto-isolator, is a solid-state component in which the light emitter (source), light detector (detector) and the light path are enclosed. This serves the purpose of establishing a coupling between a light source and a light-activated device such as a photodiode, a phototransistor, a light-activated SCR (LASCR), etc.

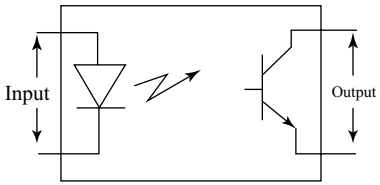


Fig. 10.46 Opto-coupler

There will be a complete isolation between the input and output. As indicated in Fig. 10.46, the light-emitting source IRED (IRED → Infrared emitting diode) is activated by the input. The IRED emits light due to the input which needs to be coupled to the output circuit. The detector at the output end is activated by the light. A light-activated device like a phototransistor or a LASCR (LASCR → Light Activated SCR) can be used as a detector. The extent of isolation between input and output depends on the type of light path, i.e. the dielectric and the distance between source and detector. The effectiveness of this isolation or the degree of isolation is given by the "current transfer ratio" given by,

$$CTR = \frac{\text{Output current}}{\text{Input current}} \tag{10.41}$$

$$CTR = \frac{I_o}{I_E} \tag{10.42}$$

Summary

- FET is a unipolar device as compared to a BJT which is a bi-polar device.
- FET is a voltage-controlled device as compared to a BJT which is a current-controlled device.
- Conventional JFETs are of two types: the *N*-channel FET and the *P*-channel FET.
- Conduction in FET is controlled by the channel-width modulation and is achieved by the gate-source voltage control.
- The three important performance parameters of a FET are the drain resistance, the transconductance and the amplification factor.
- A FET is characterised by its drain transconductance while a BJT is characterised by current gain (α, β and γ).
- A FET has high noise immunity, high input impedance, small size, etc. making it more suitable for many applications.

- A MOSFET is a JFET with gate terminal insulated from the channel and hence offers very high input impedance, larger than a conventional FET.
- A MOSFET can be depletion MOSFET or an enhancement MOSFET.
- UJT is a unipolar device that exhibits negative resistance property.
- UJT cannot be an amplifier, but can be used as an oscillator without any feedback.
- UJT is characterised by η, the intrinsic stand-off ratio.
- A silicon-controlled rectifier is a three-terminal, four-layered, three-junction device.
- The third terminal gate is used to trigger the device into conduction at lower anode-cathode voltages by the application of a small gate voltage.
- In forward blocking state of a SCR, the anode-cathode voltage is very high and this can be lowered by applying a small gate drive.
- SCRs when fired, the resulting anode current is called latching current I_L.
- SCRs are be turned off by reducing the anode-cathode voltage; in the process, the anode current falls below a value called the holding current I_H (less than I_L).
- SCR terminals may be identified by a continuity meter or an ohmmeter; the only two terminals showing any continuity between them at all should be the gate and cathode. Gate and cathode terminals connect to a *PN* junction inside the SCR, so a continuity meter should obtain a diode-like reading between these two terminals with the red (+) lead on the gate and the black (–) lead on the cathode.
- SCRs are true rectifiers; they only allow current through them in one direction. This means they cannot be used alone for full-wave ac power control.
- SCRs can replace the diodes in a rectifier forming a controlled rectifier circuit, wherein the dc power to a load may be time-proportioned by triggering the SCRs at different points along the ac power waveform.
- A silicon-controlled switch (SCS) is essentially an SCR with an extra gate terminal called the anode gate terminal.
- Typically, the load current through an SCS is carried by the anode gate and cathode terminals, with the cathode gate and anode terminals switching as control leads.
- An SCS is turned on by applying a positive voltage between the cathode gate and cathode terminals. It may be turned off (forced commutation) by applying a negative voltage between the anode and cathode terminals, or simply by shorting those two terminals together.
- The anode terminal must be kept positive with respect to the cathode in order for the SCS to latch or conduct.
- A DIAC is simply an ac diode or bidirectional diode that finds its applications in ac circuit triggering.
- A TRIAC is a three-terminal, bidirectional device that is suitable for ac power control.
- An opto-coupler, or an opto-isolator, isolates the input side and the output side; contains a light source such as an LED (transmitter) and a light receiver (a photodiode).

Review Questions

1. Compare constructional differences between a FET and a BJT in your own words.
2. FET being a unipolar device, what are the advantages?
3. Compare characteristic differences between a FET and a BJT in your own words.
4. What are the disadvantages of a FET over a BJT?

5. With gate-source terminals reverse biased, what is the advantage offered by a FET?
6. Draw the drain characteristics of a FET, mark various regions and obtain r_d from it.
7. Draw the mutual characteristics of a FET, and using Eq. (10.1) explain the curve.
8. A *P*-channel JFET has device parameters of I_{DSS} = 7.5 mA and V_P = 4 V, Sketch the transfer characteristics.
9. Sketch the basic construction of a *P*-channel depletion-type MOSFET.
10. Apply the proper drain-to-source voltage and sketch the flow of electrons.
11. In what ways is the construction of a depletion-type MOSFET similar to and different from that of a JFET?
12. Explain in your own words why the application of a positive voltage to the gate of an *N*-channel depletion-type MOSFET will result in a drain current exceeding I_{DSS}.
13. How many junctions are there in an SCR? What are their conditions when sufficient positive voltage is applied between the anode and cathode of an SCR?
14. Can we use an SCR for ac power controls? Justify your answer.
15. Define in your own words the breakover voltage, latching current and holding current for an SCR.
16. Compare a diode rectifier and a SCR rectifier in your own words.
17. Think and answer:
    (i) Can we apply two-transistor analogy during SCR conduction.
    (ii) Why only SCR, not GCR?
    (iii) Can gate terminal turn off SCR?
18. How is SCS is different from SCR? Explain.
19. Compare a diode and a DIAC in your own words.
20. Compare an SCR and a TRIAC in your own words.
21. Think and answer:
    (i) Is UJT a unipolar device or a bipolar device?
    (ii) What exactly do you mean negative resistance?
    (iii) Can we generate signals without feedback?
22. What is the physical significance of intrinsic stand-off ratio (η)?
23. Define the valley voltage VV and peak voltage V_P in your own words.
24. Compare a programmable UJT (PUT) with a conventional UJT.
25. Define cut-off region, negative resistance region and the saturation regions for an UJT in your own words.
26. List all the advantages and applications of a PUT.
27. Think and answer:
    (i) Is an opto-coupler analogous to a transformer?
    (ii) What exactly do you find inside an opto-isolator?
    (iii) Can we use photodiodes, phototransistors, LASCRs to construct an opto-coupler?
28. Draw the output waveforms for an SCR circuit with an ac signal applied between its anode and cathode terminals, given the sinusoidal input.
29. On the output waveform in Problem 27, mark clearly the conduction angle, the delay angle, V_{AK} and V_m.

Exercise Problems

1. A FET is characterised by I_{DSS} = 12 mA, VP = –6 V. Sketch the device transfer curve.
2. Repeat Problem 1 for a *P*-channel FET.
3. A FET is characterised by I_{DSS} = 6 mA, VP = 4 V. Sketch the device transfer curve
4. Repeat Problem 3 for an *N*-channel FET.
5. For an *N*-channel FET, I_D is 1.6 mA at V_{GS} = –3 V. I_D is 0.4 mA at V_{GS} = –4 V; draw its transfer characteristics by obtaining I_{DSS} and V_P.
6. For the fixed-bias circuit shown in Fig. P10.6, determine the operating point if I_{DSS} = 10 mA and V_P = –4 V.

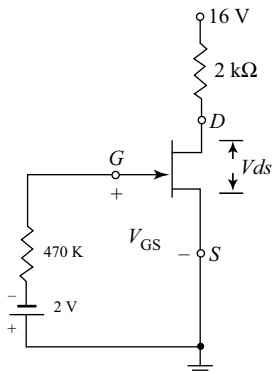


Fig. P10.6

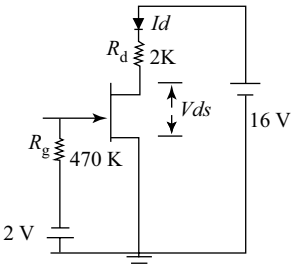


Fig. P10.7

7. Determine the following for the network of Fig. P10.7 given I_{DSS} = 8 mA and V_P = 4 V.
   (a) V_{DSQ} (b) I_{DQ} (c) V_{GSQ}
8. Determine the operating point (*Q*-Point) for the self-bias circuit shown in Fig. P10.8, given V_{DD} = 24 V, I_{DSS} = 10 mA and V_P = –8 V.

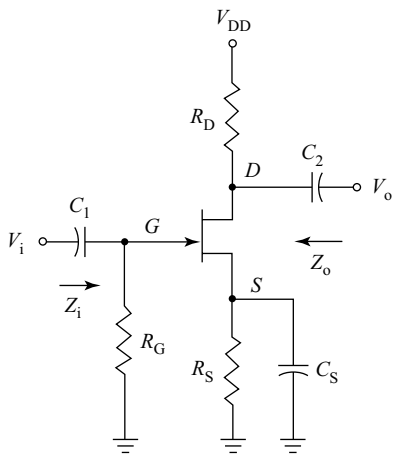


Fig. P10.8

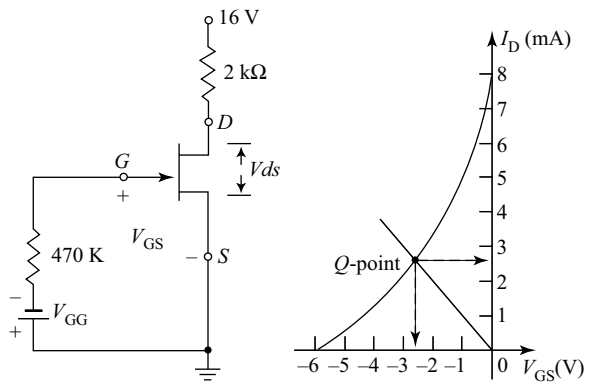


Fig. P10.9

9. Calculate the drain current and V_{GG} for the circuit shown in Fig. P10.9, given V_{DS} = 4 V.

10. Calculate the value of R_S in the circuit of Fig. P10.10 for a V_{GS} of –3 V.

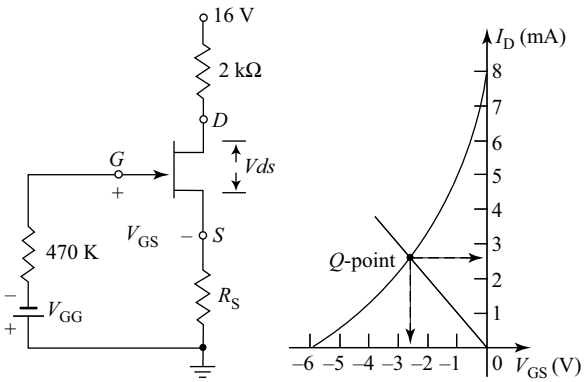


Fig. P10.10

11. In the circuit of Problem 10, find I_D and V_{DS} if I_{DSS} = 10 mA, V_P = –5 V, R_S = 1 kΩ.
12. For the JFET circuit shown in Fig. P10.12, calculate the output voltage if the device is supplying to a load of 10 kΩ.

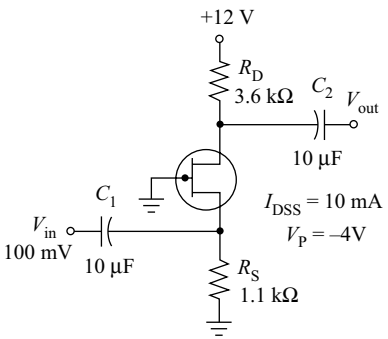


Fig. P10.12

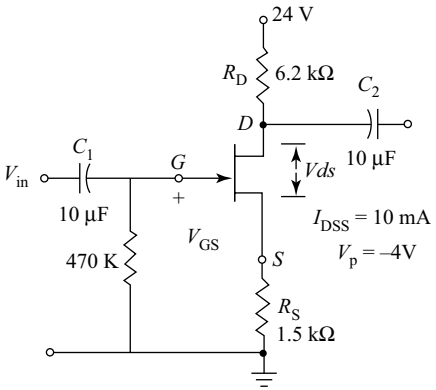


Fig. P10.13

13. For the JFET self-bias circuit shown in Fig. P10.13, calculate the operating point.
14. For the JFET self-bias circuit shown in Fig. P10.13, calculate the operating point using graphical method.
15. For the JFET voltage-divider bias circuit shown in Fig. P10.15, calculate the operating point.
16. For the JFET self-bias circuit shown in Fig. P10.15, calculate the operating point using graphical method.
17. For the circuit shown in Fig. P10.17 find I_{DQ}, V_{GSQ} at the operating point Q.
18. Draw the *VI* characteristics of an SCR and mark V_{FBO}, V_{AK}, I_L and I_H on the curve.
19. Input signal to an SCR circuit shown in Fig. P10.18 is v_i = 250 sin ωt; draw to scale the waveforms across the R_L and across the SCR with respect to input.
20. Draw the *VI* characteristics of UJT and mark V_P, VV, I_V and I_P on the curve.

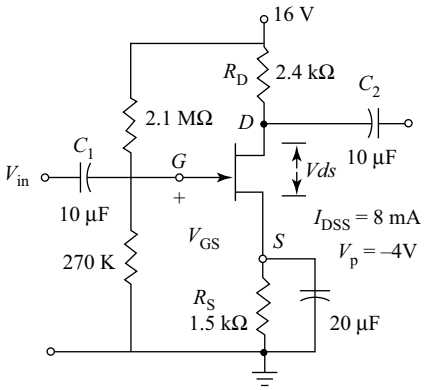


Fig. P10.15

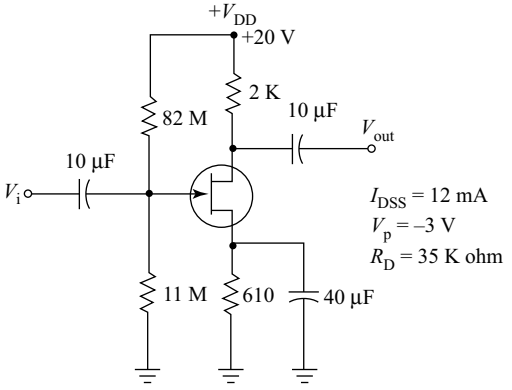


Fig. 10.17

21. The internal resistances of a UJT base terminal are R_{B1} = 12 Ω and R_{B2} = 6 Ω, calculate the intrinsic stand-off ratio for the device.
22. Calculate the frequency of the output triggering pulses generated by the UJT relaxation oscillator circuit shown in Fig. P10.21 if $\eta = 0.63$, V_{BB} = 12 V, R_T = 10 kΩ and C_T = 1 µF.

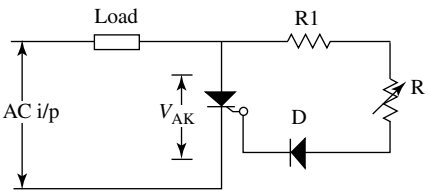


Fig. P10.18

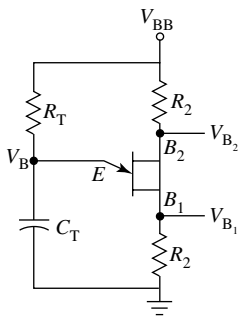


Fig. P10.21

23. It is desired to trigger an SCR using a UJT circuit at a frequency of 5 kHz. If the triggering device has a η value of 0.72, what value is needed with a capacitor of 4.7 µF?

Multiple-Choice Questions

1. The input terminal that controls the current flow across the FET is
   (a) the source (b) the drain (c) the gate (d) the base
2. A FET is a _____ device.
   (a) unipolar (b) bipolar
   (c) neither (a) nor (b) (d) both (a) and (b)

3. For an *N*-channel JFET having drain-source voltage constant, if the gate-source voltage is increased (more negative), the pinch-off would occur for
   (a) high values of drain current (b) zero drain current
   (c) saturation value of drain current (d) gate current = drain current
4. For a JFET in the pinch-off region as the drain voltage is increased, the drain current
   (a) becomes zero (b) abruptly increases
   (c) abruptly decreases (d) remains constant
5. The transfer characteristics of a JFET is a plot with
   (a) I_D v/s V_{DS} (b) I_D v/s V_{GS} (c) I_{DSS} v/s V_{GS} (d) none of the above
6. JFET has the characteristics of current source when
   (a) $V_{DS} = 0$ (b) $V_{DS} > V_T$ (c) $V_{DS} = V_T$ (d) $V_{DS} < V_T$
7. Pick the correct one:
   (a) Input resistance of a FET will be very low in the order of kΩ since the gate-to-source of FET will be forward biased.
   (b) Input resistance of a FET is very less compared to the input resistance of a BJT.
   (c) Input resistance of a FET is very high in the order of MΩ since the gate-to-source of FET is reverse biased.
   (d) FETs offer very high noise
8. FET provides _____ offset voltage.
   (a) infinite (b) less (c) very high (d) zero
9. Beyond pinch-off voltage, the drain-to-source resistance of JFET is
   (a) zero (b) low (c) high (d) infinite
10. JFET has a characteristics of a current source when
    (a) $V_{DS} = 0$ (b) $V_{DS} > V_P$ (c) $V_{DS} = V_P$ (d) $V_{DS} < V_P$
11. The three terminals of JFET are named
    (a) Source, Drain and Gate (b) Emitter, Base and Collector
    (c) Emitter, Drain and Gate (d) Source, Base and Drain
12. Which of the following symbol is the schematic symbol of an *N*-channel JFET?
    (a)  (b) (c)  (d)  (e) 
13. The current through the channel of JFET is controlled by the amount of
    (a) forward bias between gate and source (b) forward bias between gate and drain
    (c) reverse bias between gate and channel (d) gate current flowing through gate/source junction
14. The drain current of an *N*-channel JFET decrease when
    (a) the gate voltage changes in a negative direction
    (b) the gate voltage changes in a positive direction
    (c) the gate current increases
    (d) gate current decreases
15. Some JFETs are constructed in a symmetrical manner, making it possible to interchange their
    (a) gate and source leads (b) gate and drain leads
    (c) source and drain leads (d) two leads
16. JFETs are different from BJTs because they
    (a) can only amplify voltage (b) can only amplify current
    (c) are voltage-controlled devices (d) have low input impedance

17. The drain current with the gate voltage equal to zero is
    (a) I_G (b) I_D (c) I_{DSS} (d) none of the above
18. The gate-to-source voltage that stops drain current from flowing is _____
    (a) V_{GS} (b) $V_{GS\ (OFF)}$ (c) $V_{GS\ (STOP)}$ (d) V_P
19. _____ voltage is the drain-to-source voltage where the drain current becomes approximately constant.
    (a) Pinch-off (b) Cut-off
    (c) Saturation (d) Constant rate
20. Transconductance when gate to source voltage equals zero is
    (a) G_{mo} (b) B_{gm} (c) $G_{m(gate)}$ (d) G_m
21. What type of JFET biasing circuit is best at holding the drain constant with changes in JFET characteristics?
    (a) Voltage divider biasing (b) Voltage feedback biasing
    (c) Source biasing (d) Self-biasing
22. When the JFET is switched on, the resistor between the drain and source is less than _____
    (a) 1 Ω (b) R_{DS}(on) (c) R_d (d) R_{DS}(OFF)
23. In a shunt JFET switching circuit, the JFET is
    (a) in series with load and in parallel with R_s
    (b) in series with Rs and in parallel with the load
    (c) in series with the load and in series with R_s
    (d) in parallel with load and in parallel with R_s
24. In Fig. MCQ-10.24, the dc voltage on the gate terminal measures 0 V, what is wrong with the circuit?
    (a) Resistor R_g is shorted
    (b) Resistor R_g is open
    (c) The JFET is shorted between gate and source
    (d) Circuit is functioning properly

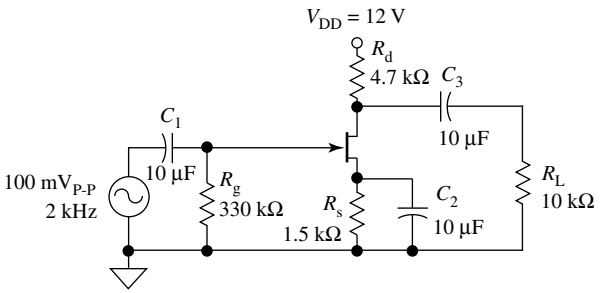


Fig. M10.24

25. In Fig. MCQ 10.24, the dc voltages are correct, but the signal voltage gain is low. What is wrong with the circuit?
    (a) Capacitor C_3 is shorted (b) Capacitor C_3 is open
    (c) Capacitor C_2 is open (d) Capacitor C_2 is shorted
26. In Fig. MCQ-10.24, the dc voltage of the drain terminal measures 12 V. What is wrong with the circuit?
    (a) Capacitor C_3 is shorted (b) Capacitor C_2 is open
    (c) The JFET is shorted (d) The JFET is open

27. The JFET depends on a reversed biased *PN* junction for isolation, but the MOSFET uses thin layers of _____ as an insulator between the gate and channel.
(a) SiO_2 (b) glass (c) rubber (d) enhanced glass
28. When the voltage on the gate of an *N*-channel D-MOSFET is negative and reduces current carriers, the MOSFET is said to be working in the _____ mode.
(a) depletion (b) enhancement
(c) conductive (d) local
29. Drain current can flow through a D-MOSFET operating in
(a) depletion mode only
(b) enhancement mode only
(c) either the depletion or the enhancement mode
(d) the local mode only
30. If an amplifier using a D-MOSFET is designed to have zero bias between the gate and the source, the drain current at quiescent will equal to _____
(a) 0 mA (b) 10 mA (c) I_{DSS} (d) R_d/g_m
31. Drain current can flow through an E-MOSFET operating in _____
(a) the depletion mode only
(b) the enhancement mode only
(c) either the depletion or the enhancement mode
(d) local mode only
32. The amount of V_{GS} needed to cause drain current to start to flow is called _____ voltage.
(a) cut-off (b) cut-on (c) saturation (d) threshold
33. With zero gate voltage applied, the E-MOSFET switching circuit acts as a/an _____ circuit.
(a) conductive path (b) short
(c) open (d) low resistance
34. When the E-MOSFET switching circuit is turned on, the resistance between the drain and source is less than _____
(a) 1 Ω (b) $R_{DS(on)}$ (c) R_g/g_m (d) R_d/g_m
35. For class-A operation, *N*-channel E-MOSFETs must have
(a) source voltage positive with respect to the gate voltage
(b) source voltage positive with respect to the drain voltage
(c) gate voltage positive with respect to the source voltage
(d) gate voltage positive with respect to the source voltage
36. The type of biasing often used with E-MOSFET amplifier circuits is the
(a) drain-feedback bias (b) source bias
(c) self-bias (d) constant-current bias
37. A _____ circuit converts a dc signal or a low-frequency signal into a high-frequency signal.
(a) multiplexing (b) clipper
(c) chopper (d) de-multiplexing
38. Circuit designing using both NMOS and PMOS is called
(a) hybrid MOS circuit (b) *PN* MOS design
(c) two-channel design (d) CMOS design
39. The current flow in a FET is due to _____ charge carriers.
(a) holes (b) electrons
(c) either (a) or (b) (d) neither (a) nor (b)

40. The channel width in a FET is controlled by the
    (a) applied current (b) applied voltage
    (c) applied temperature (d) none
41. The input terminal that controls the current flow across the MOSFET is
    (a) the source (b) the drain
    (c) the gate (d) the base
42. MOSFET is a
    (a) voltage-controlled device (b) current controlled device
    (c) minority carrier device (d) bipolar device
43. MOSFET can be used as a
    (a) current-controlled capacitor (b) voltage-controlled capacitor
    (c) current-controlled inductor (d) voltage-controlled inductor
44. In an *N*-channel enhancement operation of a MOSFET, drain current increases when
    (a) $V_{GS} > V_T$ (b) $V_{GS} = V_T$ (c) $V_{GS} < V_T$ (d) $V_{GS} = 0$
45. In an *N*-channel depletion-mode MOSFET, if the negative gate-to-source voltage increases from 2 volts to 5 volts,
    (a) channel conductivity decreases
    (b) channel conductivity increases
    (c) channel depth increases
    (d) mobile channel charge carrier density remains unchanged
46. In an SCR, the amount of power that is delivered to the load is controlled by.
    (a) anode terminal (b) cathode terminal
    (c) gate terminal (d) none of the above
47. In an SCR, the gate terminal forms a *PN* junction with
    (a) anode terminal (b) cathode terminal
    (c) gate terminal (d) none of the above
48. In an SCR, the _____ junction is reverse biased during its forward blocking state.
    (a) J_1 (b) J_2 (c) J_3 (d) all of the above
49. A conducting SCR can be turned of by
    (a) withdrawing gate drive (b) applying negative gate drive
    (c) reducing anode-cathode voltage (d) all of the above
50. In an SCR, the _____ junction is reverse biased during its forward blocking state.
    (a) J_1 (b) J_2 (c) J_3 (d) all of the above
51. For a UJT, if R_1 = resistance from emitter to the base-1, R_2 = resistance from emitter to the base 2 and $R_{BB} = (R_1 + R_2)$ then the intrinsic stand of ratio (η) is
    (a) R_1/R_2 (b) R_1/R_{BB} (c) R_2/R_1 (d) R_2/R_{BB}
52. A UJT can be used to construct an oscillator, because it exhibits
    (a) negative resistance property (b) negative feedback
    (c) positive feedback (d) all the above
53. A DIAC can be used as a bidirectional switch for ac power control. True/False.
54. A TRIAC cannot be used for ac power control. True/False.
55. In a PUT, the intrinsic stand-off ratio can be programmed. True/False.

Question Bank

Additional Solved Examples

Chapter 1: Semiconductor Physics and *PN* Junction

Example 1.1

In Example 1.3, the room temperature drops by 7°C. Calculate the resulting thermal voltage V_T.

Solution Room temperature drops by 7°C means $T = 20°C$ or 293 K

(i) Substituting into Eq. (1.3), we obtain

$$V_T = \frac{kT}{q} = \frac{1.38 \times 10^{-23} \times T}{1.6 \times 10^{-19}}$$

$$\therefore \quad V_T = \frac{1.38 \times 10^{-23} \times 293}{1.6 \times 10^{-19}}$$

$$\boxed{V_T = 25.275 \text{ mV}}$$

(ii) Substituting into Eq. (1.4), we obtain

$$V_T = \frac{T}{11600} = \frac{293}{11600}$$

$$\boxed{V_T = 25.275 \text{ mV}}$$

Example 1.2

In a certain *PN* junction diode circuit, the diode temperature changes from room temperature to 50°C. With all other conditions remaining unchanged, calculate the resulting percentage change in the thermal voltage V_T.

Solution Room temperature means $T = 27°C$ or 300 K

Substituting into Eq. (1.3), we obtain

$$V_{T_1} = \frac{kT_1}{q} = \frac{1.38 \times 10^{-23} \times T_1}{1.6 \times 10^{-9}}$$

$$\therefore \qquad V_{T_1} = \frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}}$$

$$\boxed{V_{T_1} = 25.275 \text{ mV}}$$

The temperature changes to $T = 50°C$ or 323 K
Substituting into Eq. (1.3), we obtain

$$V_{T_2} = \frac{kT_2}{q} = \frac{1.38 \times 10^{-23} \times T_2}{1.6 \times 10^{-19}}$$

$$\therefore \qquad V_{T_2} = \frac{1.38 \times 10^{-23} \times 323}{1.6 \times 10^{-19}}$$

$$\boxed{V_{T_2} = 27.209 \text{ mV}}$$

Now, the percentage change in V_T is

$$\frac{V_{T_2} - V_{T_1}}{V_{T_2}} \times 100\% = \frac{27.209 \times 10^{-23} - 25.275 \times 10^{-23}}{27.209 \times 10^{-23}} \times 100\% = 7.108\%$$

Example 1.3

In Example 1.14, find the resulting percentage change in the diode current if the voltage across the junction is 0.3 V.

Solution From Eq. (1.2), we obtain

$$I_D = I_O \left(e^{\frac{V}{\eta} VT} - 1 \right) \text{ A}$$

$$I_{D_1} = I_O \left(e^{0 \cdot \frac{3}{25} \cdot 862 \times 10^{-3}} - 1 \right) \text{A}.$$

$$I_{D2} = I_O \left(e^{0 \cdot \frac{3}{27} \cdot 209 \times 10^{-3}} - 1 \right) \text{A}$$

Now, taking the ratio of diode currents, the percentage change in the device current is

$$(I_{\downarrow} D_2 - I_{\downarrow} D_1)/I_{\downarrow} D_2 \times 100\% = ((e^{\uparrow} (0.3/27.209 \times 10 (-3)) - 1) - (e^{\uparrow} (0.3/25.862 \times 10.)$$

$$= \frac{61435.7 - 109100}{61435.7} \times 100\% = 71.08\%$$

Example 1.4

What is the percentage increase in the reverse saturation current of a diode if the temperature is increased from 25°C to 50°C?

Solution $\dfrac{I_{O_2}}{I_{O_1}} = 2^{(50-25)/10} \times 100\% = 565.7\%$

Example 1.5

In a certain *PN* junction diode circuit, the diode junction temperature is maintained at room temperature. For a forward current of 10 mA, the junction voltage is 0.3 V. Calculate the resulting diode current if the junction voltage is increased to 0.4 V.

Solution Taking the ratio of diode currents for two junction voltages, we write

$$\frac{I_{D_2}}{I_{D_1}} = \frac{I_O\left(e^{\frac{V_2}{\eta V_T}} - 1\right)\text{A}}{I_O\left(e^{\frac{V_1}{\eta V_T}} - 1\right)\text{A}} = \frac{\left(e^{0\cdot\frac{4}{25}\cdot 862\times 10^{-3}} - 1\right)}{\left(e^{0\cdot\frac{3}{25}\cdot 862\times 10^{-3}} - 1\right)} = 47.73$$

Now, $I_{D_1} = I_{D_1} \times 47.73 = 477.3$ mA

Example 1.6

In Example 1.17, find the resulting reverse saturation current.

Solution From Eq. 1.2, we can write

$$I_O = \frac{iD_1}{e^{V_{D1}/V_r} - 1} = \frac{10\times 10^{-3}}{e^{0.3/0.02587} - 1} = 91 \text{ nA}$$

Example 1.7

Determine the forward voltage and forward current for the *PN* junction diode in Fig. Ex. 7 for both practical and ideal diode models by taking $R_d = 10\ \Omega$.

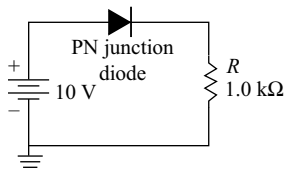


Fig. Ex. 7 For Example 1.7

Solution

Practical Diode Model:

Forward current through the diode

$$I_D = \frac{V - V_D}{R + R_d} = \frac{10 - 0.7}{1\times 10^3 + 10} = 9.208 \text{ mA}$$

Voltage drop across the *PN* junction

$$V_D = (V - V_R) = (10 - I_D \times R) = (10 - 9.208 \times 10^{-3} \times 1 \times 10^3) = 0.792 \text{ V}$$

Ideal Diode Model:

Forward current through the diode

$$I_D = \frac{V - V_D}{R + R_d} = \frac{10 - 0}{1\times 10^3 + 10} = 9.90 \text{ mA}$$

Voltage drop across the *PN* junction

$$V_D = (V - V_R) = (10 - I_D \times R) = (10 - 9.90 \times 10^{-3} \times 1 \times 10^3) = 0.1 \text{ V}$$

Example 1.8

Determine the reverse voltage and reverse current for the *PN* junction diode in Fig. Ex. 8 for both practical and ideal diode models by taking $R_d = 10\ \Omega$ and $I_R = 1\ \mu A$.

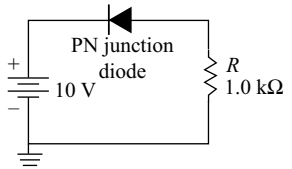


Fig. Ex. 8 For Example 1.8

Solution

Practical Diode Model:

Reverse current through the diode

$$I_R = 1 \times 10^{-6}\ A$$

Voltage drop across the *PN* junction

$$V_{DR} = (V - V_R) = (10 - I_R \times R) = (10 - 1 \times 10^{-6} \times 1 \times 10^3) = 9.999\ V$$

Ideal Diode Model:

Reverse current through the diode

$$I_R = 0\ A$$

Voltage drop across the *PN* junction

$$V_{DR} = (V - V_R) = (10 - I_R \times R) = 10\ V$$

Example 1.9

Determine the voltage across the series resistor in each case by taking $R_d = 10\ \Omega$ for the *PN* junction diode in Fig. 1.38.

Solution

Practical Diode Model:

Forward current through the diode $I_D = 9.208$ mA;

Hence, the voltage drop across the series resistor

$$V_R = I_D \times R = 9.208\ mA \times 1 \times 10^3 = 9.208\ V$$

Ideal Diode Model:

Forward current through the diode $I_D = 9.90$ mA;

Hence, the voltage drop across the series resistor

$$V_R = I_D \times R = 9.90\ mA \times 1 \times 10^3 = 9.90\ V$$

Example 1.10

Determine the voltage across the series resistor in each case by taking $R_r = 10\ M\Omega$ for the *PN* junction diode in Fig.1.39.

Solution

Practical Diode Model:

Reverse current through the *PN* junction diode $I_R = 1\ \mu A$;

Hence, the voltage drop across the series resistor

$$V_R = I_R \times R = 1 \times 10^{-6} \times 1 \times 10^3 = 1 \times 10^{-3}\ V$$

Ideal Diode Model:

Reverse current through the diode $I_R = 1\ \mu A$;

Hence, the voltage drop across the series resistor

$$V_R = I_R \times R = 1 \times 10^{-6} \times 1 \times 10^3 = 1 \times 10^{-3}\ V$$

Chapter 2: Diode Applications

Example 2.1

A half-wave rectifier supplying to a load of 480 Ω has an on-state resistance of 12 Ω and input voltage of 50 sin ωt. Calculate the load voltage and the conversion efficiency of the rectifier.

Solution Given data: R_L 480 Ω, R_f = 12 Ω, v = 50 sin ωt V_{dc} = ? and η = ?

Load voltage or Output voltage (V_{dc})

we have

$$V_{dc} = I_{dc} - R_L$$

where

$$I_{dc} = \frac{V_m}{\pi(R_L + R_f)} = \frac{50}{\pi(480 + 12)}$$

$$= 32.35 \text{ mA}$$

Now,

$$V_{dc} = (32.35 \times 10^{-3})(480\ \Omega)$$

$$V_{dc} = 15.53 \text{ V}$$

Conversion or rectification efficiency (η)

we have

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

where $P_{dc} = I_{dc}^2 \times R_L$ and $P_{ac} = I_{rms}^2 \times (R_L + R_f)$

Now $P_{dc} = (32.35 \times 10^{-3})^2\ (480) = 0.502$ W

$$P_{ac} = \left[\frac{V_m}{2(R_L + R_f)}\right]^2 (R_L + R_f) = \left[\frac{50}{2(480 + 12)}\right]^2 (480 + 12)$$

$$= 1.27 \text{ W}$$

Hence, conversion efficiency

$$\eta = \frac{0.502}{1.27} \times 100\%$$

$$\boxed{\eta = 39.55\%}$$

Example 2.2

A certain diode rectifier with *C*-filter, supplying to a load of 680 Ω produces a peak-to-peak ripple voltage of 500 mV. If the peak output voltage is 9 V, calculate the ripple factor for the rectifier.

Solution Given Data: R_L = 680 Ω, $V_{r\,(P-P)}$ = 500 mV, V_P = 9 V

we have

$$V_{r(rms)} = \frac{V_{r(P-P)}}{2\sqrt{3}} = \frac{500 \times 10^{-3}}{2\sqrt{3}} = 0.144 \text{ V}$$

$$V_{dc} = V_P - \frac{V_{r(P-P)}}{2} = 9 - \frac{500 \times 10^{-3}}{2} = 8.75 \text{ V}$$

Now, ripple factor for the rectifier

$$r = \frac{V_{r(rms)}}{V_{dc}} \times 100\%$$

$$= \frac{0.144}{8.75} \times 100\% = 1.65\%$$

$$\boxed{r = 1.65\%}$$

Example 2.3

A half-wave rectifier supplying to a load of 680 Ω uses a transformer with a turns ratio of 4:1. If the primary voltage input to the transformer is 230 V, find the peak-inverse-voltage (PIV) across the non-conducting diode.

Solution Given data: $N_1{:}N_2 = 4{:}1$, $V_1 = 230$ V, PIV = ?

We have $$\frac{N_1}{N_2} = \frac{V_1}{V_2}$$

i.e. $$V_2 = V_1 \left(\frac{N_2}{N_1}\right) = 230 \times \frac{1}{4} = 57.5 \text{ V}$$

The maximum secondary voltage is

$$V_{2(m)} = \sqrt{2} \times V_2 = \sqrt{2} \times 57.5 = 81.32 \text{ V}$$

Now, in an HWR, the PIV across the nonconducting diode is the maximum voltage itself.

i.e. $$\boxed{\text{PIV} = 81.32 \text{ V}}$$

Example 2.4

The circuit in Example 2.16 is converted to a centre-tapped FWR and the diodes used have a PIV rating of 100 V. Calculate the PIV across each non-conducting diode and comment on the safety of diodes.

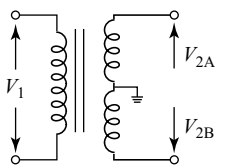


Fig. Ex. 4 For Example 2.4

Solution

(a) *For HWR*: $V_1 = 230$ V, $V_2 = 57.5$ V

$$V_m = \text{PIV} = \sqrt{2} \times V_2 = 81.32 \text{ V}$$

The PIV rating of the diode is 100 V and hence the diode is safe (even when reverse biased).

(b) *For FWR*: $V_1 = 230$ V $\quad V_{2A} = 57.5$ V and $V_{2B} = 57.5$ V.

Corresponding peak voltages are $V_{2A(m)} = V_{2B(m)} = \sqrt{2} \times V_{2A}$

$= 81.32$ V

When the diodes are nonconducting, the PIV in a FWR is

$$= 2 \times V_{2A(m)} = 2 \times V_{2B(m)}$$
$$= 2 \times 81.32 = 162.64 \text{ V}$$

The diodes have a PIV rating of 100 V each, but experience a reverse voltage of 162.64 V. Hence, diodes are not safe. In order that the FWR works without damaging the diodes, the diodes with a PIV rating greater than 162.64 V have to be used.

Example 2.5

A full-wave rectifier connected to a load of 10 V is expected to deliver a dc power of 120 mW. Give the specifications of transformer.

Solution Given data: $V_{dc} = 10$ V, $P_{dc} = 120$ watts

Now $$I_{dc} = \frac{P_{dc}}{V_{dc}} = \frac{120 \times 10^{-3}}{10} = 12 \text{ mA}$$

Also, secondary peak voltage

$$V_m = \frac{\pi \times V_{dc}}{2} \text{ ; from } V_{dc} = \frac{2V_m}{\pi}$$

$$V_m = \frac{\pi \times 10}{2} = 15.71 \text{ V}$$

The secondary rms voltage is

$$V_{2rms} = \frac{V_m}{\sqrt{2}} = \frac{15.71}{\sqrt{2}} = 11.1 \text{ V}$$

Now, the transformer turns ratio is

$$\boxed{\frac{N_1}{N_2} = \frac{V_1}{V_2} = \frac{230}{11.1}}$$

Example 2.6

A bridge rectifier uses a step-down transformer and ideal diodes. If the rectifier delivers an average output voltage of 41.4 V to a 480 Ω load find (i) transformer turns ratio, (ii) PIV requirement for diodes, and (iii) the average power delivered to the load.

Solution Given data = $V_{dc} = 41.4$ V, $R_L = 480\ \Omega$ $R_f = 0$, (i) N_1/N_2 = ? (ii) PIV = ? (iii) P_{dc} = ?

We have $$V_{dc} = \frac{2V_m}{\pi}$$

i.e. $$V_m = \frac{\pi \times V_{dc}}{2} = \frac{\pi \times 41.4}{2} = 65 \text{ V}$$

The transformer secondary rms voltage is

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{65}{\sqrt{2}} = 45.98 \text{ V}$$

(i) Transformer turns-ratio

$$\frac{N_1}{N_2} = \frac{V_1}{V_2} = \frac{230}{45.98} \simeq \frac{5}{1}$$

$$\boxed{N_1 : N_2 = 5:1}$$

(ii) PIV rating required for each diode is > 65 V.

(iii) Average power delivered to the load

$$P_{dc} = \frac{V_{dc}^2}{R_L} = \frac{(41.4)^2}{480} = 3.57 \text{ watts}$$

$$\boxed{P_{dc} = 3.57 \text{ watts}}$$

Example 2.7

A capacitor fitter connected across the rectifier in Example 2.19 is expected to produce a ripple factor not more than 0.001. Estimate the site of the filter for Indian territory usage.

Solution Given data: $R_L = 480$, $r \leq 0.001$ and $f = 50$ Hz (Indian territory), $C = ?$
For an FWR, the ripple factor from Eq. (2.60) is

$$C = \frac{1}{4\sqrt{3}R_L fr} = \frac{1}{4\sqrt{3}(480)(50)(0.001)}$$

$$\boxed{C = 6.01\ \mu\text{F}}$$

Example 2.8

A series-biased clipper shown in Fig. Ex. 8(a) uses a Si diode with a forward diode resistance of 50 Ω. The input applied to the circuit is $v_i = 50 \sin 300\,t$. Plot the output waveform for the circuit if V_{ref} is nine times the cut-in voltage of the diode.

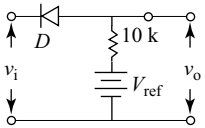


Fig. Ex. 8(a) For Example 2.8

Solution Given data: $v_i = 50 \sin 300\,t$, $R_f = 50\ \Omega$, $R = 10\ \text{k}\Omega$,

$$V_{ref} = 9 \times V_y = 5.4 \text{ V} \qquad (\because V_y = 0.6 \text{ V})$$

The input and output waveforms are shown in Fig. Ex. 8(b). For Example 8.

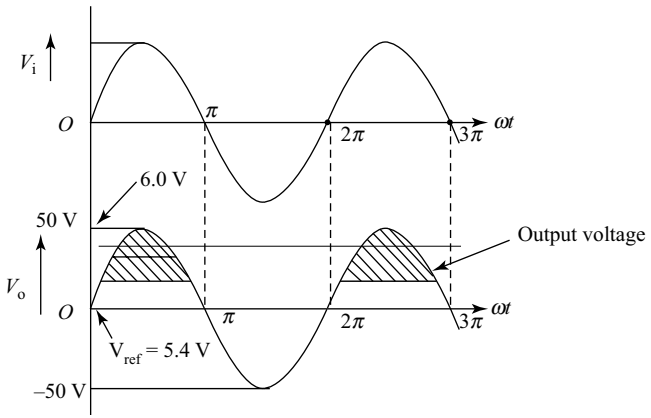


Fig. Ex. 8(b) For Example 2.8

Chapter 3: Bipolar Junction Transistors

Example 3.1

The *NPN* transistor shown in Fig. 3.1 (a) has a charge flow of 10^8 holes/μs from base to emitter and 10^{10} electrons/μs from emitter to base. If the current meter connected to the base reads 16 μA, what are the emitter and collector current values?

Solution The emitter current I_E is given by the net rate of positive charges into the emitter;

$$I_E = (1.602 \times 10^{-19}\ \text{C/hole})(10^{14}\ \text{holes/s}) - (-1.602 \times 10^{-19}\ \text{C/electron})(10^{16}\ \text{electrons/s})$$
$$= 1.602 \times 10^{-5} + 1.602 \times 10^{-3} = 1.618\ \text{mA}$$

Now, by applying Kirchhoff's Current Law (KCL), we get

$$I_C = I_E - I_B = 1.618 \times 10^{-3} - 16 \times 10^{-6} = 1.602\ \text{mA}$$

Example 3.2

Determine the values of α and β for the *NPN* transistor shown in Fig 3.1 (a) by neglecting the leakage current. Assume the transistor has constant charge flow described.

Solution The flow due to holes is negligible; i.e. with the assumption that $I_{CEO} = I_{CBO} = 0$, we get

$$\alpha = \frac{i_C}{i_E} = \frac{i_E - i_B}{i_E} = \frac{1.602 - 0.0616}{1.602} = 0.99$$
$$\beta = \frac{i_C}{i_B} = \frac{i_E - i_B}{i_B} = \frac{1.602 - 0.016}{0.016} = 99.125$$

Example 3.3

Determine the collector current for the transistor with a CB mode current gain $\alpha = 0.99$, $I_B = 25$ μA and collector-to-base leakage current of 200 nA. Assume the transistor has constant charge flow described.

Solution Given $\alpha = 0.99$, then, from Eq. (3.11),

$$\beta = \frac{\alpha}{1 - \alpha} = 99$$

Now, the collector current is

$$I_C = \beta I_B + (\beta + 1) I_{CBO} = 99(25 \times 10^{-6}) + (99 + 1)(200 \times 10^{-9}) = 2.495\ \text{mA}$$

Example 3.4

Determine the emitter current for the transistor in Example 3. If the transistor leakage current is neglected, find the resulting error in emitter current.

Solution The emitter current is

$$I_E = \frac{I_C - I_{CBO}}{\alpha} = \frac{2.495 \times 10^{-3} - 200 \times 10^{-9}}{0.99} = 2.518\ \text{mA}$$

Neglecting the leakage current, we have

$$I_C = \beta I_B = 99(25 \times 10^{-6}) = 2.475 \text{ mA}$$

so

$$I_E = \frac{I_C}{\alpha} = \frac{2.475}{0.99} = 2.5 \text{ mA}$$

Then, the resulting error in emitter current is

$$\frac{2.518 - 2.5}{2.518} (100\%) = 0.71\%$$

Example 3.5

A certain bipolar junction transistor has $I_B = 100$ μA and $I_C = 2$ mA, Find (i) β, (ii) α, and (iii) emitter current I_E.

Solution Given $I_B = 100$ μA, $I_C = 2$ mA

(i) $\beta = \frac{I_C}{I_B} = \frac{2 \times 10^{-3}}{100 \times 10^{-6}} = 20$

(ii) $\boxed{\alpha = \frac{\beta}{\beta + 1}} = 20/20+1 = 0.952$

(iii) $I_E = I_C + I_B = 2$ m + 100 μA = 2.1 mA

Example 3.6

In Example 5, if I_B changes by +25% and I_C changes by +30%, find the new value of β.

Solution Given I_B increases by 25 μA and I_C increases by 0.6 mA;

i.e.

$$I_B' = I_B + 25 \text{ μA} = 100 \text{ μA} + 25 \text{ μA} = 125 \text{ μA}$$
$$I_C' = I_C + 0.6 \text{ mA} = 2 \text{ mA} + 0.6 \text{ mA} = 2.6 \text{ mA}$$

The new β value is $\beta = \frac{I_C}{I_B} = \frac{2.6 \times 10^{-3}}{125 \times 10^{-6}} = 20.8$

Example 3.7

If for a certain bipolar junction transistor, $\alpha = 0.99$ and the base current is 100 μA, estimate collector current.

Solution Given $I_B = 100$ μA and $\alpha = 0.99$

We have $\boxed{\beta = \frac{\alpha}{1 - \alpha} \quad \beta = \frac{0.99}{1 - 0.99} = 99}$

Also, $\beta = \frac{I_C}{I_B}$, i.e. $I_C = \beta \times I_B = 99 \times 100\mu = 9.9$ mA

Example 3.8

If for a certain bipolar junction transistor, collector current is 1 mA and base current is 10 μA, determine its α and β.

Solution Given $I_C = 1$ mA and $I_B = 10$ μA

$$\beta = \frac{I_C}{I_B} = \frac{1 \times 10^{-3}}{10 \times 10^{-6}} = 100$$

$$\boxed{\alpha = \frac{\beta}{\beta + 1} = 100/100 + 1 = 0.99}$$

OR $I_E = I_C + I_B = 1$ mA + 10 μA = 1.01 mA

Therefore, $\alpha = \frac{I_E}{I_C} = \frac{1.01 \times 10^{-3}}{1 \times 10^{-3}} = 0.99$

Example 3.9

If for a certain bipolar junction transistor, $I_E = 1$ mA and $I_B = 10$ μA, determine α and β

Solution Given $I_E = 1$ mA and $I_B = 10$ μA

$I_C = I_E - I_B = 1$ mA – 10 μA = 0.99 mA

$$\boxed{\alpha = \frac{I_c}{I_e} = \frac{0.99\text{ m}}{1\text{ m}} = 0.99}$$

$$\boxed{\beta = \frac{I_c}{I_b} = \frac{0.99\text{ m}}{10\,\mu} = 99}$$

Example 3.10

A transistor amplifier connected in CE mode has $\alpha = 0.9$ and $I_E = 10$ mA, compute the values of base current I_B, collector current I_C, β and γ.

Solution Given $\alpha = 0.9$ and $I_E = 10$ mA

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}} = \boxed{\beta = \frac{0.99}{1 - 0.99} = 9}$$

$$\boxed{\gamma = \beta + 1 = 1 + 9 = 10}$$

$$\boxed{\alpha = \frac{I_C}{I_e}}$$

$I_C = \alpha I_E = 0.9 \times 10$ mA = 9 mA

$I_B = I_E - I_C = 10$ mA – 9 mA = 1 mA

Example 3.11

A transistor amplifier connected in CE mode has $\beta = 100$ and $I_B = 50\ \mu A$, compute the values of emitter current I_E, collector current I_C, α and γ.

Solution Given $\beta = 100$ and $I_B = 50\ \mu A$

$$\alpha = \frac{\beta}{1+\beta} = \frac{100}{101} = 0.991$$

$$\gamma = 1 + \beta = 1 + 100 = 101$$

$$I_C = \beta I_B = 100 \times 50\ \mu A = 5\ mA$$

$$I_E = I_B + I_C = 50\ \mu A + 5\ mA = 5.05\ mA$$

Example 3.12

A Ge transistor used in a circuit in CE mode has collector to base leakage current of 5000 nA. If the current gain for the transistor is 100, find its collector current with $I_B = 0$.

Solution Given $\beta = 100$ and $I_{CBO} = 5000\ nA = 5\ \mu A$.

With $I_B = 0$, the collector current is only the collector-to-emitter leakage current; i.e.

$$I_{CEO} = (\beta + 1)I_{CBO} = (100 + 1)(5 \times 10^{-6}) = 505\ \mu A$$

Example 3.13

In Example 12, if the base current is increased to 40 μA, what is the resulting collector current?

Solution Given $\beta = 100$, $I_{CBO} = 5000\ nA = 5\ \mu A$ and $I_B = 40\ \mu A$.

$$I_C = \beta I_B + (\beta + 1)I_{CBO}$$

$$= (100)(40 \times 10^{-6}) + (101)(5 \times 10^{-6}) = 4.505\ mA$$

Example 3.14

An Si transistor used in a circuit in CE mode has collector to base leakage current of 3000 nA. If the current gain for the transistor is 50 and the collector current is 1.2 mA, find its base and emitter currents.

Solution

Given $\beta = 50$, $I_{CEO} = 3\ \mu A$, and $I_C = 1.2\ mA$

$$I_B = \frac{I_C - I_{CEO}}{\beta}$$

$$= \frac{1.2 \times 10^{-3} - 3 \times 10^{-6}}{50} = 23.94\ \mu A$$

And, $I_E = I_C + I_B$

$$= 1.2 \times 10^{-3} - 23.94 \times 10^{-6} = 1.224\ mA$$

Example 3.15

An Si transistor used in a certain application has common base gain of 0.98 and I_{CBO} of 0.005 mA. If the biasing circuit results in a I_{BQ} = 100 μA, find the values of I_{CQ} and I_{EQ}.

Solution

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

Now, $I_{CEO} = (\beta + 1)I_{CBO}$

$= (49 + 1)(5 \times 10^{-6}) = 0.25$ mA

And, $I_{CQ} = \beta I_{BQ} + I_{CEO}$

$= (49)(100 \times 10^{-6}) + 0.25 \times 10^{-3} = 5.15$ mA

Also, $I_{EQ} = I_{CQ} + I_{BQ}$

$= 5.15 \times 10^{-3} + 100 \times 10^{-6} = 5.25$ mA

Example 3.16

A Si transistor used in Fig. 3.30 has I_B = 30 μA and a CB mode gain of 0.98. Neglecting the leakage currents, find β and the operating point.

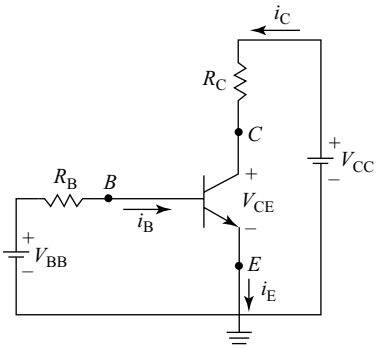


Fig. Ex. 16 For Example 3.16

Solution

Now, $\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$

with $I_{CEO} = 0$, we have $I_{CQ} = \beta I_{BQ}$

$= (49)(30 \times 10^{-6}) = 1.47$ mA

with $I_{CBO} = 0$,

$$I_{EQ} = \frac{I_{CQ}}{\alpha} = \frac{1.47}{0.98} = 1.50 \text{ mA}$$

The operating point $Q(I_{BQ}, I_{CQ}, I_{EQ})$ = **(30 μA, 1.47 mA, 1.5 mA)**

Example 3.17

In the circuit in Fig. 3.31, the silicon transistor used has β_{dc} = 100. If V_{CC} = 10 V and V_{BB} = 5 V, find the values of I_C and V_{CE}.

Solution When $V_{CE} = V_{CC;}$ $I_C = 0$

This results in **Point *A* (10 V, 0 A)**

When $V_{CE} = 0$; $I_C = V_{CC}/R_C = 10/\ 1K = 10$ mA

This results in **Point *B* (0, 10 mA)**

Applying KVL on to the input side,

$$V_{BB} - R_B \times I_B - V_{BE} = 0$$

$$5V - 100K \times I_B - V_{BE} = 0$$

$$I_B = 5 - 0.7/100K = 43 \text{ μA}$$

$$I_C = \beta \times I_B = 100 \times 43 \text{ μA} = 4.3 \text{ mA}$$

Applying KVL to output side

$$V_{CC} - R_C \times I_C - V_{CE} = 0$$
$$10 - 1K \times 4.3 \text{ mA} - V_{CE} = 0$$
$$V_{CE} = 10 - 1K \times 4.3 \text{ mA} = 5.7 \text{ V}$$

This results in **Point *Q* (5.7 V, 4.3 mA)**

Therefore, *Q*-point is $I_{BQ} = 43\ \mu A$, $I_{CQ} = 4.3$ mA and $V_{CEQ} = 5.7$ V

Example 3.18

For the circuit in Example 3.29, draw the dc load line on output characteristics and indicate the *Q*-point.

Solution Marking the three points—Point *A* (10 V, 0 A), Point *B* (0, 10 mA) and Point *Q* (5.7 V, 4.3 mA)—on the output characteristic, we get Fig. Ex. 18.

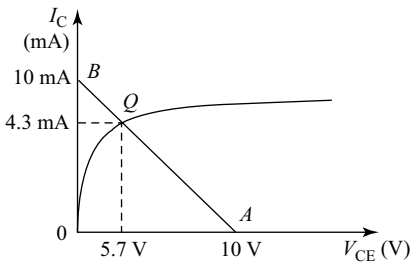


Fig. Ex. 18 For Example 3.18

Example 3.19

In the circuit shown in Fig. Ex. 19, a silicon transistor with $\beta = 50$ is used. Determine the operating point for the circuit.

Solution Given $R_B = 100$ kΩ, $\beta = 50$, $V_{CC} = 5$ V and $R_C = 1$ kΩ

Let $V_{BE} = 0.7$ V

Applying KVL to Base (input) Circuit

$$V_{CC} - I_B R_B - V_{BE} = 0$$
$$I_B = (V_{CC} - V_{BE})/R_B = (5 - 0.7)/100K = 43\ \mu A$$
$$I_C = \beta,\ I_B = 50 \times 43\ \mu A = 2.15 \text{ mA}$$

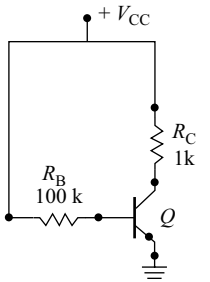


Fig. Ex. 19 For Example 3.19

Applying KVL to collector (output) circuit,

$$V_{CC} - I_C R_C - V_{CE} = 0$$
$$V_{CE} = V_{CC} - I_C R_C = 5 - (2.15 \text{ mA} \times 1K) = 2.85 \text{ V}$$

And operating point is ***Q*** (2.85 V, 2.15 mA)

Example 3.20

For the circuit of Example 3.31, draw the load line.

Solution To draw the load line, obtain Point *A*, Point *B* and Point *Q*:

When $V_{CE} = V_{CC}$; $I_C = 0$ and **Point *A* (5 V, 0 A)**

When $V_{CE} = 0$; $I_C = V_{CC}/R_C = 5/1K = 5$ mA and **Point B (0 V, 5 mA)**

And operating point is Point *Q* (2.85 V, 2.15 mA) Marking the three points Point *A* (5 V, 0 A), Point *B* (0, 5 mA) and Point *Q* (2.85 V, 2.15 mA), we get the load line shown in Fig. Ex. 20.

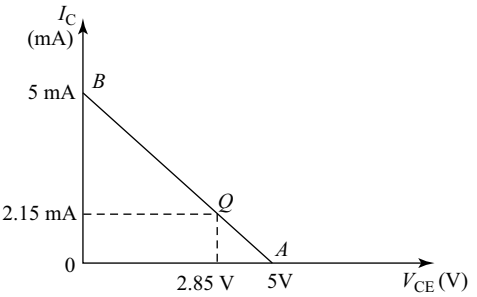


Fig. Ex. 20 For Example 3.20

Example 3.21

In the circuit shown in Fig. Ex. 21, a silicon transistor with $\beta = 50$ is used. Find I_C and V_{CE}. Draw the dc load line on output characteristics and indicate the *Q*-point.

Solution Given $R_B = 240$ kΩ , $\beta = 50$, $V_{CC} = 12$ V, $R_C = 2.2$ kΩ and $V_{BE} = 0.7$ V

Applying KVL to base (input) circuit

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = (V_{CC} - V_{BE})/R_B = (12 - 0.7)/240K = 47\mu A$$

$$I_C = \beta I_B = 50 \times 47\ \mu A = 2.35\ mA$$

Applying KVL to collector (output) circuit

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C = 12 - (2.35\ mA \times 2.2K) = 6.83\ V$$

And operating point is ***Q*** (6.83 V, 2.35 mA)

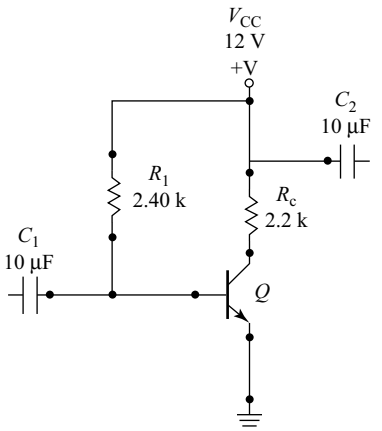


Fig. Ex. 21 For Example 3.21

Example 3.22

For the circuit in Example 3.33, obtain the *Q*-point and draw the dc load line on output characteristics.

Solution To draw the load line, obtain Point *A*, Point *B* and Point *Q*:

When $V_{CE} = V_{CC}$; $I_C = 0$ and **Point *A* (12 V, 0 A)**

When $V_{CE} = 0$; $I_C = V_{CC}/R_C = 12/2.2K = 5.45$ mA and **Point *B* (0 V, 5.45 mA)**

And operating point is Point *Q* (6.83 V, 5.45 mA) Marking the three points Point *A* (12 V, 0 A), Point *B* (0, 5.45 mA) and Point *Q* (6.83 V, 5.45 mA), we get the load line shown in Fig. Ex. 22.

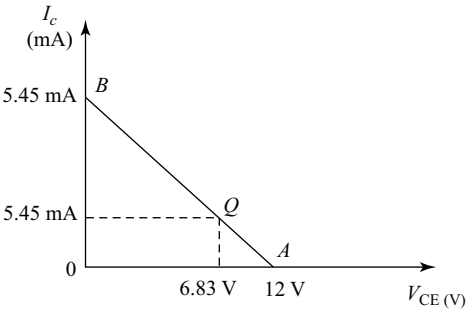


Fig. Ex. 22 For Example 3.22

Example 3.23

For the circuit shown in Fig. Ex. 23, obtain the operating point and draw the dc load line.

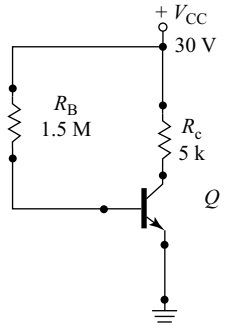


Fig. Ex. 23 For Example 3.23

Solution Given R_B =1.5 MΩ , let $\beta = 50$, $V_{CC} = 30$ V and $R_C = 5$ kΩ
Let $V_{BE} = 0.7$ V

Applying KVL to base (input) circuit

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = (V_{CC} - V_{BE})/R_B = (30 - 0.7)/1.5 \times 10^6 = 19.5\ \mu A$$

$$I_C = \beta I_B = 50 \times 19.5\ \mu A = 0.975\ mA$$

Applying KVL to collector (output) circuit

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C = 30 - (0.975m \times 5K) = 4.875\ V$$

Example 3.24

For the circuit in Example 23, draw the dc load line.

Solution Given to draw the load line:

When $V_{CE} = V_{CC}$; $I_C = 0$ and **Point *A* (30 V, 0 mA)**

When $V_{CE} = 0$; $I_C = V_{CC}/R_C = 30/5K = 6$ mA and **Point *B* (0 V, 6 mA)**

And operating point is Point ***Q*** (4.875 V, 0.975 mA)
Marking the three points—Point *A* (30 V, 0 A), Point *B* (0, 6 mA) and Point *Q* (4.875 V, 0.975 mA)—we get the load line shown in Fig. Ex. 24.

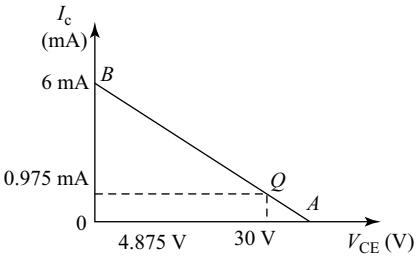


Fig. Ex. 24 For Example 3.24

Chapter 4: BJT amplifiers, Feedback and Oscillators

Example 4.1

For the single-stage CE amplifier in Fig. 4.6, if $R_1 = 82\ \text{k}\Omega$, $R_2 = 18\ \text{k}\Omega$, $R_E = 1.2\ \text{k}\Omega$, $R_C = 4.7\ \text{k}\Omega$, $\beta = 100$ and the supply voltage $V_{CC} = 12$ V, obtain the dc conditions.

Solution Given $V_{CC} = 12$ V, $\beta = 100$, $R_1 = 82\ \text{k}\Omega$, $R_2 = 18\ \text{k}\Omega$

$R_E = 1.2\ \text{k}\Omega$ and $R_C = 4.7\ \text{k}\Omega$

Generally, for an amplifier,

$$V_{CE} = \frac{V_{CC}}{2} = \frac{12\ \text{V}}{2} = 6\ \text{V}$$

$$V_E \simeq \frac{V_{CC}}{10} = \frac{12\ \text{V}}{10} = 1.2\ \text{V}$$

$$V_C = \frac{V_{CC}}{2.5} = \frac{12\ \text{V}}{2.5} = 4.8\ \text{V}$$

Now,
$$I_C = \frac{V_C}{R_C} = \frac{4.8}{4.7\ \text{k}\Omega} = 1.02\ \text{mA}$$

We have
$$\beta = \frac{I_C}{I_B}, \text{ i.e. } I_B = \frac{I_C}{\beta} = \frac{1.02 \times 10^{-3}}{100} = 10.21\ \mu\text{A}$$

There, the dc conditions for the circuit is $Q(I_{CQ}, I_{RQ}, V_{CEQ})$ = (1.02 mA, 10.21 MA, 6 V)

Example 4.2

For Example 1, draw the load line and mark the Q point.

Solution The extreme points on the load line are

$$A(I_{C\,max}, 0) \simeq \left(\frac{V_{CC}}{R_C}, 0\right)$$

$$= (2.55\ \text{mA}, 0) \text{ and}$$

$$B(0, V_{CE\,max} \simeq (0, V_{CC}) \simeq (0, 12\ \text{V})$$

The dc load line is drawn and the Q-point may be marked as in Fig. Ex 2

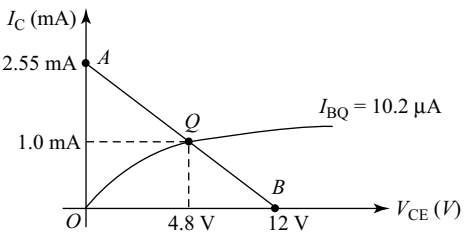


Fig Ex 2 For Example 4.2

Example 4.3

An amplifier produces an output of 40 W. If the amplifier gain is 33.9 dB, find the input power to the amplifier.

Solution For an amplifier, the power gain

From Ex 4.4, $A_P = 10 \log \frac{P_o}{P_{in}}$

i.e. $$\left(\frac{P_o}{P_{in}}\right) = \text{anti log}\left(\frac{A_P}{10}\right)$$

i.e. $$P_{in} = \frac{P_o}{\text{antilog}\left(\frac{A_P}{10}\right)} = \frac{40}{e^{\left(\frac{33.9}{10}\right)}}$$

$$\boxed{P_{in} = 0.016 \text{ W}}$$

Example 4.4

Calculate the gain for the multistage amplifier shown in Fig. Ex. 4.

Solution From Eq. (4.4), we have Amplifier gain

$$A_P = 10 \log\left(\frac{P_o}{P_{in}}\right) \text{ dB}$$

$$= 10 \log\left(\frac{0.316 \text{ W}}{0.001 \text{ W}}\right) = 25 \text{ dB}$$

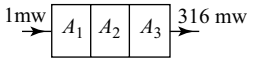


Fig. Ex. 4 For Example 4.4

Example 4.5

A multistage amplifier has a power gain of 50 dB, obtain its Neper gain.

Solution From Eq. (4.4)

$$A_P = 10 \log\left[\frac{P_o}{P_{in}}\right] \text{ dB}$$

i.e. $$\frac{P_o}{P_{in}} = \text{Anti log}\left[\frac{A_P}{10}\right] \text{ Neper}$$

$$= P\left[\frac{50}{10}\right] \text{ Neper}$$

$$\boxed{\frac{P_o}{P_{in}} = 148.41 \text{ N}}$$

Example 4.6

In example 1, find the voltage gain if the circuit has input impedance of 2.2 kΩ

Solution From Eq. 4.44(a), the voltage gain

$$A_V = \beta\frac{R_C}{R_i} = 100 \times \frac{4.7 \times 10^3}{2.2 \times 10^3}$$

$$\boxed{A_V = 213.64}$$

Example 4.7

The mid-band gain of on R_C coupled amplifier is 100 dB. The amplifier has 97 dB gain at 120 Hz and 120 kHz. Find the bandwidth of the amplifier.

Solution $A_{mid} = 100$ dB,

3 dB frequencies are $f_1 = 120$ Hz and $f_2 = 120$ kHz

$\therefore$ $\quad BW = (f_2 - f_1)Hz = (120\ kHz - 120)$

$$\boxed{BW \cong 120\ kHz}$$

Example 4.8

Find the figure of merit for the amplifier in Example 7.

Solution $A_{mid} = 100$ dB and BW = 120 kHz

$\therefore$ $\quad GBW = (A_{mid} \times 3\ dB\ BW)$

$$= (100 \times 120\ kHz)$$

$$\boxed{GW = 12000\ kHz}$$

Example 4.9

Find the effective input impedance in Example 4.13 if the input impedance without feedback is 15 kΩ

Solution $Z_{in} = 15\ k\Omega$, β 0.02

Form Eq. (4.54), $\quad Z_{if} = Z_{in}\ (1 + \beta A)$

$$= 15\ k\ (1 + 5000\ (0.02))$$

$$\boxed{Z_{if} = 1.52 \times 10^6\ \Omega}$$

Example 4.10

Find the effective output impedance in Example 4.16 if the $Z_o = 2\ k\Omega$ without any feedback.

Solution $Z_o = 2\ k\Omega$, $\beta = 0.01$.

From Eq. (4.60),

$$Z_{of} = \frac{Z_o}{1 + AB} = \frac{2 \times 10^3}{1 + 10,000 \times 0.01}$$

$$\boxed{Z_{if} = 19.8\ \Omega}$$

Chapter 5: Communication Systems

Example 5.1

A carrier of 10 MHz and 150 V is amplitude modulated to a depth of 60%. Calculate the amplitude of the modulating signal.

Solution Depth of modulation $m = 0.6$ or 60%.

Using the 'm' expression from Eq. (5.6), $m = \dfrac{V_m}{V_c} = \dfrac{V_m}{150}$

We have, information amplitude $V_m = 0.6 \times 150 = 90$ V

Example 5.2

A carrier of 10 MHz and 150 V is amplitude modulated to a depth of 30%. Calculate the side band frequencies and the bandwidth of AM output if the modulating signals frequency is 10 kHz.

Solution The USB frequency is $f_{USB} = f_c + f_m = (10 \times 10^6 + 10 \times 10^3)$
$= 10.01 \times 10^6$ Hz

and the LSB frequency is $f_{LSB} = f_c - f_m = (10 \times 10^6 - 10 \times 10^3)$
$= 09.99 \times 10^6$ Hz

Now, Bandwidth $= 2 \times f_m = 2 \times 10 \times 10^3 = 20 \times 10^3$ Hz

Example 5.3

A certain AM generator produces an output signal represented by $v = 200(1 + 0.2 \sin 6500t) \sin 6.28 \times [10]^{\uparrow} 6t]$. Find all the information available about the modulated and modulating signals.

Solution Comparing the AM expression with Eq. [5.4 (a)],
$v = V_{\downarrow}c\ (1 + m \sin \omega_{\downarrow} m\ t) \sin \omega_{\downarrow} c\ t]$, we have the carrier amplitude $V_C = 200$, carrier frequency $\omega_c = 6.28 \times 10^6$, modulating signal frequency $\omega_m = 6500$ and the modulation index $m = 0.2$.

Example 5.4

In Example 3, find the information signal frequency and the modulated signal frequency.

Solution Comparing the AM expression with Eq. [5.4 (a)],
$v = V_{\downarrow}c\ (1 + m \sin \omega_{\downarrow} m\ t) \sin \omega_{\downarrow} c\ t]$, we have $\omega_m = 6500$ rad/s and $\omega_c = 6.28 \times 10^6$ rad/s

Now, $f_m = \dfrac{\omega_m}{2 \times \pi} = 1035$ Hz and $f_c = \dfrac{\omega_c}{2 \times \pi} = 999.5$ kHz

Example 5.5

In Example 3, find the side-band frequencies and the depth of modulation.

Solution Comparing the AM expression with Eq. [5.4 (a)],
$v = V_{\downarrow}c\ (1 + m \sin \omega_{\downarrow} m\ t) \sin \omega_{\downarrow} c\ t]$, we have $m = 0.2, f_m = 1035$ Hz and $f_c = 999.5 \times 10^3$ Hz.

Now, the USB frequency is $f_{USB} = f_c + f_m = (999.5 \times 10^3 + 1035)$
$= 1000.54 \times 10^3$ Hz

and the LSB frequency is $f_{LSB} = f_c - f_m = (999.5 \times 10^3 - 1035)$

$= 999 \times 10^3$ Hz

Depth of modulation $m = 0.2$ or 20%.

Example 5.6

In Example 3, find the bandwidth and the amplitude of the information signal.

Solution Comparing the AM expression with Eq. [5.4 (a)],

$v = V_{\downarrow}c\ (1 + m \sin \omega_{\downarrow}m\ t) \sin \omega_{\downarrow}c\ t]$, we have $m = 0.2$, $f_m = 1035$ Hz and $f_c = 999.5 \times 10^3$ Hz.

Now, bandwidth $= 2 \times f_m = 2 \times 1035 = 2070$ Hz.

Depth of modulation $m = 0.2$ or 20%

Using the 'm' expression from Eq. (5.6), $m = \dfrac{V_m}{V_c} = \dfrac{V_m}{200}$

We have, information amplitude $V_m = 0.2 \times 200 = 40$ V

Example 5.7

If the carrier signal power of an amplitude modulated signal is 50 W then, calculate the maximum total transmitted power.

Solution We have from Eq. (5.15),

$$P_t = P_c \left(1 + \frac{m^2}{2}\right) \text{W}$$

P_t will maximum at $m = 1$ and the corresponding value is

$$P_t = 50\left(1 + \frac{1}{2}\right) = 75 \text{ W}$$

Example 5.8

A carrier signal of 10 V amplitude is modulated by an information signal to a depth of 80%. Calculate the V_{max} and V_{min} for the modulated wave.

Solution We have from Eq. (5.6),

$$m = \frac{V_m}{V_c}, \text{ i.e. } 0.8 = \frac{V_m}{10} \text{ i.e. } V_m = 8 \text{ V}$$

From Eq. (5.7), $V_m = \dfrac{V_{max} - V_{min}}{2}$;

This implies

$$V_{max} - V_{min} = 2V_m = 16 \text{ V}$$

From Eq. (5.9), $V_c = \dfrac{V_{max} + V_{min}}{2}$;

This implies

$$V_{max} + V_{min} = 2V_c = 20 \text{ V}$$

Solving these equations, $V_{max} = 18$ V

and $V_{min} = 2$ V

Example 5.9

If the modulated output of Example 7 is transmitted using an antenna having a radiation resistance of 10 kΩ, calculate the side-band powers.

Solution We have from Eq. (5.14),

$$P_{SB} = 0.25\ P_c\ \text{W}$$
$$= 0.25\ (50)\ \text{W} = 12.5\ \text{W}$$

Example 5.10

If a 400 W carrier signal is amplitude modulated to a depth of 45%; calculate the total transmitted power of the modulated wave.

Solution We have from Eq. (5.15),

$$P_t = P_c\left(1 + \frac{m^2}{2}\right) = 400\left(1 + \frac{0.45^2}{2}\right) = 440.5\ \text{W}$$

Example 5.11

A carrier signal is frequency modulated by a message signal and the resulting FM output is $v = 250 \sin (100 \times 10^6\ t + 10 \sin 2050t)$. Obtain all the features of the message, carrier and the output.

Solution We have from Eq. [5.27(b)], $v = A \sin (\omega_c t + \beta \sin \omega_m t)$;

Comparing this with the FM output, $V_c = 250$ V

Message frequency $\omega_m = 2050$ rad/s and carrier frequency $\omega_c = 100 \times 10^6$ rad/s

Now, $f_m = \dfrac{\omega_m}{2 \times \pi} = 327$ Hz and $f_c = \dfrac{\omega_c}{2 \times \pi} = 15.92$ MHz

Chapter 6: Linear Integrated Circuits

Example 6.1

An open-loop gain of a differential op-amp is 20,000. The two inputs read 5 μV and 10 μV, calculate its output.

Solution From Eq. (6.7), the gain of the amplifier

$$A_d = \frac{V_o}{V_{id}} = \frac{V_o}{10 \times 10^{-6} \sim 5 \times 10^{-6}}$$

$$V_o = 20000 \times 5 \times 10^{-6} = \pm 0.1 \text{ V}$$

Example 6.2

A 10 μV input signal is connected to an inverting input of an op-amp and its other input is grounded. If the open-loop gain is 200,000, find the output voltage of the amplifier.

Solution From Eq. (6.7), the gain of the amplifier

$$A_d = \frac{V_o}{V_{id}} = \frac{V_o}{10 \times 10^{-6} \sim 0}$$

$$V_o = 200000 \times 10 \times 10^{-6} = -2 \text{ V}$$

Example 6.3

An op-amp summer circuit uses equal resistances $R_F = R_1 = R_2 = R$; if the two input sources are $V_1 = 5$ V and $V_2 = 10$ V then find the summer output.

Solution From Eq. [6.38(a)] and referring to Fig 6.19(a), the output voltage of the amplifier

$$V_o = -R_F \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} \right] = -15 \text{ V}$$

Example 6.4

An inverting summer is configured to determine the average of the two input signals. If R_F is chosen as 1 kΩ then, find the values of R_1 and R_2, required at the inputs.

Solution From Eq. [6.38(a)] and referring to Fig 6.19(a), the output voltage of the amplifier

$$V_o = -R_F \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} \right]$$

The circuit is averaging the two input signals and this results in $R_1 = R_2 = 2$ kΩ.

Example 6.5

If the summer circuit in Example 3 is of non-inverting type then find the summer output.

Solution From Eq. [6.40(b)], Eq. (6.41) and referring to Fig. 6.20, the output voltage of the amplifier

$$V_{i2} = \left[\frac{V_1}{2} + \frac{V_2}{2}\right] = 7.5$$

$$V_o = V_{i2}\left[1 + \frac{R_F}{R_1}\right] = +11.25 \text{ V}$$

Example 6.6

For an inverting amplifier, $R_i = 100$ kΩ and $R_f = 600$ kΩ. What is the output voltage for an input of –3 V?

Solution From Eq. (6.24) and referring to Fig. 6.14(a), the output voltage of the amplifier

$$V_o = -\frac{R_f}{R_1}V_i$$

$$= \left[\frac{600 \times 10^3}{100 \times 10^3}\right] \times -3$$

$$V_o = 18 \text{ V}$$

Example 6.7

The input to a differentiator is a sinusoidal voltage of peak value 5 mV and frequency 2 kHz. Find the output if $R = 100$ kΩ and $C = 1$ μF.

Given

$$V_i = 5 \sin 400\,\pi t \text{ mV}$$

For differentiator $V_o = -RC\dfrac{dV_i}{dt}$

On solving $V_o = -2000\pi \cos 4000\,\pi t$ mV

Chapter 7: Digital Electronics

Example 7.1

Use truth table to prove the following Boolean equation:

$$A' \cdot B' + A \cdot B' + A \cdot B = A + B'$$

Solution Referring to the given equation, the following table may be prepared.

A	B	$A'B' + AB' + AB$	$A + B'$
0	0	1	1
0	1	0	0
1	0	1	1
1	1	1	1

Looking at the last two columns, the Boolean function is proved.

Example 7.2

Use truth table to prove the following Boolean equation:

$$A \cdot B \cdot C + A' \cdot B \cdot C + A' \cdot B \cdot C' = B \cdot C + A' \cdot B$$

Solution Referring to the given equation, the following table may be prepared

A	B	C	$ABC + A'BC + A'BC'$	$BC + A'B$
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

Looking at the last two columns, the Boolean function is proved.

Example 7.3

Prove the Absorption theorem in Boolean postulates:

Solution The Absorption theorem in Boolean postulates states

$$A + A \cdot B = A$$

$$\begin{aligned} A + A \cdot B &= A \cdot 1 + A \cdot B \\ &= A \cdot (1 + \mathrm{B}) \\ &= A \cdot (1) \\ &= A \end{aligned}$$

Example 7.4

Simplify the following Boolean switching function:

$$F = AC' + AB'C + ABCD + ABD'$$

Solution

$$\begin{aligned} F &= AC' + AB'C + ABCD + ABD' \\ &= AC' + AB'C + AB(CD + D') \\ &= AC' + AB'C + ABC + ABD' \\ &= AC' + AC(B' + B) + ABD' = AC' + AC + ABD' \\ &= A(C' + C) + ABD' = A + ABD' = A(1 + BD') = A \end{aligned}$$

Example 7.5

Simplify the following Boolean switching function:

$$F = ABC + A'D + B'D + CD$$

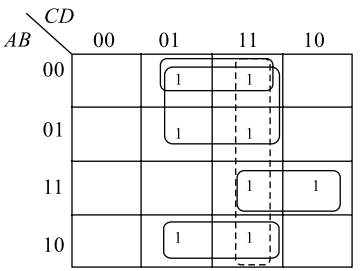
Solution

$$\begin{aligned} F &= ABC + A'D + B'D + CD \\ &= ABC + (A' + B')D + CD \\ &= ABC + (AB)'D + CD \\ &= ABC + (AB)'D \\ &= ABC + (A' + B')D \\ F &= ABC + A'D + B'D \end{aligned}$$

Example 7.6

Simplify the following Boolean switching function in Example 5 using *K*-map and verify.

Solution The 4-variable *K*-map may be drawn and the switching function may be entered as shown;



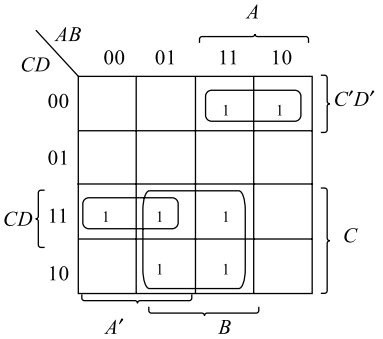
The quad formed around *CD* becomes redundant and the resulting output expression $F = ABC + A'D + B'D$ matches with that in Example 5.

Example 7.7

Simplify the following Boolean switching function using *K*-map:

$$f(A, B, C, D) = A(C + D)'(B' + D') + C(B + C' + A'D)$$

Solution The 4-variable *K*-map may be drawn and the switching function may be entered as shown;



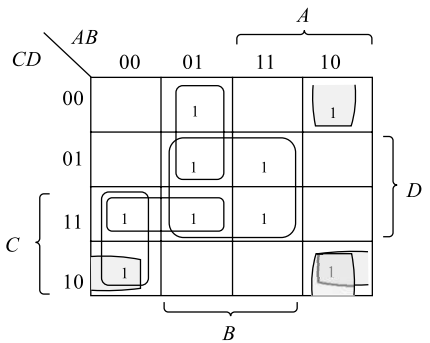
The resulting output expression is $f(A, B, C, D) = AC'D' + A'CD + BC$

Example 7.8

Simplify the following Boolean switching function using K-map.

$$f(A, B, C, D) = \Sigma m(2, 3, 4, 5, 7, 8, 10, 13, 15)$$

Solution The 4-variable K-map may be drawn and the switching function may be entered as shown;



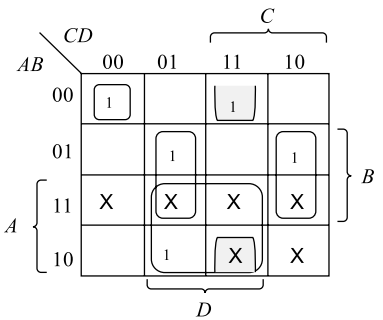
The resulting output expression is $f(A, B, C, D) = A'BC + A'CD + A'B'C + AB'D' + B'CD' + BD$

Example 7.9

Simplify the following Boolean switching function using *K*-map.

$$f(A, B, C, D) = \Sigma m(0, 3, 5, 6, 9) + \Sigma d(10,11, 12, 13, 14, 15)$$

Solution The 4-variable *K*-map may be drawn and the switching function may be entered as shown;



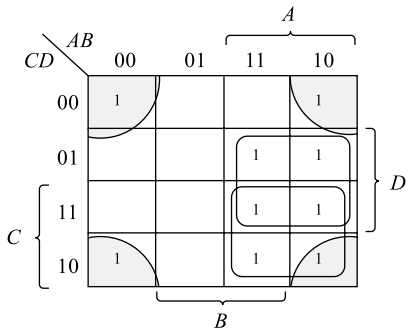
The resulting output expression is $f(A, B, C, D) = A'B'C'D' + B'CD + BC'D + BCD' + AD$

Example 7.10

Simplify the following Boolean switching function using *K*-map:

$$f(A, B, C, D) = A \cdot B \cdot C + B' \cdot C \cdot D' + A \cdot D + B' \cdot C' \cdot D'$$

Solution The 4-variable K-map may be drawn and the switching function may be entered as shown;



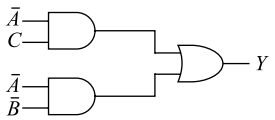
The resulting output expression is $f(A, B, C, D) = B'D' + AD + AC$

Example 7.11

Write out the truth table and draw the circuit corresponding to the Boolean function $Y = \overline{A}C + \overline{A}\overline{B}$.

Solution Truth table Logic Diagram

A	*B*	*C*	*Y*
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



Example 7.12

Write out the Boolean expression for $Y = \overline{A}C + \overline{A}\overline{B}$ in fundamental sum of products (SOP) form.

Solution The product terms (which contain all of the input variables) are called fundamental product terms or 'canonical' SOP terms.

Using the truth table written out for this function in Example 1, we can write

$$Y = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}BC.$$

Example 7.13

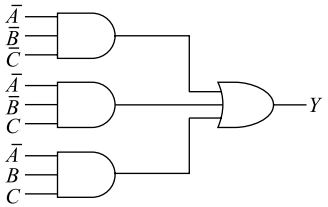
Express the Boolean expression $Y = \overline{A}C + \overline{A}\overline{B}$ in fundamental sum of products (SOP) form.

Solution The alternate canonical SOP form of the given expression $Y = \overline{A}C + \overline{A}\overline{B}$ is $Y = \Sigma(0, 1, 3)$

Example 7.14

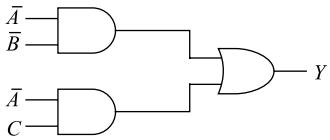
Draw the logic circuit to implement the fundamental sum of products expression below and then minimise it to obtain the simplified Boolean expression $Y = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}BC$.

Solution



(a) Circuit for unsimplified expression

$$\begin{aligned}\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}BC &= \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}\overline{B}C + \overline{A}BC \\ &= \overline{A}\overline{B}\cdot(\overline{C} + C) + \overline{A}C\cdot(\overline{B} + B) \\ &= \overline{A}\overline{B} + \overline{A}C\end{aligned}$$



(b) Circuit for simplified expression

Example 7.15

Minimise the logic expression below and draw the logic circuit for the simplified expression $Y = \overline{A}B\overline{C} + \overline{A}BC + ABC$.

Solution

$$\begin{aligned}Y &= \overline{A}B\overline{C} + \overline{A}BC + ABC \\ &= \overline{A}B\overline{C} + \overline{A}BC + \overline{A}BC + ABC \\ &= \overline{A}B(\overline{C} + C) + (\overline{A} + A)BC \\ &= \overline{A}B + BC\end{aligned}$$

Example 7.16

Minimise the logic expression below and draw the logic circuit for the simplified expression $Y = AB\overline{C} + ABC + A\overline{B}\overline{C} + A\overline{B}C$.

Solution

$$\begin{aligned}Y &= AB(\overline{C} + C) + A\overline{B}(\overline{C} + C) \\ &= AB + A\overline{B} \\ &= A(B + \overline{B}) \\ &= A\end{aligned}$$

Example 7.17

Simplify using Boolean laws:

$$F = \overline{AC} + ABC + A\overline{C}$$

Solution $F = (A' + C') + ABC + AC$; Using De Morgan's law *(Similarly, readers are required to list out all applicable laws in each step)*

$$= (A' + AC) + (C' + ABC) = (A' + C) + (C' + AB) = (C + C') + (A' + AB) = (1) + (A' + B) = 1$$

Example 7.18

Simplify using Boolean laws:

$$F = A\overline{B} + ABD + AB\overline{D} + \overline{ACD} + \overline{A}B\overline{C}$$

Solution $F = AB' + AB(D + D') + (A' + B' + C') + A'BC'$; Using De-Morgan's law*(Similarly, the reader is required to list out all applicable laws in each step)*

$$= AB' + AB(1) + (A' + B' + C') + A'BC'$$
$$= A(B' + B) + (A' (1+ BC')) + B' + C' = A (1) + (A' (1)) + B' + C'$$
$$= (A + A') + B' + C' = 1$$

Example 7.19

Simplify using Boolean laws:

$$F = BD + BC\overline{D} + A\,\overline{BCD}$$

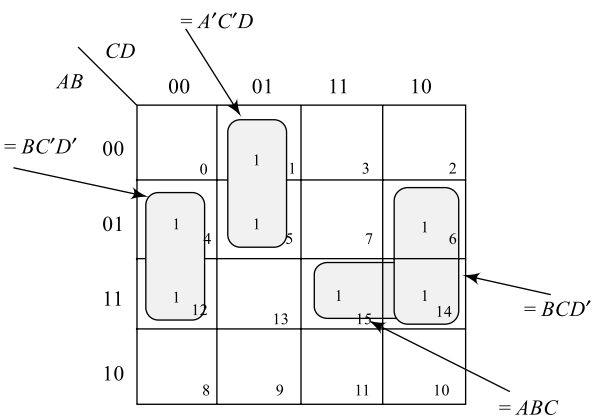
Solution $F = B (D + CD') + A(B' + C' + D') = B(D + C) + A(B' + C' + D')' = BD + BC + AB' + AC' + AD'$

Example 7.20

Simplify using *K*-map:

$$F(A, B, C, D) = \sum(1, 4, 5, 6, 12, 14, 15, 16)$$

Solution $F(A, B, C, D) = BC'D' + A'C'D + BCD' + ABC$

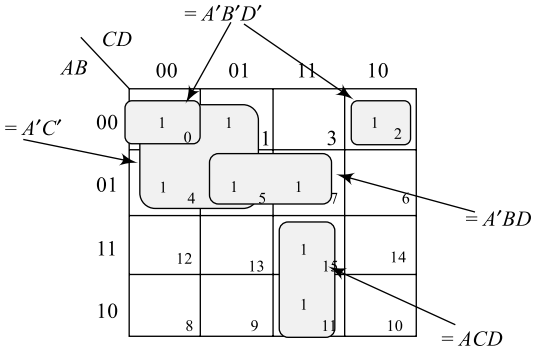


Example 7.21

Simplify using *K*-map:

$$F(A, B, C, D) = \sum(0, 1, 2, 4, 5, 7, 11, 15)$$

Solution $F(A, B, C, D) = A'B'D' + A'C' + A'BD + ACD$

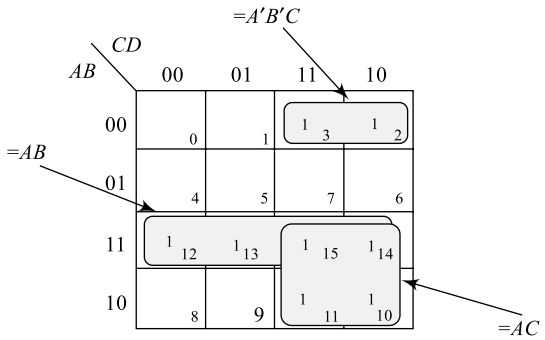


Example 7.22

Simplify using *K*-map:

$$F(A, B, C, D) = \sum(2, 3, 10, 11, 12, 13, 14, 15)$$

Solution $F(A, B, C, D) = A'B'C' + AC + AB$

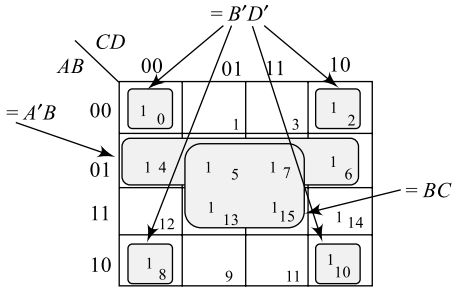


Example 7.23

Simplify using *K*-map:

$$F(A, B, C, D) = \sum(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$$

Solution $F(A, B, C, D) = B'D' + A'C'D + BCD' + ABC$



Example 7.24

Design equations for a 4-bit *BCD* to Excess-3 code converter are given in below:

$$Z = D,\ Y = C \oplus D,\ X = B \oplus (C + D),\ W = A + B(C + D)$$

Write the function table and draw the logic diagram.

Solution The function table for a 4-bit *BCD* to Excess-3 code converter is shown in Table Ex. 24.

Table Ex. 24 *BCD* to Excess-3 code converter and vice-versa

B C D				*Excess 3*			
A	***B***	***C***	***D***	***W***	***X***	***Y***	***Z***
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

The resulting circuit diagram is shown in Fig. Ex.24.

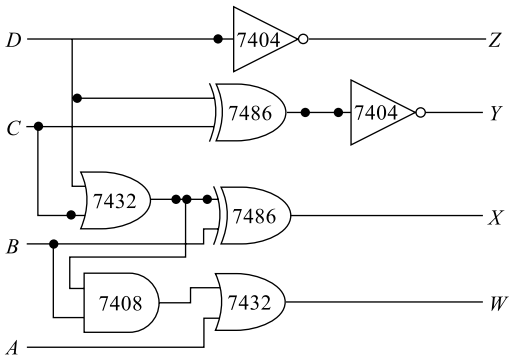


Fig. Ex.24 Logic diagram of *BCD* to Excess-3 code converter

Example 7.25

Design equations for a 4-bit Excess-3 to *BCD* code converter are given below:

$$D = Z,\ C = Y \oplus Z,\ B = X \oplus YZ,\ A = W(X + YZ)$$

Write the function table and draw the logic diagram.

Solution The function table for a 4-bit Excess-3 to *BCD* code converter is shown in Table Ex.24. The resulting circuit diagram is shown in Fig. Ex.25.

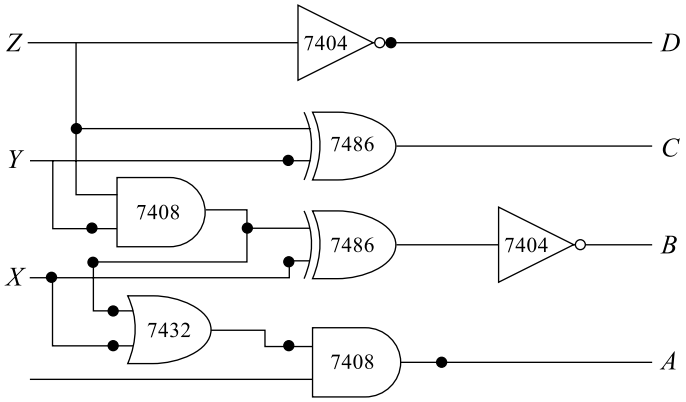


Fig. Ex.25 Logic diagram of EXCESS-3 to *BCD* code converter

Example 7.26

Convert $15_{(16)}$ into its equivalent decimal number.

Solution $15_{(16)} = 1 \times 16^1 + 5 \times 16^0$

$= 16 + 5 = 21_{(10)}$

Example 7.27

If $B8_{(16)} = X_{(10)}$, find the value of X.

Solution $B8_{(16)} = B \times 16^1 + 8 \times 16^0$

$= 11 \times 16 + 8 = 184_{(10)}$

i.e. $X = 184$

Example 7.28

What is the hexadecimal equivalent of 24(10)?

Solution

$$16 \overline{)\,24} \qquad 24_{(10)} = 18_{(16)}$$

1-8

Example 7.29

If $513_{(10)} = X_{(16)}$ then find the value of X.

Solution

$$16 \mid 513 \qquad 513_{(10)} = 201_{(16)}$$

$$16 \mid 32 \quad -1$$

$$2 \quad -0$$

i.e. $X = 201$

Chapter 9: Transducers

Example 9.1

A parallel-plate capacitive transducer has plate dimensions of 25 mm × 35 mm separated by a distance of 0.35 cm. A pressure applied to it produces a diaphragm movement of 0.06 cm; find the capacitance of the transducer if the un-pressured capacitance of the transducer is 370 pF.

Solution From Eq. (9.1), we may write

$$C_1 = \frac{\varepsilon_0 \varepsilon_r}{d_1} \text{ Farads} \qquad \text{and} \qquad C_2 = \frac{\varepsilon_0 \varepsilon_r A}{d_2} \text{ Farads}$$

Now, $$\frac{C_1}{C_2} = \frac{\dfrac{\varepsilon_0 \varepsilon_r A}{d_1}}{\dfrac{\varepsilon_0 \varepsilon_r A}{d_2}} = \frac{d_2}{d_1}$$

i.e. $$C_2 = C_1 \times \frac{d_1}{d_2} = 370 \times 10^{-12} \times \frac{0.35 \text{ cm}}{(0.35 - 0.06)\text{ cm}} = 446.5 \times 10^{-12}$$

Example 9.2

In Example 1, if the value of C_1 is 200 pF without any dielectric in between the plates. Find the value of the dielectric constant needed to produce the same displacement.

Solution From Eq. (9.1), we may write

$$C_1 = \frac{\varepsilon_0 \varepsilon_r}{d_1} \text{ Farads} \qquad \text{and} \qquad C_2 = \frac{\varepsilon_0 \varepsilon_r A}{d_2} \text{ Farads}$$

Now, $$\frac{C_1}{C_2} = \frac{\dfrac{\varepsilon_0 \varepsilon_r A}{d_1}}{\dfrac{\varepsilon_0 \varepsilon_r A}{d_2}} = \frac{d_2}{d_1}$$

i.e. $$C_2 = C_1 \times \frac{d_1}{d_2} = 200 \times 10^{-12} \times \frac{0.35 \text{ cm}}{(0.35 - 0.06)\text{ cm}} = 241.38 \times 10^{-12}$$

Now, $$C_2 = \frac{\varepsilon_0 \varepsilon_r A}{d_2} \text{ Farads}$$

$$\varepsilon_r = \frac{C_2 \times d_2}{\varepsilon_n A} = \frac{241.38 \times 10^{-12} \times (0.35 - 0.06) \times 10^{-2}}{8.85 \times 10^{-12} \times (25 \times 35) \times 10^{-6}}$$

$$\varepsilon_r = \frac{79.0963 \times 10^{-3}}{8.75 \times 10^{-4}} = 90.396$$

Example 9.3

Find the sensitivity of a LVDT that produces an output voltage of 5 mV across its output terminals, if the core movement is 0.5 mm.

Solution From Eq. (9.6b), we may write

$$S = \frac{5 \times 10^{-3}}{0.5 \times 10^{-3}} = 10 \frac{\text{mV}}{\text{mm}}$$

Example 9.4

Find the pressure value required to produce an output voltage of 89 V in a piezoelectric transducer given the voltage sensitivity of the crystal is 0.05 V-m/N and the thickness of 1.5 mm.

Solution From Eq. (9.9), we may write

$$P = \frac{V_o}{g \times t} = \frac{89}{0.05 \times 1.5 \times 10^{-3}}$$

$$P = \frac{1.87 \times 10^6 \text{ N}}{\text{m}^2}$$

Example 9.5

Find the Poisson's ratio for a strain gauge using an iron wire with a gauge factor of +4.198. Neglect all the piezo-resistive effects.

Solution From Eq. (9.12), the gauge factor may be written as

$$G_F = 1 + 2x$$

Now, the Poisson's ratio is

$$x = \frac{G_F - 1}{2} = \frac{4.198 - 1}{2}$$

$$x = 1.599$$

Example 9.6

A resistance wire strain gauge with a gauge factor of +2.00 is strained by applying a stress, resulting in a 0.5 mm deformation. If the length of the wire is 100 cm, find the percentage change in the gauge resistance.

Solution From Eq. (9.11), the strain of the gauge is given by

$$\in = \frac{\Delta L}{L} = \frac{0.5 \times 10^{-3}}{100^{-2}} = 500 \times 10^{-6}$$

From Eq. (9.11) for the gauge factor, the percentage change in resistance is given by

$$\frac{\Delta R}{R} = G_F \times \in = 2 \times 500 \times 10^{-6} = 0.001 = 0.1\%$$

The percentage change in resistance is only 0.1.

Example 9.7

The resistance of a thermistor used in an application at 25°C is 10 kΩ. Find the resistance of the thermistor if its temperature is doubled given the temperature co-efficient is –0.05/°C.

Solution From Eq. (9.13), the new resistance value is

$$R_2 = R_1(1 + \alpha (t_2 - t_1))$$
$$= R_1(1 + \alpha \Delta t) = 10 \times 10^3 \, (1 + (-0.05(50\text{-}25)))$$
$$R_2 = 2.5 \times 10^3 \Omega$$

Example 9.8

Calculate the output voltage developed across a Hall-effect transducer used for the measurement of a magnetic field of strength 0.55 Wb/m^2. The current flowing through the germanium Hall conductor of 2 mm thickness is 3000 mA and the Hall co-efficient is $-8 \times 10^{-3} \; \dfrac{V_\alpha - m}{A - \dfrac{\text{Wb}}{\text{m}^2}}$.

Solution From Eq. (9.14), the output voltage developed is

$$V_b = \frac{0.55 \times 3 \times 18 \times 10^{-3}}{2 \times 10^{-3}} = -6.6 \text{ V}$$

Example 9.9

Calculate the sensitivity of the LVDT if an output voltage 2 mV is produced when the core of LVDT moves through a distance of 0.5 mm.

Solution From Eq. [9.5(a)], the sensitivity of the LVDT is

$$S = \frac{\text{Output voltage}}{\text{Core displacement}} = \frac{2 \times 10^{-3}}{0} \cdot 5 = \frac{4 \text{ mV}}{\text{mm}}$$

Example 9.10

Calculate the LVDT core displacement if the output voltage developed across the terminals of LVDT is 1.5 V. The sensitivity of the LVDT is 2 mV/mm.

Solution From Eq. 9.5(a), the sensitivity of the LVDT is

$$S = \frac{\text{Output voltage}}{\text{Core displacement}} = \frac{2 \times 10^{-3}}{0} \cdot 5 = \frac{2 \text{ mV}}{\text{mm}}$$

$$\frac{2 \text{ mV}}{\text{mm}} = \frac{\text{Output voltage}}{\text{Core displacement}} = \frac{1.5 \times 10^{-3}}{d}$$

$$d = \frac{1.5 \times 10^{-3}}{\dfrac{2 \text{ mV}}{\text{mm}}} = 0.75 \text{ mm}$$

Example 10.1

The drain resistance of a FET is 2200Ω; the drain-source voltage changes by 5 V with $V_{GS} = -2$ V. Find the change in drain current.

Solution From Eq. (10.2),

$$\Delta I_D = \frac{\Delta V_{DS}}{r_d} = \frac{5}{2200} = 2.273 \text{ mA}.$$

Example 10.2

In Example 2, if V_{GS} changes by 2 V, find the value of transconductance.

Solution From Eq. (10.3),

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{2.273 \times 10^{-3}}{2} = 1.14 \text{ m℧}$$

Example 10.3

In examples 1 and 2, what is the resulting amplification factor?

Solution From Eq [10.4(a)]

$$\mu = r_d \times g_m$$
$$= (2200 \times 1.14 \times 10^{-3}) = 2.5$$

Example 10.4

In example 1, the drain-source voltage is increased and the device surpasses the ohmic region. If the device $V_P = 4$ V and $I_{DSS} = 10$ mA, find I_D.

Solution From Eq. (10.1),

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10 \times 10^{-3}\left(1 - \frac{-2}{-4}\right)^2 = 2.5 \text{ mA}$$

Example 10.5

In Figure 10.7 of example 10.4, find V_D, V_G and V_S.

Solution $V_D = V_{DSQ} = 7.31$ V

$V_G = V_{GS} = -1.5$ V and

$V_S = 0$ V

Example 10.6

In example 10.4, the device is damaged and replaced by a new FET. The values of I_{DSS} and V_P are only half of the first device; find the operating point.

Solution $I_{DSS\,(2)} = \dfrac{I_{DSS(1)}}{2} = 5$ mA and

$$V_{P\,(2)} = \frac{V_{P(1)}}{2} = -4 \text{ V}.$$

From Eq. (10.5); $V_{GS} = -V_{GG} = -1.5$ V

From Eq. (10.1);

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 5 \times 10^{-3}\left(1 - \frac{-1.5}{-4}\right)^2 = 1.953 \text{ mA}$$

$$I_{DQ} = 1.953 \text{ mA}$$

From Eq. (10.8);

$$V_{DS} = V_{DD} - I_D R_D$$
$$= 12 - (1.953 \times 10^{-3} \times 1.2 \times 10^3)$$

$$\boxed{V_{DS} = 9.66 \text{ V}}$$

The operating point $Q(I_{DQ}, V_{DSQ}) = (1.953 \text{ mA}, 9.66 \text{ V})$

Example 10.7

In example 6, find V_D, V_G and V_S.

Solution From Fig. 10.7.

$V_D = V_{DSQ} = 9.66$ V

$V_G = V_{GG} = -1.5$ V and

$V_S = 0$ V

Example 10.8

In example 10.5, find V_D, V_G and V_S.

Solution From Fig. 10.10

$V_D = V_{DS} + V_S$ where $V_S = I_D R_S$

i.e. $V_S = 1.6 \times 10^{-3} \times 1 \times 10^3 = 1.6$ V

i.e. $V_D = V_D + V_S = (9.12 + 1.6) = 10.72$ V

$V_G = 0$ V

Example 10.9

In example 10.5, if R_S is increased fourfold, find V_D, V_S and V_G

Solution New $R_S' = (1 + 4)R_S$

$= 5\ \text{k}\Omega$

$V_S = I_D \times R_S = 1.6 \times 10^{-3} \times 5 \times 10^3$

$= 8.0\ \text{V}$

$V_D = V_{DS} + V_S$

$= (9.12 + 8.0) = 17.12\ \text{V}$

$V_G = 0\ \text{V}$

Example 10.10

In example 10.8, find V_D and V_S.

Solution From Fig. 10.14,

$V_D = V_{DD} - I_D R_D$

$= (16 - 2.43 \times 10^{-3} \times 2.4 \times 10^3)$

$V_D = 10.17\ \text{V}$

$V_S = I_D \times R_S$

$= (2.43 \times 10^{-3} \times 1.5 \times 10^3) = 3.645\ \text{V}$

Example 10.11

In example 10.8, if the device is replaced by another FET with I_{DSS} and V_P values doubled, calculate the new operating point.

Solution For the new device

$I_{DSS} = 16\ \text{mA}$ and $V_P = -8\ \text{V}$

Equation (10.24) may be re-written as

$I_{DSS}\ (1.455)^2 + I_{DSS}\ (375\ I_D)^2 - I_{DSS}\ [2(1.455)(375\ I_D)] = 0$

$2250\ I_D^2 - 19.46\ I_D + 33.8 \times 10^{-3} = 0$

Solving for I_D, we get $I_D = 2.41\ \text{mA}$

Also, $V_{GS} = V_G - I_D R_S = -1.79\ \text{V}$

$V_{DS} = V_{DD} - I_D\ (R_D + R_S) = 6.6\ \text{V}$

The operating point $Q(I_{DQ}, V_{GSQ}, V_{DSQ}) = (2.41\ \text{mA}, -1.79\ \text{V}, 6.6\ \text{V})$

Example 10.12

In example 10.27, find V_D and V_S

From Fig. 10.14,

$V_D = V_{DD} - I_D R_S = 16 - 2.41 \times 10^{-3} \times 1.5 \times 10^3 = 12.39\ \text{V}$

$V_S = I_D R_S = 2.41 \times 10^{-3} \times 1.5 \times 10^3 = 3.62\ \text{V}$

Example 10.13

In example 10.10, find V_D and V_S

Solution From Fig. 10.16,

$$V_D = V_{DD} - I_D R_D$$
$$= (24 - 1.6 \times 10^{-3} \times 6.2 \times 10^3)$$
$$V_D = 14.08 \text{ V}$$
$$V_S = I_D R_S$$
$$= 1.6 \times 10^{-3} \times 1.5 \times 10^3$$
$$= 2.4 \text{ V}$$

Example 10.14

A relaxation oscillator constructed using UJT of example 10.15 uses $R = 10$ KΩ and $C = 1$ μF. Calculate the approximate frequency of oscillation if $V_{BB} = 10$ V.

Solution From Eq. 10.38; $f \simeq \frac{1}{T_C}$ and From Eq. 10.40

$$T_C = R_C \log_e \left[\frac{1}{1-n}\right]$$
$$= 10 \times 10^3 \times 1 \times 10^{-6} \log_e \left[\frac{1}{1-0.6}\right]$$
$$T_C = 9.163 \text{ mS}$$
$$f \cong \frac{1}{T_C} = \frac{1}{9.163 \times 10^{-3}} = 109.1 \text{ Hz}$$
$$f = 109 \text{ Hz}$$

Quiz Questions (Short-answer Questions)

Chapter 1: Semiconductor Physics and *PN* Junction

1.1 **Classify solid materials based on electrical properties**

Ans Solid materials may be classified into the following three types: (i) Insulators, (ii) Conductors, and (iii) Semiconductors.

1.2 **What do you mean by atomic number?**

Ans The number of protons or electrons in an atom is called the "atomic number".

1.3 **Give the atomic number for silicon, carbon and aluminium.**

Ans The atomic number for silicon is 14, for carbon it is 5, and for aluminium it is 13.

1.4 **What do you mean by forbidden energy gap?**

Ans The energy gap between the conduction band and the valence band is called 'forbidden energy gap'. In conductors this gap is zero; in insulators, it is too high; and in semiconductors, it is reasonably small.

1.5 **Give the forbidden-energy-gap value for silicon and germanium semiconductors.**

Ans The forbidden energy gap for silicon is 1.12 eV and for germanium it is 0.72 eV.

1.6 **The reverse saturation current is germanium is more than in silicon. Why?**

Ans The velence electrons in germanium are at higher energy level (4^{th} shell) compared to silicon (3^{rd} shell). Thus, germanium produces more electron-hole pairs them silicon (the valence electrons require less energy to become free), and hence the reverse saturation (leakage) current is more in germanium.

1.7 **What do you mean by intrinsic and extrinsic semiconductors? Explain**

Ans The semiconductor in its pure form is called intrinsic semiconductor. Silicon and germanium are intrinsic semiconductors and have 4 valence electrons.

The semiconductor with an impurity added to it to increase its conductivity is called an extrinsic semiconductor.

1.8 **What is doping? Explain**

Ans The process of converting an intrinsic semiconductor into an extrinsic semiconductor is called doping. In other words, the process of adding impurity to an intrinsic semiconductor to change its conductivity is called doping.

1.9 **Name a few impurity (dopent) materials that are commonly used.**

Ans The dopents are of two types;

(a) Donor type or pentavalent impurity: Phosphorous, Arsenic, Antimony, etc.

(b) Acceptor type or trivalent impurity: Indium, Gallium, Aluminium, etc.

1.10 **How are *P*-type and *N*-type semiconductors produced? Explain**

Ans Addition of a pentavalent impurity to an intrinsic semiconductor results in an *N*-type semiconductor.

Similarly addition of a trivalent impurity to an intrinsic semiconductor results in a *P*-type semiconductor.

1.11 **In equally doped extrinsic semiconductors, *N*-type has larger conductivity than *p*-type semiconductor. Why?**

Ans Electrons are the majority carriers in *N*-type semiconductors, and mobility of electrons is greater than holes at a given level of doping. This results in increased conductivity of *N*-type semiconductors.

1.12 **What is the effect of increasing temperature on the conductivity of semiconductors?**

Ans Semiconductors have negative temperature coefficient (α) and hence increase in temperature results in increased conductivity and reduced resistivity.

1.13 **An unbiased *PN* junction has no current flowing through it. Why?**

Ans When a *PN* junction is formed, it results in a depletion region across the junction. This in-turn stops free electrons from *N*-type and free holes from *P*-type to cross the junction. Hence, there will be no current flow.

1.14 **Leakage current in germanium is more compared to silicon. Why?**

Ans The valence electrons in germanium are at a higher energy level (4^{th} shell in Ge and 3^{rd} shell is Si) compared to silicon. Thus, even at a small additional energy. Ge results in large electron-hole pairs compared to Si. Hence, Ge has more leakage current compared to Si.

1.15 **Silicon is a widely used semiconductor as compared to germanium. Justify.**

Ans For a given amount of biasing (additional energy), the leakage current/reverse saturation current is less in Si material when compared to Ge material. This makes Si more suitable for applications than Ge, and hence Si is widely used.

1.16 **Draw the *VI* characteristics of a biased *PN* junction and mark salient parameters on the curve.**

Ans The *VI* curve of a *PN* junction is shown in Fig. Q1.16.

Legend:

(i) V_{FB}: Forward break-over voltage or knee-voltage

(ii) V_{RB}: Reverse break-over voltage

(iii) Forward dynamic resistance R_d

$$= \frac{\Delta V_{Ak}}{\Delta I_D} \Omega$$

(iv) Forward static resistance

$$R_f = \frac{V_D}{I_D} \Omega$$

(v) $V_r = V_{FB}$: Cut-in or knee voltage

(vi) Reverse resistance

$$R_r = \frac{V_{RB}}{I_R} M\Omega$$

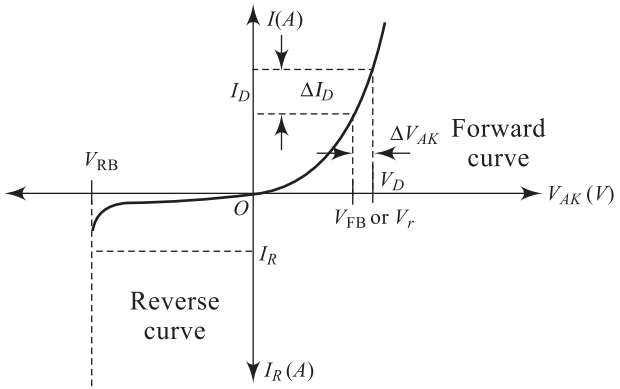


Fig. Q1.16 *VI* characteristics of a *PN* junction

1.17 **On a common scale, draw the *VI* characteristics of Si and Ge *PN* junctions.**

Ans The *VI* characteristics of Si and Ge *PN* junctions is shown in Fig. Q1.17.

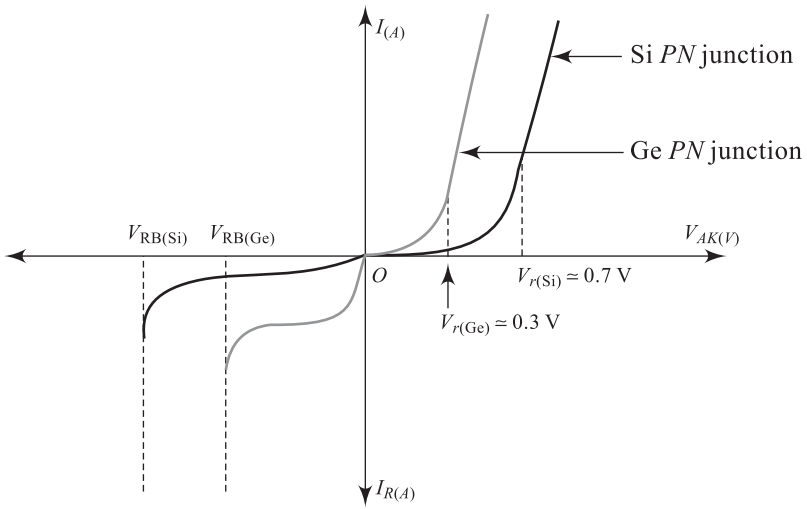


Fig. Q1.17 *VI* characteristics of Si and Ge *PN* junctions

1.18 **Define forward resistance of a *PN* junction.**

Ans For a forward biased *PN* junction, two forward resistances may be defined:

(i) *Static forward resistance (R_f)* defined as the ratio of forward voltage (V_F) to the corresponding forward current (I_D)

i.e. $$R_f = \frac{V_D}{I_D} \Omega$$

Normally, R_f is very small and will be in the order of few tens of ohms:

(ii) Dynamic forward resistance (R_d), defined as the ratio of change in forward voltage (ΔV_D or ΔV_{Ak}) to the corresponding change in forward current (ΔI_D).

i.e. $$R_d = \frac{\Delta V_D}{\Delta I_D}\ \Omega$$

Normally, R_d is very small (Approximately = R_f)

1.19 **Define reverse resistance of a *PN* junction.**

Ans It is defined as the ratio of reverse voltage (V_{RB}) to reverse current I_R.

i.e. $$R_r = \frac{V_{RB}}{I_R}\ M\Omega$$

Normally, reverse resistance R_r will be very high and will be in the order of a few mega ohms.

1.20 **Write the current equation for a *PN* junction diode.**

Ans The diode current equation is

$I_D = I_O\ [e^{V/\eta V_T} - 1]$ amperes where I_O is the reverse saturation current for the diode.

1.21 **Comment on the diode current equation.**

Ans The diode current equation is given in Q.1.20. Here, the reverse saturation current I_O is a very small value. I_O is of the order of nano-amperes (ηA): v is the voltage across diode; for possible values, I increases exponenetially and for negative values of v, I is almost I_O as indicated in the Fig. 1.42 η is a constant equal to 1 for Ge and 2 for Si. V_T is the voltage equivalent of temperature, dependent on Boltzmann constant k, charge of electron q and temperature T.

1.22 **Name the capacitances associated with the biased *PN* junction diode.**

Ans A conducting *PN* junction diode has two capacitances associated with it; C_D diffusion capacitance under forward biased condition and C_T transition capacitance under reverse biased condition.

1.23 **What is an ideal diode?**

Ans A diode is one which has zero forward resistance ($R_f = 0$), zero cut-in voltage ($V_\gamma = 0$) and infinite reverse resistance ($R_r = \propto$).

1.24 **Can an ideal diode be used as a switch?**

Ans Yes, an ideal diode is a closed switch when forward biased and an open switch when reverse biased.

1.25 **Draw the equivalent circuit of a PN junction diode.**

Ans The equivalent circuit for a *PN* junction diode is shown in Figure Q. 1.25

(a) Forward biased (b) Reverse biased

Fig. Q1.25 Diode equivalent circuit

Chapter 2: Diode Applications

2.1 **What do you mean by cut-in voltage of a diode?**

Ans In a forward-biased diode, the minimum anode-cathode voltage (V_{AK}) required for recognizable diode current flow is called cut-in voltage (V_{ξ})

2.2 **What is the effect of temperature on V_{γ}?**

Ans V_{γ} reduces with increase in temperature ($-ve\ \alpha$)

2.3 **List the value of cut-in voltage for Si and Ge diodes**

Ans The cut-in voltage for

Si diode $V_{\gamma\,(Si)} = 0.6$ V and

Ge diode $V_{\gamma\,(Ge)} = 0.2$ V

2.4 **List various blocks of a regulated power supply (RPS)?**

Ans An RPS contains a step-down transformer, a rectifier, a filter and a regulator.

2.5 **What are the main functions of the above listed blocks of a RPS?**

Ans Functions of various blocks of an RPS (i) Step-down transformer → Provides isolation between high tension voltage (230 V) and user side; steps down the voltage (ii) Rectifier → converts ac i/p to dc o/p (iii) Filter → improves quality of dc o/p and reduces ripples (iv) Regulator → Regulates o/p dc against load and line variations.

2.6 **Sketch the *VI* characteristics of an Si diode and a Ge diode on common axes and mark various parameters on the curves.**

Ans

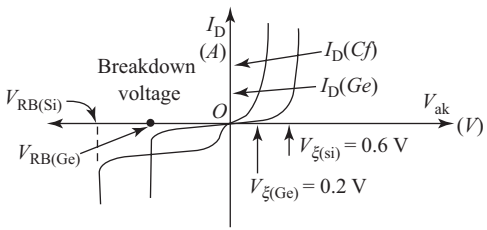


Fig. Q2.6 *VI* characteristics of Si and Ge diodes

2.7 **What the importance of load line?**

Ans A load line indicates the operating point for the circuit. The zero-signal values of diode current and anode-cathode voltage forms the dc loadline for diode circuit.

2.8 **What is a converter or rectifier?**

Ans A converter is a circuit which converts the input ac signal into output dc signal.

2.9 **How do you classify rectifier circuits?**

Ans Rectifier circuits are broadly classified into two types: (i) Half-wave rectifiers (ii) Full-wave rectifiers.

2.10 **What is the major difference between a half-wave rectifier and a full-wave rectifier?**

Ans A half-wave rectifier converts only one-half cycle of input ac into dc, but a full-wave rectifier converts both half-cycles of input ac into dc.

2.11 **List the disadvantages of a half-wave rectifier as compared to a full-wave rectifier.**

Ans Disadvantages/drawbacks/limitations of an HWR;

(i) Converts only one half-cycle of i/p ac to o/p dc and hence less conversion efficiency is only 40.6%

(ii) The output contains more ac components than the dc components and hence ripple factor is high upto 121%

(iii) The transformer utilization (TUF) is very low and is only 28.7%

2.12 **Compare the performance of the two full-wave rectifier circuits.**

Ans The two FWR circuits; the centre-tapped FWR and the bridge-type FWR have

(i) the same conversion efficiency of 81.2%

(ii) the same ripple factor of 48%

(iii) bridge-type FWR uses 4 diodes against 2 diodes in centre-tapped type.

(iv) The PIV rating of diodes in a centre-tapped FWR is twice that of bridge-type FWR ($2V_m$ against V_m)

(v) The TUF is 69.3% in

2.13 **What is the role of a filter in a dc power supply?**

Ans The o/p of a rectifier is a pulsating one and contains more ripples. In order to reduce the ripples and smoothen the o/p, filters are used.

2.14 **In the construction of filter, capacitors (c) are connected in shunt and inductors (*L*) in series with load; explain why?**

Ans For filter construction, always *L* is connected in series, because, an inductor allows dc to flow through and blocks ac components. Similarly, *C* is connected in shunt with load, because, a capacitor allows ac to ground and routes dc components to load.

2.15 **List different types of filters that are generally used.**

Ans Different filters that may be used are (i) *C*-filter, (ii) *L*-filter (iii) *LC* or choke input filter (iv) *CLC* or π filter.

2.16 **Which is the best filter to use and why?**

Ans A *CCL*-filter or a π-filter is the best filter to use; because it offers smooth output (more dc) and better ripple factor.

2.17 **What is the function of a voltage regulator? Explain.**

Ans A regulator in an RPS is to maintain a steady output voltage against any changes in the input line voltage (line regulation) or changes in the load demand (load regulation). A regulator maintains this over a range of V_{in} or I_L.

2.18 **Define regulation for a power supply.**

Ans Regulation is defined as change in output voltage from no-load condition to full-load condtion.

$$R_{egn} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

2.19 **Classify regulators that are used in a power supply.**

Ans (A) Voltage regulators → Series voltage regulators; Shunt voltage regulators

(B) Current regulators → Series current regulators; Shunt current regulators

2.20 **What is the role of a zener diode connected after a filter in an RPS?**

Ans A zener diode in an RPS acts as a regulator that provides constant output voltage against line and load variations.

2.21 **List at least one advantage and one disadvantage of a zener regulator.**

Ans *Advantage*: A zener regulator is very simple and cheap.
Disadvantage: A zener regulator output voltage is fixed to zener voltage V_z and offers poor regulation.

2.22 **What is the role of a diode voltage multiplier?**

Ans A voltage multiplier circuit is used to increase the input voltage value. A voltage doubler increases the i/p voltage by two fold, a tripler increases it by threefold, and so on.

2.23 **A voltage doubler uses V_m sin ωt as its i/p; what is its o/p?**

Ans The output of the doubler is $V = 2V_m = 2V_P$.

2.24 **Name at least two different wave-shaping circuits using diode.**

Ans Clipping circuits and clamping circuits are the two wave-shaping circuits using diodes.

2.25 **What is the main role of clipping circuit?**

Ans A clipping circuit is used to remove or clip one or more parts of an input ac waveform; the remaining part of the input signal is passed to output undistorted.

2.26 **What is the role of a clamping circuit?**

Ans A clamping circuit is used to shift the input signal above or below the given reference level without actually altering its original shape.

2.27 **Why a clamper is also called a dc restorer circuit?**

Ans A clamper is also called as a dc restorer or dc re-inserter because of the reason that the circuit re-introduces dc conditions to the input signal.

2.28 **A two-level clipper has reference voltages V_{ref} = ±2 V; if the input voltage is sinusoidal, crossing the reference voltages (well above ±2 V), what is the shape of an output?**

Ans Since the input crosses reference voltage on either side, the output is approximately a square wave as shown in Fig. Q. 2.28.

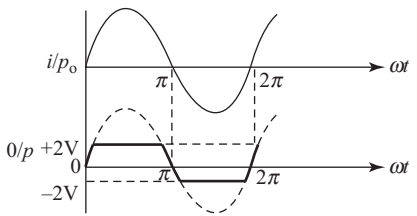


Fig. Q. 2.28

Chapter 3: Bipolar Junction Transistors

3.1 **Define in your own words a transistor.**

Ans (i) A transistor is a three-terminal, two-junction semiconductor device, generally used to increase the strength of an input, signal.

(ii) *Transistor* means 'transfer of resistance' which in turn means high resistance offered at input is transformed into low resistance at output.

(iii) A transistor is a semiconductor device that is referred to as two back-to-back connected *PN* junction diodes.

3.2 **Name the different types of transistor you know.**

Ans Bipolar Junction Transistor (BJT), Field Effect Transistor (FET) and Uni Junction Transistor (UJT) are some of the popular transistors.

3.3 **Name the three terminals of a BJT.**

Ans Base (B), Emitter (E) and Collector (C) are the three terminals of a BJT.

3.4 **Name the two junctions of a BJT.**

Ans Base-Emitter (BE or input) junction and the Base-Collector (BC or output) junction are the two junctions in a BJT.

3.5 **Name the two types of charge carriers in a BJT.**

Ans In a BJT, there are two types of charge carriers—the majority charge carriers and the minority charge carriers.

3.6 **Name two different types of popular BJTs.**

Ans The two popular BJTs that are commercially available are *NPN* and *PNP* transistors.

3.7 **Draw the basic structure and the corresponding circuit symbols of the two transistors.**

Ans Transistor structure and the corresponding symbols are given in Fig. Q3.7.

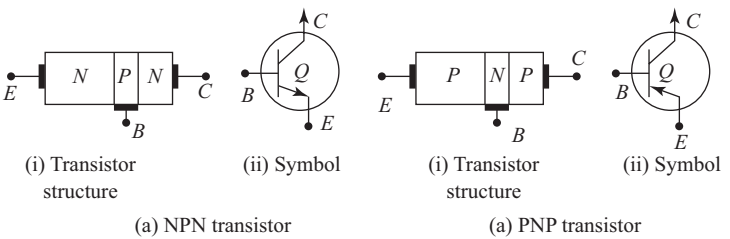


Fig. Q3.7 Bipolar junction transistors

3.8 **Comment on the doping levels of E-B-C of a BJT.**

Ans An Emitter which is largest of the three terminals is heavily doped, since it has a supply of large number of charge carriers (electrons in *NPN* and holes in *PNP* type). The base is thinnest of the three and is lightly doped. The collector is medium in width and is moderately doped.

3.9 **Name the three popular configurations of BJT.**

Ans A BJT may be connected in a circuit in one of the following three configurations:

(i) Common Emitter Configuration

(ii) Common Base Configuration

(iii) Common Collector Configuration

3.10 **What is a load line?**

Ans A load line for any device represent the relationship between the device voltage and the corresponding device current. Figure Q3.10 indicates the two load lines generally possible for any device. (Refer Q. 2.7 also)

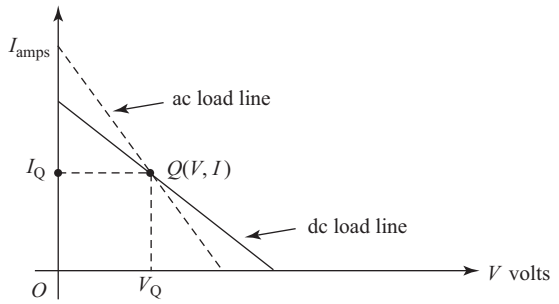


Fig. Q3.10 Load line for a device

3.11 **Define operating point (*Q*-point) for a BJT.**

Ans The quiescent point or operating point (*Q*-point) for a BJT represents the zero-signal values of the collector-emitter voltage V_{CE} and the corresponding value of collector current I_C.

As indicated in Figure Q3.11, $V_{CE(max)}$ with $I_C = 0$ and $I_{C(max)}$ with $V_{CE} = 0$ represent the extremities of the dc load line. Every point on the load line represents a *Q*-point.

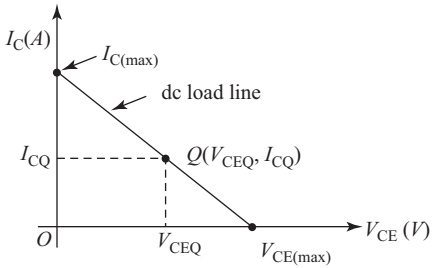


Fig. Q3.11 BJT operating point and load line

3.12 **What are the benefits of common collector (CC) configuration?**

Ans A CC configuration offers high input impedance, low output impedance and a good current amplification.

3.13 **What are the important applications of CC configuration?**

Ans A CC configuration is useful in impedance matching, current amplification, buffering, etc.

3.14 **What are the benefits of common emitter (CE) configuration?**

Ans A CE configuration offers a good voltage amplification, a moderate current amplification and hence a good power amplification.

3.15 **What are the important applications of CE configuration?**

Ans A CE configuration is useful in applications like amplification, oscillation (signal generation), power amplification, etc.

3.16 **What are the drawbacks of common base (CB) configuration?**

Ans A CB configuration has low input impedance, high output impedance, very less current amplification.

3.17 **What are the advantages of CB configuration?**

Ans A CB configuration offers good voltage amplification and suited well for high-frequency applications.

3.18 **What is an amplifier?**

Ans An amplifier is a circuit that is used to increase strength of a weak signal.

3.19 **If a transistor is used for amplification. What are the biasing conditions of transistor junctions?**

Ans In order that a transistor works as an amplifier, its base-emitter junction should be forward biased and base-collector junction should be reverse biased.

3.20 **Define operating point (*Q*-point) for a transistor.**

Ans The *Q*-point for a BJT is the zero-signal values of collector current I_C and collector-emitter voltage V_{CE} ie $Q(V_{CEQ}, I_{CQ})$. The *Q*-point lies on the BJT load line with ordinates I_{CQ} and V_{CEQ}.

3.21 **Name different biasing methods available for transistor circuits.**

Ans The following are the four important transistor biasing methods in use:
(i) Fixed bias (ii) Feed-back bias or Collector-base bias (iii) Self-bias (iv) Potential divider bias

3.22 **How do we measure the performance of a transistor biasing method?**

Ans The performance of a transistor biasing circuit is measure using the performance parameter called the stability factor.

3.23 **Define stability factor.**

Ans Stability factor for a biasing circuit may be defined as the variation of the collector current I_C due to variations in three parameters of BJT, namely current gain, leakage current and base-emitter voltage.

3.24 **Which biasing method is the best and why?**

Ans Potential divider or voltage divider or self-bias with potential divider is the best biasing method. A potential-divider bias offers very small variation of collector current or, in other words, a good stability factor, and hence is the best method.

3.25 **Can we use a transistor as a switch?**

Ans Yes, a transistor can be used as a switch.

3.26 **How can you use a transistor as a switch?**

Ans A transistor when operated in cut-off (open switch) region and saturation (closed switch) region acts as an electronic switch.

3.27 **What is an emitter follower?**

Ans The CC configuration of a BJT is referred to as an emitter follower.

3.28 **What are the salient features of an emitter follower?**

Ans An emitter follower has unity voltage gain, very high input impedance, very low output impedance and good bandwidth.

3.29 **Name important applications of an emitter follower.**

Ans An emitter follower finds its applications in impedance matching, current amplification and buffering.

3.30 **What advantage do the bias compensation circuits.**

Ans Bias compensation circuits offer good stability and minimise the gain loss.

Chapter 4: BJT amplifiers, Feedback and Oscillators

4.1 **What is an amplifier?**

Ans An amplifier is a circuit that uses a weak input signal and produces a strong output signal. It is important that the shape of the input signal is to be maintained.

4.2 **What are different parameters for the input signal that an amplifier may strengthen?**

Ans An amplifier may increase the input voltage or input current or power (both voltage and current) at the output.

4.3 **Classify amplifiers based on frequency of operation.**

Ans (a) Audio Frequency (AF) amplifiers
(b) Radio Frequency (RF) amplifiers.

4.4 **Classify amplifiers based on the parameter amplified for the input signal.**

Ans (a) Voltage amplifiers
(b) Current amplifiers
(c) Power amplifiers

4.5 **Write the expressions for A_V and A_I in dB.**

Ans
$$A_V = 10 \log \left[\frac{V_o}{V_{in}} \right]$$

$$A_I = 10 \log \left[\frac{I_o}{I_{in}} \right]$$

4.6 **Write the expression for A_P in dB.**

Ans $A_P = 10 \log \left[\frac{P_o}{P_{in}} \right] = 20 \log \left[\frac{I_o}{I_{in}} \right] = 20 \log \left[\frac{V_o}{V_{in}} \right]$

4.7 **Classify the amplifiers based on number of amplification stages used.**

Ans (a) Single-stage amplifiers
(b) Multistage amplifiers

4.8 **Write the overall gain equation for a multistage amplifier in terms of stage gain.**

Ans Overall gain

$$A = A_1 \times A_2 \times \cdots \times A_N$$

where A_1, A_2, … are stage gains of N-stages.

4.9 **If the individual stage gains are in dB, then write the overall gain expression for a multistage amplifier.**

Ans Overall gain

$$A = (A_1 + A_2 + \cdots + A_N)\text{dB}$$

where A_1, A_2 … are stage gains in dB.

4.10 **Classify the amplifiers based on the location of operating point on the load line.**

Ans (a) Class-A amplifiers
(b) Class-B amplifiers
(c) Class-C amplifiers
(d) Class-AB amplifiers
(e) Class-D amplifiers

4.11 **Classify the amplifiers based on the type of coupling used to interconnect two stages.**

Ans (a) Direct-coupled amplifies
(b) RC coupled amplifiers
(c) Transformer-coupled amplifiers

4.12 **Name the two types of Class-A amplifier.**

Ans (a) Series-fed Class-A amplifier
(b) Transformer-coupled Class-A amplifier

4.13 **What is the maximum theoretical conversion efficiency of a Class-A amplifer?**

Ans (a) For Series-fed Class-A, $\eta_{max} = 25\%$
(b) For transformer-coupled Class-A, $\eta_{max} = 50\%$

4.14 **What is the maximum theoretical conversion efficiency of a Class-B amplifier?**

Ans For Class-B, $\eta_{max} = 78.5\%$

4.15 **Name any two advantages of push-pull amplifiers.**

Ans Push-pull amplifiers
(i) offer very high conversion efficiency
(ii) eliminate even harmonies is the output and hence reduce distortion.

4.16 **List different features of Class-C operation.**

Ans In a Class-C operation,
(i) the output/collector current I_C flows for less than 180° of input.
(ii) I_C flows in the form of pulses and hence good conversion efficiency.
(iii) Lesser the conduction period (IC flow) more will be efficiency for the amplifier.

4.17 **In a Class-AB operation, can we achieve a conversion efficiency more than that in a Class-B operation?**

Ans No, that is not possible. The conversion efficiency of a Class-AB amplifier may be close to 78.5%, but not more than that.

4.18 **List at least two advantages of complementary amplifier.**

Ans A complementary-symmetry amplifer
(i) eliminates the i/p and o/p transformers.
(ii) minimizes distortion in the o/p (humming due to transformers is eliminated)

4.19 **What is the distortion that we observe in a Class-B amplifier?**

Ans A complementary-symmetry amplifier has the "Crossover distortion" in the output.

4.20 **Indicate through waveforms the crossover distortion in a Class-B amplifier.**

Ans Refer Fig. 4.12.

4.21 **Draw the frequency response of an amplifier and mark important points on the response.**

Ans Refer Fig. 4.16.

4.22 **Draw a simple block diagram to explain the principle of feedback.**

Ans Refer Fig. 4.22.

4.23 **What are the advantages of negative feedback?**

Ans Refer section 4.8.

4.24 **Give the classification of oscillators.**

Ans Refer Section 4.10.

4.25 **Give two examples each for AF oscillators and RF oscillators.**

Ans (a) AF oscillators—*RC* phase shift and wein bridge oscillators
(b) RF oscillators—Hartley and colpitts oscillators

Chapter 5: Communication Systems

5.1 **A modulation process involves two different signals, name them.**

Ans The two signals used in modulation are

(i) modulating signal or message signal

(ii) modulated signal or carrier signal

5.2 **What is modulation?**

Ans The process of changing the characteristics of the carrier signal according to variations in the information (message) signal is called modulation.

5.3 **Name the important components of a communication system.**

Ans The source of information, transmitter, receiver, channel and destination are components of a communication system.

5.4 **Draw the simple block diagram of a communication system.**

Ans Refer Fig. 5.2.

5.5 **Draw the block diagram of a wireless communication system.**

Ans Refer Fig. 5.3.

5.6 **What is the medium of communication (i.e. channel) in a wireless communication system?**

Ans Free space or air is the medium (channel) of communication in a wireless communication system.

5.7 **Name some of the important blocks of a digital communication system.**

Ans Refer Fig. 5.4.

5.8 **Draw the block diagram of a simple digital communication system.**

Ans Refer Fig. 5.4.

5.9 **List some advantages of modulation.**

Ans Some of the advantages of modulation are

(i) signal can be transmitted over longer distances,

(ii) modulation reduces interference or mixing of signals,

(iii) multiplexing of signals is possible, and

(iv) better utilization of resources is possible.

5.10 **What is amplitude modulation?**

Ans Changing the amplitude of the carrier (high frequency) signal according to the instantaneous changes in amplitude of the information (low frequency) signal is called amplitude modulation.

5.11 **Write the expression for AM output.**

Ans Refer Eq. [5.5 (a)].

5.12 **Represent graphically the AM output expression and indicate clearly all relavent information.**

Ans Refer Fig. 5.6.

5.13 **What is modulation index? Explain.**

Ans Modulation index is the ratio of amplitudes of modulating wave to modulated wave,

i.e. $$m = \frac{V_m}{V_c}$$

It indicates the depth of modulation or percentage of modulation.

5.14 **Write the expression for modulation index in terms of V_{max} and V_{min} of Am output.**

Ans Modulation index $$m = \frac{V_m}{V_c} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

5.15 **How many side bands are there in an AM output? What are they?**

Ans An AM output contains two side bands called the Lower Side Band (LSB) and the Uppar Side Band (USB).

5.16 **Express the total power transmitted in an AM signal in terms of modulation index and carrier power.**

Ans Refer Eq. (5.15).

Here m = modulation index and P_c = carrier power.

5.17 **What is the amount of power contained in each sideband of an AM output?**

Ans Refer Eq. (5.14).

5.18 **Is the bandwidth (BW) of AM signal dependent on carrier frequency? Write the expression for BW of AM signal.**

Ans No, BW is dependent only on information signal frequency 'f_m' and is given by BW = $2f_m$.

5.19 **What is the effective modulation index for an AM signal, when multiple information signals are used?**

Ans Refer Eq. (5.18).

5.20 **Write the expression for total power transmitted in Q. 5.19.**

Ans Refer Eq. (5.19).

5.21 **Name a few popular AM schemes.**

Ans These are many popular AM schemes in use; DSB-FC, DSB-SC, SSB are some of them.

5.22 **In a DSB-FC system, name the signal components contained in the output.**

Ans DSB-FC means double-side-band full carrier AM output; hence, it contains a carrier signal and the two side bands, namely USB and LSB.

5.23 **In a DSB-SC system, name the signal components contained in the output.**

Ans DSB-FC means "double-side-band suppressed carrier" AM output; hence, it contains the two sidebands, namely USB and LSB, but no carrier.

5.24 **In an SSB system, name the signal components contained in the output.**

Ans SSB means "single-side-band" AM output; hence it contains only one side band, either USB or LSB, and no carrier signal.

5.25 **Compare bandwidth required for a DSB-FC and a DSB-SC AM system.**

Ans Both DSB-FC and DSB-SC AM systems need a bandwidth of $2f_m$ for transmission.

5.26 **Compare the bandwidth requirements of DSB-SC and SSB systems.**

Ans A DSB-SC system needs a bandwidth of $2f_m$, while an SSB system needs a bandwidth of only f_m.

5.27 **What is the power contained in an SSB output in terms of total power transmitted.**

Ans An SSB output contains 25% of total power transmitted at $m = 1$.

5.28 **Explain angle modulation?**

Ans Frequency modulation (FM) and phase modulation (PM) are together called angle modulation.

5.29 **What is frequency modulation?**

Ans Changing the frequency of the carrier signal according to instantaneous changes in the amplitude of the message signal (amplitude of carrier is unchanged) is known as frequency modulation.

5.30 **What is the bandwidth needed for FM transmission?**

Ans FM transmission needs ideally infinite bandwidth; but using Carson's rule, it is approximately $2(\delta + f_m)$

5.31 **What is demodulation? Explain.**

Ans Demodulation, or detection, is the process of recovering the message signal from the modulated output. It is the reverse process of modulation.

5.32 **Name any two types of radio receivers.**

Ans (i) *TRFM* Tuned Radio Frequency radio receiver.
(ii) Superheterodyne radio receiver.

5.33 **In a superheterodyne radio receiver, if f_s and f_o are mixer inputs, express the mixer output in terms of inputs.**

Ans Mixer output is $(f_o + f_s)$.

5.34 **Name the modulation techniques used for audio and video signals in a television system.**

Ans FM for audio signal and AM for video signal.

Chapter 6: Linear Integrated Circuits

6.1 **What are linear Integrated Circuits (ICs)?**

Ans Linear ICs are those which use time-varying input and produce time-varying outputs.

6.2 **Name few popular linear ICs.**

Ans Operational Amplifier (op-amp), timer, phase-locked loops are some popular linear ICs.

6.3 **What is an op-amp?**

Ans An op-amp is a direct-coupled, high-gain, difference amplifier.

6.4 **Name important stages of an op-amp.**

Ans An op-amp mainly contains four stages; stage-1 and 2 are difference amplifiers, stage-3 is level shifter or level translater and stage-4 is driver stage (output stage).

6.5 **List some of the characteristics of an op-amp.**

Ans An op-amp is characterized by high gain, high input impedance, low output impedance, high bandwidth, low noise, high common mode rejection ratio (CMMR), etc.

6.6 **Name the op-amp parameter that measures its ability to accept only difference in input signals.**

Ans CMRR is the ability of an op-amp to reject all common-mode signals and accept difference in inputs.

6.7 **Name the op-amp parameter that measures its ability to respond to high-frequency inputs.**

Ans Slew rate

6.8 **Name the op-amp parameter that measures its sensitivity to power supply variations.**

Ans Power Supply Rejection Ratio (PSRR)

6.9 **Name the op-amp parameters that makes it a better connector between source and load.**

Ans Input impedance (Z_i) and output impedance (Z_o)

6.10 **Explain common mode rejection ratio?**

Ans CMRR of op-amp is defined as the ratio of differential mode gain A_d to common mode gain A_c.

i.e $$\text{CMRR} = \frac{A_d}{A_c}$$

It is the ability of the op-amp to reject the common mode input signals.

6.11 **Explain what is slew rate.**

Ans Slew Rate (SR) is defined as maximum rate of change of output voltage per unit time (expressed as volts per μS)

i.e. $$\text{SR} = \left.\frac{dV_o}{dt}\right|_{\max} \text{ V/μS}$$

It is the ability of an op-amp to respond to high-frequency input signals.

6.12 **What are the important characteristics of an ideal op-amp?**

Ans Refer Section 6.3 on Page 243.

6.13 **List some important applications of an op-amp.**

Ans Some of the important applications of an op-amp are
(i) amplifier, (ii) oscillator, (iii) regulator, (iv) active filter, (v) butter, and (vi) signals summing, etc.

6.14 **What is the phase relationship between input and output in an inverting amplifier?**

Ans Input and output are 180° out of phase.

6.15 **What is the phase relationship between input and output in a non-inverting amplifier?**

Ans Input and output are in phase with each other. (0° or 360° or $n \times 360°$ out of phase).

6.16 **What is the phase relationship and input-output relationship in a voltage follower?**

Ans Input v_i and out v_o are equal and in-phase with each other. ($A_v = 1$)

6.17 **Draw the input-output waveforms for a buffer.**

Ans Refer Fig. 6.18(b) and (c).

6.18 **Write the output expression for an op-amp integrator.**

Ans Refer Eq. (6.45).

6.19 **The input to an op-amp integrator is square wave of frequency greater than the cut-off frequency; what is the output?**

Ans $f > f_c$, integrator acts as high-frequency discriminator and output is a triangular wave.

6.20 **Write the output expression for op-amp differentiator.**

Ans Refer Eq. (6.48).

6.21 **The input to an op-amp differentiator is a triangular wave of frequency less than the cut-off frequency; what is the output?**

Ans $f < f_c$, differentiator acts as a low-frequency discriminator and the output is a square wave.

6.22 **What is an instrumentation amplifier?**

Ans A 3-op-amp difference amplifier that offers equal input impedance to the two inputs is called an instrumentation amplifier.

6.23 **Write the expression for LTP and UTP of Schmitt trigger**

Ans Refer Eq. [6.64(b)] and Eq. [6.65(b)].

6.24 **Write the expression for hysterisis in terms of β and V_o for a Schmitt trigger.**

Ans Refer Eq. [6.66(c)].

6.25 **Input to the Schmitt trigger is a triangular wave, what is the output?**

Ans Asymmetrical square wave

6.26 **Input to the Schmitt trigger is a sine wave, what is the output?**

Ans Asymmetrical square wave.

6.27 **List the advantages of active filter.**

Ans (i) offers gain to the output.
(ii) offers high Z_{in} and low Z_o
(iii) separation between pass band and step band is steep
(iv) offers better frequency response and slew rate

6.28 **List the disadvantages of an active filter.**

Ans (i) Two power supplies for op-amp.
(ii) Filter cost is more
(iii) Filter is bulky.

6.29 **Classify the filters based on frequency response.**

Ans (i) Low Pass filter (LPF)
(ii) High Pass filter (HPF)
(iii) Band Pass filter (BPF)
(iv) Band Elimination Filter (BEF)

6.30 **What is the slope of response for a first-order filter?**

Ans 20 dB/decade

6.31 **What is the slope of the response in a second-order filter?**

Ans 40 dB/decade

6.32 **What is the result of cascading an LPF (f_{CL}) and an HPF (f_{CH})?**

Ans Results in a BPF if $f_{CL} > f_{CH}$.

6.33 **What is the effect of connecting parallely a LPF and a HPF suitably summing their outputs?**

Ans Results in a BEF

6.34 **Define quality factor for filter.**

Ans Q-factor is defined as the ratio of cut-off frequency 'f_c' to the bandwidth.

$$Q = \frac{f_c}{\text{BW}}$$

6.35 **What is the importance of Q-factor for a filter?**

Ans Q-factor is the 'figure of merit' for the filter. It is the measure of selectivity for filter.

6.36 **Name a few applications of the 555-timer.**

Ans (i) A stable multivibrator
(ii) Monostable multivibrator
(iii) Capacitance meter

6.37 **Name some important blocks of a PLL.**

Ans (i) Phase detector
(ii) Low pass filter
(iii) Voltage controlled oscillator.

6.38 **List a few applications of PLL.**

Ans (i) Frequency multiplier
(ii) Frequency translator
(iii) AM detector
(iv) FM detector
(v) FSK detector

Chapter 7: Digital Electronics

7.1 **What is an analog signal?**

Ans A signal whose amplitude changes as a continuous function of time is called an analog signal.

7.2 **What is a digital signal?**

Ans A signal whose amplitude is a discrete function of time is called a digital signal.

7.3 **What is the circuit that converts a time-varying signal into discrete form?**

Ans Analog to Digital Converter (ADC).

7.4 **Name the circuit that converts digital signal into a continuous time signal.**

Ans Digital to Analog Converter (DAC)

7.5 **What do you mean be radix of a number system?**

Ans The radix or base of a number system is the total number of digits used in that system.

7.6 **Name two advantages of digital systems.**

Ans Fast processing, compact in size.

7.7 **Name two disadvantages of analog systems.**

Ans Complex design, costly.

7.8 **What is the radix of the octal number system?**

Ans Radix 8.

7.9 **List all valid digits of the octal system.**

Ans 0, 1, 2, 3, 4, 5, 6, and 7.

7.10 **What is the radix of the hexadecimal system?**

Ans Radix 16.

7.11 **List all valid digits of the hexadecimal system.**

Ans 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, *A*, *B*, *C*, *D*, *E* and *F*.

7.12 **Name few popular number systems in use.**

Ans Binary Number System—Radix 2
Octal Number System—Radix 8
Decimal Number System—Radix 10
Hexadecimal Number System—Radix 16

7.13 **Name the methods used for signed number representation.**

Ans (i) Sign magnitude representation
(ii) Sign 1's complement representation
(iii) Sign 2's complement representation

7.14 **What is the most commonly used method of the above in computing systems?**

Ans 2's compliment method.

7.15 **With and Example, list advantages of number-base conversions.**

Ans Decimal to hexadecimal conversion—Easy processing
Hexadecimal to Decimal conversion—Easy understanding.

7.16 **What is positive logic?**

Ans 0—logic low (Zero volts)
1—logic high (Five volts)
} positive logic

7.17 **What is negative logic?**

Ans 0—logic high (Five volts)
1—logic low (Zero volts)
} Negative logic

7.18 **Name the logic gate with *n* inputs that produces a logic high output only when all inputs are at logic high.**

Ans AND gate.

7.19 **Name the logic gate with *n* inputs that produces a logic low output only when all inputs are at logic low.**

Ans OR gate.

7.20 **Name the logic gate with single input which produces output that is a compliment of the input.**

Ans NOT gate (Inverter gate)

7.21 **Name the logic gate with *n* inputs that produces a logic high output when odd number of inputs are logical high.**

Ans EX-OR gate

7.22 **Name the logic gate with *n* inputs that produces a logic high output when even number of inputs are logic high.**

Ans EX-NOR gate.

7.23 **Name the logic gate with *n* inputs that produces a logic high output only when all inputs are logic low.**

Ans NOR gate.

7.24 **Name the logic gate with *n* inputs that produces a logic low output only when all inputs are logic high**

Ans NAND gate.

7.25 **Why are NAND and NOR called universal gates?**

Ans Using NAND or NOR, any logic gate function can be realized; hence, they are universal gates.

7.26 **List the advantages of switching function simplification**

Ans Refer page 326.

7.27 **Name a few important Boolean laws.**

Ans Commutative law, Absorption law, Associate law, Distributive law, etc.

7.28 **Give example for each of the above.**

Ans Refer Table 7.14.

7.29 **Briefly explain the important terms associated with *K*-map.**

Ans Refer page 329-330.

7.30 **What is an essential prime implicant (EPI)?**

Ans An EPI is a prime implicant that contains at least one minterm/maxterm that is not covered by any other prime implicant. The prime implicants which describe product terms/sum terms that must be used for all minterm/maxterm to be covered are called EPIs.

7.31 **Broadly classify digital circuits and name one important differences between them.**

Ans Digital circuits may be broadly classified into

(i) Combinational circuits

(ii) Sequential circuits

The major difference between them is that sequential circuits passes memory, but combinational circuits do not.

7.32 **Draw block diagrams to differentiate between combinational and sequential circuits.**

Ans Refer Fig. 7.29.

7.33 **List a few important combinational circuits that are essential building blocks of a digital system.**

Ans Multiplexers, Demultiplexers, Encoders, Decoders, arithmetic circuits, etc.

7.34 **List a few important sequential circuits that are essential building blocks of a digital system**

Ans Latches, Flip-flops, etc.

7.35 **Write the expressions for full adder outputs.**

Ans Refer Eq. (7.26) and Eq. (7.29).

7.36 **How do you convert a parallel adder into a parallel subtractor?**

Ans By adding a 'controlled inverter' for *B* inputs.

7.37 **Name some important flip-flops used in digital system design.**

Ans *SR* flip-flop, *JK* flip-flop, *T* flip-flop, *D* flip-flop, etc.

7.38 **What is 'race-around condition'? Explain**

Ans Refer Fig. 7.37(c), and Case 4 on page 340.

7.39 **List methods to eliminate race-around problem.**

Ans Refer page 340.

7.40 **List at least two uses of *D*-flip-flops.**

Ans (i) Registers—storage of data

(ii) Counters

7.41 **Name the application of *T* flip-flops.**

Ans Counters realization.

7.42 **Name at least two applications of counters.**

Ans (i) Event counting
(ii) Delay generation

7.43 **Classify counters broadly.**

Ans (i) Ripple or asynchronous counters
(ii) Synchronous counters

7.44 **Name at least two applications of shift registers.**

Ans (i) Date storage and shifting
(ii) Conversion of serial data into parallel and vice versa.

7.45 **List a few important applications of shift registers**

Ans (i) Ring counters
(ii) Twisted ring counters
(iii) Pseudo Random Binary Sequence (PRBS) generators
(iv) Sequence generator

Chapter 8: Measuring Instuments

8.1 **Name the important circuit parameters to be measured.**

Ans Voltage, current and power.

8.2 **Name the meters used to measure these qualities**

Ans Voltage—voltmeter
Current—ammeter
Power—wattmeter.

8.3 **Give equations for ac power and dc power in a circuit.**

Ans Eq. (8.1) and Eq. (8.2).

8.4 **List a few popular ammeter/voltmeter types.**

Ans Permanent Magnet Moving Coil (PMMC) meter, moving-iron type, electrostatic type, rectifier type, etc.

8.5 **What type of meter is suitable for dc measurements?**

Ans PMMC meter, electrodynamometer, Digital multi-meter (DMM), etc.

8.6 **What type of meter is suitable for ac measurement**

Ans Induction type, electrodynamometer, DMM, etc.

8.7 **Why is a mirror provided beneath the scale in a PMMC meter?**

Ans To avoid 'parallox' error

8.8 **What is the role of multiplier in a PMMC voltmeter?**

Ans R_s—The series resistance or multiplier is to safeguard the meter and avoid excess current flow.

8.9 **How do you estimate the value of R_s in a PMMC voltmeter?**

Ans Refer Eq. (8.7).

8.10 **How do you estimate the value of R_{sh} in a PMMC ammeter?**

Ans Refer Eq. (8.10).

8.11 **What is the role of R_{sh} in a PMMC ammeter?**

Ans Protecting the meter from excess current flow.

8.12 **How do you measure very small voltage or current in a circuit?**

Ans Using a galvanometer.

8.13 **What is a multimeter?**

Ans An instrument used to measure voltage, current, resistance, both ac and dc quantities.

8.14 **Name the important blocks of a DMM.**

Ans Refer Fig. (8.8).

8.15 **List various parameters that a CRO can measure.**

Ans Voltage, current, frequency, time, phase angle, etc.

8.16 **Name the important blocks of a CRO.**

Ans Refer Fig. (8.10).

8.17 **Name the use of LT and HT supply in CRO.**

Ans LT supply—for filament heating.
HT supply—for focusing and acceleration the electron beam.

8.18 **What is the role of time-base generator is CRO?**

Ans The horizontal (time axis) movement of the signal, i.e. *y*-axis movement of the signal.

8.19 **What is the role of aquadag coating?**

Ans Recollection of unfocussed electrons and aligning them in to beam for re-focusing.

8.20 **Write the equation for displacement of electron beam in a CRO.**

Ans Refer Eq. (8.16).

8.21 **On what parameters does the displacement '*D*' depend?**

Ans Length of deflection plates (l), distance between the screen and deflection plates (L), accelerating voltage (V_a), plates voltage (V_d) and separation between plates (d).

8.22 **Write the equation for deflection sensitivity of a CRO.**

Ans Refer Eq. (8.18).

8.23 **List front panel controls of a CRO.**

Ans Refer Table 8.2.

8.24 **What are lissajous figures?**

Ans The x-y pattern displayed on CRO by comparing an unknown signal with respect to a reference signal.

8.25 **List uses of Lissajous figures.**

Ans (i) Frequency measurement
(ii) Phase measurement
(iii) Time measurement

Chapter 9: Transducers

9.1 **What is a transducer?**

Ans A transducer is a device used to convert one form of energy into another. For example, a loudspeaker-converts electrical energy into sound energy.

9.2 **Name the two basic forms of a transducer.**

Ans Sensor and actuator.

9.3 **Brief the role of a sensor.**

Ans A sensor is used to detect an input signal and report it in another form. For example a Light Dependent Resistor (LDR) detects the intensity of light input and reports it in the form of output current.

9.4 **Brief the role of an actuator.**

Ans An actuator gets actuated by the input and stands responsible for the output action. For example, a loudspeaker uses electrical signal as input and produces the audio sound output.

9.5 **List different sensors and actuators.**

Ans Refer Table 9.1.

9.6 **Classify transducers based on input/output.**

Ans Refer Section 9.2.

9.7 **Classify transducers based on the power source for their operation.**

Ans (i) Active Transducers (ii) Passive transducers

9.8 **Classify transducers based on the generated output signal.**

Ans (i) Analog transducers (ii) Digital transducers.

9.9 **Classify transducers based on the application.**

Ans Refer section 9.2.

9.10 **Estimate capacitance '*C*' for a capacitive transducer.**

Ans Refer Eq. (9.1).

9.11 **Estimate sensitivity '*S*' of a capacitive transducer.**

Ans Refer Eq. (9.2).

9.12 **Estimate inductance '*L*' for inductive transducer.**

Ans Refer Eq. (9.3).

9.13 **Estimate the sensitivity 'S' of a potentiometric transducer.**

Ans Refer Eq. (9.7).

9.14 **What is piezoelectric effect?**

Ans Materials such as quartz (SiO_2) when applied with a mechanical force produce electric field due to the deformation. This phenomenon is known as piezoelectric effect.

9.15 **Name the transducer that converts input light into equivalent resistance.**

Ans Light Dependent Resistor (LDR)

9.16 **Name the transducer that converts input temperature into equivalent resistance.**

Ans Thermistor.

9.17 **Name the transducer that converts input electrical voltage into output light.**

Ans Light Emitting Diode (LED)

9.18 **Establish the relationship between resistance (*R*), temperature (*t*) and temperature co-efficient (α) in a thermistor.**

Ans Refer Eq. (9.10).

9.19 **What do you mean by 'α'-temperature co-efficient of a material?**

Ans Variation of material resistivity (ρ) as a function of temperature variation is called the temperature co-efficient (α) of material.

9.20 **A material is said to have 'passive α'; Explain.**

Ans If the resistivity 'ρ' of the metal increases with the increase in temperature then the metal is said to have positive temperature co-efficient.

9.21 **A metal is said to have 'negative α'; Explain.**

Ans If the resistivity 'ρ' of the metal decreases with the increase in temperature then the metal is said to have negative temperature co-efficient.

Chapter 10: Field Effect Transistors and Other Devices

10.1 **Name one mipolar and one bipolar device.**

Ans (i) unipolar—Field effect transistor (FET)
(ii) Bipolar—Bipolar junction transistor (BJT)

10.2 **Name one current-controlled device and one voltage-controlled device**

Ans (i) Current-controlled device—BJT
(ii) Voltage-controlled device—FET

10.3 **List all popular two-terminal electronic devices you know.**

Ans PN junction diode, zener diod, light-emitting diode, point contact diode, tunnel diode, Schottky diode, Diac etc.

10.4 **List all popular three-terminal electronic devices you know**

Ans Bipolar Junction Transistor (BJT), Junction Field Effect Transistor (JFET), unipolar Junction Transistor (UJT), Metal Oxide Semiconductor Field Effect Transistor (MOSFET), Triac, silicon controlled rectifier (SCR), Light Activated SCR (LASCR), silicon Controlled Switch (SCS), Programmable UJT (PUT), etc.

10.5 **Name some devices that are used for high power applications.**

Ans Diac, Triac, SCR, SCS, etc.

10.6 **Name one/two negative resistance devices.**

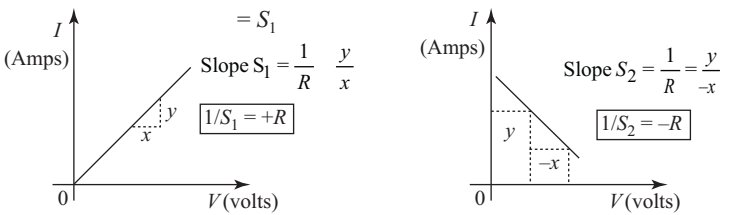
Ans Tunnel diode, unijuction transistor, etc.

10.7 **What is negative resistance property? Explain.**

Ans According to ohms law, device current increases with increase in voltage; but, in certain devices increase in voltage decreases current. This results in negative slope for *V-I* curve and is called negative resistance of the device.

10.8 **Graphically contradict conventional and negative resistance of devices.**

Ans Figure Q10.8 indicates positive *R* and negative *R*.



(a) Convention *R* (b) Negative *R*

Fig. Q10.8 Positive and negative resistances

10.9 **Name one application of negative resistance.**

Ans Negative resistance property is exploited in negative resistance oscillators.

10.10 **What specialty do you observe in a negative resistance oscillator?**

Ans A negative resistance oscillator uses no feedback, but a negative resistance device.

10.11 **Draw the circuit symbols for FET.**

Ans Refer Fig. [10.1(c)].

10.12 **Draw the *VI* curve for FET and mark salient features.**

Ans Refer Fig. 10.3.

10.13 **Write drain current equation for JFET.**

Ans Eq. (10.1).

10.14 **List important FET parameters**

Ans Refer Section 10.2.1.

10.15 **Draw the drain characteristics for an FET.**

Ans Refer Fig. [10.4(a)].

10.16 **Draw the mutual characteristics for a FET.**

Ans Refer Fig. 10.4(b).

10.17 **Name the current equation for JFET in the saturation region.**

Ans Shockley's current equation (Eq. 10.1)

10.18 **Define drain resistance for a JFET.**

Ans Drain resistance (r_d) is the ratio of change in the drain-source voltage (V_{DS}) to corresponding change in drain current (I_D) at a given gate-source voltage (V_{GS}). It is expressed in ohms (Ω).

$$r_d = \left.\frac{\Delta V_{GS}}{\Delta I_D}\right|_{V_{GS}} \Omega$$

10.19 **Define mutual conductance for a JFET.**

Ans Mutual conductance (g_m) for JFET is defined as the ratio of change in drain current (ΔI_D) to a corresponding change in gate-source voltage (ΔV_{GS}) at a given drain-source voltage. It is expressed in mhos (Ω)

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}} \text{℧}.$$

10.20 **Define amplification factor for a JFET.**

Ans Amplification factor (μ) for a JFET is defined as the ratio of change in drain-source voltage (V_{DS}) to the corresponding change in gate-source voltage (V_{GS}).

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = r_d \times g_m}$$

10.21 **What is the physical significance of μ?**

Ans Amplification factor 'μ' for a JFET signifies the ac amplification capability.

10.22 **For a JFET, the gate-source voltage at which device channel completely seizes is called what?**

Ans Pinch-off voltage (V_P).

10.23 **FET needs biasing. Why?**

Ans To fix-24, the operating point $Q(I_{DQ}, V_{DSQ}, V_{GSQ})$, FET needs biasing.

10.24 **List few popular FET biasing methods.**

Ans Refer Section 10.2.2.

10.25 **Explain the graphical method of obtaining *Q*-point for FET.**

Ans Refer explanation on page 415.

10.26 **Compare FET biasing methods.**

Ans Refer Table 10.2.

10.27 **State whether the following statements are true of false.**
(i) FET is a voltage controlled device.
(ii) BJT is a current controlled device.

Ans Both (i) and (ii) are true.

10.28 **State whether BJT offers high input impedance as compared to FET.**

Ans FET offers very high input impedance compared to a BJT.

10.29 **Why do FET circuit offers high input impedance?**

Ans Input circuit of FET is reverse biased.

10.30 **State whether FET has high noise immunity compared to a BJT.**

Ans FET has high noise immunity than BJT.

10.31 **Name few parameters that characterize FET.**

Ans Transconductance (g_m), drain resistance (r_d) and amplification factor (μ).

10.32 **FET is less noisy compared to BJT; why?**

Ans In FET, charge carriers need not cross junctions (unlike in BJT), hence device is less noisy.

10.33 **What characters make FET suitable for Integrated Circuits (ICs)?**

Ans Smaller size and low power consumption.

10.34 **List a few applications of FET.**

Ans Switch, amplifier, oscillators, dc-to-dc converters, voltage Variable Resistors (VVRs), etc.

10.35 **Name an application where FET is used as VVR.**

Ans FET is used as VVR or voltage dependent resistor (VDR) in automatic gain control (AGC) circuits of a television.

10.36 **Draw the circuit and symbol of depletion MOSFETs.**

Ans Refer Fig. 10.20, Fig. 10.22.

10.37 **Give the commercially available FET number.**

Ans BFW-10, BFW-11, 2N 5457

10.38 **Draw the circuit and symbol of enhancement MOSFETs.**

Ans Refer Fig. 10.24 on page 432.

10.39 **Name commercially available MOSFET.**

Ans 2N 3797, 2N 4351

10.40 **What is a silicon-controlled rectifier?**

Ans A silicon-controlled Rectifier (SCR) is a rectifier with a precise control on the dc output voltage produced, i.e. control on the conduction angle. The device is built with silicon material.

10.41 **How many junctions and layers does SCR have?**

Ans SCR has three junctions (J_1, J_2, J_3) and four layers (*P-N-P-N*).

10.42 **Give the biasing conditions for J_1, J_2 and J_3 of SCR.**

Ans J_1 and J_2—need forward bias
J_2—needs reverse bias

10.43 **Write structure and symbol for SCR.**

Ans Refer Fig. 10.31 (a) and (c) on page 439.

10.44 **Write the two transistor equivalent models for a SCR.**

Ans Refer Fig. 10.31 (b).

10.45 **Draw *VI* characteristics SCR and mark all features.**

Ans Refer Fig. 10.32 (a).

10.46 **Write the anode current expression for SCR.**

Ans Refer Eq. (10.33)

10.47 **List various turn-on methods for SCR.**

Ans Refer SCR turn-on methods on page 440.

10.48 **List different turn-off methods for SCR.**

Ans Refer SCR turn-off methods on page 440.

10.49 **Why is Germanium Controlled Rectifier (GCR) is not possible?**

Ans Refering to anode current, Eq. (10.33); for SCR latching α_1 and α_2 need to be controlled below a value 0.5. This is not a reality in germanium material and hence no GCR.

10.50 **List a few applications of SCR.**

Ans Refer section 10.4.2.

10.51 **Explain latching current (I_1) of SCR.**

Ans When SCR is in forward blocking state (Fig. 10.32), SCR anode current is almost negligible. Further increase in anode-cathode voltage (VAK), SCR starts conduction. The value of anode current when SCR starts conduction from forward blocking state is called 'latching current'.

10.52 **Explain holding current (I_μ) of SCR.**

Ans Once SCR starts conduction, the two transistor analogy fails. In order to stop SCR conduction, V_{AK} is reduced; reducing V_{AK} reduces anode current. The value of anode current below which SCR fails to remain on is called 'holding current'.

10.53 **Draw the structure and symbol of UJT.**

Ans Refer Fig. 10.36.

10.54 **Draw the equivalent circuit of UJT.**

Ans Refer Fig. 10.37 (b).

10.55 **Draw *VI* characteristics of UJT.**

Ans Refer Fig. 10.37 (a).

10.56 **Write the expression for 'η' of UJT.**

Ans Refer Eq. (10.36).

10.57 **List a few applications of UJT.**

Ans Refer page 445.

10.58 **Write the expression for peak voltage for UJT.**

Ans Refer Eq. (10.37)

10.59 **Write the expression for output frequency of a UJT relaxation oscillator.**

Ans Refer Eq. (10.40)

10.60 **Draw schematic symbol and VI characteristics of diac.**

Ans Refer Fig. 10.39.

10.61 **Draw the schematic, symbol and *VI* characteristics of Triac.**

Ans Refer Fig. 10.41

10.62 **What are the other names for a PUT?**

Ans Complementary SCR (CSCR) or Silicon Unilateral Switch (SUS).

10.63 **What do you mean by programmable UJT?**

Ans Here, 'η' for the device is programmable.

Appendix

A

Important Tables

Table A.1 Units and symbols

S. No.	Physical Quantity	SI Unit and Symbol
1	Frequency	hertz, Hz: Cycles per second
2	Force	newton, N: kg m /s^2
3	Energy or Work	joule, J: Nm
4	Power	watt, W: J/s
5	Electric Charge	coulomb, C: A s
6	Electric Potential	volt, V: W/A
7	Capacitance	farad, F: A s/V
8	Inductance	henry, H: V s/A
9	Resistance	ohm, Ω: V/A
10	Conductance	mho or siemens, ℧: A/V
11	Temperature	degree Celsius, °C
12	Temperature	degree Kelvin, K

Table A.2 Constant multipliers

Prefix	Symbol	Multiplier
tera	T	10^{12}
giga	G	10^{9}
mega	M	10^{6}
kilo	k	10^{3}
hecto	h	10^{2}
deca	da	10^{1}
decci	d	10^{-1}
centi	c	10^{-2}
milli	m	10^{-3}
micro	μ	10^{-6}
nano	n	10^{-9}
pico	p	10^{-12}
femto	f	10^{-15}
atto	a	10^{-18}

Table A.3 Constants

Quantity	Value	Equation
Charge of an electron (e)	1.602×10^{-19} C	
Velocity of light (c)	3×10^{8} m/s	
Boltzmann constant (k)	1.38054×10^{-23} J/K (8.62×10^{-5} eV/K)	
Planck's constant (h)	6.625×10^{-34} Js	
Avogadro's number (No)	6.023×10^{26} (kg-mole)$^{-1}$	
Faraday's constant (F)	9.652×10^{26} (kg-mole)$^{-1}$	
Angstrom unit (Å)	10^{-10} m (10^{-4} microns)	
Electron Volt (eV)	1.602×10^{-19} J	
Thermal Voltage (kT)	25.876×10^{-3} V(at 300° K)	$kT = T/11600$
Free space Permittivity (ε_o)	8.854×10^{-12} F/m	$10^7/4\ \Pi\ c^2$ F/m
Free space permeability (μ_o)	1.257×10^{-6} H/m	$4\Pi \times 10^{-7}$ H/m
Centre of gravity (g)	9.81 m/s^2	
Free-space Characteristic Imp (Z_o)	376.7 Ω	$(\mu_o/\varepsilon_o)^{1/2} = 120\Pi\ \Omega$

Table A.4 Properties of silicon, germanium and gallium arsenide

Sl. No.	Property Name	Silicon	Germanium	Gallium Arsenide
1	Atomic Weight	28.08	72.6	144.63
2	Atomic Number	14	32	—
3	Crystal Structure	Diamond	Diamond	Zincblende
4	Dielectric Constant(ε_r)	11.8	16	10.9
5	Forbidden Energy Gap E_G at 300 K(eV)	1.1	0.72	1.32
6	Minority Carriers Life Time(s)	2.5×10^{-3}	10^{-3}	10^{-8}
7	Work Function(V)	4.8	4.4	4.7
8	Melting point(°C)	1420	936	1250
9	Electron Mobility at 300 K μ_n(m ^{2}/Vs)	0.13	0.38	0.85
10	Hole Mobility at 300 K-μ_p (m ^{2}/Vs)	0.05	0.18	0.04

Appendix

B

Important Inventions

Sl. No.	Device	Year	Inventor	Remarks
1	Vacuum-tube diode	1904	J A Fleming	
2	Vacuum-tube triode	1906	Lee De Forest	
3	Tetrode and pentode	1930		
4	Amplification	December 23, 1947	Walter H Brattain and John Bardeen	

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