BASIC ELECTRONICS AND DEVICES

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Preface

Basic Electronics and Devices is designed specifically to cater to the needs of second year students of B.Tech. (Electrical and Electronics Engineering) of JNTU. The book has a perfect blend of focused content and complete coverage. Simple, easy-to-understand and difficult-jargon-free text elucidates the fundamentals of electronics. Several solved examples, circuit diagrams and adequate questions further help students understand and apply the concepts.

The book will also serve the purpose of a text to the engineering students of degree, diploma, AIME and graduate IETE courses and as a useful reference for those preparing for competitive examinations. Additionally, it will meet the pressing needs of interested readers who wish to gain a sound knowledge and understanding of the principles of electronic devices. Practicing engineers will find the content of significant relevance in their day-to-day functioning.

The book contains six chapters. *Chapter 1* gives a Review of Semiconductor Physics, *Chapter 2* is devoted to Junction Diode Characteristics and Special Diodes, *Chapter 3* explains Rectifiers and Regulators, *Chapter 4* deals with Transistors, *Chapter 5* covers Power Semiconductor Devices and Field Effect Transistor, and *Chapter 6* describes Amplifiers and Oscillators.

All the topics have been profusely illustrated with diagrams for better understanding. Equal emphasis has been laid on mathematical derivations as well as their physical interpretations. Illustrative examples are discussed to emphasize the concepts and typical applications. Review questions and Objective-type questions have been given at the end of each chapter with a view to help the readers increase their understanding of the subject and to encourage further reading.

We are highly indebted to the management of our institutions for encouraging us from time to time and providing all the necessary facilities. Thanks are due to our colleagues, especially Mr. S. Karthie, Assistant Professor, Department of ECE, SSNCE, for their valuable suggestions and useful comments in the preparation of the manuscript. Our thanks are also due to Mr. R. Gopalakrishnan, Mr. K. Rajan and Mr. S. Sankar Kumar for efficiently word processing the manuscript.

We are thankful to McGraw Hill Education (India) for stimulating interest in this project and bringing out this book in a short span of time.

Further, we would like to extend the warmest thanks to our family members for their enormous patience and cooperation.

Constructive suggestions and corrections for the improvement of the book would be most welcome and highly appreciated.

S. Salivahanan
N. Suresh Kumar

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JNTU Kakinada

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1 Review of Semiconductor Physics

1.1 INTRODUCTION

Electronics is the branch of science and engineering which relates to the conduction of electricity either through vacuum by electrons or through gases by electrons and ions. Basically, it is a study of electronic devices and their utilisation. An electron device is that in which electrons flow through vacuum or gas or semiconductor. In the beginning of 20th century, electrons began to take technological shape and they have enjoyed an explosive development in the last few decades.

Electronics has a wide range of applications, such as rectification, amplification, power generation, industrial control, photo-electricity, communications and so on. The electronic industry turns out a variety of items in the range of consumer electronics, control and industrial electronics, communication and broadcasting equipment, biomedical equipment, calculators, computers, microprocessors, aerospace and defence equipment and components.

A semiconductor is a material that has a resistivity value in between that of a conductor and an insulator. The conductivity of a semiconductor material can be varied under an external electric field. Devices made from semiconductor materials are the foundation of modern electronics which include radio, computers, telephones, and many other devices. Semiconductor devices include transistor, many kinds of diodes including the light emitting diode, the silicon controlled rectifier, and digital and analog integrated circuits.

This chapter deals with the classification of semiconductors based on energy band diagram. It also discusses the doping in semiconductors, Hall effect and Fermi level in semiconductors.

1.2 INSULATORS, SEMICONDUCTOR AND METAL CLASSIFICATION USING ENERGY BAND DIAGRAMS

A very poor conductor of electricity is called an insulator; an excellent conductor is a metal; and a material whose conductivity lies between these two extremes is a semiconductor. A material may be classified as one of these three depending upon its energy-band structure.

1.2.1 Insulator

An insulator is a material having extremely poor electrical conductivity. The energy-band structure at the normal lattice spacing is indicated schematically in Fig. 1.1(a). The forbidden energy gap is large; for diamond, the energy gap is about 6 eV. If additional energy is given to an electron in the upper level

of valence band, this electron attempts to cross the forbidden energy gap and enter the conduction band. However, in an insulator, the additional energy which may ordinarily be given to an electron is, in general, much smaller than this high value of forbidden energy gap. Hence, no electrical conduction is possible. The number of free electrons in an insulator is very small, roughly about 10^7 electrons/m^3.

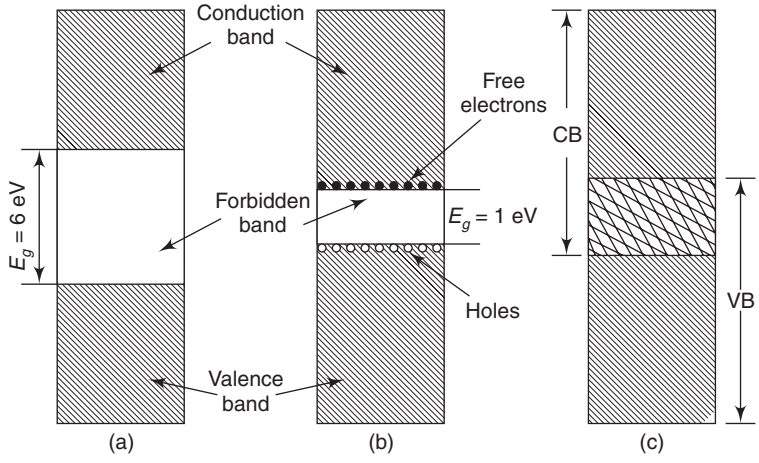


Fig. 1.1 *Energy-band gap in (a) insulators, (b) semiconductors, and (c) metals*

1.2.2 Metal

Conduction in metals is only due to the electrons. A metal has overlapping valence and conduction bands. The valence band is only partially filled and the conduction band extends beyond the upper end of filled valence band. The outer electrons of an atom are as much associated with one ion as with another, so that the electron attachment to any individual atom is almost zero. The band occupied by the valence electrons may not be completely filled and that there are no forbidden levels at higher energies. Depending upon the metal, at least one, and sometimes two or three, electrons per atom are free to move throughout the interior of the metal under the action of applied fields. When an electric field is applied, few electrons may acquire enough additional energy and move to higher energy levels within the conduction band. Thus, the electrons become mobile. Since the additional energy required for transfer of electrons from valence band to conduction band is extremely small, the conductivity of a metal is excellent.

In *electron-gas theory* description of a metal, the metal is visualized as a region containing a periodic three-dimensional array of heavy, tightly bound ions permeated with a swarm of electrons that may move about quite freely. According to this theory, the electrons in a metal are continuously moving and the direction of motion changes whenever the electron collides with other electrons. The average distance travelled by an electron between successive collisions is called *mean-free-path* of an electron. In the absence of any applied potential, the average current in a metal is zero because the number of electrons passing through unit area in any direction is almost same as the number of electrons passing through the same unit area in the opposite direction. This can be attributed to the random nature of motion of electrons.

When a constant electric field E (volt per metre) is applied to a metal, the electrons would be accelerated and its velocity would increase indefinitely with time. However, because of collision of electrons, electrons lose energy and a steady-state condition is reached where a finite value of drift velocity v_d is attained. The drift velocity, v_d is in the direction opposite to that of the electric field and its magnitude is proportional to E. Thus,

$$v_d = \mu E \tag{1.1}$$

where μ = mobility of the electron, m^2/volt-second. Due to the applied field, a steady-state drift velocity has been superimposed upon the random thermal motion of the electrons. Such a directed flow of electrons constitutes a current. If the concentration of free electrons is n (electrons per cubic meter), the current density J (ampere per square metre) is

$$J = nqv_d = nq\mu E = \sigma E \tag{1.2}$$

where
$$\sigma = nq\mu \tag{1.3}$$

σ is the *conductivity* of the metal in (ohm-metre)$^{-1}$. For a good conductor, n is very large, approximately, 10^{28} electrons/m^3. Equation (1.2) can be recognized as Ohm's law which states that the conduction current density is proportional to the applied electric field. The energy acquired by the electrons from the applied field is given to the lattice ions as a result of collisions. Hence, power is dissipated within the metal by the electrons, and the power density (joule heat) is given by

$$JE = \sigma E^2 \text{ watt/metre}^3 \tag{1.4}$$

1.3 CLASSIFICATION OF SEMICONDUCTORS

Semiconductors are classified as (i) intrinsic (pure), and (ii) extrinsic (impure) types. The extrinsic semiconductors are of *N*-type and *P*-type.

➤ ***Intrinsic Semiconductor*** A pure semiconductor is called an intrinsic semiconductor. As already explained in the first chapter, even at room temperature, some of the valence electrons may acquire sufficient energy to enter the conduction band to form free electrons. Under the influence of an electric field, these electrons constitute electric current. A missing electron in the valence band leaves a vacant space, which is known as *hole*, as shown in Fig. 1.2. Holes also contribute to electric current.

In an intrinsic semiconductor, even at room temperature, electron-hole pairs are created. When an electric field is applied across an intrinsic semiconductor, the current conduction takes place due to free electrons and holes. Under the influence of an electric field, the total current through the semiconductor is the sum of currents due to free electrons and holes.

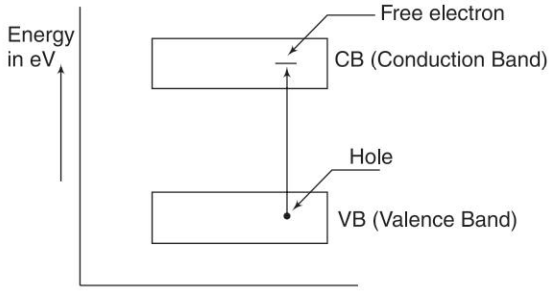


Fig. 1.2 *Creation of electron-hole pair in a semiconductor*

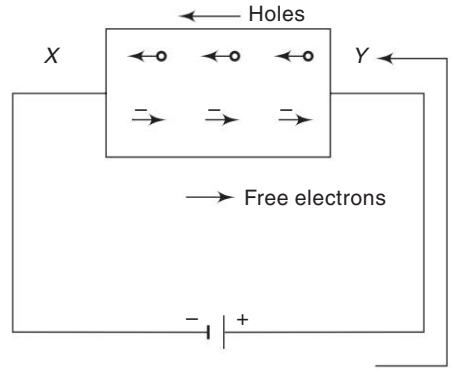


Fig. 1.3 *Current conduction in semiconductor*

Though the total current inside the semiconductor is due to free electrons and holes, the current in the external wire is only by electrons. In Fig. 1.3, holes being positively charged move towards the negative terminal of the battery.

As the holes reach the negative terminal of the battery, electrons enter the semiconductor near the terminal (X) and combine with the holes. At the same time, the loosely held electrons near the positive terminal (Y) are attracted towards the positive terminal. This creates new holes near the positive terminal which again drift towards the negative terminal.

➤ ***Extrinsic Semiconductor*** Due to the poor conduction at room temperature, the intrinsic semiconductor as such, is not useful in the electronic devices. Hence, the current conduction capability of the intrinsic semiconductor should be increased. This can be achieved by adding a small amount of impurity to the intrinsic semiconductor, so that it becomes impure or extrinsic semiconductor. This process of adding impurity is known as *doping*.

The amount of impurity added is extremely small, say 1 to 2 atoms of impurity in 10^6 intrinsic atoms.

➤ ***N-type Semiconductor*** A small amount of pentavalent impurity such as arsenic, antimony, or phosphorus is added to the pure semiconductor (germanium or silicon crystal) to get an *N*-type semiconductor.

The germanium atom has four valence electrons and antimony has five valence electrons. As shown in Fig. 1.4, each antimony atom forms a covalent bond with surrounding four germanium atoms. Thus, four valence electrons of the antimony atom form a covalent bond with four valence electrons of an individual germanium atom and the fifth valence electron is left free which is loosely bound to the antimony atom.

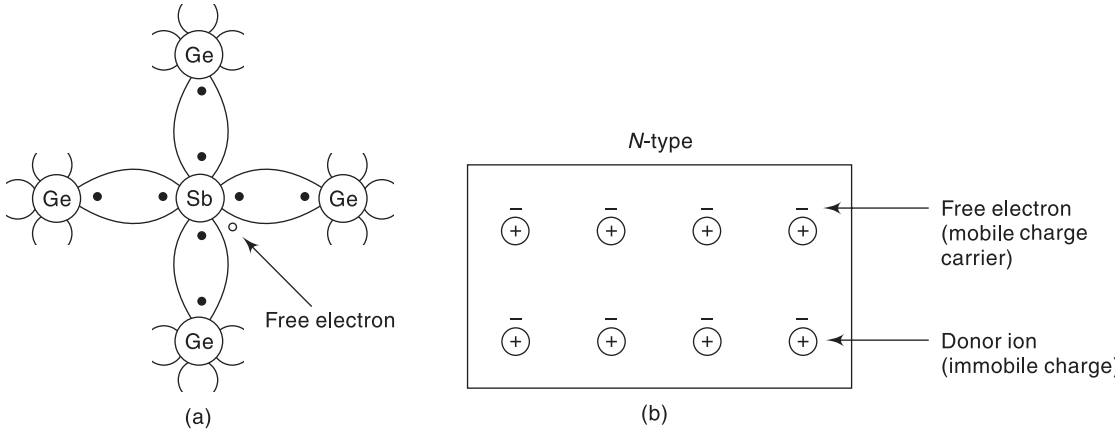


Fig. 1.4 *N-type semiconductor: (a) Formation of covalent bonds (b) Charged carriers*

This loosely bound electron can be easily excited from the valence band to the conduction band by the application of electric field or increasing the thermal energy. Thus, every antimony atom contributes one conduction electron without creating a hole. Such a pentavalent impurity is called a donor impurity because it donates one electron for conduction. On giving an electron for conduction, the donor atom becomes a positively charged ion because it loses one electron. But it cannot take part in conduction because it is firmly fixed in the crystal lattice.

Thus, the addition of a pentavalent impurity (antimony) increases the number of electrons in the conduction band, thereby increasing the conductivity of an *N*-type semiconductor. As a result of doping, the number of free electrons far exceeds the number of holes in an *N*-type semiconductor. So electrons are called majority carriers and holes are called minority carriers.

➤ ***P-type Semiconductor*** A small amount of trivalent impurity such as aluminium or boron is added to the pure semiconductor to get the *P*-type semiconductor. The germanium (Ge) atom has four valence electrons and boron has three valence electrons as shown in Fig. 1.5. Three valence electrons in boron form a covalent bond with four surrounding atoms of Ge leaving one bond incomplete which gives rise to a hole. Thus, the trivalent impurity (boron) when added to the intrinsic semiconductor (germanium) introduces a large number of holes in the valence band. These positively charged holes increase the conductivity of the *P*-type semiconductor. A trivalent impurity such as boron is called *acceptor impurity* because it accepts free electrons in the place of holes. As each boron atom donates a hole for conduction, it becomes a negatively charged ion. As the number of holes is very much greater than the number of free electrons in a *P*-type material, holes are termed *majority carriers* and electrons *minority carriers*.

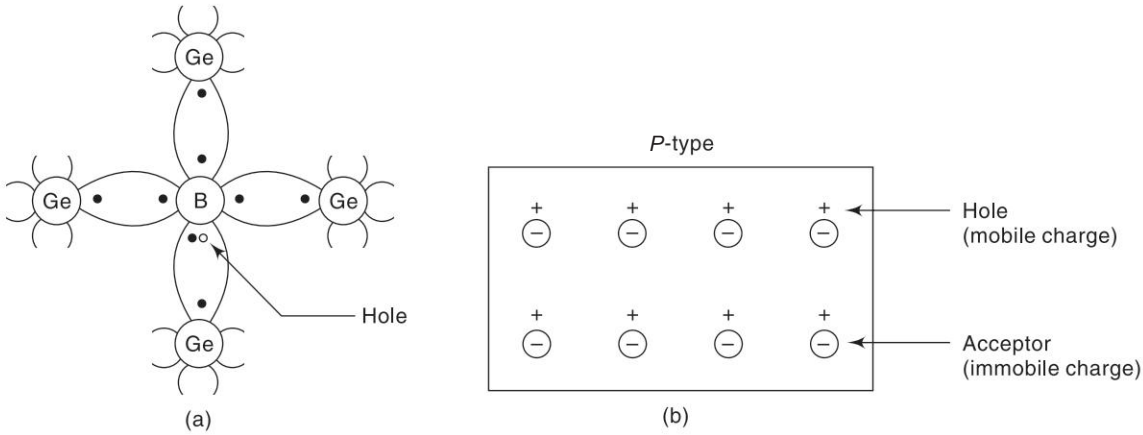


Fig. 1.5 *P-type semiconductor: (a) Formation of covalent bonds (b) Charged carriers*

1.4 MOBILITY AND CONDUCTIVITY

The conductivity of a material is proportional to the concentration of free electrons. The number of free electrons in a semiconductor lies between 10^7 and 10^{28} electrons/m^3. Thus, a semiconductor has conductivity much greater than that of an insulator but much smaller than that of a metal. Typically, a semiconductor has a forbidden energy gap of about 1 eV. The most important practical semiconductor materials are germanium and silicon, which have values of E_g of 0.785 and 1.21 eV, respectively, at 0 degree Kelvin. Energies of this magnitude normally cannot be acquired from an applied field. At low temperatures the valence band remains full, the conduction band empty, and these materials are insulators at low temperatures. The conductivity of these materials increases with temperature and hence, these materials are called as intrinsic semiconductors. As the temperature is increased, some of the electrons in the valence band acquire thermal energy greater than the gap energy and move into the conduction band. These electrons are now free to move about under the influence of even a small applied field. These free electrons, also called *conduction*

electrons, constitute for conduction and the material becomes slightly conducting. The current density due to the motion of electrons is given by

$$J_n = n\mu_n qE = \sigma_n E \tag{1.5}$$

where, μ_n is the electron mobility, and the suffix 'n' represents that the respective terms are due to motion of electrons. The absence of an electron in the valence band is represented by a small circle and is called a hole. The hole may serve as a carrier of electricity whose effectiveness is comparable with the free electron. The hole conduction current density is given by

$$J_p = p\mu_p qE = \sigma_p E \tag{1.6}$$

where μ_p is the hole mobility and p is the hole concentration.

Hence, the total current density J in a semiconductor is given by

$$J = (n\mu_n + p\mu_p)qE = \sigma E \tag{1.7}$$

where $\sigma = (n\mu_n + p\mu_p)q$ is the total conductivity of a semiconductor. For a pure semiconductor (intrinsic semiconductor), the number of free electrons is exactly same as the number of holes. Thus, the total current density is

$$J = n_i(\mu_n + \mu_p)\, qE \tag{1.8}$$

where $n_i = n = p$ is the intrinsic concentration of a semiconductor.

The conductivity of an intrinsic semiconductor can be increased by introducing certain impurity atoms into the crystal. This results in allowable energy states which lie in the forbidden energy gap and these impurity levels also contribute to the conduction. Such a semiconductor material is called an extrinsic semiconductor.

➤ ***Effective Mass*** An electron travelling through a crystal under the influence of an externally applied field hardly notices the electrostatic field of the ions making up the lattice, i.e., it behaves as if the applied field were the only one present. This is the basis of the electron-gas approximation and the assumption will now be looked at a little more closely. If the electrons were to experience only the applied field, E, then immediately after a collision it would accelerate in the direction of the field with an acceleration a, proportional to the applied force, i.e.,

$$qE = ma \tag{1.9}$$

where the constant of proportionality is the electron mass, m. When quantum theory is applied to the problem of an electron moving through a crystal lattice, it predicts that under the action of an applied field, the electron acceleration will indeed be proportional to the field, but that the constant of proportionality will be different from the normal mass of an electron:

$$qE = m_n a \tag{1.10}$$

The field due to the lattice ions can, therefore, be ignored providing we treat the electrons inside the crystal as if they had a slightly different mass to the real electron mass or, to put it another way, the effect of the lattice ions on an electron is to make it behave as if it had a different mass. This new mass is called the effective mass of the electron, m_n, and the effective mass of a hole, m_p, can be similarly defined. In general, m_n and m_p are not the same. Usually, m_n is of the same order as m; in germanium, for instance, $m_n = 0.2$ m and in silicon, $m_n = 0.4$ m.

The value of effective mass is an important parameter for any semiconductor, especially from the device point of view. Certain semiconductors, for instance, have low electron effective mass and hence, high electron mobility. This makes them very suitable for high-frequency devices. The III-V semiconductor GaAs comes into this category and some of the best microwave transistors are made from this material.

In a pure semiconductor, the number of holes is equal to the number of electrons. Thermal agitation continues to produce new electron-hole pairs and the electron-hole pair disappears because of recombination. With each electron-hole pair created, two charge-carrying particles are formed. One is negative which is the free electron with mobility μ_n. The other is positive, i.e., the hole with mobility μ_p. The electrons and holes move in opposite directions in an electric field E, but since they are of opposite sign, the current due to each is in the same direction. Hence, the total current density J within the intrinsic semiconductor is given by

$$\begin{aligned} J &= J_n + J_p \\ &= qn\,\mu_n E + qp\,\mu_p E \\ &= (n\mu_n + p\mu_p)qE \\ &= \sigma E \end{aligned} \tag{1.11}$$

where J_n = electron-drift current density
J_p = hole-drift current density
n = number of electrons per unit volume, i.e., magnitude of free-electron (negative) concentration
p = number of holes per unit volume, i.e., magnitude of hole (positive) concentration
E = applied electric field strength, V/m
q = charge of electron or hole, coulomb

Hence, σ is the conductivity of a semiconductor which is equal to $(n\,\mu_n + p\,\mu_p)q$. The resistivity (ρ) of a semiconductor is the reciprocal of conductivity, i.e., $\rho = \dfrac{1}{\sigma}$.

It is evident from the above equation that current density within a semiconductor is directly proportional to the applied electric field.

For a pure (intrinsic) semiconductor, $n = p = n_i$, where n_i is the intrinsic carrier concentration.

Therefore, $J = n_i\,(\mu_n + \mu_p)\,qE$

and conductivity of an intrinsic semiconductor is $\sigma_i = qn_i(\mu_n + \mu_p)$. Hence, it is clear that conductivity of an intrinsic semiconductor depends upon its intrinsic concentration (n_i) and the mobility of electrons (μ_n) and holes (μ_p). The intrinsic conductivity of germanium and silicon increase by approximately 5 percent per °C and 7 percent per °C rise in temperature respectively due to the influence of n_i.

➤ ***Conductivities of N- and P-type Semiconductors*** The conductivity of an intrinsic semiconductor,

$$\sigma_i = q \cdot n_i(\mu_n + \mu_p) = q \cdot (n\,\mu_n + p\mu_p) \tag{1.12}$$

For an N-type semiconductor, as $n>>p$, then the conductivity, $\sigma = q \cdot n \cdot \mu_n$.

For a P-type semiconductor, as $p>>n$, the conductivity, $\sigma = q \cdot p \cdot \mu_p$.

EXAMPLE 1.1

The mobility of free electrons and holes in pure germanium are 3,800 and 1,800 cm^2 /V-s, respectively. The corresponding values for pure silicon are 1,300 and 500 cm^2/V-s, respectively. Determine the values of intrinsic conductivity for both germanium and silicon. Assume $n_i = 2.5 \times 10^{13}$ cm^{-3} for germanium and $n_i = 1.5 \times 10^{10}$ cm^{-3} for silicon at room temperature.

Solution

The intrinsic conductivity for germanium,

$$\sigma_i = qn_i(\mu_n + \mu_p)$$
$$= (1.602 \times 10^{-19})\ (2.5 \times 10^{13})\ (3800 + 1800)$$
$$= 0.0224 \text{ S/cm}$$

The intrinsic conductivity for silicon,

$$\sigma_i = qn_i\ (\mu_n + \mu_p)$$
$$= (1.602 \times 10^{-19})\ (1.5 \times 10^{10})\ (1300 + 500)$$
$$= 4.32 \times 10^{-6} \text{ S/cm}$$

1.5 DRIFT AND DIFFUSION CURRENTS

The flow of charge, i.e., current, through a semiconductor material is of two types, namely, drift and diffusion. The net current that flows through a *PN* junction diode also has two components, viz., (i) drift current, and (ii) diffusion current.

➤ ***Drift Current*** When an electric field is applied across the semiconductor material, the charge carriers attain a certain drift velocity v_d, which is equal to the product of the mobility of the charge carriers and the applied electric field intensity, E. The holes move towards the negative terminal of the battery and electrons move towards the positive terminal. This combined effect of movement of the charge carriers constitutes a current known as *drift current*. Thus, drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field.

▪ **Drift current density** Figure 1.6 shows that a conducting wire of length l cm contains N electrons. If an electron travels a distance of l cm in the conductor in time T sec, the total number of electrons passing through any cross section of wire per second is $\frac{N}{T}$.

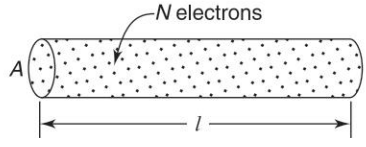


Fig. 1.6 *Conducting wire to determine drift current density*

The total current flowing through the wire with area of cross-section A is given by

$$I = \frac{Nq}{T} = \frac{Nqv_d}{l}$$

where v_d is the drift velocity and time $T = \frac{l}{v_d}$. The drift current density J is defined as the current per unit area of the conducting medium.

i.e., $$J = \frac{I}{A} = \frac{Nqv_d}{lA} \text{ A/cm}^2$$

Here, lA is the volume containing N electrons and the electron concentration, $n = \frac{N}{lA}$.

Therefore, $$J = nqv_d = \rho v_d$$

where $\rho = nq$ is the charge density, in coulomb per cubic centimeter. Generally, the above current density can also be written as

$$J = nqv_d = nq\mu E = \sigma E$$

where E is the applied electric field intensity in V/cm, μ is the mobility of electrons in cm^2/V-s, the drift velocity, $v_d = \mu E$ in cm/s, and the conductivity, $\sigma = nq\mu$ in $\text{S} \cdot \text{m}^{-1}$. The equation $J = \sigma E$ is also called Ohm's law.

The drift current density due to the charge carriers such as free electrons and holes are the current passing through a square centimeter perpendicular to the direction of flow. The equation for the drift current density, J_n, due to free electrons is given by

$$J_n = qn\mu_n E \quad \text{A/cm}^2$$

and the drift current density, J_p, due to holes is given by

$$J_p = qp\mu_p E \quad \text{A/cm}^2$$

where n = number of free electrons per cubic centimetre
p = number of holes per cubic centimetre
μ_n = mobility of electrons in cm^2/V-s
μ_p = mobility of holes in cm^2/V-s
E = applied electric field intensity in V/cm
q = charge of an electron = 1.602×10^{-19} coulomb

➤ ***Diffusion Current*** It is possible for an electric current to flow in a semiconductor even in the absence of the applied voltage, provided a concentration gradient exists in the material. A concentration gradient exists if the number of either electrons or holes is greater in one region of a semiconductor as compared to the rest of the region. In a semiconductor material, the charge carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers. Thus, the movement of charge carriers takes place resulting in a current called *diffusion current*. The diffusion current depends on the material of the semiconductor, type of charge carriers, and the concentration gradient.

As indicated in Fig. 1.7(a), the hole concentration $p(x)$ in a semiconductor bar varies from a high value to a low value along the x-axis and is constant in the y- and z-directions.

Diffusion current density due to holes, J_p, is given by

$$J_p = -qD_p \frac{dp}{dx} \text{ A/cm}^2 \tag{1.13}$$

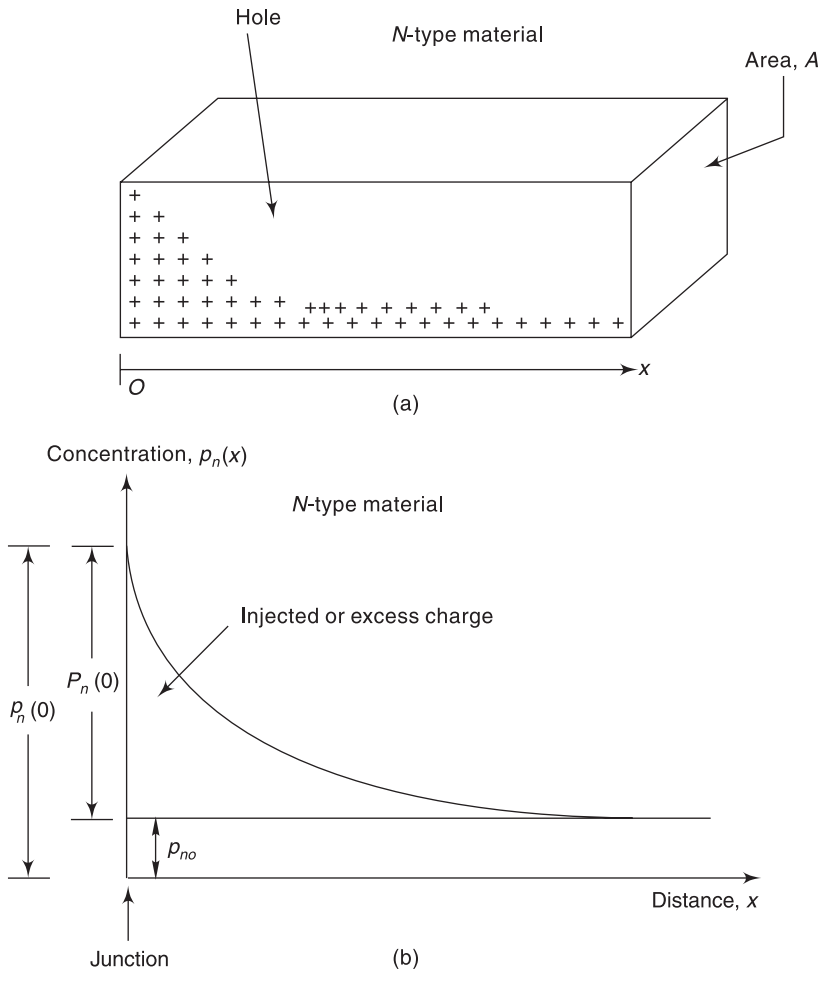


Fig. 1.7 *(a) Excess hole concentration varying along the axis in an N-type semiconductor bar (b) The resulting diffusion current*

Since the hole density $p(x)$ decreases with increasing x as shown in Fig. 1.7(b), dp/dx is negative and the minus sign in the above equation is needed in order that J_p has a positive sign in the positive x-direction.

Diffusion current density due to the free electrons, J_n, is given by

$$J_n = qD_n \frac{dn}{dx} \text{ A/cm}^2$$

where dn/dx and dp/dx are the concentration gradients for electrons and holes respectively, in the x-direction, and D_n and D_p are the diffusion coefficients expressed in cm^2/s for electrons and holes, respectively.

➤ ***Total Current*** The total current in a semiconductor is the sum of drift current and diffusion current. Therefore, for a *P*-type semiconductor, the total current per unit area, i.e., the total current density is given by

$$J_p = qp\mu_p E - qD_p \frac{dp}{dx}$$

Similarly, the total current density for an *N*-type semiconductor is given by

$$J_n = qn\mu_n E + qD_n \frac{dn}{dx}$$

Einstein Relationship for a Semiconductor

There exists a definite relationship between the mobility and diffusion coefficient of a particular type of charge carrier in the same semiconductor. The higher the value of mobility of a charge carrier, the greater will be its tendency to diffuse. The equation which relates the mobility μ and the diffusion coefficient D is known as the *Einstein relationship*. The Einstein relationship is expressed as

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{kT}{q} = V_T \tag{1.14}$$

The importance of the Einstein relationship is that it can be used to determine D_p (or D_n), if the mobility of holes (or electrons) is measured experimentally. For an intrinsic silicon, $D_p = 13$ cm^2/s and $D_n = 34$ cm^2/s. For an intrinsic germanium, $D_p = 47$ cm^2/s and $D_n = 99$ cm^2/s.

➤ ***Diffusion Length (L)*** As shown in Fig. 1.6, the excess hole or electron densities fall off exponentially with distance as a result of the recombination of these excess minority carriers with the majority carriers of the semiconductor. Here, the excess charge carriers have a finite lifetime, τ, before they are totally destroyed by recombination. The average distance that an excess charge carrier can diffuse during its lifetime is called the diffusion length L, which is given by

$$L = \sqrt{D\tau}$$

where D is the diffusion coefficient that may be related to the drift mobility, μ, through the Einstein relation as

$$D = \mu \frac{kT}{q}$$

If the transverse length of the semiconductor is greater than the diffusion length L then the terminal currents are the recombination currents arising out of the recombination, as every electron lost by recombination is supplanted by the terminal electrode to maintain the charge neutrality.

1.6 GENERATION AND RECOMBINATION OF CHARGES

If a pure semiconductor is doped with *N*-type impurities, the number of electrons in the conduction band increases above a level and the number of holes in the valence band decreases below a level, which would be available in the intrinsic (pure) semiconductor. Similarly, the addition of *P*-type impurities to a pure semiconductor increases the number of holes in the valence band above a level and decreases the number of electrons in the conduction band below a level, which would have been available in the intrinsic semiconductor. This is because the rate of recombination increases due to the presence of large number of free electrons (or holes).

Further, the experimental results state that under thermal equilibrium for any semiconductor, the product of the number of holes and the number of electrons is constant and is independent of the amount of donor and acceptor impurity doping. This relation is known as *mass-action law* and is given by

$$n \cdot p = n_i^2 \tag{1.15}$$

where n is the number of free electrons per unit volume, p is the number of holes per unit volume, and n_i is the intrinsic concentration.

While considering the conductivity of the doped semiconductors, only the dominant majority charge carriers have to be considered.

➤ ***Charge Densities in N-type and P-type Semiconductors*** The law of mass-action provides the relationship between free-electron concentration and hole concentration. These concentrations are further related by the *law of electrical neutrality* as given below.

Let N_D be the concentration of donor atoms in an N-type semiconductor. In order to maintain the electric neutrality of the crystal, we have

$$\begin{aligned} n_N &= N_D + p_N \\ &\approx N_D \end{aligned}$$

where n_N and p_N are the electron and hole concentrations in the N-type semiconductor. The value of p_N is obtained from the relations of mass-action law as

$$\begin{aligned} p_N &= \frac{n_i^2}{n_N} \\ &\approx \frac{n_i^2}{N_D}, \text{ which is} \ll n_N \quad \text{or} \quad N_D \end{aligned}$$

Similarly, in a P-type semiconductor, we have

$$\begin{aligned} p_P &= N_A + n_P \\ &\approx N_A \end{aligned}$$

where N_A, p_P, and n_P are the concentrations of acceptor impurities, holes, and electrons respectively in a P-type semiconductor.

From the mass-action law, $n_P = \dfrac{n_i^2}{p_P}$

Therefore, $n_P = \dfrac{n_i^2}{N_A}$, which is $<< p_P$ or N_A

➤ ***Extrinsic Conductivity*** The conductivity of an N-type semiconductor is given by

$$\sigma_N = q n_N \mu_n \approx q N_D \mu_n, \text{ since } n_N \approx N_D$$

The conductivity of a P-type semiconductor is given by

$$\sigma_P = q p_P \mu_P \approx q N_A \mu_P, \text{ since } p_P \approx N_A$$

The doping of intrinsic semiconductor considerably increases its conductivity.

If the concentration of donor atoms added to a P-type semiconductor exceeds the concentration of acceptor

atoms, i.e., $N_D >> N_A$, then the semiconductor is converted from *P*-type to *N*-type. Similarly, a large number of acceptor atoms added to an *N*-type semiconductor can convert it to a *P*-type semiconductor if $N_A >> N_D$. This concept is precisely used in the fabrication of a *PN* junction, which is an essential part of semiconductor devices and integrated circuits.

EXAMPLE 1.2

Consider a silicon *PN* junction at $T = 300$ K so that $n_i = 1.5 \times 10^{10}$ cm^{-3}. The *N* type doping is 1×10^{10} cm^{-3} and a forward bias of 0.6 V is applied to the *PN* junction. Calculate the minority hole concentration at the edge of the space charge region.

Solution Given $T = 300$ K, $n_i = 1.5 \times 10^{10}$ cm^{-3}, $n = 1 \times 10^{10}$ cm^{-3} and $V_F = 0.6$ V

From mass action law,

$$n \cdot p = n_i^2$$

Therefore, the concentration of holes is

$$p = \frac{n_i^2}{n} = \frac{(1.5 \times 10^{10})^2}{1 \times 10^{10}} = 2.25 \times 10^{10} \text{ cm}^{-3}$$

EXAMPLE 1.3

Find the conductivity of silicon (a) in intrinsic condition at a room temperature of 300 K, (b) with donor impurity of 1 in 10^8, (c) with acceptor impurity of 1 in 5×10^7, and (d) with both the above impurities present simultaneously. Given that n_i for silicon at 300 K is 1.5×10^{10} cm^{-3}, $\mu_n = 1300$ cm^2/V-s, $\mu_p = 500$ cm^2/V-s, number of Si atoms per cm^3 $= 5 \times 10^{22}$.

Solution

(a) In intrinsic condition, $n = p = n_i$

Hence, $$\sigma_i = qn_i (\mu_n + \mu_p)$$
$$= (1.602 \times 10^{-19}) (1.5 \times 10^{10}) (1300 + 500)$$
$$= 4.32 \times 10^{-6} \text{ S/cm}$$

(b) Number of silicon atoms/cm^3 $= 5 \times 10^{22}$

Hence, $$N_D = \frac{5 \times 10^{22}}{10^8} = 5 \times 10^{14} \text{ cm}^{-3}$$

Further, $$n \approx N_D$$

Therefore, $$p = \frac{n_i^2}{n} \approx \frac{n_i^2}{N_D} = \frac{(1.5 \times 10^{10})^2}{5 \times 10^{14}} = 0.46 \times 10^6 \text{ cm}^{-3}$$

Thus, $p << n$. Hence, p may be neglected while calculating the conductivity.

Hence, $$\sigma = nq\mu_n = N_D q \mu_n$$
$$= (5 \times 10^{14}) (1.602 \times 10^{-19}) (1300) = 0.104 \text{ S/cm}.$$

(c) $$N_A = \frac{5 \times 10^{22}}{5 \times 10^7} = 10^{15} \text{ cm}^{-3}$$

Further, $p \approx N_A$

Hence, $$n = \frac{n_i^2}{p} \approx \frac{n_i^2}{N_A} = \frac{(1.5 \times 10^{10})^2}{10^{15}} = 2.25 \times 10^5 \text{ cm}^{-3}$$

Thus, $p >> n$. Hence, n may be neglected while calculating the conductivity.

Hence, $\sigma = pq\mu_P = N_A q\mu_P$

$= (10^{15} \times 1.602 \times 10^{-19} \times 500) = 0.08$ S/cm.

(d) With both types of impurities present simultaneously, the net acceptor impurity density is,

$$N_A' = N_A - N_D = 10^{15} - 5 \times 10^{14} = 5 \times 10^{14} \text{ cm}^{-3}$$

Hence, $\sigma = N_A' \, q\mu_p$

$= (5 \times 10^{14})\ (1.602 \times 10^{-19})\ (500) = 0.04$ S/cm.

EXAMPLE 1.4

Determine the resistivity of germanium (a) in intrinsic condition at 300 K, (b) with donor impurity of 1 in 10^7, (c) with acceptor impurity of 1 in 10^8, and (d) with both the above impurities simultaneously. Given that for germanium at room temperature, $n_i = 2.5 \times 10^{13}/\text{cm}^3$, $\mu_n = 3{,}800$ cm^2/V-Vs, $\mu_p = 1{,}800$ cm^2/V-Vs, and number of germanium atoms/cm^3 $= 4.4 \times 10^{22}$.

Solution

(a) $$n = p = n_i = 2.5 \times 10^{13} \text{ cm}^{-3}$$

Therefore, conductivity, $\sigma = qn_i(\mu_n + \mu_p)$

$= (1.602 \times 10^{-19})(2.5 \times 10^{13})(3800 + 1800)$

$= 0.0224$ S/cm

Hence, resistivity, $$\rho = \frac{1}{\sigma} = \frac{1}{0.02254} = 44.64 \ \Omega\text{-cm}$$

(b) $$N_D = \frac{4.4 \times 10^{22}}{10^7} = 4.4 \times 10^{15} \text{ cm}^{-3}$$

Also, $n = N_D$

Therefore, $$p = \frac{n_i^2}{n} = \frac{n_i^2}{N_D} = \frac{(2.5 \times 10^{13})^2}{4.4 \times 10^{15}} = 1.42 \times 10^{11} \text{ holes/cm}^3$$

Here, as $n >> p$, p can be neglected.

Therefore, conductivity, $\sigma = nq\mu_n = N_D q\mu_n$

$= (4.4 \times 10^{15})\ (1.602 \times 10^{-19})\ (3800) = 2.675$ S/cm

Hence, resistivity, $$\rho = \frac{1}{\sigma} = \frac{1}{2.675} = 0.374 \ \Omega\text{-cm}$$

(c) $$N_A = \frac{4.4 \times 10^{22}}{10^8} = 4.4 \times 10^{14} \text{ cm}^{-3}$$

Also, $$p = N_A$$

Therefore, $$n = \frac{n_i^2}{p} = \frac{n_i^2}{N_A} = \frac{(2.5 \times 10^{13})^2}{4.4 \times 10^{14}} = 1.42 \times 10^{12} \text{ electron/cm}^3$$

Here, as $p >> n$, n may be neglected. Then

Conductivity, $$\sigma = pq\mu_p = N_A q \mu_p$$
$$= (4.4 \times 10^{14})\ (1.602 \times 10^{-19})\ (1800) = 0.1267 \text{ S/cm}$$

Hence, resistivity, $$\rho = \frac{1}{\sigma} = \frac{1}{0.1267} = 7.89\ \Omega\text{-cm}$$

(d) With both *P*- and *N*-type impurities present,

$$N_D = 4.4 \times 10^{15} \text{ cm}^{-3} \text{ and } N_A = 4.4 \times 10^{14} \text{ cm}^{-3}$$

Therefore, the net donor density N_D' is

$$N_D' = (N_D - N_A) = (4.4 \times 10^{15} - 4.4 \times 10^{14}) = 3.96 \times 10^{15} \text{ cm}^{-3}$$

Therefore, effective $n = N_D' = 3.96 \times 10^{15} \text{ cm}^{-3}$

$$p = \frac{n_i^2}{N_D'} = \frac{(2.5 \times 10^{13})^2}{3.96 \times 10^{15}} = 1.578 \times 10^{11} \text{ cm}^{-3}$$

Here again, $p\left(= \frac{n_i^2}{N_D'}\right)$ is very small compared with N_D' and may be neglected in calculating the effective conductivity.

Therefore, $$\sigma = N_D' q \mu_n$$
$$= (3.96 \times 10^{15})\ (1.6 \times 10^{-19})\ (3800) = 2.408 \text{ S/cm}$$

Hence, resistivity $$\rho = \frac{1}{\sigma} = \frac{1}{2.408} = 0.415\ \Omega\text{-cm}$$

EXAMPLE 1.5

A sample of silicon at a given temperature T in intrinsic condition has a resistivity of 25×10^4 Ω-cm. The sample is now doped to the extent of 4×10^{10} donor atoms/cm^3 and 10^{10} acceptor atoms/cm^3. Find the total conduction current density if an electric field of 4 V/cm is applied across the sample. Given that $\mu_n = 1{,}250$ cm^2/V-s, $\mu_p = 475$ cm^2/V-s at the given temperature.

Solution

$$\sigma_i = qn_i(\mu_n + \mu_p) = \frac{1}{25 \times 10^4} \text{ S/cm}$$

Therefore, $$n_i = \frac{\sigma_i}{q(\mu_n + \mu_p)} = \frac{1}{(25 \times 10^4)(1.602 \times 10^{-19})(1250 + 475)} = 1.45 \times 10^{10} \text{ cm}^{-3}$$

Net donor density $$N_D\ (= n) = (4 \times 10^{10} - 10^{10}) = 3 \times 10^{10} \text{ cm}^{-3}$$

Hence, $$p = \frac{n_i^2}{N_D} = \frac{(1.45 \times 10^{10})^2}{3 \times 10^{10}} = 0.7 \times 10^{10} \text{ cm}^{-3}$$

Hence, $\sigma = q(n\mu_n + p\mu_p)$

$= (1.602 \times 10^{-19})\ (3 \times 10^{10} \times 1250 + 0.7 \times 10^{10} \times 475)$

$= 6.532 \times 10^{-6}$ S/cm

Therefore, total conduction current density,

$$J = \sigma E = 6.532 \times 10^{-6} \times 4 \ = 26.128 \times 10^{-6}\ \text{A/cm}^2$$

EXAMPLE 1.6

Find the concentration (densities) of holes and electrons in *N*-type silicon at 300 K, if the conductivity is 300 S/cm. Also find these values for *P*-type silicon. Given that for silicon at 300 K, $n_i = 1.5 \times 10^{10}/\text{cm}^3$, $\mu_n = 1{,}300\ \text{cm}^2/\text{V-s}$ and $\mu_p = 500\ \text{cm}^2/\text{V-s}$.

Solution

(a) *Concentration in N-type silicon*

The conductivity of *N*-type silicon is $\sigma = qn\mu_n$

Concentration of electrons, $$n = \frac{\sigma}{q\mu_n} = \frac{300}{(1.602 \times 10^{-19})(1300)} = 1.442 \times 10^{18}\ \text{cm}^{-3}$$

Hence, concentration of holes, $$p = \frac{n_i^2}{n} = \frac{(1.5 \times 10^{10})^2}{1.442 \times 10^{18}} = 1.56 \times 10^{2}\ \text{cm}^{-3}$$

(b) *Concentration in P-type silicon*

The conductivity of *P*-type silicon is $\sigma = qp\mu_p$

Hence, concentration of holes $$p = \frac{\sigma}{q\mu_p} = \frac{300}{(1.602 \times 10^{-19})(500)} = 3.75 \times 10^{18}\ \text{cm}^{-3}$$

and concentration of electrons, $$n = \frac{n_i^2}{p} = \frac{(1.5 \times 10^{10})^2}{3.75 \times 10^{18}} = 0.6 \times 10^{2}\ \text{cm}^{-3}$$

1.7 HALL EFFECT

When a transverse magnetic field *B* is applied to a specimen (thin strip of metal or semiconductor) carrying current *I*, an electric field *E* is induced in the direction perpendicular to both *I* and *B*. This phenomenon is known as the *Hall effect*.

A Hall-effect measurement experimentally confirms the validity of the concept that it is possible for two independent types of charge carriers, electrons and holes, to exist in a semiconductor.

The schematic arrangement of the semiconductor, the magnetic field and the current flow pertaining to the Hall effect are shown in Fig. 1.8. Under the equilibrium condition, the electric field intensity, *E*, due to the Hall effect must exert a force on the carrier of charge, *q*, which just balances the magnetic force, i.e.,

$$qE = Bqv_d$$

where v_d is the drift velocity. Also, the electric field intensity due to Hall effect is

$$E = \frac{V_H}{d}$$

where d is the distance between surfaces 1 and 2, and V_H is the Hall voltage appearing between surfaces 1 and 2. In an N-type semiconductor, the current is carried by electrons and these electrons will be forced downward towards side 1 which becomes negatively charged with respect to side 2.

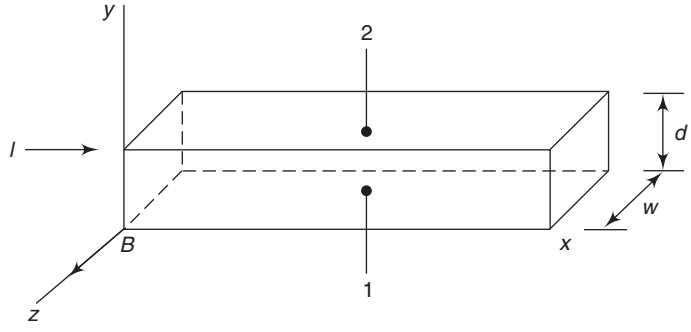


Fig. 1.8 *Schematic arrangement to observe the Hall effect*

The current density (J) is related to charge density (ρ) by

$$J = \rho v_d$$

Further, the current density (J) is related to current (I) by

$$J = \frac{I}{\text{Area}} = \frac{I}{wd}$$

where w is the width of the specimen in the direction of magnetic field (B).

Combining the above relations, we get

$$V_H = Ed = B\, v_d d = \frac{BJd}{\rho} = \frac{BI}{\rho w}$$

The Hall coefficient, R_H, is defined by

$$R_H = \frac{1}{\rho}$$

so that $V_H = \frac{R_H}{w} BI$. A measurement of the Hall coefficient R_H determines not only the sign of the charge carriers but also their concentration. The Hall coefficient for a P-type semiconductor is positive, whereas it is a negative for an N-type semiconductor. This is true because the Hall voltage in a P-type semiconductor is of opposite polarity to that in an N-type semiconductor.

The advantage of Hall-effect transducers is that they are non-contact devices with high resolution and small size.

➤ ***Applications*** The Hall effect is used to find whether a semiconductor is N- or P-type and to determine the carrier concentration. If the terminal 2 becomes positively charged with respect to terminal 1, the semiconductor must be N-type and $\rho = nq$, where n is the electron concentration. On the other hand, if the polarity of V_H is positive at terminal 1 with respect to terminal 2, the semiconductor must be P-type and $\rho = pq$, where p is the hole concentration.

The mobility (μ) can also be calculated with simultaneous measurement of the conductivity (σ). The conductivity and the mobility are related by the equation $\sigma = \rho\mu$ or $\mu = \sigma R_H$.

Therefore, the conductivity for *N*-type semiconductor is $\sigma = nq\mu_n$ and for *P*-type semiconductor, $\sigma = pq\mu_p$, where μ_n is the electron mobility and μ_p is the hole mobility.

Thus, if the conductivity of a semiconductor is measured along with R_H, then mobility can be determined from the following relations.

For *N*-type semiconductor, $\mu_n = \dfrac{\sigma}{nq} = \sigma R_H$

and for *P*-type semiconductor, $\mu_p = \dfrac{\sigma}{pq} = \sigma R_H$

Since V_H is proportional to B for a given current I, Hall effect can be used to measure the ac power and the strength of magnetic field and sense the angular position of static magnetic fields in a magnetic field meter. It is also used in an instrument called Hall-effect multiplier which gives the output proportional to the product of two input signals. If I is made proportional to one of the inputs and B is made proportional to the second signal, then from the equation, $V_H = \dfrac{BI}{\rho w}$, V_H will be proportional to the product of two inputs. Hall devices for such applications are made from a thin wafer or film of indium antimonide (InSb) or indium arsenide. As the material has a very high electron mobility, it has high Hall coefficient and high sensitivity.

An electrical current can be controlled by a magnetic field because the magnetic field changes the resistances of some elements with which it comes in contact. In the magnetic bubble memory, while read-out, the Hall effect element is passed over the bubble. Hence, a change in current of the circuit will create, say, a *one*. If there is no bubble, there will be a *zero* and there will be no current change in the output circuit. The read-in device would have an opposite effect, wherein the Hall device creates a magnetic field when supplied with a pulse of current. This, in turn, creates a little domain and then a magnetic bubble is created.

Some of the other applications are in measurement of velocity, rpm, sorting, limit sensing, and non-contact current measurements.

EXAMPLE 1.7

An *N*-type semiconductor has a Hall coefficient of 200 cm^3/C and its conductivity is 10 S/m. Find its electron mobility.

Solution Given $R_H = 200$ cm^3/C and $\sigma = 10$ S/m.

Therefore, the electron mobility, $\mu_n = \sigma R_H = 10 \times 200 = 2000$ cm^2/V-s

EXAMPLE 1.8

The conductivity of an *N*-type semiconductor is 10 S/m and its electron mobility is 50×10^{-4} m^2/V-s. Determine the electron concentration.

Solution Given $\sigma = 10$ s/m and $\mu_n = 50 \times 10^{-4}$ m^2/V-s.

We know that the electron mobility, $\mu_n = \dfrac{\sigma}{nq}$

Therefore, the electron concentration,

$$n = \frac{\sigma}{\mu q} = \frac{10}{50 \times 10^{-4} \times 1.6 \times 10^{-19}} = 12.5 \times 10^{21} \text{ m}^{-3}$$

EXAMPLE 1.9

A current of 20 A is passed through a thin metal strip, which is subjected to a magnetic flux density of 1.2 Wb/m^2. The magnetic field is directed perpendicular to the current. The thickness of the strip in the direction of the magnetic field is 0.5 mm. The Hall voltage is 60 V. Find the electron density.

Solution Given: $I = 20$ A, $B = 1.2$ Wb/m^2, $V_H = 60$ V and $w = 0.5$ mm

We know that the number of conduction electrons, i.e., electron density,

$$n = \frac{BI}{V_H q w} = \frac{1.2 \times 20}{60 \times 1.6 \times 10^{-19} \times 0.5 \times 10^{-3}} = 5 \times 10^{21} \text{ m}^3$$

1.8 CONTINUITY EQUATION

The fundamental law governing the flow of charge is called the *continuity equation*. The continuity equation as applied to semiconductors describes how the carrier concentration in a given elemental volume of the crystal varies with time and distance. The variation in density is attributable to two basic causes, viz., (i) the rate of generation and loss by recombination of carriers within the element, and (ii) drift of carriers into or out of the element. The continuity equations enable us to calculate the excess density of electrons or holes in time and space.

As shown Fig. 1.9, consider an infinitesimal *N*-type semiconductor bar of volume of area *A* and length *dx* and the average minority carrier (hole) concentration *p*, which is very small compared to the density of majority carriers. At time *t*, if minority carriers (holes) are injected, the minority current entering the volume at *x* is I_p and leaving at $x + dx$ is $I_p + dI_p$ which is predominantly due to diffusion. The minority carrier concentration injected into one end of the semiconductor bar decreases exponentially, with distance into the specimen, as a result of diffusion and recombination. Here, dI_p is the decrease in number of coulomb per second within the volume.

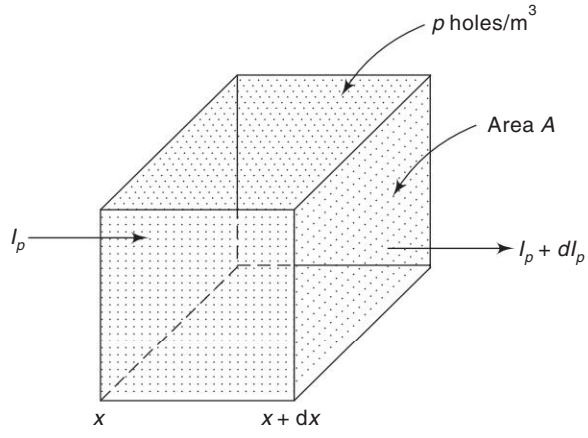


Fig. 1.9 *Relating to continuity equation*

Since the magnitude of the carrier charge is *q*, then $\frac{dI_p}{p}$ equals the decrease in the number of holes per second within the elemental volume $A \propto x$. As the current density $J_p = \frac{I_p}{A}$, we have

$$\frac{1}{Aq} \cdot \frac{dI_p}{dx} = \frac{1}{q} \cdot \frac{dJ_p}{dx} = \text{decrease in hole concentration per second, due to current } I_p$$

We know that an increase in number of holes per unit volume per second is given by $G = p_o/\tau_p$ due to thermal generation. Further, there is a decrease of holes per unit volume per second given by $R = p/\tau_p$ due to recombination but charge can neither be created nor destroyed. Hence, increase in holes per unit volume per second, $\partial p/\partial t$, must equal the algebraic sum of all the increases in hole concentration. Thus,

$$\frac{\partial p}{\partial t} = -\frac{p - p_o}{\tau_p} - \frac{1}{q}\frac{\partial J_p}{\partial x}$$

where $$J_p = -qD_p \frac{dp}{dx} + qp\mu_p E$$

Therefore, $$\frac{\partial p}{\partial t} = -\frac{p - p_o}{\tau_p} + D_p \frac{d^2 p}{dx^2} - \mu_p \frac{d(pE)}{dx}$$

This is the *continuity equation* or *equation of conservation of charge* for holes stating the condition of dynamic equilibrium for the density of mobile carrier holes. Here, partial derivatives have been used since both p and J_p are functions of both t and x.

Similarly, the continuity equation for electrons states the condition of dynamic equilibrium for the density of mobile carrier electrons and is given by

$$\frac{\partial n}{\partial t} = \frac{n_o - n}{\tau_n} - \frac{1}{q}\frac{\partial J_n}{\partial x}$$

where $$J_n = -qD_n \frac{dn}{dx} + qn\mu_n E$$

Therefore, $$\frac{\partial n}{\partial t} = -\frac{n - n_o}{\tau_n} + D_n \frac{d^2 n}{dx^2} - \mu_n \frac{d(nE)}{dx}$$

We now consider three special cases of the continuity equation.

➤ ***Concentration Independent of Distance with Zero Electric Field*** For this special case, the continuity equation can be changed into

$$\frac{\partial p}{\partial t} = -\frac{p - p_0}{\tau_p}$$

Solving the above equation, we get

$$p - p_o = A_1 e^{-t/\tau_p} \text{ where } A \text{ is a constant}$$

➤ ***Concentration Independent of Time with Zero Electric Field*** For this special case, the continuity equation can be changed into

$$0 = -\frac{p - p_o}{\tau_p} + D_p \frac{d^2 p}{dx^2}$$

$$\frac{d^2 p}{dx^2} = \frac{p - p_o}{\tau_p D_p}$$

Solving this equation, we get

$$p - p_o = A_1 e^{-x/L_p} + A_2 e^{x/L_p}$$

where A_1 and A_2 are constants.

$$L_p = \sqrt{D_p \tau_p} \text{ = diffusion length for holes}$$

➤ *Concentration varies Sinusoidally with Time and with Zero Electric Field*

Let $P(x, t) = P(x) e^{j\omega t}$

For this special case, the continuity equation can be changed into

$$j\omega P(x) = -\frac{P(x)}{\tau_p} + D_p \frac{d^2P(x)}{dx^2}$$

$$\frac{d^2p}{dx^2} = \frac{(1 + j\omega\tau_p)}{L_p^2} P$$

At $\omega = 0$, $$\frac{d^2p}{dx^2} = \frac{P}{L_p^2}$$

The above equation is the same as that of the second special case.

➤ ***Minority Carrier Injection in Homogeneous Semiconductors*** Consider the semiconductor bar shown in Fig. 1.7(a). This bar is uniformly doped with donor atoms so that the charge concentration $n = N_D$ is uniform throughout the bar on which radiation falls on one end of the bar at $x = 0$. Near the illuminated surface, the bound electrons in the covalent bonds capture some of the photons. This energy transfer results in breaking of covalent bonds and generation of hole-electron pairs.

The minority carrier (hole) concentration P is very small compared with the doping level, i.e., $P << n$. The condition $p = P + p_o << n$ which states that the minority concentration is much smaller than the majority concentration is called the low-level injection. The controlling differential equation for p is

$$\frac{d^2p}{dx^2} = \frac{p - p_0}{D_p \tau_p}$$

The diffusion length for holes L_p is given by

$$L_p = \sqrt{D_p \tau_p}$$

The differential equation for the injected concentration $P = p - p_0$ becomes

$$\frac{d^2p}{dx^2} = \frac{P}{L_p^2}$$

The solution of the equation is

$$P(x) = A_1 e^{-x/AL_p} + A_2 e^{x/L_p}$$

when $x \to \infty$, $A_2 = 0$. At $x = 0$, the injected concentration $P(0)$ to satisfy this boundary condition, $A_1 = P(0)$.

Therefore,

$$P(x) = P(0)\, e^{-x/L_p} = p(x) - p_0$$

Here, the hole concentration decreases exponentially with distance as shown in Fig. 1.7(b).

➤ ***Diffusion Current*** The minority (hole) diffusion current is $I_p = AJ_p$, where A is the area of cross section of the bar. Therefore,

$$I_p(x) = \frac{Aq\,D_p\,P(0)}{L_p} e^{-x/L_p} = \frac{Aq\,D_p}{L_p}(p(0) - p_o)e^{-x/L_p}$$

This current decreases exponentially with distance x as that of minority carrier concentration.

The majority (electron) diffusion current is

$$Aq\,D_n \frac{dn}{dx} = Aq\,D_n \frac{dp}{dx} = -\frac{D_n}{D_p} I_p$$

where $I_p = -Aq\,D_n \dfrac{dp}{dx}$. The magnitude of ratio of majority to minority diffusion current is $D_n/D_p \approx 3$ for Si and 2 for Ge.

➤ ***Drift Current*** For an open-circuit semiconductor bar, the sum of the hole and electron currents should be zero everywhere. Therefore, a majority (electron) drift current I_{nd} exists such that

$$I_p + \left(I_{nd} - \frac{D_n I_p}{D_p} \right) = 0$$

Therefore,

$$I_{nd} = \left(\frac{D_n}{D_p} - 1 \right) I_p$$

The hole drift current I_{pd} is given by

$$I_{pd} = Aqp\mu_p E = \frac{p}{n} \frac{\mu_p}{\mu_n} \left(\frac{D_n}{D_p} - 1 \right) I_p$$

where the electric field,

$$E = \frac{1}{Aqn\,\mu_n} \left(\frac{D_n}{D_p} - 1 \right) I_p$$

Here as $p << n$, we have $I_{pd} << I_p$, i.e., the hole-drift current is negligible compared to the hole-diffusion current.

1.9 LAW OF JUNCTION

Let us now derive the expression for the total current as a function of applied voltage assuming that the width of the depletion region is zero. When a forward bias is applied to a diode, holes are injected from the P-side into the N-side. Due to this, the concentration of holes in the N-side (p_n) is increased from its thermal equilibrium value (p_{n0}) and injected hole concentration [$P_n(x)$] decreases exponentially with respect to the distance (x).

$$P_n(x) = p_n - p_{n0} = P_n(0) e^{-x/L_p}$$

where L_p is the diffusion length for holes in the *N*-material.

$$p_n(x) = p_{n0} + P_n(0)e^{-x/L_p} \tag{1.16}$$

Injected hole concentration at $x = 0$ is

$$P_n(0) = p_n(0) - p_{n0} \tag{1.17}$$

The several components of hole concentration in the *N*-side of a forward-biased diode are shown in Fig. 1.6, in which the density $p_n(x)$ decreases exponentially with the distance (x).

Let p_p and p_n be the hole concentrations at the edges of the space charge in the *P*- and *N*-sides, respectively. Let V_B ($= V_0 - V$) be the effective barrier potential across the depletion layer. Then

$$p_p = P_n e^{V_B/V_T} \tag{1.18}$$

where V_T is the volt-equivalent of temperature.

This is the Boltzmann's relation of kinetic gas theory. This equation is valid as long as the hole current is small compared to diffusion or drift currents. This condition is called *low-level-injection*.

Under open-circuit condition (i.e., $V = 0$), $p_p = p_{p0}$, $p_n = p_{n0}$ and $V_B = V_0$. Equation (1.18) can be changed into

$$p_{p0} = p_{n0} e^{V_0/V_T} \tag{1.19}$$

Under forward-bias condition, let V be the applied voltage; then the effective barrier voltage

$$V_B = V_0 - V$$

The hole concentration throughout the *P*-side is constant and equal to the thermal equilibrium value ($p_p = p_{p0}$). The hole concentration varies exponentially with distance into the *N*-side.

At $x = 0$, $p_n = p_n(0)$

Equation (1.18) can be changed into

$$p_{p0} = p_n(0)e^{(V_0 - V)/V_T} \tag{1.20}$$

Comparing Eqs (1.19) and (1.20),

$$p_n(0) = p_{n0} e^{V/V_T}$$

This boundary condition is called the *law of the junction*. Substituting this into Eq. (1.17), we get

$$P_n(0) = p_{n0}(e^{V/V_T} - 1) \tag{1.21}$$

The diffusion-hole current in the *N*-side is

$$\begin{aligned} I_{pn}(x) &= -Aq D_p \frac{dp_n(x)}{dx} \\ &= -Aq D_p \frac{d}{dx}\left[p_{n0} + P_n(0)e^{-x/L_p}\right] \\ &= \frac{AqD_pP_n(0)}{L_p} e^{-x/L_p} \end{aligned}$$

From this equation, it is evident that the injected hole current decreases exponentially with distance.

➤ ***Forward Currents*** The hole current crossing the junction into the *N*-side with $x = 0$ is

$$I_{pn}(0) = \frac{AqD_p P_n(0)}{L_p} = \frac{AqD_p p_{n0}}{L_p}(e^{V/V_T} - 1)$$

The electron current crossing the junction into the *P*-side with $x = 0$ is

$$I_{np}(0) = \frac{AqD_n N_p(0)}{L_n} = \frac{AqD_n n_{p0}}{L_n}(e^{V/V_T} - 1)$$

The total diode current,

$$I = I_{pn}(0) + I_{np}(0) = I_o(e^{V/V_T} - 1)$$

where $I_o = \frac{Aq D_p p_{n0}}{L_p} + \frac{AqD_n n_{p0}}{L_n}$ = reverse saturation current.

If we consider carrier generation and recombination in the space-charge region, the general equation of the diode current is approximately given by

$$I = I_o \left[e^{(V/\eta V_T)} - 1\right]$$

where V = external voltage applied to the diode and η = a constant, 1 for germanium and 2 for silicon.

➤ ***Reverse Saturation Current*** We know that $p_n = \frac{n_i^2}{N_D}$ and $n_p = \frac{n_i^2}{N_A}$. Applying these relationships in the above equation of reverse saturation current, I_o, we get

$$I_o = Aq\left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right] n_i^2$$

where $n_i^2 = A_o T^3 e^{-E_{Go}/kT} = A_o T^3 e^{-V_{Go}/V_T}$, where V_{Go} is a voltage which is numerically equal to the forbidden-gap energy E_{Go} in electronvolt.

For a germanium diode, the diffusion constants D_p and D_n vary approximately inversely proportional to T. Hence, the temperature dependence of I_o is

$$I_o = K_1 T^2 e^{\frac{-V_{Go}}{V_T}}$$

where K_1 is a constant independent of temperature.

For a silicon diode, I_o is proportional to n_i instead of n_i^2. Hence,

$$I_o = K_2 T^{\frac{3}{2}} e^{\frac{-V_{Go}}{2V_T}}$$

where K_2 is a constant independent of temperature.

1.10 FERMI DIRAC FUNCTION

An electron inside the metal must possess an energy level that is at least greater than the surface barrier energy E_B, so as to escape to a higher level. It is, therefore, important to know about the energies possessed by the electrons in a metal. This is given by the energy-distribution function.

➤ ***Energy Density*** The distribution in energy of the free electrons in a metal is given by

$$dn = \rho dE$$

where dn is the number of electrons per cubic metre whose energies lie in the energy interval dE, and ρ is the density of electrons in a given energy interval.

It is assumed that there are no potential variations within the metal, since only free electrons are considered. Hence, there must be the same number of electrons in each cubic metre of the metal. That is, the density in space (electrons per cubic metre) is a constant. However, there will be electrons having all possible energies within each unit volume of the metal. This distribution in energy is expressed by

$$\rho = f(E)\, N(E)$$

where $N(E)$ is the density of states in the conductance band, and $f(E)$ is the probability that a quantum state with energy 'E' is occupied by an electron. Therefore,

$$N(E) = \gamma E^{\frac{1}{2}}$$

Here, γ is a constant defined by

$$\gamma = \frac{4\pi}{h^3}(2m)^{\frac{3}{2}}\,(1.602 \times 10^{-19})^{\frac{3}{2}} = 6.82 \times 10^{27}$$

where the dimensions of γ are $(m^{-3})\ (eV)^{-\frac{3}{2}}$, m is the mass of the electron in kg, and h is the Planck's constant in joule-second.

➤ ***Fermi–Dirac Function*** The Fermi–Dirac probability function $f(E)$ specifies the fraction of all states at energy E (in eV) occupied under conditions of thermal equilibrium. From quantum physics,

$$f(E) = \frac{1}{1 + e^{(E - E_F)/kT}}$$

where k is the Boltzmann constant in eV/K, T is the temperature in K, and E_F is the Fermi level or characteristic energy for the crystal in eV.

The Fermi level represents the energy state with 50 percent probability of being filled if no forbidden band exists. That is, if $E = E_F$ then $f(E) = \frac{1}{2}$ for any value of temperature.

The plots of $f(E)$ vs $(E - E_F)$ and $(E - E_F)$ vs $f(E)$ are shown in Fig. 1.10(a) and (b) respectively for $T = 0$ K and larger values of temperature.

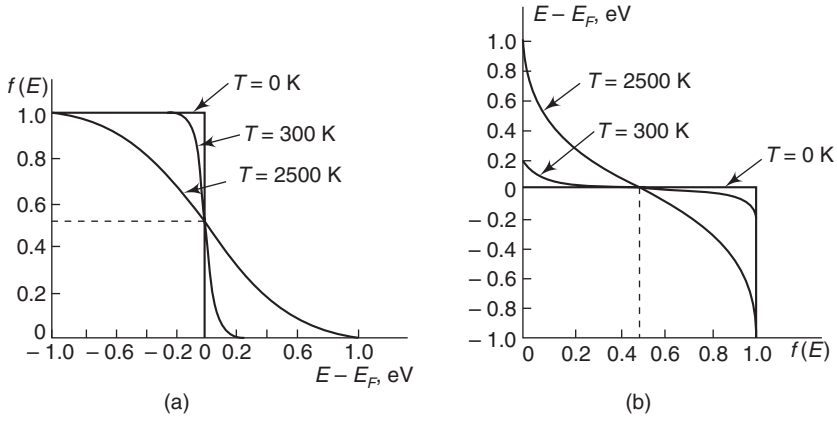


Fig. 1.10 *Fermi–Dirac distribution function f(E) gives the probability that a state of energy E is occupied*

At $T = 0$ K, the following conditions exist:

(i) If $E > E_F$, the exponential term becomes infinite and $f(E) = 0$. Consequently, there is no probability of finding an occupied quantum state of energy greater than E_F at absolute zero temperature.

(ii) If $E < E_F$, the exponential becomes zero and $f(E) = 1$. All quantum levels with energies less than E_F will be occupied at $T = 0$ K.

From these equations, we get at absolute zero temperature,

$$\rho = \begin{cases} \gamma E^{\frac{1}{2}}; & \text{for } E < E_F \\ 0 & \text{for } E > E_F \end{cases}$$

It implies that there are no electrons at 0 K which have energies in excess of E_F. Therefore, the Fermi energy is the maximum energy that any electron may possess at absolute zero temperature.

The relationship given by the above equation is called the *completely degenerate energy distribution function*. In fact, all particles should have zero energy at 0 K. Based on Pauli's exclusion principle, it is also to be mentioned that since no two electrons have the same set of quantum numbers, not all the electrons can have the same energy even at 0 K.

➤ ***Fermi Level*** An expression for E_F may be obtained on the basis of the completely degenerate function. The total number of free electrons is given by

$$n = \int_0^{E_F} \gamma E^{\frac{1}{2}}\, dE = \frac{2}{3}\gamma E_F^{\frac{3}{2}}$$

i.e., $$E_F = \left(\frac{3n}{2\gamma}\right)^{\frac{2}{3}}, \text{ where } \gamma = 6.82 \times 10^{27}$$

Therefore, $$E_F = 3.64 \times 10^{-19}\, n^{\frac{2}{3}}$$

Since the density of free electrons, n, varies from metal to metal, E_F will also vary among metals. Generally, the numerical value of E_F is less than 10 eV.

1.11 FERMI LEVEL IN INTRINSIC AND EXTRINSIC SEMICONDUCTORS

To calculate the conductivity of a semiconductor, the concentration of free electrons n and the concentration of free holes p must be known.

$$dn = N(E)\, f(E)\, dE$$

where dn represents the number of conduction electrons per cubic metre whose energies lie between E and $E + dE$, and $N(E)$ is the density of states. In a semiconductor, the lowest energy in the conduction band is E_C and hence,

$$N(E) = \gamma (E - E_C)^{1/2}$$

The Fermi–Dirac probability function $f(E)$ is given by

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

where E_F is the Fermi level or characteristic energy for the crystal in eV.

The concentration of electrons in the conduction band is,

$$n = \int_{E_C}^{\infty} N(E)\, f(E)\, \mathrm{d}E$$

For $E \geq E_C$, $E - E_F >> kT$,

$$f(E) = e^{-(E - E_F)/kT}$$

and

$$n = \int_{E_C}^{\infty} \gamma (E - E_C)^{\frac{1}{2}}\, e^{-(E-E_F)/kT}\, dE$$

Substitute $(E - E_C) = x^2$, i.e., $E = x^2 + E_C$ and $dE = 2xdx$

At $x = 0$, $E = E_c$,

At $x = \infty$, $E = \infty$

Therefore,

$$n = \int_0^{\infty} \gamma x e^{\left(-\frac{x^2 + E_C - E_F}{kT}\right)} [2xdx]$$

$$= 2\gamma e^{-\left(\frac{E_C - E_F}{kT}\right)} \int_0^{\infty} x^2 e^{-\frac{x^2}{kT}} dx$$

We know that, $\int_0^{\infty} x^{2n}\, e^{-x^2/a^2} dx = \sqrt{\pi}\, \frac{2n!}{n!} \left(\frac{a}{2}\right)^{2n+1}$

Here, $n = 1$ and $a = \sqrt{kT}$

Therefore, $$n = 2\gamma e^{-\left(\frac{E_C - E_F)}{kT}\right)} \times 2\sqrt{\pi}\left(\frac{\sqrt{kT}}{2}\right)^3$$

Substituting $\gamma = \frac{4\pi}{h^3}(2m_n)^{\frac{3}{2}}(1.602 \times 10^{-19})^{\frac{3}{2}}$, we have

$$n = 2 \times \frac{4\pi}{h^3}(2m_n)^{\frac{3}{2}}(1.602 \times 10^{-19})^{\frac{3}{2}} \times \frac{\sqrt{\pi}\,(kT)^{\frac{3}{2}}}{4} \times e^{-\left(\frac{E_C - E_F}{kT}\right)}$$

$$= 2\left(\frac{2m_n \pi kT}{h^2}\right)^{\frac{3}{2}} \times (1.602 \times 10^{-19})^{\frac{3}{2}} e^{-\left(\frac{E_C - E_F}{kT}\right)} = N_C e^{-\left(\frac{E_C - E_F}{kT}\right)}$$

where $N_C = 2\left(\frac{2\pi m_n kt}{h^2}\right)^{\frac{3}{2}}(1.602 \times 10^{-19})^{\frac{3}{2}}$, where m_n is the effective mass of an electron.

When the maximum energy in the valence band is E_V, the density of states is given by

$$N(E) = \gamma(E_V - E)^{1/2}$$

The Fermi function of a hole is $[1 - f(E)]$ and is given by

$$1 - f(E) = \frac{e^{(E - E_F)/kT}}{1 + e^{(E - E_F)/kT}} = e^{-(E_F - E)/kT}$$

where $E_F - E >> kT$ for $E \leq E_V$.

The concentration of holes in the valence band is,

$$p = \int_{-\infty}^{E_V} \gamma(E_V - E)^{1/2}\, e^{-(E_F - E)/kT}\, dE$$

This integral evaluates to

$$p = N_V e^{-(E_F - E_V)/kT}$$

where $N_V = 2\left(\frac{2\pi m_p kT}{h^2}\right)^{3/2}(1.602 \times 10^{-19})^{3/2}$, where m_p is the effective mass of a hole.

➤ ***Fermi Level in an Intrinsic Semiconductor*** In the case of an intrinsic material, the crystal must be electrically neutral.

$$n_i = p_i$$

Therefore, $N_C e^{-(E_C - E_F)/kT} = N_V e^{-(E_F - E_V)/kT}$

Taking logarithm on both sides,

$$\ln \frac{N_C}{N_V} = \frac{E_C + E_V - 2E_F}{kT}$$

$$E_F = \frac{E_C + E_V}{2} - \frac{kT}{2} \ln \frac{N_C}{N_V}$$

If the effective masses of a free electron and hole are the same,

$$N_C = N_V$$

Then,
$$E_F = \frac{E_C + E_V}{2}$$

From the above equation, Fermi level is present at the centre of the forbidden energy band.

➤ ***Donor and Acceptor Impurities*** If a pentavalent substance (antimony, phosphorous, or arsenic) is added as an impurity to pure germanium, four of the five valence electrons of the impurity atoms will occupy covalent bonds and the fifth electron will be available as a carrier of current. These impurities donate excess electron carriers and are, hence, called *donor* or *N*-type impurities.

If a trivalent impurity (boron, gallium, or indium) is added to an intrinsic semiconductor, only three covalent bonds are filled, and the vacancy in the fourth bond constitutes a hole. These impurities are known as *acceptor* or *P*-type impurities.

➤ ***Fermi Level in a Semiconductor having Impurities*** The Fermi level in an *N*-type material is given by

$$E_F = E_C - kT \ln \frac{N_C}{N_D}$$

where $N_D = N_C e^{-(E_C - E_F)/kT}$, the concentration of donor atoms.

The Fermi level in a *P*-type material is given by

$$E_F = E_V + kT \ln \frac{N_V}{N_A}$$

where $N_A = N_V e^{-(E_F - E_V)/kT}$, the concentration of acceptor atoms. The change in the position of Fermi level in *N*- and *P*-type semiconductors is shown in Fig. 1.11.

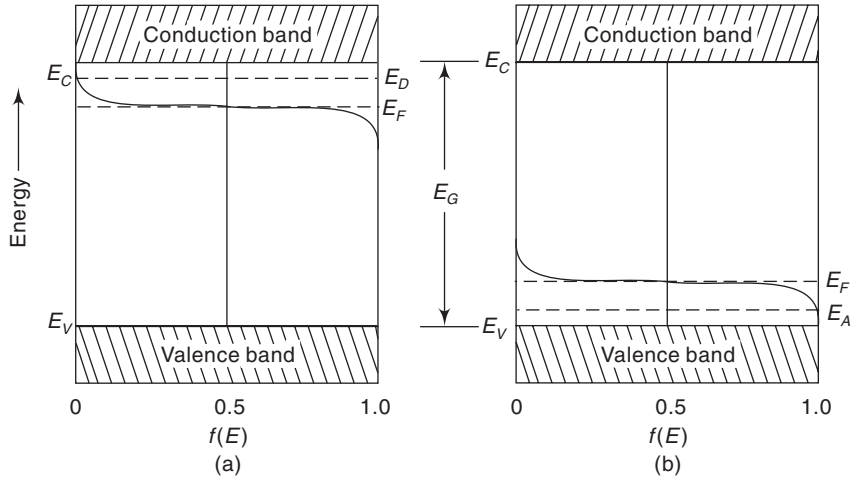


Fig. 1.11 *Positions of Fermi level in (a) N-type, and (b) P-type semiconductors*

➤ ***Movement of E_F with Temperature*** In an *N*-type semiconductor, as the temperature *T* increases, more of electron-hole pairs are formed. At a very high temperature *T*, the concentration of thermally generated electrons in the conduction band will be far greater than the concentration of donor electrons. In such a case, as concentration of electrons and holes become equal, the semiconductor becomes essentially intrinsic and E_F returns to the middle of the forbidden energy gap. Hence, it is concluded that as the temperature of the *P*-type and *N*-type semiconductor increases, E_F progressively moves towards the middle of the forbidden energy gap.

EXAMPLE 1.10

In an *N*-type semiconductor, the Fermi level is 0.3 eV below the conduction level at a room temperature of 300 K. If the temperature is increased to 360 K, determine the new position of the Fermi level.

Solution The Fermi level in an *N*-type material is given by

$$E_F = E_C - kT \ln \frac{N_C}{N_D}$$

Therefore, $$(E_C - E_F) = kT \ln \frac{N_C}{N_D}$$

At $T = 300$ K, $$0.3 = 300k \ln \frac{N_C}{N_D} \quad (1)$$

Similarly, $$E_C - E_{F1} = 360k \ln \frac{N_C}{N_D} \quad (2)$$

Equation (2) divided by Eq. (1) gives

$$\frac{E_C - E_{F1}}{0.3} = \frac{360}{300}$$

Therefore, $$E_C - E_{F1} = \frac{360}{300} \times 0.3 = 0.36 \text{ eV}$$

Hence, the new position of the Fermi level lies 0.36 eV below the conduction level.

EXAMPLE 1.11

In a *P*-type semiconductor, the Fermi level is 0.3 eV above the valence band at a room temperature of 300 K. Determine the new position of the Fermi level for temperatures of (a) 350 K, and (b) 400 K.

Solution The Fermi level in a *P*-type material is given by

$$E_F = E_V + kT \ln \frac{N_V}{N_A}$$

Therefore, $$(E_F - E_V) = kT \ln \frac{N_V}{N_A}$$

At $T = 300$ K, $$0.3 = 300k \ln \frac{N_V}{N_A}$$

(a) At $T = 350$ K, $(E_{F1} - E_V) = 350\ k \ln \frac{N_V}{N_A}$

Hence, from the above equation

$$\frac{E_{F1} - E_V}{0.3} = \frac{350}{300}$$

Therefore, $$E_{F1} - E_V = \frac{350}{300} \times 0.3 = 0.35 \text{ eV}$$

(b) At $T = 400$ K, $(E_{F2} - E_V) = 400\ k \ln \frac{N_V}{N_A}$

Hence, from the above equation,

$$\frac{E_{F2} - E_V}{0.3} = \frac{400}{300}$$

Therefore, $$E_{F2} - E_V = \frac{400}{300} \times 0.3 = 0.4 \text{ eV}$$

EXAMPLE 1.12

In an *N*-type semiconductor, the Fermi level lies 0.2 eV below the conduction band. Find the new position of the Fermi level if the concentration of donor atoms is increased by a factor of (a) 4, and (b) 8. Assume $kT = 0.025$ eV.

Solution In an *N*-type material, the concentration of donor atoms is given by

$$N_D = N_C\, e^{-(E_C - E_F)/kT}$$

Let initially, $N_D = N_{DO}$, $E_F = E_{FO}$ and $E_C - E_{FO} = 0.2$ eV

Therefore, $$N_{DO} = N_C\, e^{-0.2/0.025} = N_C\, e^{-8}$$

(a) When $N_D = 4N_{DO}$ and $E_F = E_{F1}$ then

$$4N_{DO} = N_C\, e^{-(E_C - E_{F1})/0.025} = N_C\, e^{-40(E_C - E_{F1})}$$

Therefore, $$4 \times N_C\, e^{-8} = N_C\, e^{-40(E_C - E_{F1})}$$

Therefore, $$4 = e^{-40(E_C - E_{F1}) + 8}$$

Taking natural logarithm on both sides, we get

$$\ln 4 = -40\,(E_C - E_{F1}) + 8$$

$$1.386 = -40\,(E_C - E_{F1}) + 8$$

Therefore, $$E_C - E_{F1} = 0.165 \text{ eV}$$

(b) When $N_D = 8N_{DO}$ and $E_F = E_{F2}$ then

$$\ln 8 = -40\,(E_C - E_{F2}) + 8$$

$$2.08 = -40\,(E_C - E_{F2}) + 8$$

Therefore, $$E_C - E_{F2} = 0.148 \text{ eV}$$

EXAMPLE 1.13

In a *P*-type semiconductor, the Fermi level lies 0.4 eV above the valence band. Determine the new position of the Fermi level if the concentration of acceptor atoms is multiplied by a factor of (a) 0.5, and (b). Assume $kT = 0.025$ eV.

Solution In a *P*-type material, the concentration of acceptor atoms is given by

$$N_A = N_V e^{-(E_F - E_V)/kT}$$

Let initially, $N_A = N_{AO}$, $E_F = E_{FO}$ and $E_{FO} - E_V = 0.4$ eV

Therefore, $$N_{AO} = N_V e^{-0.4/0.025} = N_V e^{-16}$$

(a) When $N_A = 0.5$, N_{AO} and $E_F = E_{F1}$ then

$$0.5N_{AO} = N_V e^{-(E_{F1} - E_V)/0.025} = N_V e^{-40(E_{F1} - E_V)}$$

Therefore, $$0.5 \times N_V e^{-16} = N_V e^{-40(E_{F1} - E_V)}$$

Therefore, $$0.5 = e^{-40(E_{F1} + E_V) + 16}$$

Taking natural logarithm on both sides, we get

$$\ln (0.5) = -40(E_{F1} - E_V) + 16$$

Therefore, $$E_{F1} - E_V = 0.417 \text{ eV}$$

(b) When $N_A = 4N_{AO}$ and $E_F = E_{F2}$ then

$$\ln 4 = -40(E_{F2} - E_V) + 16$$

Therefore, $$E_{F2} - E_V = 0.365 \text{ eV}$$

REVIEW QUESTIONS

1. Describe the energy-band structures of an insulator, a metal, and a semiconductor.
2. What are the three commonly used semiconductors?
3. What is meant by intrinsic semiconductor?
4. Explain the differences between intrinsic and extrinsic semiconductors.
5. What is meant by hole? How do the holes move in an intrinsic semiconductor?
6. What is meant by doping in a semiconductor?
7. Discuss the following with respect to semiconductor: (i) doping (ii) dopant (iii) donor (iv) acceptor.
8. Explain "majority and minority carriers" in a semiconductor.
9. What is meant by *N*-type impurity in a semiconductor?
10. What is meant by *P*-type impurity in a semiconductor?
11. Define the terms *conductivity* and *mobility* in a semiconductor.
12. Derive the conductivity equation for *N*-type and *P*-type semiconductors.
13. Prove that the conductivity of a semiconductor is given by, $\sigma = q(P\,\mu_p + n\,\mu_n)$.
14. Describe the phenomenon of diffusion of charge carriers in semiconductors.

15. In an *N*-type semiconductor, the Fermi level lies 0.4 eV below the conduction band at 300 K. Determine the new position of the Fermi level if (i) the temperature is increased to 400 K, and (ii) the concentration of donor atoms is increased by a factor of 6. Assume $kT = 0.03$ eV.

(*Ans.*: (i) 0.533 eV (ii) 0.3463 eV below the conduction band)

16. In a *P*-type semiconductor, the Fermi level lies 0.4 eV above the valence band at 300 K. Determine the new position of the Fermi level (i) at 450 K, and (ii) if the concentration of acceptor atoms is multiplied by a factor of 2. Assume $kT = 0.03$ eV. (*Ans.*: (i) 0.6 eV and (ii) 0.38 eV above the valence band)

17. The mobilies of electrons and holes in a sample of intrinsic germanium at room temperature are 0.36 m^2/V-s and 0.17 m^2/V-s, respectively. If the electron and hole densities are each equal to $2.5 \times 10^{19}/m^3$, calculate the conductivity. (*Ans.*: $\sigma_i = 2.12$ S/m)

18. Compute the conductivity of a silicon semiconductor which is doped with acceptor impurity to a density of 10^{22} atoms/m^3. Given that $n_i = 1.4 \times 10^{16}/m^3$, $\mu_n = 0.145$ m^2/V-s and $\mu_p = 0.05$ m^2/V-s.

(*Ans.:* 80 S/m)

19. The conductivity of pure silicon at room temperature is 5×10^{-4} S/m. How many aluminium atoms per m^3 are required so that a saturation conductivity of 200 S/m could be achieved in silicon using aluminium as an impurity? Given that the mobility of holes in silicon is 0.05 m^2/V-s and the mobility of electrons is 0.13 m^2/V-s. (*Ans.*: $2.5 \times 10^{22}/m^3$)

20. Calculate the conductivity of pure silicon at room temperature of 300 K. Given that $n_i = 1.5 \times 10^{16}/m^3$, $\mu_n = 0.13$ m^2/V-s, $\mu_p = 0.05$ m^2/V-s and $q = 1.602 \times 10^{-19}$ C. Now the silicon is doped 2 in 10^8 of a donor impurity. Calculate its conductivity if there are 5×10^{28} silicon atoms/m^3. By what factor has the conductivity increased?

(*Ans.:* 4.32×10^{-4} S/m; 20.8 S/m; ≈ 48,000)

21. The mobilies of free electrons and holes in pure silicon are 0.13 and 0.05 m^2/V-s and the corresponding values for pure germanium are 0.38 and 0.18 m^2/V-s respectively. Determine the values of intrinsic conductivity for both silicon and germanium. Given that $n_i = 2.5 \times 10^{19}/m^3$ for germanium and $n_i = 1.5 \times 10^{16}/m^3$ for silicon at room temperature. (*Ans.:* 0.43 S/m; 2.24 S/m).

22. (i) A crystal of pure germanium has sufficient antimony (*N*-type or donor impurities) added to produce 1.5×10^{22} antimony atoms/m^3. The electron and hole mobility are 0.38 m^2/V-s and 0.18 m^2/V-s respectively, and the intrinsic charge carrier density is $2.5 \times 10^{19}/m^3$. Calculate (a) the density of electrons and holes in the crystal, and (b) the conductivity.

(ii) A second germanium crystal is produced which is doped with 2.5×10^{22} indium (*P*-types or acceptor impurities) atoms/m^3. Repeat the calculations listed in part (i).

(iii) A *PN* junction is made by joining the two crystals described above. Calculate its barrier voltage at 300 K.

(*Ans.:* (i) $n = 1.5 \times 10^{22}/m^3$, $p = 4.167 \times 10^{16}/m^3$, $\sigma = 912/\Omega$-m
(ii) $n = 2.5 \times 10^{16}/m^3$, $p = 2.5 \times 10^{22}/m^3$, $\sigma = 720/\Omega$-m (iii) 0.335 V

23. Explain the drift and diffusion currents for a semiconductor.

24. State and explain mass-action law.

25. What is Einstein relationship in a *PN* junction?

26. Derive the continuity equation from the first principle.

27. Show that in an intrinsic semiconductor, the Fermi level is located at the middle of the unallowable energy gap.

28. Explain Hall effect. How can Hall effect be used to determine some of the properties of a semiconductor?

29. Describe the applications of Hall effect.

30. A sample of *N*-type semiconductor has a Hall coefficient of 150 cm^3/coulomb. If its resistivity is 0.15 Ω-cm, estimate the electron mobility in the sample. [*Ans:* 1000 cm^2/V-s]

31. The conductivity of a pure silicon bar is $5 \times 10^{-4}/\Omega$-m. The magnetic flux density is 0.1 Wb/m^2 and the thickness of the bar in the direction of the magnetic field is 3 mm. The measured values of Hall voltage and current are 50 mV and 10 μA, respectively. Find the hole mobility. [*Ans:* 0.075m^2/V-s]

OBJECTIVE-TYPE QUESTIONS

1. One of the following is not a semiconductor:
(a) Gallium arsenide (b) Indium (c) Germanium (d) Silicon

2. Referring to energy-level diagram of semiconductor materials, the width of the forbidden band-gap is about
(a) 10 eV (b) 100 eV (c) 1 eV (d) 0.1 eV

3. The electron mobility of the following semiconductor material is higher:
(a) Germanium (b) Silicon (c) Gallium arsenide (d) Indium

4. The energy required for relegating an electron from the valence bond for germanium is
(a) 0.66 eV (b) 1.08 eV (c) 1.58 eV (d) 1.88 eV

5. The unit of mobility is
(a) $m^2V^{-1}s^{-1}$ (b) $mV^{-1}s^{-1}$ (c) Vsm^{-1} (d) Vms^{-1}

6. The conductivity of a semiconductor crystal due to any current carrier is NOT proportional to
(a) mobility of the carrier (b) effective density of state in conduction band
(c) electronic charge (d) surface states in the semiconductor

7. A long specimen of *P*-type semiconductor
(a) is positively charged (b) is electrically neutral
(c) has an electric field along its length (d) acts as a dipole

8. With increasing temperature, the resistivity of an intrinsic semiconductor decreases. This is because, with the increase of temperature,
(a) both the carrier concentration and mobility of carriers decrease
(b) the carrier concentration increases but the mobility of carriers decreases
(c) the carrier concentration decreases but the mobility of carriers increases
(d) the carrier concentration remains the same but the mobility of carriers decreases

9. If an intrinsic semiconductor is doped with a very small amount of boron, then in the extrinsic semiconductor so formed, the number of electrons and holes will
(a) decrease. (b) increase and decrease
(c) increase (d) decrease and increase

10. In an *N*-type semiconductor, the concentration of minority carriers mainly depends upon the
(a) doping technique (b) temperature of material
(c) number of donor atoms (d) quality of the intrinsic semiconductor material

11. Consider the following statements for an *N*-type semiconductor:
1. E_F lies below E_D at a room temperature (T)
2. E_F lies above E_D at $T \to 0$
3. $E_F = E_D$ at some intermediate temperature
4. E_F is invariant with temperature

where E_F is Fermi energy and E_D is donor level energy.
Which of these statement is/are correct?
(a) 1 and 2 (b) 2 and 3 (c) 4 only (d) 1, 2 and 3

12. The intrinsic carrier concentration of a silicon sample at 300 K is 1.5×10^{11} /m^3. If after doping, the number of majority carriers is 5×10^{20} /m^3, the minority carrier density is
(a) 4.50×10^{11} /m^3 (b) 3.33×10^{4} /m^3
(c) 5.00×10^{20} /m^3 (d) 3.00×10^{-5} /m^3

13. For intrinsic GaAs, the room-temperature electrical conductivity is 10^{-6}(ohm–m)$^{-1}$, the electron and hole mobilities are, respectively, 0.85 and 0.04 m^2/V–s. What is the intrinsic carrier concentration n_i at the room temperature?
(a) 10^{-21} m^{-3} (b) 10^{-20} m^{-3} (c) 7.0×10^{12} m^{-3} (d) 7.0×10^{-20} m^{-3}

14. Drift current in semiconductors depends upon
(a) only the electric field

(b) only the carrier concentration gradient
(c) both the electric field and the carrier concentration
(d) both electric field and the carrier concentration gradient

15. Diffusion current of holes in a semiconductor is proportional to (with p = concentration of holes/unit volume)

(a) $\frac{dp}{dx^2}$ (b) $\frac{dp}{dx}$

(c) $\frac{dp}{dt}$ (d) $\frac{d^2p}{dx^2}$

16. Consider two energy levels; E_1, E eV above the Fermi level and E_2, E eV below the Fermi level. P_1 and P_2 are respectively the probabilities of E_1 being occupied by an electron and E_2 being empty. Then
(a) $P_1 > P_2$ (b) $P_1 = P_2$ (c) $P_1 < P_2$
(d) P_1 and P_2 depend on number of free electrons

17. In an intrinsic semiconductor, the free electron concentration depends on
(a) effective mass of electrons only
(b) effective mass of holes only
(c) temperature of the semiconductor
(d) width of the forbidden energy band of the semiconductor

18. Which of the following quantities cannot be measured/determined using Hall effect?
(a) Type of semiconductor (P or N) (b) Mobility of charge carriers
(c) Diffusion constant (d) Carrier concentration

19. What does a Hall-effect sensor sense?
(a) Temperature (b) Moisture
(c) Magnetic fields (d) Pressure

20. A current of 20 A is passed through a thin metal strip which is subjected to a magnetic flux density of 1.2 Wb/m^2. The magnetic field is directed perpendicular to the current. The thickness of the strip in the direction of the magnetic field is 0.5 mm. The Hall voltage is 60 V. Find the electron density.
(a) 0.5×10^{21} m^3 (b) 5×10^{21} m^3
(c) 0.05×10^{21} m^3 (d) 5.5×10^{21} m^3

21. The current density as per Hall effect is _____ to charge density.
(a) directly proportional (b) inversely proportional
(c) not proportional (d) none of the above

22. In an extrinsic semiconductor, the Hall coefficient R_H
(a) increases with increase of temperature
(b) decreases with increase of temperature
(c) is independent of the change of temperature
(d) changes with the change of magnetic field

2 Junction Diode Characteristics and Special Diodes

2.1 INTRODUCTION

The *PN* junction diode is one of the semiconductor devices with two semiconductor materials in physical contact, one with excess of holes (*P*-type) and other with excess of electrons (*N*-type). A *PN* junction diode may be formed from a single crystal intrinsic semiconductor by doping part of it with acceptor impurities and the remaining with donors. Such junctions can form the basis of very efficient rectifiers. The most important characteristic of a *PN* junction is its ability to allow the flow of current in only one direction. In the opposite direction, it offers very high resistance. The high vacuum diode has largely been replaced by silicon and selenium rectifiers. Semiconductor diodes find wide applications in all phases of electronics, viz. radio and TV, optoelectronics, power supplies, industrial electronics, instrumentation, computers, etc. The chapter deals with the working of *PN* junction diode and its characteristics.

In addition to the *PN* junction diode, other types of diodes like Zener diode, varactor diode, tunnel diode, LED, PIN diode and PIN Photodiode are also discussed in this chapter and they are manufactured for specific applications. These special diodes are two terminal devices with their doping levels carefully selected to give the desired characteristics.

2.2 OPERATION AND CHARACTERISTICS OF *PN* JUNCTION DIODE

2.2.1 *PN* Junction Diode in Equilibrium with no Applied Voltage

In a piece of semiconductor material, if one half is doped by *P*-type impurity and the other half is doped by *N*-type impurity, a *PN* junction is formed. The plane dividing the two halves or zones is called the *PN* junction. As shown in Fig. 2.1, the *N*-type material has high concentration of free electrons, while the *P*-type material has high concentration of holes. Therefore, at the junction there is a tendency for the free electrons to diffuse over to the *P*-side and holes to the *N*-side. This process is called *diffusion.* As the free electrons move across the junction from *N*-type to *P*-type, the donor ions become positively charged. Hence, a positive charge is built on the *N*-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filling in the holes. Therefore, a net negative charge is established on the *P*-side of the junction. This net negative charge on the *P*-side prevents further diffusion of electrons into the *P*-side. Similarly, the net positive charge on the *N*-side repels the hole crossing from *P*-side to *N*-side. Thus, a barrier is set up near the junction which prevents further movement of charge carriers, i.e., electrons and holes. As a consequence of the induced electric field across the depletion layer, an electrostatic potential difference is established between *P*- and *N*-regions, which is called the potential barrier, junction barrier, diffusion potential, or contact potential, V_o. The magnitude of the

contact potential V_o varies with doping levels and temperature. V_o is 0.3 V for germanium and 0.72 V for silicon.

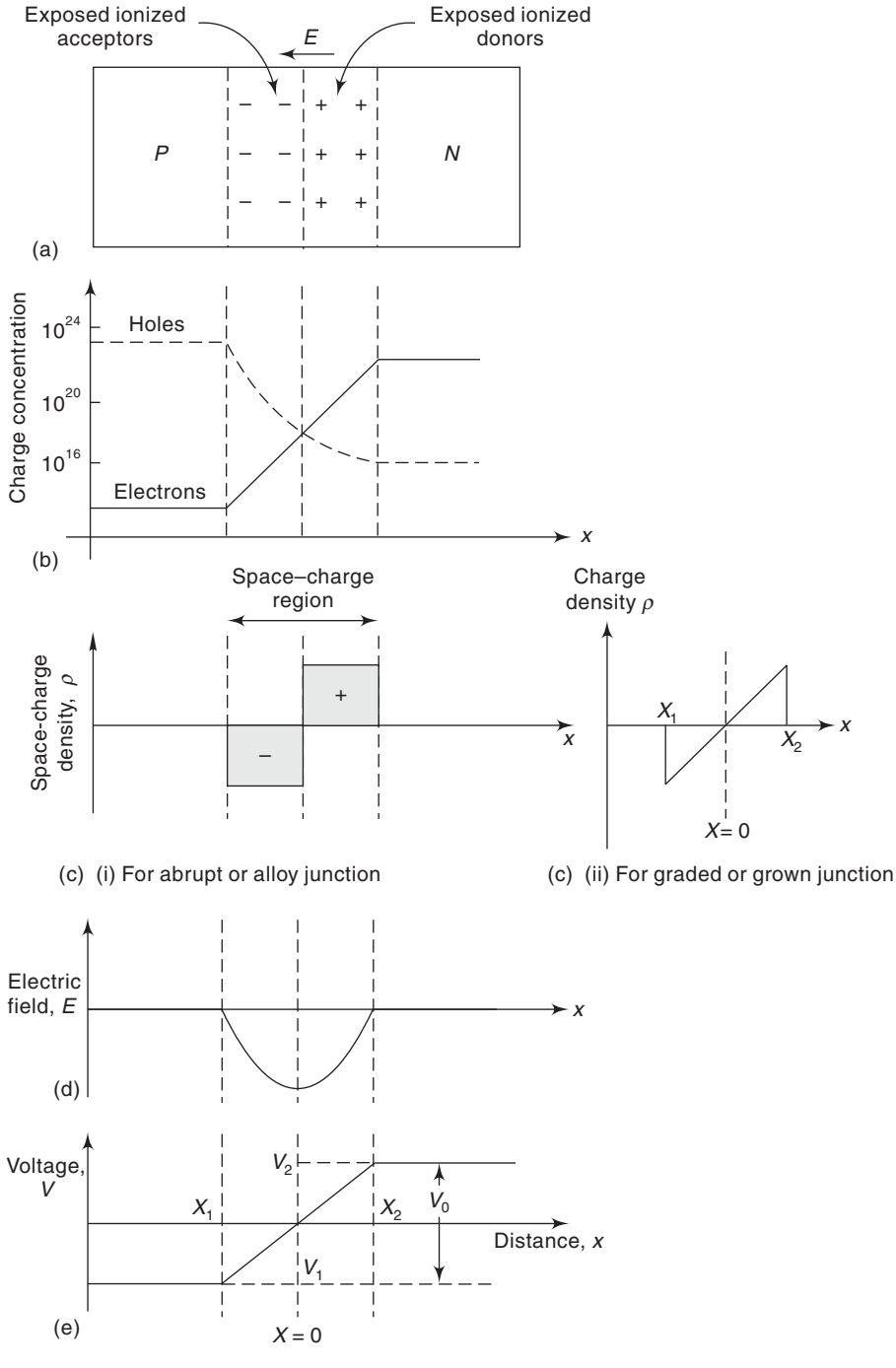


Fig. 2.1 *Formation of PN junction*

The electrostatic field across the junction caused by the positively charged *N*-type region tends to drive the holes away from the junction and negatively charged *P*-type region tends to drive the electrons away from the junction. The majority holes diffusing out of the *P*-region leave behind negatively charged acceptor atoms bound to the lattice, thus exposing negative space charge in a previously neutral region. Similarly, electrons diffusing from the *N*-region expose positively ionized donor atoms, and a double-space-charge layer builds up at the junction as shown in Figs 2.1(a) and (c).

It is noticed that the space-charge layers are of opposite sign to the majority carriers diffusing into them, which tends to reduce the diffusion rate. Thus, the double space of the layer causes an electric field to be set up across the junction directed from *N*- to *P*-regions, which is in such a direction to inhibit diffusion of majority electrons and holes, as illustrated in Figs 2.1(a) and (d). The shape of the charge density, ρ, depends upon how the diode is doped, Thus, the junction region is depleted of mobile charge carriers. Hence, it is called the depletion region (layer), the space-charge region, or the transition region. The depletion region is of order 0.5 μm thick. There are no mobile carriers in this very narrow depletion layer. Hence, no current flows across the junction and the system is in equilibrium. To the left of this depletion layer, the carrier concentration is $p \approx N_A$, and to its right, it is $n \approx N_D$.

➤ ***Calculation of Depletion Width*** Let us now consider the width of the depletion region in the junction of Fig. 2.1. The region contains space charge due to the fact that donors on the *N*-side and acceptors on the *P*-side have lost their accompanying electrons and holes. Hence, an electric field is established which, in turn, causes a difference in potential energy, qV_o, between the two parts of the specimen. Thus, a potential is built up across the junction and Fig. 2.1(e) represents the variation in potential. Here, the *P*-side of the junction is at a lower potential than the *N*-side which means that the electrons on the *P*-side have a great potential energy.

In this analysis, let us consider an *alloy junction* in which there is an abrupt change from acceptor ions on *P*-side to donor ions on *N*-side. Assume that the concentration of electrons and holes in the depletion region is negligible and that all of the donors and acceptors are ionized. Hence, the regions of space charge may be described as

$$\rho = -qN_A,\ 0 > x > X_1$$
$$\rho = +qN_D,\ X_2 > x > 0$$
$$\rho = 0, \text{ elsewhere}$$

where ρ is the space-charge density, as indicated in Fig. 2.1(c)(i). The axes have been chosen in Fig. 2.1(e) in such a way that V_1 and X_1 have negative values. The potential variation in the space-charge region can be calculated by using Poisson's equation, which is given by

$$\nabla^2 V = -\frac{\rho(x, y, z)}{\varepsilon_0 \varepsilon_r}$$

where ε_r is the relative permittivity. The relevant equation for the required one-dimensional problem is

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon_0 \varepsilon_r}$$

Applying the above equation to the *P*-side of the junction, we get

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\varepsilon_0 \varepsilon_r}$$

Integrating twice, we get

$$V = \frac{qN_A x^2}{2\varepsilon_0 \varepsilon_r} + Cx + D$$

where C and D are the constants of integration.

From Fig. 2.1(e), we have $V = 0$ at $x = 0$, and, hence, $D = 0$. When $x < X_1$ on the P-side, the potential is constant, so that $\frac{dV}{dx} = 0$ at $x = X_1$. Hence,

$$C = -\frac{qN_A}{\varepsilon_o \varepsilon_r} \cdot X_1$$

Therefore,
$$V = \frac{qN_A x^2}{2\varepsilon_o \varepsilon_r} - \frac{qN_A}{\varepsilon_o \varepsilon_r} \cdot X_1 \cdot x$$

i.e.,
$$V = \frac{qN_A}{\varepsilon_o \varepsilon_r}\left(\frac{x^2}{2} - X_1 \cdot x\right)$$

As $V = V_1$ at $x = X_1$, we have

$$V_1 = -\frac{qN_A}{2\varepsilon_o \varepsilon_r} \cdot X_1^2$$

If we apply the same procedure to the N-side, we get

$$V_2 = \frac{qN_D}{2\varepsilon_o \varepsilon_r} \cdot X_2^2$$

Therefore, the total built-in potential or the contact potential is V_o, where

$$V_o = V_2 - V_1 = \frac{q}{2\varepsilon_o \varepsilon_r}(N_A X_1^2 + N_D X_2^2)$$

We know the fact that the positive charge on the N-side must be equal in magnitude to the negative charge on the P-side for the neutral specimen. Hence,

$$N_A X_1 = -N_D X_2$$

and substituting this relationship in the above equation and using the fact that X_1 is a negative quantity, we get

$$X_1 = -\left[\frac{2\varepsilon_o \varepsilon_r V_o}{qN_A\left(1 + \frac{N_A}{N_D}\right)}\right]^{1/2}$$

Similarly,
$$X_2 = \left[\frac{2\varepsilon_o \varepsilon_r V_o}{qN_D\left(1 + \frac{N_D}{N_A}\right)}\right]^{1/2}$$

The total depletion width, $W = X_2 - X_1$ and, hence, $W^2 = X_1^2 + X_2^2 - 2X_1 X_2$, and then substituting for X_1 and X_2 from the above equations, we find

$$W = \left[\frac{2\varepsilon_o \varepsilon_r V_o}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) \right]^{1/2}$$

Here, in an *alloy junction*, the depletion width W is proportional to $(V_o)^{1/2}$.

In a *grown junction,* the charge density (ρ) varies linearly with distance (x) as shown in Fig. 2.1(c)(ii). If a similar analysis is carried for this junction, it is found that W varies as $(V_o)^{1/3}$ instead of $(V_o)^{1/2}$.

2.2.2 Under Forward-Bias Condition

When the positive terminal of the battery is connected to the *P*-type and negative terminal to the *N*-type of the *PN* junction diode, the bias applied is known as forward bias.

➤ ***Operation*** As shown in Fig. 2.2, the applied potential with external battery acts in opposition to the internal potential barrier and disturbs the equilibrium. As soon as equilibrium is disturbed by the application of an external voltage, the Fermi level is no longer continuous across the junction. Under the forward-bias condition, the applied positive potential repels the holes in the *P*-type region so that the holes move towards the junction and the applied negative potential repels the electrons in the *N*-type region and the electrons move towards the junction. Eventually, when the applied potential is more than the internal barrier potential, the depletion region and internal potential barrier disappear.

➤ ***V–I Characteristics of a Diode under Forward Bias*** Under forward-bias condition, the *V–I* characteristics of a *PN* junction diode are shown in Fig. 2.3. As the forward voltage (V_F) is increased, for $V_F < V_O$, the forward current I_F is almost zero (region *OA*) because the potential barrier prevents the holes from *P*-region and electrons from *N*-region to flow across the depletion region in the opposite direction.

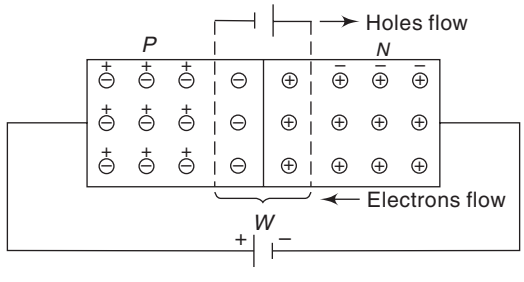


Fig. 2.2 *PN junction under forward bias*

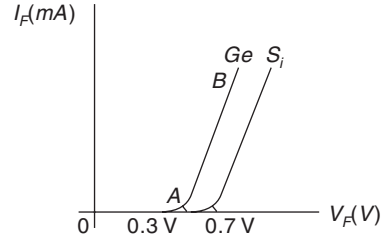


Fig. 2.3 *V–I characteristics of a diode under forward-bias condition*

For $V_F > V_O$, the potential barrier at the junction completely disappears and, hence, the holes cross the junction from *P*-type to *N*-type and the electrons cross the junction in the opposite direction, resulting in relatively large current flow in the external circuit.

A feature worth to be noted in the forward characteristics shown in Fig. 2.3 is the cut in or threshold voltage (V_r) below which the current is very small. It is 0.3 V and 0.7 V for germanium and silicon, respectively. At the cut-in voltage, the potential barrier is overcome and the current through the junction starts to increase rapidly.

2.2.3 Under Reverse-Bias Condition

When the negative terminal of the battery is connected to the *P*-type and positive terminal of the battery is connected to the *N*-type of the *PN* junction, the bias applied is known as reverse bias.

➤ ***Operation*** Under applied reverse bias as shown in Fig. 2.4, holes which form the majority carriers of the *P*-side move towards the negative terminal of the battery and electrons which form the majority carrier of the *N*-side are attracted towards the positive terminal of the battery. Hence, the width of the depletion region which is depleted of mobile charge carriers increases. Thus, the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier. Hence, the resultant potential barrier is increased which prevents the flow of majority carriers in both directions; the depletion width, *W*, is proportional to $\sqrt{V_o}$ under reverse bias. Therefore, theoretically, no current should flow in the external circuit. But in practice, a very small current of the order of a few microampere flows under reverse bias as shown in Fig. 2.5. Electrons forming covalent bonds of the semiconductor atoms in the *P*- and *N*-type regions may absorb sufficient energy from heat and light to cause breaking of some covalent bonds. Hence, electron-hole pairs are continually produced in both the regions. Under the reverse-bias condition, the thermally generated holes in the *P*-region are attracted towards the negative terminal of the battery and the electrons in the *N*-region are attracted towards the positive terminal of the battery. Consequently, the minority carriers, electrons in the *P*-region and holes in the *N*-region, wander over to the junction and flow towards their majority carrier side giving rise to a small reverse current. This current is known as *reverse saturation current, I_o*. The magnitude of the reverse saturation current mainly depends upon junction temperature because the major source of minority carriers is thermally broken covalent bonds.

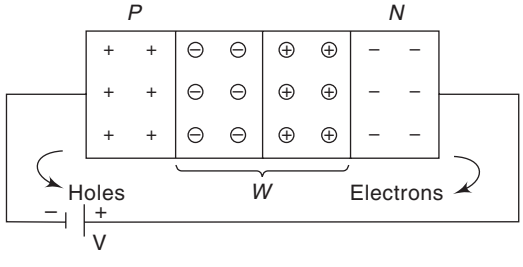


Fig. 2.4 *PN junction under reverse bias*

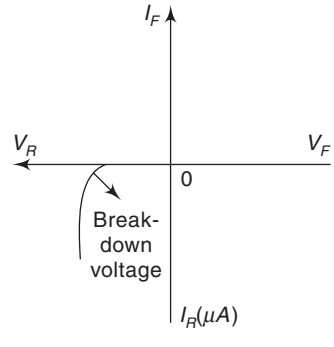


Fig. 2.5 *V–I characteristics under reverse bias*

For large applied reverse bias, the free electrons from the *N*-type moving towards the positive terminal of the battery acquire sufficient energy to move with high velocity to dislodge valence electrons from semiconductor atoms in the crystal. These newly liberated electrons, in turn, acquire sufficient energy to dislodge other parent electrons. Thus, a large number of free electrons are formed which is commonly called an avalanche of free electrons. This leads to the breakdown of the junction leading to very large reverse current. The reverse voltage at which the junction breakdown occurs is known as *breakdown voltage*, V_{BD}.

2.2.4 *PN* Junction as a Diode

Figure 2.6 shows the current-voltage characteristics of *PN* junction. The characteristics of the *PN* junction vary enormously depending upon the polarity of the applied voltage. For a forward-bias voltage, the current

increases exponentially with the increase of voltage. A small change in the forward-bias voltage increases the corresponding forward-bias current by orders of magnitude and, hence, the forward-bias *PN* junction will have a very small resistance. The level of current flowing across a forward-biased *PN* junction largely depends upon the junction area. In the reverse-bias direction, the current remains small, i.e., almost zero, irrespective of the magnitude of the applied voltage and hence the reverse-bias *PN* junction will have a high resistance. The reverse-bias current depends on the area, temperature and type of semiconductor material.

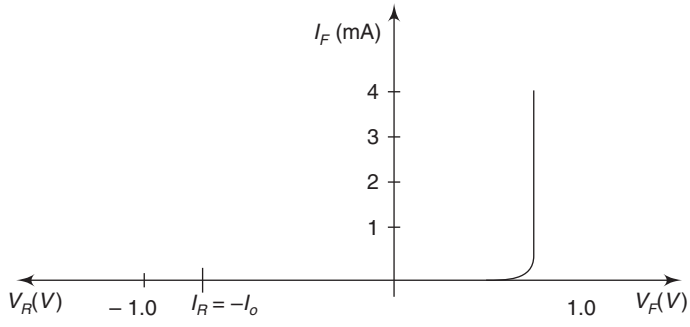


Fig. 2.6 *Ideal I–V characteristics of a PN junction diode*

The semiconductor device that displays these *I–V* characteristics is called a *PN* junction diode. Figure 2.7 shows the *PN* junction diode with forward-bias and reverse-bias and their circuit symbols. The metal contacts are indicated with which the homogeneous *P*-type and *N*-type materials are provided. Thus, two metal-semiconductor junctions, one at each end of the diode, are introduced. The contact potential across these junctions is approximately independent of the direction and magnitude of the current. A contact of this type is called an *ohmic contact*, which has low resistance. In the forward bias, a relatively large current is produced by a fairly small applied voltage. In the reverse bias, only a very small current, ranging from nanoamps to microamps is produced. The diode can be used as a voltage controlled switch, i.e., OFF for a reverse-bias voltage and ON for a forward-bias voltage.

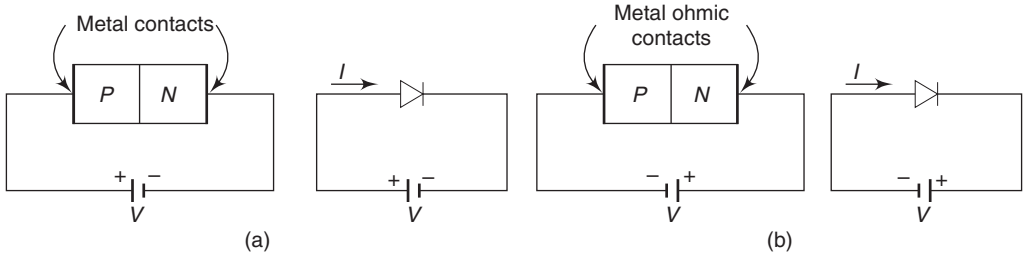


Fig. 2.7 *(a) Forward-biased PN junction diode and its circuit symbol*
(b) Reverse-biased PN junction diode and its circuit symbol

When a diode is reverse-biased by at least 0.1 V, the diode current is $I_R = -I_o$. As the current is in the reverse direction and is a constant, it is called the diode *reverse saturation current.* Real diodes exhibit reverse-bias current that are considerably larger than I_o. This additional current is called a *generation current* which is due to electrons and holes being generated within the space-charge region. A typical value of I_0 may be 10^{-14} A and a typical value of reverse-bias current may be 10^{-9} A.

2.2.5 *PN* Junction Diode as a Rectifier

A *PN* junction diode is a two-terminal device that is polarity sensitive. When the diode is forward biased, the diode conducts and allows current to flow through it without any resistance, i.e., the diode is ON. When the diode is reverse biased, the diode does not conduct and no current flows through it, i.e., the diode is OFF, or providing a blocking function. Thus, an ideal diode acts as a switch, either open or closed, depending upon the polarity of the voltage placed across it. The ideal diode has zero resistance under forward bias and infinite resistance under reverse bias.

2.2.6 Diode Ratings or Limiting Values of *PN* Junction Diode

The *PN* junction diode will perform satisfactorily only if it is operated within certain limiting values. They are the following:

- **Maximum Forward Current** It is the highest instantaneous current under forward-bias condition that can flow through the junction.
- **Peak Inverse Voltage (PIV)** It is the maximum reverse voltage that can be applied to the *PN* junction. If the voltage across the junction exceeds PIV under reverse-bias condition, the junction gets damaged.
- **Maximum Power Rating** It is the maximum power that can be dissipated at the junction without damaging the junction. Power dissipation is the product of voltage across the junction and current through the junction.
- **Maximum Average Forward Current** It is given at a special temperature, usually 25°C, (77°F) and refers to the maximum amount of average current that can be permitted to flow in the forward direction. If this rating exceeds its limit then the structure breakdown can occur.
- **Repetitive Peak Forward Current** It is the maximum peak current that can be permitted to flow in the forward direction in the form of recurring pulses. The limiting value of this current is 450 mA.
- **Maximum Surge Current** It is the maximum current permitted to flow in the forward direction in the form of non-recurring pulses. The current should not equal this value for more than a few milliseconds.

The above diode ratings are subject to change with temperature variations. If the operating temperature is more than that stated for the rating then the ratings must be decreased.

2.3 CURRENT COMPONENTS IN *PN* JUNCTION DIODE

Let us now derive the expression for the total current as a function of applied voltage assuming that the width of the depletion region is zero. When a forward bias is applied to a diode, holes are injected from the *P*-side into the *N*-side. Due to this, the concentration of holes in the *N*-side (p_n) is increased from its thermal equilibrium value (p_{n0}) and injected hole concentration [$P_n(x)$] decreases exponentially with respect to the distance (x).

$$P_n(x) = p_n - p_{n0} = P_n(0)e^{-x/L_p}$$

where L_p is the diffusion length for holes in the *N*-material.

$$p_n(x) = p_{n0} + P_n(0)e^{-x/L_p} \tag{2.1}$$

Injected hole concentration at $x = 0$ is

$$P_n(0) = p_n(0) - p_{n0} \tag{2.2}$$

Let p_p and p_n be the hole concentrations at the edges of the space charge in the *P*- and *N*-sides, respectively. Let V_B (= $V_0 - V$) be the effective barrier potential across the depletion layer. Then

$$p_p = P_n e^{V_B/V_T} \tag{2.3}$$

where V_T is the volt-equivalent of temperature.

This is the Boltzmann's relation of kinetic gas theory. This equation is valid as long as the hole current is small compared with diffusion or drift currents. This condition is called *low-level-injection*.

Under open-circuit condition (i.e., $V = 0$), $p_p = p_{p0}$, $p_n = p_{n0}$ and $V_B = V_0$. Equation (2.3) can be changed into

$$p_{p0} = p_{n0} e^{V_0/V_T} \tag{2.4}$$

Under forward-bias condition, let V be the applied voltage; then the effective barrier voltage

$$V_B = V_0 - V$$

The hole concentration throughout the *P*-side is constant and equal to the thermal equilibrium value ($p_p = p_{p0}$). The hole concentration varies exponentially with distance into the *N*-side.

At $x = 0$, $p_n = p_n(0)$

Equation (2.3) can be changed into

$$p_{p0} = p_n(0) e^{(V_0 - V)/V_T} \tag{2.5}$$

Comparing Eqs (2.4) and (2.5),

$$p_n(0) = p_{n0} e^{V/V_T}$$

This boundary condition is called the *law of the junction*. Substituting this into Eq. (2.2), we get

$$P_n(0) = p_{n0}(e^{V/V_T} - 1) \tag{2.6}$$

The diffusion-hole current in the *N*-side is

$$I_{pn}(x) = -Aq D_p \frac{dp_n(x)}{dx}$$

$$= -Aq D_p \frac{d}{dx}\left[p_{n0} + P_n(0) e^{-x/L_p}\right]$$

$$= \frac{AqD_p P_n(0)}{L_p} e^{-x/L_p}$$

From this equation, it is evident that the injected hole current decreases exponentially with distance.

➤ ***Forward Currents*** The hole current crossing the junction into the *N*-side with $x = 0$ is

$$I_{pn}(0) = \frac{AqD_p\, P_n(0)}{L_p} = \frac{AqD_p p_{n0}}{L_p}(e^{V/V_T} - 1)$$

The electron current crossing the junction into the *P*-side with $x = 0$ is

$$I_{np}(0) = \frac{AqD_n\, N_p(0)}{L_n} = \frac{AqD_n\, n_{p0}}{L_n}(e^{V/V_T} - 1)$$

The total diode current,

$$I = I_{pn}(0) + I_{np}(0) = I_o(e^{V/V_T} - 1)$$

where $I_o = \frac{Aq\, D_p\, p_{n0}}{L_p} + \frac{AqD_n\, n_{p0}}{L_n}$ = reverse saturation current.

If we consider carrier generation and recombination in the space-charge region, the general equation of the diode current is approximately given by

$$I = I_o\left[e^{(V/\eta V_T)} - 1\right]$$

where V = external voltage applied to the diode and η = a constant, 1 for germanium and 2 for silicon.

➤ ***Reverse Saturation Current*** We know that $p_n = \frac{n_i^2}{N_D}$ and $n_p = \frac{n_i^2}{N_A}$. Applying these relationships in the above equation of reverse saturation current, I_o, we get

$$I_o = Aq\left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right] n_i^2$$

where $n_i^2 = A_o T^3\, e^{-E_{Go}/kT} = A_o T^3\, e^{-V_{Go}/V_T}$, where V_{Go} is a voltage which is numerically equal to the forbidden-gap energy E_{Go} in electronvolt.

For a germanium diode, the diffusion constants D_p and D_n vary approximately inversely proportional to T. Hence, the temperature dependence of I_o is

$$I_o = K_1 T^2\, e^{\frac{-V_{Go}}{V_T}}$$

where K_1 is a constant independent of temperature.

For a silicon diode, I_o is proportional to n_i instead of n_i^2. Hence,

$$I_o = K_2 T^{\frac{3}{2}}\, e^{\frac{-V_{Go}}{2V_T}}$$

where K_2 is a constant independent of temperature.

2.4 DIODE EQUATION

The diode-current equation relating the voltage V and current I is given by

$$I = I_o [e^{(V/\eta V_T)} - 1]$$

where I = diode current

I_o = diode reverse saturation current at room temperature

V = external voltage applied to the diode

η = a constant, 1 for germanium and 2 for silicon

Now, $V_T = kT/q = T/11600$, volt-equivalent of temperature, i.e., thermal voltage,

where k = Boltzmann's constant (1.38×10^{-23} J/K)

q = charge of the electron (1.602×10^{-19} C)

T = temperature of the diode junction (K) = (°C + 273)

At room temperature (T = 300 K), V_T = 26 mV. Substituting this value in the current equation, we get

$$I = I_o[e^{(40\ V/\eta)} - 1]$$

Therefore, for a germanium diode, $I = I_o [e^{40V} - 1]$, since $\eta = 1$ for germanium. For a silicon diode, $I = I_o[e^{20V} - 1]$, since $\eta = 2$ for silicon.

If the value of applied voltage is greater than unity then the equation of diode current for germanium,

$$I = I_o (e^{40V})$$

and for silicon, $$I = I_o (e^{20V})$$

When the diode is reverse biased, its current equation may be obtained by changing the sign of the applied voltage V. Thus, the diode current with reverse bias is

$$I = I_o [e^{(-V/\eta V_T)} - 1]$$

If $V >> V_T$ then the term $e^{(-V/\eta V_T)} \ll 1$; therefore, $I \approx -I_o$, termed as reverse saturation current, which is valid as long as the external voltage is below the breakdown value.

EXAMPLE 2.1

When a reverse bias is applied to a germanium *PN* junction diode, the reverse saturation current at room temperature is 0.3 μA. Determine the current flowing in the diode when 0.15 V forward bias is applied at room temperature.

Solution Given, $I_o = 0.3 \times 10^{-6}$ A and $V_F = 0.15$ V

The current flowing through the *PN* diode under forward bias is

$$I = I_o (e^{40V_F} - 1)$$

$$= 0.3 \times 10^{-6} (e^{40 \times 0.15} - 1)$$

$$= 120.73\ \mu A$$

EXAMPLE 2.2

The reverse saturation current of a silicon *PN* junction diode is 10 μA. Calculate the diode current for the forward-bias voltage of 0.6 V at 25 °C.

Solution Given $V_F = 0.6$ V, $T = 273 + 25 = 298$ K

$I_o = 10\ \mu\text{A} = 1 \times 10^{-5}$ A and $\eta = 2$ for silicon

The volt-equivalent of the temperature (T) is

$$V_T = \frac{T}{11{,}600} = \frac{298}{11{,}600} = 25.7 \times 10^{-3}\ \text{V}$$

Therefore, the diode current,

$$I = I_o\left(e^{\frac{V_F}{\eta V_T}} - 1\right)$$

$$= 10^{-5}\left(e^{\frac{0.6}{2 \times 25.7 \times 10^{-3}}} - 1\right) = 1.174\ \text{A}$$

EXAMPLE 2.3

The diode current is 0.6 mA when the applied voltage is 400 mV, and 20 mA when the applied voltage is 500 mV. Determine η. Assume $\frac{kT}{q} = 25$ mV.

Solution

The diode current, $I = I_o\left(e^{\frac{qV}{\eta kT}} - 1\right)$

Therefore, $0.6 \times 10^{-3} = I_o\left(e^{\frac{qV}{\eta kT}} - 1\right) = I_o\, e^{\frac{qV}{\eta kT}}$

$$= I_o \cdot e^{\frac{400}{25\eta}} = I_o \cdot e^{\frac{16}{\eta}} \quad (1)$$

Also, $20 \times 10^{-3} = I_o \cdot e^{\frac{500}{25\eta}} = I_o \cdot e^{\frac{20}{\eta}}$ (2)

Dividing Eq. (2) by Eq. (1), we get

$$\frac{20 \times 10^{-3}}{0.6 \times 10^{-3}} = \frac{I_o \cdot e^{\frac{20}{\eta}}}{I_o \cdot e^{\frac{16}{\eta}}}$$

Therefore, $$\frac{100}{3} = e^{\frac{4}{\eta}}$$

Taking natural logarithms on both sides, we get

$$\log_e \frac{100}{3} = \frac{4}{\eta}$$

$$3.507 = \frac{4}{\eta}$$

Therefore, $$\eta = \frac{4}{3.507} = 1.14$$

EXAMPLE 2.4

Find the voltage at which the reverse current in a germanium *PN* junction diode attains a value of 90 percent of its saturation value at room temperature.

Solution We know that the current of a *PN* junction diode is

$$I = I_o\left(e^{\frac{V}{V_T}} - 1\right)$$

Therefore, $$-0.90\, I_o = I_o\left(e^{\frac{V}{V_T}} - 1\right)$$

where $$V_T = \frac{T}{11{,}600} = 26 \text{ mV}$$

$$-0.9 = \left(e^{\frac{V}{0.026}} - 1\right)$$

$$0.1 = e^{\frac{V}{0.026}}$$

Therefore, $$V = -0.06 \text{ V}$$

EXAMPLE 2.5

Determine the ideal reverse saturation current density in a silicon *PN* junction at $T = 300$ K. Consider the following parameters in the silicon *PN* junction:
$N_A = N_D = 10^{16}$ cm^{-3}, $n_i = 1.5 \times 10^{10}$ cm^{-3}, $D_n = 25$ cm^2/s, $T_{po} = T_{no} = 5 \times 10^{-7}$ s, $D_p = 10$ cm^2/s, $\varepsilon_r = 11.7$. Comment on the result.

Solution Given, $T = 300$ K, $N_A = N_D = 10^{16}$ cm^{-3}, $n_i = 1.5 \times 10^{10}$ cm^{-3}, $D_n = 25$ cm^2/s,
$T_{po} = T_{no} = 5 \times 10^{-7}$ s, $D_p = 10$ cm^2/s

The reverse saturation current is given by

$$I_o = Aq\left[\frac{D_p}{L_p \cdot N_D} + \frac{D_n}{L_n \cdot N_A}\right] n_i^2$$

We know that, $J_o = \dfrac{I_o}{A}$

Therefore, reverse saturation current density is,

$$J_o = q\left[\frac{D_p}{L_p \cdot N_D} + \frac{D_n}{L_n \cdot N_A}\right] n_i^2$$

where $$L_p = \sqrt{D_p \cdot T_{po}} = \sqrt{10 \times 10^{-4} \times 5 \times 10^{-7}} = 2.236 \times 10^{-5}$$

and $$L_n = \sqrt{D_n \cdot T_{no}} = \sqrt{25 \times 10^{-4} \times 5 \times 10^{-7}} = 3.535 \times 10^{-5}$$

Hence, $$J_o = 1.602 \times 10^{-19}\left[\frac{10 \times 10^{-4}}{2.236 \times 10^{-5} \times 10^{22}} + \frac{25 \times 10^{-4}}{3.535 \times 10^{-5} \times 10^{22}}\right](1.5 \times 10^{-16})^2$$

$$= 0.416\ \mu A/s$$

2.5 TEMPERATURE DEPENDENCE ON *V–I* CHARACTERISTICS

The reverse saturation current I_o is temperature dependent while voltage equivalent of temperature V_T is also temperature dependent. Hence, the diode current involving I_o and V_T is temperature dependent. Therefore, the overall diode characteristics depend on the temperature.

The dependence of I_o on temperature T is given by

$$I_o = KT^m e^{-V_{Go}/\eta V_T} \tag{2.7}$$

where K = constant independent of temperature (not the Boltzmann's constant)
m = 2 for Ge and 1.5 for Si
and V_{Go} = forbidden energy gap = 0.785 V for Ge and 1.21 V for Si.

As temperature increases, the value of I_o increases and, hence, the diode current increases. To keep diode current constant, it is necessary to reduce the applied voltage V of the diode.

Let us calculate, the rate of change of the applied voltage to keep the diode current constant. For a constant diode current, $\dfrac{dI}{dT} = 0$. Hence, the change in voltage has to be calculated.

A diode current equation is given by

$$I = I_o\,(e^{V/\eta V_T} - 1)$$

Since $I >> I_o$ for a forward characteristics, we have

$$I = I_o\, e^{V/\eta V_T} \tag{2.8}$$

Substituting Eq. (2.7) into Eq. (2.8), we get

$$I = KT^m\, e^{-V_{Go}/\eta V_T} \cdot e^{V/\eta V_T}$$

$$= KT^m\, e^{(V - V_{Go})/\eta V_T} \tag{2.9}$$

Since $V_T = kT$, where k is Boltzmann's constant,

$$I = KT^m\, e^{(V - V_{Go})/\eta k_T}$$

For a constant diode current, $dI/dT = 0$. Hence, differentiating the above equation with respect to T, we get

$$\frac{dI}{dT} = K\left[mT^{m-1}\, e^{(V-V_{Go})/\eta k_T} + T^m\, e^{(V-VG_o)/\eta k_T} \cdot \frac{d}{dT}\left(\frac{V-V_{Go}}{\eta kT}\right)\right]$$

$$= K\, e^{(V-V_{Go})/\eta k_T}\left[mT^{m-1} + \frac{T^m}{\eta^k}\left(\frac{T\frac{dV}{dT} - (V-V_{Go})\times 1}{T^2}\right)\right]$$

$$= K\, e^{(V-V_{Go})/\eta k_T}\left[\frac{mT^m}{T} + \frac{T^m}{\eta kT^2}\left(T\frac{dV}{dT} - (V-V_{Go}\right)\right]$$

Note that V_{Go} is forbidden energy gap at 0 K and, hence, it is a constant from differentiation point of view.

Taking T^m outside and rearranging the above equation, we get

$$\frac{dI}{dT} = K\, e^{(V-V_{Go})/\eta k_T} \times T^m\left[\frac{m\eta kT + \left(T\frac{dV}{dT} - (V-V_{Go})\right)}{\eta kT}\right]$$

$$= K\, e^{(V-V_{Go})/\eta k_T} \times \frac{T^m}{\eta kT^2}\left[m\eta kT + \left(T\frac{dV}{dT} - (V-V_{Go})\right)\right]$$

Replacing kT with V_T, we get

$$\frac{dI}{dT} = K\, e^{(V-V_{Go})/\eta k_T} \times \frac{T^{m-1}}{\eta V_T}\left[m\eta V_T + \left(T\frac{dV}{dT} - (V-V_{Go})\right)\right]$$

Now, $\frac{dI}{dT} = 0$ for constant diode current. Hence, equating the above equation to zero, we get

$$m\eta V_T + T\frac{dV}{dT} - (V-V_{Go}) = 0$$

$$T\frac{dV}{dT} = V - V_{Go} - m\eta V_T$$

$$\frac{dV}{dT} = \frac{V-(V_{Go} - m\eta V_T)}{T}$$

This is the required change in voltage necessary to keep diode current constant.

Hence, for germanium, at cut-in voltage, $V = V_\gamma = 0.2$ V and with $m = 2$, $\eta = 1$, $T = 30$ K, and $V_{Go} = 0.785$ V in the above equation, we get

$$\frac{dV}{dT} = \frac{0.2 - (0.785 + 2\times 1\times 26\times 10^{-3})}{300} = -2.12 \text{ mV/°C for Ge}$$

The negative sign indicates that the voltage must be reduced at a rate of 2.12 mV per degree change in temperature to keep diode current constant.

Similarly, $\frac{dV}{dT} = -2.3$ mV/°C for Si.

Practically, the value of $\frac{dV}{dT}$ is assumed to be –2.5 mV/°C for either Ge or Si at room temperature.

Thus, $$\frac{dV}{dT} = -2.5 \text{ mV/°C} \tag{2.10}$$

The negative sign indicates that dV/dT decreases with increase in temperature.

2.5.1 Effect of Temperature on Reverse Saturation Current

To study by what rate I_o changes with respect to temperature, consider Eq. (2.7) again. That is,

$$I_o = KT^m \, e^{-V_{Go}/\eta V_T}$$

Taking logarithm on both sides, we get

$$\ln (I_o) = \ln (KT^m \, e^{-V_{Go}/\eta V_T})$$

$$= \ln K + \ln T^m - \frac{V_{Go}}{\eta V_T}$$

$$= \ln K + m \ln T - \frac{V_{Go}}{\eta V_T}$$

Substituting $V_T = kT$, we get

$$\ln (I_o) = \ln K + m \ln T - \frac{V_{Go}}{\eta kT}$$

Differentiating this equation with respect to T, we get

$$\frac{d \ln(I_o)}{dT} = 0 + \frac{m}{T} - \frac{V_{Go}}{\eta k} \cdot \left(\frac{-1}{T^2}\right) = \frac{m}{T} + \frac{V_{Go}}{\eta kT^2}$$

Replacing kT with V_T we have

$$\frac{d[\ln I_o]}{dT} = \frac{m}{T} + \frac{V_{Go}}{\eta T V_T}$$

For germanium, substituting the values of various terms at room temperature, we get

$$\frac{d[\ln I_o]}{dT} = \frac{2}{300} + \frac{0.785}{1 \times 300 \times 26 \times 10^{-3}} = 0.11 \text{ per °C}$$

This indicates that I_o increases by 11 percent per °C rise in temperature. For silicon, we get

$$\frac{d[\ln I_o]}{dT} = 0.08 \text{ per °C}$$

This indicates that I_o increases by 8 percent per °C rise in temperature.

Practically, it is found that the reverse saturation current I_o increases by 7 percent per °C change in temperature for both silicon and germanium diodes. If at T°C is 1 μA then at $(T + 1)$ °C, it becomes 1.07 μA, and so on. From this, it can be concluded that reverse saturation current approximately doubles, i.e., 1.07^{10} for every 10°C rise in temperature.

The above result can be mathematically represented as,

$$I_{02} = \left(2^{\frac{T_2 - T_1}{10}}\right) I_{01} = \left(2^{\frac{\Delta T}{10}}\right) I_{01}$$

where I_{02} is the reverse saturation current at T_2 and I_{01} is the reverse saturation current at T_1.

2.5.2 Temperature Dependence of *V–I* Characteristics

The rise in temperature increases the generation of electron-hole pairs in semiconductors and increases their conductivity. As a result, the current through the *PN* junction diode increases with temperature as given by the diode-current equation,

$$I = I_o \left[e^{(V/\eta VT)} - 1\right]$$

The reverse saturation current I_o of the diode increases approximately 7 percent/°C for both germanium and silicon. Since $(1.07)^{10} \approx 2$, reverse saturation current approximately doubles for every 10°C rise in temperature. Hence, if the temperature is increased at fixed voltage, the current I increases. To bring the current I to its original value, the voltage V has to be reduced. It is found that at room temperature, for either germanium or silicon, $\frac{dV}{dT} \approx -2.5 \text{ mV/°C}$ in order to maintain the current I to a constant value.

At room temperature, i.e., at 300 K, the value of barrier voltage or cut-in voltage is about 0.3 V for germanium and 0.7 V for silicon. The barrier voltage is temperature dependent and it decreases by 2 mV/°C for both germanium and silicon. This fact may be expressed in mathematical form, which is given by

$$I_{o2} = I_{o1} \times 2^{(T_2 - T_1)/10}$$

where I_{o1} = saturation current of the diode at the temperature (T_1), and I_{o2} = saturation current of the diode at the temperature (T_2).

Figure 2.8 shows the effect of increased temperature on the characteristic curve of a *PN* junction diode. A germanium diode can be used up to a maximum of 75°C and a silicon diode, to a maximum of 175°C.

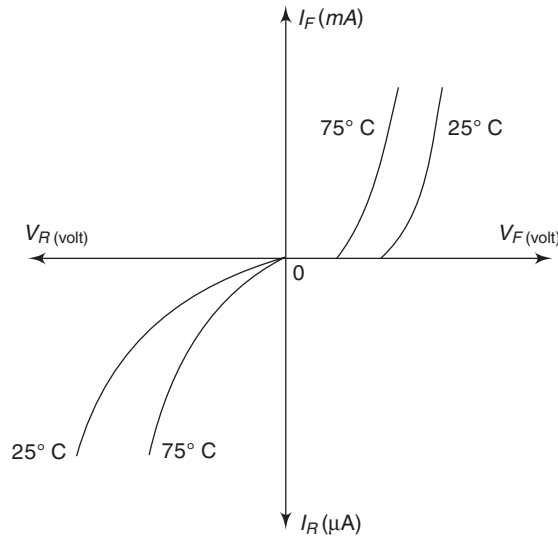


Fig. 2.8 *Effect of temperature on diode characteristics*

EXAMPLE 2.6

The voltage across a silicon diode at room temperature (300 K) is 0.7 volt when 2 mA current flows through it. If the voltage increases to 0.75 V, calculate the diode current (assume $V_T = 26$ mV).

Solution Given, room temperature = 300 K

Voltage across a silicon diode, $V_{D1} = 0.7$ V

Current through the diode, $I_{D1} = 2$ mA

When the voltage increases to 0.75 V, V_{D2} then

$$\frac{I_{D2}}{I_{D1}} = \frac{I_o(e^{V_{D2}/V_T\eta} - 1)}{I_o(e^{V_{D1}/V_T\eta} - 1)} = \frac{e^{0.75/26\times10^{-3}\times2} - 1}{e^{0.7/26\times10^{-3}\times2} - 1} = 2.615$$

Therefore, $I_{D2} = 2.615 \times I_{D1} = 2.615 \times 2 \times 10^{-3} = 5.23$ mA

EXAMPLE 2.7

A silicon diode has a saturation current of 7.5 μA at room temperature of 300 K. Calculate the saturation current at 400 K.

Solution Given, $I_{o1} = 7.5 \times 10^{-6}$ A at $T_1 = 300$ K = 27°C and $T_2 = 400$ K = 127°C

Therefore, the saturation current at 400 K is

$$I_{o2} = I_{o1} \times 2^{(T_2 - T_1)/10}$$
$$= 7.5 \times 10^{-6} \times 2^{(127-27)/10}$$
$$= 7.5 \times 10^{-6} \times 2^{10} = 7.68 \text{ mA}$$

EXAMPLE 2.8

The reverse saturation current of the Ge transistor is 2 μA at room temperature of 25°C and increases by a factor of 2 for each temperature increase of 10°C. Find the reverse saturation current of the transistor at a temperature of 75°C.

Solution Given, $I_{o1} = 2$ μA at $T_1 = 25$°C, $T_2 = 75$°C

Therefore, the reverse saturation current of the transistor at $T_2 = 75$°C is

$$I_{o2} = I_{o1} \times 2^{(T_2 - T_1)/10} = 2 \times 10^{-6} \times 2^{\left(\frac{75-25}{10}\right)}$$
$$= 2 \times 10^{-6} \times 2^5 = 64 \text{ μA}$$

2.6 DIODE RESISTANCE LEVELS (STATIC AND DYNAMIC)

An ideal diode should offer zero resistance in forward bias and infinite resistance in the reverse bias. But in practice, no diode can act as an ideal diode, i.e., an actual diode does not behave as a perfect conductor when forward biased and as a perfect insulator when reverse biased. Let us consider four resistances of the diode (i) dc or static resistance, (ii) ac or dynamic resistance, (iii) average ac resistance, and (iv) reverse resistance.

➤ ***dc or Static Resistance (R_F)*** It is defined as the ratio of the voltage to the current, *V/I*, in the forward-bias characteristics of the *PN* junction diode. In the forward-bias characteristics of the diode as shown in Fig. 2.9, the dc or static resistance (R_F) at the operating point can be determined by using

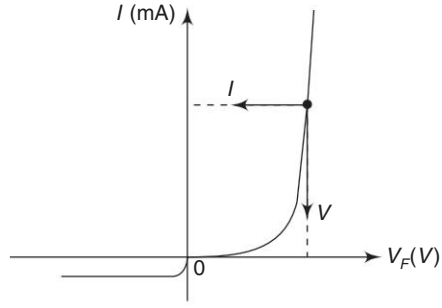


Fig. 2.9 *Forward biasing of a diode*

the corresponding levels of the voltage V and current I, i.e., $R_F = \frac{V}{I}$. Here, the dc resistance is independent of the shape of the characteristics in the region surrounding the point of interest. The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the characteristics above the knee. Hence, the dc resistance will be low when the diode current is high. As the static resistance varies widely with V and I, it is not a useful parameter.

➤ ***ac or Dynamic Resistance (r_f)*** It is defined as the reciprocal of the slope of the volt-ampere characteristics.

$$r_f = \frac{\text{change in voltage}}{\text{resulting change in current}} = \frac{\Delta V}{\Delta I}$$

A straight line drawn tangent to the curve through the quiescent point (Q-point) as shown in Fig. 2.10(a) will define a specific change in voltage and current which may be used to determine the ac or dynamic resistance for this region of the diode characteristics. As shown in Fig. 2.10(b), for a small change in voltage, there will be a corresponding change in current, which is equidistant to either side of the Q-point. Hence, the ac or dynamic resistance is determined as $r_f = \frac{\Delta V}{\Delta I}$.

The derivative of a function at a point is equal to the slope of the tangent line drawn at the point. The Schockley's equation for the forward and reverse-bias regions is defined by

$$I = I_o (e^{V/\eta V_T} - 1)$$

Taking the derivative of the above equation w.r.t. the applied voltage, V, we get

$$\frac{dI}{dV} = \frac{d}{dV}[I_o (e^{V/\eta V_T} - 1)]$$

$$= I_o \left[\frac{1}{\eta V_T} \cdot e^{V/\eta V_T}\right]$$

$$= \frac{I_o e^{V/\eta V_T}}{\eta V_T}$$

$$= \frac{I + I_o}{\eta V_T}$$

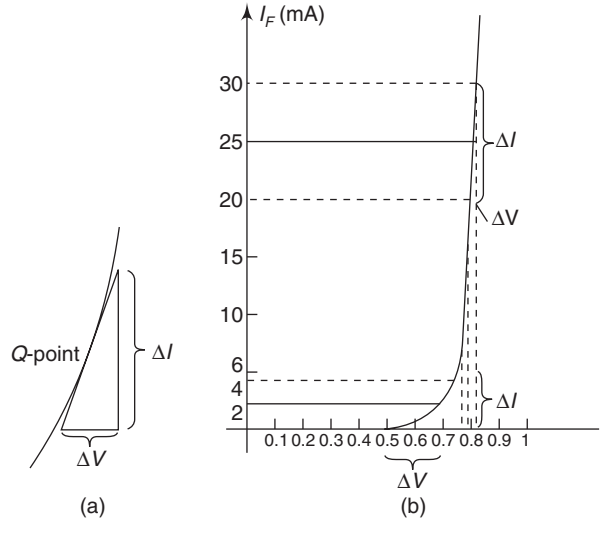


Fig. 2.10 *Dynamic resistance*

Generally, $I >> I_o$ in the vertical-slope section of the characteristics. Therefore,

$$\frac{dI}{dV} \cong \frac{I}{\eta V_T}$$

Therefore,

$$\frac{dV}{dI} = r_f = \frac{\eta V_T}{I}$$

The dynamic resistance varies inversely with current, i.e., $r_f = \dfrac{\eta V_T}{I}$, where $V_T = T/1600$, the volt equivalent of temperature (T) of the diode junction (K) and η is a constant whose value is equal to 1 for germanium and 2 for silicon diodes. At room temperature $V_T = 26$ mV.

The ac resistance of a diode is the sum of bulk resistance r_b and junction resistance r_j. Bulk resistance (r_b) is the sum of ohmic resistance of the *P*- and *N*-type semiconductors.

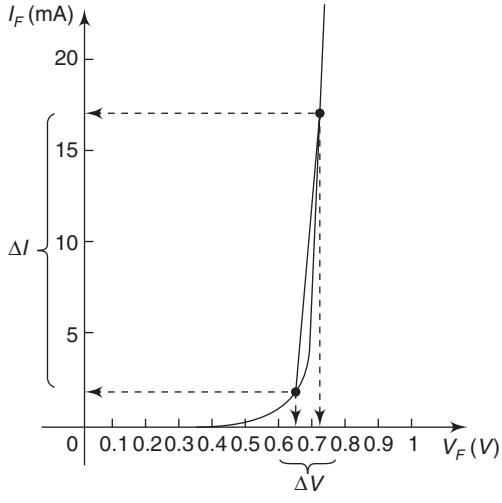


Fig. 2.11 *Average ac resistance*

➤ ***Average ac Resistance*** It is the resistance associated with the device for the region if the input signal is sufficiently large to produce a wide range of the characteristics as shown in Fig. 2.11. Therefore,

$$r_{av} = \left.\frac{\Delta V}{\Delta I}\right|_{\text{point to point}}$$

As with the dc and ac resistance levels, the lower the level of currents used to determine the average, the higher is the resistance level.

➤ ***Reverse Resistance*** It is the resistance offered by the *PN* junction diode under reverse-bias condition. It is very large compared to the forward resistance, which is in the range of several MΩ.

EXAMPLE 2.9

Determine the forward resistance of a *PN* junction diode when the forward current is 5 mA at $T = 300$ K. Assume silicon diode.

Solution Given, for a silicon diode, the forward current, $I = 5$ mA, $T = 300$ K

Forward resistance of a *PN* junction diode, $r_f = \dfrac{\eta V_T}{I}$, where $V_T = \dfrac{T}{11{,}600}$ and $\eta = 2$ for silicon

Therefore,
$$r_f = \frac{2 \times \dfrac{T}{11{,}600}}{5 \times 10^{-3}} = \frac{2 \times 300}{11{,}600 \times 5 \times 10^{-3}} = 10.34\ \Omega$$

EXAMPLE 2.10

Find the value of dc resistance and ac resistance of a germanium junction diode at 25°C with $I_o = 25$ μA and at an applied voltage of 0.2 V across the diode.

Solution Given, $I_o = 25$ μA, $T = 25°C = 298$ K and $V = 0.2$ volt

$$I = I_o\left(e^{\frac{V}{\eta V_T}} - 1\right) = 25 \times 10^{-6}\left(e^{\frac{0.2}{26 \times 10^{-3}}} - 1\right) = 54.79\ \text{mA}$$

dc resistance $R_F = \dfrac{V}{I} = \dfrac{0.2}{54.79 \times 10^{-3}} = 3.65\ \Omega$

For germanium, $\eta = 1, V_T = \dfrac{KT}{q} = 25.71\ \text{mV}$

ac resistance $r_f = \dfrac{\eta V_T}{I} = \dfrac{25.71 \times 10^{-3}}{54.79 \times 10^{-3}} = 0.47\ \Omega$

EXAMPLE 2.11

Calculate the dynamic forward and reverse resistances of a *PN* junction diode when the applied voltage is 0.25 V at $T = 300$ K given $I_o = 2\ \mu\text{A}$.

Solution Given, $V = 0.25$ V, $T = 300$ K, $I_o = 2\ \mu\text{A}$

At $T = 300$ K, $V_T = 26$ mV.

Assuming it to be a silicon diode, $\eta = 2$

Therefore, $I = I_o\left(e^{\frac{V}{\eta V_T}} - 1\right) = 2 \times 10^{-6}\left(e^{\frac{0.25}{2 \times 26 \times 10^{-3}}} - 1\right) = 0.24\ \text{mA}$

$$r_f = \frac{\eta V_T}{I} = \frac{2 \times 26 \times 10^{-3}}{0.24 \times 10^{-3}} = 216.67\ \Omega$$

For a germanium diode, $\eta = 1$

$$I = I_o\left(e^{\frac{V}{\eta V_T}} - 1\right) = 2 \times 10^{-6}\left(e^{\frac{0.25}{26 \times 10^{-3}}} - 1\right) = 0.03\ \text{A}$$

$$r_f = \frac{\eta V_T}{I} = \frac{26 \times 10^{-3}}{0.03} = 0.867\ \Omega$$

Reverse resistance, $\dfrac{V}{I_o} = \dfrac{0.25}{2 \times 10^{-6}} = 125\ \text{k}\Omega$

EXAMPLE 2.12

A *PN* junction diode has a reverse saturation current of 30 μA at a temperature, of 125°C. At the same temperature, find the dynamic resistance for 0.2 V bias in forward and reverse directions.

Solution Given, the reverse saturation current, $I_o = 30 \times 10^{-6}$ A and $V = 0.2$ V

We know that, the dynamic resistance, $r_f = \dfrac{\eta V_T}{I_o e^{V/\eta V_T}}$

Here, $\eta = 1$ for germanium and $V_T = \dfrac{T}{11{,}600} = \dfrac{125 + 273}{11{,}600} = 34.3\ \text{mV}$

Therefore, forward dynamic resistance, $r_f = \dfrac{34.3 \times 10^{-3}}{30 \times 10^{-6}(e^{0.2/34.3 \times 10^{-3}})} = 3.356\ \Omega$

Reverse dynamic resistance, $r_r = \dfrac{\eta V_T}{I_o e^{-V/\eta V_T}} = \dfrac{34.3 \times 10^{-3}}{30 \times 10^{-6}(e^{-0.2/34.3\times10^{-3}})} = 389.5\ \text{k}\Omega$

EXAMPLE 2.13

If two similar germanium diodes are connected back to back and the voltage V is impressed upon, calculate the voltage across each diode and current through each diode. Assume similar value of $I_o = 1\ \mu\text{A}$ for both the diodes and $\eta = 1$.

Solution The arrangement is shown in Fig. 2.12.

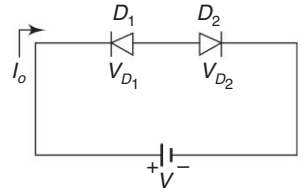


Fig. 2.12

As D_1 is reverse biased, the total current flowing in the circuit is $I_o = 1\ \mu\text{A}$. The diode D_2 is forward biased and its forward current is equal to the reverse current $I_o = 1\ \mu\text{A}$, which can flow as D_1 is reverse biased.

For the diode D_2, $I = I_o = 1\ \mu\text{A}$ and voltage across D_2 is V_{D_2}.

Therefore, $I = I_o[e^{V/\eta V_T} - 1]$

or $I = I_o[e^{V_{D_2}/\eta V_T} - 1]$

Hence, $e^{V_{D_2}/\eta V_T} = 1 + 1 = 2$

$$\frac{V_{D_2}}{\eta V_T} = \ln 2$$

$$V_{D_2} = \eta V_T \times \ln 2 = 1 \times 26 \times 10^{-3} \times 0.6931 = 0.01802\ \text{V}$$

Therefore, $V_{D_1} = V - V_{D_2} = V - 0.01802\ \text{V}$

The current through the diodes D_1 and D_2 is $I = I_0 = 1\ \mu\text{A}$

EXAMPLE 2.14

Determine the forward resistance of a *PN* junction diode, when the forward current is 5 mA at $T = 300$ K. Assume silicon diode.

Solution Given, for a silicon diode, the forward current, $I = 5$ mA. $T = 300$ K

Forward resistance of a *PN* junction diode, $r_f = \dfrac{\eta V_T}{I}$ where $V_T = \dfrac{T}{11{,}600}$ and $\eta = 2$ for silicon

Therefore, $$r_f = \frac{2 \times \dfrac{T}{11{,}600}}{5 \times 10^{-3}} = \frac{2 \times 300}{11{,}600 \times 5 \times 10^{-3}} = 10.34\ \Omega$$

2.7 DIFFUSION CAPACITANCE (C_D)

The capacitance that exists in a forward-biased junction is called a diffusion or storage capacitance (C_D), whose value is usually much larger than C_T, which exists in a reverse-biased junction. This is also defined as the rate of change of injected charge with applied voltage, i.e., $C_D = \dfrac{dQ}{dV}$, where dQ represents the change

in the number of minority carriers stored outside the depletion region when a change in voltage across the diode, dV, is applied.

➤ ***Calculation of C_D*** Let us assume that the P-material in one side of the diode is heavily doped in comparison with the N-side. Since the holes move from the P- to the N-side, the hole current $I \approx I_{pn}(0)$.

The excess minority charge Q existing on the N-side is given by

$$Q = \int_0^\infty AqP_n(0)e^{-x/L_p}dx = \left[\frac{AqP_n(0)e^{-x/L_p}}{-1/L_p}\right]_0^\infty = L_pAqP_n(0)$$

Differentiating the above equation, we get

$$C_D = \frac{dQ}{dV} = AqL_p\frac{d[P_n(0)]}{dV} \tag{2.11}$$

We know that the diffusion hole current in the N-side is $I_{pn}(x) = AqD_pP_n(0)/L_p\, e^{-x/L_p}$. The hole current crossing the junction into the N-side with $x = 0$ is $I_{pn}(0) = \dfrac{AqD_pP_n(0)}{L_p}$.

Therefore, $$I = \frac{AqD_p\,P_n(0)}{L_p}$$

$$P_n(0) = \frac{IL_p}{AqD_p}$$

Differentiating the above equation w.r.t. V, we get

$$\frac{d[P_n(0)]}{dV} = \frac{dI}{dV}\frac{L_p}{AqD_p}$$

Upon substituting in Eq. (2.11), we have

$$C_D = \frac{dQ}{dV} = \frac{dI\,L_p^2}{dV\,D_p}$$

Therefore, $C_D = g\tau$, where $g = \dfrac{dI}{dV}$ is the diode conductance and $\tau = \dfrac{L_p^2}{D_p}$ is the mean lifetime of holes in the N-region.

From the diode-current equation, $g = \dfrac{I}{\eta V_T}$

Therefore, $$C_D = \frac{\tau I}{\eta V_T}$$

where τ is the mean lifetime for holes and electrons.

Diffusion capacitance C_D increases exponentially with forward bias or, alternatively, that it is proportional to diode forward current, I. The values of C_D range from 10 to 1,000 pF, the larger values being associated with the diode carrying a larger anode current, I.

The effect of C_D is negligible for a reverse-biased *PN* junction. As the value of C_D is inversely proportional to frequency, it is high at low frequencies and it decreases with the increase in frequency.

2.8 ENERGY-BAND DIAGRAM OF *PN* JUNCTION DIODE

Consider that a *PN* junction has *P*-type and *N*-type materials in close physical contact at the junction on an atomic scale. Hence, the energy-band diagrams of these two regions undergo relative shift to equalise the Fermi level. The Fermi level E_F should be constant throughout the specimen at equilibrium. The distribution of electrons or holes in allowed energy states is dependent on the position of the Fermi level. If this is not so, electrons on one side of the junction would have an average energy higher than those on the other side, and this causes transfer of electrons and energy until the Fermi levels on the two sides get equalized. However, such a shift does not disturb the relative position of the conduction band, valence band, and Fermi level in any region. Equalization of Fermi levels in the *P* and *N* materials of a *PN* junction is similar to equalization of levels of water in two containers on being joined together.

The energy-band diagram for a *PN* junction is shown in Fig. 2.13, where the Fermi level E_F is closer to the conduction-band edge E_{cn} in the *N*-type material while it is closer to the valence-band edge E_{vp} in the *P*-type material. It is clear that the conduction-band edge E_{cp} in the *P*-type material is higher than the conduction band edge E_{cn} in the *N*-type material. Similarly, the valence-band edge E_{vp} in the *P*-type material is higher than the valence-band edge E_{vn} in the *N*-type material. As illustrated in Fig. 2.13, E_1 and E_2 indicate the shifts in the Fermi level from the intrinsic conditions in the *P* and *N* materials respectively. Then the total shift in the energy level E_0 is given by

$$E_0 = E_1 + E_2 = E_{cp} - E_{cn} = E_{vp} - E_{vn}$$

This energy E_0 (in eV) is the potential energy of the electrons at the *PN* junction, and is equal to qV_0, where V_0 is the contact potential (in volt) or contact difference of potential or the barrier potential.

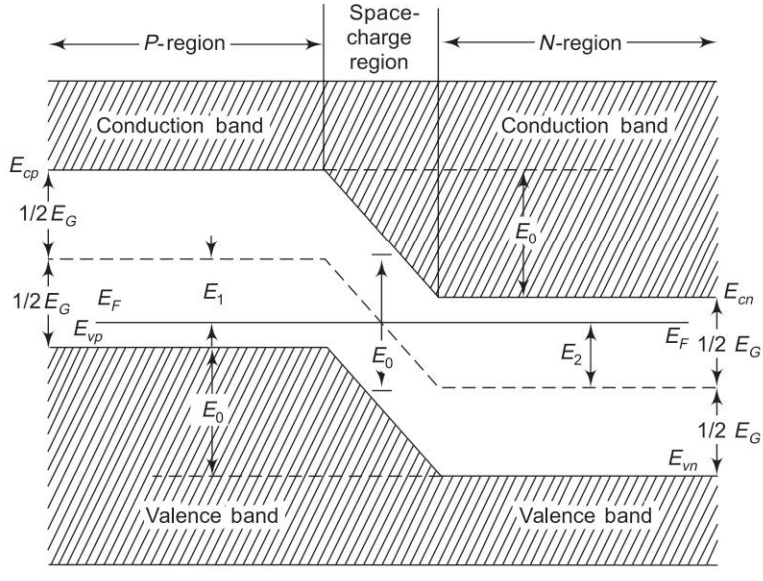


Fig. 2.13 *Energy-band structure*

➤ ***Contact Difference of Potential*** A contact difference of potential exists across an open-circuited *PN* junction. We now proceed to obtain an expression for E_0. From Fig. 2.13, we find that

$$E_F - E_{vp} = \frac{1}{2}E_G - E_1 \tag{2.12}$$

$$E_{cn} - E_F = \frac{1}{2}E_G - E_2 \tag{2.13}$$

Combining Eqs (2.12) and (2.13), we get

$$E_0 = E_1 + E_2 = E_G - (E_{cn} - E_F) - (E_F - E_{vp}) \tag{2.14}$$

We know that

$$np = N_C N_V e^{-E_G/kT}$$

and $$np = n_i^2 \text{ (Mass-action law)}$$

From the above equations, we get

$$E_G = kT \ln \frac{N_C N_V}{n_i^2} \tag{2.15}$$

We know that for an *N*-type material, $E_F = E_C - kT \ln \frac{N_C}{N_D}$. Therefore, from this equation, we get

$$E_{cn} - E_F = kT \ln \frac{N_C}{n_n} = kT \ln \frac{N_C}{N_D} \tag{2.16}$$

Similarly, for a *P*-type material, $E_F = E_V + kT \ln \frac{N_V}{N_A}$. Therefore, from this equation, we get

$$E_F - E_{vp} = kT \ln \frac{N_V}{p_p} = kT \ln \frac{N_V}{N_A} \tag{2.17}$$

Substituting from Eqs (2.15), (2.16), and (2.17) into Eq. (2.14), we get

$$\begin{aligned} E_0 &= kT \left[\ln \frac{N_C N_V}{n_i^2} - \ln \frac{N_C}{N_D} - \ln \frac{N_V}{N_A} \right] \\ &= kT \ln \left[\frac{N_C N_V}{n_i^2} \times \frac{N_D}{N_C} \times \frac{N_A}{N_V} \right] \\ &= kT \ln \frac{N_D N_A}{n_i^2} \end{aligned} \tag{2.18}$$

As $E_0 = qV_0$, the contact difference of potential or barrier voltage is given by

$$V_0 = \frac{kT}{q} \ln \frac{N_D N_A}{n_i^2}$$

In the above equations, E is in electronvolt and k is in electronvolt per degree Kelvin. The contact difference of potential V_0 is expressed in volt and is numerically equal to E_0. From Eq. (2.18), we note that E_0 (hence, V_0) depends upon the equilibrium concentrations and not on the charge density in the transition region.

An alternative expression for E_0 may be obtained by substituting the equations of $n_n \approx N_D$, $p_n = \frac{n_i^2}{N_D}$, $n_n p_p = n_i^2$, $p_p \approx N_A$ and $n_p = \frac{n_i^2}{N_A}$ into Eq. (2.18). Then we get

$$E_0 = kT \ln \frac{p_{p0}}{p_{n0}} = kT \ln \frac{n_{n0}}{n_{p0}} \tag{2.19}$$

where the subscript 0 represents the thermal equilibrium condition.

EXAMPLE 2.15

(a) The resistivities of the *P*-region and *N*-region of a germanium diode are 6 Ω-cm and 4 Ω-cm, respectively. Calculate the contact potential V_0 and potential energy barrier E_0. (b) If the doping densities of both *P* and *N*-regions are doubled, determine V_0 and E_0. Given that $q = 1.602 \times 10^{-19}$ C, $n_i = 2.5 \times 10^{13}/\text{cm}^3$, $\mu_p = 1800\ \text{cm}^2/\text{V-s}$, $\mu_n = 3800\ \text{cm}^2/\text{V-s}$, and $V_T = 0.026$ V at 300 K.

Solution

(a) Resistivity, $\rho = \frac{1}{\sigma} = \frac{1}{N_A q \mu_p} = 6\ \Omega\text{-cm}$

Therefore, $N_A = \frac{1}{6q\mu p} = \frac{1}{6 \times 1.602 \times 10^{-19} \times 1800} = 0.579 \times 10^{15}/\text{cm}^3$

Similarly, $N_D = \frac{1}{4q\mu_n} = \frac{1}{4 \times 1.602 \times 10^{-19} \times 3800} = 0.411 \times 10^{15}/\text{cm}^3$

Therefore, $V_0 = V_T \ln \frac{N_D N_A}{n_i^2} = 0.026 \ln \frac{0.579 \times 0.411 \times 10^{30}}{(2.5 \times 10^{13})^2} = 0.1545$ V

Hence, $E_0 = 0.1545$ eV

(b) $V_0 = 0.026 \ln \frac{2 \times 0.579 \times 10^{15} \times 2 \times 0.411 \times 10^{15}}{(2.5 \times 10^{13})^2} = 0.1906$ V

Therefore, $E_0 = 0.1906$ eV

2.9 ZENER CHARACTERISTICS

When the reverse voltage reaches breakdown voltage in a normal *PN* junction diode, the current through the junction and the power dissipated at the junction will be high. Such an operation is destructive and the diode gets damaged. Whereas diodes can be designed with adequate power dissipation capabilities to operate in the breakdown region. One such diode is known as the Zener diode. The Zener diode is heavily doped than the ordinary diode.

From the *V–I* characteristics of the Zener diode, shown in Fig. 2.14, it is found that the operation of the Zener diode is same as that of an ordinary *PN* diode under forward-biased condition. Whereas under reverse-baised condition, breakdown of the junction occurs. The breakdown voltage

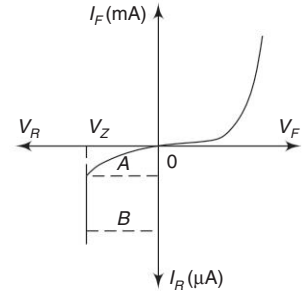


Fig. 2.14 *V–I characteristics of a Zener diode*

depends upon the amount of doping. If the diode is heavily doped, the depletion layer will be thin and, consequently, breakdown occurs at lower reverse voltage and further, the breakdown voltage is sharp. Whereas a lightly doped diode has a higher breakdown voltage. Thus, breakdown voltage can be selected with the amount of doping.

The sharp increasing currents under breakdown conditions are due to the following two mechanisms.

1. Avalanche breakdown
2. Zener breakdown

2.10 AVALANCHE AND ZENER BREAKDOWN

➤ *Avalanche breakdown*

As the applied reverse bias increases, the field across the junction increases correspondingly. Thermally generated carriers, while traversing the junction, acquire a large amount of kinetic energy from this field. As a result, the velocity of these carriers increases. These electrons disrupt covalent bond by colliding with immobile ions and create new electron-hole pairs. These new carriers again acquire sufficient energy from the field and collide with other immobile ions thereby generating further electron-hole pairs. This process is cumulative in nature and results in generation of avalanche of charge carriers within a short time. This mechanism of carrier generation is known as *avalanche multiplication*. This process results in flow of large amount of current at the same value of reverse bias.

➤ *Zener Breakdown*

When the *P*- and *N*-regions are heavily doped, direct rupture of covalent bonds takes place because of the strong electric fields, at the junction of the *PN* diode. The new electron-hole pairs so created increase the reverse current in a reverse-biased *PN* diode. The increase in current takes place at a constant value of reverse bias typically below 6 V for heavily doped diodes. As a result of heavy doping of *P*- and *N*-regions, the depletion-region width becomes very small and for an applied voltage of 6 V or less, the field across the depletion region becomes very high, of the order of 10^7 V/m, making conditions suitable for Zener breakdown. For lightly doped diodes, Zener breakdown voltage becomes high and breakdown is then predominantly by avalanche multiplication. Though Zener breakdown occurs for lower breakdown voltage and avalanche breakdown occurs for higher breakdown voltage, such diodes are normally called Zener diodes.

2.11 ZENER DIODE APPLICATIONS

From the Zener characteristics shown in Fig. 2.14, under the reverse-bias condition, the voltage across the diode remains almost constant although the current through the diode increases as shown in region *AB*. Thus, the voltage across the Zener diode serves as a reference voltage. Hence, the diode can be used as a voltage regulator.

In Fig. 2.15, it is required to provide constant voltage across load resistance R_L, whereas the input voltage may be varying over a range. As shown, Zener diode is reverse biased and as long as the input voltage does not fall below V_Z (Zener breakdown voltage), the voltage across the diode will be constant and hence the load voltage will also be constant.

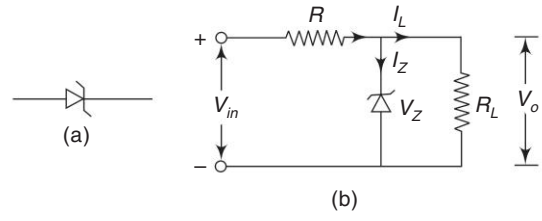


Fig. 2.15 *Zener diode: (a) Circuit symbol (b) As a voltage regulator*

2.12 TUNNEL DIODE CHARACTERISTICS WITH THE HELP OF ENERGY BAND DIAGRAMS

The tunnel diode, or Esaki diode, is a thin-junction diode which exhibits negative resistance under low forward-bias conditions.

An ordinary *PN* junction diode has an impurity concentration of about 1 part in 10^8. With this amount of doping, the width of the depletion layer is of the order of 5 microns. This potential barrier restrains the flow of carriers from the majority carrier side to the minority carrier side. If the concentration of impurity atoms is greatly increased to the level of 1 part in 10^3, the device characteristics are completely changed. The width of the junction barrier varies inversely as the square root of the impurity concentration and, therefore, is reduced from 5 microns to less than 100 Å (10^{-8} m). This thickness is only about 1/50th of the wavelength of visible light. For such thin potential-energy barriers, the electrons will penetrate through the junction rather than surmounting them. This quantum mechanical behavior is referred to as tunneling and hence, these high-impurity-density *PN* junction devices are called tunnel diodes.

The *V–I* characteristic for a typical germanium tunnel diode is shown in Fig. 2.16. It is seen that at first forward current rises sharply as applied voltage is increased, where it would have risen slowly for an ordinary *PN* junction diode (which is shown as dashed line for comparison). Also, reverse current is much larger for comparable back bias than in other diodes due to the thinness of the junction. The interesting portion of the characteristic starts at the point *A* on the curve, i.e., the peak voltage. As the forward bias is increased beyond this point, the forward current drops and continues to drop until point *B* is reached. This is the valley voltage. At *B*, the current starts to increase once again and does so very rapidly as bias is increased further. Beyond this point, the characteristic resembles that of an ordinary diode. Apart from the peak voltage and valley voltage, the other two parameters normally used to specify the diode behaviour are the peak current and the peak-to-valley current ratio, which are 2 mA and 10 respectively, as shown.

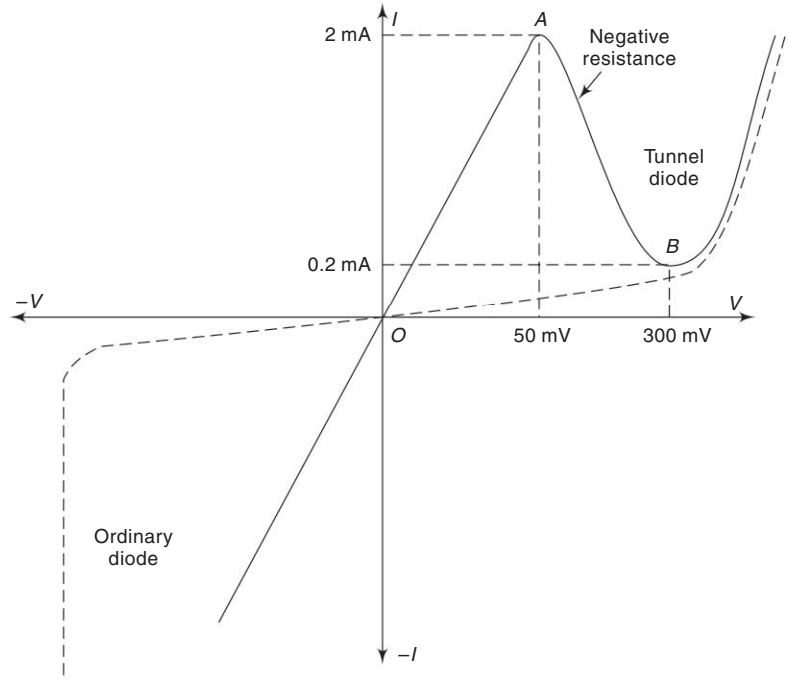


Fig. 2.16 *V–I characteristic of a tunnel diode*

The *V–I* characteristic of the tunnel diode illustrates that it exhibits dynamic resistance between *A* and *B*. Figure 2.17 shows energy level diagrams of the tunnel diode for three interesting bias levels. The shaded areas show the energy states occupied by electrons in the valence band, whereas the cross hatched regions represent energy states in the conduction band occupied by the electrons. The levels to which the energy states are occupied by electrons on either side of the junctions are shown by dotted lines. When the bias is zero, these lines are at the same height. Unless energy is imparted to the electrons from some external source, the energy possessed by the electrons on the *N*-side of the junction is insufficient to permit to climb over the junction barrier to reach the *P*-side. However, quantum mechanics show that there is a finite probability for the electrons to tunnel through the junction to reach the other side, provided there are allowed empty energy states in the *P*-side of the junction at the same energy level. Hence, the forward current is zero.

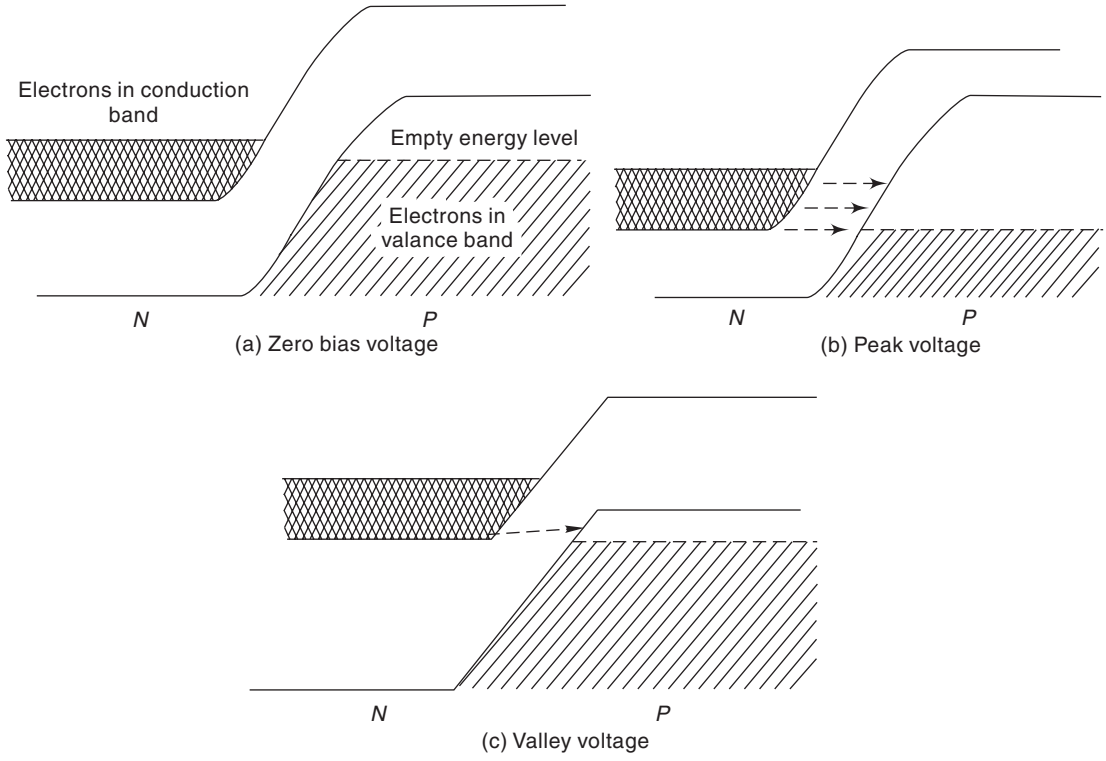


Fig. 2.17 *Energy level diagrams of tunnel diode*

When a small forward bias is applied to the junction, the energy level of the *P*-side is lower as compared with the *N*-side. As shown in Fig. 2.17(b), electrons in the conduction band of the *N*-side see an empty energy level on the *P*-side. Hence, tunnelling from *N*-side to *P*-side takes place. Tunnelling in other directions is not possible because the valence band electrons on the *P*-side are now opposite to the forbidden energy gap on the *N*-side. The energy band diagram shown in Fig. 2.17(b), is for the peak of the diode characteristic.

When the forward bias is raised beyond this point, tunnelling will decrease as shown in Fig. 2.17(c). The energy of the *P*-side is now depressed further, with the result that fewer conduction band electrons on the *N*-side are opposite to the unoccupied *P*-side energy levels. As the bias is raised, forward current drops. This

corresponds to the negative resistance region of the diode characteristic. As forward bias is raised still further, tunneling stops altogether and it behaves as a normal *PN* junction diode.

2.12.1 Equivalent Circuit

The equivalent circuit of the tunnel diode, when biased in the negative resistance region, is as shown in Fig. 2.18(a). In the circuit, R_s is the series resistance and L_s is the series inductance which may be ignored except at highest frequencies. The resulting diode equivalent circuit is thus reduced to parallel combination of the junction capacitance C_j and the negative resistance $-R_n$. Typical values of the circuit components are $R_s = 6\ \Omega$, $L_s = 0.1$ nH, $C_j = 0.6$ pF and $R_n = 75\ \Omega$.

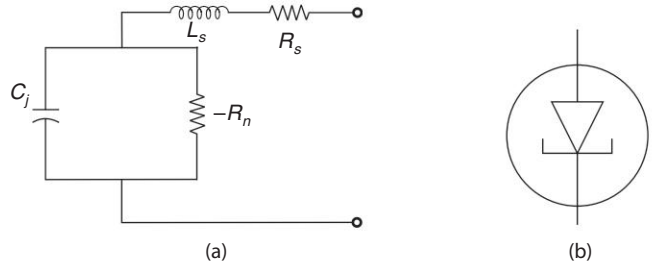


Fig. 2.18 *(a) Equivalent circuit of a tunnel diode (b) Symbol of a tunnel diode*

➤ ***Applications*** Tunnel diode is used as:

1. An ultra-high speed switch with switching speed of the order of *ns* or *ps*
2. Logic memory storage device
3. Microwave oscillator
4. A relaxation oscillator circuit
5. An amplifier

➤ ***Advantages***

1. Low noise
2. Ease of operation
3. High speed
4. Low power

➤ ***Disadvantages***

1. Voltage range over which it can be operated is 1 V or less.
2. Being a two-terminal device, there is no isolation between the input and output circuits.

2.13 VARACTOR DIODE

The varactor, also called a *varicap*, tuning or voltage variable capacitor diode, is a junction diode with a small impurity dose at its junction, which has the useful property that its junction or transition capacitance is easily varied electronically.

When any diode is reverse biased, a depletion region is formed, as seen in Fig. 2.19. The larger the reverse bias applied across the diode, the width of the depletion layer *W* becomes wider. Conversely, by decreasing

the reverse bias voltage, the depletion region width *W* becomes narrower. This depletion region is devoid of majority carriers and acts like an insulator preventing conduction between the *N*- and *P*-regions of the diode, just like a dielectric, which separates the two plates of a capacitor. The varactor diode with its symbol is shown in Fig. 2.20(a).

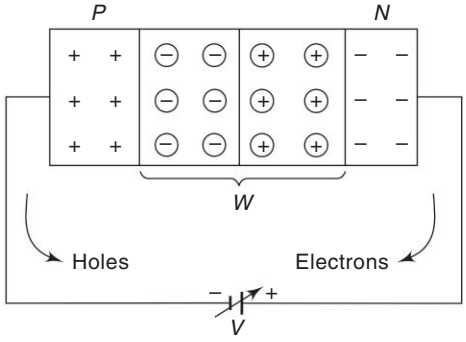


Fig. 2.19 *Depletion region in a reverse-biased PN junction*

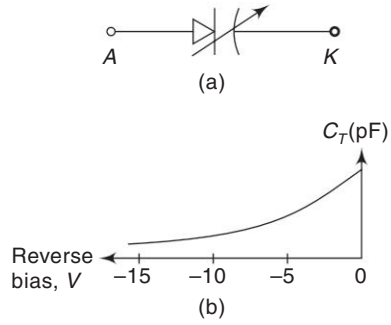


Fig. 2.20 *(a) Circuit symbol of a varactor diode (b) Characteristics of a varactor diode*

As the capacitance is inversely proportional to the distance between the plates ($C_T \propto 1/W$), the transition capacitance C_T varies inversely with the reverse voltage as shown in Fig. 2.20(b). Consequently, an increase in reverse-bias voltage will result in an increase in the depletion region width and a subsequent decrease in transition capacitance C_T. At zero volt, the varactor depletion region *W* is small and the capacitance is large at approximately 600 pF. When the reverse-bias voltage across the varactor is 15 V, the capacitance is 30 pF.

The varactor diodes are used in FM radio, TV receivers, AFC circuits, self-adjusting bridge circuits and adjustable bandpass filters. With improvement in the type of materials used and construction, varactor diodes find application in tuning of *LC* resonant circuit in microwave frequency multipliers and in very low noise microwave parametric amplifiers.

2.14 LIGHT EMITTING DIODE (LED)

The Light Emitting Diode (LED) is a *PN* junction device which emits light when forward biased, by a phenomenon called electroluminescence. In all semiconductor *PN* junctions, some of the energy will be radiated as heat and some in the form of photons. In silicon and germanium, greater percentage of energy is given out in the form of heat and the emitted light is insignificant. In other materials such as gallium phosphide (GaP) or gallium arsenide phosphide (GaAsP), the number of photons of light energy emitted is sufficient to create a visible light source. Here, the charge carrier recombination takes place when electrons from the *N*-side cross the junction and recombine with the holes on the *P*-side.

LED under forward bias and its symbol are shown in Figs 2.21(a) and (b), respectively. When an LED is forward biased, the electrons and holes move towards the junction and recombination takes place. As a result of recombination, the electrons lying in the conduction bands of *N*-region fall into the holes lying in the valence band of a *P*-region. The difference of energy between the conduction band and the valence band is radiated in the form of light energy. Each recombination causes radiation of light energy. Light is generated by recombination of electrons and holes whereby their excess energy is transferred to an emitted photon. The brightness of the emitted light is directly proportional to the forward-bias current.

Figure 2.21(c) shows the basic structure of an LED showing recombination of carriers and emission of light. Here, an *N*-type layer is grown on a substrate and a *P*-type is deposited on it by diffusion. Since carrier recombination takes place in the *P*-layer, it is kept uppermost. The metal anode connections are made at the outer edges of the *P*-layer so as to allow more central surface area for the light to escape. LEDs are manufactured with domed lenses in order to reduce the reabsorption problem. A metal (gold) film is applied to the bottom of the substrate for reflecting as much light as possible to the surface of the device and also to provide cathode connection. LEDs are always encased to protect their delicate wires.

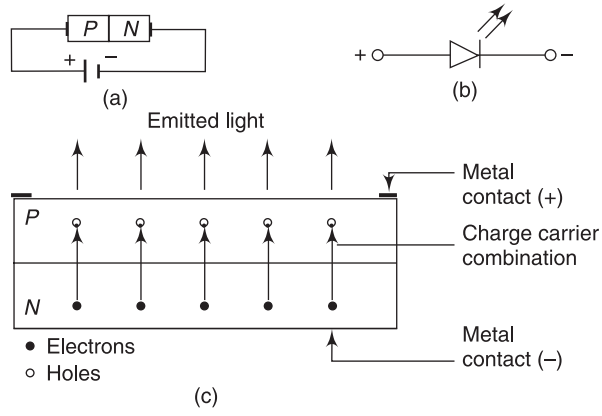


Fig. 2.21 *LED (a) LED under forward bias (b) Symbol (c) Recombinations and emission of light*

The efficiency of generation of light increases with the increases in injected current and with a decrease in temperature. The light is concentrated near the junction as the carriers are available within a diffusion length of the junction.

LEDs radiate different colours such as red, green, yellow, orange, blue and white. Some of the LEDs emit infrared (invisible) light also. The wavelength of emitted light depends on the energy gap of the material. Hence, the colour of the emitted light depends on the type of material used is given as follows.

Gallium arsenide (GaAs) – infrared radiation (invisible)

Gallium phosphide (GaP) – red or green

Gallium arsenide phosphide (GaAsP) – red or yellow

In order to protect LEDs, resistance of 1 kΩ or 1.5 kΩ must be connected in series with the LED. LEDs emit no light when reverse biased. LEDs operate at voltage levels from 1.5 to 3.3 V, with the current of some tens of milliamperes. The power requirement is typically from 10 to 150 mW with a lifetime of 1,00,000 + hours. LEDs can be switched ON and OFF at a very fast speed of 1 ns.

They are used in burglar alarm systems, picture phones, multimeters, calculators, digital meters, microprocessors, digital computers, electronic telephone exchange, intercoms, electronic panels, digital watches, solid state video displays, and optical communication systems. Also, there are two-lead LED lamps which contain two LEDs, so that a reversal in biasing will change the colour from green to red, or vice-versa.

When the emitted light is coherent, i.e., essentially monocromatic, then such a diode is referred to as an Injection Laser Diode (ILD). The LED and ILD are the two main types used as optical sources. ILD has a shorter rise time than LED, which makes the ILD more suitable for wide-bandwidth and high-data-rate applications. In addition, more optical power can be coupled into a fibre with an ILD, which is important for long distance transmission. A disadvantage of the ILD is the strong temperature dependence of the output characteristic curve.

2.15 PIN DIODE

It is composed of three regions. In addition to the usual *N*- and *P*-regions, an intrinsic layer (I-region) is sandwiched between them, to form the *PIN* structure as shown in Fig. 2.22. Being intrinsic, the intermediate layer offers relatively high resistance which gives it two advantages compared to an ordinary *PN* diode. They are (i) decrease in capacitance between *P* and *N* regions as it is inversely proportional to the separation between these regions. It allows a faster response time for the diode. Hence, *PIN* diodes are used at high frequencies (more than 300 MHz), and (ii) possibility of greater electric field between the *P*- and *N*-junctions, so that the charge carriers drift towards their majority carrier side. This enhances faster response of the diode.

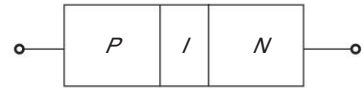


Fig. 2.22 *Structure of PIN diode*

It offers a variable resistance under forward-bias condition as shown in Fig. 2.23. Forward resistance offered is given by $r_{ac} \propto 50/I$, where I is the dc current in mA.

Hence, for large dc currents, the diode will look like a short circuit. In reverse-biased condition, it looks like an open circuit, i.e., it offers an infinite resistance.

It is used as a switching diode for signal frequencies up to GHz range and as an AM modulator of very high frequency signals.

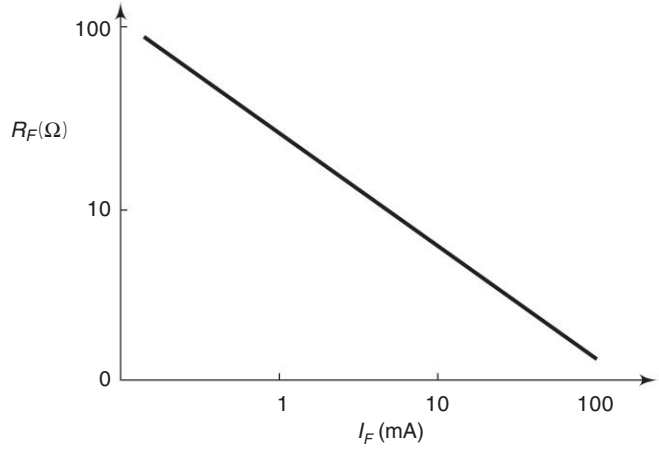


Fig. 2.23 *Variation of forward resistance in a PIN diode*

2.16 PIN PHOTODIODE

It is used for the detection of light at the receiving end in optical communication. It is a three-region reverse-biased junction diode. A layer of intrinsic silicon is sandwitched between heavily doped *P* and *N*-type semiconductor materials. As shown in Fig. 2.24, the depletion region extends almost to the entire intrinsic layer where most of the absorption of light photons take place. The width of the intrinsic layer is large compared to the width of the other two layers. This ensures large absorption of light photons in the depletion region which also forms the absorption region. Light photons incident on the *PIN* photodiode are absorbed in the absorption region which leads to the generation of electron-hole pairs. These charge carriers present in the depletion region drift under the influence of the existing electric field that is set up due to the applied reverse bias. The reverse current flowing in the external circuit increases linearly with the level of illumination.

As the process of drifting is quicker than diffusion, the transit time of the charge carriers is small so that the response time is considerably reduced. The large width of the depletion region results in achieving high quantum efficiency.

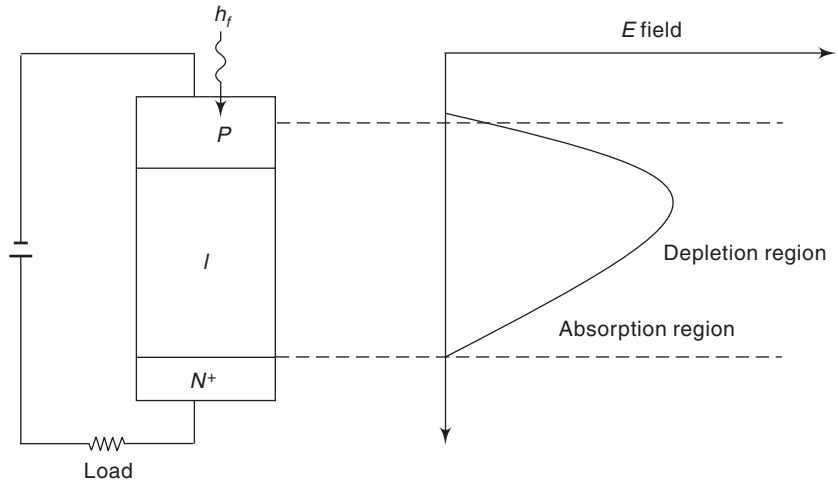


Fig. 2.24 *Structure of PIN photodiode*

REVIEW QUESTIONS

1. What is a *PN* junction? How is it formed?
2. Explain the formation of depletion region in a *PN* junction.
3. Draw the energy-band diagram of a *PN* junction and explain the working of a diode.
4. Sketch the conduction and valence bands before and after diffusion of carriers in a *PN* junction.
5. Explain how a barrier potential is developed at the *PN* junction.
6. Describe the action of *PN* junction diode under forward bias and reverse bias.
7. Show that the *PN* diode works as a rectifier.
8. Explain how unidirectional current flow is possible through a *PN* junction diode.
9. Explain *V–I* characteristics of a *PN* junction diode.
10. Indicate the differences between the characteristics of silicon and germanium diodes and state approximately their cut-in voltages.
11. Explain the following terms in a *PN* junction diode:
    (i) Maximum forward current
    (ii) Peak inverse voltage
    (iii) Maximum power rating
12. Explain the terms (i) static resistance, (ii) dynamic resistance, (iii) junction resistance, and (iv) reverse resistance of a diode.
13. Write the volt–ampere equation for a *PN* diode. Give the meaning of each symbol.
14. What are the factors governing the reverse saturation current in a *PN* junction diode?
15. Determine the forward-bias voltage applied to a silicon diode to cause a forward current of 10 mA and reverse saturation current, $I_o = 25 \times 10^{-7}$ A at room temperature. (*Ans.*: 0.4 V)
16. The reverse saturation current I_o in a germanium diode is 6 μA. Calculate the current flowing through the diode when the applied forward bias voltages are 0.2, 0.3 and 0.4 V at room temperature.
    (*Ans.*: 13.15 mA, 21.5 mA, 28.8 mA)
17. Define the term *transition capacitance* C_T of a *PN* diode.

18. Explain the term *diffusion capacitance* C_D of a forward biased diode.
19. Explain the effect of temperature of a diode.
20. Explain avalanche breakdown and Zener breakdown.
21. Draw the *V–I* characteristic of Zener diode and explain its operation.
22. Show that the Zener diode can be used as a voltage regulator.
23. Show that a reverse biased *PN* junction can be used as a variable capacitor.
24. Explain the principle behind the varactor diode and list out its applications.
25. What is tunnelling?
26. From the energy-band diagram, explain the *V–I* characteristic of a tunnel diode.
27. Draw the equivalent circuit of a tunnel diode and explain it.
28. List the applications of tunnel diode and mention its advantages and disadvantages.
29. Explain the construction of a *PIN* diode and give its two advantages over a *PN* diode.
30. What are the applications of a *PIN* diode?
31. Explain in brief the working of a *PIN* photodiode as an optical detector.
32. Describe with the help of a relevant diagram, the construction of an LED and explain its working.
33. List the applications of an LED.
34. In what respect is an LED different from an ordinary *PN* junction diode?

OBJECTIVE-TYPE QUESTIONS

1. In a *PN* junction, the barrier potential offers opposition to only
(a) holes in *P*-region (b) free electrons in *N*-region
(c) majority carriers in both regions (d) minority carriers in both regions

2. In a forward-biased *PN* junction diode, the sequence of events that best describes the mechanism of current flow is
(a) injection and subsequent diffusion and recombination of minority carriers
(b) injection and subsequent drift and generation of minority carriers
(c) extraction and subsequent diffusion and generation of minority carriers
(d) extraction and subsequent drift and recombination of minority carriers

3. Which of the following is not associated with a *PN* junction?
(a) Junction capacitance (b) Charge storage capacitance
(c) Depletion (d) Channel-length modulation

4. The diffusion capacitance of a *PN* junction
(a) decreases with increasing current and increasing temperature
(b) decreases with decreasing current and increasing temperature
(c) increases with increasing current and increasing temperature
(d) does not depend on current and temperature

5. In an abrupt *PN* junction, the doping concentrations on the *P*-side and *N*-side are $N_A = 9 \times 10^{16}$ /cm^3 and $N_D = 1 \times 10^{16}$ /cm^3 respectively. The *PN* junction is reverse biased and the total depletion width is 3 μm. The depletion width on the *P*-side is
(a) 2.7 μm (b) 0.3 μm (c) 2.25 μm (d) 0.75 μm

6. A *PN* junction has a built-in potential of 0.8 V. The depletion layer width at a reverse bias of 1.2 V is 2 μm . For a reverse bias of 7.2 V, the depletion layer width will be
(a) 4 μm (b) 4.9 μm (c) 8 μm (d) 12 μm

7. A tunnel diode is
(a) a high resistivity *PN* junction diode (b) a slow switching device
(c) an amplifying device (d) a very heavily doped *PN* junction diode.

8. Consider a Ge diode operation at 27°C and just beyond the threshold voltage of Ge. What is the value of *dv/dt*?
(a) –1.9 mV/°C (b) –2.0 mV/°C (c) –2.1 mV/°C (d) –2.3 mV/°C

9. For a *PN* junction, match the type of breakdown with phenomenon
1. Avalanche breakdown
2. Zener breakdown
3. Collision of carriers with crystal ions

A. Collision of carriers with crystal ions
B. Early effect
C. Rupture of covalent bond due to strong electric field

(a) 1-B, 2-A, 3-C (b) 1-c, 2-A, 3-B (c) 1-A, 2-B, 3-C (d) 1-A, 2-C, 3-B

10. A Zener diode works on the principle of
(a) tunnelling of charge carriers across the junction
(b) thermionic emission
(c) diffusion of charge carriers across the junction
(d) doping of charge carriers across the junction

11. Zener diodes have breakdown voltage which
(a) has positive temperature coefficient (b) has negative temperature coefficient
(c) is independent of temperature (d) none of these

12. In a tunnel diode, impurity concentration is of the order of
(a) 1 in 10^3 (b) 1 in 10^5 (c) 1 in 10^7 (d) 1 in 10^9

13. In a Zener diode,
(a) only the *P*-region is heavily doped (b) only the *N*-region is heavily doped
(c) both *P* and *N*-regions are heavily doped (d) both *P* and *N*-regions are lightly doped

14. A Zener diode, when used in voltage stabilization circuits, is biased in
(a) reverse-bias region below the breakdown voltage
(b) reverse breakdown region
(c) forward-bias region
(d) forward-bias constant current mode

15. In a tunnel diode, the width of the depletion layer is of the order of
(a) 0.1 micron (b) 1.0 micron
(c) 0.1 armstrong (d) 100 armstrong

16. A PIN diode is frequently used as a
(a) peak clipper (b) voltage regulator
(c) harmonic generator (d) switching diode for frequencies up to GHz range

17. The following is not an application of varactor diode
(a) Parametric amplifier (b) Frequency tuner
(c) Voltage-controlled oscillator (d) Phase shifter

18. The light emitting diode (LED) emits light of a particular colour because
(a) it is fabricated from a fluorescent material
(b) transition between energy levels of the carriers takes place while crossing the *p-n* junction
(c) heat generated in the diode is converted into light
(d) the bandgap of the semiconductor material used in the fabrication of the diode is equal to the energy h_v of the light photon

19. The photoconductive cell most popularly used for visible light spectrum uses
(a) Ge (b) Si (c) GaAs (d) cadmium sulphide

20. The colour of the emitted light while using gallium phosphide GaP in a light emitting diode is
(a) invisible (b) red or green (c) red or yellow (d) green or yellow

21. LEDs operate at voltage levels from
(a) 10 to 150 V (b) 1 to 15 V (c) 1.5 to 3.3 V (d) 15 to 33 V

3 Rectifiers and Regulators

3.1 INTRODUCTION

All electronic circuits need dc power supply either from battery or power-pack units. Transformer, rectifier, filters and regulators form the basic building blocks of a linear mode power supply. A transformer supplies ac voltage at the required level. This bidirectional ac voltage is converted into a unidirectional pulsating dc using a rectifier. The unwanted ripple contents of this pulsating dc are removed by a filter to get pure dc voltage. The output of the filter is fed to a regulator which gives a steady dc output independent of load variations and input supply fluctuations. This chapter mainly discusses the operation and characteristics of different types of rectifiers, filters and regulators.

3.2 LINEAR MODE POWER SUPPLY

The basic building blocks of the linear power supply are shown in Fig. 3.1. A transformer supplies ac voltage at the required level. This bidirectional ac voltage is converted into a unidirectional pulsating dc using a rectifier. The unwanted ripple contents of this pulsating dc are removed by a filter to get pure dc voltage. The output of the filter is fed to a regulator which gives a steady dc output independent of load variations and input supply fluctuations.

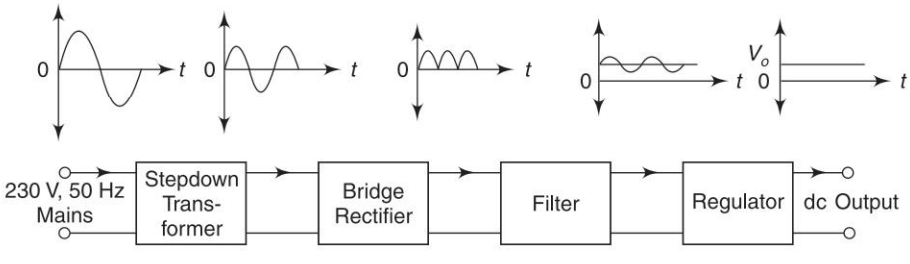


Fig. 3.1 *Basic building block of linear-mode power supply*

3.2.1 Requirements of Linear-Mode Power Supply

1. The most important consideration in designing a power supply is the dc voltage at the output. It should be able to give minimum operable dc voltage at the rated current.

2. It should be able to furnish the maximum current needed for the unit, maintaining the voltage constant. In other words, the regulation of the power supply should be good.
3. The ac ripple should be low.
4. The power supply should be protected in the event of short-circuit on the load side.
5. Overvoltage (spike and surges) protection must be incorporated.
6. The response of the power supply to temperature changes should be minimum.

3.3 RECTIFIERS

Rectifier is defined as an electronic device used for converting ac voltage into unidirectional voltage. A rectifier utilizes unidirectional conduction device like a vacuum diode or *PN* junction diode. Rectifiers are classified depending upon the period of conduction as half-wave rectifier and full-wave rectifier.

3.3.1 Half-wave Rectifier

It converts an ac voltage into a pulsating dc voltage using only one half of the applied ac voltage. The rectifying diode conducts during one half of the ac cycle only. Figure 3.2 shows the basic circuit and waveforms of a half-wave rectifier (HWR).

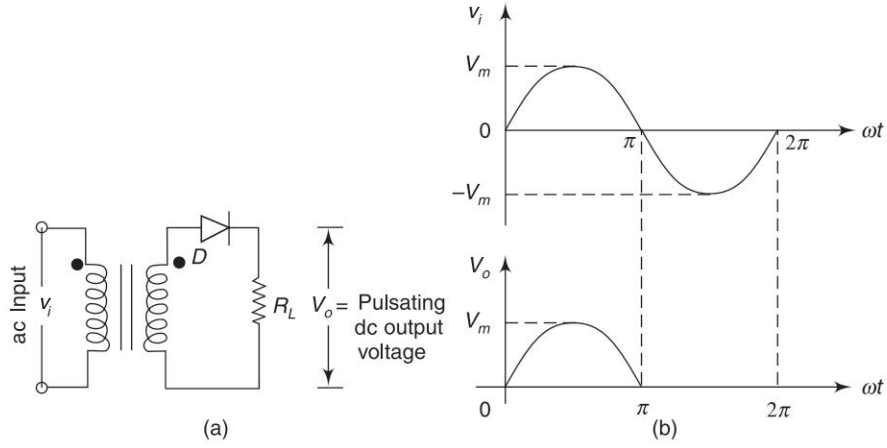


Fig. 3.2 *(a) Basic structure of a half-wave rectifier (b) Input output waveforms of half-wave rectifier*

Let v_i be the voltage to the primary of the transformer and given by the equation

$$v_i = V_m \sin \omega t;\ V_m >> V_\gamma$$

where V_γ is the cut-in voltage of the diode. During the positive half cycle of the input signal, the anode of the diode becomes more positive with respect to the cathode and hence, the diode *D* conducts. For an ideal diode, the forward voltage drop is zero. So, the whole input voltage will appear across the load resistance, R_L.

During negative half cycle of the input signal, the anode of the diode becomes negative with respect to the cathode and hence, diode *D* does not conduct. For an ideal diode, the impedance offered by the diode is infinity. So the whole input voltage appears across diode *D*. Hence, the voltage drop across R_L is zero.

➤ ***Ripple Factor (Γ)*** The ratio of rms value of ac component to the dc component in the output is known as ripple factor (Γ).

$$\Gamma = \frac{\text{rms value of ac component}}{\text{dc value of component}} = \frac{V_{r,\text{rms}}}{V_{\text{dc}}}$$

where $V_{r,\text{rms}} = \sqrt{V_{\text{rms}}^2 - V_{\text{dc}}^2}$.

Therefore, $$\Gamma = \sqrt{\left(\frac{V_{\text{rms}}}{V_{\text{dc}}}\right)^2 - 1}$$

The rms value of a continuous-time periodic waveform is the square root of the ratio of the square of that waveform function to the time period T, as given by

$$V_{\text{rms}} = \sqrt{\frac{\text{Square of the area under the curve for one cycle}}{\text{Time period}}}$$

$$= \sqrt{\frac{1}{T}\int_0^T [x(t)]^2\, dt}$$

The average or the dc content of the voltage across the load is given by

$$V_{av} = V_{\text{dc}} = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin \omega t\, d(\omega t) + \int_{\pi}^{2\pi} 0.d(\omega t)\right]$$

$$= \frac{V_m}{2\pi}[-\cos \omega t]_0^{\pi} = \frac{V_m}{\pi}$$

Therefore, $$I_{\text{dc}} = \frac{V_{\text{dc}}}{R_L} = \frac{V_m}{\pi R_L} = \frac{I_m}{\pi}$$

If the values of diode forward resistance (r_f) and the transformer secondary winding resistance (r_s) are also taken into account, then

$$V_{\text{dc}} = \frac{V_m}{\pi} - I_{\text{dc}}(r_s + r_f)$$

$$I_{\text{dc}} = \frac{V_{\text{dc}}}{(r_s + r_f) + R_L} = \frac{V_m}{\pi(r_s + r_f + R_L)}$$

The rms voltage at the load resistance can be calculated as

$$V_{\text{rms}} = \left[\frac{1}{2\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t\, d(\omega t)\right]^{\frac{1}{2}}$$

$$= V_m\left[\frac{1}{4\pi}\int_0^{\pi} (1 - \cos 2\omega t)\, d\omega t\right]^{\frac{1}{2}} = \frac{V_m}{2}$$

Therefore, $$\Gamma = \sqrt{\left[\frac{V_m/2}{V_m/\pi}\right]^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21$$

From this expression, it is clear that the amount of ac present in the output is 121% of the dc voltage. So the half-wave rectifier is not practically useful in converting ac into dc.

➤ ***Efficiency (η)*** The ratio of dc output power to ac input power is known as rectifier efficiency (η).

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{\frac{(V_{dc})^2}{R_L}}{\frac{(V_{rms})^2}{R_L}} = \frac{\left(\frac{V_m}{\pi}\right)^2}{\left(\frac{V_m}{2}\right)^2} = \frac{4}{\pi^2} = 0.406 = 40.6\%$$

The maximum efficiency of a half-wave rectifier is 40.6%.

➤ ***Peak Inverse Voltage (PIV)*** It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half cycle. For half-wave rectifier, PIV is V_m.

➤ ***Transformer Utilization Factor (TUF)*** In the design of any power supply, the rating of the transformer should be determined. This can be done with a knowledge of the dc power delivered to the load and the type of rectifying circuit used.

$$\text{TUF} = \frac{\text{dc power delivered to the load}}{\text{ac rating of the transformer secondary}}$$

$$= \frac{P_{dc}}{P_{ac}\ \text{rated}}$$

In the half-wave rectifying circuit, the rated voltage of the transformer secondary is $V_m/\sqrt{2}$, but the actual rms current flowing through the winding is only $\frac{I_m}{2}$, not $I_m/\sqrt{2}$.

$$\text{TUF} = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{2}} = \frac{\frac{V_m^2}{\pi^2}\frac{1}{R_L}}{\frac{V_m}{\sqrt{2}}\frac{V_m}{2R_L}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

The TUF for a half-wave rectifier is 0.287.

- **Form Factor**

$$\text{Form factor} = \frac{\text{rms value}}{\text{average value}} = \frac{V_m/2}{V_m/\pi} = \frac{\pi}{2} = 1.57$$

- **Peak Factor**

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}} = \frac{V_m}{V_m/2} = 2$$

EXAMPLE 3.1

A half-wave rectifier, having a resistive load of 1000 Ω, rectifies an alternating voltage of 325 V peak value and the diode has a forward resistance of 100 Ω. Calculate (a) peak, average and rms values of current (b) dc power output (c) ac input power and (d) efficiency of the rectifier.

Solution

(a) Peak value of current, $I_m = \dfrac{V_m}{r_f + R_L} = \dfrac{325}{100 + 1000} = 295.45 \text{ mA}$

Average current, $I_{dc} = \dfrac{I_m}{\pi} = \dfrac{295.45}{\pi} \text{ mA} = 94.046 \text{ mA}$

RMS value of current, $I_{rms} = \dfrac{I_m}{2} = \dfrac{295.45}{2} = 147.725 \text{ mA}$

(b) The dc power output, $P_{dc} = I_{dc}^2 \times R_L$

$= (94.046 \times 10^{-3})^2 \times 1000 = 8.845 \text{ W}$

(c) The ac input power, $P_{ac} = (I_{rms})^2 \times (r_f + R_L)$

$= (147.725 \times 10^{-3})^2 (1100) = 24 \text{ W}$

(d) Efficiency of rectification, $\eta = \dfrac{P_{dc}}{P_{ac}} = \dfrac{8.845}{24} = 36.85\%$.

EXAMPLE 3.2

A half-wave rectifier is used to supply 24 V dc to a resistive load of 500 Ω and the diode has a forward resistance of 50 Ω. Calculate the maximum value of the ac voltage required at the input.

Solution Average value of load current,

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{24}{500} = 48 \text{ mA}$$

Maximum value of load current, $I_m = \pi \times I_{dc} = \pi \times 48 \text{ mA} = 150.8 \text{ mA}$

Therefore, maximum ac voltage required at the input,

$$V_m = I_m \times (r_f + R_L) = 150.8 \times 10^{-3} \times 550 = 82.94 \text{ V}$$

EXAMPLE 3.3

An ac supply of 230 V is applied to a half-wave rectifier circuit through transformer of turns ratio 5:1. Assume the diode is an ideal one. The load resistance is 300 Ω. Find (a) dc output voltage, (b) PIV, (c) maximum, and (d) average values of power delivered to the load.

Solution

(a) The transformer secondary voltage = $\frac{230}{5} = 46$ V

Maximum value of secondary voltage, $V_m = \sqrt{2} \times 46 = 65$ V

Therefore, dc output voltage, $V_{dc} = \frac{V_m}{\pi} = \frac{65}{\pi} = 20.7$ V

(b) PIV of a diode $V_m = 65$ V

(c) Maximum value of load current, $I_m = \frac{V_m}{R_L} = \frac{65}{300} = 0.217$ A

Therefore, maximum value of power delivered to the load,

$$P_m = I_m^2 \times R_L = (0.217)^2 \times 300 = 14.1 \text{ W}$$

(d) The average value of load current, $I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.7}{300} = 0.069$ A

Therefore, average value of power delivered to the load,

$$P_{dc} = I_{dc}^2 \times R_L = (0.069)^2 \times 300 = 1.43 \text{ W}$$

EXAMPLE 3.4

An HWR has a load of 3.5 kΩ. If the diode resistance and secondary coil resistance together have a resistance of 800 Ω and the input voltage has a signal voltage of peak value 240 V. Calculate

(a) peak, average and rms values of current flowing
(b) dc power output
(c) ac power input
(d) efficiency of the rectifier

Solution Load resistance in an HWR, $R_L = 3{,}500\ \Omega$

Diode resistance and secondary coil resistance, $r_f + r_s = 800\ \Omega$

Peak value of input voltage = 240 V

(a) Peak value of current, $I_m = \frac{V_m}{r_s + r_f + R_L} = \frac{240}{4300} = 55.81$ mA

Average value of current, $I_{dc} = \frac{I_m}{\pi} = \frac{55.81 \times 10^{-3}}{\pi} = 17.77$ mA

The rms value of current, $I_{rms} = \frac{I_m}{2} = \frac{55.81 \times 10^{-3}}{2} = 27.905$ mA

(b) The dc power output is

$$P_{dc} = (I_{dc})^2 R_L = (17.77 \times 10^{-3})^2 \times 3500 = 1.105 \text{ W}$$

(c) The ac power input is

$$P_{ac} = (I_{rms})^2 \times (r_f + R_L) = (27.905 \times 10^{-3})^2 \times 4300 = 3.348 \text{ W}$$

(d) Efficiency of the rectifier is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{1.105}{3.348} \times 100 = 33\%$$

EXAMPLE 3.5

An HWR circuit supplies 100 mA dc to a 250 Ω load. Find the dc output voltage, PIV rating of a diode and the rms voltage for the transformer supplying the rectifier.

Solution Given $I_{dc} = 100$ mA, $R_L = 250\ \Omega$

(a) The dc output voltage,

$$V_{dc} = I_{dc} \times R_L = 100 \times 10^{-3} \times 250 = 25 \text{ V}$$

(b) The maximum value of secondary voltage,

$$V_m = \pi \times V_{dc} = \pi \times 25 = 78.54 \text{ V}$$

(c) PIV rating of a diode, $V_m = 78.54$ V

(d) The rms voltage for the transformer supplying the rectifier,

$$V_{rms} = \frac{V_m}{2} = \frac{78.54}{2} = 39.27 \text{ V}$$

EXAMPLE 3.6

A voltage of 200 cos ωt is applied to HWR with load resistance of 5 kΩ. Find (a) the maximum dc current component, (b) rms current, (c) ripple factor, (d) TUF and (e) rectifier efficiency.

Solution Given applied voltage = 200 cosωt, $V_m = 200$ V, $R_L = 5$ kΩ

(a) *To find dc current:*

$$I_m = \frac{V_m}{R_L} = \frac{200}{5 \times 10^3} = 40 \text{ mA}$$

Therefore,
$$I_{dc} = \frac{I_m}{\pi} = \frac{40 \times 10^{-3}}{\pi} = 12.73 \text{ mA}$$

(b) *To find rms current:*

$$I_{rms} = \frac{I_m}{2} = \frac{40 \times 10^{-3}}{2} = 20 \text{ mA}$$

(c) *Ripple factor:*
$$\Gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{20 \times 10^{-3}}{12.73 \times 10^{-3}}\right)^2 - 1} = 1.21$$

(d) *To determine TUF:*

$$\text{TUF} = \frac{P_{dc}}{P_{ac(\text{rated})}}$$

$$P_{dc} = I_{dc}^2 R_L = (12.73 \times 10^{-3})^2 \times 5 \times 10^3 = 0.81 \text{ W}$$

$$P_{ac\,(rated)} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{2} = \frac{200}{\sqrt{2}} \times \frac{40 \times 10^{-3}}{2} = 2.828$$

Therefore, $$\text{TUF} = \frac{P_{dc}}{P_{ac\,(rated)}} = \frac{0.81}{2.828} = 0.2863$$

(e) *Rectifier efficiency:* $$\eta = \frac{P_{dc}}{P_{ac}}$$

$$P_{dc} = 0.81 \text{ W}$$

$$P_{ac} = I_{rms}^2 R_L = (20 \times 10^{-3})^2 \times 5 \times 10^3 = 2 \text{ W}$$

Therefore, $$\eta = \frac{P_{dc}}{P_{ac}} \times 100 = \frac{0.81}{2} \times 100 = 40.5\%$$

EXAMPLE 3.7

A diode has an internal resistance of 20 Ω and 1000 Ω load from a 110 V rms source of supply. Calculate (a) the efficiency of rectification and (b) the percentage regulation from no load to full load.

Solution Given $r_f = 20\ \Omega$, $R_L = 1000\ \Omega$ and V_{rms} (secondary) = 110 V

(a) The half-wave rectifier uses a single diode.

Therefore, $$V_m = \sqrt{2}\, V_{rms}(\text{secondary}) = \sqrt{2} \times 110 = 155.56 \text{ V}$$

$$I_m = \frac{V_m}{r_f + R_L} = \frac{155.56}{20 + 1000} = 0.1525 \text{ A}$$

$$I_{dc} = \frac{I_m}{\pi} = \frac{0.1525}{\pi} = 0.04854 \text{ A}$$

$$V_{dc} = I_{dc} R_L = 0.04854 \times 1000 = 48.54 \text{ V}$$

$$P_{dc} = V_{dc} I_{dc} = 48.54 \times 0.04854 = 2.36 \text{ W}$$

$$P_{ac} = I_{rms}^2 (r_f + R_L) = \left(\frac{I_m}{2}\right)^2 (r_f + R_L) \qquad \left(\text{since } I_{rms} = \frac{I_m}{2} \text{ for half-wave}\right)$$

$$= \left(\frac{0.1525}{2}\right)^2 (20 + 1000) = 5.93 \text{ W}$$

Efficiency, $$\eta = \frac{P_{dc}}{P_{ac}} \times 100 = \frac{2.36}{5.93} \times 100 = 39.7346\%$$

(b) Percentage of line regulation $$= \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{\frac{V_m}{\pi} - V_{dc}}{V_{dc}} \times 100$$

$$= \frac{\frac{155.56}{\pi} - 48.54}{48.54} \times 100 = 2\%$$

EXAMPLE 3.8

Show that maximum dc output power $P_{dc} = V_{dc} \times I_{dc}$ in a half-wave single-phase circuit occurs when the load resistance equals diode resistance r_f.

Solution For a half-wave rectifier,

$$I_m = \frac{V_m}{r_f + R_L}$$

$$I_{dc} = \frac{I_m}{\pi} = \frac{V_m}{\pi (r_f + R_L)}$$

and $$V_{dc} = I_{dc} \times R_L$$

Therefore, $$P_{dc} = V_{dc} \times I_{dc} = I_{dc}^2 R_L = \frac{V_m^2 R_L}{\pi^2 (r_f + R_L)^2}$$

For this power to be maximum,

$$\frac{dP_{dc}}{dR_L} = 0$$

$$\frac{d}{dR_L}\left[\frac{V_m^2 R_L}{\pi^2 (r_f + R_L)^2}\right] = \frac{V_m^2}{\pi^2}\left[\frac{(r_f + R_L)^2 - R_L \times 2(r_f + R_L)}{(r_f + R_L)^4}\right] = 0$$

$$(r_f + R_L)^2 - 2R_L(r_f + R_L) = 0$$

$$r_f^2 + 2r_f R_L + R_L^2 - 2r_f R_L - 2R_L^2 = 0$$

$$r_f^2 - R_L^2 = 0$$

$$R_L^2 = r_f^2$$

Thus, the power output is maximum if $R_L = r_f$

EXAMPLE 3.9

The transformer of a half-wave rectifier has a secondary voltage of 30 V_{rms} with a winding resistance of 10 Ω. The semiconductor diode in the circuit has a forward resistance of 100 Ω. Calculate (a) no load dc voltage (b) dc output voltage at $I_L = 25$ mA (c) % regulation at $I_L = 25$ mA (d) ripple voltage across the load (e) ripple frequency (f) ripple factor (g) dc power output and (h) PIV of the semiconductor diode.

Solution

V_{rms} (secondary) $= 30$ V, $r_s = 10$ Ω, $r_f = 100$ Ω

$$V_m = \sqrt{2} \times V_{rms} = \sqrt{2} \times 30 = 42.4264 \text{ V}$$

(a) $$V_{dc} = \frac{V_m}{\pi} = \frac{42.4264}{\pi} = 13.5047 \text{ V}$$

(b) $$I_L = I_{dc} = 25 \text{ mA}$$

$$V_{dc} = I_{dc} R_L = \frac{I_m}{\pi} R_L = \frac{V_m}{\pi (r_f + r_s + R_L)} \times R_L$$

Here, $$R_L = \frac{V_{dc}}{I_{dc}}$$

Therefore, $$V_{dc} = \frac{V_m}{\pi\left(r_f + r_s + \frac{V_{dc}}{I_{dc}}\right)} \times \frac{V_{dc}}{I_{dc}}$$

$$V_{dc} = \frac{42.426\, V_{dc}}{\pi\left(100 + 10 + \frac{V_{dc}}{25 \times 10^{-3}}\right)} \times \frac{1}{25 \times 10^{-3}}$$

$$V_{dc}\,(110 + 40V_{dc}) = 540.1897\, V_{dc}$$

$$V_{dc} = \frac{540.1897 - 110}{40} = 10.7547 \text{ V}$$

(c) Percentage of regulation $$= \frac{V_{dc(NL)} - V_{dc(FL)}}{V_{dc(FL)}} \times 100 = \frac{13.5047 - 10.7547}{10.7547} \times 100 = 25.569\%$$

(d) $$I_m = \frac{V_m}{r_f + r_s + R_L}, \text{ where } R_L = \frac{V_{dc}}{I_{dc}} = \frac{10.7547}{25 \times 10^{-3}} = 430.188 \text{ V}$$

Therefore, $$I_m = \frac{42.4264}{100 + 10 + 430.188} = 0.07854 \text{ A}$$

$$I_{rms} = \frac{I_m}{2} = 0.03927 \text{ A}$$

$$\Gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{0.03927}{25 \times 10^{-3}}\right)^2 - 1} = 1.21$$

Ripple voltage $\Gamma \times V_{dc} = 1.21 \times 10.7547 = 13.02791$ V

(e) Ripple frequency, $f = 50$ Hz

(f) Γ = ripple factor = 1.21

(g) $P_{dc} = V_{dc} I_{dc} = 10.7547 \times 25 \times 10^{-3} = 0.2688$ W

(h) PIV $= V_m = 42.4264$ V

3.3.2 Full-wave Rectifier

It converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. It uses two diodes of which one conducts during one half-cycle while the other diode conducts during the other half-cycle of the applied ac voltage. There are two types of full-wave rectifiers, viz., (i), full-wave rectifier with centre tapped transformer, and (ii) full-wave rectifier without transformer (bridge rectifier).

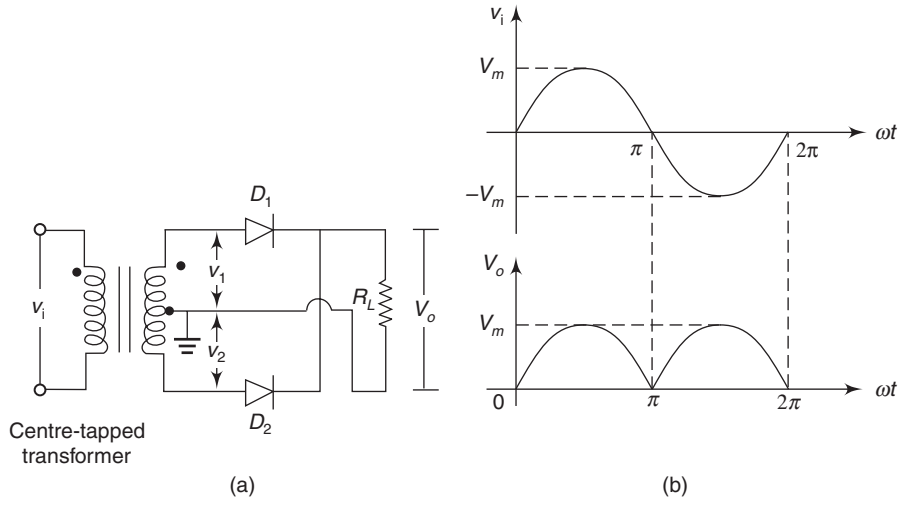


Fig. 3.3 *Full-wave rectifier*

Figure 3.3 shows the basic circuit and waveforms of full-wave rectifier with a center tap transformer. During positive half of the input signal, the anode of the diode D_1 becomes positive and at the same time, the anode of diode D_2 becomes negative. Hence, D_1 conducts and D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.

During the negative half-cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage.

➤ *Ripple Factor (Γ)*

$$\Gamma = \sqrt{\left(\frac{V_{\text{rms}}}{V_{\text{dc}}}\right)^2 - 1}$$

The average voltage or dc voltage available across the load resistance is

$$V_{\text{dc}} = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \, \text{d}(\omega t)$$

$$= \frac{V_m}{\pi}[-\cos \omega t]_0^{\pi} = \frac{2V_m}{\pi}$$

$$I_{\text{dc}} = \frac{V_{\text{dc}}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \text{ and } I_{\text{rms}} = \frac{I_m}{\sqrt{2}}$$

If the diode forward resistance (r_f) and the transformer secondary winding resistance (r_s) are included in the analysis, then

$$V_{\text{dc}} = \frac{2V_m}{\pi} - I_{\text{dc}}\,(r_s + r_f)$$

$$I_{dc} = \frac{V_{dc}}{(r_s + r_f) + R_L} = \frac{2V_m}{\pi(r_s + r_f + R_L)}$$

The rms value of the voltage at the load resistance is

$$V_{rms} = \sqrt{\left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \, d(\omega t)\right]} = \frac{V_m}{\sqrt{2}}$$

Therefore,
$$\Gamma = \sqrt{\left(\frac{V_m/\sqrt{2}}{2V_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.482$$

➤ ***Efficiency (η)*** The ratio of dc output power to ac input power is known as rectifier efficiency (η).

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{(V_{dc})^2/R_L}{(V_{rms})^2/R_L} = \frac{\left[\frac{2V_m}{\pi}\right]^2}{\left[\frac{V_m}{\sqrt{2}}\right]^2}$$

$$= \frac{8}{\pi^2} = 0.812 = 81.2\%$$

The maximum efficiency of a full-wave rectifier is 81.2%.

➤ ***Transformer Utilization Factor (TUF)*** The average TUF in a full-wave rectifying circuit is determined by considering the primary and secondary windings separately and it gives a value of 0.693.

- **Form Factor**

$$\text{Form factor} = \frac{\text{rms value of the output voltage}}{\text{average value of the output voltage}} = \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

- **Peak Factor**

$$\text{Peak factor} = \frac{\text{peak value of the output voltage}}{\text{rms value of the output voltage}} = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$$

Peak inverse voltage for full-wave rectifier is $2V_m$ because the entire secondary voltage appears across the non-conducting diode.

EXAMPLE 3.10

A 230 V, 60 Hz voltage is applied to the primary of a 5:1 step-down, centre-tap transformer use in a full-wave rectifier having a load of 900 Ω. If the diode resistance and secondary coil resistance together has a resistance of 100 Ω, determine (a) dc voltage across the load, (b) dc current flowing through the load, (c) dc power delivered to the load, (d) PIV across each diode, (e) ripple voltage and its frequency and (f) rectification efficiency.

Solution The voltage across the two ends of secondary $= \frac{230}{5} = 46$ V

Voltage from centre tapping to one end, $V_{rms} = \frac{46}{2} = 23$ V

(a) The dc voltage across the load, $V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 23 \times \sqrt{2}}{\pi} = 20.7$ V

(b) The dc current flowing through the load, $I_{dc} = \frac{V_{dc}}{(r_s + r_f + R_L)} = \frac{20.7}{1000} = 20.7$ mA

(c) The dc power delivered to the load,

$$P_{dc} = (I_{dc})^2 \times R_L = (20.7 \times 10^{-3})^2 \times 900 = 0.386 \text{ W}$$

(d) PIV across each diode $= 2V_m = 2 \times 23 \times \sqrt{2} = 65$ V

(e) Ripple voltage, $V_{r,rms} = \sqrt{(V_{rms})^2 - (V_{dc})^2}$

$$= \sqrt{(23)^2 - (20.7)^2} = 10.05 \text{ V}$$

Frequency of ripple voltage $= 2 \times 60 = 120$ Hz

(f) Rectification efficiency, $\eta = \frac{P_{dc}}{P_{ac}} = \frac{(V_{dc})^2/R_L}{(V_{rms})^2/R_L} = \frac{(V_{dc})^2}{(V_{rms})^2}$

$$= \frac{(20.7)^2}{(23)^2} = \frac{428.49}{529} = 0.81$$

Therefore, percentage of rectification efficiency = 81%

EXAMPLE 3.11

A full-wave rectifier has a centre-tap transformer of 100-0-100 V and each one of the diodes is rated at $I_{max} = 400$ mA and $I_{av} = 150$ mA. Neglecting the voltage drop across the diodes, determine (a) the value of load resistor that gives the largest dc power output, (b) dc load voltage and current, and (c) PIV of each diode.

Solution

(a) We know that the maximum value of current flowing through the diode for normal operation should not exceed 80% of its rated current.

Therefore, $I_{max} = 0.8 \times 400 = 320$ mA

The maximum value of the secondary voltage,

$$V_m = \sqrt{2} \times 100 = 141.4 \text{ V}$$

Therefore, the value of load resistor that gives the largest dc power output

$$R_L = \frac{V_m}{I_{max}} = \frac{141.4}{320 \times 10^{-3}} = 442 \ \Omega$$

(b) The dc (load) voltage, $V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 141.4}{\pi} = 90$ V

The dc load current, $I_{dc} = \frac{V_{dc}}{R_L} = \frac{90}{442} = 0.204$ A

(c) PIV of each diode = $2V_m = 2 \times 141.4 = 282.8$ V

EXAMPLE 3.12

A full-wave rectifier delivers 50 W to a load of 200 Ω. If the ripple factor is 1%, calculate the ac ripple voltage across the load.

Solution The dc power delivered to the load,

$$P_{dc} = \frac{V_{dc}^2}{R_L}$$

Therefore, $V_{dc} = \sqrt{P_{dc} \times R_L} = \sqrt{50 \times 200} = 100$ V

The ripple factor, $\Gamma = \frac{V_{ac}}{V_{dc}}$

i.e., $0.01 = \frac{V_{ac}}{100}$

Therefore, the ac ripple voltage across the load, $V_{ac} = 1$ V

EXAMPLE 3.13

In a full-wave rectifier, the transformer rms secondary voltage from centre tap to each end of the secondary is 50 V. The load resistance is 900 Ω. If the diode resistance and transformer secondary winding resistance together has a resistance of 100 Ω, determine the average load current and rms value of load current?

Solution Voltage from centre tapping to one end, $V_{rms} = 50$ V

Maximum load current, $I_m = \frac{V_m}{r_s + r_f + R_L} = \frac{V_{rms} \times \sqrt{2}}{r_s + r_f + R_L} = \frac{70.7}{1000} = 70.7$ mA

Average load current, $I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 70.7 \times 10^{-3}}{\pi} = 45$ mA

RMS value of load current, $I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{70.7 \times 10^{-3}}{\sqrt{2}} = 50$ mA

EXAMPLE 3.14

A full-wave rectifier circuit uses two silicon diodes with a forward resistance of 20 Ω each. A dc voltmeter connected across the load of 1 kΩ reads 55.4 volt. Calculate

(a) I_{rms}
(b) average voltage across each diode
(c) ripple factor and
(d) transformer secondary voltage rating.

Solution Given $V_{dc} = 55.4$ V and $R_L = 1$ kΩ

(a) $$I_{dc} = \frac{V_{dc}}{(r_f + R_L)} = \frac{55.4}{20 + 1000} = 54.31 \text{ mA}$$

We know that $$I_{dc} = \frac{2I_m}{\pi} \text{ and } I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$I_m = I_{dc} \times \frac{\pi}{2} = 54.31 \times 10^{-3} \times \frac{\pi}{2} = 85.31 \text{ mA}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{85.31 \times 10^{-3}}{\sqrt{2}} = 60.32 \text{ mA}$$

(b) The average voltage across each silicon diode will be 0.72 V.

(c) *To find ripple factor Γ*

$$\Gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{60.32 \times 10^{-3}}{54.31 \times 10^{-3}}\right) - 1} = 0.4833$$

To find transformer secondary voltage rating

We know that, $$V_{dc} = \frac{2V_m}{\pi} - I_{dc}\,(r_s + r_f)$$

where r_f is the diode forward resistance and r_s is the transformer secondary winding resistance.

$$55.4 = \frac{2V_m}{\pi} - 54.31 \times 10^{-3} \times 20 = \frac{2V_m}{\pi} - 1.086$$

$$56.49 = \frac{2V_m}{\pi}$$

Therefore, $$V_m = 56.49 \times \frac{\pi}{2} = 88.73 \text{ V}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{88.73}{\sqrt{2}} = 62.74 \text{ V}$$

Hence, transformer secondary voltage rating is 65 V.

3.3.3 Bridge Rectifier

The need for a centre-tapped transformer in a full-wave rectifier is eliminated in the bridge rectifier. As shown in Fig. 3.4, the bridge rectifier has four diodes connected to form a bridge. The ac input voltage is applied to the diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge.

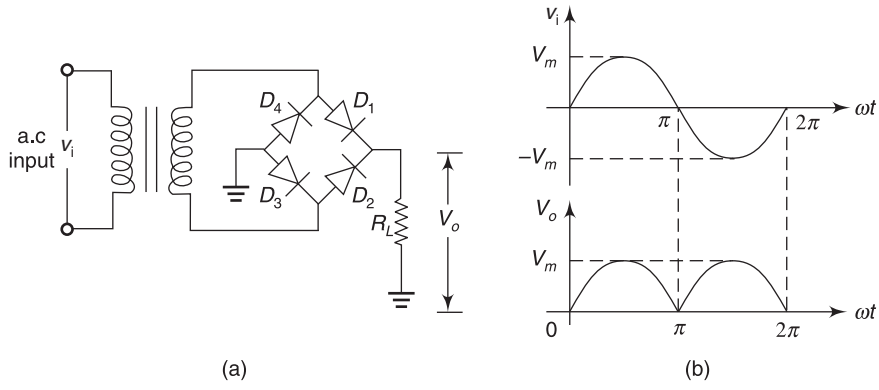


Fig. 3.4 *Bridge rectifier*

For the positive half-cycle of the input ac voltage, diodes D_1 and D_3 conduct, whereas diodes D_2 and D_4 do not conduct. The conducting diodes will be in series through the load resistance R_L. So the load current flows through R_L.

During the negative half-cycle of the input ac voltage, diodes D_2 and D_4 conduct, whereas diodes D_1 and D_3 do not conduct. The conducting diode D_2 and D_4 will be in series through the load R_L and the current flows through R_L in the same direction as in the previous half-cycle. Thus, a bidirectional wave is converted into an unidirectional one.

The average values of output voltage and load current for bridge rectifier are the same as for a centre-tapped full-wave rectifier. Hence,

$$V_{dc} = \frac{2V_m}{\pi} \quad \text{and} \quad I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi}$$

If the values of the transformer secondary winding resistance (r_s) and diode forward resistance (r_f) are considered in the analysis, then

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc}\,(r_s + r_f)$$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi\,(r_s + r_f + R_L)}$$

The maximum efficiency of a bridge rectifier is 81.2% and the ripple factor is 0.48. The PIV is V_m.

- **Advantages of the Bridge Rectifier** In the bridge rectifier, the ripple factor and efficiency of the rectification are the same as for the full-wave rectifier. The PIV across either of the non-conducting diodes is equal to the peak value of the transformer secondary voltage, V_m. The bulky centre-tapped transformer is not required. Transformer utilization factor is considerably high. Since the current flowing in the transformer secondary is purely alternating, the TUF increases to 0.812, which is the main reason for the popularity of a bridge rectifier. The bridge rectifiers are used in applications allowing floating output terminals, i.e., no output terminal is grounded.

The bridge rectifier has only one disadvantage that it requires four diodes as compared to two diodes for centre-tapped full-wave rectifier. But the diodes are readily available at cheaper rate in the market. Apart

from this, the PIV rating required for the diodes in a bridge rectifier is only half of that for a centre tapped full-wave rectifier. This is a great advantage, which offsets the disadvantage of using extra two diodes in a bridge rectifier.

➤ ***Comparison of Rectifiers*** The comparison of rectifiers is given in Table 3.1.

Table 3.1 *A comparison of rectifiers*

Particulars	Type of rectifier		
	Half-wave	Full-wave	Bridge
No. of diodes	1	2	4
Maximum efficiency	40.6%	81.2%	81.2%
V_{dc} (no load)	V_m/π	$2V_m/\pi$	$2V_m/\pi$
Average current/diode	I_{dc}	$I_{dc}/2$	$I_{dc}/2$
Ripple factor	1.21	0.48	0.48
Peak inverse voltage	V_m	$2V_m$	V_m
Output frequency	f	$2f$	$2f$
Transformer utilisation factor	0.287	0.693	0.812
Form factor	1.57	1.11	1.11
Peak factor	2	$\sqrt{2}$	$\sqrt{2}$

EXAMPLE 3.15

A 230 V, 50 Hz voltage is applied to the primary of a 4:1 step-down transformer used in a bridge rectifier having a load resistance of 600 Ω. Assuming the diodes to be ideal, determine (a) dc output voltage, (b) dc power delivered to the load, (c) PIV, and (d) output frequency.

Solution

(a) The rms value of the transformer secondary voltage,

$$V_{\text{rms (secondary)}} = \frac{V_{\text{rms(primary)}}}{\text{Turns ratio}} = \frac{230}{4} = 57.5$$

The maximum value of the secondary voltage

$$V_m = \sqrt{2} \times 57.5 = 81.3 \text{ V}$$

Therefore, dc output voltage,

$$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 81.3}{\pi} = 52 \text{ V}$$

(b) The dc power delivered to the load,

$$P_{dc} = \frac{V_{dc}^2}{R_L} = \frac{52^2}{600} = 2.704 \text{ W}$$

(c) PIV across each diode = $V_m = 81.3$ V

(d) Output frequency = $2 \times 50 = 100$ Hz

EXAMPLE 3.16

In a bridge rectifier, the transformer is connected to 200 V, 60 Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diode is ideal, find (a) V_{dc} (b) I_{dc} and (c) PIV.

Solution Given in a bridge rectifier, input voltage = 200 V, 60 Hz and turns ratio = 11:1

(a) *To find the voltage across load,* V_{dc}

$$V_{dc} = \frac{2V_m}{\pi}$$

where $$V_m = \sqrt{2}\, V_{rms(secondary)}$$

$$V_{rms(secondary)} = \frac{V_{rms(primary)}}{\text{Turns ratio}} = \frac{200}{11} = 18.18 \text{ V}$$

Therefore, $$V_m = 18.18 \times \sqrt{2} = 25.7 \text{ V}$$

Hence, $$V_{dc} = \frac{2 \times 25.7}{\pi} = 16.36 \text{ V}$$

(b) *To find* I_{dc}

Assuming that $R_L = 600\ \Omega$, then

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{16.36}{600} = 27.26 \text{ mA}$$

(c) *To find PIV*

$$PIV = V_m = 25.7 \text{ V}$$

EXAMPLE 3.17

A bridge rectifier uses four identical diodes having forward resistance of 5 Ω and the secondary voltage is 30 V(rms). Determine the dc output voltage for $I_{dc} = 200$ mA and value of the output ripple voltage.

Solution Given, transformer secondary resistance = 5 Ω

Secondary voltage $V_{rms} = 30$ V, $I_{dc} = 200$ mA

Since only two diodes of the bridge rectifier circuit will conduct during positive of negative half cycle of the input signal, the diode forward resistance, $r_f = 2 \times 5\ \Omega = 10\ \Omega$.

We know that,

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc}\,(r_f + r_s) \text{ where } V_m = \sqrt{2}V_{rms} = \sqrt{2} \times 30 \text{ V}$$

Therefore, $$V_{dc} = \frac{2 \times \sqrt{2} \times 30}{\pi} - 200 \times 10^{-3}\,(10 + 5) = 24 \text{ V}$$

$$\text{Ripple factor} = \frac{\text{rms value of ripple at the output}}{\text{average value of output voltage}}$$

Therefore, $$0.48 = \frac{\text{rms value of ripple at the output}}{24}$$

Hence, rms value of ripple at the output = $0.48 \times 24 = 11.52$ V

EXAMPLE 3.18

In a full-wave rectifier, the required dc voltage is 9 V and the diode drop is 0.8 V. Calculate ac rms input voltage required in centre-tapped full-wave rectifier and bridge rectifier circuits.

Solution (a) The dc voltage across the load of the center tapped full-wave rectifier circuit,

$$V_{dc} = 9 = \frac{2V_m}{\pi} - 0.8 = \frac{2\sqrt{2} \times V_{rms}}{\pi} - 0.8$$

where V_{rms} is the rms input voltage from centre tapping to on end. That is,

$$9.8 = \frac{2\sqrt{2}\, V_{rms}}{\pi}$$

Therefore, $$V_{rms} = \frac{9.8\,\pi}{2\sqrt{2}} = 10.885 \text{ V}$$

Hence, the voltage across the two ends of the secondary = $2 \times 10.885 = 21.77$ V

(b) In the bridge rectifier, $V_{dc} = 9 = \frac{2\sqrt{2}V_{rms}}{\pi} - 2 \times 0.8$

Therefore, the voltage across two ends of secondary, $V_{rms} = \frac{10.6\,\pi}{2\sqrt{2}} = 11.77$ V

3.4 HARMONIC COMPONENTS IN A RECTIFIER CIRCUIT

The term *harmonic* is defined as "a sinusoidal component of a periodic waveform or quantity possessing a frequency, which is an integral multiple of the fundamental frequency." By definition, a perfect sine wave has no harmonics, except fundamental component at one frequency. Harmonics are present in waveforms that are not perfect sine waves due to distortion from nonlinear loads. The French mathematician Fourier discovered that a distorted waveform can be represented as a series of sine waves, with each being an integer multiple of the fundamental frequency and each with a specific magnitude.

That is, the harmonic frequencies are integer multiples [2, 3, 4,….] of the fundamental frequency. For example, the second harmonic on a 50 Hz system is 2×50 or 100 Hz. The sixth harmonic in a 50 Hz system, or the fifth harmonic in a 60 Hz system is 300 Hz. There are a number of different types of equipment that may experience faulty operations or failures due to high harmonic voltage and/ or current levels. The amount of the harmonic voltage and current levels that a system can tolerate is dependent on the equipment and the source.

The sum of the fundamental and all the harmonics is called the ***Fourier series***. This series can be viewed as a spectrum analysis where the fundamental frequency and the harmonic component are identified.

The result of such an analysis for the current waveform of a half-wave rectifier circuit using a single diode is given by

$$i = I_m \left[\frac{1}{\pi} + \frac{1}{2} \sin \omega t - \frac{2}{\pi} \sum_{k=2,4,6} \frac{\cos k\omega t}{(k+1)(k-1)} \right]$$

The angular frequency of the power supply is the lowest angular frequency present in the above expression. All the other terms are the even harmonics of the power frequency.

The full-wave rectifier consists of two half-wave rectifier circuits, arranged in such a way that one circuit conducts during one half cycle and the second circuit operates during the second half cycle. Therefore, the currents are functionally related by the expression $i_1(\alpha) = i_2(\alpha + \pi)$. Thus, the total current of the full-wave rectifier is $i = i_1 + i_2$ as expressed by

$$i = I_m \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{\substack{k=\text{even} \\ k \neq 0}} \frac{\cos k\omega t}{(k+1)(k-1)} \right]$$

From the above equation, it can be seen that the fundamental angular frequency is eliminated and the lowest frequency is the second harmonic term 2ω. This is the advantage that the full-wave rectifier presents in filtering of the output. Additionally, the current pulses in the two halves of the transformer winding are in such directions that the magnetic cycles formed through the iron core is essentially that of the alternating current. This avoids any dc saturation of the transformer core that could give rise to additional harmonics at the output.

3.5 FILTERS

The output of a rectifier contains dc component as well as ac component. Filters are used to minimise the undesirable ac, i.e., ripple leaving only the dc component to appear at the output.

The ripple in the rectified wave being very high, the factor being 48% in the full-wave rectifier; majority of the applications which cannot tolerate this, will need an output which has been further processed.

Figure 3.5 shows the concept of a filter, where the full-wave rectified output voltage is applied at its input. The output of a filter is not exactly a constant dc level. But it also contains a small amount of ac component. Some important filters are

(i) Inductor filter
(ii) Capacitor filter
(iii) LC or L-section filter
(iv) CLC or π-type filter

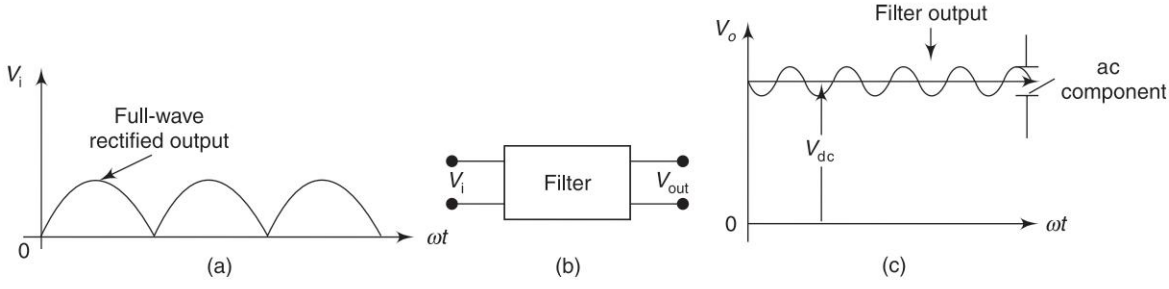


Fig. 3.5 *Concept of a filter*

3.6 INDUCTOR FILTER

Figure 3.6 shows the inductor filter. When the output of the rectifier passes through an inductor, it blocks the ac component and allows only the dc component to reach the load.

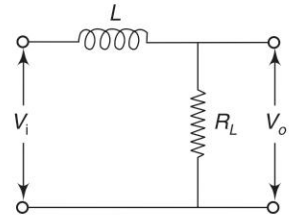


Fig. 3.6 *Inductor filter*

The ripple factor of the inductor filter is given by

$$\Gamma = \frac{R_L}{3\sqrt{2}\,\omega L}$$

It shows that the ripple factor will decrease when L is increased and R_L is decreased. Clearly, the inductor filter is more effective only when the load current is high (small R_L). The larger value of the inductor can reduce the ripple and at the same time the output dc voltage will be lowered as the inductor has a higher dc resistance.

The operation of the inductor filter depends on its well known fundamental property to oppose any change of current passing through it.

To analyse this filter for a full-wave, the Fourier series can be written as

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left[\frac{1}{3}\cos 2\,\omega t + \frac{1}{15}\cos 4\omega t + \frac{1}{35}\cos 6\,\omega t + \cdots\right]$$

The dc component is $\frac{2V_m}{\pi}$.

Assuming the third and higher terms contribute little output, the output voltage is

$$V_o = \frac{2V_m}{2\pi} - \frac{4V_m}{3\pi}\cos 2\,\omega t$$

The diode, choke and transformer resistances can be neglected since they are very small as compared with R_L. Therefore, the dc component of current $I_m = \frac{V_m}{R_L}$. The impedance of series combination of L and R_L at 2ω is

$$Z = \sqrt{R_L^2 + (2\,\omega L)^2} = \sqrt{R_L^2 + 4\omega^2\,L^2}$$

Therefore, for the ac component,

$$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2\,L^2}}$$

Therefore, the resulting current i is given by,

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi}\frac{\cos(2\,\omega t - \varphi)}{\sqrt{R_L^2 + 4\omega^2\,L^2}}$$

where $\varphi = \tan^{-1}\left(\frac{2\omega L}{R_L}\right)$.

The ripple factor, which can be defined as the ratio of the rms value of the ripple to the dc value of the wave, is

$$\Gamma = \frac{\frac{4V_m}{3\pi\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}} = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

If $\frac{4\omega^2 L^2}{R_L^2} >> 1$, then a simplified expression for Γ is

$$\Gamma = \frac{R_L}{3\sqrt{2}\,\omega L}$$

In case, the load resistance is infinity, i.e., the output is an open circuit, then the ripple factor is

$$\Gamma = \frac{2}{3\sqrt{2}} = 0.471$$

This is slightly less than the value of 0.482. The difference being attributable to the omission of higher harmonics as mentioned. It is clear that the inductor filter should only be used where R_L is consistently small.

EXAMPLE 3.19

Calculate the value of inductance to use in the inductor filter connected to a full-wave rectifier operating at 60 Hz to provide a dc output with 4% ripple for a 100 Ω load.

Solution We know that the ripple factor for inductor filter is $\Gamma = \frac{R_L}{3\sqrt{2}\,\omega L}$

Therefore, $$0.04 = \frac{100}{3\sqrt{2}\,(2\pi \times 60 \times L)} = \frac{0.0625}{L}$$

$$L = \frac{0.0625}{0.04} = 1.5625 \text{ H}$$

3.7 CAPACITOR FILTER

An inexpensive filter for light loads is found in the capacitor filter which is connected directly across the load, as shown in Fig. 3.7(a). The property of a capacitor is that it allows ac component and blocks the dc component. The operation of a capacitor filter is to short the ripple to ground but leave the dc to appear at the output when it is connected across a pulsating dc voltage.

During the positive half-cycle, the capacitor charges up to the peak value of the transformer secondary voltage, V_m, and will try to maintain this value as the full-wave input drops to zero. The capacitor will discharge through R_L slowly until the transformer secondary voltage again increases to a value greater than the capacitor voltage (equal to the load voltage). The diode conducts for a period which depends on the

capacitor voltage. The diode will conduct when the transformer secondary voltage becomes more than the 'cut-in' voltage of the diode. The diode stops conducting when the transformer voltage becomes less than the diode voltage. This is called cut-out voltage.

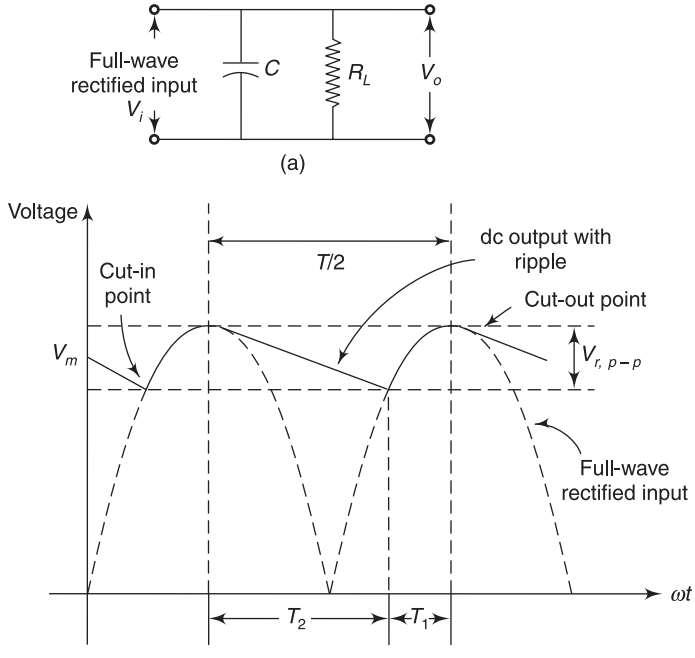


Fig. 3.7 *(a) Capacitor filter (b) Ripple voltage triangular waveform*

Referring to Fig. 3.7(b) with slight approximation, the ripple voltage waveform can be assumed as triangular. From the cut-in point to the cut-out point, whatever charge the capacitor acquires is equal to the charge the capacitor has lost during the period of non-conduction, i.e., from cut-out point to the next cut-in point.

The charge it has acquired = $V_{r,\,p-p} \times C$

The charge it has lost = $I_{dc} \times T_2$

Therefore, $V_{r,\,p-p} \times C = I_{dc} \times T_2$

If the value of the capacitor is fairly large, or the value of the load resistance is very large, then it can be assumed that the time T_2 is equal to half the periodic time of the waveform,

i.e., $$T_2 = \frac{T}{2} = \frac{1}{2f}, \quad \text{then} \quad V_{r,p-p} = \frac{I_{dc}}{2fC}$$

With the assumptions made above, the ripple waveform will be triangular in nature and the rms value of the ripple is given by

$$V_{r,\,rms} = \frac{V_{r,p-p}}{2\sqrt{3}}$$

Therefore, from this equation, we have

$$V_{r,\text{rms}} = \frac{I_{\text{dc}}}{4\sqrt{3}\ fC}$$

$$= \frac{V_{\text{dc}}}{4\sqrt{3}\ fCR_L}, \text{ since } I_{\text{dc}} = \frac{V_{\text{dc}}}{R_L}$$

Therefore, ripple factor $\Gamma = \dfrac{V_{r,\text{rms}}}{V_{\text{dc}}} = \dfrac{1}{4\sqrt{3}\ fCR_L}$

The ripple may be decreased by increasing C or R_L (or both) with a resulting increase in dc output voltage.

If $f = 50$ Hz, C in μF and R_L in Ω, $\Gamma = \dfrac{2890}{CR_L}$.

EXAMPLE 3.20

Calculate the value of capacitance to use in a capacitor filter connected to a full-wave rectifier operating at a standard aircraft power frequency of 400 Hz, if the ripple factor is 10% for a load of 500 Ω.

Solution We know that the ripple factor for capacitor filter is

$$\Gamma = \frac{1}{4\sqrt{3}\ fCR_L}$$

Therefore, $$0.01 = \frac{1}{4\sqrt{3} \times 400 \times C \times 500} = \frac{0.722 \times 10^{-6}}{C}$$

$$C = \frac{0.722 \times 10^{-6}}{0.01} = 72.2\ \mu\text{F}$$

EXAMPLE 3.21

A15-0-15 volt (rms) 50 Hz ideal transformer is used with a full-wave rectifier circuit with diodes having forward drop of 1 volt. The load is a resistance of 100 Ω and a capacitor of 10,000 μF is used as a filter across the load resistance. Calculate the dc load current and voltage.

Solution Given transformer secondary voltage = 15-0-15 V (rms);
Diode forward drop = 1 V; $R_L = 100\ \Omega$; $C = 10{,}000\ \mu\text{F}$

We know that, $$V_{\text{dc}} = V_m - \frac{V_{r,p-p}}{2} = V_m - \frac{I_{\text{dc}}}{4fC}$$

Therefore, $$V_{\text{dc}} = V_m - \frac{V_{\text{dc}}}{R_L\, 4fC}, \left[\text{since } I_{\text{dc}} = \frac{V_{\text{dc}}}{R_L}\right]$$

Simplifying, we get $$V_{\text{dc}} = \left[\frac{4f R_L C}{4f R_L C + 1}\right] V_m$$

We know that $$V_m = V_{\text{rms}} \times \sqrt{2} = 15 \times \sqrt{2}$$

Therefore, $$V_{dc} = \left[\frac{4 \times 50 \times 100 \times 10000 \times 10^{-6}}{4 \times 50 \times 100 \times 10000 \times 10^{-6} + 1}\right] \times 15 \times \sqrt{2} = 21.105 \text{ V}$$

Considering the given voltage drop of 1 volt due to diodes,

$$V_{dc} = 21.105 - 1 = 20.105 \text{ V}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.105}{100} = 0.20105 \text{ A}$$

EXAMPLE 3.22

A full-wave rectified voltage of 18 V peak is applied across a 500 μF filter capacitor. Calculate the ripple and dc voltages if the load takes a current of 100 mA.

Solution

Given $V_m = 18$ V, $C = 500$ μF and $I_{dc} = 100$ mA

$$V_{dc} = V_m - \frac{I_{dc}}{4fC} = 18 - \frac{100 \times 10^{-3}}{4 \times 50 \times 500 \times 10^{-6}} = 17 \text{ V}$$

$$V_{r,\text{rms}} = \frac{I_{dc}}{4\sqrt{3}fC} = \frac{100 \times 10^{-3}}{4\sqrt{3} \times 50 \times 500 \times 10^{-6}} = 0.577 \text{ V}$$

Therefore, ripple, $$\Gamma = \frac{V_{r,rms}}{V_{dc}} = \frac{0.577}{17} \times 100 = 3.39\%$$

EXAMPLE 3.23

A bridge rectifier with capacitor filter is fed from 220 V to 40 V step down transformer. If average dc current in load is 1 A and capacitor filter of 800 μF, calculate the load regulation and ripple factor. Assume power line frequency of 50 Hz. Neglect diode forward resistance and dc resistance of secondary of transformer.

Solution

$V_{\text{rms (secondary)}} = 40$ V, $I_{dc} = 1$A, $C = 800$ μF, and $f = 50$ Hz

$$V_m = \sqrt{2}V_{\text{rms}} = \sqrt{2} \times 40 = 56.5685 \text{ V}$$

$$V_{dc(FL)} = V_m - \frac{I_{dc}}{4fC} = 56.5685 - \frac{1}{4 \times 50 \times 800 \times 10^{-6}} = 50.3185 \text{ V}$$

On no load, $I_{dc} = 0$

Hence, $V_{dc(NL)} = V_m = 56.5685$ V

Therefore, percentage of regulation $= \dfrac{V_{dc(NL)} - V_{dc(NL)}}{I_{dc(NL)}} \times 100$

$$= \frac{56.5685 - 50.3185}{50.1385} \times 100 = 12.42\%$$

$$R_L = \frac{V_{dc}}{I_{dc}} = \frac{50.1385}{1} = 50.1385\ \Omega$$

$$\Gamma = \frac{1}{4\sqrt{3}\, fCR_L} = \frac{1}{4\sqrt{3} \times 50 \times 800 \times 10^{-6} \times 50.3185} = 0.0717, \text{ i.e., } 7.17\%$$

3.8 L-SECTION FILTER (LC FILTER)

We know that the ripple factor is directly proportional to the load resistance R_L in the inductor filter and inversely proportional to R_L in the capacitor filter. Therefore, if these two filters are combined as LC filter or L-section filter as shown in Fig. 3.8, the ripple factor will be independent of R_L.

If the value of the inductance is increased, it will increase the time of conduction. At some critical value of inductance, one diode, either D_1 or D_2 in full-wave rectifier, will always be conducting.

From Fourier series, the output voltage can be expressed as

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t$$

The dc output voltage, $V_{dc} = \frac{2V_m}{\pi}$

Therefore, $I_{rms} = \frac{4V_m}{3\pi\sqrt{2}} \cdot \frac{1}{X_L} = \frac{\sqrt{2}}{3} \cdot \frac{V_{dc}}{X_L}$

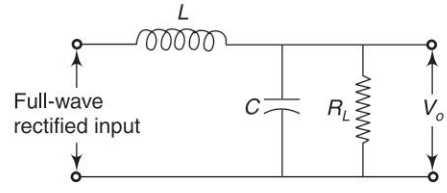


Fig. 3.8 *LC filter*

This current flowing through X_C creates the ripple voltage ($V_{r,\,rms}$) in the output.

Therefore, $V_{r,\,rms} = I_{rms} \cdot X_C = \frac{\sqrt{2}}{3} \cdot V_{dc} \cdot \frac{X_C}{X_L}$

The ripple factor, $\Gamma = \frac{V_{r,\,rms}}{V_{dc}} = \frac{\sqrt{2}}{3} \cdot \frac{X_C}{X_L}$

$$= \frac{\sqrt{2}}{3} \cdot \frac{1}{4\omega^2 C_L}, \text{ since } X_C = \frac{1}{2\omega C} \text{ and } X_L = 2\omega L$$

If $f = 50$ Hz, C is in μF and L is in Henry, ripple factor $\Gamma = \frac{1.194}{LC}$.

➤ ***Bleeder Resistor*** It was assumed in the analysis given above that for a critical value of inductor, either of the diodes is always conducting, i.e., current does not fall to zero. The incoming current consists of two components:

(i) $I_{dc} = \frac{V_{dc}}{R_L}$, and (ii) a sinusoidal varying components with peak value of $\frac{4V_m}{3\pi X_L}$. The negative peak of the ac current must always be less than dc, i.e., $\sqrt{2}\, I_{rms} \le \frac{V_{dc}}{R_L}$.

We know that for *LC* filter, $I_{\text{rms}} = \frac{\sqrt{2}}{3} \times \frac{V_{\text{dc}}}{X_L}$

Hence, $\frac{2V_{\text{dc}}}{X_L} \leq \frac{V_{\text{dc}}}{R_L}$, i.e., $X_L \geq \frac{2}{3} R_L$

i.e., $L_C = \frac{R_L}{2\omega}$, where L_C is the critical inductance.

It should be noted that the condition $X_L \geq \frac{2}{3} R_L$ cannot be satisfied for all load requirements. At no load, i.e., when the load resistance is infinity, the value of the inductance will also tend to be infinity. To overcome this problem, a bleeder resistor R_B is connected in parallel with the load resistance as shown in Fig. 3.9. Therefore, a minimum current will always be present for optimum operation of the inductor. It improves voltage regulation of the supply by acting as the pre-load on the supply. Also, it provides safety by acting as a discharging path for capacitor.

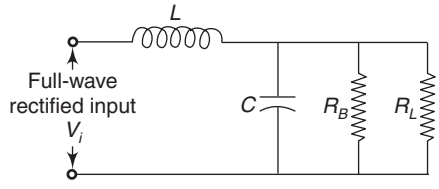


Fig. 3.9 *Bleeder resistor connected at the filter output*

EXAMPLE 3.24

Design a filter for full-wave circuit with *LC* filter to provide an output voltage of 10 V with a load current of 200 mA and the ripple is limited to 2%.

Solution The effective load resistance, $R_L = \frac{10}{200 \times 10^{-3}} = 50\ \Omega$

We know that the ripple factor,

$$\Gamma = \frac{1.194}{LC}$$

i.e., $$0.02 = \frac{1.194}{LC}$$

i.e., $$LC = \frac{1.194}{0.02} = 59.7$$

Critical value of $L = \frac{R_L}{3\omega} = \frac{50}{3 \times 2\pi f} = 53$ mH

Taking $L = 60$ mH (about 20% higher), C will be about 1000 μF.

EXAMPLE 3.25

A full-wave rectifier (FWR) supplies a load requiring 300 V at 200 mA. Calculate the transformer secondary voltage for (a) a capacitor input filter using a capacitor of 10 mF, and (b) a choke input filter using a choke of 10 H and a capacitance of 10 μF. Neglect the resistance of choke.

Solution Given $V_{dc} = 300$ V; $I_{dc} = 200$ mA

(a) For the capacitor filter with $C = 10$ μF,

$$V_{dc} = V_m - \frac{I_{dc}}{4fC}$$

$$300 = V_m - \frac{200 \times 10^{-3}}{4(50)(10 \times 10^{-6})} = V_m - 100$$

Therefore, $V_m = 400\ V_{(p-p)}$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = 282.84 \text{ V}$$

(b) For the choke, i.e., *LC* filter with $L = 10$ H; $C = 10$ μF

$$V_{dc} = \frac{2V_m}{\pi}$$

$$300 = \frac{2V_m}{\pi}$$

Therefore, $V_m = 471.23$ V

$$V_{rms} = \frac{V_m}{\sqrt{2}} = 333.21 \text{ V}$$

EXAMPLE 3.26

Determine the ripple factor of a *L*-type choke input filter comprising a 10 H choke and 8 μF capacitor used with a FWR. Compare with a simple 8 μF capacitor input filter at a load current of 50 mA and also at 150 mA. Assume the dc voltage of 50 V.

Solution $V_{dc} = 50$ V, $L = 10$ H, $C = 8$ μF

Assume $f = 50$ Hz, i.e., $\omega = 2\pi f = 100\pi$ rad/sec.

For *LC* filter, the ripple factor is

$$\Gamma = \frac{1}{6\sqrt{2}\omega^2 LC} = \frac{1}{6\sqrt{2} \times (100\pi)^2 \times 10 \times 8 \times 10^{-6}} = 0.01492 \text{ i.e., } 1.492\%$$

For the simple capacitor filter, $C = 8$ μF.

(a) At $I_L = 50$ mA,

$$R_L = \frac{V_{dc}}{I_L} = \frac{50}{50 \times 10^{-3}} = 1000\ \Omega$$

$$\Gamma = \frac{1}{4\sqrt{3}fCR_L} = \frac{1}{4\sqrt{3} \times 50 \times 8 \times 10^{-6} \times 1000} = 0.3608, \text{ i.e., } 36.08\%$$

(b) At $I_L = 150$ mA,

$$R_L = \frac{V_{dc}}{I_L} = \frac{50}{150 \times 10^{-3}} = 333.33\ \Omega$$

$$\Gamma = \frac{1}{4\sqrt{3} f C R_L} = \frac{1}{4\sqrt{3} \times 50 \times 8 \times 10^{-6} \times 333.33} = 1.082, \text{ i.e., } 108.2\%$$

Thus, it is inferred that the *LC* choke input filter is more effective than capacitor input filter and the ripple factor of *LC* choke input filter does not depend on the load resistance.

EXAMPLE 3.27

In a full-wave rectifier using an *LC* filter, $L = 10$ H, $C = 100$ μF, and $R_L = 500$ Ω. Calculate I_{dc},$V_{dc,}$ and ripple factor for an input of $v_i = 30 \sin (100 \pi t)$V.

Solution Comparing the input with $v_i = V_m \sin \omega t$

V_m (secondary) $= V_m = 30$ V

$$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 30}{\pi} = 19.0985 \text{ V}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{19.0985}{500} = 0.03819 \text{ A} = 38.19 \text{ mA}$$

$$\text{Ripple factor} = \frac{1}{6\sqrt{2}\, \omega^2 LC}$$

$$= \frac{1}{6\sqrt{2} \times (100\pi)^2 \times 10 \times 100 \times 10^{-6}} = 1.194 \times 10^{-3}$$

➤ ***Multiple L-section Filter*** The filtering level can be improved by using two of more L-section filters in series, as shown in Fig. 3.10. It is assumed that the reactance of all the inductances are much larger than the reactance of the capacitors and the reactance of the last capacitor is small compared with the resistance of the load. Under these conditions, the impedance between 3 and 3′ is X_{C2}, the impedance between 2 and 2′ is X_{C1}, and the impedance between 1 and 1′ is X_{L1}. The alternating current I_1 through L_1 is, given by

$$I_1 = \frac{\sqrt{2}\, V_{dc}}{3} \frac{1}{X_{L1}}$$

The ac voltage across C_1 is given by

$$V_{22'} = I_1 X_{C1}$$

The alternating current I_2 through L_2 is given by

$$I_2 = \frac{V_{22'}}{X_{L2}}$$

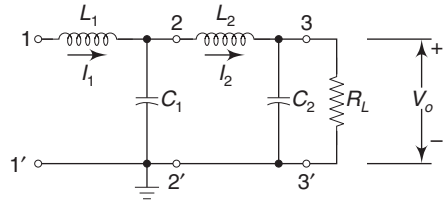


Fig. 3.10 *A multiple (two-section) L-section filter*

The ac voltage across C_2 and hence, across the load is given by

$$V_{33'} = I_2 X_{C2} = I_1 \frac{X_{C2} X_{C1}}{X_{L2}} = \frac{\sqrt{2}\, V_{d.c.}}{3} \frac{X_{C2} X_{C1}}{X_{L2} X_{L1}}$$

The ripple factor is obtained by dividing the above equation by V_{dc}. Hence,

$$\Gamma = \frac{\sqrt{2}}{3} \frac{X_{C1} X_{C2}}{X_{L1} X_{L2}}$$

The generalized expression for any number of sections can be obtained by comparing the above equation with that of a single L-section. For example, the ripple factor of a multiple L-section filter (Γ_n) is given by

$$\Gamma_n = \frac{\sqrt{2}}{3}\left(\frac{X_C}{X_L}\right)^n = \frac{\sqrt{2}}{3}\frac{1}{(16\pi^2 f^2 LC)^n}$$

where n is the number of similar L-sections.

3.9 π-SECTION FILTER

Figure 3.11 shows the CLC or π-type filter which basically consists of a capacitor filter followed by an LC section. This filter provided a fairly smooth output, and is characterized by a highly peaked diode currents and poor regulation.

The action of a π-section filter can best be understood by considering the inductor and the second capacitor as an L-section filter that acts upon the triangular output-voltage wave from the first capacitor. The output voltage is then approximately that from the input capacitor, decreased by the dc voltage drop in the inductor. The ripple contained in this output is reduced by the L-section filter.

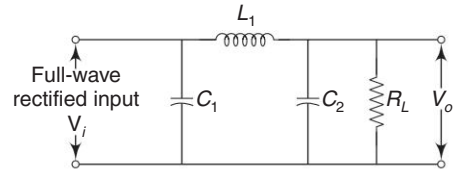


Fig. 3.11 *CLC or π-type filter*

The ripple voltage can be calculated by analyzing the triangular wave into a Fourier series and then multiplying each component by X_{C2}/X_{L1} for this harmonic. The Fourier analysis of this waveform is given by

$$v = V_{\text{dc}} - \frac{V_r}{\pi}\left(\sin 2\,\omega t - \frac{\sin 2\omega t}{2} + \frac{\sin 6\omega t}{3} - \cdots\right)$$

We know that

$$V_r = \frac{I_{\text{dc}}}{2fC_1}$$

The rms second-harmonic voltage is

$$V_{\text{rms}} = V_2' = \frac{V_r}{\pi\sqrt{2}} = \frac{I_{\text{dc}}}{2\pi fC_1\sqrt{2}} = \sqrt{2}I_{\text{dc}}X_{C1}$$

where X_{C1} is the reactance of C_1 at the second-harmonic frequency.

The voltage V_2' is impressed on an L-section, and the output ripple is $V_2'X_{C2}/X_{L1}$.

Hence, the ripple factor is

$$\Gamma = \frac{V_{\text{rms}}}{V_{\text{dc}}} = \frac{\sqrt{2}\,I_{\text{dc}}X_{C1}}{V_{\text{dc}}}\frac{X_{C2}}{X_{L1}} = \sqrt{2}\,\frac{X_{C1}}{R_L}\frac{X_{C2}}{X_{L1}}$$

where all reactance are calculated at the second-harmonic frequency.

For $f = 60$ Hz, the above equation reduces to

$$\Gamma = \frac{3{,}300}{C_1C_2L_1R_L}$$

3.10 MULTIPLE L-SECTION AND π-SECTION FILTERS

In order to obtain pure dc at the output, more number of π-sections may be used in series. Such a filter using more than one π-section, as shown in Fig. 3.12, is called a multiple π-section filter.

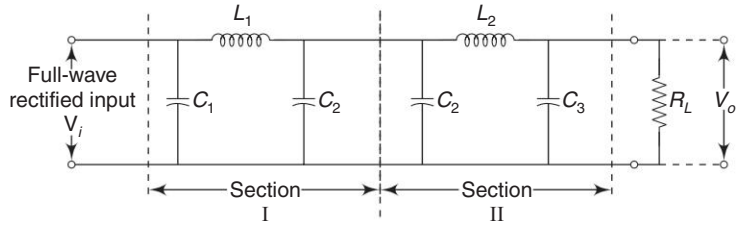


Fig. 3.12 *Multiple π-section filter*

The ripple factor for multiple π-section filler is given by

$$\Gamma = \frac{X_{C1}}{R_L} \cdot \frac{X_{C2}}{X_{L1}} \cdot \frac{X_{C3}}{X_{L2}} \cdots \frac{X_{Cn}}{X_{L(n-1)}}$$

where n is the number of π-sections.

EXAMPLE 3.28

Design a CLC or π-section filter for $V_{dc} = 10$ V, $I_L = 200$ mA, and $\Gamma = 2\%$.

Solution

$$R_L = \frac{10}{200 \times 10^{-3}} = 50\ \Omega$$

$$0.02 = \frac{5700}{LC_1C_2 \times 50} = \frac{114}{LC_1C_2}$$

If we assume $L = 10$ H and $C_1 = C_2 = C$, we have

$$0.02 = \frac{114}{LC^2} = \frac{11.4}{C^2}$$

$$C^2 = 570; \text{ therefore, } C = \sqrt{570} \approx 24\ \mu\text{F}$$

EXAMPLE 3.29

A full-wave single-phase rectifier employs a π-section filter consisting of two 4 μF capacitances and a 20 H choke. The transformer voltage to the centre tap is 300 V rms. The load current is 500 mA. Calculate the dc output voltage and the ripple voltage. The resistance of the choke is 200 Ω.

Solution

$$C_1 = C_2 = 4\ \mu\text{F}, L = 20\ \text{H}$$

$$I_{dc} = 500\ \text{mA}, R_x = 200\ \Omega$$

Maximum value of secondary voltage,

$$V_{s(\max)} = \sqrt{2} \times 300 = 424.2\ \text{V}$$

$$R_L = \frac{V_{dc}}{I_{dc}} = \frac{270.19}{500 \times 10^{-3}} = 540\ \Omega$$

$$V_{dc} = V_{s(max)} - \frac{V_r}{2} - I_{dc} R_x$$

Ripple voltage, $$V_r = \frac{I_{dc}}{2fC} = \frac{500 \times 10^{-3}}{2 \times 50 \times 4 \times 10^{-6}} = 1.25\ \text{mV}$$

The dc output voltage, $$V_{dc} = 424.2 - \frac{1.25 \times 10^{-3}}{2} - (500 \times 10^{-3} \times 200) = 324.19\ \text{V}$$

➤ ***R–C Filters*** Consider the *CLC* filter with the inductor *L* replaced by a resistor *R*. This type of filter called *RC* filter is shown in Fig. 3.13. The expression for the ripple factor can be obtained by replacing X_L by *R*. Then,

$$\Gamma = \sqrt{2}\, \frac{X_{C1}}{R_L} \cdot \frac{X_{C2}}{R}$$

Therefore, if resistor *R* is chosen equal to the reactance of the inductor which it replaces, the ripple remains unchanged.

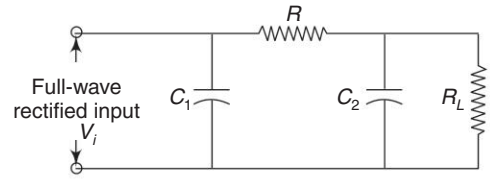


Fig. 3.13 *R–C filter*

The resistance *R* will increase the voltage drop and hence, the regulation will be poor. This type of filters are often used for economic reasons, as well as the space and weight requirement of the iron-cored choke for the *LC* filter. Such *RC* filters are often used only for low current power supplies.

3.11 COMPARISON OF VARIOUS FILTER CIRCUITS

Table 3.2 shows the comparison of various types of filters, when used with full-wave circuits. In all these filters, the resistances of diodes, transformer and filter elements are considered negligible and a 60 Hz power line is assumed.

Table 3.2 *Comparison of various types of filters*

Particulars	Type of Filter				
	None	L	C	L-Section	π-Section
V_{dc} at no load	0.636 V_m	0.636 V_m	V_m	V_m	V_m
V_{dc} at load I_{dc}	0.636 V_m	0.636 V_m	$V_m - \frac{4170 I_{dc}}{C}$	0.636 V_m	$V_m - \frac{4170 I_{dc}}{C}$
Ripple factor Γ	0.48	$\frac{R_L}{16000\ L}$	$\frac{2410}{CR_L}$	$\frac{0.83}{LC}$	$\frac{3330}{LC_1C_2R_L}$
Peak inverse voltage (PIV)	2 V_m	2 V_m	2 V_m	2 V_m	2 V_m

3.12 VOLTAGE REGULATORS

In an unregulated power supply, the output voltage changes whenever the input voltage or load changes. An ideal regulated power supply is an electronic circuit designed to provide a predetermined dc voltage V_o which is independent of the load current and variations in the input voltage. A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations.

➤ ***Factors Determining the Stability*** The output dc voltage V_o depends on the input unregulated dc voltage V_i, load current I_L and temperature T. Hence, the change in output voltage of power supply can be expressed as follows:

$$\Delta V_o = \frac{\partial V_o}{\partial V_i}\Delta V_i + \frac{\partial V_o}{\partial I_L}\Delta I_L + \frac{\partial V_o}{\partial T}\Delta T$$

or $$\Delta V_o = S_V \Delta V_i + R_o \Delta I_L + S_T \Delta T$$

where the three coefficients are defined as

Input regulation factor, $$S_V = \frac{\Delta V_o}{\Delta V_i} \mid \Delta I_L = 0; \Delta T = 0$$

Output resistance, $$R_o = \frac{\Delta V_o}{\Delta I_L} \mid \Delta V_i = 0; \Delta T = 0$$

Temperature coefficient, $$S_T = \frac{\Delta V_o}{\Delta T} \mid \Delta V_i = 0; \Delta I_L = 0$$

Smaller the value of the three coefficients, better the regulation of the power supply.

➤ ***Line Regulation*** Line regulation is defined as the change in output voltage for a change in line supply voltage, keeping the load current and temperature constant. Line regulation is given by

$$\text{Line regulation} = \frac{\text{Change in output voltage}}{\text{Change in input voltage}} = \frac{\Delta V_o}{\Delta V_i}$$

➤ ***Load Regulation*** Load regulation is defined as a change in regulated output voltage as the load current changes from no load to full load. It is expressed as a percentage of no-load voltage or full-load voltage.

$$\% \text{ Load regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{no load}}} \times 100$$

or $$\% \text{ Load regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{full load}}} \times 100$$

where $V_{\text{no load}}$ is the output voltage at zero load current and $V_{\text{full load}}$ is the output voltage at rated load current. This is usually denoted in percentage. The plot of the output voltage V_o versus the load current I_L for a full-wave rectifier is given in Fig. 3.14. The drop in the characteristics is a measure of the internal resistance of the power supply.

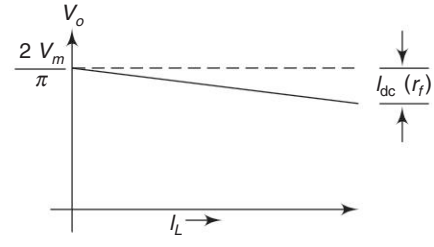


Fig. 3.14 *Load regulation characteristics*

3.13 SHUNT VOLTAGE REGULATOR

A Zener diode, under reverse bias breakdown condition, can be used to regulate the voltage across a load, irrespective of the supply voltage or load current variations. A simple Zener voltage regulator circuit is shown in Fig. 3.15. The Zener diode is selected with V_Z equal to the voltage desired across the load. The Zener diode has a characteristic that under reverse bias condition, the voltage across it practically remains constant, even if the current through it changes by a large extent. Under normal conditions, the input current $I_i = I_L + I_Z$ flows through resistor R. The input voltage V_i can be written as $V_i = I_iR + V_Z = (I_L + I_Z)\,R + V_Z$.

When the input voltage V_i increases (say due to supply voltage variations), as the voltage across Zener diode remains constant, the drop across resistor R will increase with a corresponding increase in $I_L + I_Z$. As V_Z is a constant, the voltage across the load will also remain constant and hence, I_L will be a constant. Therefore, an increase in $I_L + I_Z$ will result in an increase in I_Z which will not alter the voltage across the load.

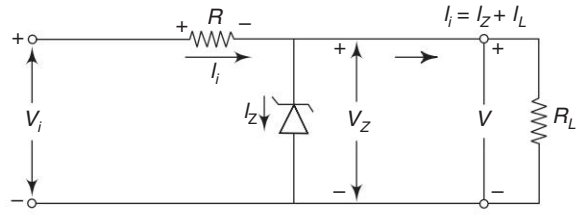


Fig. 3.15 *Zener voltage regulator*

It must be ensured that the reverse voltage applied to the Zener diode never exceeds PIV of the diode and at the same time, the applied input voltage must be greater than the breakdown voltage of the Zener diode for its operation. The Zener diodes can be used as 'stand-alone' regulator circuits and also as reference voltage sources.

EXAMPLE 3.30

Design a Zener shunt voltage regulator with the following specifications: V_o = 10 V; V_{in} = 20–30 V; I_L = (30–50) mA; I_Z = (20–40) mA

Solution Refer Fig. 3.15.

Selection of Zener diode

$$V_Z = V_o = 10 \text{ V}$$

$$I_{Z\,(\max)} = 40 \text{ mA}$$

$$P_Z = V_Z \times I_{Z(\max)} = 10 \times 40 \times 10^{-3} = 0.4 \text{ W}$$

Hence, a 0.5 WZ 10 Zener can be selected

Value of load resistance, R_L

$$R_{L\,(\min)} = \frac{V_o}{I_{L(\max)}} = \frac{10}{50 \times 10^{-3}} = 200\ \Omega$$

$$R_{L\,(\max)} = \frac{V_o}{I_{L(\min)}} = \frac{10}{30 \times 10^{-3}} = 333\ \Omega$$

Value of input resistance, R

$$R_{\max} = \frac{V_{\text{in}(\max)} - V_o}{I_{L(\min)} + I_{Z(\max)}}$$

$$= \frac{30-10}{(30+40)\times 10^{-3}} = 286\ \Omega$$

$$R_{\min} = \frac{V_{\text{in(min)}} - V_o}{I_{L(\max)} + I_{Z(\min)}}$$

$$= \frac{20-10}{(50+20)\times 10^{-3}} = 143\ \Omega$$

Therefore, $$R = \frac{R_{\max} + R_{\min}}{2} = 215\ \Omega$$

EXAMPLE 3.31

In a Zener regulator, the dc input is 10 V ± 20%. The output requirements are 5 V, 20 mA. Assume $I_{Z(\min)}$ and $I_{Z(\max)}$ as 5 mA and 80 mA. Design the Zener regulator.

Solution The minimum Zener current is $I_{Z(\min)} = 5$ mA when the input voltage is minimum. Here the input voltage varies between 10 V ± 20%, i.e., 8 V and 12 V.

Therefore, the input voltage $V_{i(\min)} = 8$ V

Given load current $I_L = 20$ mA and the voltage across the load, $V_o = 5$ V.

Therefore,

$$R_L = \frac{V_o}{I_L} = \frac{5\ \text{V}}{20\times 10^{-3}} = 250\ \Omega$$

Hence, the series resistance $$R = \frac{V_{i(\min)} - V_o}{(I_{Z(\min)} + I_L)}$$

$$= \frac{(8-5)}{(5+20)\times 10^{-3}} = 120\ \Omega$$

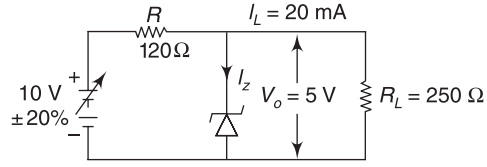


Fig. 3.16

The various values are given in the Zener regulator shown in Fig. 3.16.

EXAMPLE 3.32

If dc unregulated input is 20 V, $V_o = 10$ V and load current is 0–20 mA, design the Zener voltage regulator. Assume for the Zener, $I_{Z(\min)} = 10$ mA and $I_{Z(\max)} = 100$ mA.

Solution Given input voltage, $V_i = 20$ V

Output voltage $V_o = 10$ V

Load current varies from 0 to 20 mA

$I_{Z(\min)} = 10$ mA, $I_{Z(\max)} = 100$ mA

Here, $V_Z = V_o = 10$ V (constant)

Applying KVL to a closed-loop circuit, $V_i = IR + V_Z$

Hence, $20 = IR + 10$

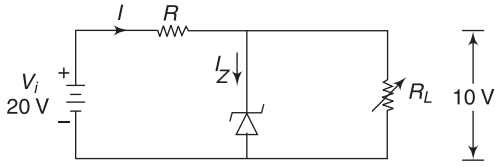


Fig. 3.17

or $IR = 10$

Therefore, $R = \frac{10}{I}\ \Omega$, where I is the loop current in ampere

(i) For $I_Z = I_{Z(\min)} = 10\text{mA}$ and $I_L = 0$

The total current $I = I_L + I_Z = 10\text{ mA}$

Therefore, $R_{\max} = \frac{V_o}{I_{Z(\min)}} = \frac{10}{10 \times 10^{-3}} = 1000\ \Omega$

(ii) For $I_Z = I_{Z(\max)} = 100\text{ mA}$ and $I_L = 20\text{ mA}$

$$I = I_L + I_{Z(\max)} = 20 \times 10^{-3} + 100 \times 10^{-3} = 120\text{ mA}$$

Therefore, $R_{\min} = \frac{V_o}{I} = \frac{10}{120 \times 10^{-3}} = 83.33\ \Omega$

(iii) The range of R varies from 83.33 Ω to 1000 Ω.

EXAMPLE 3.33

Design a Zener voltage regulator to meet the following specifications: Output voltage = 5 V, Load current = 10 mA, Zener wattage = 400 mW and input voltage = 10 V ± 2 V.

Solution Given $V_o = 5\text{ V}, I_L = 10\text{ mA}$

Here, load resistance is $R_L = \frac{V_o}{I_L} = \frac{5}{10 \times 10^{-3}} = 500\ \Omega$

Maximum Zener current $I_{Z(\max)} = \frac{400\text{ mW}}{5\text{ V}} = 80\text{ mA}$

The minimum input voltage required will be when $I_z = 0$. Under this condition,

$I = I_L = 10\text{ mA}$

Minimum input voltage $V_{i(\min)} = V_o + IR$

Hence, $V_{i(\min)} = 10 - 2 = 8\text{ V}$

or $8 = 5 + (10 \times 10^{-3})\ R$

Therefore, $R_{\max} = \frac{3}{10 \times 10^{-3}} = 300\ \Omega$

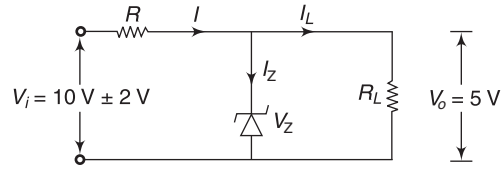


Fig. 3.18

Now, maximum input voltage, $V_{i(\max)} = V_o + \lfloor I_{Z(\max)} + I_L \rfloor R = 5 + [(80 + 10)10^{-3}]R$

or $12 = 5 + (90 \times 10^{-3})R$

$$R_{\min} = \frac{7}{90 \times 10^{-3}} = 77.77\ \Omega$$

The value of R is chosen between 77.77 Ω and 300 Ω.

EXAMPLE 3.34

A 24 V, 600 mW Zener diode is used for providing a 24 V stabilized supply to a variable load. If the input voltage is 32 V, calculate (a) the value of series resistance required and (b) diode current when the load is 1200 Ω.

Solution Given $V_o = 24$ V, $V_i = 32$ V, $P_Z = 600$ mW and $R_L = 1200\ \Omega$

The load current, $$I_L = \frac{V_o}{R_L} = \frac{24}{1200} = 20 \text{ mA}$$

Maximum Zener current, $$I_{Z(\max)} = \frac{P_Z}{V_o} = \frac{600 \times 10^{-3}}{24} = 25 \text{ mA}$$

$$R_{\max} = \frac{V_i - V_o}{I_{L(\min)} + I_{Z(\max)}}$$

$$= \frac{32 - 24}{(20 + 25) \times 10^{-3}} = \frac{8}{45 \times 10^{-3}} = 177.78\ \Omega$$

EXAMPLE 3.35

A Zener voltage regulator circuit is to maintain constant voltage at 60 V, over a current range from 5 to 50 mA. The input supply voltage is 200 V. Determine the value of the resistance R to be connected in the circuit, for voltage regulation from load current $I_L = 0$ mA to I_L max, the maximum possible value of I_L. What is the value of I_L max?

Solution Given $V_Z = V_o = 60$ V and $V_i = 200$ V

(a) *To find the value of resistance* (R):

$$R = \frac{V_i - V_o}{I_{Z(\max)} + I_{L(\min)}}$$

$$= \frac{200 - 60}{50 \times 10^{-3}} = \frac{140}{50 \times 10^{-3}} = 2.8 \text{ k}\Omega$$

(b) *To find the value of* $I_{L(\max)}$:

If $I_{Z(\max)} = 50$ mA, $I_{L(\min)} = 0$ mA

If $I_{Z(\min)} = 5$ mA, $I_{L(\max)} = 45$ mA

Therefore, $I_{L(\max)} = 45$ mA

EXAMPLE 3.36

For the Zener voltage regulation shown, determine the range of R_L and I_L that gives the stabilizer voltage of 10 V.

Solution From the circuit, $I = I_Z + I_L$

But from R, $$I = \frac{V_i - V_o}{R} = \frac{40 - 10}{1 \times 10^3} = 30 \text{ mA}$$

When I_L is minimum, I_Z is maximum and vice versa.

$$I = I_{Z(\max)} + I_{L(\min)}$$

$$30 \text{ mA} = 24 \text{ mA} + I_{L(\min)}$$

Therefore, $I_{L(\min)} = 6$ mA

But $$I_{L(\min)} = \frac{V_o}{R_{L(\max)}}$$

$$R_{L(\max)} = \frac{V_o}{I_{L(\min)}} = \frac{10}{6 \times 10^{-3}} = 1.667 \text{ k}\Omega$$

and $$I = I_{Z(\min)} + I_{L(\max)}$$

$$30 \text{ mA} = 5 \text{ mA} + I_{L(\max)}$$

$$I_{L(\max)} = 25 \text{ mA}$$

But $$I_{L(\max)} = \frac{V_o}{R_{L(\min)}}$$

$$R_{L(\min)} = \frac{V_o}{I_{L(\max)}} = \frac{10}{25 \times 10^{-3}} = 400 \ \Omega$$

Hence, the range of I_L is 6 mA to 25 mA and that of R_L is 400 W to 1.667 kW.

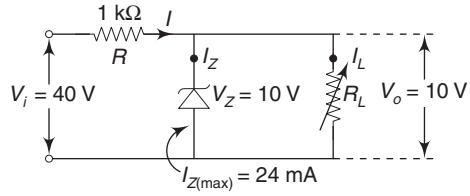


Fig. 3.19

EXAMPLE 3.37

Determine the range of input voltage that maintains the output voltage of 10 V, for the regulator circuit shown.

Solution As $V_o = 10$ V constant and $R_L = 10$ kΩ constant, we have

$$I_L = \frac{V_o}{R_L} = \frac{10}{10 \times 10^3} = 1 \text{ mA}$$

When $V_i = V_{i(\max)}$, $I_Z = I_{Z(\max)}$

Now $I = I_Z + I_L$

Therefore, $I_{(\max)} = I_{Z(\max)} + I_L = 24 \text{ mA} + 1 \text{ mA} = 2 \text{ mA}.$

$$\frac{V_{i(\max)} - V_Z}{R} = 25 \text{ mA}$$

Therefore, $V_{i(\max)} - 10 = 1 \times 10^3 (25 \times 10^{-3})$

$$V_{i(\max)} = 35 \text{ V}.$$

When $V_i = V_{i(\min)}$, $I_Z = I_{Z(\min)} = 5$ mA

Therefore, $I_{\min} = I_{Z(\min)} + I_L = 5 \text{ mA} + 1 \text{ mA} = 6 \text{ mA}$

$$\frac{V_{i(\min)} - V_Z}{R} = 6 \times 10^{-3}$$

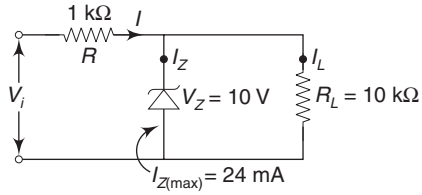


Fig. 3.20

$$V_{i(\min)} - 10 = 1 \times 10^3 (6 \times 10^{-3})$$

$$V_{i(\min)} = 16 \text{ V}$$

Thus, range of input voltage is 16 V to 35 V for which the output voltage will be of 10 V.

3.14 SERIES VOLTAGE REGULATOR

In the Zener voltage regulator, the Zener current varies over a wide range as the input voltage and load current vary. As a result, the output voltage which is equal to V_z also changes by a small amount. This change in the output voltage can be minimized by reducing the change in the Zener current with the help of a circuit called emitter-follower type regulator as shown in Fig. 3.21.

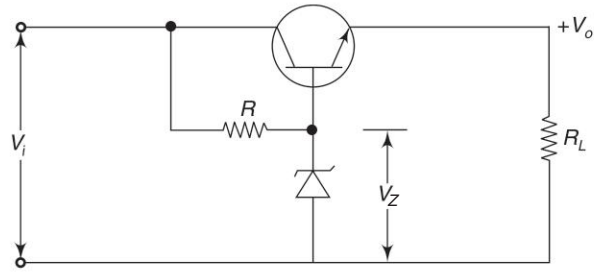


Fig. 3.21 *Emitter-follower type regulator*

Here, the load resistance, R_L, is not connected across the Zener directly as in the Zener regulator, but is connected through an amplifier/buffer circuit. The transistor is connected as an emitter-follower. As can be seen, the output voltage, $V_o = (V_Z - V_{BE})$.

However, the load current I_L is supplied by the transistor from the input voltage V_i, deriving its base current from the Zener circuit. The base current I_B is equal to $\frac{I_L}{\beta}$, where β is the current-gain of the transistor. As far as the Zener circuit is concerned, it is supplying only the base current. Any change in the load current is reduced by β times, i.e., change in the Zener current.

3.15 OVERLOAD VOLTAGE PROTECTION

Figure 3.22(a) shows overload protection circuit in which a small sensing resistance R_{SC} is added in series with the load resistance and two diodes are connected from the base of the transistor to the output.

The emitter voltage is equal to $(V_Z - V_{BE})$. The voltage drop across the sensing resistance R_{SC} is equal to $(I_L \times R_{SC})$. As long as the voltage drop across R_{SC} is less than twice the cut-in voltage of the diode, the diodes are effectively as good as not connected in the circuit. If the voltage drop across R_{SC} increases suddenly due to overcurrent in the load, then the diodes will be forward biased and will start conducting. This will divert a part of the base current, which will be directly led to the output, thus restricting the base current and hence, the transistor current. With proper design, the transistor can be turned off in the case of a short circuit.

The protective diodes can be replaced by another transistor Q_2 as shown in Fig. 3.22(b). In this case, the voltage across R_{SC} is used in turning ON transistor Q_2, giving the same effect as before.

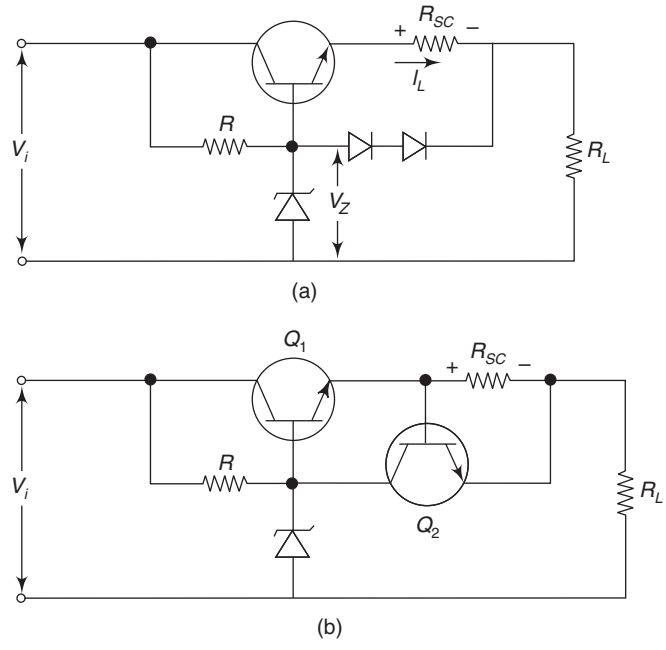


Fig. 3.22 *(a) and (b) Overload protection circuits*

REVIEW QUESTIONS

1. What is a rectifier?
2. Show that a *PN* diode works as rectifier.
3. Define the following terms:
   (i) ripple factor (ii) peak inverse voltage (iii) efficiency (iv) transformer utilization factor (v) form factor (vi) peak factor.
4. Draw the circuit diagram of an half-wave rectifier, and explain its operation.
5. Derive expressions for rectification efficiency, ripple factor, transformer utilization factor, form factor, and peak factor of an half-wave rectifier with resistive load.
6. A half-wave rectifier has a load of 3.5 kΩ. If the diode resistance and secondary coil resistance together have a resistance of 800 Ω and the input voltage has a signal voltage of peak value 240 V, calculate
   (i) Peak, average and rms value of current flowing
   (ii) dc power output
   (iii) ac power input
   (iv) Efficiency of the rectifier

   [*Ans.* (i) 55.81 mA, 17.78 mA and 27.9 mA (ii) 1.1 W (iii) 3.35 W (iv) 32.9%]
7. Explain the action of a full-wave rectifier and give waveforms of input and output voltages.
8. Derive expressions of dc or average value of voltage and rms value of voltage of a full-wave rectifier with resistive load.
9. Derive an expression for a ripple factor in a full-wave rectifier with resistive load.

10. Determine the value of ripple factor in the full-wave rectifier operating at 50 Hz with a 100 μF capacitor filter and 100 Ω load. [*Ans.* 29%]

11. Show that a full-wave rectifier is twice as efficient as a half-wave rectifier.

12. Describe the action of a full-wave bridge rectifier.

13. What are the advantages of a bridge rectifier?

14. Compare half-wave, full-wave and bridge rectifiers.

15. What is the need for filters in power supplies?

16. Explain the various types of filters used in power supplies.

17. Obtain the ripple factor of a full-wave rectifier with shunt capacitor filter.

18. Derive an expression for the ripple factor in a full-wave rectifier using inductor filter.

19. Compare the performance of inductive, L-section and π-section filters.

20. An $L-C$ filter is to be used to provide a dc output with 1% ripple from a full-wave rectifier operating at 50 Hz. Assuming $L/C = 0.01$, determine the required values of L and C. [*Ans.* 1.093 H, 109.27 μF]

21. In a full-wave rectifier using an $L-C$ filter, it is known that $L = 10$ H, $C = 100$ μF, and $R_L = 500$ Ω. Calculate I_{dc}, V_{dc}, I_{ac}, V_{ac} if $V_m = 30$ V and $f = 50$ Hz. [*Ans.* 38.2 mA, 19.1 V, 1.43 mA, 22.7 mV]

22. The turns ratio of the transformer used in a half-wave rectifier is 2:1 and the primary is connected to 230 V, 50 Hz power mains. Assuming the diodes to be ideal, determine (i) dc voltage across the load, (ii) PIV of each diode, and (iii) medium and average values of power delivered to the load having a resistance of 200 Ω. Also find the efficiency of the rectifier and output ripple frequency.

[*Ans.* 51.7 V, 162.2 V, 132.2 W, 13.5 W, 10.21%, 50 Hz]

23. In a full-wave rectifier, the voltage applied to each diode is 240 sin 377t, the load resistance is $R_L = 2000$ Ω and each diode has a forward resistance of 400 Ω. Determine the (i) peak value of current, (ii) dc value of current, (iii) rms value of current, (iv) rectifier efficiency, (v) ripple factor, and (vi) output ripple frequency. [*Ans.* 100 mA, 63.8 mA, 70.7 mA, 67.6%, 0.482, 120 Hz]

24. In a bridge rectifier, the transformer is connected to 220 V, 60 Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diodes to be ideal, find (i) the voltage across the load, (ii) I_{dc} and (iii) PIV. [*Ans.* 18 V, 18 mA, 28.28 V]

25. In a full-wave rectifier, the transformer rms secondary voltage from centre tap to each end of secondary is 50 V. The load resistance is 900 Ω. If the diode resistance and transformer secondary winding resistance together has a resistance of 100 Ω. Determine the average load current and rms value of load current. [*Ans.* 45 mA, 50 mA]

26. A Zener diode shunt regulator circuit is to be designed to maintain a constant load current of 400 mA and voltage of 40 V. The input voltage is 90 ± 5 V. The Zener diode voltage is 40 V and its dynamic resistance is 2.5 Ω. Find the following quantities for the regulator: (i) the series dropping resistance, (ii) Zener power dissipation, and (iii) load resistance. Assume the Zener current to be 10% of load current.

[*Ans.* 112.5 Ω, 3.6 Ω, 100 Ω]

27. In a half-wave rectifier, an ac voltage of peak value 24 V is connected in series with a silicon diode and load resistance of 480 Ω. If the forward resistance of the diode is 20 Ω, find the peak current flowing through the diode.

[*Ans.* 46.6 mA]

28. A Zener diode voltage regulator shown in Fig. 3.18 has the following specifications:
$V_z = 15$ V, $I_{z(min)} = 2$ μA, $P_z = 120$ W, $R_z = 40$ Ω, $R_L = 5$ kΩ and $V_i = 18$–24 V.
Determine the minimum and maximum value of series dropping resistance R. [*Ans.* 158 Ω, 1 kΩ]

29. Design a Zener regulator for the following specifications: Output voltage, $V_o = 5$ V, Load current, $I_L = 20$ mA, Input voltage, $V_i = 12$ V ± 3V, Zener wattage, $P_z = 500$ mW.

[*Ans.* $R_L = 250$ Ω, $R = 83.33$ Ω to 200 Ω]

OBJECTIVE-TYPE QUESTIONS

1. A rectifier is used to
(a) convert ac voltage to dc voltage (b) convert dc voltage to ac voltage
(c) both ((a) and (b) (d) convert voltage to current

2. The maximum efficiency of a half-wave rectifier is
(a) 40.6% (b) 81.2% (c) 1.12% (d) 48.2%

3. In a full-wave rectifier, the current in each diode flows for
(a) whole cycle of the input signal (b) half-cycle of the input signal
(c) more than half-cycle of the input signal (d) none of the above

4. In a full-wave bridge rectifier, if V_m is the peak voltage across the secondary of the transformer, the maximum voltage coming across each reverse-biased diode is
(a) V_m (b) $2V_m$ (c) $\frac{1}{2}V_m$ (d) $\frac{V_m}{\sqrt{2}}$

5. The rectifier efficiency is
(a) $\frac{P_{dc}}{P_{ac}}$ (b) $\frac{\text{rms value}}{\text{average value}}$ (c) $\frac{\text{Peak value}}{\text{rms value}}$ (d) $\sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{dc}}}\right)^2 - 1}$

6. The major advantages of a bridge rectifier is that
(a) no centre-tap transformer is required
(b) the required peak inverse voltage of each diode is double that for a full-wave rectifier
(c) peak inverse voltage of each diode is half that for a full-wave rectifier
(d) the output is more smooth

7. The ripple factor decreases with
(a) decrease in C (b) increase in C
(c) increase in frequency (d) decrease in frequency

8. The primary function of a rectifier filter is to
(a) suppress odd harmonics (b) remove ripples
(c) stabilize the output dc level (d) minimize the input ac variations

9. The diode used in voltage regulator is
(a) *PN*-junction diode (b) varactor diode
(c) Zener diode (d) GUNN diode

10. A bleeder resistor is used in a dc power supply because it
(a) keeps the supply OFF (b) keeps the supply ON
(c) improves filtering action (d) improves voltage regulation

11. The ripple factor of a power supply is given by
(a) $\frac{P_{\text{dc}}}{P_{\text{ac}}}$ (b) $\sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{dc}}}\right)^2 - 1}$ (c) $\sqrt{\left(\frac{I_{\text{dc}}}{I_{\text{rms}}}\right) - 1}$ (d) $\frac{I_{\text{dc}}}{I_{\text{rms}}}$

12. For constructing a full-wave rectifier,
(a) at least two diodes are needed (b) more than two diodes are needed
(c) at least four diodes are needed (d) none of the above

13. Ripple factor of an ideal rectifier is
(a) 1 (b) 0 (c) infinity (d) none of the above

14. The bridge rectifier is preferable to a full-wave rectifier with centre-tap connections because it uses four diodes
(a) its transformer has no centre tap (b) it needs much small transformer for the same output
(c) it has higher safety factor (d) both (b) and (c)

15. In a rectifier, larger the value of shunt capacitor filter,
(a) larger the peak current in the rectifying diode
(b) smaller the dc voltage across the load
(c) longer the time that current pulse flows through the diode
(d) all of the above

16. In an *LC* filter, the ripple factor
(a) increases with the load current (b) increases with the load resistance
(c) remains constant with the load current (d) has the lowest value

17. Consider the following rectifier circuits:
1. Half-wave rectifier without filter
2. Full-wave rectifier without filter
3. Full-wave rectifier with series inductance filter
4. Full-wave rectifier with capacitance filter.

The sequence of these rectifier circuits in decreasing order of their ripple factor is
(a) 1, 2, 3, 4 (b) 3, 4, 1, 2 (c) 1, 4, 3, 2 (d) 3, 2, 1, 4

18. Zener breakdown is observed in a Zener diode having V_Z less than
(a) 5 V (b) 8 V (c) 50 V (d) 100 V

19. The RMS value of a half-wave rectified symmetrical square-wave current of 2 A is
(a) $\sqrt{2}$A (b) 1 A (c) $1/\sqrt{2}A$ (d) $\sqrt{3}A$

20. A constant current signal across a parallel *RLC* circuit gives an output of 1.4 V at the signal frequency of 3.89 kHz. At a frequency of 4 kHz, the output voltage will be
(a) 1 V (b) 2 V (c) 1.4 V (d) 2.8 V

4 Transistors

4.1 INTRODUCTION

A Bipolar Junction Transistor (BJT) is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogous to a vacuum triode and is comparatively smaller in size. It is used in amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

The quiescent operating point of a transistor amplifier should be established in the active region of its characteristics. Since the transistor parameters such as β, I_{CO} and V_{BE} are functions of temperature, the operating point shifts with changes in temperature. The stability of different methods of biasing transistor circuits and compensation techniques for stabilizing the operating point are discussed in this chapter.

4.2 BIPOLAR JUNCTION TRANSISTOR

4.2.1 Construction

The BJT consists of a silicon (or germanium) crystal in which a thin layer of *N*-type silicon is sandwiched between two layers of *P*-type silicon. This transistor is referred to as *PNP*. Alternatively, in an *NPN* transistor, a layer of *P*-type material is sandwiched between two layers of *N*-type material. The two types of the BJT are represented in Fig. 4.1.

The symbolic representation of the two types of the BJT is shown in Fig. 4.2. The three portions of the transistor are emitter, base, and collector, shown as *E*, *B*, and *C*, respectively. The arrow on the emitter specifies the direction of current flow when the *EB* junction is forward biased.

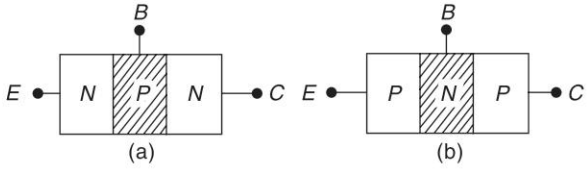


Fig. 4.1 *Transistor: (a) NPN (b) PNP*

The emitter is heavily doped so that it can inject a large number of charge carriers into the base. The base is lightly doped and very thin. It passes most of the injected charge carriers from the emitter into the collector. The collector is moderately doped.

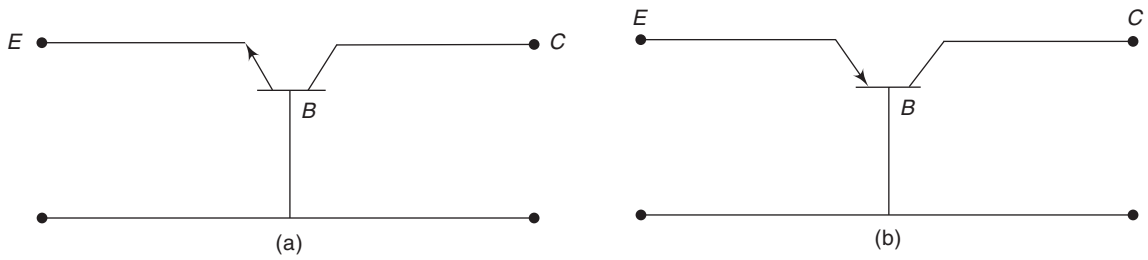


Fig. 4.2 *Circuit symbol: (a) NPN transistor (b) PNP transistor*

4.2.2 Transistor Biasing

As shown in Fig. 4.3, usually the emitter-base junction is forward biased and the collector-base junction is reverse biased. Due to the forward bias on the emitter-base junction, an emitter current flows through the base into the collector. Though the collector-base junction is reverse biased, almost the entire emitter current flows through the collector circuit.

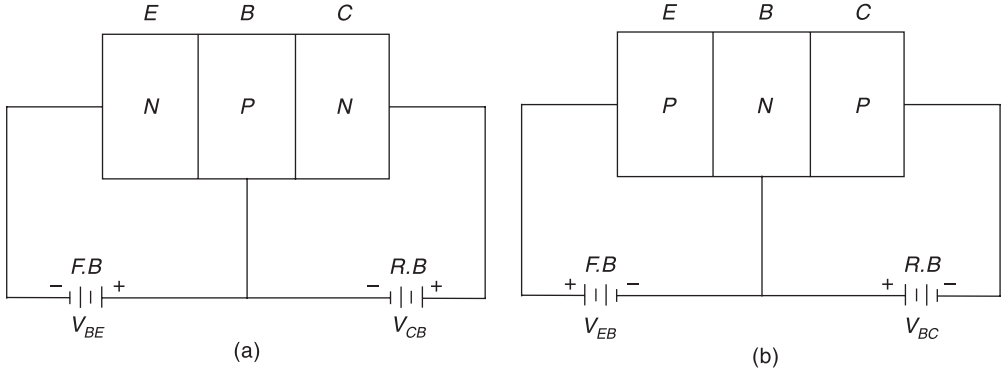


Fig. 4.3 *Transistor biasing: (a) NPN transistor (b) PNP transistor*

4.2.3 Operation of an NPN Transistor

As shown in Fig. 4.4, the forward bias applied to the emitter base junction of an *NPN* transistor causes a lot of electrons from the emitter region to cross over to the base region. As the base is lightly doped with *P*-type impurity, the number of holes in the base region is very small and, hence, the number of electrons that combine with holes in the *P*-type base region is also very small. Hence, a few electrons recombine with holes to constitute a base current I_B. The remaining electrons (more than 95 percent) cross over into the collector region to constitute a collector current I_C. Thus, the base and collector current summed up gives the emitter current, i.e., $I_E = -(I_C + I_B)$.

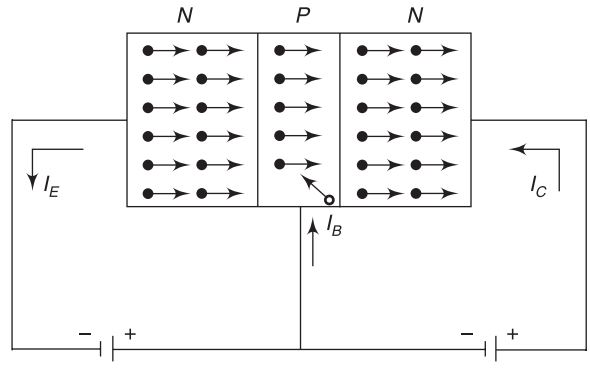


Fig. 4.4 *Current in an NPN transistor*

In the external circuit of the *NPN* bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B, and the collector current I_C are related by $I_E = I_C + I_B$.

4.2.4 Operation of a *PNP* Transistor

As shown in Fig. 4.5, the forward bias applied to the emitter-base junction of a *PNP* transistor causes a lot of holes from the emitter region to cross over to the base region as the base is lightly doped with *N*-type impurity. The number of electrons in the base region is very small and, hence, the number of holes combined with electrons in the *N*-type base region is also very small. Hence, a few holes combined with electrons to constitute a base current I_B. The remaining holes (more than 95 percent) cross over into the collector region to constitute a collector current I_C. Thus, the collector and base current when summed up gives the emitter current, i.e., $I_E = -(I_C + I_B)$.

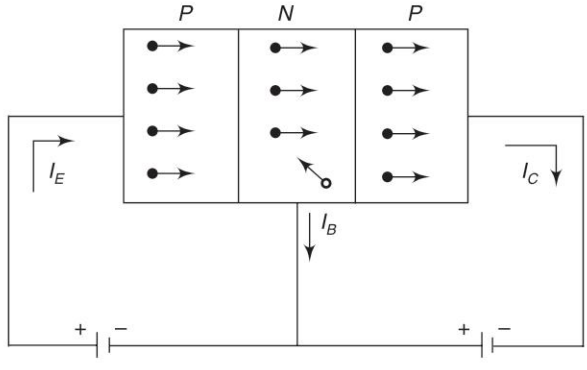


Fig. 4.5 *Current in a PNP transistor*

In the external circuit of the *PNP* bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B and the collector current I_C are related by

$$I_E = I_C + I_B \tag{4.1}$$

This equation gives the fundamental relationship between the currents in a bipolar transistor circuit. Also, this fundamental equation shows that there are current amplification factors α and β in common-base transistor configuration and common-emitter transistor configuration respectively for the static (dc) currents, and for small changes in the currents.

4.3 TRANSISTOR CURRENT COMPONENTS

4.3.1 Current Amplification Factor

In a transistor amplifier with ac input signal, the ratio of change in output current to the change in input current is known as the current amplification factor.

In the CB configuration, the current amplification factor, $\alpha = \dfrac{\Delta I_C}{\Delta I_E}$ (4.2)

In the CE configuration, the current amplification factor, $\beta = \dfrac{\Delta I_C}{\Delta I_B}$ (4.3)

In the CC configuration, the current amplification factor, $\gamma = \dfrac{\Delta I_E}{\Delta I_B}$ (4.4)

4.3.2 Relationship between α and β

We know that $\Delta I_E = \Delta I_C + \Delta I_B$

By definition, $\Delta I_C = \alpha \Delta I_E$

Therefore, $\Delta I_E = \alpha \Delta I_E + \Delta I_B$

i.e., $\Delta I_B = \Delta I_E (1 - \alpha)$

Dividing both sides by ΔI_C, we get

$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C}(1 - \alpha)$$

Therefore, $$\frac{1}{\beta} = \frac{1}{\alpha}(1 - \alpha)$$

$$\beta = \frac{\alpha}{(1 - \alpha)}$$

Rearranging, we also get $\alpha = \dfrac{\beta}{(1 + \beta)}$, or $\dfrac{1}{\alpha} - \dfrac{1}{\beta} = 1$ (4.5)

From this relationship, it is clear that as α approaches unity, β approaches infinity. The CE configuration is used for almost all transistor applications because of its high current gain, β.

4.3.3 Relation among α, β, and γ

In the CC transistor amplifier circuit, I_B is the input current and I_E is the output current.

From Eq. (4.2), $$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Substituting $\Delta I_B = \Delta I_E - \Delta I_C$,

we get $$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator on RHS by ΔI_E, we get

$$\gamma = \frac{\dfrac{\Delta I_E}{\Delta I_E}}{\dfrac{\Delta I_E}{\Delta I_E} - \dfrac{\Delta I_C}{\Delta I_E}} = \frac{1}{1 - \alpha}$$

Therefore, $$\gamma = \frac{1}{1 - \alpha} = (\beta + 1)$$ (4.6)

4.3.4 Large-Signal Current Gain (α)

The large-signal current gain of a common-base transistor is defined as the ratio of the negative of the collector-current increment to the emitter-current change from cut-off ($I_E = 0$) to I_E, i.e.,

$$\alpha = \frac{(I_C - I_{CBO})}{I_E - 0} \tag{4.7}$$

where I_{CBO} (or I_{CO}) is the reverse saturation current flowing through the reverse-biased collector-base junction, i.e., the collector-to-base leakage current with the emitter open. As the magnitude of I_{CBO} is negligible when compared to I_C, the above expression can be written as

$$\alpha = \frac{I_C}{I_E} \tag{4.8}$$

Since I_C and I_E are flowing in opposite directions, α is always positive. The typical value of α ranges from 0.90 to 0.995. Also, α is not a constant but varies with emitter current I_E, collector voltage V_{CB}, and temperature.

4.3.5 General Transistor Equation

In the active region of the transistor, the emitter-base junction is forward biased and the collector-base junction is reverse biased. The generalized expression for collector current I_C for collector junction voltage V_C and emitter current I_E is given by

$$I_C = -\alpha I_E + I_{CBO}\left(1 - e^{V_C/V_T}\right) \tag{4.9}$$

If V_C is negative and $|V_C|$ is very large compared with V_T, then the above equation reduces to

$$I_C = -\alpha I_E + I_{CBO} \tag{4.10}$$

If V_C, i.e., V_{CB}, is a few volts, then I_C is independent of V_C. Hence, the collector current I_C is determined only by the fraction α of the current I_E flowing in the emitter.

4.3.6 Relation Among I_C, I_B, and I_{CBO}

From Eq. (4.10), we have

$$I_C = -\alpha I_E + I_{CBO}$$

Since I_C and I_E are flowing in opposite directions,

$$I_E = -(I_C + I_B)$$

Therefore,

$$I_C = -\alpha[-(I_C + I_B)] + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

Since

$$\beta = \frac{\alpha}{1-\alpha}, \tag{4.11}$$

the above expression becomes

$$I_C = (1+\beta)\, I_{CBO} + \beta I_B \tag{4.12}$$

4.3.7 Relation Among I_C, I_B, and I_{CEO}

In the common-emitter (CE) transistor circuit, I_B is the input current and I_C is the output current. If the base circuit is open, i.e., $I_B = 0$, then a small collector current flows from the collector to emitter. This is denoted as I_{CEO}, the collector-emitter current with base open. This current I_{CEO} is also called the collector-to-emitter leakage current.

In this CE configuration of the transistor, the emitter-base junction is forward-biased and collector-base junction is reverse-biased and, hence, the collector current I_C is the sum of the part of the emitter current I_E that reaches the collector, and the collector-emitter leakage current I_{CEO}. Therefore, the part of I_E, which reaches collector is equal to $(I_C - I_{CEO})$.

Hence, the *large-signal current gain* (β) is defined as,

$$\beta = \frac{(I_C - I_{CEO})}{I_B} \tag{4.13}$$

From the equation, we have

$$I_C = \beta I_B + I_{CEO} \tag{4.14}$$

4.3.8 Relation Between I_{CBO} and I_{CEO}

Comparing Eqs (4.12) and (4.14), we get the relationship between the leakage currents of transistor common-base (CB) and common-emitter (CE) configurations as

$$I_{CEO} = (1 + \beta)\, I_{CBO} \tag{4.15}$$

From this equation, it is evident that the collector-emitter leakage current (I_{CEO}) in CE configuration is $(1 + \beta)$ times larger than that in CB configuration. As I_{CBO} is temperature-dependent, I_{CEO} varies by large amount when temperature of the junctions changes.

- **Expression for Emitter Current** The magnitude of emitter current is

$$I_E = I_C + I_B$$

Substituting Eq. (4.12) in the above equation, we get

$$I_E = (1 + \beta)\, I_{CBO} + (1 + \beta)\, I_B \tag{4.16}$$

Substituting Eq. (4.11) into Eq. (4.16), we have

$$I_E = \frac{1}{1 - \alpha} I_{CBO} + \frac{1}{1 - \alpha} I_B \tag{4.17}$$

4.3.9 dc Current Gain (β_{dc} or h_{FE})

The dc current gain is defined as the ratio of the collector current I_C to the base current I_B. That is,

$$\beta_{dc} = h_{FE} = \frac{I_C}{I_B} \tag{4.18}$$

As I_C is large compared with I_{CEO}, the large-signal current gain (β) and the dc current gain (h_{FE}) are approximately equal.

4.4 CHARACTERISTICS OF TRANSISTOR (CE, CB AND CC CONFIGURATIONS)

When a transistor is to be connected in a circuit, one terminal is used as an input terminal, the other terminal is used as an output terminal, and the third terminal is common to the input and output. Depending upon the input, output, and common terminals, a transistor can be connected in three configurations. They are (i) Common Base (CB) configuration, (ii) Common Emitter (CE) configuration, and (iii) Common Collector (CC) configuration.

- **CB Configuration** This is also called *grounded-base configuration*. In this configuration, the emitter is the input terminal, the collector is the output terminal, and the base is the common terminal.

- **CE Configuration** This is also called *grounded-emitter configuration*. In this configuration, the base is the input terminal, the collector is the output terminal, and the emitter is the common terminal.

- **CC Configuration** This is also called *grounded-collector configuration*. In this configuration, the base is the input terminal, the emitter is the output terminal, and the collector is the common terminal.

The supply voltage connections for normal operation of an *NPN* transistor in the three configurations are shown in Fig. 4.6.

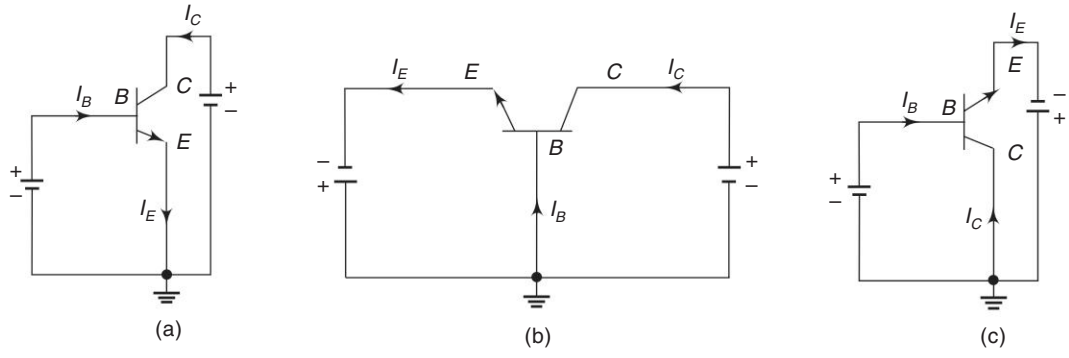


Fig. 4.6 *Transistor configuration: (a) Common emitter (b) Common base (c) Common collector*

4.4.1 CB Configuration

The circuit diagram for determining the static characteristics curves of an *NPN* transistor in the common-base configuration is shown in Fig. 4.7.

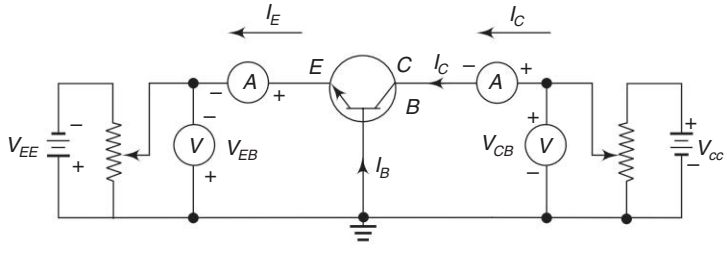


Fig. 4.7 *Circuit to determine CB static characteristics*

➤ ***Input Characteristics*** To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volt and the emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}. The input characteristics thus obtained are shown in Fig. 4.8.

When V_{CB} is equal to zero and the emitter-base junction is forward biased as shown in the characteristics, the junction behaves as a forward-biased diode so that emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}. When V_{CB} is increased keeping V_{EB} constant, the width of the base region will decrease. This effect results in an increase of I_E. Therefore, the curves shift towards the left as V_{CB} is increased.

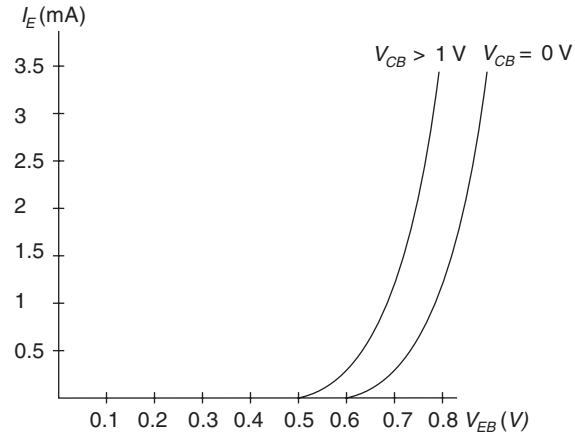


Fig. 4.8 *CB input characteristics*

➤ ***Output Characteristics*** To determine the output characteristics, the emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}. Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of I_E. This is repeated for different fixed values of I_E. Now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in Fig. 4.9.

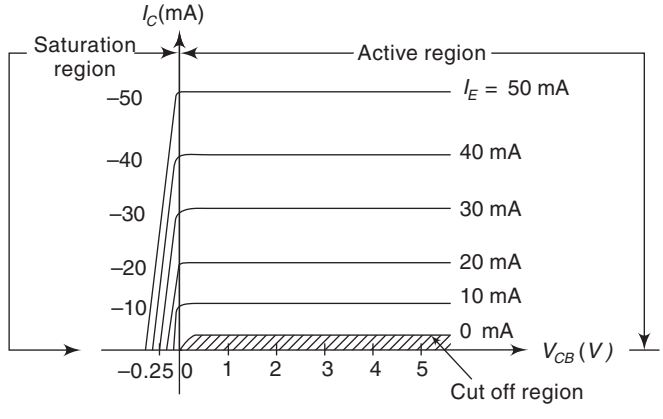


Fig. 4.9 *CB output characteristics*

From the characteristics, it is seen that for a constant value of I_E, I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CB}. Further, I_C flows even when V_{CB} is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e., electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse-biased collector-base junction, they flow to the collector region and give rise to I_C even when V_{CB} is equal to zero.

➤ ***Early Effect or Base Width Modulation*** As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the

effective width of the base decreases. This dependency of base width on collector-to-base voltage is known as the *Early effect*. This decrease in effective base width has three consequences:

(i) There is less chance for recombination within the base region. Hence, α increases with increasing $|V_{CB}|$.

(ii) The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

(iii) For extremely large voltages, the effective base width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the *punch-through*.

For higher values of V_{CB}, due to Early effect, the value of α increases. For example, α changes, say from 0.98 to 0.985. Hence, there is a very small positive slope in the CB output characteristics and, hence, the output resistance is not zero.

➤ ***Transistor Parameters*** The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common-base *hybrid parameters* or *h-parameters*.

▪ **Input Impedance (h_{ib})** It is defined as the ratio of the change in (input) emitter voltage to the change in (input) emitter current with the (output) collector voltage V_{CB} kept constant. Therefore,

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, V_{CB} \text{ constant} \tag{4.19}$$

It is the slope of CB input characteristics I_E versus V_{EB} as shown in Fig. 4.8. The typical value of h_{ib} ranges from 20 Ω to 50 Ω.

▪ **Output Admittance (h_{ob})** It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) emitter current I_E kept constant. Therefore,

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, I_E \text{ constant} \tag{4.20}$$

It is the slope of CB output characteristics I_C versus V_{CB} as shown in Fig. 4.9. The typical value of this parameter is of the order of 0.1 to 10 μ mhos.

▪ **Forward Current Gain (h_{fb})** It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant. Hence,

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, V_{CB} \text{ constant} \tag{4.21}$$

It is the slope of I_C versus I_E curve. Its typical value varies from 0.9 to 1.0.

▪ **Reverse Voltage Gain (h_{rb})** It is defined as the ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current, I_E. Hence,

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, I_E \text{ constant} \tag{4.22}$$

It is the slope of V_{EB} versus V_{CB} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.

4.4.2 CE Configuration

➤ ***Input Characteristics*** To determine the input characteristics, the collector-to-emitter voltage is kept constant at zero volt, and the base current is increased from zero in equal steps by increasing V_{BE} in the circuit shown in Fig. 4.10.

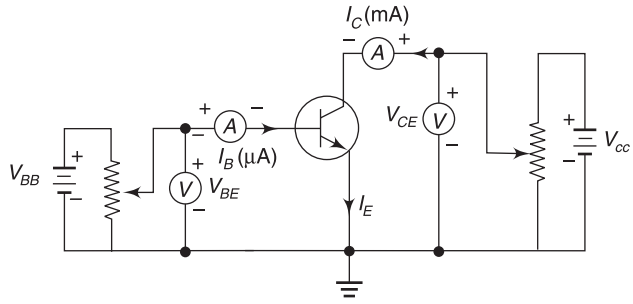


Fig. 4.10 *Circuit to determine CE static characteristics*

The value of V_{BE} is noted for each setting of I_B. This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B V_s. V_{BE} are drawn. The input characteristics thus obtained are shown in Fig. 4.11.

When $V_{CE} = 0$, the emitter-base junction is forward biased and the junction behaves as a forward biased diode. Hence, the input characteristic for $V_{CE} = 0$ is similar to that of a forward-biased diode. When V_{CE} is increased, the width of the depletion region at the reverse-biased collector-base junction will increase. Hence, the effective width of the base will decrease. This effect causes a decrease in the base current I_B. Hence, to get the same value of I_B as that for $V_{CE} = 0$, V_{BE} should be increased. Therefore, the curve shifts to the right as V_{CE} increases.

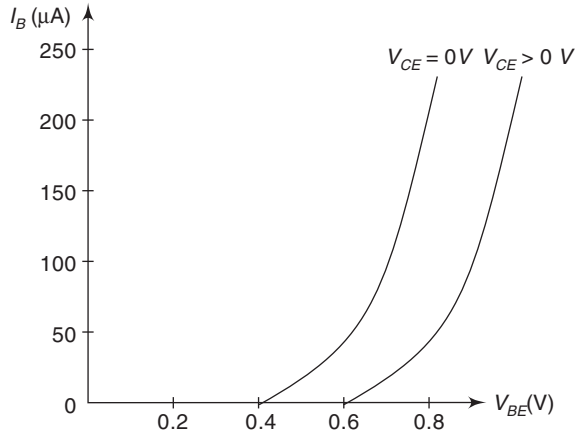


Fig. 4.11 *CE input characteristics*

➤ ***Output Characteristics*** To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting the base-emitter voltage, V_{BE}. The magnitude of the collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting V_{CE}. Now, the curves of I_C versus V_{CE} are plotted for different constant values of I_B. The output characteristics thus obtained are shown in Fig. 4.12.

From Eqs. (4.11) and (4.12), we have

$$\beta = \frac{\alpha}{1-\alpha} \quad \text{and} \quad I_C = (1+\beta)\, I_{CBO} + \beta I_B$$

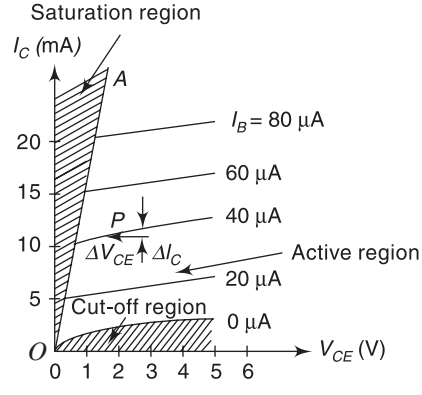


Fig. 4.12 *CE output characteristics*

For larger values of V_{CE}, due to Early effect, a very small change in α is reflected as a very large change in β. For example, when $\alpha = 0.98$, $\beta = \frac{0.98}{1 - 0.98} = 49$. If α increases to 0.985, then $\beta = \frac{0.985}{1 - 0.985} = 66$. Here, a slight increase in α by about 0.5 percent results in an increase in β by about 34 percent. Hence, the output characteristics of CE configuration show a larger slope when compared with CB configuration.

The output characteristics have three regions, namely, saturation region, cut-off region, and active region. The region of curves to the left of the line *OA* is called the *saturation region* (hatched), and the line *OA* is called the saturation line. In this region, both junctions are forward biased and an increase in the base current does not cause a corresponding large change in I_C. The ratio of $V_{CE(sat)}$ to I_C in this region is called saturation resistance.

The region below the curve for $I_B = 0$ is called the *cut-off region* (hatched). In this region, both junctions are reverse biased. When the operating point for the transistor enters the cut-off region, the transistor is OFF. Hence, the collector current becomes almost zero and the collector voltage almost equals V_{CC}, the collector-supply voltage. The transistor is virtually an open circuit between collector and emitter.

The central region where the curves are uniform in spacing and slope is called the *active region* (unhatched). In this region, emitter-base junction is forward biased and the collector-base junction is reverse biased. If the transistor is to be used as a linear amplifier, it should be operated in the active region.

If the base current is subsequently driven large and positive, the transistor switches into the saturation region via the active region, which is traversed at a rate that is dependent on factors such as gain and frequency response. In this ON condition, large collector current flows and collector voltage falls to a very low value, called $V_{CE\text{sat}}$, typically around 0.2 V for a silicon transistor. The transistor is virtually a short circuit in this state.

High-speed switching circuits are designed in such a way that transistors are not allowed to saturate, thus reducing switching times between ON and OFF times.

➤ *Transistor Parameters*

The slope of the CE characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common-emitter *hybrid parameters* or *h-parameters.*

- **Input Impedance (h_{ie})** It is defined as the ratio of the change in (input) base voltage to the change in (input) base current with the (output) collector voltage V_{CE} kept constant. Therefore,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, V_{CE} \text{ constant} \tag{4.23}$$

It is the slope of CE input characteristics I_B versus V_{BE} as shown in Fig. 4.11. The typical value of h_{ie} ranges from 500 to 2000 Ω.

- **Output Admittance (h_{oe})** It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) base current I_B kept constant. Therefore,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, I_B \text{ constant} \tag{4.24}$$

It is the slope of CE output characteristic I_C versus V_{CE} as shown in Fig. 4.12. The typical value of this parameter is of the order of 0.1 to 10 μ mhos.

- **Forward Current Gain (h_{fe})** It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) base current keeping the (output) collector voltage V_{CE} constant. Hence,

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, V_{CE} \text{ constant} \tag{4.25}$$

It is the slope of I_C versus I_B curve. Its typical value varies from 20 to 200.

- **Reverse Voltage Gain (h_{re})** It is defined as the ratio of the change in the (input) base voltage and the corresponding change in (output) collector voltage with constant (input) base current, I_B. Hence,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, I_B \text{ constant} \tag{4.26}$$

It is the slope of V_{BE} versus V_{CE} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.

➤ *Derivation of analytical expression for CE output characteristics of BJT*

We know that, for a *PNP* transistor, the collector-emitter voltage V_{CE} is given by

$$V_{CE} = V_C - V_E$$

where $V_C = V_T \ln\left(1 - \frac{\alpha_N I_E + I_C}{I_{CO}}\right)$ and $V_E = V_T \ln\left(1 - \frac{\alpha_I I_C + I_E}{I_{EO}}\right)$.

Here, α_N is the current gain when the transistor is in the normal operation and α_I is the current gain when the transistor is in the inverted operation.

Therefore,

$$\begin{aligned} V_{CE} &= V_T \ln\left(1 - \frac{\alpha_N I_E + I_C}{I_{CO}}\right) - V_T \ln\left(1 - \frac{\alpha_I I_C + I_E}{I_{EO}}\right) \\ &= V_T \ln\left(\frac{I_{CO} - \alpha_N I_E - I_C}{I_{CO}}\right) - V_T \ln\left(\frac{I_{EO} - \alpha_I I_C - I_E}{I_{EO}}\right) \\ &= V_T \ln\left(\frac{I_{CO} - \alpha_N I_E - I_C}{I_{EO} - \alpha_I I_C - I_E}\right)\left(\frac{I_{EO}}{I_{CO}}\right) \end{aligned}$$

We know that, $I_E = -(I_B + I_C)$

Hence,

$$\begin{aligned} V_{CE} &= V_T \ln\left(\frac{I_{CO} + \alpha_N I_B + \alpha_N I_C - I_C}{I_{EO} - \alpha_I I_C + I_B + I_C}\right)\left(\frac{\alpha_I}{\alpha_N}\right) \qquad \left(\text{since } \frac{I_{EO}}{I_{CO}} = \frac{\alpha_I}{\alpha_N}\right) \\ &= V_T \ln\left(\frac{I_{CO} + \alpha_N I_B + (\alpha_N - 1) I_C}{I_{EO} + I_B + (1 - \alpha_I) I_C}\right)\left(\frac{\alpha_I}{\alpha_N}\right) \\ &= V_T \ln\frac{\alpha_I}{\alpha_N} + V_T \ln\left(\frac{I_{CO} + \alpha_N I_B - I_C(1 - \alpha_N)}{I_{EO} + I_B + I_C(1 - \alpha_I)}\right) \end{aligned}$$

If $I_B >> I_{EO}$ and $I_B >> \dfrac{I_{CO}}{\alpha_N}$, we have

$$V_{CE} = V_T \ln\left[\left(\frac{\alpha_I}{\alpha_N}\right)\left(\frac{\alpha_N I_B - I_C(1-\alpha_N)}{I_B + I_C(1-\alpha_I)}\right)\right]$$

$$= V_T \ln\left[\frac{I_B - \left(\dfrac{1-\alpha_N}{\alpha_N}\right) I_C}{\dfrac{I_B}{\alpha_I} + \left(\dfrac{1-\alpha_I}{\alpha_I}\right) I_C}\right]$$

Now dividing both numerator and denominator by I_B, we get

$$V_{CE} = V_T \ln\left[\frac{1 - \left(\dfrac{1-\alpha_N}{\alpha_N}\right)\dfrac{I_C}{I_B}}{\dfrac{1}{\alpha_I} + \left(\dfrac{1-\alpha_I}{\alpha_I}\right)\dfrac{I_C}{I_B}}\right]$$

$$= V_T \ln\left[\frac{1 - \dfrac{1}{\beta_N}\dfrac{I_C}{I_B}}{\dfrac{1}{\alpha_I} + \dfrac{1}{\beta_I}\dfrac{I_C}{I_B}}\right] \quad \left(\text{since} \quad \beta = \frac{\alpha}{1-\alpha}\right)$$

or

$$V_{CE} = -V_T \ln\left[\frac{\dfrac{1}{\alpha_I} + \dfrac{1}{\beta_I}\dfrac{I_C}{I_B}}{1 - \dfrac{1}{\beta_N}\dfrac{I_C}{I_B}}\right]$$

Here, if $I_C = 0$, $V_{CE} = -V_T \ln\left(\dfrac{1}{\alpha_I}\right)$. This shows that V_{CE} is not equal to zero even if I_C becomes zero and hence, the common emitter characteristic curves do not pass through the origin.

4.4.3 CC Configuration

The circuit diagram for determining the static characteristics of an *NPN* transistor in the common collector configuration is shown in Fig. 4.13.

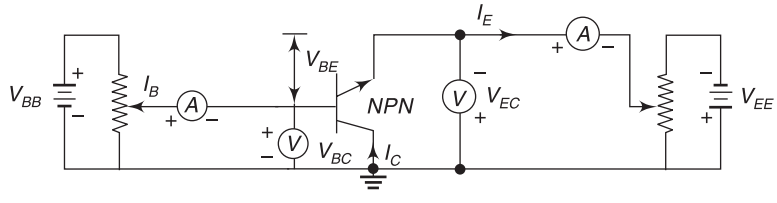


Fig. 4.13 *Circuit to determine CC static characteristics*

➤ ***Input Characteristics*** To determine the input characteristics, V_{EC} is kept at a suitable fixed value. The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. Plots of V_{BC} versus I_B for different values of V_{EC} shown in Fig. 4.14 are the input characteristics.

➤ ***Output Characteristics*** To determine the output characteristics, the base current, I_B, is kept constant at a suitable value by adjusting the base-collector voltage, V_{BC}. The magnitude of the emitter-collector voltage, V_{EC}, is increased in suitable equal steps from zero and the emitter current, I_E, is noted for each setting V_{EC}. Now, the curves of I_E versus V_{EC} are plotted for different constant values of I_B. The output characteristics thus obtained are shown in Fig. 4.15. These output characteristics are the same as those of the common emitter configuration.

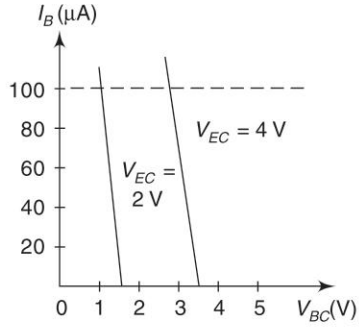


Fig. 4.14 *CC input characteristics*

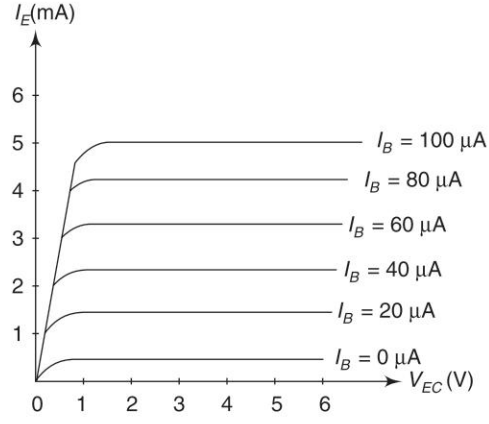


Fig. 4.15 *CC output characteristics*

4.4.4 Comparison of Different Configurations

Table 4.1 *A comparison of CB, CE, and CC configurations*

Property	CB	CE	CC
Input resistance	Low (about 100 Ω)	Moderate (about 750 Ω)	High (about 750 kΩ)
Output resistance	High (about 450 kΩ)	Moderate (about 45 kΩ)	Low (about 25 Ω)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift between input and output voltages	0 or 360°	180°	0 or 360°
Applications	for high frequency circuits	for audio frequency circuits	for impedance matching

4.5 TRANSISTOR AS AN AMPLIFIER

➤ ***CE Transistor as an Amplifier*** Figure 4.16(a) shows an amplifier circuit using CE transistor configuration. In this circuit, an NPN transistor is used in CE configuration. Here, V_{BB} supply will forward bias the emitter-base junction and V_{CC} supply will reverse bias the collector-base junction. This biasing

arrangement makes the transistor to operate in the active region. The magnitude of the input ac signal v_i always forward bias the emitter-base junction regardless of the polarity of the signal.

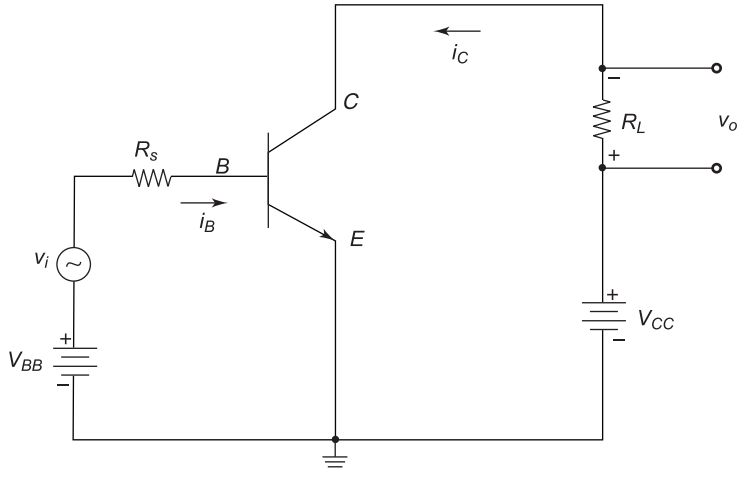


Fig. 4.16(a) *CE transistor as an amplifier*

During the positive half cycle of the input signal v_i, the forward bias across the emitter-base junction is increased. As a result, more electrons are injected into the base and reaches the collector, resulting in an increase in collector current i_c. This increase in collector current produces a greater voltage drop across the load resistance R_L.

However, during the negative half cycle of the input signal v_i, the forward bias across the emitter-base junction is decreased, resulting in a decrease in collector current i_c. This decrease in collector current produces a smaller voltage drop across the load resistance R_L. Hence, it is clear that a small change in the input ac signal in CE transistor amplifier produces a large change at the output with a voltage gain of around 500 and a phase shift of 180°. Here, the voltage gain is the ratio of output voltage to input voltage. Comparing to *CB* and *CC* transistor configurations, this *CE* transistor configuration is widely used in amplifier circuits due to its high voltage gain.

➤ ***CB Transistor as an Amplifier*** A load resistor R_L is connected in series with the collector supply voltage V_{CC} of the CB transistor configuration as shown in Fig. 4.16(b).

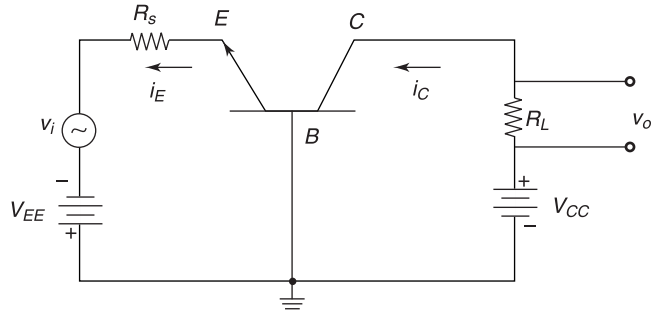


Fig. 4.16(b) *CB transistor as an amplifier*

A small change in the input voltage between emitter and base, say ΔV_i, causes a relatively larger change in the emitter current, say ΔI_E. A fraction of this change in current is collected and passed through R_L and is denoted by the symbol α'. Therefore, the corresponding change in voltage across the load resistor R_L due to this current is $\Delta V_0 = \alpha' R_L \Delta I_E$.

Here, the voltage amplification $A_v = \dfrac{\Delta V_0}{\Delta V_i}$ is around 150 without any phase shift and thus, the transistor acts as an amplifier.

4.6 LARGE SIGNAL, dc AND SMALL-SIGNAL CE VALUES OF CURRENT GAIN

We know from the characteristics of CE configuration, the current amplification factor is $\beta \equiv \dfrac{\alpha}{1-\alpha}$,

and $I_C = (1 + \beta)\, I_{CBO} + \beta I_B$.

The above equation can be expressed as

$$I_C - I_{CBO} = \beta I_{CBO} + \beta I_B$$

Therefore,
$$\beta = \frac{I_C - I_{CBO}}{I_B - (-I_{CBO})}$$

The output characteristics of CE configuration show that in the *cut-off* region, the values $I_E = 0$, $I_C = I_{CBO}$, and $I_B = -I_{CBO}$. Therefore, the above equation gives the ratio of the collector-current increment to the base-current change from cut-off to I_B, and, hence, β *is called the large-signal current gain of common-emitter transistor*.

The dc current gain of the transistor is given by

$$\beta_{\text{dc}} \equiv h_{FE} \equiv \frac{I_C}{I_B}$$

Based on this h_{FE} value, we can determine whether the transistor is in saturation or not. For any transistor, in general, I_B is large compared to I_{CBO}. Under this condition, the value of $h_{FE} \approx \beta$.

The small-signal CE forward short-circuit gain β' is defined as the ratio of a collector-current increment ΔI_C for a small base-current change ΔI_B, at a fixed collector-to-emitter voltage V_{CE}.

i.e.,
$$\beta' \equiv \left.\frac{\partial I_C}{\partial I_B}\right|_{V_{CE}}$$

If β is independent of currents then $\beta' = \beta \approx h_{FE}$. However, β is a function of current, then $\beta' = \beta + (I_{CBO} + I_B)\, \dfrac{\partial \beta}{\partial I_B}$. By using $\beta' = h_{fe}$ and $\beta \approx h_{FE}$. Therefore, the above equation becomes

$$h_{fe} = \frac{h_{FE}}{1 - (I_{CBO} + I_B)\dfrac{\partial h_{FE}}{\partial I_C}}$$

In Fig. 4.17, the h_{FE} versus I_C shows a maximum and, hence, $h_{fe} > h_{FE}$ for smaller currents, and $h_{fe} < h_{FE}$ for larger currents. Therefore, the above equation is valid only for the active region.

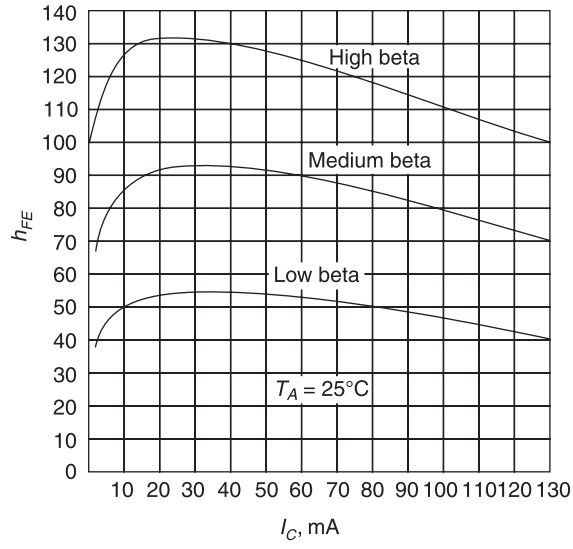


Fig. 4.17 *Characteristic curves of dc current gain h_{FE} (at V_{CE} = −0.25 V) versus collector current for low, medium, and high beta values*

EXAMPLE 4.1

In a common-base transistor circuit, the emitter current I_E is 10 mA and the collector current I_C is 9.8 mA. Find the value of the base current I_B.

Solution Given $I_E = 10$ mA and $I_C = 9.8$ mA

We know that emitter current is

$$I_E = I_B + I_C$$

i.e., $$10 \times 10^{-3} = I_B + 9.8 \times 10^{-3}$$

Therefore, $$I_B = 0.2 \text{ mA}$$

EXAMPLE 4.2

In a common-base connection, the emitter current I_E is 6.28 mA and the collector current I_C is 6.20 mA. Determine the common-base dc current gain.

Solution Given, $I_E = 6.28$ mA and $I_C = 6.20$ mA

We know that common-base dc current gain,

$$\alpha = \frac{I_C}{I_E} = \frac{6.20 \times 10^{-3}}{6.28 \times 10^{-3}} = 0.987$$

EXAMPLE 4.3

The common-base dc current gain of a transistor is 0.967. If the emitter current is 10 mA, what is the value of base current?

Solution Given $\alpha = 0.967$ and $I_E = 10$ mA

The common-base dc current gain (α) is

$$\alpha = 0.967 = \frac{I_C}{I_E} = \frac{I_C}{10 \times 10^{-3}}$$

Therefore, $I_C = 0.967 \times 10 \times 10^{-3} = 9.67$ mA

The emitter current $I_E = I_B + I_C$

i.e., $10 \times 10^{-3} = I_B + 9.67 \times 10^{-3}$

Therefore, $I_B = 0.33$ mA

EXAMPLE 4.4

The transistor has $I_E = 10$ mA and $\alpha = 0.98$. Determine the values of I_C and I_B.

Solution Given, $I_E = 10$ mA and $\alpha = 0.98$

The common-base dc current gain, $\alpha = \frac{I_C}{I_E}$

i.e., $0.98 = \frac{I_C}{10 \times 10^{-3}}$

Therefore, $I_C = 0.98 \times 10 \times 10^{-3} = 9.8$ mA

The emitter current $I_E = I_B + I_C$

i.e., $10 \times 10^{-3} = I_B + 9.8 \times 10^{-3}$

Therefore, $I_B = 0.2$ mA

EXAMPLE 4.5

If a transistor has a α of 0.97, find the value of β. If $\beta = 200$, find the value of α.

Solution If $\alpha = 0.97$, $\beta = \frac{\alpha}{1-\alpha} = \frac{0.97}{1-0.97} = 32.33$

If $\beta = 200$, $\alpha = \frac{\beta}{\beta+1} = \frac{200}{200+1} = 0.995$

EXAMPLE 4.6

A transistor has $\beta = 100$. If the collector current is 40 mA, find the value of the emitter current.

Solution Given, $\beta = 100$ and $I_C = 40$ mA

$$\beta = 100 = \frac{I_C}{I_B} = \frac{40 \times 10^{-3}}{I_B}$$

Therefore, $I_B = 40 \times 10^{-3}/100 = 0.4$ mA and

$I_E = I_B + I_C = (0.4 + 40) \times 10^{-3} = 40.4$ mA

EXAMPLE 4.7

A transistor has $\beta = 150$. Find the collector and base currents, if $I_E = 10$ mA.

Solution Given, $\beta = 150$ and $I_E = 10$ mA

The common-base current gain, $\alpha = \frac{\beta}{\beta + 1} = \frac{150}{150 + 1} = 0.993$

Also, $\alpha = \frac{I_C}{I_E}$

i.e., $0.993 = \frac{I_C}{10}$

Therefore, $I_C = 0.993 \times 10 \times 10^{-3} = 9.93$ mA

The emitter current $I_E = I_B + I_C$

i.e., $10 \times 10^{-3} = I_B + 9.93 \times 10^{-3}$

Therefore, $I_B = (10 - 9.93) \times 10^{-3} = 0.07$ mA

EXAMPLE 4.8

Determine the values of I_B and I_E for the transistor circuit if $I_C = 80$ mA and $\beta = 170$.

Solution Given, $\beta = 170$ and $I_C = 80$ mA

We know that (β), $\beta = 170 = \frac{I_C}{I_B} = \frac{80 \times 10^{-3}}{I_B}$

Therefore, $I_B = \frac{80 \times 10^{-3}}{170} = 0.47$ mA

and $I_E = I_B + I_C = (0.47 + 80)$ mA $= 80.47$ mA

EXAMPLE 4.9

Determine the values of I_C and I_E for the transistor circuit of $\beta = 200$ and $I_B = 0.125$ mA.

Solution Given, $I_B = 0.125$ mA and $\beta = 200$

Therefore, $\beta = 200 = \frac{I_C}{I_B} = \frac{I_C}{0.125 \times 10^{-3}}$

Therefore, $I_C = 200 \times 0.125 \times 10^{-3} = 25$ mA

and $I_E = I_B + I_C = (0.125 + 25) \times 10^{-3} = 25.125$ mA

EXAMPLE 4.10

Determine the values of I_C and I_B for the transistor circuit of $I_E = 12$ mA and $\beta = 100$.

Solution Given, $I_E = 12$ mA and $\beta = 100$

We know that base current, $I_B = \dfrac{I_E}{1+\beta} = \dfrac{12 \times 10^{-3}}{1+100} = 0.1188$ mA

and collector current, $I_C = I_E - I_B = (12 - 0.1188) \times 10^{-3} = 11.8812$ mA

EXAMPLE 4.11

A transistor has $I_B = 100$ μA and $I_C = 2$ μA. Find (a) β of the transistor, (b) α of the transistor, (c) emitter current I_E, and (d) if I_B changes by + 25 μA and I_C changes by + 0.6 mA, find the new value of β.

Solution Given, $I_B = 100$ μA $= 100 \times 10^{-6}$ A and $I_C = 2$ mA $= 2 \times 10^{-3}$ A.

(a) To find β of the transistor

$$\beta = \frac{I_C}{I_B} = \frac{2 \times 10^{-3}}{100 \times 10^{-6}} = 20$$

(b) To find α of the transistor

$$\alpha = \frac{\beta}{\beta + 1} = \frac{20}{1+20} = 0.952$$

(c) To find emitter current, I_E

$$I_E = I_B + I_C = 100 \times 10^{-6} + 2 \times 10^{-3} \text{ A}$$
$$= (0.01 + 2) \times 10^{-3} = 2.01 \times 10^{-3} \text{ A} = 2.01 \text{ mA}$$

(d) To find the new value of β when $\Delta I_B = 25$ μA and $\Delta I_C = 0.6$ mA

Therefore, $I_B = (100 + 25)$ μA $= 125$ μA

$I_C = (2 + 0.6)$ mA $= 2.6$ mA

New value of β of the transistor,

$$\beta = \frac{I_C}{I_B} = \frac{2.6 \times 10^{-3}}{125 \times 10^{-6}} = 20.8$$

EXAMPLE 4.12

For a transistor circuit having $\alpha = 0.98$, $I_{CBO} = I_{CO} = 5$ μA, and $I_B = 100$ μA, find I_C and I_E.

Solution Given, $\alpha = 0.98$, $I_{CBO} = I_{CO} = 5$ μA and $I_B = 100$ μA

The collector current is

$$I_C = \frac{\alpha \cdot I_B}{1-\alpha} + \frac{I_{CO}}{1-\alpha} = \frac{0.98 \times 100 \times 10^{-6}}{1 - 0.98} + \frac{5 \times 10^{-6}}{1 - 0.98} = 5.15 \text{ mA}$$

The emitter current is

$$I_E = I_B + I_C = 100 \times 10^{-6} + 5.15 \times 10^{-3} = 5.25 \text{ mA}$$

EXAMPLE 4.13

A germanium transistor used in a complementary symmetry amplifier has $I_{CBO} = 10\ \mu A$ at 27°C and $h_{FE} = 50$. (a) Find I_C when $I_B = 0.25$ mA, and (b) assuming h_{FE} does not increase with temperature, find the value of new collector current, if the transistor's temperature rises to 50°C.

Solution Given, $I_{CBO} = 10\ \mu A$ and $h_{FE}\ (= \beta) = 50$

(a) To find the value of collector current when $I_B = 0.25$ mA

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

$$= 50 \times (0.25 \times 10^{-3}) + (1 + 50) \times (10 \times 10^{-6})\ A = 13.01\ mA$$

(b) To find the value of new collector current if the temperature rises to 50°C

We know that I_{CBO} doubles for every 10°C rise in temperature. Therefore,

$$I'_{CBO}\ (\beta = 50) = I_{CBO} \times 2^{(T_2 - T_1)/10} = 10 \times 2^{(50 - 27)/10}\ \mu A$$

$$= 10 \times 2^{2.3}\ \mu A = 49.2\ \mu A$$

Therefore, the collector current at 50°C is

$$I_C = \beta \cdot I_B + (1 + \beta) I'_{CBO}$$

$$= 50 \times (0.25 \times 10^{-3}) + (1 + 50) \times 49.2 \times 10^{-6} = 15.01\ mA$$

EXAMPLE 4.14

When the emitter current of a transistor is changed by 1 mA, there is a change in collector current by 0.99 mA. Find the current gain of the transistor.

Solution The current gain of the transistor is $\alpha = \dfrac{\Delta I_C}{\Delta I_E} = \dfrac{0.99 \times 10^{-3}}{1 \times 10^{-3}} = 0.99$

EXAMPLE 4.15

The dc current gain of a transistor in CE mode is 100. Determine its dc current gain in CB mode.

Solution The dc current gain of the transistor in CB mode is

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} = \frac{100}{1 + 100} = 0.99$$

EXAMPLE 4.16

When I_E of a transistor is changed by 1 mA, its I_C changes by 0.995 mA. Find its common-base current gain α, and common-emitter current gain β.

Solution Common-base current gain is $\alpha = \dfrac{\Delta I_C}{\Delta I_E} = \dfrac{0.995 \times 10^{-3}}{1 \times 10^{-3}} = 0.995$

Common-emitter current gain is $\beta = \dfrac{\alpha}{1 - \alpha} = \dfrac{0.995}{1 - 0.995} = 199$

EXAMPLE 4.17

The current gain of a transistor in CE mode is 49. Calculate its common-base current gain. Find the base current when the emitter current is 3 mA.

Solution Given, $\beta = 49$

We know that $\alpha = \dfrac{\beta}{1+\beta}$

Therefore, the common-base current gain is $\alpha = \dfrac{49}{1+49} = 0.98$

We also know that $\alpha = \dfrac{I_C}{I_E}$

Therefore, $I_C = \alpha I_E = 0.98 \times 3 \times 10^{-3} = 2.94$ mA

EXAMPLE 4.18

Determine I_C, I_E, and α for a transistor circuit having $I_B = 15$ μA and $\beta = 150$.

Solution The collector current, $I_C = \beta I_B = 150 \times 15 \times 10^{-6} = 2.25$ mA

The emitter current,

$$I_E = I_C + I_B$$
$$= 2.25 \times 10^{-3} + 15 \times 10^{-6}$$
$$= 2.265 \text{ mA}$$

Common-base current gain, $\alpha = \dfrac{\beta}{1+\beta} = \dfrac{150}{151} = 0.9934$

EXAMPLE 4.19

Determine the base, collector, and emitter currents and V_{CE} for the CE circuit shown in Fig. 4.18. For $V_{CC} = 10$ V, $V_{BB} = 4$ V, $R_B = 200$ kΩ, $R_C = 2$ kΩ, $V_{BE\,(on)} = 0.7$ V, $\beta = 200$.

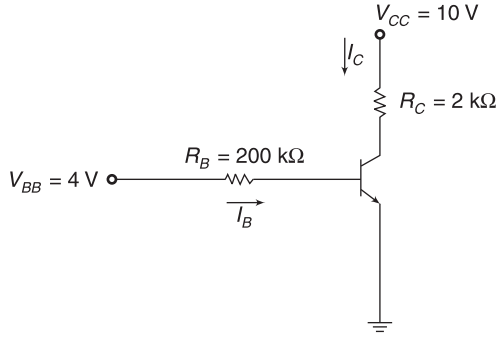


Fig. 4.18

Solution Referring to Fig. 4.18, the base current is

$$I_B = \frac{V_{BB} - V_{BE(on)}}{R_B} = \frac{4 - 0.7}{200 \times 10^3} = 16.5\ \mu A$$

The collector current is $I_C = \beta I_B = 200 \times 16.5 \times 10^{-6} = 3.3$ mA

The emitter current is $I_E = I_C + I_B = 3.3 \times 10^{-3} + 16.5 \times 10^{-6} = 3.3165$ mA

Therefore, $V_{CE} = V_{CC} - I_C R_C = 10 - 3.3 \times 10^{-3} \times 2 \times 10^3 = 3.4$ V

EXAMPLE 4.20

Calculate the values of I_C and I_E for a transistor with $\alpha_{dc} = 0.99$ and $I_{CBO} = 5\ \mu A$. I_B is measured as 20 μA.

Solution Given, $\alpha_{dc} = 0.99$, $I_{CBO} = 5\ \mu A$ and $I_B = 20\ \mu A$

$$I_C = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} + \frac{I_{CBO}}{1 - \alpha_{dc}}$$

$$= \frac{0.99 \times 20 \times 10^{-6}}{1 - 0.99} + \frac{5 \times 10^{-6}}{1 - 0.99} = 2.48\ \text{mA}$$

Therefore, $I_E = I_B + I_C = 20 \times 10^{-6} + 2.48 \times 10^{-3} = 2.5$ mA

EXAMPLE 4.21

The reverse leakage current of the transistor when connected in CB configuration is 0.2 μA and it is 18 μA when the same transistor is connected in CE configuration. Calculate α_{dc} and β_{dc} of the transistor.

Solution The leakage current $I_{CBO} = 0.2\ \mu A$

$I_{CEO} = 18\ \mu A$

Assume that $I_B = 30$ mA

$I_E = I_B + I_C$

$I_C = I_E - I_B = \beta I_B + (1 + \beta)\, I_{CBO}$

We know that $I_{CEO} = \frac{I_{CBO}}{1 - \alpha} = (1 + \beta)\, I_{CBO}$

$$\beta = \frac{I_{CEO}}{I_{CBO}} - 1 = \frac{18}{0.2} - 1 = 89$$

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

$$= 89\ (30 \times 10^{-3}) + (1 + 89)\ (0.2 \times 10^{-6}) = 2.67\ \text{A}$$

$$\alpha_{dc} = 1 - \frac{I_{CBO}}{I_{CEO}} = 1 - \frac{0.2 \times 10^{-6}}{18 \times 10^{-6}} = 0.988$$

$$\beta_{dc} = \frac{I_C - I_{CBO}}{I_B - I_{CEO}} = \frac{2.67 - 0.2 \times 10^{-6}}{30 \times 10^{-3} - 18 \times 10^{-6}} = 89$$

EXAMPLE 4.22

If $\alpha_{dc} = 0.99$ and $I_{CBO} = 50\ \mu A$, find emitter current.

Solution Given $\alpha_{dc} = 0.99$ and $I_{CBO} = 50\ \mu A$,

Assume that $I_B = 1$ mA

$$I_C = \frac{\alpha_{dc} I_B}{1-\alpha_{dc}} + \frac{I_{CBO}}{1-\alpha_{dc}} = \frac{0.99(1\times10^{-3})}{1-0.99} + \frac{50\times10^{-6}}{1-0.99}$$

$$= \frac{0.99\times10^{-3}}{0.01} + \frac{50\times10^{-6}}{0.01} = 99\text{ mA} + 5\text{ mA} = 104\text{ mA}$$

$$I_E = I_C + I_B = 104\text{ mA} + 1\text{ mA} = 105\text{ mA}$$

EXAMPLE 4.23

For the CE amplifier circuit shown in Fig. 4.19, find the percentage change in the collector current if the transistor with $h_{fe} = 50$ is replaced by another transistor with $h_{fe} = 150$. Assume $V_{BE} = 0.6$.

Solution

$$V_B = \frac{R_2}{R_1+R_2}\times V_{CC} = \frac{5\times10^3}{5\times10^3+25\times10^3}\times12 = 2\text{ V}$$

$$V_E = V_B - V_{BE} = 2 - 0.6 = 1.4\text{ V}$$

Here, $I_E = \frac{V_E}{R_E} = \frac{1.4}{100} = 14\text{ mA}$

For $\beta = 50$, $I_B = \frac{I_E}{1+\beta} = \frac{14\times10^{-3}}{51} = 274.5\ \mu A$

Therefore, $I_{C1} = \beta I_B = 50\times274.5\times10^{-6} = 13.725$ mA

For $\beta = 150$, $I_B = \frac{I_E}{1+\beta} = \frac{14\times10^{-3}}{151} = 92.715$ mA

Therefore, $I_{C2} = \beta I_B = 150\times92.715\times10^{-6} = 13.907$ mA

Hence, the percentage change in the collector current is calculated as

$$\frac{I_{C2} - I_{CE}}{I_{C1}}\times100 = \frac{13.907\times10^{-3} - 13.725\times10\times10^{-3}}{13.725\times10^{-3}}\times100 = 1.326\%$$

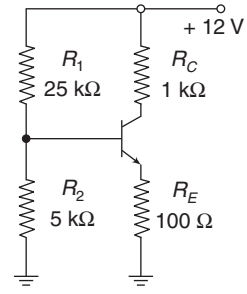


Fig. 4.19

EXAMPLE 4.24

Given an *NPN* transistor for which $\alpha = 0.98$, $I_{CO} = 2\ \mu A$, and $I_{CEO} = 16\ \mu A$. A common-emitter connection is used as shown in Fig. 4.20 with $V_{CC} = 12$ V and $R_C = 4$ kΩ. What is the minimum base current required in order for the transistor to enter into saturation region?

Solution Given, $\alpha = 0.98$, $I_{CO} = 2\ \mu A$, $I_{CEO} = 1.6\ \mu A$, $V_{CC} = 12\ V$ and $R_C = 4\ k\Omega$.

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{12}{4 \times 10^3} = 3\ mA$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta}$$

$$= \frac{3 \times 10^{-3}}{49} = 61.224 \times 10^{-6} = 61.224\ \mu A$$

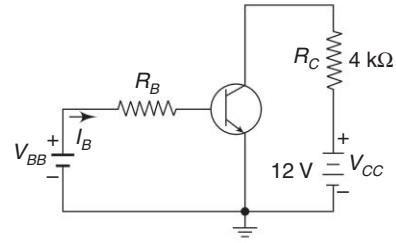


Fig. 4.20

EXAMPLE 4.25

A transistor operating in *CB* configuration has $I_C = 2.98$ mA, $I_E = 3$ mA, and $I_{CO} = 0.01$ mA . What current will flow in the collector circuit of this transistor when connected in *CE* configuration with a base current of 30 μA?

Solution Given $I_C = 2.98$ mA, $I_E = 3$ mA, $I_{CO} = 0.01$ mA and $I_B = 30\ \mu A$.

For CB configuration, $I_C = \alpha I_E + I_{CO}$

Therefore, $$\alpha = \frac{I_C - I_{CO}}{I_E} = \frac{(2.98 - 0.01) \times 10^{-3}}{3 \times 10^{-3}} = 0.99$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$$

For CE configuration, $I_C = \beta I_B + (1 + \beta)\, I_{CO}$

$= 99 \times 30 \times 10^{-6} + (1 + 99) \times 0.01 \times 10^{-3} = 3.97$ mA.

4.7 TRANSISTOR BIASING

The quiescent operating point of a transistor amplifier should be established in the active region of its characteristics. Since the transistor parameters such as β, I_{CO}, and V_{BE} are functions of temperature, the operating point shifts with changes in temperature. The stability of different methods of biasing transistor (BJT, FET, and MOSFET) circuits and compensation techniques for stabilizing the operating point are discussed in this chapter.

4.7.1 Need for Biasing

In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chosen. These voltages and resistances establish a set of dc voltage V_{CEQ} and current I_{CQ} to operate the transistor in the active region. These voltages and currents are called *quiescent values* which determine the *operating point* or *Q*-point for the transistor. The process of giving proper supply voltages and

resistances for obtaining the desired Q-point is called *biasing*. The circuits used for getting the desired and proper operating point are known as *biasing circuits*.

The collector current for a common-emitter amplifier is expressed by

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1 + \beta) I_{CO}$$

Here, the three variables h_{FE}, i.e., β, I_B, and I_{CO} are found to increase with temperature. For every 10°C rise in temperature, I_{CO} doubles itself. When I_{CO} increases, I_C increases significantly. This causes power dissipation to increase and hence, to make I_{CO} increase. This will cause I_C to increase further and the process becomes cumulative which will lead to thermal runaway that will destroy the transistor. In addition, the quiescent operating point can shift due to temperature changes and the transistor can be driven into the region of saturation. The effect of β on the Q-point is shown in Fig. 4.21. One more source of bias instability to be considered is due to the variation of V_{BE} with temperature. V_{BE} is about 0.6 V for a silicon transistor and 0.2 V for a germanium transistor at room temperature. As the temperature increases, $|V_{BE}|$ decreases at the rate of 2.5 mV/°C for both silicon and germanium transistors. The transfer-characteristic curve shifts to the left at the rate of 2.5 mV/°C (at constant I_C) for increasing temperature and, hence, the operating point shifts accordingly. To establish the operating point in the active region, compensation techniques are needed.

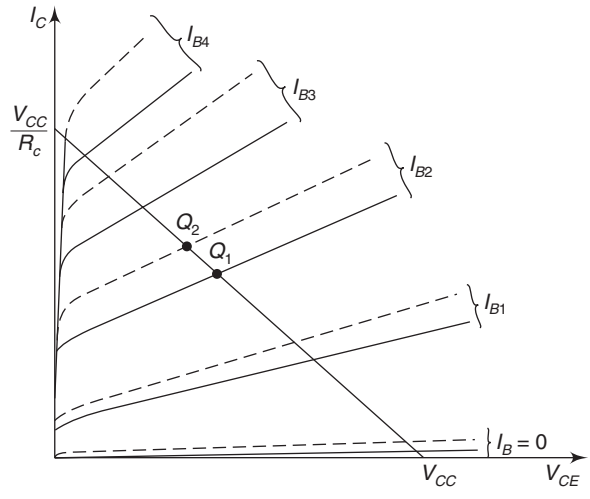


Fig. 4.21 *Effect of β on Q-point*

➤ ***dc Load Line*** Referring to the biasing circuit of Fig. 4.22(a), the values of V_{CC} and R_C are fixed and I_C and V_{CE} are dependent on R_B.

Applying Kirchhoff's voltage law to the collector circuit in Fig. 4.22(a), we get $V_{CC} = I_C R_C + V_{CE}$.

The straight line represented by AB in Fig. 4.22(b) is called the dc *load line.* The coordinates of the end point A are obtained by substituting $V_{CE} = 0$ in the above equation. Then $I_C = \frac{V_{CC}}{R_C}$. Therefore, the coordinates of A are $V_{CE} = 0$ and $I_C = \frac{V_{CC}}{R_C}$.

The coordinates of B are obtained by substituting $I_C = 0$ in the above equation. Then $V_{CE} = V_{CC}$. Therefore, the coordinates of B are $V_{CE} = V_{CC}$ and $I_C = 0$. Thus, the dc load line AB can be drawn if the values of R_C and V_{CC} are known.

As shown in Fig. 4.22(b), the optimum Q-point is located at the midpoint of the dc load line AB between the saturation and cut-off regions, i.e., Q is exactly midway between A and B. In order to get faithful amplification, the Q-point must be well within the active region of the transistor.

Even though the Q-point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q-point shifts nearer to either A or B, the output voltage and current get clipped, thereby output signal is distorted.

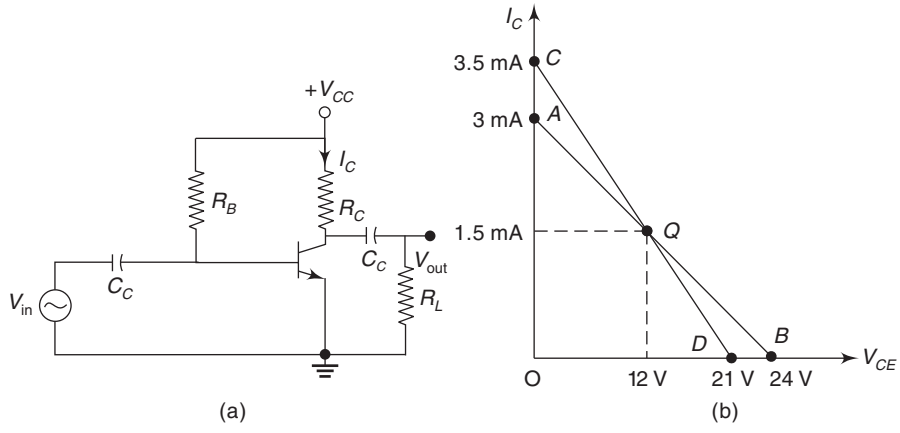


Fig. 4.22 *(a) Biasing circuit (b) CE output characteristics and load line*

In practice, the Q-point tends to shift its position due to any or all of the following three main factors:

(i) Reverse saturation current, I_{CO}, which doubles for every 10 °C increase in temperature.
(ii) Base-emitter voltage, V_{BE}, which decreases by 2.5 mV per °C.
(iii) Transistor current gain, β, i.e., h_{FE} which increases with temperature.

Referring to Fig. 4.22(a), the base current I_B is kept constant since I_B is approximately equal to V_{CC}/R_B. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current I_C for a given I_B. Hence, in the output characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

➤ ***ac Load Line*** After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence, the ac load line should also pass through the operating point Q. The effective ac load resistance, R_{ac}, is the combination of R_C parallel to R_L, i.e., $R_{ac} = R_C \| R_L$. So the slope of the ac load line CQD will be $\left(-\frac{1}{R_{a.c.}}\right)$.

To draw an ac load line, two end points, viz., maximum V_{CE} and maximum I_C when the signal is applied are required.

Maximum $V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$, which locates the point $D\,(OD)$ on the V_{CE} axis.

Maximum $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{a.c.}}$, which locates the point $C\,(OC)$ on the I_C axis.

By joining points C and D, ac load line CD is constructed. As $R_C > R_{ac}$, the dc load line is less steep than the ac load line.

When the signal is zero, we have the exact dc conditions. From Fig. 4.22(b), it is clear that the intersection of dc and ac load lines is the operating point Q.

➤ ***Voltage Swing Limitations*** In a linear amplifier, symmetrical sinusoidal signals at the input gets amplified as sinusoidal signal at the output, without any clipping. The maximum output symmetrical swing provided by the amplifier can be obtained from the ac load line. The output signal will be clipped if it exceeds this limit, resulting in signal distortion.

EXAMPLE 4.26

Determine the maximum voltage swing at the output of common emitter amplifier in which the quiescent point is I_{CQ} = 0.9 mA and V_{CEQ} = 9 V. The ac resistance seen at the output terminal is $R_{ac} = (R_C \parallel R_L)$ = 2 kΩ.

Solution The maximum symmetrical peak to peak ac collector current is

$$\Delta i_C = 2\, I_{CQ} = 2 \times 0.9 \text{ mA} = 1.8 \text{ mA}$$

The maximum symmetrical peak to peak output voltage is

$$\left|\Delta v_{EC}\right| = \left|\Delta i_C\right| R_{ac} = 1.8 \times 10^{-3} \times 2 \times 10^{-3} = 3.6 \text{ V}$$

EXAMPLE 4.27

In the transistor amplifier shown in Fig. 4.22(a), R_C = 8 kΩ, R_L = 24 kΩ and V_{CC} = 24 V. Draw the dc load line and determine the optimum operating point. Also draw the ac load line.

Solution

(a) *dc load line:* Referring to Fig. 4.22(a), we have $V_{CC} = V_{CE} + I_C R_C$.
For drawing the dc load line, the two end points, viz., maximum V_{CE} point (at $I_C = 0$) and maximum I_C point (at $V_{CE} = 0$) are required.

Maximum $V_{CE} = V_{CC} = 24$ V

Maximum $I_C = \dfrac{V_{CC}}{R_C} = \dfrac{24}{8 \times 10^3} = 3$ mA

Therefore, the dc load line AB is drawn with the point B (OB = 24 V) on the V_{CE} axis and the point A (OA = 3 mA) on the I_C axis, as shown in Fig. 4.22(b).

(b) For fixing the optimum operating point Q, mark the middle of the dc load line AB and the corresponding V_{CE} and I_C values can be found.

Here, $V_{CEQ} = \dfrac{V_{CC}}{2} = 12$ V and $I_{CQ} = 1.5$ mA

(c) *ac load line:* To draw an ac load line, two end points, viz., maximum V_{CE} and maximum I_C when the signal is applied, are required.

The ac load, $R_{ac} = R_C \parallel R_L = \dfrac{8 \times 24}{8 + 24} = 6$ kΩ

Maximum $V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$

$= 12 + 1.5 \times 10^{-3} \times 6 \times 10^3 = 21$ V

This locates the point D (OD = 21 V) on the V_{CE} axis.

$$\text{Maximum collector current} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 1.5 \times 10^{-3} + \frac{12}{6 \times 10^3} = 3.5 \text{ mA}$$

This locates the point $C (OC = 3.5 \text{ mA})$ on the I_C axis. By joining points C and D, the ac load line CD is constructed.

EXAMPLE 4.28

For the transistor amplifier shown in Fig. 4.23(a), $V_{CC} = 12$ V, $R_1 = 8$ kΩ, $R_2 = 4$ kΩ, $R_C = 1$ kΩ, $R_E = 1$ kΩ and $R_L = 1.5$ kΩ. Assume $V_{BE} = 0.7$ V. (a) Draw the dc load line, (b) determine the operating point, and (c) draw the ac load line.

Solution

(a) *dc load line:* Referring to Fig. 4.23(a), we have $V_{CC} = V_{CE} + I_C (R_C + R_E)$.
To draw the dc load line, we need two end points, viz., maximum V_{CE} point (at $I_C = 0$) and maximum I_C point (at $V_{CE} = 0$).

Maximum $V_{CE} = V_{CC} = 12$ V, which locates the point $B (OB = 12 \text{ V})$ of the dc load line.

$$\text{Maximum} \qquad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{12}{(1+1) \times 10^3} = 6 \text{ mA}$$

This locates the point A $(OA = 6 \text{ mA})$ of the dc load line. Figure 4.23(b) shows the dc load line AB, with (12 V, 6 mA).

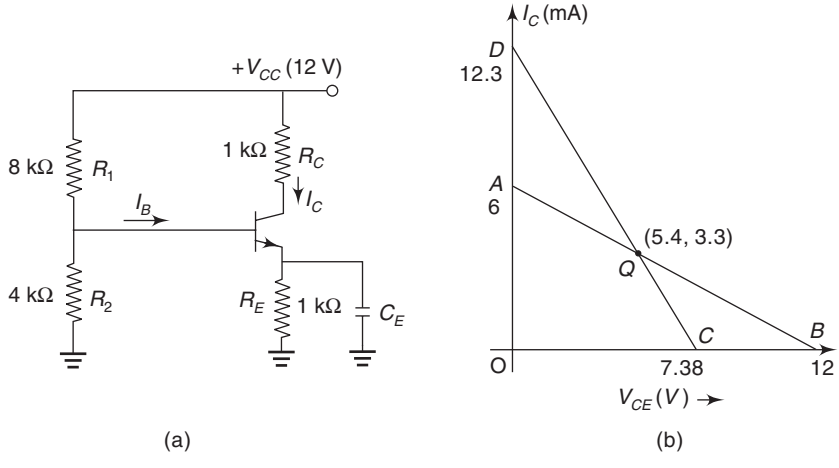


Fig. 4.23

(b) *Operating point Q*

$$\text{The voltage across} \quad R_2 \text{ is } V_2 = \frac{R}{R_1 + R_2} V_{CC}$$

$$\text{Therefore,} \qquad V_2 = \frac{4 \times 10^3}{12 \times 10^3} \times 12 = 4 \text{ V}$$

$$V_2 = V_{BE} + I_E R_E$$

Therefore, $$I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{4 - 0.7}{1 \times 10^3} = 3.3 \text{ mA}$$

$$I_C \approx I_E = 3.3 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 12 - 3.3 \times 10^{-3} \times 2 \times 10^3 = 5.4 \text{ V}$$

Therefore, the operating point Q is at 5.4 V and 3.3 mA, which is shown on the dc load line.

(c) *ac load line:* To draw the ac load line, we need two end points, viz., maximum V_{CE} and maximum I_C when signal is applied.

ac load, $$R_{ac} = R_C \parallel R_L = \frac{1 \times 1.5\text{k}\Omega}{2.5} = 0.6 \text{ k}\Omega$$

Therefore, maximum $$V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$$

$$= 5.4 + 3.3 \times 10^{-3} \times 0.6 \times 10^3 = 7.38 \text{ V}$$

This locates the point C ($OC = 7.38$ V) on the V_{CE} axis.

Maximum $$I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$$

$$= 3.3 \times 10^{-3} + \frac{5.4}{0.6 \times 10^3} = 12.3 \text{ mA}$$

This locates the point D ($OD = 12.3$ mA) on the I_C axis. By joining points C and D, the ac load line CD is constructed.

EXAMPLE 4.29

Design the circuit shown in Fig. 4.24, given Q-point values are to be $I_{CQ} = 1$ mA and $V_{CEQ} = 6$ V. Assume that $V_{CC} = 10$ V, $\beta = 100$ and $V_{BE\,(on)} = 0.7$ V.

Solution The collector resistance is

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{10 - 6}{1 \times 10^{-3}} = 4 \text{ k}\Omega$$

The base current is

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1 \times 10^{-3}}{100} = 10 \text{ μA}$$

The base resistance is

$$R_B = \frac{V_{CC} - V_{BE(on)}}{I_{BQ}} = \frac{10 - 0.7}{10 \times 10^{-6}} = 0.93 \text{ M}\Omega$$

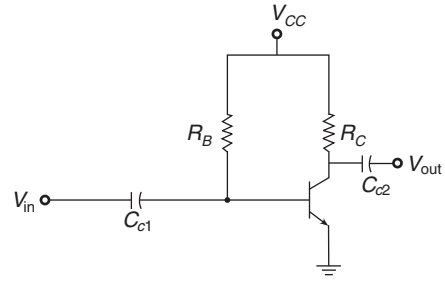


Fig. 4.24

EXAMPLE 4.30

Determine the characteristics of a circuit shown in Fig. 4.25. Assume that $\beta = 100$ and $V_{BE\ (on)} = 0.7$ V.

Solution Referring to Fig. 4.25, Kirchhoff's voltage law equation is

$$V_{BB} = I_B R_B + V_{BE\ (on)} + I_E R_E$$

We know that

$$I_E = I_B + I_C = I_B + \beta I_B = (1 + \beta) I_B$$

The base current $I_B = \dfrac{V_{BB} - V_{BE(on)}}{R_B + (1 + \beta) R_E}$

$$= \frac{5 - 0.7}{20 \times 10^3 + 101 \times 600} = 53.34\ \mu\text{A}$$

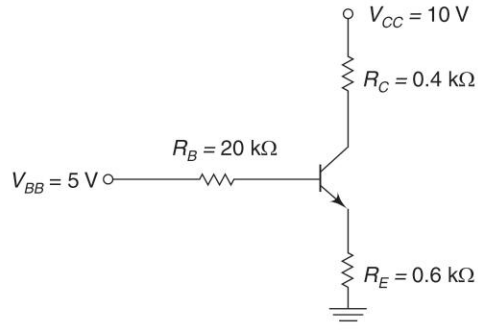


Fig. 4.25

Therefore, $I_C = \beta I_B = 100 \times 53.34 \times 10^{-6}$

$$= 5.334\ \text{mA}$$

$$I_E = I_C + I_B = 5.334 \times 10^{-3} + 53.34 \times 10^{-6}$$

$$= 5.38734\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 10 - 5.334 \times 10^{-3} \times 400 - 5.38734 \times 10^{-3} \times 600$$

$$= 4.634\ \text{V}$$

The Q point is at $V_{CEQ} = 4.634$ V and $I_{CQ} = 5.334$ mA

4.8 THERMAL RUNAWAY

The collector current for the CE circuit of Fig. 4.22 is given by $I_C = \beta I_B + (1 + \beta)\ I_{CO}$. The three variables in the equation, β, I_B, and I_{CO} increase with rise in temperature. In particular, the reverse saturation current or leakage current I_{CO} changes greatly with temperature. Specifically, it doubles for every 10 °C rise in temperature. The collector current I_C causes the collector-base junction temperature to rise which, in turn, increase I_{CO}, as a result I_C will increase still further, which will further raise the temperature at the collector-base junction. This process will become cumulative leading to *thermal runaway*. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is normally made larger in size than the emitter in order to help dissipate the heat developed at the collector junction.

However, if the circuit is designed such that the base current I_B is made to decrease automatically with rise in temperature then the decrease in βI_B will compensate for the increase in $(1 + \beta) I_{CO}$, keeping I_C almost constant.

In power transistors, the heat developed at the collector junction may be removed by the use of a heat sink, which is a metal sheet fitted to the collector and whose surface radiates heat quickly.

4.9 STABILITY FACTOR

The extent to which the collector current I_C is stabilized with varying I_{CO} is measured by a stability factor S. It is defined as the rate of change of collector current I_C with respect to the collector-base leakage current I_{CO}, keeping both the current I_B and the current gain β constant.

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \beta \text{ and } I_B \text{ constant} \tag{4.27}$$

The collector current for a CE amplifier is given by

$$I_C = \beta I_B + (\beta + 1) I_{CO} \tag{4.28}$$

Differentiating the above equation with respect to I_C, we get

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

Therefore,
$$\left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta + 1)}{S}$$

$$S = \frac{1 + \beta}{1 - \beta\left(\frac{dI_B}{dI_C}\right)} \tag{4.29}$$

From this equation, it is clear that this factor S should be as small as possible to have better thermal stability.

➤ ***Stability Factors S′ and S″*** The stability factor S' is defined as the rate of change of I_C with V_{BE}, keeping I_{CO} and β constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

The stability factor S'' is defined as the rate of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta}$$

4.10 THERMAL STABILIZATION (TO FIXED BIAS, COLLECTOR TO BASE BIAS, SELF BIAS)

The stability factors for some commonly used biasing circuits are discussed here.

4.10.1 Fixed Bias or Base Resistor Method

A common-emitter amplifier using a fixed-bias circuit is shown in Fig. 4.26. The dc analysis of the circuit yields the following equation.

$$V_{CC} = I_B R_B + V_{BE} \tag{4.30}$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

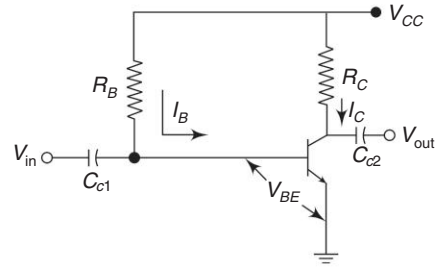


Fig. 4.26 *Fixed bias circuit*

Since this equation is independent of the current I_C, $dI_B/dI_C = 0$ and the stability factor given in Eq. (4.29) reduces to

$$S = 1 + \beta$$

Since β is a large quantity, this is a very poor bias stable circuit. Therefore, in practice, this circuit is not used for biasing the base.

The advantages of this method are (i) simplicity, (ii) small number of components required, and (iii) if the supply voltage is very large as compared to V_{BE} of the transistor, then the base current becomes largely independent of the voltage V_{BE}.

EXAMPLE 4.31

In the fixed-bias compensation method shown in Fig. 4.27, a silicon transistor with $\beta = 100$ is used. $V_{CC} = 6$ V, $R_C = 3$ kΩ, $R_B = 530$ kΩ. Draw the dc load line and determine the operating point. What is the stability factor?

Solution (a) *dc load line*

$$V_{CE} = V_{CC} - I_C R_C$$

When $I_C = 0$, $V_{CE} = V_{CC} = 6$ V

When $V_{CE} = 0$, $I_C = \dfrac{V_{CC}}{R_C} = \dfrac{6}{3 \times 10^3} = 2$ mA

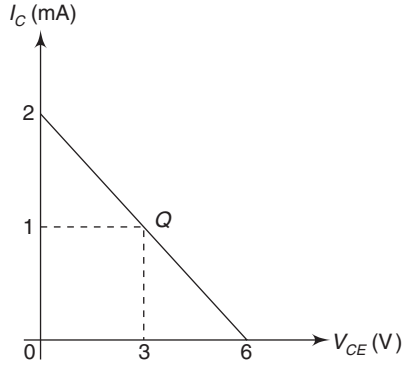


Fig. 4.27

(b) *Operating point Q*

For a silicon transistor, $V_{BE} = 0.7$ V

$$V_{CC} = I_B R_B + V_{BE}$$

Therefore, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{6 - 0.7}{530 \times 10^3} = 10$ mA

Therefore, $I_C = \beta I_B = 100 \times 10 \times 10^{-6} = 1$ mA

$$V_{CE} = V_{CC} - I_C R_C = 6 - 1 \times 10^{-3} \times 3 \times 10^3 = 3 \text{ V}$$

Therefore operating point is $V_{CEQ} = 3$ V and $I_{CQ} = 1$ mA.

(c) *Stability factor* $S = 1 + \beta = 1 + 100 = 101$

EXAMPLE 4.32

Find the collector current and collector-to-emitter voltage for the given circuit as shown in Fig. 4.28.

Solution For a silicon transistor, $V_{BE} = 0.7$ V

Base current $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{9 - 0.7}{300 \times 10^3} = 27.67$ μA

Collector current $I_C = \beta I_B = 50 \times 27.67 \times 10^{-6} = 1.38$ mA

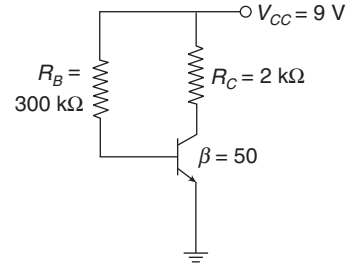


Fig. 4.28

Collector-to-emitter voltage

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 9 - 1.38 \times 10^{-3} \times 2 \times 10^3 = 6.24 \text{ V}$$

EXAMPLE 4.33

A germanium transistor having $\beta = 100$ and $V_{BE} = 0.2$ V is used in a fixed-bias amplifier circuit where $V_{CC} = 16$ V, $R_C = 5$ kΩ and $R_B = 790$ kΩ. Determine its operating point.

Solution For a germanium transistor, $V_{BE} = 0.2$ V

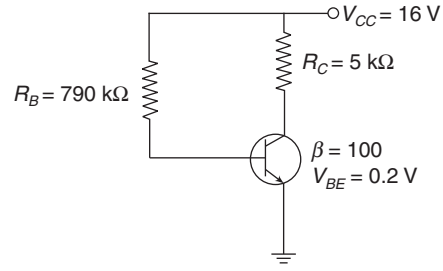


Fig. 4.29

Applying KVL to the base circuit, we have

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{16 - 0.2}{790 \times 10^3} = 20 \text{ μA}$$
$$I_C = \beta I_B = 100 \times 20 \text{ μA} = 2 \text{ mA}$$

Applying KVL to the collector circuit, we have

$$V_{CC} - I_C R_C - V_{CE} = 0$$
$$V_{CE} = V_{CC} - I_C R_C = 16 - 2 \times 10^{-3} \times 5 \times 10^3 = 6 \text{ V}$$

Hence, the operating point is $I_C = 2$ mA and $V_{CE} = 6$ V.

EXAMPLE 4.34

The circuit as shown in Fig. 4.30 has fixed bias using an *NPN* transistor. Determine the value of base current, collector current, and collector-to-emitter voltage.

Solution Applying KVL to the base circuit, we have

$$V_{CC} - I_B R_B - V_{BE} = 0$$

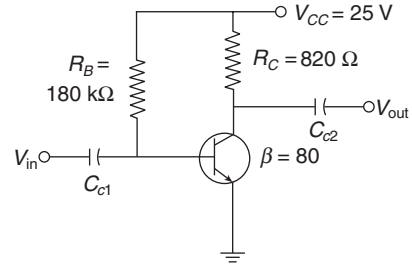


Fig. 4.30

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{25 - 0.7}{180 \times 10^3} = 135 \text{ μA}$$
$$I_C = \beta I_B = 80 \times 135 \times 10^{-6} = 10.8 \text{ mA}$$

Applying KVL to the collector circuit, we have

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Therefore,
$$V_{CE} = V_{CC} - I_C R_C$$
$$= 25 - 10.8 \times 10^{-3} \times 820 = 16.144 \text{ V}$$

EXAMPLE 4.35

For a fixed-bias configuration shown in Fig. 4.26, determine I_C, R_C, R_B, and V_{CE} using the following specifications: $V_{CC} = 12$ V, $V_C = 6$ V, $\beta = 80$, and $I_B = 40$ μA.

Solution Assume $V_{BE} = 0.7$ V for a silicon transistor.

$$I_C = \beta I_B = 80 \times 40\ \mu\text{A} = 3.2\ \text{mA}$$

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{12 - 6}{3.2 \times 10^{-3}} = 1.875\ \text{k}\Omega$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.7}{40 \times 10^{-6}} = 282.5\ \text{k}\Omega$$

Since the emitter is grounded, $V_E = 0$.

$$V_{CE} = V_C = 6\ \text{V}$$

4.10.2 Emitter-Feedback Bias

The emitter-feedback bias network shown in Fig. 4.31 contains an emitter resistor for improving the stability level over that of the fixed-bias configuration. The analysis will be performed by first examining the base-emitter loop and then using the results to investigate the collector-emitter loop.

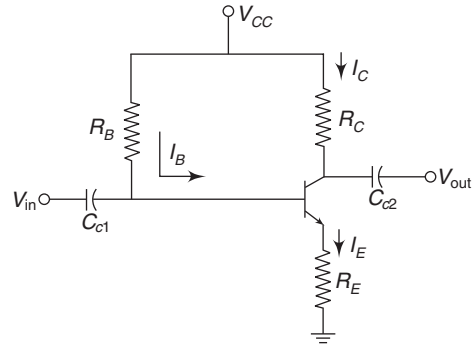


Fig. 4.31 *Emitter-feedback bias circuit*

➤ ***Base-emitter Loop*** Applying Kirchhoff's voltage law for the base-feedback emitter loop, we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \qquad (4.31)$$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{CC} - I_B (R_B + R_E) - V_{BE} - I_C R_E = 0$$

$$V_{CC} - V_{BE} = I_B (R_B + R_E) + I_C R_E$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_E + R_B} - \left(\frac{R_E}{R_E + R_B}\right) I_C \qquad (4.32)$$

Here, V_{BE} is independent of I_C.

Hence,
$$\frac{dI_B}{dI_C} = -\left(\frac{R_E}{R_E + R_B}\right) \qquad (4.33)$$

Substituting Eq. (4.32) in Eq. (4.29), we get the stability factor as

$$S = \frac{1 + \beta}{1 + \beta \dfrac{R_E}{R_E + R_B}} \qquad (4.34)$$

Since $1 + \dfrac{\beta R_E}{(R_E + R_B)} > 1$, $S < (1 + \beta)$. Note that the value of the stability factor S is always lower in emitter-feedback bias circuit than that of the fixed-bias circuit. Hence, it is clear that a better thermal stability can be achieved in an emitter-feedback bias circuit than the fixed-bias circuit.

➤ ***Collector-Emitter Loop*** Applying Kirchhoff's voltage law for the collector-emitter loop, we get

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E = I_C$, we have

$$V_{CE} - V_{CC} + I_C (R_C + R_E) = 0$$

and
$$V_{CE} = V_{CC} - I_C (R_C + R_E) \tag{4.35}$$

V_E is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E \tag{4.36}$$

The voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and
$$V_C = V_{CE} + V_E \tag{4.37}$$

or
$$V_C = V_{CC} - I_C R_C \tag{4.38}$$

The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_E \tag{4.39}$$

or
$$V_B = V_{BE} + V_E \tag{4.40}$$

EXAMPLE 4.36

For the emitter-feedback bias circuit, $V_{CC} = 10$ V, $R_C = 1.5$ kΩ, $R_B = 270$ kΩ, and $R_E = 1$ kΩ. Assuming $\beta = 50$, determine (a) stability factor, S (b) I_B, (c) I_C, (d) V_{CE}, (e) V_C, (f) V_E, (g) V_B, and (h) V_{BC}.

Solution

(a) The stability factor is

$$S = \frac{1+\beta}{1+\dfrac{\beta R_E}{(R_E + R_B)}} = \frac{1+50}{1+\dfrac{(50\times 1\times 10^3)}{1\times 10^3 + 270\times 10^3}}$$

$$= \frac{51}{1+0.185} = \frac{51}{1.185} = 43.04$$

(b)
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E} = \frac{10 - 0.7}{27\times 10^3 + (51)(1\times 10^3)} = \frac{9.3}{321} = 28.97\ \mu\text{A}$$

(c)
$$I_C = \beta I_B = (50)\ (28.97 \times 10^{-6}) = 1.45\ \text{mA}$$

(d)
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$
$$= 10 - 1.45 \times 10^{-3}\ (1.5 \times 10^3 + 1 \times 10^3) = 10 - 3.62 = 6.38\ \text{V}$$

(e)
$$V_C = V_{CC} - I_C R_C = 10 - 1.45 \times 10^{-3}\ (1.5 \times 10^3) = 7.825\ \text{V}$$

(f)
$$V_E = V_C - V_{CE} = 7.825 - 6.38 = 1.445\ \text{V}$$

or
$$V_E = I_E R_E = I_C R_E = 1.45 \times 10^{-3} \times 1 \times 10^3 = 1.45\ \text{V}$$

(g) $V_B = V_{BE} + V_E = 0.7 + 1.45 = 2.15$ V

(h) $V_{BC} = V_B - V_C = 2.15 - 7.825 = |5.675|$ V (reverse bias as required)

EXAMPLE 4.37

Calculate dc bias voltage and currents in the circuit in Fig. 4.32. Neglect V_{BE} of the transistor.

Solution Given, $V_{CC} = 20$ V; $R_B = 400$ kΩ, $\beta = 100$, $R_E = 1$ kΩ; $R_C = 2$ kΩ

$$I_B R_B + V_{BE} + I_E R_E = V_{CC}$$

$$\frac{I_C}{\beta} R_B + 0 + (I_C + I_B) R_E = 20$$

$$I_C \left[\frac{R_B}{\beta} + R_E + \frac{R_E}{\beta} \right] = 20$$

Therefore,
$$I_C = \frac{20}{\left[\frac{400 \times 10^3}{100} + 1 \times 10^3 + 10 \right]} = 4 \text{ mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{4 \times 10^{-3}}{100} = 0.4 \, \mu\text{A}$$

$$V_B = V_{BE} + I_E R_E$$

$$= 0 + 4 \times 10^{-3} \times 1 \times 10^3 = 4 \text{ V, since } I_C \approx I_E$$

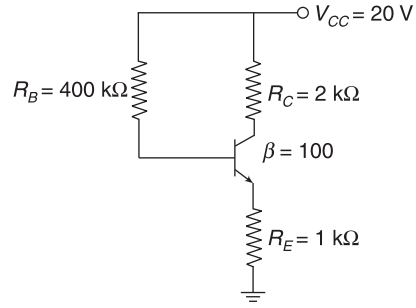


Fig. 4.32

4.10.3 Collector-to-Base Bias or Collector-Feedback Bias

A common-emitter amplifier using collector-to-base bias circuit is shown in Fig. 4.33. This circuit is the simplest way to provide some degree of stabilization to the amplifier operating point.

If the collector current I_C tends to increase due to either increase in temperature or the transistor has been replaced by the one with a higher β, the voltage drop across R_C increases, thereby reducing the value or V_{CE}. Therefore, I_B decreases which, in turn, compensates the increase in I_C. Thus, greater stability is obtained.

The loop equation for this circuit is

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE} \quad (4.41)$$

i.e.,
$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \quad (4.42)$$

Therefore,
$$\frac{dI_B}{dI_C} = \frac{-R_C}{R_C + R_B} \quad (4.43)$$

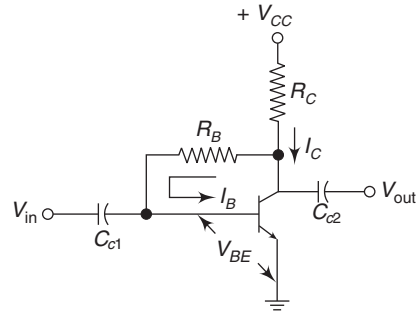


Fig. 4.33 *Collector-to-base bias circuit*

Substituting Eq. (4.43) into Eq. (4.29), we get

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)} \tag{4.44}$$

As can be seen, this value of the stability factor is smaller than the value obtained by fixed-bias circuit. Also, S can be made small and the stability can be improved by making R_B small or R_C large.

If R_C is very small, then $S = (\beta + 1)$, i.e., stability is very poor. Hence, the value of R_C must be quite large for good stabilization. Thus, collector-to-base bias arrangement is not satisfactory for the amplifier circuits like transformer-coupled amplifier where the dc load resistance in the collector circuit is very small. For such amplifiers, emitter bias or self-bias will be the most satisfactory transistor biasing for stabilization.

EXAMPLE 4.38

In the biasing with feedback resistor method, a silicon transistor with feedback resistor is used. The operating point is at 7 V, 1 mA and $V_{CC} = 12$ V. Assume $\beta = 100$. Determine (a) the value of R_B, (b) stability factor, and (c) what will be the new operating point if $\beta = 50$ with all other circuit values are same?

Solution Refer to Fig. 4.26. We know that for a silicon transistor, $V_{BE} = 0.7$ V.

(a) *To determine* R_B

The operating point is at $V_{CE} = 7$ V and $I_C = 1$ mA

Here,
$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12-7}{1\times10^{-3}} = 5\ \text{k}\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{1\times10^{-3}}{100} = 10\ \mu\text{A}$$

Using the relation,

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B} = \frac{12 - 0.7 - 1\times10^{-3}\times5\times10^{3}}{10\times10^{-6}} = 630\ \text{k}\Omega$$

(b) *Stability factor*
$$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C+R_B}\right]} = \frac{1+100}{1+100\left[\frac{5\times10^{3}}{(5+630)\times10^{3}}\right]} = 56.5$$

(c) *To determine new operating point when* $\beta = 50$

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE}$$

$$= I_B(\beta R_C + R_B) + V_{BE}$$

i.e.,
$$12 = I_B(50\times5\times10^{3} + 630\times10^{3}) + 0.7$$

$$I_B = \frac{11.3}{880\times10^{3}} = 12.84\ \mu\text{A}$$

Therefore, $I_C = \beta I_B = 50 \times 12.84 \times 10^{-6} = 0.642$ mA

$$V_{CE} = V_{CC} - I_C R_C = 12 - 0.642 \times 10^{-3} \times 5 \times 10^3 = 8.79 \text{ V}$$

Therefore, the coordinates of the new operating point are $V_{CEQ} = 8.79$ V and $I_{CQ} = 0.642$ mA.

EXAMPLE 4.39

In an *NPN* transistor, if $\beta = 50$ is used in common-emitter circuit with $V_{CC} = 10$ V and $R_C = 2$ kΩ. The bias is obtained by connecting 100 kΩ resistor from collector to base. Find the quiescent point and stability factor.

Solution Given, $V_{CC} = 10$ V, $R_C = 2$ kΩ,

$\beta = 50$ and collector to base resistor $R_B = 100$ kΩ

To determine the quiescent point: We know that for the collector-to-base bias-transistor circuit,

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE}$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta \cdot R_C}$$

$$= \frac{10 - 0.7}{100 \times 10^3 + 50 \times 2 \times 10^{-3}} = 46.5 \text{ μA}$$

Hence, $I_C = \beta \cdot I_B = 50 \times 46.5 \times 10^{-6} = 2.325$ mA

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.325 \times 10^{-3} \times 2 \times 10^3 = 5.35 \text{ V}$$

Therefore, the coordinates of the new operating point are

$$V_{CEQ} = 5.35 \text{ V and } I_{CQ} = 2.325 \text{ mA}$$

To find the stability factor S

$$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C + R_B}\right]} = \frac{1+50}{1+50\left[\frac{2\times10^3}{2\times10^3 + 100\times10^3}\right]} = 25.75$$

EXAMPLE 4.40

In the collector-to-base *CE* amplifier circuit of Fig. 4.26 having $V_{CC} = 12$ V, $R_C = 250$ kΩ, $I_B = 0.25$ mA, $\beta = 100$, and $V_{CEQ} = 8$ V, calculate R_B and stability factor.

Solution
$$R_B = \frac{V_{CEQ}}{I_B} = \frac{8}{0.25 \times 10^{-3}} = 32 \text{ kΩ}$$

Stability factor,
$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)} = \frac{101}{1+100\left(\frac{250}{32+250}\right)} = 56.9$$

EXAMPLE 4.41

Calculate the quiescent current and voltage of a collector-to-base bias arrangement using the following data: $V_{CC} = 10$ V, $R_B = 100$ kΩ, $R_C = 2$ kΩ, $\beta = 50$, and also specify a value of R_B so that $V_{CE} = 7$ V.

Solution

(a) Applying KVL to the base circuit, we have

$$V_{CC} - I_B(1 + \beta) R_C - I_B R_B - V_{BE} = 0$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_C} = \frac{10 - 0.7}{100 \times 10^3 + (1 + 50) \times 2 \times 10^3} = 46\ \mu A$$

$$I_C = \beta I_B = 50 \times 46\ \mu A = 2.3\ mA$$

Applying KVL to the collector circuit, as shown in figure 4.34, we have

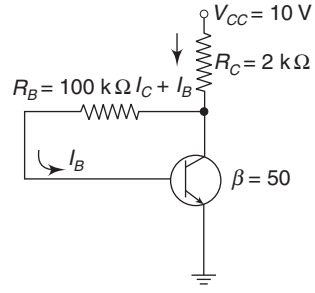


Fig. 4.34

$$V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$$

Therefore,
$$V_{CE} = V_{CC} - (I_B + I_C) R_C$$
$$= 10 - (46 \times 10^{-6} + 2.3 \times 10^{-3}) \times 2 \times 10^3$$
$$= 5.308\ V$$

Quiescent current, $I_{CQ} = 2.3$ mA and

Quiescent voltage, $V_{CEQ} = 5.308$ V

(b) Given, $V_{CE} = 7$ V

$$(I_B + I_C) R_C = V_{CC} - V_{CE}$$
$$(1 + \beta) I_B R_C = V_{CC} - V_{CE}$$
$$I_B = \frac{V_{CC} - V_{CE}}{(1 + \beta) R_C} = \frac{10 - 7}{(1 + 50) \times 2 \times 10^3} = 29.41\ \mu A$$

We have,

$$V_{CC} = I_B R_B + V_{BE}$$
$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{7 - 0.7}{29.41 \times 10^{-6}} = 214.2\ k\Omega$$

4.10.4 Collector-Emitter Feedback Bias

Figure 4.35 shows the collector-emitter feedback-bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here, collector feedback is provided by connecting a resistance R_B from the collector to the base and emitter feedback is provided by connecting an emitter resistance R_E from the emitter to ground. Both the feedbacks are used to control the collector current I_C and the base current I_B in the opposite direction to increase the stability as compared to the previous biasing circuits.

Applying Kirchhoff's voltage law to the current, we get

$$(I_B + I_C) R_E + V_{BE} + I_B R_B + (I_B + I_C) R_C - V_{CC} = 0$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_E + R_C + R_B} - \left(\frac{R_E + R_C}{R_E + R_C + R_B}\right) I_C$$

Since V_{BE} is independent of I_C,
$$\frac{dI_B}{dI_C} = -\left(\frac{R_E + R_C}{R_E + R_C + R_B}\right)$$

Substituting the above equation in Eq. (4.29), we get
$$S = \frac{1 + \beta}{1 + \dfrac{\beta(R_E + R_C)}{R_E + R_C + R_B}} \qquad (4.45)$$

From this, it is clear that the stability of the collector-emitter feedback bias circuit is always better than that of the collector-feedback and emitter-feedback circuits.

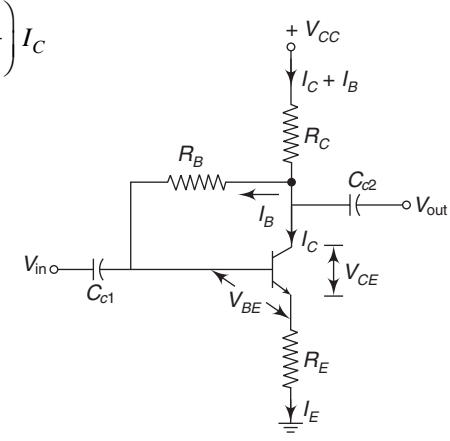


Fig. 4.35 *Collector-emitter feedback circuit*

4.10.5 Voltage-Divider Bias, Self-Bias, or Emitter Bias

A simple circuit used to establish a stable operating point is the self-biasing configuration. The self-bias, also called emitter bias, or emitter resistor, and potential divider circuit, that can be used for low collector resistance, is shown in Fig. 4.36. The current in the emitter resistor R_E causes a voltage drop which is in the direction to reverse bias the emitter junction. For the transistor to remain in the active region, the base-emitter junction has to be forward biased. The required base bias is obtained from the power supply through the potential divider network of the resistances R_1 and R_2.

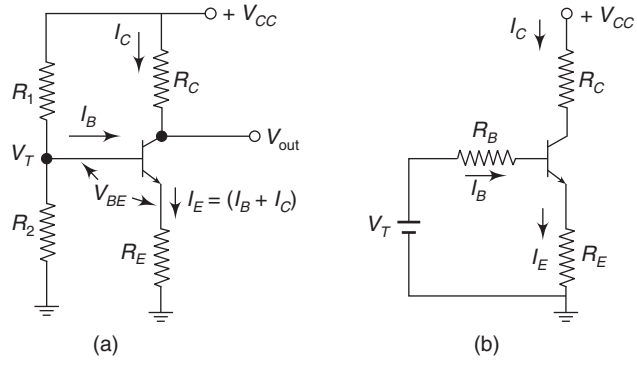


Fig. 4.36 *(a) Self-bias circuit (b) Thevenin's equivalent circuit*

➤ ***Use of Self-bias Circuit as a Constant Current Circuit*** If I_C tends to increase, say, due to increase in I_{CO} with temperature, the current in R_E increases. Hence, the voltage drop across R_E increases thereby decreasing the base current. As a result, I_C is maintained almost constant.

4.10.6 Stabilization Factors

➤ ***To Determine Stability Factor, S*** Applying Thevenin's theorem to the circuit of Fig. 4.36, for finding the base current, we have,

$$V_T = \frac{R_2 V_{CC}}{R_1 + R_2} \text{ and } R_B = \frac{R_1 R_2}{R_1 + R_2}$$

The loop equation around the base circuit can be written as

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating this equation with respect to I_C, we get

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B}$$

Substituting this equation in Eq. (4.35), we get

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_E}{R_E + R_B} \right)}$$

Therefore,

$$S = (1 + \beta) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} \quad (4.46)$$

As can be seen, the value of S is equal to one if the ratio R_B/R_E is very small as compared to 1. As this ratio becomes comparable to unity, and beyond towards infinity, the value of the stability factor goes on increasing till $S = 1 + \beta$.

This improvement in the stability up to a factor equal to 1 is achieved at the cost of power dissipation. To improve the stability, the equivalent resistance R_B must be decreased, forcing more current in the voltage divider network of R_1 and R_2.

Often, to prevent the loss of gain due to the negative feedback, R_E is shunted by a capacitor C_E. The capacitive reactance X_{CE} must be equal to about one-tenth of the value of the resistance R_E at the lowest operating frequency.

➤ ***To Determine the Stability Factor S′*** The stability factor S' is defined as the rate of change of I_C with V_{BE}, keeping I_{CO} and β constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}}$$

From Fig. 4.36 (b),

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$= I_B [R_B + R_E] + I_C R_E + V_{BE} \text{ since } [I_E = I_B + I_C] \quad (4.47)$$

We have

$$I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta} \tag{4.48}$$

Substituting Eq. (4.47) in Eq. (4.48), we get

$$V_T = \frac{I_C}{\beta}(R_B + R_E) + V_{BE} + I_C R_E + \frac{I_{CO}}{\beta}(1+\beta)\{R_B + R_E\} \tag{4.49}$$

Differentiating the above equation w.r.t. V_{BE}, we get

$$0 = \frac{dI_C}{dV_{BE}}\left(\frac{R_B + R_E}{\beta}\right) + 1 + R_E \frac{dI_C}{dV_{BE}} + 0$$

$$-1 = \frac{dI_C}{dV_{BE}}\left[R_E + \frac{R_B + R_E}{\beta}\right]$$

$$-1 = \frac{dI_C}{dV_{BE}}\left[\frac{R_B + (1+\beta) R_E}{\beta}\right]$$

Therefore,

$$S' = \frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B + (1+\beta) R_E} \tag{4.50}$$

➤ ***To Determine the Stability of S″*** The stability factor S'' is defined as the rate of change of I_C w.r.t. β, keeping I_{CO} and V_{BE} constant.

Rearranging Eq. (4.49), we have

$$I_C = \frac{\beta(V_T - V_{BE})}{R_B + (1+\beta) R_E} + \frac{\beta\left(\frac{1+\beta}{\beta}\right) I_{CO}(R_B + R_E)}{R_B + (1+\beta) R_E} \tag{4.51}$$

Since $\beta >> 1$, the numerator of the second term can be written as

$$(R_B + R_E)\left(\frac{1+\beta}{\beta}\right) I_{CO} = (R_B + R_E)\, I_{CO} \tag{4.52}$$

Substituting Eq. (4.52) in Eq. (4.51), we have

$$I_C = \frac{\beta(V_T - V_{BE})}{R_E + (1+\beta) R_E} + \frac{\beta(R_B + R_E) I_{CO}}{R_B + (1+\beta) R_E}$$

Therefore,

$$I_C = \frac{\beta[V_T - V_{BE} + (R_B + R_E) I_{CO}]}{R_B + (1+\beta) R_E}$$

Let,

$$V' = (R_B + R_E) I_{CO}.$$

Therefore,

$$I_C = \frac{\beta[V_T - V_{BE} + V']}{R_B + (1+\beta) R_E} \tag{4.53}$$

Differentiating Eq. (4.53) w.r.t. β and simplifying, we obtain

$$S'' = \frac{dI_C}{d\beta} = \frac{I_C}{\beta\left[1+\beta\left(\frac{R_E}{R_E+R_B}\right)\right]} = \frac{SI_C}{\beta(1+\beta)} \tag{4.54}$$

EXAMPLE 4.42

In a CE germanium transistor-amplifier circuit, the bias is provided by self-bias, i.e., emitter resistor and potential-divider arrangement (refer to Fig. 4.27). The various parameters are V_{CC} = 16 V, R_C = 3 kΩ, R_E = 2 kΩ, R_1 = 56 kΩ, R_2 = 20 kΩ, and α = 0.985. Determine (a) the coordinates of the operating point, and (b) the stability factor S.

Solution For a germanium transistor, V_{BE} = 0.3 V. As α = 0.985,

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1-0.985} = 66$$

(a) *To find the coordinates of the operating point*

Referring to Fig. 4.36, we have

Thevenin's voltage, $$V_T = \frac{R_2}{R_1+R_2}V_{CC} = \frac{20\times10^3}{76\times10^3}\times16 = 4.21 \text{ V}$$

Thevenin's resistance, $$R_B = \frac{R_1R_2}{R_1+R_2} = \frac{20\times10^3\times56\times10^3}{76\times10^3} = 14.737 \text{ kΩ}$$

The loop equation around the base circuit is

$$V_T = I_BR_B + V_{BE} + (I_B + I_C)R_E$$

$$= \frac{I_C}{\beta}R_B + V_{BE} + \left(\frac{I_C}{\beta} + I_C\right)R_E$$

$$4.21 = \frac{I_C}{66}\times14.737\times10^3 + 0.3 + I_C\left(\frac{1}{66}+1\right)\times2\times10^3$$

$$3.91 = I_C\,[0.223 + 2.03]\times10^3$$

Therefore, $$I_C = \frac{3.91}{2.253\times10^3} = 1.73 \text{ mA}$$

Since I_B is very small, $I_C \approx I_E$ = 1.73 mA

Therefore, $$V_{CE} = V_{CC} - I_CR_C - I_ER_E$$

$$= V_{CC} - I_C\,[R_C + R_E]$$

$$= 16 - 1.73\times10^{-3}\times5\times10^3 = 7.35 \text{ V}$$

Therefore, the coordinates of the operating point are I_C = 1.73 mA and V_{CE} = 7.35 V.

(b) *To find the stability factor S,*

$$S = (1+\beta)\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}} = (1+66)\frac{1+\frac{14.737}{2}}{1+66+\frac{14.737}{2}} = 67\times\frac{8.3685}{74.3685} = 7.537$$

EXAMPLE 4.43

Consider the self-bias circuit where V_{CC} = 22.5 Volt, R_C = 5.6 kΩ, R_2 = 10 kΩ, and R_1 = 90 kΩ, h_{fe} = 55, V_{BE} = 0.6 V. The transistor operates in active region. Determine (a) operating point, and (b) stability factor.

Solution For the given circuit, V_{BE} = 0.6 V, h_{fe} = 55

(a) *To determine the operating point*

Thevenin's voltage, $$V_T = \frac{R_2}{R_1+R_2}V_{CC} = \frac{10\times10^3}{100\times10^3}\times 22.5 = 2.25 \text{ V}$$

Thevenin's resistance, $$R_B = \frac{R_1R_2}{R_1+R_2} = \frac{10\times10^3\times90\times10^3}{100\times10^3} = 9 \text{ k}\Omega$$

The loop equation around the base circuit is

$$V_B = I_BR_B + V_{BE} + (I_B + I_C)R_E$$

$$= \frac{I_C}{h_{fe}}R_B + V_{BE} + \left(\frac{I_C}{h_{fe}} + I_C\right)R_E$$

$$2.25 = \frac{I_C}{55}\times 9\times10^3 + 0.6 + \left(\frac{1}{55}+1\right)I_C\times1\times10^3$$

$$2.25 = I_C\times0.16\times10^3 + 0.6 + 1.01\times I_C\times10^3$$

$$2.25 = I_C\times1.17\times10^3 + 0.6$$

Therefore, $$I_C = \frac{2.25-0.6}{1.17\times10^3} = 1.41 \text{ mA}$$

Since I_B is very small, $I_C \approx I_E$ = 1.41 mA

Therefore, $$V_{CE} = V_{CC} - I_CR_C - I_ER_E = V_{CC} - I_C(R_C + R_E)$$

$$= 22.5 - 1.41\times10^{-3}\times6.6\times10^3 = 13.19 \text{ V}$$

Operating point coordinates are V_{CE} = 13.19 V and I_C = 1.41 mA

(b) *To find the stability factor, S*

$$S = (1+\beta)\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}} = (1+55)\frac{1+\frac{9\times10^3}{1\times10^3}}{1+55+\frac{9\times10^3}{1\times10^3}} = \frac{56\times10}{65} = \frac{560}{65} = 8.6$$

EXAMPLE 4.44

Figure 4.37 shows the dc bias circuit of a common-emitter transistor amplifier. Find the percentage change in the collector current, if the transistor with $h_{fe} = 50$ is replaced by another transistor with $h_{fe} = 150$. It is given that the base-emitter drop $V_{BE} = 0.6$ V.

Solution

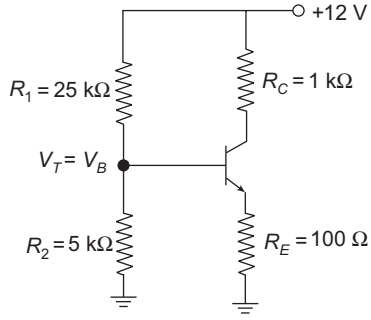


Fig. 4.37

(a) For the given circuit, $V_{BE} = 0.6$ V, $h_{fe} = 50$

Thevenin's voltage, $$V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{30 \times 10^3} \times 12 = 2 \text{ V}$$

Thevenin's resistance, $$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{25 \times 10^3 \times 5 \times 10^3}{30 \times 10^3} = 4.16 \text{ k}\Omega$$

The loop equation around the base circuit is

$$V_T = V_B = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{h_{fe}} R_B + V_{BE} + \left(\frac{I_C}{h_{fe}} + I_C \right) R_E$$

$$2 = \frac{I_C}{50} \times 4.6 \times 10^3 + 0.6 + \left(\frac{1}{50} + 1 \right) \times I_C \times 0.1 \times 10^3$$

$$2 - 0.6 = I_C \times (0.08 + 0.102) \times 10^3$$

Therefore, $$I_C = \frac{14}{0.182 \times 10^3} = 7.69 \text{ mA}$$

(b) For the given circuit, $V_{BE} = 0.6$ V, $h_{fe} = 150$

The loop equation around the base circuit is

$$V_B = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{h_{fe}} R_B + V_{BE} + \left(\frac{I_C}{h_{fe}} + I_C \right) R_E$$

$$2 = \frac{I_C}{50} \times 4.6 \times 10^3 + 0.6 + \left(\frac{1}{50} + 1 \right) \times I_C \times 0.1 \times 10^3$$

$$2 - 0.6 = I_C \times (0.028 + 0.1) \times 10^3$$

Therefore, $$I_C = \frac{1.4}{0.128 \times 10^3} = 10.93 \text{ mA}$$

Change in collector current $$= \frac{10.93 - 7.69}{7.69} = 0.42, \text{ i.e., } 42\%$$

There is 42% change in I_C when h_{fe} changes from 50 to 150.

EXAMPLE 4.45

If the various parameters of a *CE* amplifier which uses the self-bias method are V_{CC} = 12 V, R_1 = 10 kΩ, R_2 = 5 kΩ, R_C = 1 kΩ, R_E = 2 kΩ, and β = 100, find (a) the coordinates of the operating point, and (b) the stability factor, assuming the transistor to be silicon.

Solution

(a) *To find the coordinates of the operating point*

Refer Fig. 4.36.

Thevenin's voltage, $$V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{15 \times 10^3} \times 12 = 4 \text{ V}$$

Thevenin's resistance, $$R_B = \frac{R_1 R_2}{(R_1 + R_2)} = \frac{5 \times 10^3 \times 10 \times 10^3}{15 \times 10^3} = 3.33 \text{ k}\Omega$$

The loop equation around the basic circuit is

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{\beta} R_B + V_{BE} + \left(\frac{I_C}{\beta} + I_C \right) R_E$$

$$4 = \frac{I_C}{100} \times 3.33 \times 10^3 + 0.7 + I_C \left(\frac{1}{100} + 1 \right) \times 2 \times 10^3$$

$$3.3 = (33.3 + 2020)\, I_C$$

$$I_C = \frac{3.3}{2053.3} = 1.61 \text{ mA}$$

Since I_B is very small, $I_C \approx I_E = 1.61$ mA

Therefore, $$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= V_{CC} - I_C [R_C + R_E]$$

$$= 12 - 1.61 \times 10^{-3} \times 3 \times 10^3 = 7.17 \text{ V}$$

Therefore, the coordinates of the operating point are I_C = 1.61 mA and V_{CE} = 7.17 V.

(b) *To find the stability factor S*

$$S = (1 + \beta) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} = (1 + 100) \frac{1 + \frac{3.33 \times 10^3}{2 \times 10^3}}{1 + 100 + \frac{3.33 \times 10^3}{2 \times 10^3}} = 2.6$$

EXAMPLE 4.46

Determine the quiescent current and collector-to-emitter voltage for a germanium transistor with β = 50 in self-biasing arrangement. Draw the circuit with a given component value with V_{CC} = 20 V, R_C = 2 kΩ, R_E = 100 Ω, R_1 = 100 kΩ, and R_2 = 5 kΩ. Also find the stability factor.

Solution For a germanium transistor, $V_{BE} = 0.3$ V and $\beta = 50$

To find the coordinates of the operating point

Thevenin's voltage, $$V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{105 \times 10^3} \times 20 = 0.95 \text{ V}$$

Thevenin's resistance, $$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 10^3 \times 5 \times 10^3}{105 \times 10^3} = 4.76 \text{ k}\Omega$$

The loop equation around the base circuit is

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{\beta} R_B + V_{BE} + \left(\frac{I_C}{\beta} + I_C \right) R_E$$

$$0.95 = \frac{I_C}{50} \times 4.76 \times 10^3 + 0.3 + I_C \times \frac{51}{50} \times 100$$

$$0.65 = 197.2\, I_C$$

Therefore, $$I_C = \frac{0.65}{197.2} = 3.296 \text{ mA}$$

Since I_B is very small, $I_C \approx I_E = 3.296$ mA

Therefore, $$V_{CE} = V_{CC} - I_C R_C - I_E R_E = V_{CC} - I_C (R_C + R_E)$$

$$= 20 - 3.296 \times 10^{-3} \times 2.01 \times 10^3 = 13.375 \text{ V}$$

Therefore, the coordinates of the operating point are $I_C = 3.296$ mA and $V_{CE} = 13.375$ V.

To find the stability factor S

$$S = (1 + \beta) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} = (1 + 50) \frac{1 + \frac{4.76 \times 10^3}{100}}{1 + 50 + \frac{4.76 \times 10^3}{100}} = 25.18$$

EXAMPLE 4.47

A germanium transistor is used in a self-biasing circuit configuration as shown below with $V_{CC} = 16$ V, $R_C = 1.5$ kΩ and $\beta = 50$. The operating point desired is $V_{CE} = 8$ V and $I_C = 4$ mA. If a stability factor $S = 10$ is desired, calculate the values of R_1 and R_2 and R_E of the circuit (Fig. 4.38).

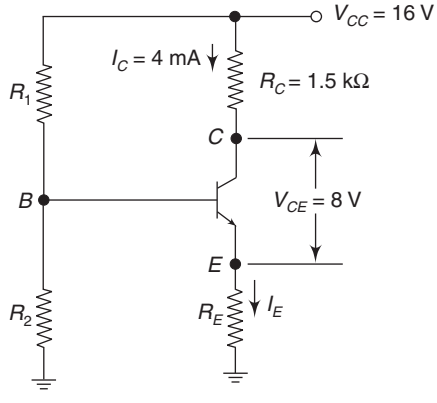


Fig. 4.38

Solution

(a) To determine R_E

We know that, $$V_{CC} = V_{CE} + I_C (R_C + R_E)$$

$$16 = 8 + 4 \times 10^{-3} (1.5 \times 10^3 + R_E)$$

Therefore, $$R_E = 500\ \Omega$$

(b) To determine R_{TH}

Given, $S = 10$

Stability factor $$S = \frac{1+\beta}{1+\beta\dfrac{R_E}{R_{TH}+R_E}} = \frac{1+50}{1+50\left(\dfrac{500}{R_{TH}+500}\right)}$$

Upon solving, we get $R_{TH} = 5.58\ \text{k}\Omega$

(c) To determine R_2

$$R_2 = 0.1\ \beta R_E = 27.98\ \text{k}\Omega$$

(d) To determine R_1

We know that, $$R_{TH} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$5.58 \times 10^3 = \frac{R_1 \times 27.98 \times 10^3}{R_1 + 27.98 \times 10^3}$$

Therefore, $R_1 = 6.97\ \text{k}\Omega$

EXAMPLE 4.48

A *CE* transistor amplifier with the voltage-divider bias circuit of Fig. 4.36 is designed to establish the quiescent point at $V_{CE} = 12$ V, $I_C = 2$ mA and stability factor ≤ 5.1. If $V_{CC} = 24$ V, $V_{BE} = 0.7$ V, $\beta = 50$, and $R_C = 4.7\ \text{k}\Omega$, determine the values of resistors R_E, R_1, and R_2.

Solution

(a) *To determine R_E*

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$
$$= V_{CC} - I_C\,[R_C + R_E], \text{ since } I_C \approx I_E$$
$$12 = 24 - 2 \times 10^{-3}\,[4.7 \times 10^3 + R_E]$$

Therefore, $R_E = 1.3\ \text{k}\Omega$

(b) *To determine R_1 and R_2*

Stability factor, $$S = \frac{1+\beta}{1+\beta\left(\dfrac{R_E}{R_E+R_B}\right)}, \text{ where } R_B = \frac{R_1 R_2}{(R_1 + R_2)}$$

$$5.1 = \frac{51}{1+50\left(\dfrac{1.3\times10^3}{1.3\times10^3 + R_B}\right)}$$

i.e., $$1+50\left(\frac{1.3\times10^3}{1.3\times10^3 + R_B}\right) = \frac{51}{5.1} = 10$$

Therefore, $$\left(\frac{50 \times 1.3 \times 10^3}{1.3 \times 10^3 + R_B}\right) = 9$$

$$1.3 \times 10^3 + R_B = \frac{50 \times 1.3 \times 10^3}{9} = 7.2 \text{ k}\Omega$$

$$R_B = 5.9 \text{ k}\Omega$$

Also, we know that for a good voltage divider, the value of the resistance $R_2 = 0.1\ \beta R_E$

Therefore, $$R_2 = 0.1 \times 50 \times 1.3 \times 10^3 = 6.5 \text{ k}\Omega$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$5.9 \times 10^3 = \frac{R_1 \times 6.5 \times 10^3}{R_1 + 6.5 \times 10^3}$$

Simplifying, we get $R_1 = 64 \text{ k}\Omega$

EXAMPLE 4.49

In the circuit shown in Fig. 4.39, if $I_C = 2$ mA and $V_{CE} = 3$ V, calculate R_1 and R_3.

Solution Given, $\beta = 100$, $I_C = 2$ mA, $V_{CE} = 3$ V, $V_{BE} = 0.6$ V, $R_2 = 10$ kΩ and $R_4 = 500\ \Omega$

We know that $$\beta = \frac{I_C}{I_B}$$

Hence, $$I_B = \frac{I_C}{\beta} = \frac{2 \times 10^{-3}}{100} = 20\ \mu\text{A}$$

$$V_{CC} = I_C R_3 + V_{CE} + I_E R_4$$

$$I_E = I_C + I_B = 20 \times 10^{-6} + 2 \times 10^{-3} = 2.02 \text{ mA}$$

Substituting the values, we get

$$15 = 2 \times 10^{-3} \times R_3 + 3 + 2.02 \times 10^{-3} \times 500$$

Therefore, $$R_3 = 5.495 \text{ k}\Omega$$

$$V_B = V_{BE} + I_E R_4 = 0.6 + 2.02 \times 10^{-3} \times 500 = 1.61$$

From the circuit, $$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$1.61 = \frac{10 \times 10^3 \times 15}{R_1 + 10 \times 10^3}$$

Therefore, $$R_1 = 83.17 \text{ k}\Omega$$

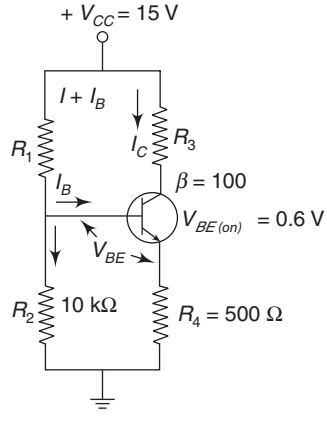


Fig. 4.39

EXAMPLE 4.50

In an *NPN* transistor, $\beta = 50$ is used in common-emitter circuit with $V_{CC} = 10$ V and $R_C = 2$ kΩ. The bias is obtained by connecting the 100 kΩ resistor from collector to base. Find the quiescent point and stability factor.

Solution Given, $V_{CC} = 10$ V, $R_C = 2$ kΩ, $\beta = 50$ and collector to base resistor, $R_B = 100$ kΩ

To determine the quiescent point

We know that the collector-to-base bias-transistor circuit

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE}$$

Therefore,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta \cdot R_C} = \frac{10 - 0.7}{100 \times 10^3 + 50 \times 2 \times 10^{+3}} = 46.5\ \mu A$$

Hence,
$$I_C = \beta I_B = 50 \times 46.5 \times 10^{-6} = 2.325\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.325 \times 10^{-3} \times 2 \times 10^3 = 5.35\ \text{V}$$

Therefore, the coordinates of the new operating point are

$$V_{CEQ} = 5.35\ \text{V and } I_{CQ} = 2.325\ \text{mA}$$

To find the stability factor S

$$S = \frac{1 + \beta}{1 + \beta\left[\frac{R_C}{R_C + R_B}\right]} = \frac{1 + 50}{1 + 50\left[\frac{2 \times 10^3}{2 \times 10^3 + 100 \times 10^3}\right]} = 25.75$$

EXAMPLE 4.51

Design a voltage-divider bias network using a supply of 24 V, $\beta = 110$ and $I_{CQ} = 4$ mA, $V_{CEQ} = 8$ V. Choose $V_E = V_{CC}/8$.

Solution Given: $I_{CQ} = 4$ mA, $V_{CEQ} = 8$ V, $V_E = V_{CC}/8$, $V_{CC} = 24$ V, $\beta = 110$

(a) *To determine I_B, I_E and V_E*

$$I_B = \frac{I_{CQ}}{\beta} = \frac{4 \times 10^3}{110} = 36.36\ \mu A$$

$$I_E = I_B + I_C = 36.36 \times 10^{-6} + 4 \times 10^{-3} = 4.03636\ \text{mA}$$

$$V_E = \frac{V_{CC}}{8} = \frac{24}{8} = 3\ \text{V}$$

(b) *To determine R_E and R_2*

$$R_E = \frac{V_E}{I_E} = \frac{3}{4.03636 \times 10^{-3}} = 743.244\ \Omega$$

Applying KVL to the collector circuit,

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

Therefore,
$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{24 - 8 - 3}{4 \times 10^{-3}} = 3.25 \text{ k}\Omega$$

(c) *To determine R_1 and R_2*

$$V_B = V_E + V_{BE} = 3 + 0.7 = 3.7 \text{ V}$$

Referring to Fig. 4.36, consider the current through R_1 to be $I + I_B$ and that through R_2 to be I. Resistors R_1 and R_2 form the potential divider. For proper operation of the potential divider, the current I should be atleast ten times the I_B, i.e., $I \geq 10\ I_B$. Therefore,

$$I = 10\ I_B = 10 \times 36.36 \times 10^{-6} = 363.6\ \mu\text{A}$$

$$R_2 = \frac{V_B}{I} = \frac{3.7}{363.6 \times 10^{-6}} = 10.176\ \text{k}\Omega$$

$$R_1 = \frac{V_{CC} - V_B}{I + I_B} = \frac{24 - 3.7}{(363.6 + 36.36) \times 10^{-6}} = 50.755\ \text{k}\Omega$$

EXAMPLE 4.52

Determine the stability factor for the circuit shown in Fig. 4.40.

Solution

$$I_2 = \frac{V_{BE} + (I_C + I_B) R_E}{R_2}$$

$$I_1 = I_B + I_2$$

Therefore,
$$I_1 = I_B + \frac{V_{BE} + (I_C + I_B) R_E}{R_2}$$

$$= \frac{I_B R_2 + V_{BE} + (I_C + I_B) R_E}{R_2}$$

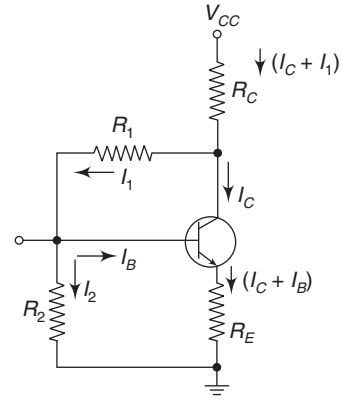


Fig. 4.40

Applying KVL to the collector base-emitter loop, we have

$$V_{CC} = (I_C + I_1) R_C - I_1 R_1 - V_{BE} - (I_C + I_B) R_E$$

$$= (I_C + I_1) R_C + I_1 R_1 + V_{BE} + (I_C + I_B) R_E$$

$$= I_C R_C + I_1 R_C + I_1 R_1 + V_{BE} + I_C R_E + I_B R_E$$

$$= I_C (R_C + R_E) + I_1 (R_C + R_1) + V_{BE} + I_B R_E$$

Substituting the value of I_1 from the equation determined above, we get

$$V_{CC} = I_C (R_C + R_E) + \frac{I_B R_2 + V_{BE} + (I_C + I_B) R_E}{R_2} (R_C + R_1) + V_{BE} + I_B R_E$$

$$= I_C \left[R_C + R_E + \frac{(R_C + R_1)}{R_2} \right] + I_B \left[R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] + \left[1 + \frac{(R_C + R_1)}{R_2} \right] V_{BE}$$

We know that $I_C = \beta I_B + (1 + \beta)\, I_{CO}$

Therefore, $I_B = \dfrac{I_C - (1 + \beta)\, I_{CO}}{\beta}$

Substituting the value of I_B, we get

$$V_{CC} = I_C \left[R_C + R_E + \frac{R_E (R_C + R_1)}{R_2} \right] + \frac{I_C - (1+\beta) I_{CO}}{\beta} \times \left[R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] + \left[1 + \frac{(R_C + R_1)}{R_2} \right] V_{BE}$$

We know that $S = \dfrac{dI_C}{dI_{CO}}$. Hence, differentiating the above equation and assuming V_{BE} constant, we get

$$0 = \frac{\partial I_C}{\partial I_{CO}} \left[R_C + R_E + \frac{R_E (R_C + R_1)}{R_2} \right] + \frac{\partial I_C}{\partial I_{CO}} \times \frac{1}{\beta} \left[R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] - \frac{(1+\beta)}{\beta} \left[R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right]$$

$$= \frac{\partial I_C}{\partial I_{CO}} \left[\frac{R_2 R_C + R_2 R_E + R_E R_C + R_E R_1}{R_2} \right] + \frac{\partial I_C}{\partial I_{CO}} \times \frac{1}{\beta} \times \left[\frac{R_2 R_E + R_E R_C + R_E R_1 + R_2 R_C + R_1 R_2}{R_2} \right] - \frac{1+\beta}{\beta} \left[\frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{R_2} \right]$$

$$= \frac{\partial I_C}{\partial I_{CO}} \left[\frac{R_2 R_C + R_E (R_1 + R_2 + R_C)}{R_2} \right] + \frac{\partial I_C}{\partial I_{CO}} \times \frac{1}{\beta} \times \left[\frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{R_2} \right] - \frac{1+\beta}{\beta} \left[\frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{R_2} \right]$$

$$= \frac{\partial I_C}{\partial I_{CO}} \left[\frac{R_2 R_C + R_E (R_1 + R_2 + R_C)}{R_2} \right] + \left[\frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{\beta R_2} \right]$$

$$\frac{\partial I_C}{\partial I_{CO}} = \frac{\dfrac{1+\beta}{\beta} [R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)]}{R_2 R_C + R_E (R_1 + R_2 + R_C) + \dfrac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{\beta}}$$

$$= \frac{\dfrac{1+\beta}{\beta} [R_2 (R_C + R_1) + (R_E (R_1 + R_2 + R_C)]}{\dfrac{\beta (R_2 R_C + R_E (R_1 + R_2 + R_C)) + R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{\beta}}$$

Stability factor, $$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)[R_2(R_C + R_1) + R_E(R_1 + R_2 + R_C)]}{R_1R_2 + (\beta+1)[R_2R_C + R_E(R_1 + R_2 + R_C)]}$$

4.10.7 Common Base Stability

In a common-base amplifier circuit, the equation for the collector current I_C is given by

$$I_C = \alpha I_E + I_{CO}$$

$$S \approx \frac{dI_C}{dI_{CO}} = 1$$

Since this is highly stable, the common-base amplifier circuit is not in need of bias stabilization.

4.10.8 Advantage of Self-bias (Voltage-Divider Bias) Over Other Types of Biasing

In the fixed-bias method discussed in Section 4.10.1, the stability factor is given by

$$S = 1 + \beta$$

Since β is normally a large quantity, this circuit provides very poor stability. Therefore, the fixed biasing technique is not preferred for biasing the base.

In the collector-to-base bias method, when R_C is very small, $S \approx 1 + \beta$, which is equal to that of fixed bias. Hence, the collector-to-base bias method is also not preferable. In the self-bias method discussed in Section 4.10.5, when $\frac{R_B}{R_E}$ is very small, $S \approx 1$, which provides good stability. Hence, the self-bias method is the best method over other types of 'biasing'.

4.11 COMPENSATION AGAINST VARIATION IN BASE EMITTER VOLTAGE AND COLLECTOR CURRENT

➤ *Compensation for V_{BE}*

▪ **Diode Compensation in Emitter Circuit** Figure 4.41 shows the Thevenin's equivalent circuit of the voltage-divider bias with bias-compensation technique.

Here, V_{DD} is separately used to keep the diode in the forward-biased condition. If the diode is of same material and type as the transistor, then the voltage across the diode V_D will have the same temperature coefficient (2.5 m V/°C) as the base-to-emitter voltage V_{BE}. If V_{BE} changes by a small amount with change in temperature, then V_D also changes by the same amount and, therefore, the changes cancel each other.

We know that,

$$V_{BE} = V_T - \frac{[R_B + (1+\beta)R_E]}{\beta} I_C + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

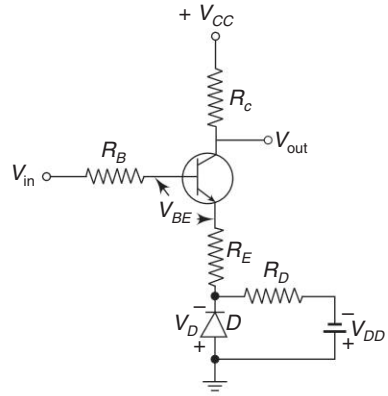


Fig. 4.41 *Stabilization by voltage-divider bias compensation*

Rearranging, we have

$$\frac{[R_B + (1+\beta)R_E}{\beta I_C} I_C = V_T - V_{BE} + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

Hence,
$$I_C = \frac{\beta[V_T - V_{BE}] + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E}$$

From KVL equation of the base circuit of Fig. 4.41, the above equation can be written as

$$I_C = \frac{\beta[V_{\text{in}} - V_{BE} - V_D] + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E}$$

Since variation of V_D is same as V_{BE}, the collector current I_C will be insensitive to variation in V_{BE}.

▪ **Diode Compensation in Voltage-Divider Circuit** Figure 4.42 shows the diode compensation technique used in voltage-divider bias. Here, the diode is connected in series with the resistance R_2 and it is in forward-biased condition. Therefore,

$$I_E = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E}$$

and
$$I_C \approx I_E$$

When V_{BE} changes with temperature, I_C also changes. To cancel the change in I_C, a diode is used at the base terminal to compensate the change in V_{BE} as shown in Fig. 4.42. The voltage at the base, V_B, becomes

$$V_B = V_{R2} + V_D$$

Substituting in the above equation for I_C, we get

$$I_C \approx \frac{V_{R2} + V_D - V_{BE}}{R_E}$$

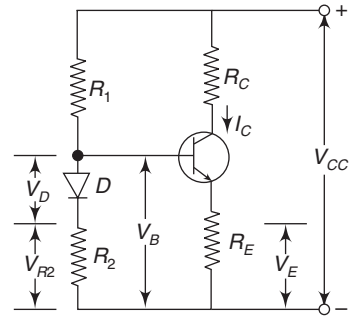


Fig. 4.42 *Diode compensation in voltage-divider bias circuit*

If the diode is of the same material and type as the transistor, then the voltage across the diode will have the same temperature coefficient (2.5 mV/°C) as the base-to-emitter voltage V_{BE}. When V_{BE} changes by a small amount with change in temperature, V_D also changes by the same amount and thus, they cancel each other and the collector current remains constant. Therefore,

$$I_C = \frac{V_{R2}}{R_E}$$

The change in V_{BE} due to temperature is compensated by a change in the diode voltage that keeps I_C stable at the Q point.

➤ ***Diode Compensation Against Variation in I_{CO}*** Figure 4.43 shows a transistor amplifier with a diode D connected across the base-emitter junction for compensation of change in the collector saturation current I_{CO}. The diode is of the same material as the transistor and it is reverse biased by the base-emitter junction voltage V_{BE}, allowing the diode reverse saturation current I_o to flow through the diode D. The base current $I_B = I - I_o$.

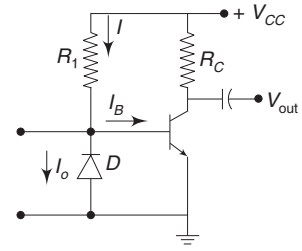


Fig. 4.43 *Diode-bias compensation*

As long as temperature is constant, the diode D operates as a resistor. As the temperature increases, I_{CO} of the transistor increases. Hence, to compensate for this, the base current I_B should be decreased.

The increase in temperature will also cause the leakage current I_o through D to increase and thereby decreasing the base current I_B. This is the required action to keep I_C constant.

This method of bias compensation does not need a change in I_C to effect the change in I_B, as both I_o and I_{CO} can track almost equally according to the change in temperature.

4.12 HYBRID MODEL OF TRANSISTOR

Based on the definition of hybrid parameters, the mathematical model for two-port networks known as h-parameter model can be developed. The following equations can be written

$$v_1 = h_i i_1 + h_r v_2 \tag{4.55}$$

$$i_2 = h_f i_1 + h_o v_2 \tag{4.56}$$

The proposed model shown in Fig. 4.44 should satisfy these two equations and it can be readily verified by writing Kirchhoff's voltage law equation in the input loop and Kirchhoff's current law equation for the output node. It is to be noted that the input circuit has a dependent voltage generator and the output circuit contains a dependent current generator.

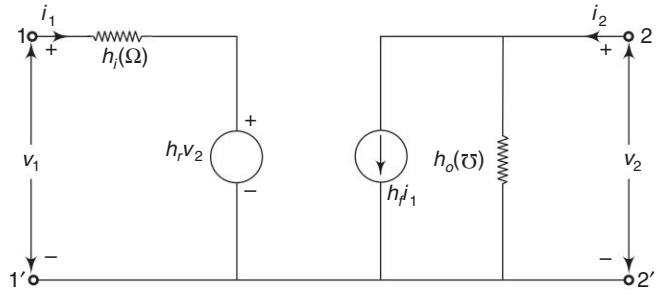


Fig. 4.44 *Hybrid model for a two-port network*

Transistor Hybrid Model

On extending the hybrid model for a two-port network to a transistor, it is assumed that the signal excursion about the Q-point is small so that the transistor parameters may be considered constant over the signal excursion.

Use of h-parameters to describe a transistor has the following advantages:

(i) h-parameters are real numbers up to radio frequencies.
(ii) They are easy to measure.
(iii) They can be determined from the transistor static characteristics curves.
(iv) They are convenient to use in circuit analysis and design.
(v) They are easily convertible from one configuration to other.
(vi) They are readily supplied by manufacturers.

In order to derive a hybrid model for a transistor, consider the CE circuit of Fig. 4.45. The variables are i_b, i_c, v_b (= v_{be}) and v_c (= v_{ce}). i_b and v_c are considered independent variables.

Then, $$v_b = f_1(i_b, v_c) \quad (4.57)$$

$$i_c = f_2(i_b, v_c) \quad (4.58)$$

Making a Taylor's series expansion around the quiescent point I_b, V_c and neglecting higher order terms, the following two equations are obtained:

$$\Delta v_b = \left(\frac{\partial f_1}{\partial i_b}\right)_{V_c} \Delta i_b + \left(\frac{\partial f_1}{\partial v_c}\right)_{I_b} \Delta v_c \quad (4.59)$$

$$\Delta i_c = \left(\frac{\partial f_2}{\partial i_b}\right)_{V_c} \Delta i_b + \left(\frac{\partial f_2}{\partial v_c}\right)_{I_b} \Delta v_c \quad (4.60)$$

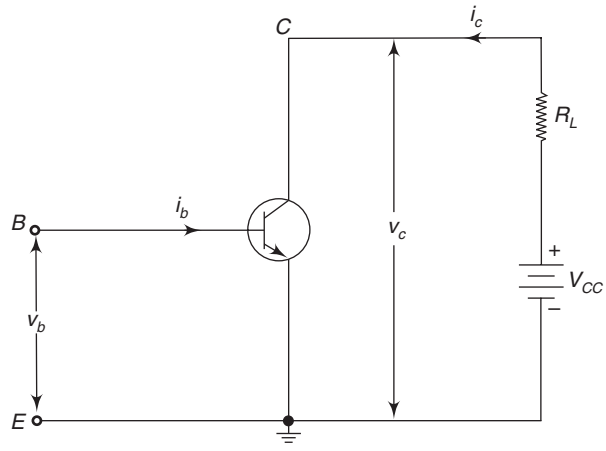


Fig. 4.45 *CE transistor circuit*

The partial derivatives are taken keeping the collector voltage or base current constant as indicated by the subscript attached to the derivative. Δv_b, Δv_c, Δi_b, and Δi_c represent the small-signal (incremental) base and collector voltages and currents. They are represented by symbols v_b, v_c, i_b, and i_c, respectively. Hence, Eqs (4.59) and (4.60) may be written as

$$v_b = h_{ie} i_b + h_{re} v_c$$

$$i_c = h_{fe} i_b + h_{oe} v_c$$

where

$$h_{ie} = \left(\frac{\partial f_1}{\partial i_b}\right)_{v_c} = \left(\frac{\partial v_b}{\partial i_b}\right)_{v_c} \approx \left(\frac{\Delta v_b}{\partial i_b}\right)_{v_c} = \left(\frac{v_b}{i_b}\right)_{v_c} \quad (4.61)$$

$$h_{re} = \left(\frac{\partial f_1}{\partial v_c}\right)_{i_b} = \left(\frac{\partial v_b}{\partial v_c}\right)_{i_b} \approx \left(\frac{\Delta v_b}{\partial v_c}\right)_{i_b} = \left(\frac{v_b}{v_c}\right)_{i_b} \quad (4.62)$$

$$h_{fe} = \left(\frac{\partial f_2}{\partial i_b}\right)_{v_c} = \left(\frac{\partial i_c}{\partial i_b}\right)_{v_c} \approx \left(\frac{\Delta i_c}{\partial i_b}\right)_{v_c} = \left(\frac{i_c}{i_b}\right)_{v_c} \quad (4.63)$$

$$h_{oe} = \left(\frac{\partial f_2}{\partial v_c}\right)_{i_b} = \left(\frac{\partial i_c}{\partial v_c}\right)_{i_b} \approx \left(\frac{\Delta i_c}{\partial v_c}\right)_{i_b} = \left(\frac{i_c}{v_c}\right)_{i_b} \quad (4.64)$$

The above equations define the *h*-parameters of the transistor in CE configuration. The same theory can be extended to transistors in other configurations.

The hybrid models and equations given in Table 4.2 are valid for *NPN* as well as *PNP* transistors and hold good for all types of loads and methods of biasing. Table 4.3 gives the typical *h*-parameter values for a transistor and Table 4.4 gives the conversion formulae to find the *h*-parameters for CC and CB configurations given the *h*-parameters for CE configuration.

Table 4.2 *Hybrid model for the transistor in three different configurations*

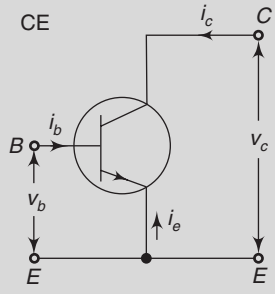
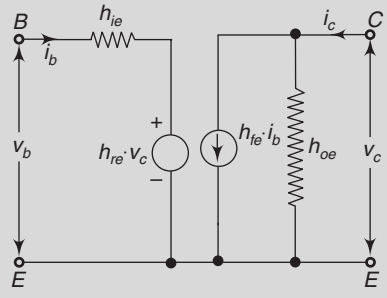
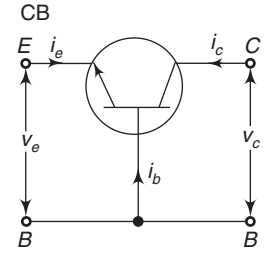
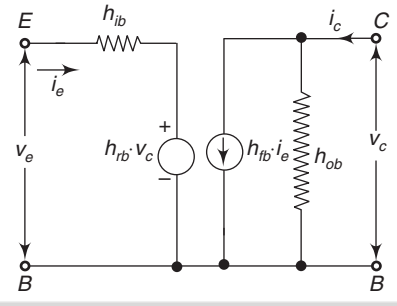
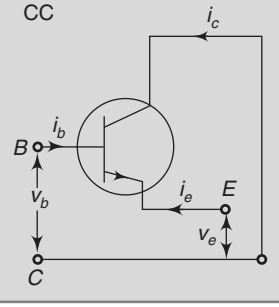
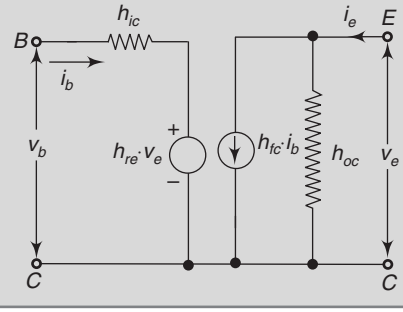
CE 		$v_b = h_{ie} \cdot i_b + h_{re} \cdot v_c$ $i_c = h_{fe} \cdot i_b + h_{oe} \cdot v_c$
CB 		$v_e = h_{ib} \cdot i_e + h_{rb} \cdot v_c$ $i_c = h_{fb} \cdot i_e + h_{ob} \cdot v_c$
CC 		$v_b = h_{ic} \cdot i_b + h_{rc} \cdot v_e$ $i_e = h_{fc} \cdot i_b + h_{oc} \cdot v_e$

Table 4.3 *Typical h-parameter values for a transistor*

Parameter	CE	CC	CB
h_i	1100 Ω	1100 Ω	22 Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	–51	–0.98
h_o	25 μA/V	25 μA/V	0.49 μA/V

Table 4.4 *Conversion formulae for hybrid parameters*

CC	CB
$h_{ic} = h_{ie}$	$h_{ib} = \dfrac{h_{ie}}{1 + h_{fe}}$
$h_{rc} = 1$	$h_{rb} = \dfrac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$
$h_{fc} = -(1 + h_{fe})$	$h_{fb} = \dfrac{-h_{fe}}{1 + h_{fe}}$
$h_{oc} = h_{oe}$	$h_{ob} = \dfrac{h_{oe}}{1 + h_{fe}}$

4.13 ANALYSIS OF TRANSISTOR AMPLIFIER CIRCUIT USING *h*-PARAMETERS

A transistor amplifier can be constructed by connecting an external load and signal source as indicated in Fig. 4.46 and biasing the transistor properly.

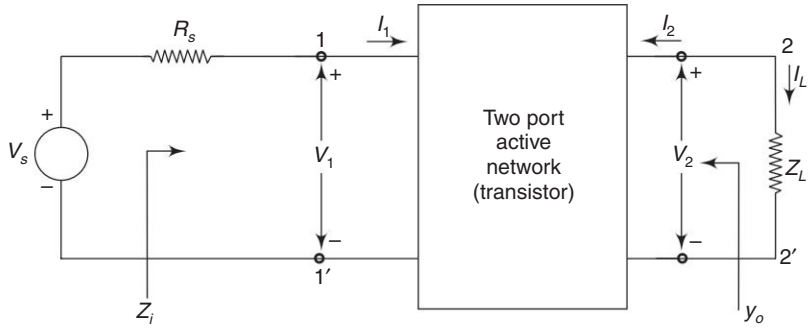


Fig. 4.46 *Basic amplifier circuit*

The two-port active network of Fig. 4.47 represents a transistor in any one of its configurations. The hybrid equivalent circuit is valid for any type of load whether it is pure resistance or impedance or another transistor. It is assumed that *h*-parameters remain constant over the operating range. Further, the input is sinusoidal and I_1, V_1, I_2, and V_2 are phasor quantities.

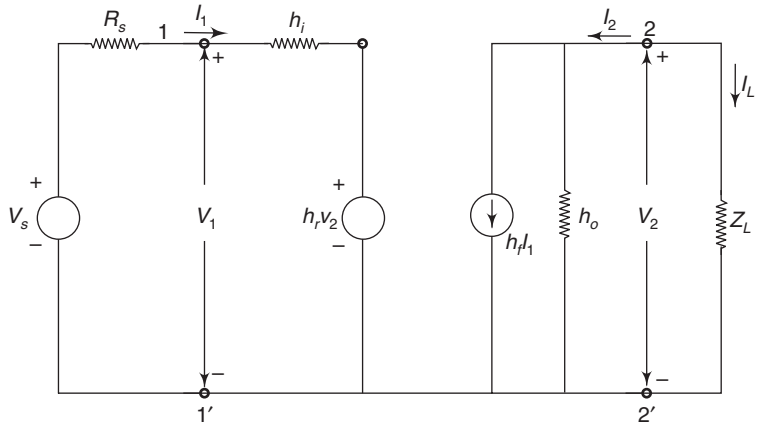


Fig. 4.47 *Circuit of Fig. 4.46 with transistor replaced by its hybrid model*

4.13.1 Current Gain or Current Amplification, A_I

For a transistor amplifier, the current gain A_I is defined as the ratio of output current to input current, i.e.,

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1} \tag{4.65}$$

From the circuit of Fig. 4.47,

$$I_2 = h_f I_1 + h_o V_2 \tag{4.66}$$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$,

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f I_1$$

$$I_2(1 + Z_L h_o) = h_f I_1$$

$$A_I = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L} \tag{4.67}$$

Therefore,

$$A_I = \frac{-h_f}{1 + h_o Z_L}$$

4.13.2 Input Impedance, Z_i

In the circuit of Fig. 4.47, R_s is the signal source resistance. The impedance seen when looking into the amplifier terminals (1,1′) is the amplifier input impedance Z_i, i.e.,

$$Z_i = \frac{V_1}{I_1} \tag{4.68}$$

From the input circuit of Fig. 4.47, $V_1 = h_i I_1 + h_r V_2$

Hence, $$Z_i = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$= h_i + h_r \frac{V_2}{I_1}$$

Substituting

$$V_2 = -I_2 Z_L = A_I I_1 Z_L$$

$$Z_i = h_i + h_r \frac{A_I I_1 Z_L}{I_1}$$

resulting in

$$Z_i = h_i + h_r A_I Z_L \tag{4.69}$$

Substituting for A_I,

$$Z_i = h_i - \frac{h_f}{1 + h_o Z_L} h_r Z_L$$

$$= h_i - \frac{h_f h_r}{Z_L \left(\frac{1}{Z_L} + h_o \right)} Z_L$$

Taking the load admittance as $Y_L = \frac{1}{Z_L}$

$$Z_i = h_i - \frac{h_f h_r}{Y_L + h_o} \tag{4.70}$$

Note that the input impedance is a function of load impedance.

4.13.3 Voltage Gain or Voltage Amplification Factor, A_V

The ratio of output voltage V_2 to input voltage V_1 gives the voltage gain of the transistor, i.e.,

$$A_V = \frac{V_2}{V_1} \tag{4.71}$$

Substituting $$V_2 = -I_2 Z_L = A_I I_1 Z_L$$

$$A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i} \tag{4.72}$$

4.13.4 Output Admittance, Y_o

By definition, Y_o is obtained by setting V_s to zero, Z_L to infinity and by driving the output terminals from a generator V_2. If the current drawn from V_2 is I_2, then $Y_o \equiv \frac{I_2}{V_2}$ with $V_s = 0$ and $R_L = \infty$.

From the circuit of Fig. 4.47,

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by V_2,

$$\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o \tag{4.73}$$

With $V_s = 0$, by KVL in the input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0 \tag{4.74}$$

$$I_1 (R_s + h_i) + h_r V_2 = 0$$

Hence, $$\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}$$

Substituting Eq. (4.74) in Eq. (4.73), we get

$$\frac{I_2}{V_2} = h_f \left(\frac{-h_r}{R_s + h_i} \right) + h_o$$

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} \tag{4.75}$$

From Eq. (4.75), the output admittance is a function of the source resistance. If the source impedance is resistive, then Y_o is real.

4.13.5 Voltage Amplification (A_{Vs}) taking into account the Source Resistance (R_s)

This overall voltage gain A_{Vs} is given by

$$A_{Vs} = \frac{V_2}{V_s} = \frac{V_2 V_1}{V_1 V_s} = A_V \frac{V_1}{V_s} \tag{4.76}$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 4.48,

$$V_1 = \frac{V_s Z_i}{Z_i + R_s} \tag{4.77}$$

$$\frac{V_1}{V_s} = \frac{Z_i}{Z_i + R_s}$$

Then, $$A_{Vs} = \frac{A_V Z_i}{Z_i + R_s} \tag{4.78}$$

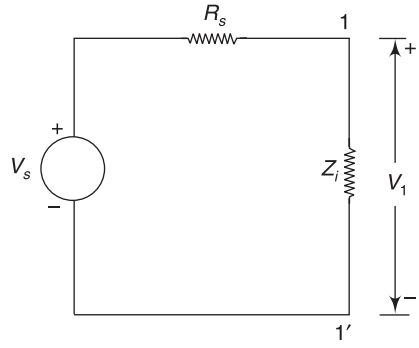


Fig. 4.48 *Equivalent input circuit*

Substituting $$A_V = \frac{A_I Z_L}{Z_i}$$

$$A_{Vs} = \frac{A_I Z_L}{Z_i + R_s} \tag{4.79}$$

Note that if $R_s = 0$, then $A_{Vs} = \dfrac{A_I Z_L}{Z_i} = A_V$. Hence, A_V is the voltage gain with an ideal voltage source (with $R_s = 0$). In practice, A_{Vs} is more meaningful than A_V because the source resistance has an appreciable effect on the overall amplification.

4.13.6 Current Amplification (A_{Is}) taking into account the Source Resistance (R_s)

The modified input circuit using Norton's equivalent circuit for the source for the calculation of A_{Is} is shown in Fig. 4.49.

Overall current gain, $A_{Is} = \dfrac{-I_2}{I_s} = \dfrac{-I_2}{I_1} \cdot \dfrac{I_1}{I_s} = A_I \dfrac{I_1}{I_s}$ (4.80)

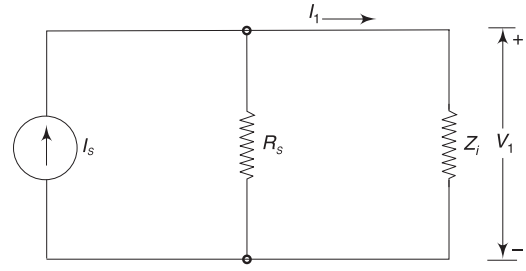


Fig. 4.49 *Modified input equivalent circuit*

From Fig. 4.49, $I_1 = I_s \dfrac{R_s}{R_s + Z_i}$ (4.81)

$$\frac{I_1}{I_s} = \frac{R_s}{R_s + Z_i}$$

and hence, $A_{Is} = A_I \dfrac{R_s}{R_s + Z_i}$ (4.82)

If $R_s = \infty$, then $A_{Is} = A_I$. Hence, A_I is the current gain with an ideal current source (one with infinite source resistance).

From Eq. (4.79),

$$A_{Vs} = \frac{A_I Z_L}{Z_i + R_s} \frac{R_s}{R_s}$$

Then, $A_{Vs} = \dfrac{A_{IS} Z_L}{R_s}$ (4.83)

4.13.7 Operating Power Gain, A_P

From Fig. 4.47, average power delivered to the load is $P_2 = |V_2|\,|I_L| \cos\theta$, where θ is the phase angle between V_2 and I_L. Assume that Z_L is resistive, i.e., $Z_L = R_L$. Since h-parameters are real at low frequencies, the power delivered to the load is $P_2 = V_2 I_L = -V_2 I_2$. Since the input power $P_1 = V_1 I_1$, the operating power gain A_P of the transistor is defined as

$$A_P = \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_V A_I = A_I A_I \frac{R_L}{R_i}$$

$$A_P = A_I^2 \left(\frac{R_L}{R_i} \right) \tag{4.84}$$

The important relations derived above are summarized in Table 4.5.

Table 4.5 *Small signal analysis of a transistor amplifier*

$A_I = \dfrac{-h_f}{1 + h_o Z_L}$	$A_V = \dfrac{A_I Z_L}{Z_i}$
$Z_i = h_i + h_r A_I Z_L = h_i - \dfrac{h_f h_r}{Y_L + h_o}$	$A_{Vs} = \dfrac{A_V Z_i}{Z_i + R_s} = \dfrac{A_I Z_L}{Z_i + R_s} = A_{IS} \dfrac{Z_L}{R_s}$
$Y_o = h_o - \dfrac{h_f h_r}{h_i + R_s} = \dfrac{1}{Z_o}$	$A_{Is} = \dfrac{A_I R_s}{Z_i + R_s} = A_{Vs} \dfrac{R_s}{Z_L}$

EXAMPLE 4.53

A CE amplifier has the *h*-parameters given by h_{ie} = 1000 Ω, $h_{re} = 2 \times 10^{-4}$, h_{fe} = 50, and h_{oe} = 25 μ mho. If both the load and source resistances are 1 kΩ, determine the (a) current gain, and (b) voltage gain.

Solution Given R_s = 1 kΩ and R_L = 1 kΩ

(a) Current gain, $$A_i = \frac{h_{fe}}{1 + h_{oe} \times R_L}$$

$$= \frac{50}{1 + 25 \times 10^{-6} \times 1 \times 10^3} = 48.78$$

(b) Voltage gain, $$A_V = \frac{-h_{fe}}{\left(h_{oe} + \dfrac{1}{R_L}\right) Z_{\text{in}}}$$

Here, $$Z_{\text{in}} = h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + \dfrac{1}{R_L}}$$

$$= 1000 - \frac{2 \times 10^{-4} \times 50}{25 \times 10^{-6} + 1 \times 10^{-3}} = 990.24\ \Omega$$

Therefore, $$A_V = \frac{-50}{(25 \times 10^{-6} + 1 \times 10^{-3}) \times 990.24} = -49.26$$

The output voltage is 180° out of phase to the input signal with a gain of 49.26.

EXAMPLE 4.54

A transistor amplifier circuit R_1 = 100 kΩ, R_2 = 50 kΩ, R_c = 10 kΩ and R_L = 40 kΩ has the *h*-parameters as follows: h_{ie} = 1100 Ω, h_{fe} = 100, $h_{re} = 10 \times 10^{-4}$, $h_{oe} = 4 \times 10^{-4}$ mho. Determine the (a) ac input impedance of the amplifier, and (b) the voltage gain.

Solution At load resistance of the amplifier,

$$R'_L = R_C \| R_L \frac{10 \times 10^3 \times 40 \times 10^3}{10 \times 10^3 + 40 \times 10^3} = 8 \text{ k}\Omega = 8000\ \Omega$$

(a) Input impedance, $$Z_{\text{in}} = h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + \frac{1}{R'_L}}$$

$$= 1100 - \frac{4 \times 10^{-4} \times 100}{4 \times 10^{-4} + \frac{1}{8000}} = 1024\ \Omega$$

The ac input resistance of the entire stage R_{ac} is

$$R_{\text{ac}} = Z_{\text{in}} \| R_1 \| R_2$$

$$= 1024 \| 100 \times 1000 \| 50 \times 1000 = 993.4\ \Omega$$

(b) Voltage gain, $$A_V = \frac{-h_{fe}}{\left(h_{oe} + \frac{1}{R'_L}\right) Z_{\text{in}}} = \frac{-100}{\left(4 \times 10^{-4} + \frac{1}{8000}\right) 1024} = -186.34$$

The output is 180° out of phase to the input with a gain of 186.34.

4.13.8 Comparison of Transistor Amplifier Configurations

The characteristics of three configurations are summarized in Table 4.6. Here, the quantities A_i, A_V, R_i, R_o and A_P, are calculated for a typical transistor whose *h*-parameters are given in Table 4.3. The values of R_L and R_s are taken as 3 kΩ.

Table 4.6 *Performance schedule of three-transistor configurations*

Quantity	CB	CC	CE
A_I	0.98	47.5	– 46.5
A_V	131	0.989	– 131
A_P	128.38	46.98	6091.5
R_i	22.6 Ω	144 kΩ	1065 Ω
R_o	1.72 MΩ	80.5 Ω	45.5 kΩ

The values of current gain, voltage gain, input impedance, and output impedance calculated as a function of load and source impedances can be shown graphically as in Fig. 4.50.

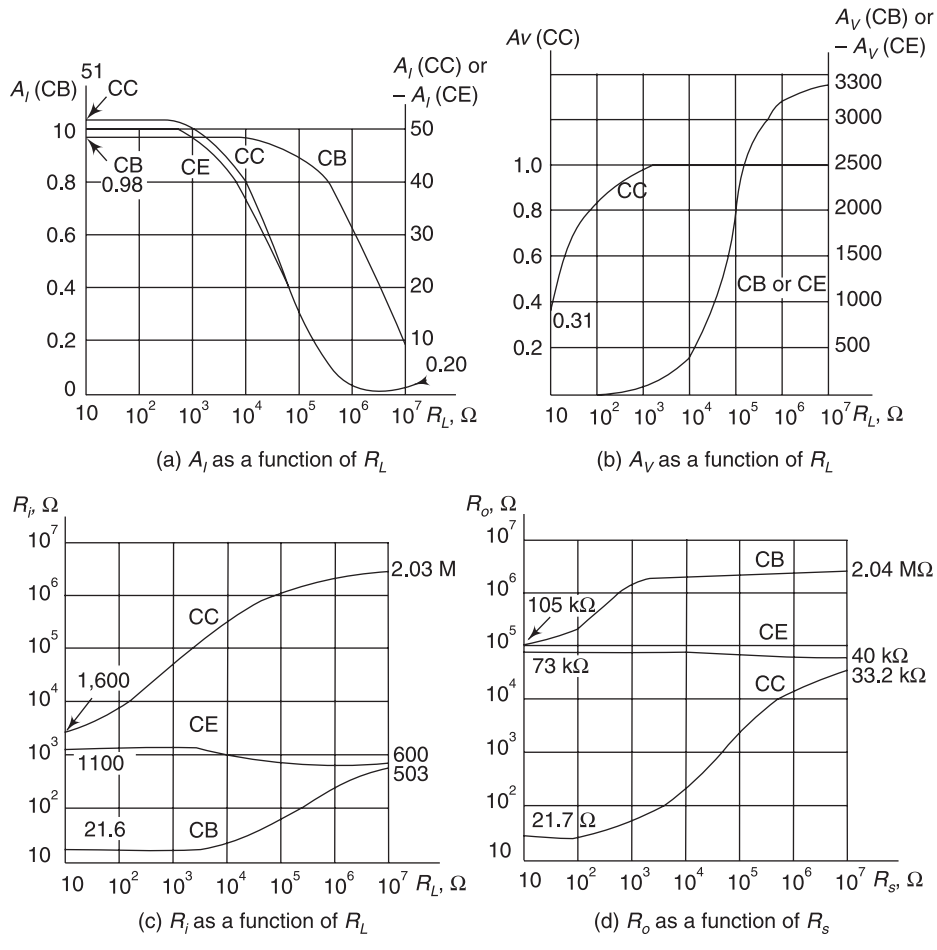


Fig. 4.50 *Comparison of transistor amplifier configurations: (a) Current gain as a function on R_L (b) Voltage gain as a function of R_L (c) Input impedance as a function of R_L (d) Output impedance as a function of R_s*

From Table 4.6 and Fig. 4.50, the performance of the CB, CC, and CE amplifiers can be summarized as follows:

➤ *Characteristics of Common-Base Amplifiers*

(i) Current gain is less than unity and its magnitude decreases with the increase of load resistance R_L.
(ii) Voltage gain A_V is high for normal values of R_L.
(iii) The input resistance R_i is the lowest of all the three configurations.
(iv) The output resistance R_o is the highest of all the three configurations.

- **Applications** The CB amplifier is not commonly used for amplification purpose. It is used for
  (i) matching a very low impedance source
  (ii) as a non-inverting amplifier with voltage gain exceeding unity
  (iii) for driving a high impedance load
  (iv) as a constant current source

➤ *Characteristics of Common-Collector Amplifiers*

(i) For low value of R_L (< 10 kΩ), the current gain A_I is high and almost equal to that of a CE amplifier.
(ii) The voltage gain A_V is less than unity.
(iii) The input resistance is the highest of all the three configurations.
(iv) The output resistance is the lowest of all the three configurations.

▪ **Applications** The CC amplifier is widely used as a buffer stage between a high-impedance source and a low-impedance load. The CC amplifier is called the *emitter follower*.

➤ *Characteristics of Common-Emitter Amplifiers*

(i) The current gain A_I is high for $R_L < 10$ kΩ.
(ii) The voltage gain is high for normal values of load resistance R_L.
(iii) The input resistance R_i is medium.
(iv) The output resistance R_o is moderately high.

▪ **Applications** Of the three configurations, the CE amplifier alone is capable of providing both voltage gain and current gain. Further, the input resistance R_i and the output resistance R_o are moderately high. Hence, the CE amplifier is widely used for amplification purpose.

REVIEW QUESTIONS

1. What is a bipolar junction transistor? How are its terminals named?
2. Explain the operations of *NPN* and *PNP* transistors.
3. What are the different configurations of BJT?
4. Explain the input and output characteristics of a transistor in CB configuration.
5. Explain the Early effect and its consequences.
6. Derive the relationship between α and β.
7. Why does the CE configuration provide large current amplification while the CB configuration does not?
8. Draw the circuit diagram of an *NPN* junction transistor CE configuration and describe the static input and output characteristics. Also, define active, saturation and cut-off regions, and saturation resistance of a CE transistor.
9. How will you determine *h*-parameters from the characteristics of CE configuration?
10. Determine the *h*-parameters from the characteristics of CB configuration.
11. What is the relation between I_B, I_E and I_C in CB configuration?
12. Explain the laboratory setup for obtaining the CC characteristics.
13. Compare the performance of a transistor in different configurations.
14. Define α, β, and γ of a transistor. Show how they are related to each other.
15. Explain how a transistor is used as an amplifier.
16. From the characteristics of CE configuration, explain the large signal, dc, and small signal CE values of current gain.
17. Calculate the values of I_C and I_E for a transistor with $\alpha_{dc} = 0.99$ and $I_{CBO} = 5$ μA. I_B is measured as 20 μA. [*Ans.* $I_C = 2.48$ mA, $I_E = 2.5$ mA]
18. If $\alpha_{dc} = 0.99$ and $I_{CBO} = 50$ μA, find emitter current. [*Ans.* $I_C = 104$ mA, $I_E = 105$ mA]
19. If I_C is 100 times larger than I_B, find the value of β_{dc}. [*Ans.* 100]
20. Find the value of α_{dc}, if β_{dc} is equal to 100. [*Ans.* 0.99]
21. Find the voltage gain of a transistor amplifier if its output is 5 V rms and the input is 100 mV rms. [*Ans.* 50]
22. Find the value of α_{dc}, when $I_C = 8.2$ mA and $I_E = 8.7$ mA. [*Ans.* 0.943]

23. If α_{dc} is 0.96 and $I_E = 9.35$ mA, determine I_C. [*Ans.* 8.98 mA]

24. Describe the two types of breakdown in transistors.

25. Draw the Ebers–Moll model for a *PNP* transistor and give the equations for emitter current and collector current.

26. What is meant by *Q*-point?

27. What is the need for biasing a transistor?

28. What factors are to be considered for selecting the operating point *Q* for an amplifier?

29. Distinguish between dc and ac load lines with suitable diagrams.

30. Briefly explain the reasons for keeping the operating point of a transistor fixed.

31. What is thermal runaway? How can it be avoided?

32. What three factors contribute to thermal instability?

33. Define 'stability factor.' Why would it seem more reasonable to call this an instability factor?

34. Draw a fixed-bias circuit and derive an expression for the stability factor.

35. If the coordinates of the operating point of a CE amplifier using fixed bias or base-resistor method of biasing are $V_{CE} = 6$ V and $I_C = 1$ mA, determine the value of R_C and R_B. [*Ans.* $R_C = 3$ kΩ, $R_B = 300$ kΩ]

36. Consider a common emitter *NPN* transistor with fixed bias as shown in Fig. 4.26. If $\beta = 80$, $R_B = 390$ kΩ, $R_C = 1.5$ kΩ, and $V_{CC} = 30$ V, find the coordinates of the *Q*-point. [*Ans.* 21 V, 6 mA]

37. A germanium transistor having $\beta = 100$ and $V_{BE} = 0.2$ V is used in a fixed-bias amplifier circuit where $V_{CC} = 16$ V, $R_C = 5$ kΩ and $R_B = 790$ kΩ. Determine its operating point.

38. Derive an expression for the stability factor of a collector-to-base bias circuit.

39. Mention the disadvantages of collector-to-base bias. Can they be overcome?

40. In a germanium transistor CE amplifier biased by feedback resistor method, $V_{CC} = 20$ V, $V_{BE} = 0.2$ V, $\beta = 100$ and the operating point is chosen such that $V_{CE} = 10.4$ V and $I_C = 9.9$ mA. Determine the values of R_B and R_C. [*Ans.* 100 kΩ, 1 kΩ]

41. Draw a circuit diagram of CE transistor amplifier using emitter biasing. Describe qualitatively the stability action of the circuit.

42. Draw a voltage-divider bias circuit and derive an expression for its stability factor.

43. Why does the potential divider method of biasing become universal?

44. If the various parameters of a CE amplifier which uses the self-bias method are $V_{CC} = 12$ V, $R_1 = 10$ kΩ, $R_2 = 5$ kΩ, $R_C = 1$ kΩ, $R_E = 2$ kΩ and $\beta = 100$, find (i) the coordinates of the operating point, and (ii) the stability factor, assuming the transistor to be of silicon. [*Ans.* $V_{CE} = 7.05$ V, $I_C = 1.65$ mA, $S = 2.62$]

45. In a CE germanium transistor amplifier using self-bias circuit, $R_C = 2.2$ kΩ, $\beta = 50$, $V_{CC} = 9$ V and the operating point is required to be set at $I_C = 2$ mA and $V_{CE} = 3$V. Determine the values of R_1, R_2 and R_E.
[*Ans.* $R_1 = 17.75$ kΩ, $R_2 = 4.75$ kΩ, $R_E = 800$ Ω]

46. Determine the operating point for the circuit of a potential-divider bias arrangement with $R_2 = R_C = 5$ kΩ, $R_E = 1$ kΩ and $R_1 = 40$ kΩ. [*Ans.* $V_{CE} = 6$ V, $I_C = 1$ mA]

47. Calculate the values of R_1 and R_C in the voltage-divider bias circuit so that *Q*-point is at $V_{CE} = 6$ V and $I_C = 2$ mA. Assume the transistor parameters are: $\alpha = 0.985$, $I_{CBO} = 4$ μA and $V_{BE} = 0.2$ V.
[*Ans.* $R_C = 3$ kΩ, $R_1 = 5.54$ kΩ]

48. Determine the stability factor for a CB amplifier circuit.

49. Draw a circuit which uses a diode to compensate for changes in I_{CO}. Explain how stabilization is achieved in the circuit.

50. How will you provide temperature compensation for the variations of V_{BE} and stabilization of the operating point?

51. Why are hybrid parameters called so? Define them.

52. What are the salient features of hybrid parameters?

53. Derive the equations for voltage gain, current gain, input impedance, and output admittance for a BJT using low frequency *h*-parameter model for (i) CE configuration (ii) CB configuration, and (iii) CC configuration.

54. A CE amplifier is drawn by a voltage source of internal resistance R_s = 1000 Ω and the load impedance is a resistance R_L = 1200 Ω. The *h*-parameters are h_{ie} = 1.2 kΩ, $h_{re} = 2 \times 10^{-4}$, h_{fe} = 60 and h_{oe} = 25 μA/V. Compute the current gain A_I, input resistance R_i, voltage gain A_V and output resistance R_o using exact analysis and using approximate analysis.

[*Ans.* Exact analysis: $A_I = -58.25$, R_i = 1.186 kΩ, $A_V = -58.937$, R_o = 51.162 kΩ,
Approximate analysis: $A_i = -60$, R_i = 1.2 kΩ, $A_V = -60$, $Z_o = \infty$]

55. A CE amplifier uses a load resistor R_C = 2.5 kΩ in the collector circuit and is given by the voltage source V_s of internal resistance 600 Ω. The *h*-parameters of the transistor are h_{ie} = 1300 Ω, $h_{re} = 2 \times 10^{-4}$, h_{fe} = 55 and h_{oe} = 22 μ mhos. Neglecting the biasing resistors across the V_{CC} supply, compute the current gain A_I, input resistance R_i, voltage gain A_V, output resistance R_o, and output terminal resistance R_{oT} for the following values of emitter resistor R_E inserted in the emitter circuit: (i) 200 Ω, (ii) 400 Ω, and (iii) 1000 Ω. Use the approximate model for the transistor if permissible.

[*Ans.* (i) $A_I = -55$, R_i = 12.5 kΩ, $A_V = -11$, $R_o = \infty$, R_{oT} = 2.5 kΩ
(ii) $A_I = -55$, R_i = 23.7 kΩ, $A_V = -5.8$, $R_o = \infty$, R_{oT} = 2.5 kΩ
(iii) $A_I = -55$, R_i = 57.3 kΩ, $A_V = -2.399$, $R_o = \infty$, R_{oT} = 2.5 kΩ.]

OBJECTIVE-TYPE QUESTIONS

1. Which of the following statements is correct for basic transistor amplifier configurations?
(a) CB amplifier has low input impedance and a low current gain.
(b) CC amplifier has low output impedance and a low current gain.
(c) CE amplifier has very poor voltage gain but very high input impedance

2. For a BJT, the common-base current gain $\alpha = 0.98$ and the collector-base junction reverse-bias saturation current I_{CO} = 0.6 μA. This BJT is connected in the common-emitter mode and operated in the active region with a base drive current I_B = 20 μA. The collector current I_C for this mode of operation is
(a) 0.98 mA (b) 0.99 mA (c) 1.0 mA (d) 1.01 mA

3. In most transistors, the collector region is made physically larger than the emitter region
(a) for dissipating heat (b) to distinguish it from other regions
(c) as it is sensitive to ultraviolet rays (d) to reduce resistance in the path of flow of electrons

4. As temperature is increased, the *h*-parameters h_{ie}, h_{re}, h_{fe} and h_{oe} of a transistor
(a) decrease (b) increase (c) remain constant (d) none

5. The biasing method which is considered independent of transistor β_{dc} is
(a) fixed biasing (b) collector feedback bias
(c) voltage-divider bias (d) base bias with collector feedback

6. The power gain of a CB amplifier is approximately equal to
(a) current gain (b) voltage gain (c) both (a) and (b) (d) none of the above

7. The following is a non-inverting amplifier with voltage gain exceeding unity.
(a) CE amplifier (b) CB amplifier (c) CC amplifier (d) None of the above

8. The voltage gain of a CB amplifier has the same magnitude as that of
(a) CE amplifier (b) CC amplifier
(c) both CE and CC amplifiers (d) none of the above

9. An amplifier has good voltage, current, and power gains and the input resistance is low. It is
(a) common-base (b) common-emitter
(c) common-collector (d) none

10. The transistor configuration which provides highest output impedance is
(a) common base (b) common emitter
(c) common collector (d) none of the above

11. When a healthy *NPN* transistor is connected to an ohmmeter such that the base terminal is connected to the red lead of the meter and the emitter terminal to the black lead, then the meter shows
(a) an open circuit (b) some medium resistance
(c) a very small resistance (d) none of the above

12. For $\alpha = 0.9$, the value of β is
(a) 9.9 (b) 49 (c) 99 (d) 100

13. A BJT is said to be operating in the saturation region, if
(a) both junctions are reverse biased
(b) base-emitter junction is reverse biased and base collector junction is forward biased
(c) base-emitter junction is forward biased and base-collector junction reverse biased
(d) both the junctions are forward biased

14. For an *NPN* bipolar transistor, what is the main stream of current in the base region?
(a) Drift of holes (b) Diffusion of holes
(c) Drift of electrons (d) Diffusion of electrons

15. In saturation region in an *NPN* transistor,
(a) V_{CB} is –ve and V_{BE} is +ve (b) V_{CB} is +ve and V_{BE} is –ve
(c) both V_{CB} and V_{BE} are +ve (d) both V_{CB} and V_{BE} are –ve

16. The internal resistance of a current source used in the model of a BJT while analyzing a circuit using BJT is
(a) very high (b) very low
(c) zero (d) of the order of a few mega-ohms

17. The common-emitter short-circuit current gain β of a transistor
(a) is a monotonically increasing function of the collector current I_C.
(b) is a monotonically decreasing function of I_C.
(c) increases with I_C, for low I_C, reaches a maximum and then decreases with further increase in I_C.
(d) is not a function of I_C.

18. The resistance of thermistor
(a) decreases exponentially with increase of temperature
(b) decreases exponentially with decrease of temperature
(c) increases exponentially with increase of temperature
(d) increases exponentially with decrease of temperature

19. The Ebers–Moll model is applicable to
(a) bipolar junction transistors (b) NMOS transistors
(c) unipolar junction transistors (d) junction field-effect

20. The Early effect in a bipolar junction transistor is caused by
(a) fast-turn-on (b) fast-turn-off
(c) large collector-bass reverse bias (d) large emitter-base forward bias

21. If the base resistor is shorted in the fixed-bias circuit, then
(a) the transistor may get damaged
(b) the base voltage will be zero
(c) the collector voltage will be equal to the supply voltage
(d) the collector current is zero

22. The parameter h_1 has the dimension of
(a) Ω (b) ℧ (c) V (d) dimensionless

23. The amplifier that gives unity voltage gain is
(a) common emitter (b) common collector (c) common base (d) all the above

24. The amplifier that gives 180^o voltage phase shift is
(a) common emitter (b) common collector (c) common base (d) all the above

25. The amplifier that gives power gain approximately equal to current gain is
(a) common emitter (b) common collector (c) common base (d) all the above

26. In a common-emitter amplifier having a small unbypassed emitter resistance (R_E), the input resistance is approximately equal to
(a) R_E (b) h_{fe} (c) $h_{fe} \cdot R_E$ (d) R_E/h_{fe}

27. Which of the following transistor amplifiers has the highest voltage gain?
(a) Common-base (b) Common-collector (c) Common-emitter (d) all of them

28. If the internal resistance of the ac signal source in an ac amplifier is larger, then its
(a) overall voltage gain is greater (b) input impedance is greater
(c) current gain is smaller (d) circuit voltage gain is smaller

29. In a single-stage amplifier, the voltage gain is increased when
(a) its ac load is decreased (b) the load resistance is increased
(c) the emitter resistance R_E is increased (d) the resistance of signal source is increased

30. The *h*-parameter is called hybrid parameter because it is
(a) different from *y*- and *z*-parameters
(b) mixed with other parameters
(c) applied to circuits contained in a box
(d) defined by using both open-circuit and short-circuit terminations

31. The input impedance h_{11} of a network with output shorted is expressed by
(a) v_1/i_1 (b) v_1/v_2 (c) i_2/i_1 (d) i_1/v_2

32. If the spacing between the curves of the output characteristics of a transistor is larger, then
(a) the value of h_{fe} is smaller
(b) the value of h_{fe} is larger
(c) h_{fe} is independent of the spacing
(d) h_{fe} can increase or decrease depending upon the circuit configuration

33. Choose the correct match for input resistance of various amplifier configurations shown below:

Configuration	*Input resistance*
CB: Common Base	LO: low
CC: Common Collector	MO: Moderate
CE: Common Emitter	HI: High

(a) CB–LO, CC–MO, CE–Hi (b) CB–LO, CC–HI, CE–MO
(c) CB–MO, CC–HI, CE–LO (d) CB–HI, CC–LO, CE–MO

5 Power Semiconductor Devices and Field Effect Transistor

5.1 INTRODUCTION

In general, a thyristor is a power semiconductor device having three or more junctions. Such a device acts as a switch without any bias and can be fabricated to have voltage ratings of several hundred volts and current ratings from a few amperes to almost thousand amperes. Physical transistors have certain limitations in terms of maximum current, voltage and power. These limitations are not considered for normal transistors, because it was assumed that the transistors which are capable of handling the current, voltage and power dissipation within a transistor does not cause any damage to the circuit. But in the design of power amplifiers, it is necessary to consider the limitations of a transistor. The limitations are maximum rated current (amp), maximum rated voltage (volts) and maximum rated power (watts). As power amplifiers use BJTs and MOSFETs, the limitation effect is considered on these two transistors. The maximum power limitation is related to maximum allowed temperature of a transistor (BJTs or MOSFETs) which in turn is a function of the rate at which heat is removed. The operation and characteristics of thyristors, silicon controlled rectifier, power BJT and power MOSFET are discussed in this chapter.

A Field Effect Transistor (FET) is a device in which the flow of current through the conducting region is controlled by an electric field. As current conduction is only by majority carriers, FET is said to be a unipolar device. Based on the construction, the FET can be classified into two types as Junction FET (JFET) and Metal Oxide Semiconductor FET (MOSFET). The construction, operation, characteristics and applications of both FET and MOSFET are discussed in this chapter.

5.2 PRINCIPLE OF OPERATION AND CHARACTERISTICS OF THYRISTORS

Conventional thyristors are used as ideal switches in power electronic applications. They have the capability of blocking several thousand volt in the OFF-state and conducting several thousand ampere in the ON-state with only small ON-state voltage drop.

The only disadvantage of a conventional thyristor is that when the gate turns into ON-state, the gate loses its control on the device and hence, its use in switch-mode applications is prevented. The only way to bring the device back to OFF-state is by reducing the anode forward current to a level below that of the holding current.

In order to speed up turn-OFF capability, the thyristor requires structural modifications and the performance compromises. This section discusses the structure and operation of Gate Turn-OFF Thyristor (GTO) that has turn-OFF capability. GTOs can be turned OFF by applying a negative gate current.

5.2.1 Basic Structure of the GTO

The GTO is a three-terminal device with anode, cathode, and gate terminals. The GTO has the same four layer structure as the conventional thyristor, but special modifications are made to the structure to enable the gate to turn-OFF the device.

The operation of a GTO is very simple. Stopping the current through the gate can turn OFF the GTO. Injecting current into the gate as in the conventional thyristor can turn it ON. The GTO has a complex structure that enables such simpler operation of turning ON and OFF. Figure 5.1 gives the structure of a GTO.

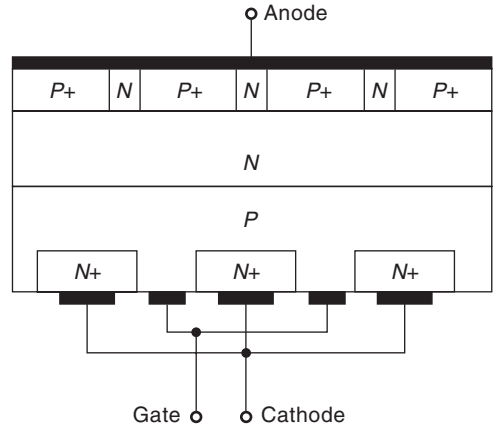


Fig. 5.1 *Gate turn-OFF thyristor*

The GTO has highly doped *N*-regions in the *P*-layer at the anode, the '+' sign indicates a higher concentration of *N*- or *P*-type materials. The major modifications include a highly interdigited gate cathode structure with small cathode and gate widths, the use of anode shorts, and a shorter carrier lifetime in the drift region than that in a conventional thyristor.

In the GTO, during the absence of the gate current, a positive voltage at the anode with respect to the cathode, will reverse bias the *N*-*P* junction at the center of the device and as a result, no conduction occurs. A negative voltage at the anode and a positive voltage at the cathode will break down the anode junction at a low level.

The interdigitated nature of the gate (i.e., the cathode and gate electrodes are arranged alternatively in a large number of closely located narrow channels) results in a very rapid spread of conduction in the silicon, but it is necessary to maintain the gate current at a high level for a longer time to ensure that latching takes place. To minimize the anode–cathode voltage drop, it is advantageous to maintain a low level of gate current throughout conduction, otherwise the ON-state voltage and hence, conduction losses will be slightly higher. Applying a single positive current pulse at the gate can turn ON a GTO thyristor, and a pulse of negative gate current can turn it OFF. The gate current, therefore, controls both ON-state and OFF-state operation of the device. Gate turn-OFF thyristor should be protected against over currents because the gate turn OFF current cannot exceed a specified maximum value.

The symbols of GTO are shown in Fig. 5.2. The two-transistor analogy of GTO is shown in Fig. 5.3.

When a positive pulse is applied to the base of an *NPN* transistor, the GTO switches regeneratively into the ON-state. This pronounced regenerative latching effect enables the thyristor not to stay in the ON-state at the gate. In GTO, internal regeneration is reduced by a reduction in the current gain of the *PNP* transistor, while by drawing sufficient current from the gate, turn-OFF can be achieved.

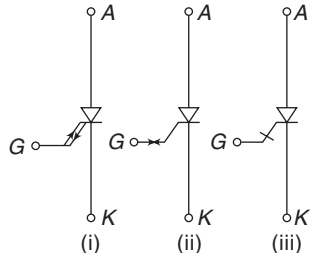


Fig. 5.2 *Circuit symbols*

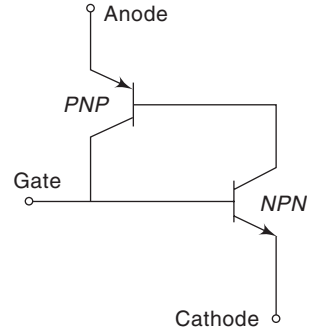


Fig. 5.3 *Two-transistor analogy of GTO*

When a negative pulse is applied to the gate, excess carriers are drawn from the base region of *NPN* transistor and the collector current of the *PNP* transistor is diverted into the external gate circuit. Thus, the base drive

of the *NPN* transistor is removed, and which in turn removes the base drive of the *PNP* transistor and stops conduction.

The reduction in gain of the *PNP* transistor can be achieved by either of the following two techniques or by the combination of both. One technique involves the diffusion of gold or other heavy metal to reduce minority carrier lifetime. The other technique is introduction of anode to *N*-base short-circuiting spots. Device characteristics depend on the technique used. The gold-doped GTO retains its reverse blocking capacity, and has a high ON-state voltage drop. On the other hand, the shorted anode emitter construction has a lower ON-state voltage, but it loses the ability to block reverse voltage.

5.2.2 Switching Characteristics

A simplified gate-drive circuit for a GTO with separate dc supplies for turn-ON and turn-OFF is shown in Fig. 5.4. The GTO is gated into conduction by transistor T_1 in the turn-ON circuit.

The switching device in the turn-OFF circuit should have a high peak current achieved by an auxiliary thyristor (TH_1) in the circuit. Thyristor initiates the turn-OFF programme. The inductor L will enhance the turn-OFF performance. The energy required to turn OFF the GTO is much less than that needed to turn OFF a conventional thyristor.

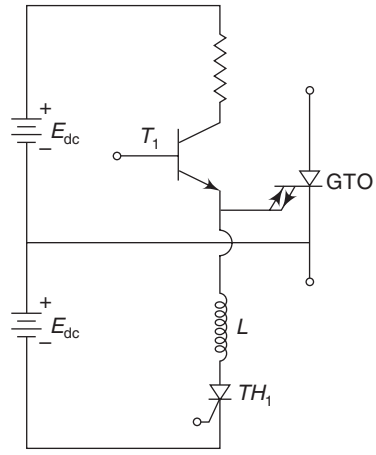


Fig. 5.4 *A simplified gate-drive circuit for a GTO*

5.2.3 Gate Turn-ON

The turn-ON process of a GTO is similar to that of the conventional thyristor. The device is turned ON by a steep fronted pulse of gate current, and the gate drive can be removed without the loss of conduction when the anode current exceeds the latching current level. The anode current of the GTO does not respond immediately to the applied gate signal. As shown in Fig. 5.5, the turn-ON response of the anode current is characterized by a turn-ON time, T_{on}, which consists of a delay time, t_d, and a rise time t_r.

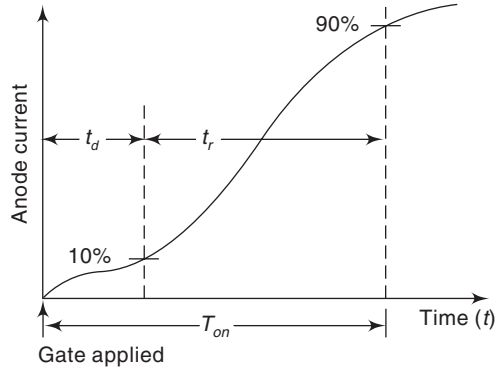


Fig. 5.5 *The turn-ON response of the anode current characterized by turn-ON time consisting of delay and rise times*

The GTO has a faster turn-ON time than conventional thyristors because of its narrow emitter width. The delay time decreases as the gate current increases. The rise time does not vary as long as the gate current is smaller than the anode current in the ON-state. It is observed that since the delay time is reduced and rise time rate is faster, the turn-ON time becomes shorter.

5.2.4 Gate Turn-OFF

The conducting electron-hole plasma occupies the central region of the GTO crystal in the conducting state. In order to turn OFF the device, a negative pulse is applied to the gate and thereby, the excess holes in the P region are removed. During the storage phase of the turn-OFF process, the negative gate current extracts the excess holes in the *P*-base through the gate terminal. As a result, the anode current path is pinched into a

narrow filament under each cathode finger. In this non-regenerative three-layer section of the crystal, current cannot sustain itself and, thus, the current filaments quickly collapse during the full period. Thus, there is a small but slowly decaying tail of anode current due to residual charges in the remote regions of the crystal.

5.2.5 Current-Voltage Characteristics

The peak value of OFF-gate current, I_{gp} is a function of the anode current, I_A, prior to turn-OFF. The turn-OFF gain, β_{off} expressed as $\beta_{\text{off}} = \dfrac{I_d}{I_{gp}} = \dfrac{\alpha_2}{\alpha_1 + \alpha_2 - 1}$ is typically between 3 and 5. The turn-OFF gain must be very large while converting a conventional thyristor into a GTO so that large values of negative gate current can be avoided. Here, α_2 should be near unity and α_1 should be small. The controllable current is the maximum anode current that can be interrupted by gate turn-off. This is dependent on the device structure and gate-drive conditions. The GTO will get damaged if an attempt is made to turn-OFF an anode current that is greater than the maximum controllable current.

The *I–V* characteristic of GTO is shown in Fig. 5.6. In the forward direction, the *I–V* characteristics are identical to that of a conventional thyristor. In the reverse direction, the GTO has virtually no blocking capability because of the anode short structure. The latching current is about 400 mA for conventional thyristor and 2 A for GTO.

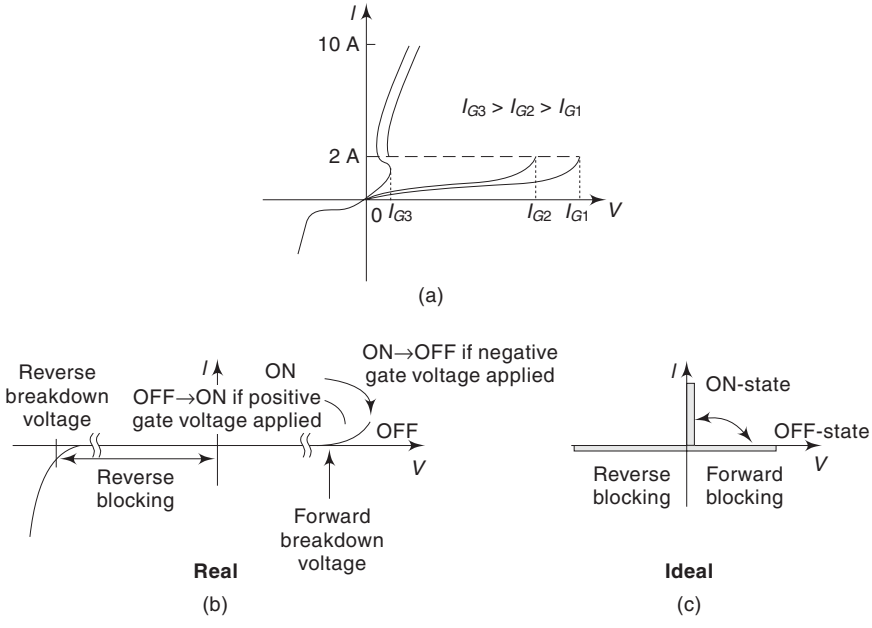


Fig. 5.6 *I-V characteristics of GTO*

Large-power GTOs require several ampere of latching current as compared to conventional thyristors of the same rating. If the gate current is insufficient to turn on the GTO, it behaves like a high voltage, low-gain transistor with considerable anode current. This leads to a noticeable power loss under such conditions. The ON-state voltage is 3.4 V for a typical 550 A, 1200 V GTO. GTOs are available to handle thousands of voltage and current up to the frequency of 10 kHz.

5.2.6 Advantages of GTO

The GTO has the following advantages compared to conventional thyristor:

(i) Since the GTO is a faster turn-OFF device, it is used for high frequency switching applications.
(ii) It has high blocking voltage and large current capability.
(iii) It eliminates commutating components in forced commutation and hence, GTO inverter has 60 percent of size and weight of the conventional thyristor unit and has a higher efficiency.
(iv) It is used as a switching element and its use in inverter is growing rapidly.
(v) It reduces acoustic and electromagnetic noises.

5.2.7 Disadvantages of GTO

(i) Latching and holding current values are high.
(ii) The ON-state voltage drop and the associated loss are more.
(iii) The triggering gate current of GTO is higher due to multi-cathode structure as compared to conventional thyristor.

5.2.8 Applications of GTO

The GTO has a higher blocking voltage capability and higher ON-state gain. In high-power applications, the GTO eliminates the conventional thyristor in various applications like dc-ac inverters and dc-dc choppers.

5.3 SILICON-CONTROLLED RECTIFIERS

The basic structure and circuit symbol of an SCR is shown in Fig. 5.7. It is a four-layer three-terminal device in which the end *P*-layer acts as anode, the end *N*-layer acts as cathode, and the *P*-layer nearer to cathode acts as gate. As leakage current in silicon is very small compared to germanium, SCRs are made of silicon and not germanium.

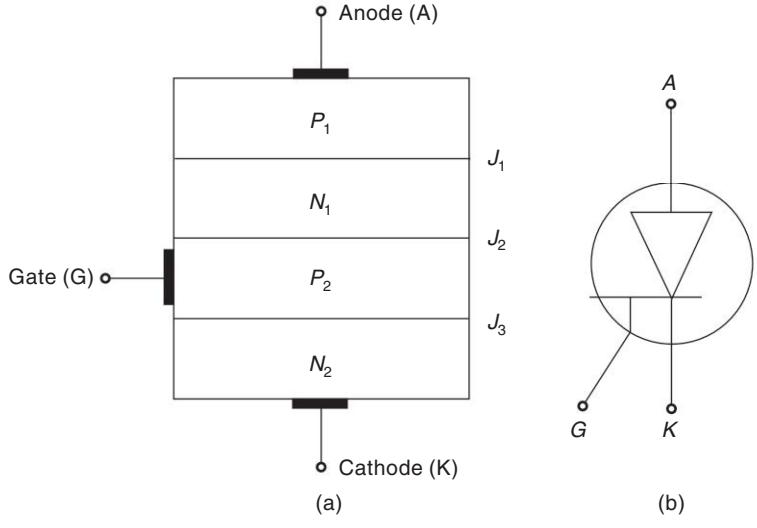


Fig. 5.7 *SCR (a) Basic Structure and (b) Circuit symbol*

➤ ***Characteristics of SCR*** The characteristics of the SCR are shown in Fig. 5.8. SCR acts as a switch when it is forward biased. When the gate is kept open, i.e., gate current $I_G = 0$, operation of SCR is similar to the *PNPN* diode. When $I_G < 0$, the amount of reverse bias applied to J_2 is increased. So the breakover voltage V_{BO} is increased. When $I_G > 0$, the amount of reverse bias applied to J_2 is decreased, thereby decreasing the breakover voltage. With very large positive gate current, breakover may occur at a very low voltage such that the characteristics of SCR is similar to that of the ordinary *PN* diode. As the voltage at which the SCR is switched 'ON' can be controlled by varying the gate current I_G, it is commonly called as controlled switch. Once the SCR is turned ON, the gate loses control, i.e., the gate cannot be used to switch the device OFF. One way to turn the device OFF is by lowering the anode current below the holding current I_H by reducing the supply voltage below the holding voltage V_H, keeping the gate open.

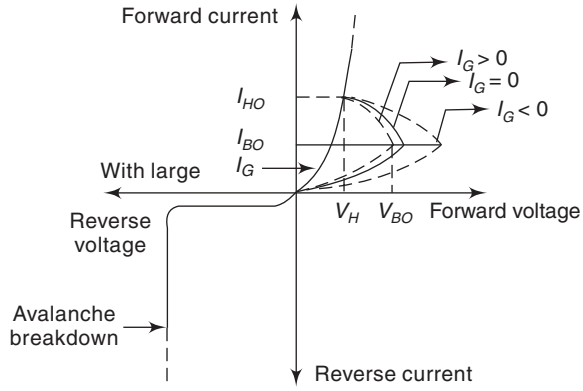


Fig. 5.8 *Characteristics of SCR*

➤ ***Application of SCR*** The SCR is used in relay control, motor control, phase control, heater control, battery chargers, inverters, regulated power supplies, and as static switches.

➤ ***Two-transistor Version of SCR*** The operation of an SCR can be explained in a very simple way by considering it in terms of two transistors, called the two-transistor version of SCR. As shown in Fig. 5.9, an SCR can be split into two parts and displaced mechanically from one another but connected electrically. Thus, the device may be considered to be constituted by two transistors T_1 (PNP) and T_2 (NPN) connected back to back.

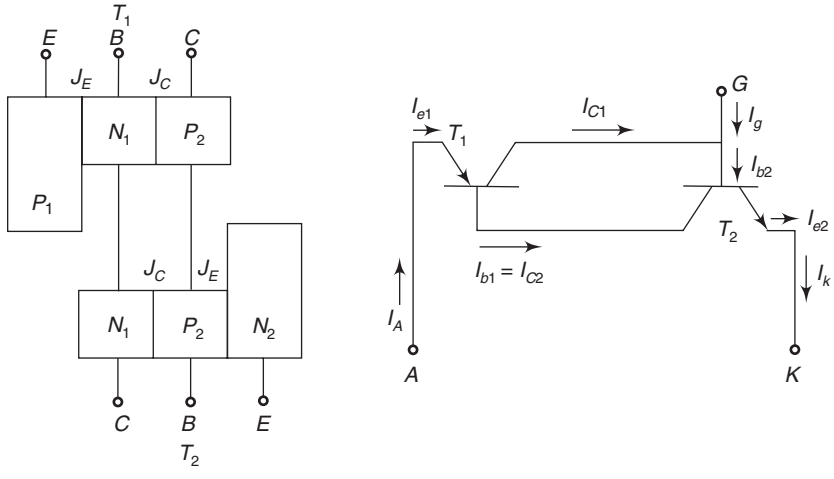


Fig. 5.9 *Two-transistor version of SCR*

Assuming the leakage current of T_1 to be negligibly small, we obtain

$$I_{b1} = I_A - I_{c1} = I_A - \alpha_1 I_A = (1 - \alpha_1)\, I_A \tag{5.1}$$

Also, from Fig. 5.9, it is clear that

$$I_{b1} = I_{C2} \tag{5.2}$$

and

$$I_{C2} = \alpha_2 I_K \tag{5.3}$$

Substituting the values given in Eqs (5.2) and (5.3) in Eq. (5.1), we get

$$(1 - \alpha_1)\, I_A = \alpha_2 I_K \tag{5.4}$$

We know that

$$I_K = I_A + I_g \tag{5.5}$$

Substituting Eq. (5.5) in Eq. (5.4), we obtain

$$(1 - \alpha_1)\, I_A = \alpha_2 (I_A + I_g)$$

i.e.,

$$(1 - \alpha_1 - \alpha_2) I_A = \alpha_2 I_g$$

i.e.,

$$I_A = \left[\frac{\alpha_2 I_g}{1 - (\alpha_1 + \alpha_2)}\right] \tag{5.6}$$

Equation (5.6) indicates that if $(\alpha_1 + \alpha_2) = 1$, then $I_A = \infty$, i.e., the anode current I_A suddenly reaches a very high value approaching infinity. Therefore, the device suddenly triggers into ON state from the original OFF state. This characteristic of the device is known as its *regenerative action.*

The value of $(\alpha_1 + \alpha_2)$ can be made almost equal to unity by giving a proper value of positive current I_g for a short duration. This signal I_g applied at the gate which is the base of T_2 will cause a flow of collector current I_{C2} by transferring T_2 to its ON state. As $I_{C2} = I_{b1}$, the transistor T_1 will also be switched ON. Now, the action is regenerative since each of the transistors would supply base current to the other. At this point even if the gate signal is removed, the device keeps on conducting, till the current level is maintained to a minimum value of holding current.

5.4 THYRISTOR RATINGS

➤ ***Latching Current (I_L)*** Latching current is the minimum current required to latch or trigger the device from its OFF-state to its ON-state.

➤ ***Holding Current (I_H)*** Holding current is the minimum value of current to hold the device in the ON-state. For turning the device OFF, the anode current should be lowered below I_H by increasing the external circuit resistance.

➤ ***Gate Current (I_g)*** Gate current is the current applied to the gate of the device for control purposes. The minimum gate current is the minimum value of current required at the gate for triggering the device. The maximum gate current is the maximum value of current applied to the device without damaging the gate. More the gate current, earlier is the triggering of the device and vice versa.

➤ ***Voltage Safety Factor (V_f)*** Voltage safety factor V_f is a ratio which is related to the PIV, the RMS value of the normal operating voltage as,

$$V_f = \frac{\text{peak inverse voltage (PIV)}}{\sqrt{2} \times \text{rms value of the operating voltage}}$$

The value of V_f normally lies between 2 and 2.7. For a safe operation, the normal working voltage of the device is much below its PIV.

5.5 POWER BJT

➤ *Construction*

The structure of a vertically oriented *NPN* power transistor with the doping levels and thickness of the layers is shown in Fig. 5.10. This type of configuration has a large cross sectional area to handle large currents and minimize the thermal resistance of the transistor. Here, the collector terminal is at the bottom.

The primary collector N^- region, called drift region, has a low-doped impurity concentration 10^{20} m^{-3} in such a way that the voltage can be applied across base-collector terminals without initiating breakdown. This region has a thickness of about 50–200 μm. The thickness of the drift region determines the breakdown voltage of the transistor.

Another N^+ region has a higher doping concentration (typically 10^{25} m^{-3}) which reduces the collector resistance and makes contact with the external terminal. This region has a thickness of around 250 μm. The doping in the emitter layer is large (typically 10^{25} m^{-3}), whereas the base doping is comparatively less (10^{22} m^{-3}).

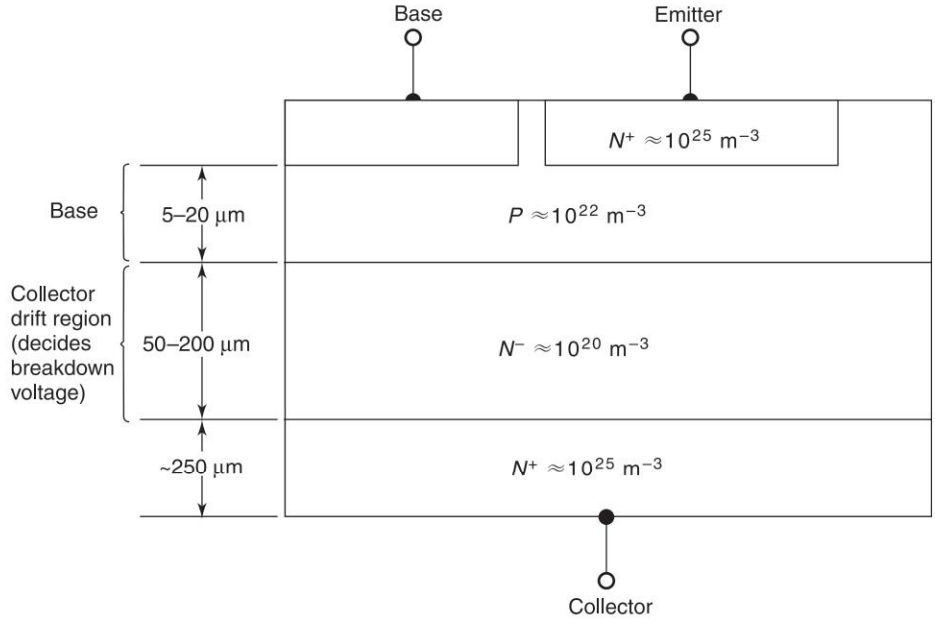


Fig. 5.10 *Cross section of a vertical NPN power BJT*

A sufficient base width is required to prevent punch-through breakdown. Since the small base thickness of about 5–20 μm reduces the breakdown voltage, the amplification capabilities and the breakdown voltages are to be compromised in power transistors. A large base-collector voltage implies a relatively large space-charge width induced in the collector and base regions.

➤ V-I Characteristics

Power transistors are generally large area devices. The properties of power transistors vary from small-signal devices in terms of differences in geometry and doping concentrations. Table 5.1 compares the various parameters of small-signal BJT to those of two-power BJTs. The current gain of power transistors is in the range of 5 to 20 which is smaller to that of small-signal BJTs. But the current gain is a strong function of collector current and temperature. The current gain versus collector current characteristics of 2N3055 power BJT at various temperatures is shown in Fig. 5.11. The current gain drops off for high current levels. The parasitic resistances in the base and collector regions may become significant by affecting the transistor terminal characteristics.

Table 5.1

Parameter	Small-Signal BJT (2N2222A)	Power BJT (2N3055)	Power BJT (2N6078)
$V_{CE\,(max)}$ in V	40	60	250
$I_{C\,(max)}$ in A	0.8	15	7
$P_{D(max)}$ in W (at T =25°C)	1.2	115	45
b	35–100	5–20	12–70
f_T in MHz	300	0.8	1

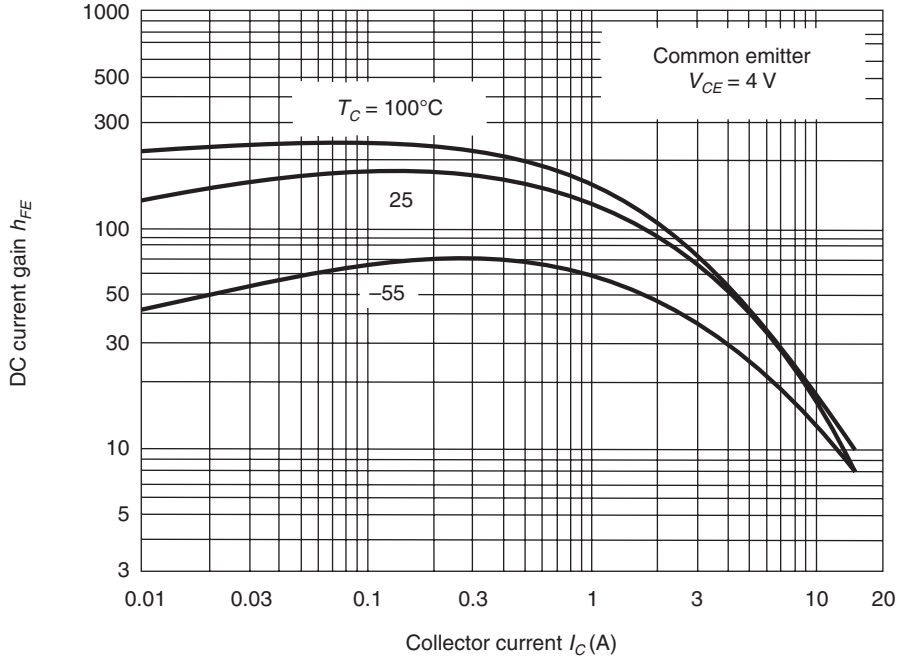


Fig. 5.11 *DC characteristics of β vs I_c*

The maximum rated collector current $I_{C(\text{rated})}$ is related to the maximum current that the wires connecting the semiconductor to the external terminals can handle or the collector current at which the current gain falls below a minimum specified value or the current that leads to the maximum power dissipation when the transistor is in saturation.

In BJTs, the maximum voltage limitation is associated with avalanche breakdown in the reverse-biased base-collector junction. In common-emitter configuration, the breakdown voltage mechanism involves the transistor gain and breakdown phenomenon on the *PN* junction. Typical I_C versus V_{CE} characteristics curve of BJT is shown in Fig. 5.12. When the base terminal is open circuited, i.e., $I_B = 0$, the breakdown voltage is V_{CE0} and from Fig. 5.12, its value is 130 V.

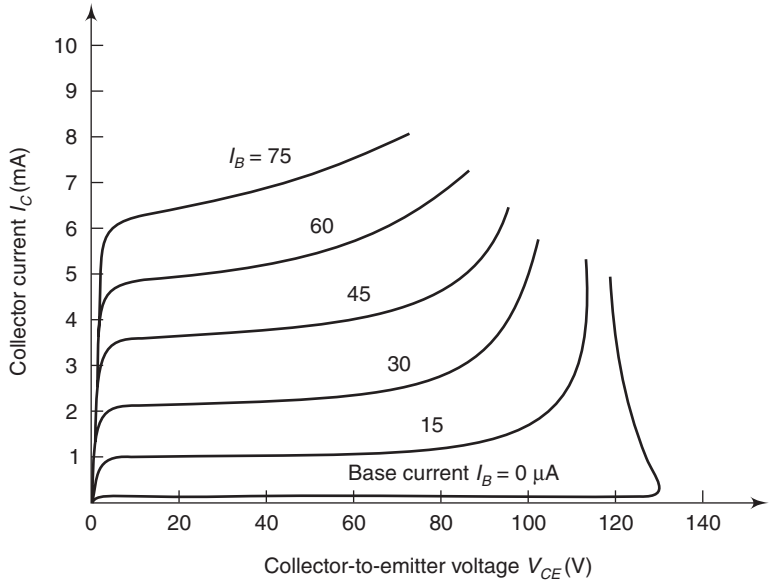


Fig. 5.12 *I_C versus V_{CE} characteristics*

When the transistor is biased in the active region, the collector current begins to increase significantly before breakdown voltage V_{CE0} is reached. Once the breakdown has occurred, all the curves tend to merge to the same collector-emitter voltage. The curves merging voltage is denoted as $V_{CE\,(\text{sus})}$ and it is the minimum voltage necessary to sustain the transistor in breakdown and from Fig. 5.12, the approximate value of $V_{CE\,(\text{sus})}$ is 115 V.

When operating BJT at high voltage and at high current, another breakdown effect will occur and it is called *second breakdown*. Slight non-uniformities in the current density produce an increased heating of local region. The resistance level of the semiconductor material is decreased because of increased heating in the local region.

The effect results in positive feedback, and the current continues to increase, which further increases the temperature, until the semiconductor material may actually be melt.

The instantaneous power dissipation in a BJT is given by

$$P_Q = V_{CE}I_C + V_{BE}I_B \tag{5.7}$$

where the base current I_B is generally much smaller than the collector current I_C. Therefore, the instantaneous power dissipation is approximated to

$$P_Q \cong V_{CE}I_C \tag{5.8}$$

By integrating Eq. (5.8) over one cycle, the average power is given by

$$\overline{P}_Q = \frac{1}{T}\int_O^T V_{CE}I_C dt \tag{5.9}$$

The average power dissipated in BJT must be kept below a specified maximum value, to ensure that the temperature of the device remains below the maximum value. If the collector current and collector-emitter voltage are DC quantities, then maximum rated power P_T for BJT can be written as

$$P_T = V_{CE}I_C \tag{5.10}$$

The average power limitation P_T is a hyperbola as per the above equation.

The maximum current, voltage and power limitations are illustrated on the I_C versus V_{CE} characteristics as shown in Fig. 5.13(a). Safe Operating Area (SoA) is the region where a transistor can be operated safely and is bounded by $I_{C\max}$, $V_{CE(\text{sus})}$, P_T and transistor's second breakdown characteristics. Figure 5.13(b) shows the safe operating area in linear scale and in logarithmic scale. The $I_C - V_{CE}$ operating point may move momentarily outside the safe operating area without damaging the transistor. But this depends on how far and how long the *Q*-point moves outside the area.

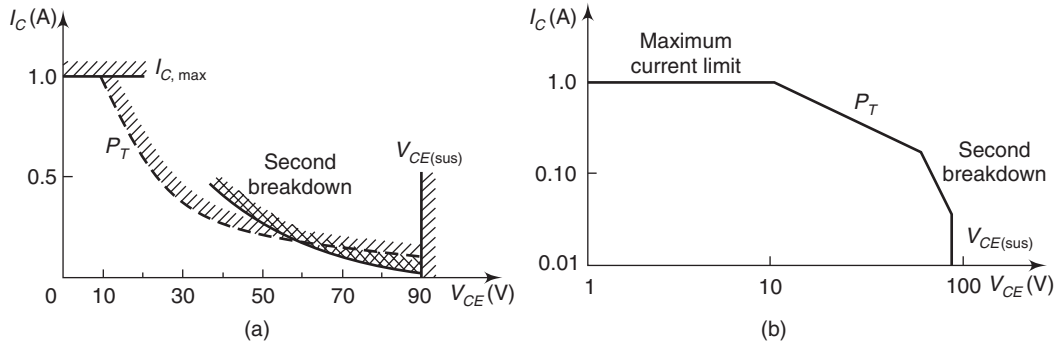


Fig. 5.13 *(a) I_C versus V_{CE} characteristics (b) SoA*

Power transistors which are designed to handle large current require large emitter areas to maintain reasonable current densities. These transistors are usually designed with narrow emitter widths to minimize the parasitic base resistance and fabricated as an interdigitated structure as shown in Fig. 5.14. In each emitter leg, small resistors are incorporated which helps to maintain equal current in each *B-E* junction.

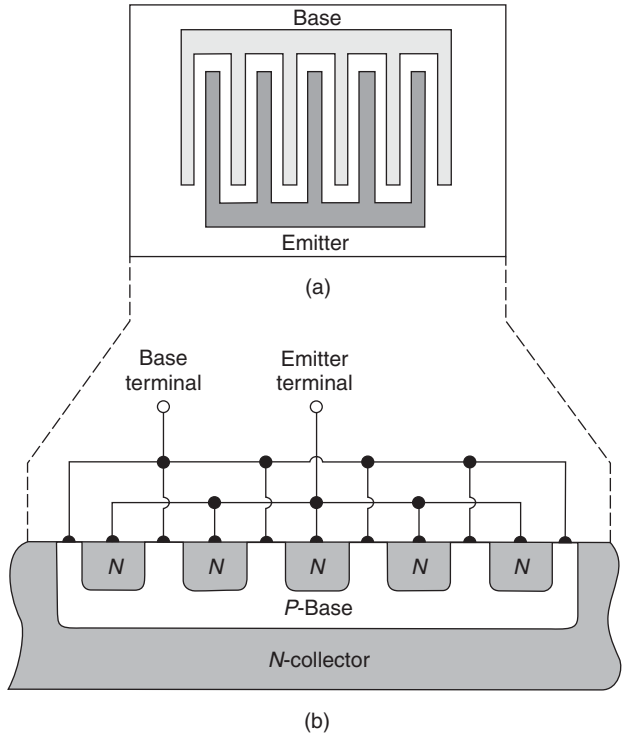


Fig. 5.14 *Interdigitated structure for power transistor (a) Top view and (b) Cross-sectional view*

5.6 POWER MOSFET

Two *N*-channel power MOSFETs with parameters are listed in Table 5.2. The drain currents are in ampere range and breakdown voltages are in the hundreds of volt range. Like BJT, a MOSFET has also to be operated in safe region.

Table 5.2

Parameter	2N6757	2N6792
V_{DS}(max) in V	150	400
I_D max (at $T = 25^{\circ}C$)	8	2
P_D in W	75	20

Power MOSFETS are different from bipolar power transistor in terms of operating principles and performance. The performance characteristics of power MOSFETs include faster switching time, no second breakdown, stable gain and response time over a wide temperature range. Transconductance versus drain current curves for different temperatures is shown in Fig. 5.15(a). The variation with temperature of the MOSFET transconductance is less.

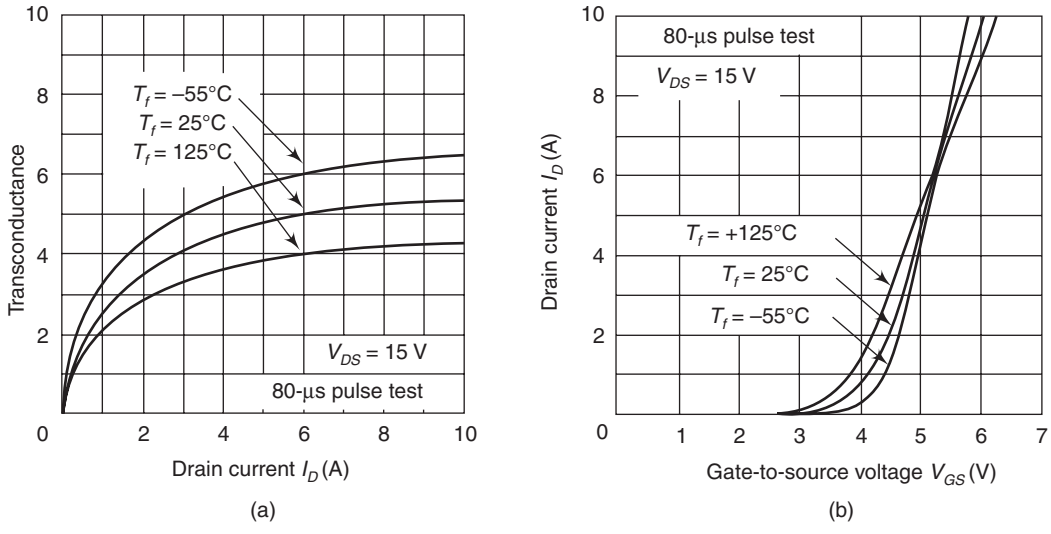


Fig. 5.15 *(a) Transconductance vs drain current characteristics*
(b) I_D versus V_{GS} characteristics for different temperatures

The MOSFET has high input impedance and it is a voltage-controlled device like JFET. Unlike the driver circuit of BJT, a MOSFET driver circuit is simple. The gate of a 10 A power MOSFET may be driven by the output of a standard logic circuit. The MOSFET is a majority carrier device and any increase in temperature of the device affects the mobility of the majority carriers, which results in increase of resistivity of the semiconductor. From this, it is clear that MOSFETs are more immune to the thermal runaway effects and second breakdown phenomena experienced in BJTs. Figure 5.15(b) shows typical I_D versus V_{GS} characteristics at several temperatures. From the characteristics curve, for the given gate-to-source voltage at high current level, the current actually decreases with increase in temperature.

Compared to BJT, typical MOSFET power-handling level is much less. This disadvantage of a MOSFET is compensated by changing the construction mode from planar structure to a vertical one. So, power MOSFETs have different structures comparing to lateral MOSFETs by having a double diffused or vertical diffused process called DMOS or VMOS respectively.

5.7 DMOS

DMOS is an FET structure created specifically for high power applications and it is a planar transistor whose name is derived from the double-diffusion process used to construct it. DMOS is also used in switching applications with high-voltage and high-frequency behaviour, like inkjet printhead power supplies and automobile control electronics.

The cross-sectional view of a DMOS structure is shown in Fig. 5.16. The *P*-substrate region and the N^+ source contact are diffused through a common window defined by the edge of the gate. The *P*-substrate region is diffused deeper than the N^+ source. The surface channel length is defined as the lateral diffusion distance between the *P*-substrate and the N^+ source.

Electrons outside the source terminal flow laterally through the inversion layer under the gate to the *N*-drift region. Then, electrons flow vertically through the *N*-drift region to the drain terminal. The conventional current direction is from the drain to the source. The most important characteristics of DMOS device is their breakdown voltage and on-resistance. DMOS is similar to a BJT, due to the high-voltage and high-frequency characteristics. A lightly doped drift region between the drain contact and the channel region helps to ensure a very high breakdown voltage. Moreover, the *N*-drift region must be moderately doped so that the drain breakdown voltage is sufficiently large. The thickness of the *N*-drift region should be as small as possible to minimize drain resistance.

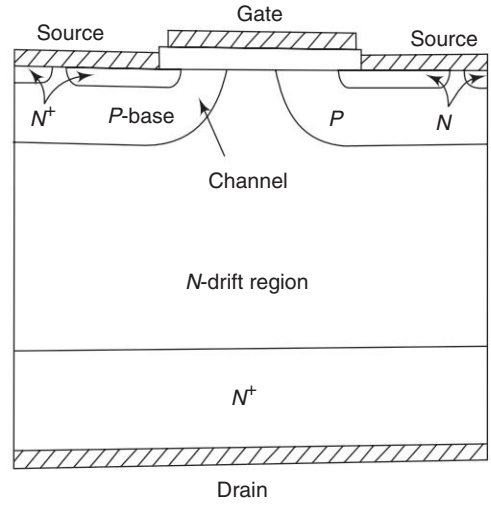


Fig. 5.16 *Cross section of the DMOS structure*

5.8 VMOS

Elements of the planar MOSFET are present in the vertical metal-oxide-silicon FET (VMOS) as shown in Fig. 5.17. The terminals of the device are connected to the metallic surface. The SiO_2 layer is placed between the gate and the *P*-type region and between the drain and source for the growth of the induced *N*-channel (enhancement-mode operation). The term *vertical* in VMOS is because of the fact that the channel is formed in the vertical direction rather than horizontal direction in the planar device. Moreover, the channel has the appearance of a "V" cut in the semiconductor base, which is also an important characteristic of the device. The construction of VMOS is simple by leaving out some of the transition levels of doping.

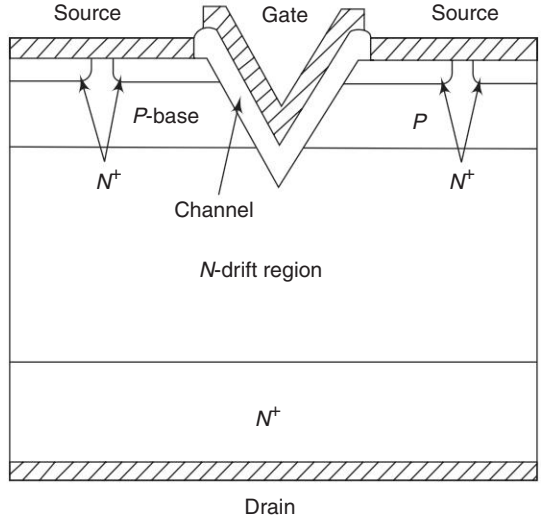


Fig. 5.17 *VMOS structure*

The *N*-channel is induced or enhanced in the narrow *P*-type region of the device if a positive voltage is applied to the drain, negative voltage to the source and 0 V or same positive voltage level to the gate. The vertical height of the *P*-region defines the length of the channel and this length on a horizontal plane is limited to 1 μm to 2 μm. Diffusion layers such as *P*-region of the device can be controlled to small fraction of μm.

Resistance levels and the power dissipation levels of the device at operating current will be reduced because of reduced channel length. Also, the contact area between the channel and the N^+ region is much increased by the vertical mode construction, which contributes to a further reduction in the resistance level and increased area between doping layers for current flow. Two conduction paths exist between drain and source. This conduction path further contributes to a higher current rating. The final result is that VMOS is a device with drain currents that can reach the ampere levels with power levels exceeding low. The VMOS FETs have reduced channel resistance levels, higher current rating and higher power rating when compared to planar MOSFET. Due to its high current-handling capability, VMOS transistors are useful in power amplifier applications.

Another important characteristic of vertical construction in VMOS FET is to have positive temperature coefficient which overcomes the possibility of thermal runaway. The resistance level of a device increases with increase in temperature of the device because of surrounding medium and current. This causes a reduction in drain current of the device, whereas for conventional devices, the drain current will increase. Negative temperature coefficient results in decreased levels of resistance with increase in temperature, which increases the current level, which in turn results in temperature stability and thermal runaway.

The reduced charge storage level in VMOS results in faster switching time when compared to conventional planar construction. The switching time of VMOS device is less than one-half that encountered in conventional BJT transistors.

5.9 JFET CONSTRUCTION

It consists of an *N*-type bar which is made of silicon. Ohmic contacts (terminals), made at the two ends of the bar, are called source and drain.

- **Source (*S*)** This terminal is connected to the negative pole of the battery. Electrons which are the majority carriers in the *N*-type bar enter the bar through this terminal.

- **Drain (*D*)** This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

- **Gate (*G*)** Heavily doped *P*-type silicon is diffused on both sides of the *N*-type silicon bar by which *PN* junctions are formed. These layers are joined together and called the gate *G*.

- **Channel** The region *BC* of the *N*-type bar between the depletion region is called the channel. Majority carriers move from the source to drain when a potential difference V_{DS} is applied between the source and drain.

5.10 OPERATION AND CHARACTERISTICS OF JFET

➤ ***When V_{GS} = 0 and V_{DS} = 0*** When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions around the *PN* junction is uniform as shown in Fig. 5.18.

➤ ***When V_{DS} = 0 and V_{GS} is Decreased from Zero*** In this case, the *PN* junctions are reverse biased and, hence, the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse-bias voltage across the *PN* junction is increased and, hence, the thickness of the depletion region in the channel also increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cut-off. The value of V_{GS} which is required to cut off the channel is called the cut off voltage V_C.

➤ ***When V_{GS} = 0 and V_{DS} is Increased from Zero*** Drain is positive with respect to the source with $V_{GS} = 0$. Now the majority carriers (electrons) flow through the *N*-channel from source to drain. Therefore, the conventional current I_D flows from drain to source. The magnitude of the current will depend upon the following factors:

1. The number of majority carriers (electrons) available in the channel, i.e., the conductivity of the channel.
2. The length *L* of the channel.
3. The cross-sectional area *A* of the channel at *B*.
4. The magnitude of the applied voltage V_{DS}. Thus, the channel acts as a resistor of resistance *R* given by

$$R = \frac{\rho L}{A} \qquad (5.11)$$

$$I_D = \frac{V_{DS}}{R} = \frac{AV_{DS}}{\rho L} \qquad (5.12)$$

where ρ is the resistivity of the channel. Because of the resistance of the channel and the applied voltage V_{DS}, there is a gradual increase of positive potential along the channel from source to drain. Thus, the reverse voltage across the *PN* junctions increases and hence the thickness of the depletion regions also increases. Therefore, the channel is wedge-shaped as shown in Fig. 5.19.

As V_{DS} is increased, the cross-sectional area of the channel will be reduced. At a certain value V_P of V_{DS}, the cross-sectional area at *B* becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off voltage.

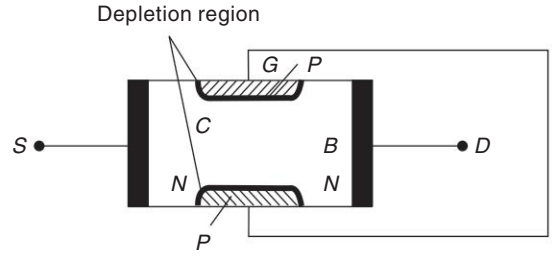


Fig. 5.18 *JFET construction*

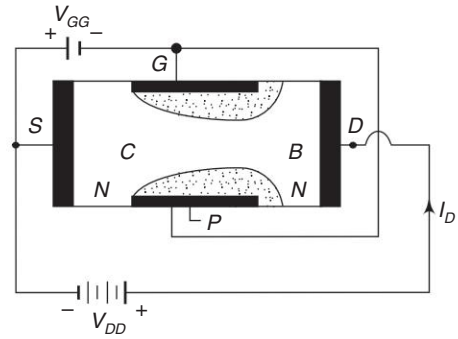


Fig. 5.19 *JFET under applied bias*

As a result of the decreasing cross section of the channel with the increase of V_{DS}, the following results are obtained.

(i) As V_{DS} is increased from zero, I_D increases along OP, and the rate of increase of I_D with V_{DS} decreases as shown in Fig. 5.20. The region from $V_{DS} = 0$ V to $V_{DS} = V_P$ is called the ohmic region. In the ohmic region, the drain-to-source resistance $\frac{V_{DS}}{I_D}$ is related to the gate voltage V_{GS}, in an almost linear manner. This is useful as a Voltage Variable Resistor (VVR) or Voltage Dependent Resistor (VDR).

(ii) When $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off or saturation region increases. Hence, there is no further increase of I_D.

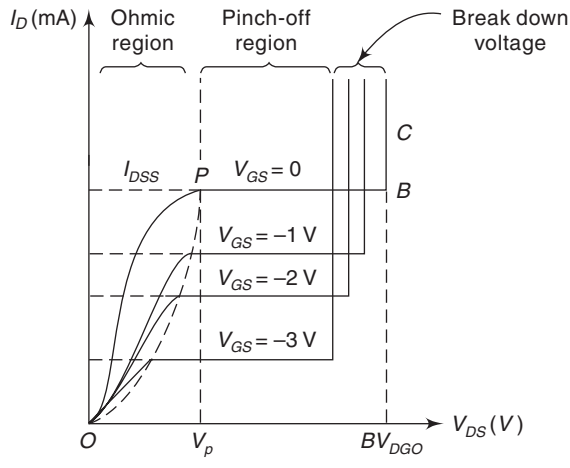


Fig. 5.20 *Drain characteristics*

(iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by BV_{DGO}. The variation of I_D with V_{DS} when $V_{GS} = 0$ is shown in Fig. 5.20 by the curve $OPBC$.

▪ **When V_{GS} is Negative and V_{DS} is Increased** When the gate is maintained at a negative voltage less than the negative cut-off voltage, the reverse voltage across the junction is further increased. Hence, for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for $V_{GS} = 0$, but the values of V_P and BV_{DGO} are lower, as shown in Fig. 5.20.

From the curves, it is seen that above the pinch-off voltage, at a constant value of V_{DS}, I_D increases with an increase of V_{GS}. Hence, a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

It can be seen from the curve that for voltage $V_{DS} = V_P$, the drain current is not reduced to zero. If the drain current is to be reduced to zero, then the ohmic voltage drop along the channel should also be reduced to zero. Further, the reverse biasing to the gate-source PN junction essential for pinching off the channel would also be absent.

The drain current I_D is controlled by the electric field that extends into the channel due to reverse-biased voltage applied to the gate; hence, this device has been given the name *Field Effect Transistor*.

In a bar of P-type semiconductor, the gate is formed due to N-type semiconductor. The working of the P-channel JFET will be similar to that of N-channel JFET with proper alterations in the biasing circuits; in this case, holes will be the current carriers instead of electrons. The circuit symbols for N-channel and P-channel JFETs are shown in Fig. 5.21. It should be noted that the direction of the arrow points in the direction of conventional current which would flow into the gate if the PN junction was forward biased.

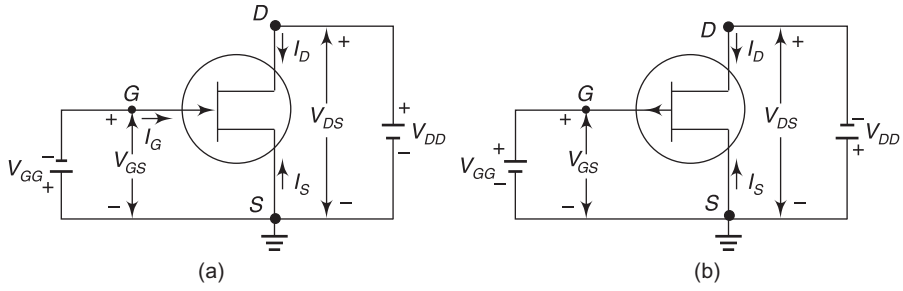


Fig. 5.21 *Circuit symbols for (a) N-channel JFET and (b) P-channel JFET*

5.11 JFET PARAMETERS

In a JFET, the drain current I_D depends upon the drain voltage V_{DS} and the gate voltage V_{GS}. Any one of these variables may be fixed and the relation between the other two are determined. These relations are determined by the three parameters which are defined below.

➤ ***Mutual Conductance or Transconductance, g_m*** It is the slope of the transfer characteristic curves, and is defined by

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} \text{ held constant}$$

It is the ratio of a small change in the drain current to the corresponding small change in the gate voltage at a constant drain voltage. The change in I_D and V_{GS} should be taken on the straight part of the transfer characteristics. It has the unit of conductance in mho.

➤ ***Drain Resistance, r_d*** It is the reciprocal of the slope of the drain characteristics and is defined by

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}, V_{GS} \text{ held constant}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the drain current at a constant gate voltage. It has the unit of resistance in ohms.

The drain resistance at $V_{GS} = 0$ V, i.e., when the depletion regions of the channel are absent, is called as *drain-source ON resistance,* represented as R_{DS} or $R_{DS(ON)}$.

The reciprocal of r_d is called the drain conductance. It is denoted by g_d or g_{ds}.

➤ ***Amplification Factor, μ*** It is defined by

$$\mu = \left(\frac{\partial V_{DS}}{\partial V_{GS}}\right) I_D = -\frac{\Delta V_{DS}}{\Delta V_{GS}}, I_D \text{ held constant}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current. Here, the negative sign shows that when V_{GS} is increased, V_{DS} must be decreased for I_D to remain constant.

➤ ***Relationship among FET Parameters*** As I_D depends on V_{DS} and V_{GS}, the functional equation can be expressed as

$$I_D = f(V_{DS}, V_{GS})$$

If the drain voltage is changed by a small amount from V_{DS} to $(V_{DS} + \Delta V_{DS})$ and the gate voltage is changed by a small amount from V_{GS} to $(V_{GS} + \Delta V_{GS})$ then the corresponding small change in I_D may be obtained by applying Taylor's theorem with neglecting higher order terms. Thus, the small change ΔI_D is given by

$$\Delta I_D = \left(\frac{\Delta I_D}{\Delta V_{DS}}\right)_{V_{GS}} \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS}$$

Dividing both the sides of this equation by ΔV_{GS}, we obtain

$$\frac{\partial I_D}{\partial V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D is constant, then $\dfrac{\Delta I_D}{\Delta V_{GS}} = 0$

Therefore, we have

$$0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

Substituting the values of the partial differential coefficients, we get

$$0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m$$

Hence, $$\mu = g_m r_d$$

Therefore, amplification factor (μ) is the product of drain resistance (r_d) and transconductance (g_m).

➤ ***Power Dissipation, P_D*** The FET's continuous power dissipation, P_D, is the product of I_D and V_{DS}.

➤ ***Pinch-off Voltage, V_P*** A single-ended-geometry junction FET is shown in Fig. 5.22 in which the diffusion is done from one side only. The substrate is of *P*-type material which is epitaxially grown on an *N*-type channel. A *P*-type gate is then diffused into the *N*-type channel. The substrate functions as a second gate which is of relatively low-resistivity material. The diffused gate is also of very low-resistivity material, allowing the depletion region to spread mostly into the *N*-type channel. A slab of *N*-type semiconductor is sandwiched between two layers of *P*-type material forming two *PN* junction in this device.

The gate-reverse voltage that removes all the free charge from the channel is called the pinch-off voltage V_P. We consider that the *P*-type region is doped with N_A acceptor atoms, the *N*-type region is doped with N_D donor atoms and the junction formed is abrupt.

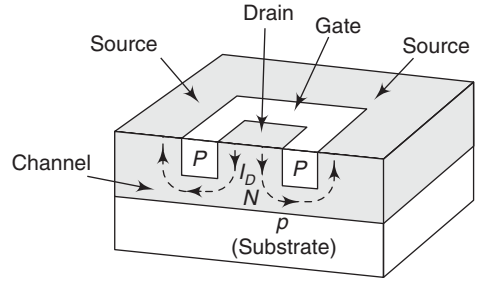


Fig. 5.22 *Single-ended-geometry junction FET*

Moreover, if the acceptor impurity density is assumed to be much larger than the donor density, then the depletion region width in the *P*-region will be much smaller than the depletion width of the *N*-region, i.e., $N_A >> N_D$, then $W_P << W_N$ and $W_P = W$. We know that, the relationship between potential and charge density is given by

$$\frac{d^2V}{dx^2} = \frac{-qN_D}{\varepsilon}$$

Integrating the above equation subject to boundary conditions, we get

$$\frac{dV}{dx} = \frac{-qN_D}{\varepsilon}(x - W)$$

Integrating again, we get

$$V = \frac{-qN_D}{2\varepsilon}(x^2 - 2Wx)$$

At $x = W$, $V = V_B$ which is the junction or barrier potential. Thus,

$$V_B = \frac{qN_D W^2}{2\varepsilon}$$

As the barrier potential represents a reverse voltage, it is lowered by an applied forward voltage $V(x)$ at x and it is expressed as $V_B = V_P - V(x)$. Now, the space-charge width, $W_n(x) = W(x)$ at a distance x along the channel in Fig. 5.23 becomes

$$W(x) = a - h(x) = \left\{\frac{2\varepsilon}{qN_D}[V_0 - V(x)]\right\}^{\frac{1}{2}}$$

where ε is the dielectric constant of channel material, q is the magnitude of electronic charge, V_0 is the junction contact potential at x, $V(x)$ is the applied potential across space-charge region at x and is a negative value for an applied reverse bias, a is the metallurgical channel thickness between the substrate and P^+ gate region, $a - h(x)$ is the penetration $W(x)$ of depletion region into channel at a point x along channel as shown in Fig. 5.23 and W_{PO} is the depletion region width at pinch-off.

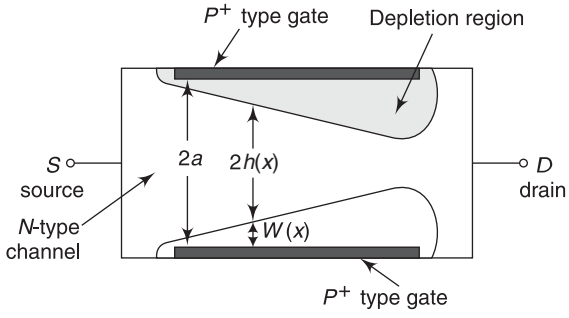


Fig. 5.23 *Detailed structure of N-channel JFET*

If the drain current is zero, $h(x)$ and $V(x)$ are independent of x and hence $h(x) = h$. If we substitute $h(x) = h = 0$ in the previous equation and solve for V with the assumption that $|V_0| << |V|$, the pinch-off voltage V_P can be obtained as

$$|V_P| = \frac{qN_D}{2\varepsilon}a^2$$

Here, at pinch-off, the depletion width $W_{PO} = a$ when $|V_P| = |V_{GS}|$ and hence,

$$W_{PO} = \left(\frac{2\varepsilon}{qN_D}V_{GS}\right)^{\frac{1}{2}}$$

To study the effect of V_{GS}, given $V_{GS} = V_0 - V(x)$ in the space charge width equation, we get

$$a - h = \left\{ \frac{2\varepsilon}{qN_D} V_{GS} \right\}^{\frac{1}{2}}$$

Substituting $V_p = \frac{qN_D}{2\varepsilon} a^2$ in the above equation, we get

$$a - h = \left[\frac{a^2}{V_P} V_{GS} \right]^{\frac{1}{2}}$$

i.e., $$\frac{a - h}{a} = \left(\frac{V_{GS}}{V_P} \right)^{\frac{1}{2}}$$

Therefore, $$\left(1 - \frac{h}{a}\right)^2 = \frac{V_{GS}}{V_P}$$

Hence, the gate-source voltage is

$$V_{GS} = \left(1 - \frac{h}{a}\right)^2 V_P$$

For a reverse-biased P^+N junction, V_{GS} must be a negative voltage across the gate junction and is independent of distance along the channel if $I_D = 0$.

EXAMPLE 5.1

When a reverse gate voltage of 12 V is applied to JFET, the gate current is 1 nA. Determine the resistance between gate and source.

Solution

Given $V_{GS} = 12$ V, $I_G = 10^{-9}$ A.

Therefore, gate-to-source resistance = $\frac{V_{GS}}{I_G} = \frac{12}{10^{-9}} = 12{,}000\ \text{M}\Omega$

EXAMPLE 5.2

When the reverse gate voltage of JFET changes from 4.0 to 3.9 V, the drain current changes from 1.3 to 1.6 mA. Find the value of transconductance.

Solution

$$\Delta V_{GS} = 4.0 - 3.9 = 0.1 \text{ V}$$

$$\Delta I_D = 1.6 - 1.3 = 0.3 \text{ mA}$$

Therefore, transconductance, $g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3 \times 10^{-3}}{0.1} = 3 \text{ m mho}$

5.11.1 Expression for Saturation Drain Current

For the transfer characteristics, V_{DS} is maintained constant at a suitable value greater than the pinch-off voltage V_P. The gate voltage V_{GS} is decreased from zero till I_D is reduced to zero. The transfer characteristics I_D versus V_{GS} is shown in Fig. 5.24. The shape of the transfer characteristic is very nearly a parabola. It is found that the characteristic is approximately represented by the parabola,

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{5.13}$$

where I_{DS} is the saturation drain current, I_{DSS} is the value of I_{DS} when $V_{GS} = 0$, and V_P is the pinch-off voltage.

Differentiating Eq. (5.13) with respect to V_{GS}, we can obtain an expression for g_m.

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} \times 2\left(1 - \frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right)$$

We know that, $g_m = \dfrac{\delta I_{DS}}{\delta V_{GS}}, V_{DS}$ is constant.

Therefore, $$g_m = \frac{-2 I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{5.14}$$

Now from Eq. (5.13), we have

$$\left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}} \tag{5.15}$$

Substituting this value in Eq. (5.14), we get

$$g_m = \frac{-2\sqrt{I_{DS} I_{DSS}}}{V_P}$$

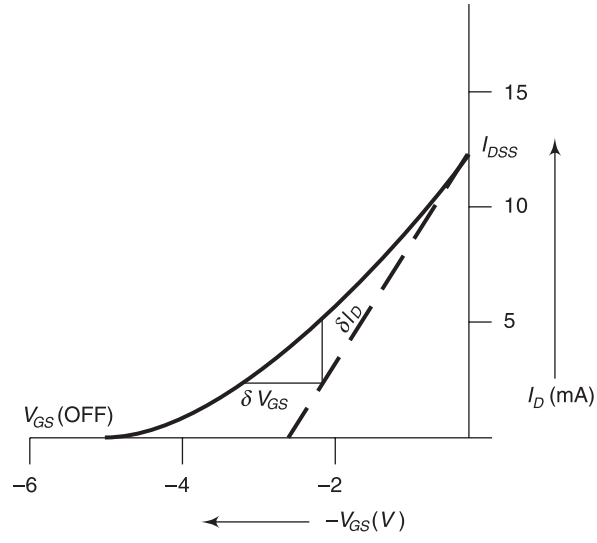


Fig. 5.24 *Transfer characteristics of JFET*

Suppose $g_m = g_{mo}$, when $V_{GS} = 0$, then from Eq. (5.15),

$$g_{mo} = -\frac{2 I_{DSS}}{V_P} \tag{5.16}$$

Therefore, from Eqs (5.14) and (5.16),

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{5.17}$$

Equation (5.15) shows that g_m varies as the square root of the saturation drain current I_{DS}, and Eq. (5.17) shows that g_m decreases linearly with increase of V_{GS}.

5.11.2 Slope of the Transfer Characteristic at I_{DSS}

From Eq. (5.17), we have

$$g_m = \frac{-2\sqrt{I_{DS} I_{DSS}}}{V_P}$$

or $$\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{2\sqrt{I_{DSS} I_{DSS}}}{V_P}$$

Substituting $I_{DS} = I_{DSS}$,

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2 I_{DS}}{V_P} = \frac{I_{DSS}}{\frac{-V_P}{2}}$$

This equation shows that the tangent to the curve at $I_{DS} = I_{DSS}$, $V_{GS} = 0$, will have an intercept at $\frac{-V_P}{2}$ on the axis of V_{GS} as shown in Fig. 5.22. Therefore, the value of V_P can be found by drawing the tangent at $I_{DS} = I_{DSS}$, $V_{GS} = 0$.

The gate-source cut-off voltage, $V_{GS(\text{off})}$, on the transfer characteristic is equal to the pinch-off voltage, V_P, on the drain characteristics, i.e., $V_P = |V_{GS(\text{off})}|$.

Therefore, $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right]^2$$

5.11.3 Biasing for Zero Current Drift

Figure 5.25 shows the transfer characteristics of *N* channel JFET for different values of temperature. Here, the drain current varies due to change in temperature. The two factors which make drain current to change with temperature are the mobility of majority carriers and the depletion region width.

The mobility of majority carriers decreases with increase in temperature. As the temperature increases, the lattice ions vibrate more vigorously and hence, the carriers cannot move freely in the crystalline structure. For the given gate-source voltage V_{GS}, their velocity is decreased and this reduces the drain current. The reduction in I_D is 0.7 percent for 1°C increase in the temperature.

The width of the depletion region (increase in channel width) decreases with increase in temperature. This allows I_D to increase and the increase in I_D is equivalent to a change of 2.2 mV/1°C in $|V_{GS}|$. This is a similar phenomenon to the change of $|V_{BE}|$ of 2.5 mV/°C in bipolar transistor.

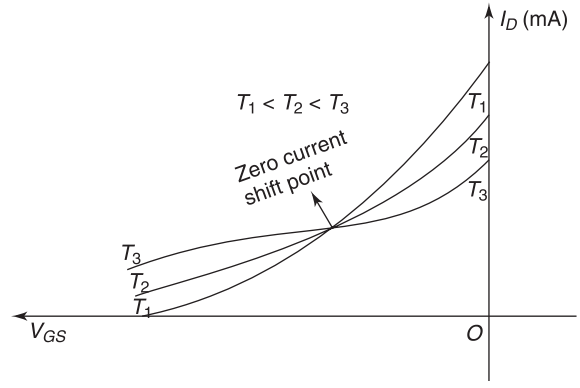


Fig. 5.25 *Transfer characteristics for an N channel FET as a function of temperature T*

Hence, it is required to design a biasing circuit which compensates for these two factors, so that there is no change of drain current with temperature. Such a biasing is called Biasing for zero current drift.

Due to the change in I_D and change in V_{GS} for 1°C, the condition for zero current drift can be obtained as

$$0.007\left|I_D\right| = 0.0022\, g_m$$

i.e., $$\frac{|I_D|}{g_m} = 0.314 \text{ V}$$

We know that, $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$ and $g_m = \frac{-2I_{DSS}}{V_P}\left[1-\frac{V_{GS}}{V_P}\right]$.

Hence, $$\frac{|I_D|}{g_m} = \frac{I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2}{-\frac{2I_{DSS}}{V_P}\left[1-\frac{V_{GS}}{V_P}\right]} = \frac{|V_P|-|V_{GS}|}{-2} = 0.314 \text{ V}$$

Therefore, $$|V_P|-|V_{GS}| = -0.628\text{V} \approx -0.63 \text{ V}$$

From the above equation, it is seen that, if the value of V_P is known, the value of V_{GS} for zero drift current can be obtained.

When V_{GS} is adjusted for zero drift current, the drain current I_D and the transconductance g_m are given by

$$I_D = I_{DSS}\left[1-\frac{V_P+0.63}{V_P}\right]^2 = I_{DSS}\left[\frac{0.63}{V_P}\right]^2$$

and $$g_m = g_{mo}\left[1-\frac{V_P+0.63}{V_P}\right] = g_{mo}\left(\frac{0.63}{|V_P|}\right)$$

EXAMPLE 5.3

A FET has a drain current of 4 mA. If I_{DSS} = 8 mA and $V_{GS(\text{off})} = -6$ V. Find the values of V_{GS} and V_P.

Solution

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(\text{off})}}\right]^2$$

$$4 = 8\left[1+\frac{V_{GS}}{6}\right]^2$$

$$1+\frac{V_{GS}}{6} = \sqrt{\frac{4}{8}} = \frac{1}{\sqrt{2}} = 0.707$$

Therefore, $$V_{GS} = -1.76 \text{ V}$$

$$V_P = |V_{GS(\text{off})}| = 6\text{V}$$

EXAMPLE 5.4

An *N*-channel JFET has I_{DSS} = 8 mA and V_P = – 5 V. Determine the minimum value of V_{DS} for pinch-off region and the drain current I_{DS}, for V_{GS} = – 2V in the pinch-off region.

Solution The minimum value of V_{DS} for pinch-off to occur for $V_{GS} = -2$ V is

$$V_{DS\,\min} = V_{GS} - V_P = -2 - (-5) = 3 \text{ V}$$

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 8 \times 10^{-3}\,[1 - (-2)/(-5)]^2 = 2.88 \text{ mA}$$

EXAMPLE 5.5

Determine the pinch-off voltage for an *N*-channel silicon FET with a channel width of 5.6×10^{-4} cm and a donor concentration of 10^{15} /cm^3. Given, the dielectric constant of Si is 12.

Solution

Given $N_D = 10^{15}/\text{cm}^3 = 10^{21}/\text{m}^3$, $\varepsilon = \varepsilon_r\,\varepsilon_o = 12\,\varepsilon_o$.

$a = 5.6 \times 10^{-4}$ cm $= 5.6 \times 10^{-6}$ m

The pinch-off voltage, $|V_P| = \dfrac{qN_D}{2\varepsilon}a^2$

where $\varepsilon =$ dielectric constant of channel material (Si) $= \varepsilon_r\,\varepsilon_o = 12\,\varepsilon_o$

$q =$ magnitude of electronic charge

$a =$ in metres and N_D is in electrons/m^3

$$|V_P| = \frac{1.602 \times 10^{-19} \times 10^{21}}{2 \times 12 \times 8.854 \times 10^{-12}} \times (5.6 \times 10^{-6})^2 = 23.6 \text{ V}$$

EXAMPLE 5.6

For a *P*-channel silicon FET, with an effective channel width, $a = 2 \times 10^{-4}$ cm and channel resistively $\rho = 20$ Ω-cm, find the pinch-off voltage.

Solution We know that the pinch-off voltage for *P*-channel FET, $V_P = \dfrac{qN_A}{2\varepsilon} \times a^2$.

For silicon, $\varepsilon = 12\varepsilon_o$ and $\mu_p = 500$ cm^2/V-s

$$\sigma = \frac{1}{\rho} = p\mu_p \times q = N_A\mu_p \times q$$

i.e., $$qN_A = \frac{1}{\rho\mu_p} = \frac{1}{20 \times 500} = 1 \times 10^{-4}$$

Therefore, $$V_P = \frac{qN_A}{2\varepsilon} \times a^2 = \frac{1 \times 10^{-4}}{2 \times 12 \times 8.854 \times 10^{-12}} \times (2 \times 10^{-4})^2 = 1.89 \text{ V}$$

5.11.4 Comparison of JFET and BJT

1. FET operation depends only on the flow of majority carriers—holes for *P*-channel FETs and electrons for *N*-channel FETs. Therefore, they are called *unipolar devices*. Bipolar transistor (BJT) operation depends on both minority and majority current carriers.

2. As FET has no junctions and the conduction is through an *N*-type or *P*-type semiconductor material, FET is less noisy than BJT.
3. As the input circuit of FET is reverse biased, FET exhibits a much higher input impedance (in the order of 100 MΩ) and lower output impedance and there will be a high degree of isolation between input and output. So, FET can act as an excellent buffer amplifier but the BJT has low input impedance because its input circuit is forward biased.
4. FET is a voltage controlled device, i.e., voltage at the input terminal controls the output current, whereas BJT is a current controlled device, i.e., the input current controls the output current.
5. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
6. The performance of a BJT is degraded by neutron radiation because of the reduction in minority-carrier lifetime, whereas FETs can tolerate a much higher level of radiation since they do not rely on minority carriers for their operation.
7. The performance of an FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature co-efficient at high current levels which leads to thermal breakdown.
8. Since the FET does not suffer from minority carrier storage effects, it has higher switching speeds and cut-off frequencies. BJT suffers from minority carrier storage effects and, therefore, has lower switching speed and cut-off frequencies.
9. FET amplifiers have low gain-bandwidth product due to the junction capacitive effects and produce more signal distortion except for small-signal operation.
10. BJTs are cheaper to produce than FETs.

5.11.5 Applications of JFET

1. FETs are used as a buffer in measuring instruments and receivers since they have high input impedance and low output impedance.
2. FETs are used in RF amplifiers in FM tuners, and in communication equipment for its low noise level.
3. Since the input capacitance is low, FETs are used in cascade amplifiers in measuring and test equipments.
4. Since the device is voltage controlled, FETs are used as a voltage variable resistors in operational amplifiers and tone controls.
5. FETs are used in mixer circuits in FM and TV receivers, and in communication equipment because their intermodulation distortion is low.
6. They are used in oscillator circuits because frequency drift is low.
7. As the coupling capacitor is small, FETs are used in low-frequency amplifiers in hearing aids and in inductive transducers.
8. FETs are used in digital circuits in computers, LSD, and memory circuits because of their small size.

5.12 MOSFET – TYPES AND CONSTRUCTION

MOSFET is the common term for the Insulated Gate Field Effect Transistor (IGFET). There are two basic forms of MOSFET: (i) Enhancement MOSFET, and (ii) Depletion MOSFET.

➤ ***Principle*** By applying a transverse electric field across an insulator deposited on the semiconducting material, the thickness and, hence, the resistance of a conducting channel of a semiconducting material can be controlled.

In a depletion MOSFET, the controlling electric field reduces the number of majority carriers available for conduction, whereas in the enhancement MOSFET, application of electric field causes an increase in the majority carrier density in the conducting regions of the transistor.

5.13 ENHANCEMENT MOSFET

➤ ***Construction*** The construction of an *N*-channel enhancement MOSFET is shown in Fig. 5.26(a), and the circuit symbols for an *N*-channel and a *P*-channel enhancement MOSFET are shown in Figs 5.26(b) and (c), respectively. As there is no continuous channel in an enhancement MOSFET, this condition is represented by the broken line in the symbols.

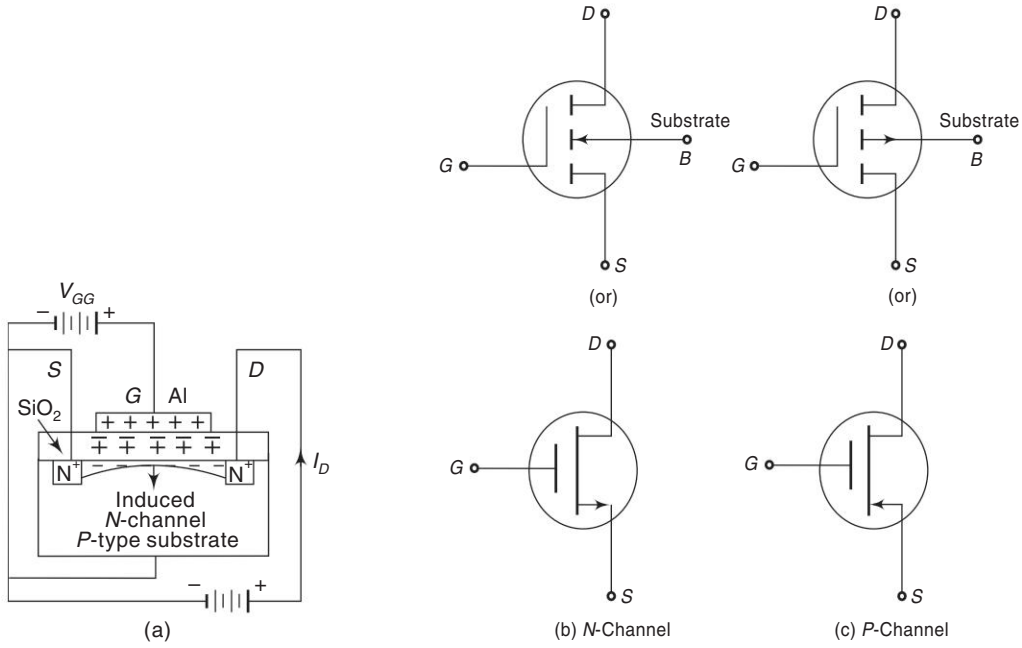


Fig. 5.26 *(a) N-channel enhancement MOSFET, (b) and (c) Circuit symbols for enhancement MOSFET*

Two highly doped N^+ regions are diffused in a lightly doped substrate of *P*-type silicon substrate. One N^+ region is called the source *S* and the other one is called the drain *D*. They are separated by 1 mil (10^{-3} inch). A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with source and drain. Then a thin layer of metal aluminium is formed over the layer of SiO_2. This metal layer covers the entire channel region and it forms the gate *G*.

The metal area of the gate, in conjunction with the insulating oxide layer of SiO_2 and the semiconductor channel forms a parallel-plate capacitor. This device is called the insulated gate FET because of the insulating layer of SiO_2. This layer gives an extremely high input impedance for the MOSFET.

➤ ***Operation*** If the substrate is grounded and a positive voltage is applied at the gate, the positive charge on *G* induces an equal negative charge on the substrate side between the source and drain regions. Thus, an electric field is produced between the source and drain regions. The direction of the electric field is perpendicular to the plates of the capacitor through the oxide. The negative charge of electrons which are minority carriers in the *P*-type substrate forms an inversion layer. As the positive voltage on the gate increases, the induced negative charge in the semiconductor increases. Hence, the conductivity increases and current flows from source to drain through the induced channel. Thus, the drain current is enhanced by the positive gate voltage as shown in Fig. 5.27.

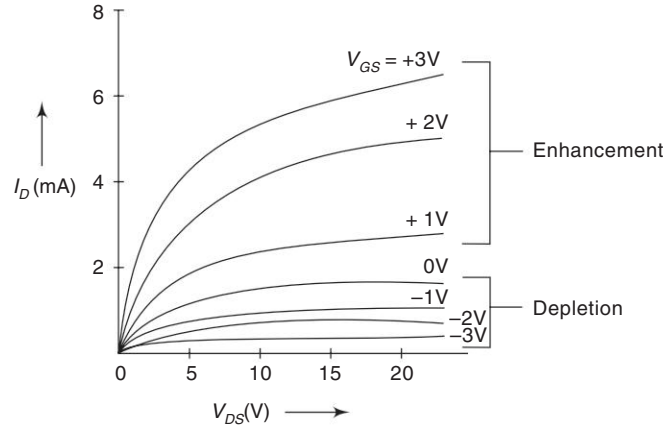


Fig. 5.27 *Volt-ampere characteristics of MOSFET*

5.14 DEPLETION MOSFET

The construction of an *N*-channel depletion MOSFET is shown in Fig. 5.28(a) where an *N*-channel is diffused between the source and drain to the basic structure of MOSFET. The circuit symbols for an *N*-channel and a *P*-channel depletion MOSFET are shown in Figs 5.28(b) and (c), respectively.

With V_{GS} = 0 and the drain *D* at a positive potential with respect to the source, the electrons (majority carriers) flow through the *N*-channel from *S* to *D*. Therefore, the conventional current I_D flows through the channel *D* to *S*. If the gate voltage is made negative, positive charge consisting of holes is induced in the channel through SiO_2 of the gate-channel capacitor. The introduction of the positive charge causes depletion of mobile electrons in the channel. Thus, a depletion region is produced in the channel. The shape of the depletion region depends on V_{GS} and V_{DS}. Hence, the channel will be wedge shaped as shown in Fig. 5.28(a). When V_{DS} is increased, I_D increases and it becomes practically constant at a certain value of V_{DS}, called the pinch-off voltage. The drain current I_D almost gets saturated beyond the pinch-off voltage.

Since the current in an FET is due to majority carriers (electrons for an *N*-type material), the induced positive charges make the channel less conductive, and I_D drops as V_{GS} is made negative.

The depletion MOSFET may also be operated in an enhancement mode. It is only necessary to apply a positive gate voltage so that negative charges are induced into the *N*-type channel. Hence, the conductivity of the channel increases and I_D increases. As the depletion MOSFET can be operated with bipolar input signals irrespective of doping of the channel, it is also called *dual-mode MOSFET*. The volt-ampere characteristics are indicated in Fig. 5.27.

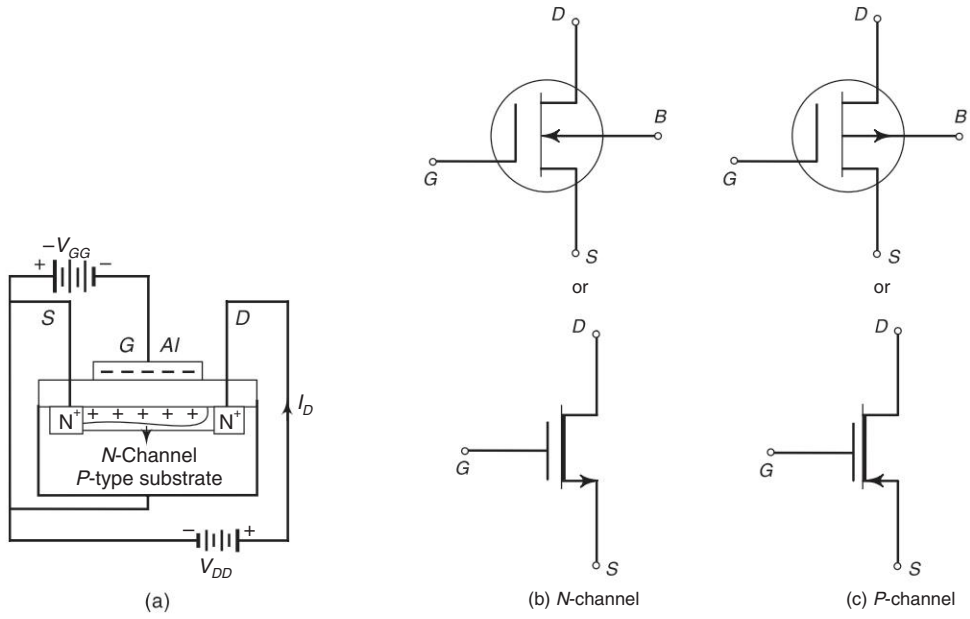


Fig. 5.28 *(a) N-channel depletion MOSFET, (b) and (c) Circuit symbols for depletion MOSFETs*

The curve of I_D versus V_{GS} for constant V_{DS} is called the transfer characteristics of the MOSFET and is shown in Fig. 5.29.

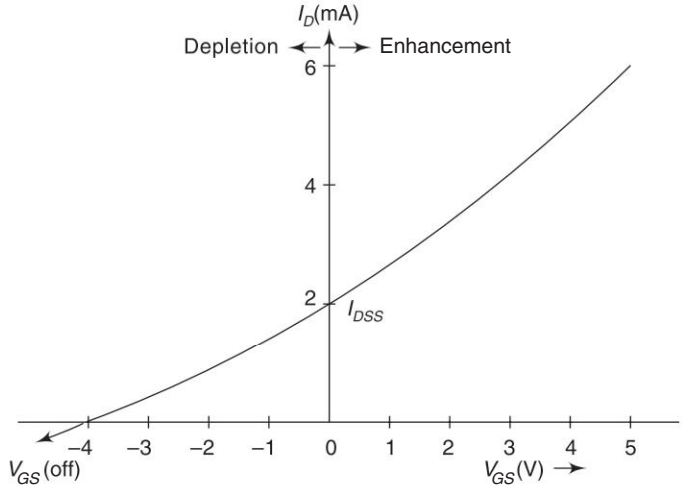


Fig. 5.29 *Transfer characteristics of MOSFET*

5.15 COMPARISON OF MOSFET WITH JFET

1. In enhancement and depletion types of MOSFETs, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel. In

the JFET, the transverse electric field across the reverse-biased *PN* junction controls the conductivity of the channel.

2. The gate-leakage current in a MOSFET is of the order of 10^{-12} A. Hence, the input resistance of a MOSFET is very high in the order of 10^{10} to 10^{15} Ω. The gate-leakage current of a JFET is of the order of 10^{-9} A and its input resistance is of the order of 10^{8} Ω.
3. The output characteristics of the JFET are flatter than those of the MOSFET and, hence, the drain resistance of a JFET (0.1 to 1 MΩ) is much higher than that of a MOSFET (1 to 50 kΩ).
4. JFETs are operated only in the depletion mode. The depletion-type MOSFET may be operated in both depletion and enhancement mode.
5. Comparing to JFET, MOSFETs are easier to fabricate.
6. A MOSFET is very susceptible to overload voltage and needs special handling during installation. It gets damaged easily if it is not properly handled.
7. A MOSFET has zero offset voltage. As it is a symmetrical device, the source and drain can be interchanged. These two properties are very useful in analog signal switching.
8. Special digital CMOS circuits are available which involve near-zero power dissipation and very low voltage and current requirements. This makes them most suitable for portable systems.

MOSFETs are widely used in digital VLSI circuits than JFETs because of their advantages.

5.16 COMPARISON OF *N*-CHANNEL WITH *P*-CHANNEL MOSFETs

1. The *P*-channel enhancement MOSFET is very popular because it is much easier and cheaper to produce than the *N*-channel device.
2. The hole mobility is nearly 2.5 times lower than the electron mobility. Thus, a *P*-channel MOSFET occupies a larger area than an *N*-channel MOSFET having the same I_D rating.
3. The drain resistance of *P*-channel MOSFET is three times higher than that for an identical *N*-channel MOSFET.
4. The *N*-channel MOSFET has the higher packing density which makes it faster in switching applications due to the smaller junction areas and lower inherent capacitances.
5. The *N*-channel MOSFET is smaller for the same complexity than *P*-channel device.
6. Due to the positively charged contaminants, the *N*-channel MOSFET may turn ON prematurely, whereas the *P*-channel device will not be affected.

5.17 LOW FREQUENCY MODEL OF FET

The cross section of an *N*-channel JFET is shown in Fig. 5.30, which includes the series resistances of source and drain terminal. The substrate used is a P^+ type Si substrate. The corresponding small-signal equivalent circuit for the JFET is shown in Fig. 5.31. The internal gate-source voltage is denoted by $V_{g's'}$ that controls the drain current. The gate-source diffusion resistance and junction capacitance are represented by parameters r_{gs} and C_{gs} respectively. The gate-source junction is reverse biased for depletion-mode devices and forward biased for enhancement-mode devices, so that normally r_{gs} is large. The parameters r_{gd} and C_{gd} are the gate-drain resistance and capacitance respectively. The resistance r_{ds} is the finite drain source resistance, which is a function of the channel-length modulation effect. The capacitance C_{ds} mainly a drain-source parasitic capacitance and C_s is the drain-substrate capacitance.

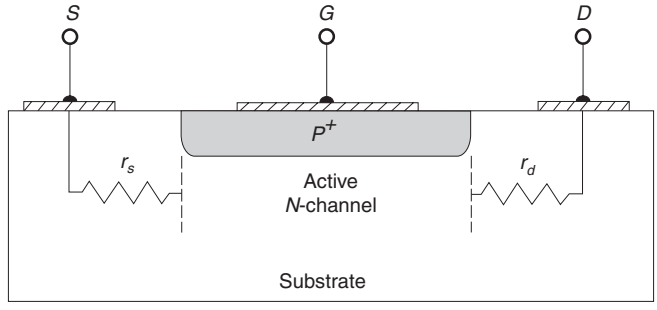


Fig. 5.30 *Cross section of JFET with source and drain series resistance*

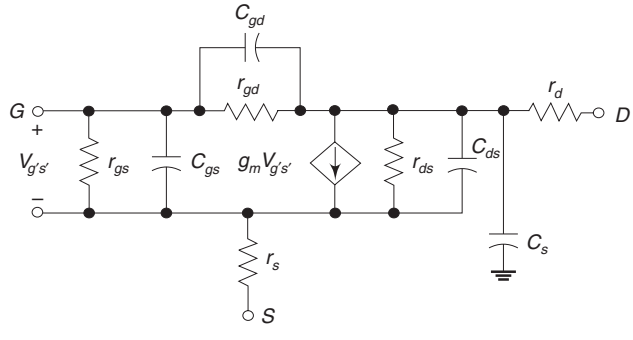


Fig. 5.31 *Small-signal equivalent circuit of JFET*

The ideal small-signal equivalent circuit at low frequency is shown in Fig. 5.32(a). All diffusion resistances are infinite, the series resistances are zero and the capacitances become open circuits. The small-signal drain current is given by

$$I_{ds} = g_m V_{gs}$$

which is a function of transconductance and input signal voltage. Figure 5.32(b) shows the equivalent circuit of JFET which includes the series source resistance. From Fig. 5.32(b), we know that,

$$I_{ds} = g_m V_{g's'}$$

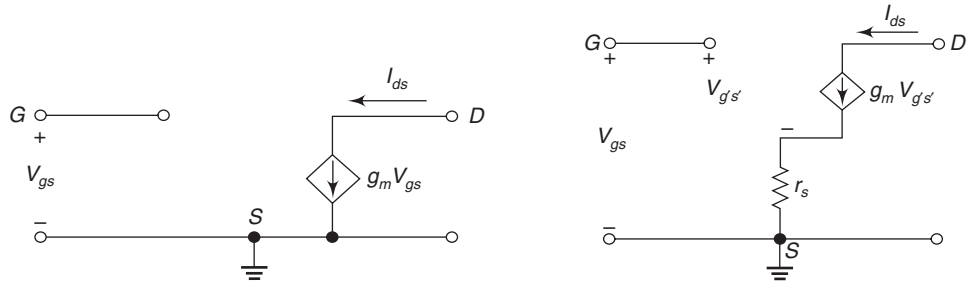


Fig. 5.32 *Small-signal equivalent circuit (a) without r_s, (b) with r_s*

The relation between V_{gs} and $V_{g's'}$ can be obtained from

$$V_{gs} = V_{g's'} + (g_m V_{g's'})\, r_s = (1 + g_m r_s) V_{g's'}$$

Then, the drain current can be written as

$$I_{ds} = \left(\frac{g_m}{1 + g_m r_s} \right) V_{gs} = g'_m V_{gs}$$

where g_m is the transconductance without r_s and g'_m is the transconductance with r_s. The effect of the source resistance is to reduce the effective transconductance or transistor gain. As g_m is a function of V_{gs}, g'_m will also be a function of V_{gs} as shown in Fig. 5.33.

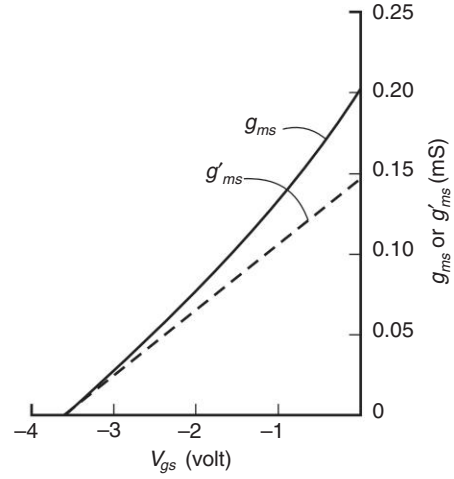


Fig. 5.33 *JFET transconductance versus V_{gs} (without r_s and with r_s)*

There are two frequency limitation factors in a JFET. The first is the channel transit time τ_t. For a channel length L of 1 μm and assuming the carriers are travelling at their saturation velocity cm/s, the transit time is of the order of

$$\tau_t = \frac{L}{v_s} = \frac{1 \times 10^{-4}}{1 \times 10^{7}} = 10\ ps$$

The channel transit time is, normally, not the limiting factor except in very high frequency devices.

The second frequency limitation factor is the capacitance charging time. Figure 5.34 is a simplified equivalent circuit at high frequency that includes the primary capacitances and ignores the diffusion resistances. The output current will be the short-circuit current. As the frequency of the input signal voltage V_{gs} increases, the impedance of C_{gd} and C_{gs} decreases and the current through C_{gd} will increase. For a constant $g_m V_{gs}$, the current I_{ds} will then decrease. The output current then becomes a function of frequency.

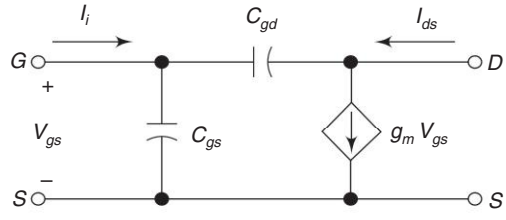


Fig. 5.34 *Small-signal equivalent circuit at high frequency including C_{gd} and C_{gs}*

5.18 FET AS AN AMPLIFIER

The small-signal models for the common source FET can be used for analyzing the three basic FET amplifier configurations: (i) Common source (CS), (ii) Common drain (CD) or *source-follower*, and (iii) Common gate (CG). The CS amplifier which provides good voltage amplification is most frequently used. The CD amplifier with high input impedance and near-unity voltage gain is used as a buffer amplifier and the CG amplifier is

used as a high-frequency amplifier. The small-signal current-source model for the FET in CS configuration is redrawn in Fig. 5.35(a) and the voltage-source model shown in Fig. 5.35(b) can be derived by finding the Thevenin's equivalent for the output part of Fig. 5.35(a). μ, r_d and g_m are the amplification factor, drain resistance, and mutual conductance of the FET.

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain with the added feature of high input impedance. They have low power consumption with a good frequency range, and minimal size and weight. The noise output level is low. This feature makes them very useful in the amplifier circuits meant for very small-signal amplifications. JFETs, depletion MOSFETs and enhancement MOSFETs are used in the design of amplifiers having comparable voltage gains. However, the depletion MOSFET circuit realizes much higher input impedance than the equivalent JFET configuration. Because of the high input impedance characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. The common-source configuration is the most popular one, providing an inverted and amplified signal. However, one also finds the common drain (source follower) circuits providing unity gain with no inversion and common gate circuits providing gain with no inversion. Due to very high input impedance, the input current is generally assumed to be negligible, and it is of the order of few microamperes and the current gain is an undefined quantity. Output impedance values are comparable for both the BJT and FET circuits

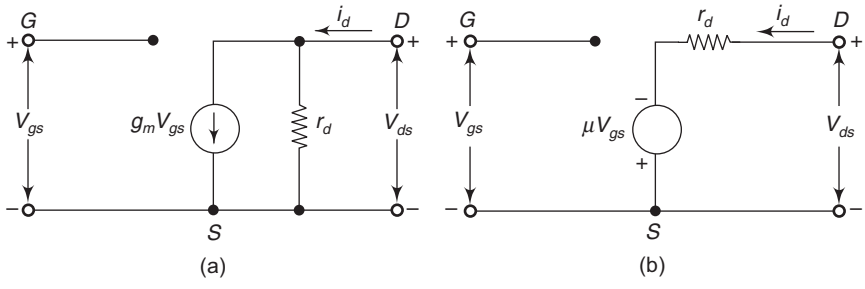


Fig. 5.35 *(a) Small-signal current-source model for FET in CS configuration*
(b) Voltage-source model for FET in CS configuration

5.18.1 Common-Source (CS) Amplifier

A simple common-source amplifier is shown in Fig. 5.36(a), and the associated small-signal equivalent circuit using the voltage-source model of FET is shown in Fig. 5.36(b).

➤ ***Voltage Gain*** Source resistor (R_s) is used to set the Q-point but is bypassed by C_S for mid-frequency operation. From the small-signal equivalent circuit, the output voltage,

$$V_o = \frac{-R_D}{R_D + r_d} \mu V_{gs} \tag{5.18}$$

where $V_{gs} = V_i$, the input voltage.

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d} \tag{5.19}$$

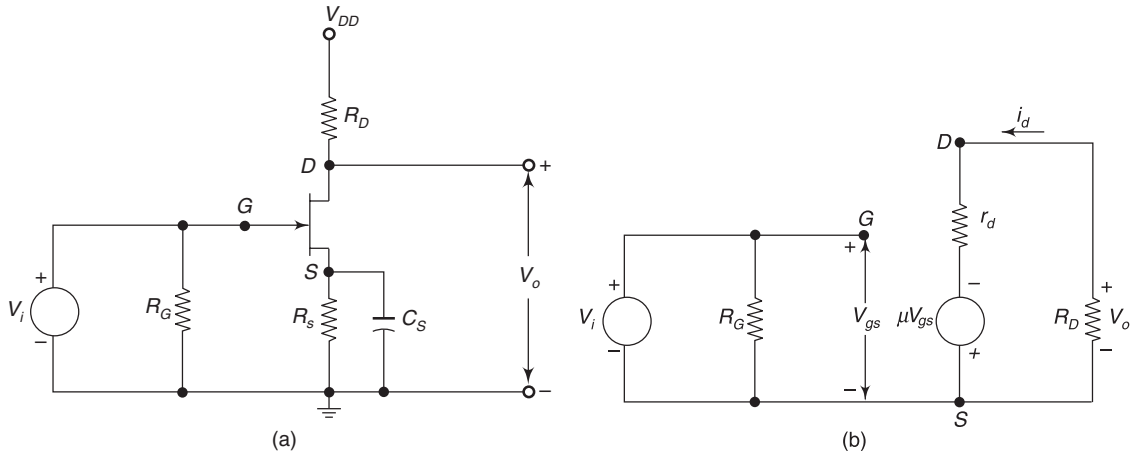


Fig. 5.36 *(a) Common source amplifier (b) Small-signal equivalent circuit of CS amplifier*

➤ ***Input Impedance*** From Fig. 5.36(b), the input impedance is given by

$$Z_i = R_G$$

For voltage divider bias as in *CE* amplifiers of BJT,

$$R_G = R_1 \parallel R_2$$

➤ ***Output Impedance*** Output impedance is the impedance measured at the output terminals with the input voltage $V_i = 0$.

From Fig. 5.36(b), when $V_i = 0$, $V_{gs} = 0$ and hence,

$$\mu V_{gs} = 0$$

Then the equivalent circuit for calculating output impedance is given in Fig. 5.36(c).

Output impedance $Z_o = r_d \parallel R_D$

Normally, r_d will be far greater than R_D.

Hence, $Z_o \approx R_D$

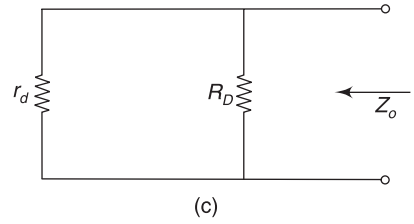


Fig. 5.36 *(c) Calculation of output impedance*

EXAMPLE 5.7

In the CS amplifier of Fig. 5.36(a), let $R_D = 5$ kΩ, $R_G = 10$ MΩ, μ = 50, and $r_d = 35$ kΩ. Evaluate the voltage gain A_V, input impedance Z_i, and output impedance Z_o.

Solution The voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d}$$

$$= \frac{-50 \times 5 \times 10^3}{5 \times 10^3 + 35 \times 10^3}$$

$$= \frac{-250 \times 10^3}{40 \times 10^3} = -6.25$$

The minus sign indicates a 180° phase shift between V_i and V_o.

Input impedance $Z_i = R_G = 10\ \text{M}\Omega$

Output impedance $Z_o \approx R_D = 5\ \text{k}\Omega$

EXAMPLE 5.8

A FET amplifier in the common-source configuration uses a load resistance of 500 kΩ. The ac drain resistance of the device is 100 kΩ and the transconductance is 0.8 mAV^{-1}. Calculate the voltage gain of the amplifier.

Solution

Given load resistance, $R_L = R_D = 500\ \text{k}\Omega$, $r_d = 100\ \Omega$, $g_m = 0.8\ \text{mAV}^{-1}$

The transconductance $\mu = g_m r_d = 0.8 \times 10^{-3} \times 100 \times 10^3 = 80$

The voltage gain, $$A_V = -\frac{\mu R_D}{R_D + r_d} = \frac{-80 \times 500 \times 10^3}{500 \times 10^3 + 100 \times 10^3} = -\frac{40 \times 10^6}{600 \times 10^3} = -66.67$$

5.18.2 Common-Drain (CD) Amplifier

A simple common-drain amplifier is shown in Fig. 5.37(a) and the associated small-signal equivalent circuit using the voltage-source model of FET is shown in Fig. 5.37(b). Since voltage V_{gd} is more easily determined than V_{gs}, the voltage source in the output circuit is expressed in terms of V_{gd} using Thevenin's theorem. The output voltage,

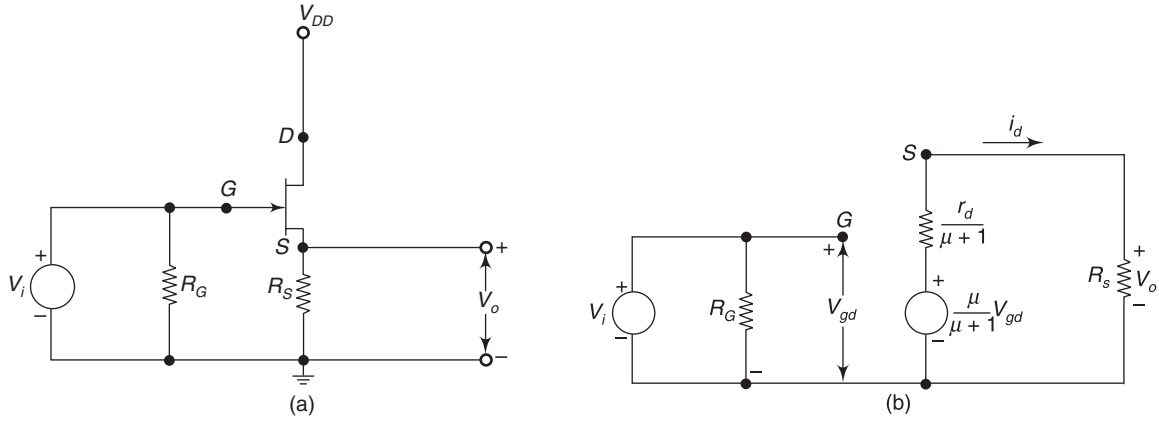


Fig. 5.37 *(a) Common drain amplifier (b) Small-signal equivalent circuit of a CD amplifier*

$$V_o = \frac{R_s}{R_s + \dfrac{r_d}{\mu + 1}} \times \frac{\mu}{\mu + 1} V_{gd} = \frac{\mu R_s V_{gd}}{(\mu + 1) R_s + r_d} \tag{5.20}$$

where $V_{gd} = V_i$, the input voltage.

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_s}{(\mu + 1) R_s + r_d} \tag{5.21}$$

➤ ***Input Impedance*** From Fig. 5.37(b), input impedance $Z_i = R_G$

➤ ***Output Impedance*** From Fig. 5.37(c), output impedance measured at the output terminals with input voltage $V_i = 0$ can be simply calculated from the following equivalent circuit.

As $V_i = 0$; $V_{gd} = 0$; $\dfrac{\mu}{\mu + 1} V_{gd} = 0$

Output impedance $Z_o = \dfrac{r_d}{\mu + 1} \| R_s$

when $\mu >> 1$ (typical value of $\mu = 50$)

$$Z_o \approx \frac{r_d}{\mu} \| R_s = \frac{1}{g_m} \| R_s$$

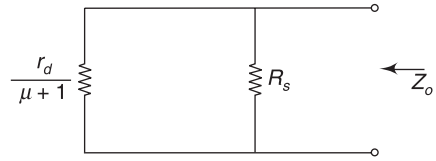


Fig. 5.37 *(c) Calculation of output impedance*

EXAMPLE 5.9

In the CD amplifier of Fig. 5.37(b), let $R_s = 4$ kΩ, $R_G = 10$ MΩ, μ = 50, and $r_d = 35$ kΩ. Evaluate the voltage gain A_V, input impedance Z_i and output impedance Z_o.

Solution The voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_s}{(\mu + 1)\, R_s + r_d}$$

$$= \frac{50 \times 4 \times 10^3}{(50 + 1) \times 4 \times 10^3 + 35 \times 10^3} = 0.836$$

The positive value indicates that V_o and V_i are in-phase and further note that $A_V < 1$ for CD amplifier.

Input impedance $Z_i = R_G = 10$ MΩ

Output impedance $Z_o = \dfrac{1}{g_m} \| R_s$

$$= \left(\frac{r_d}{\mu} \right) \| R_s$$

$$Z_o = \frac{35 \times 10^3}{50} \| 4 \times 10^3 = 595.7\ \Omega$$

5.18.3 Common-Gate (CG) Amplifier

A simple common-gate amplifier is shown in Fig. 5.38(a) and the associated small-signal equivalent circuit using the current-source model of FET is shown in Fig. 5.38(b).

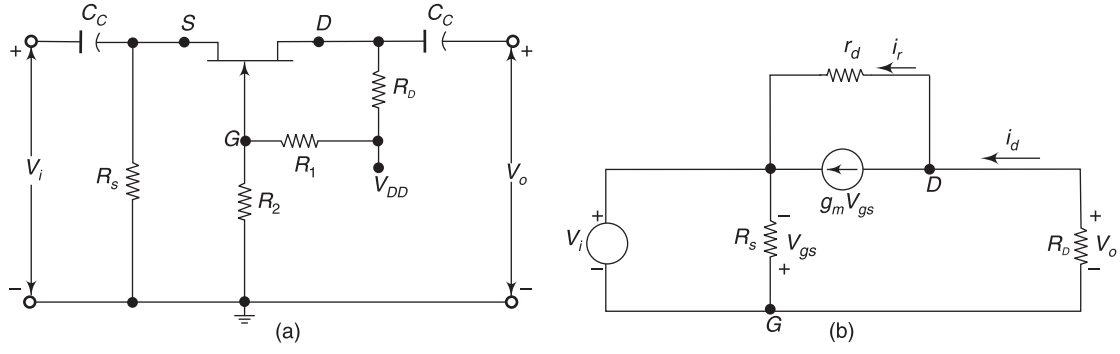


Fig. 5.38 *(a) Common-gate amplifier (b) Small-signal equivalent circuit of a CG amplifier*

➤ ***Voltage Gain*** From the small-signal equivalent circuit by applying KCL, $i_r = i_d - g_m V_{gs}$. Applying KVL around the outer loop gives

$$V_o = (i_d - g_m V_{gs})\, r_d - V_{gs}$$

But $$V_i = -V_{gs} \quad \text{and} \quad i_d = \frac{-V_o}{R_D}$$

Thus, $$V_o = \left(\frac{-V_o}{R_D} + g_m V_i\right) r_d + V_i$$

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{(g_m r_d + 1) R_D}{R_D + r_d} \tag{5.22}$$

➤ ***Input Impedance*** Figure 5.38(b) is modified for calculation of input impedance as shown in Fig. 5.38(c).

Current through r_d is given by

$$I_{rd} = -I_r = I_1 + g_m V_{gs}$$

$$I_1 = I_{rd} - g_m V_{gs}$$

where $$I_{rd} = \frac{V_i - V_o}{r_d}$$

$$= \frac{V_i - I_{RD} R_D}{r_d}$$

Hence, $$I_1 = \frac{V_i - I_{RD} R_D}{r_d} - g_m V_{gs}$$

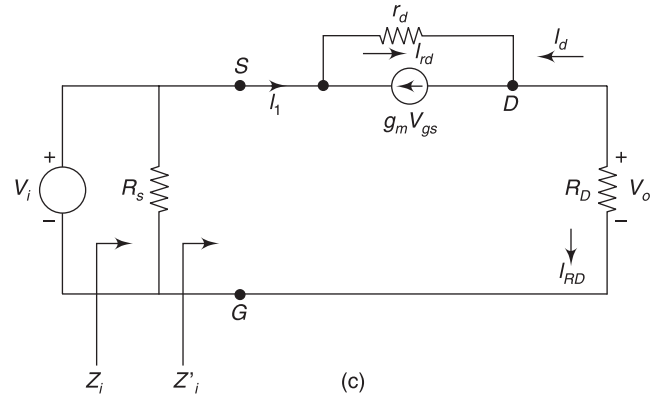


Fig. 5.38 *(c) Modified equivalent circuit*

From Fig. 5.38(c),

$$V_i = -V_{gs}$$

$$I_1 = \frac{V_i - I_{RD} R_D}{r_d} + g_m V_i$$

$$= \frac{V_i}{r_d} - \frac{I_{RD} R_D}{r_d} + g_m V_i$$

$$I_1 + \frac{I_{RD} R_D}{r_d} = \frac{V_i}{r_d} + g_m V_i$$

From Fig. 5.38(c),

$$I_1 = I_{RD}$$

Therefore, $$I_1 \left[\frac{r_d + R_D}{r_d}\right] = V_i \left[\frac{1}{r_d} + g_m\right]$$

$$\frac{V_i}{I_1} = \frac{r_d + R_D}{1 + g_m r_d} = Z_i'$$

From Fig. 5.38(c),

$$Z_i = R_s \parallel Z_i'$$

$$= R_s \parallel \frac{r_d + R_D}{1 + g_m r_d}$$

In practice, $r_d >> R_D$ and $g_m r_d >> 1$.

Therefore, $$Z_i = R_s \parallel \frac{r_d}{g_m r_d}$$

Therefore, $$Z_i = R_s \parallel \frac{1}{g_m}$$

➤ ***Output Impedance*** It is the impedance seen from the output, terminals with input short-circuited.

From Fig. 5.38(c), when $V_i = 0$, $V_{sg} = 0$, the resultant equivalent circuit is shown in Fig. 5.38(d).

$$Z_o = r_d \parallel R_D$$

as $$r_d >> R_D$$

$$Z_o \approx R_D$$

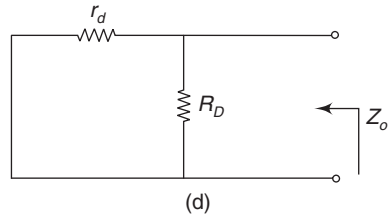


Fig. 5.38 *(d) Equivalent circuit for output impedance*

EXAMPLE 5.10

In the CG amplifier of Fig. 5.38(b), let $R_D = 2$ kΩ, $R_s = 1$ kΩ, $g_m = 1.43 \times 10^{-3}$ mho, and $r_d = 35$ kΩ. Evaluate the voltage gain A_V, input impedance Z_i, and output impedance Z_o.

Solution The voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{(g_m r_d + 1) R_D}{R_D + r_d} = \frac{(1.43 \times 10^{-3} \times 35 \times 10^3 + 1)\, 2 \times 10^3}{2 \times 10^3 + 35 \times 10^3} = 2.75$$

Input impedance $Z_i = R_s \parallel \frac{1}{g_m} = 1 \times 10^3 \parallel \frac{10^3}{1.4} = 0.41\ \text{k}\Omega$

Output impedance $Z_o \approx R_D = 2\ \text{k}\Omega$

REVIEW QUESTIONS

1. What is a thyristor? Mention some of them.
2. Describe the working principle of an SCR with *V–I* characteristics
3. Draw the two-transistor model of an SCR and explain its breakdown operation.
4. Once the SCR is triggered, the gate loses its control. Explain.
5. Explain the two transistor analogy of an SCR.
6. What is the disadvantage of conventional thyristor? Explain how GTO will overcome this disadvantage.
7. Draw the basic structure of GTO and explain its operation.
8. Draw the symbols of GTO.
9. Draw the two-transistor analogy of GTO and explain its functions.
10. Explain the operation of a simplified gate drive circuit for a GTO.
11. Explain the turn-ON and turn-OFF processes of GTO.
12. Explain the operation of GTO with its neat *I–V* characteristics.
13. What are the advantages and disadvantages of a GTO?
14. What are the applications of GTO?
15. Describe briefly about power BJT and power MOSFET.
16. Explain in detail DMOS structure.
17. Write briefly about VMOS structure and its characteristics.
18. Why is a Field Effect Transistor called so?
19. Explain the construction of *N* channel JFET.
20. With the help of neat sketches and characteristic curves, explain the operation of the junction FET.
11. What are the relative merits of an *N*-channel and *P*-channel FET?
22. Compare JFET with BJT.
23. Explain why BJTs are called bipolar devices while FETs are called unipolar devices.
24. Briefly describe some applications of JFET.
25. What is a MOSFET? How many types of MOSFETs are there?
26. With the help of suitable diagrams, explain the working of different types of MOSFET.
27. How does the constructional feature of a MOSFET differ from that of a JFET?
28. Why are *N*-channel MOSFETs preferred over *P*-channel MOSFETs?
29. Describe briefly about the small signal equivalent circuit of JFET and its associated parameters with necessary diagrams.
30. Draw the small-signal equivalent circuit of FET amplifier in CS connection and derive the equations for voltage gain, input impedance, and output impedance.

31. In the CS amplifier of Fig. 5.34(a), let $R_D = 4$ kΩ, $R_G = 50$ MΩ, μ = 40, $r_d = 40$ kΩ. Evaluate A_V, Z_i and Z_o. [*Ans.* $A_V = -3.64$, $Z_i = 50$ MΩ $Z_o = 4$ kΩ]

32. Draw the small-signal equivalent circuit of FET amplifier in CD connection and derive the equation for voltage gain, input impedance, and output impedance.

33. In the CD amplifier of Fig. 5.35(a), let $R_s = 2$ kΩ, $R_G = 10$ MΩ, μ = 40, $r_d = 40$ kΩ. Calculate A_v, Z_i, and Z_o. [*Ans.* $A_V = 0.66$, $Z_i = 10$ MΩ $Z_o = 0.67$ kΩ]

34. Draw the small-signal equivalent circuit of a FET amplifier in CG connection and derive the equation for voltage gain, input impedance and output impedance.

35. In the CG amplifier of Fig. 5.36(b), let $R_D = 4$ kΩ, $R_s = 2$ kΩ, $g_m = 2 \times 10^{-3}$ mho, $r_d = 40$ kΩ. Calculate A_V, Z_i and Z_o. [*Ans.* $A_V = 7.36$, $Z_i = 0.4$ kΩ, $Z_o = 4$ kΩ]

OBJECTIVE-TYPE QUESTIONS

1. In the forward blocking region of a silicon-controlled rectifier, the SCR is
(a) in the OFF-state (b) in the ON-state
(c) reverse biased (d) at the point of breakdown

2. The *di/dt* protection for an SCR is achieved through the use of
(a) *R* in series with SCR (b) *RL* in series with SCR
(c) *RL* across SCR (d) *L* in series with SCR.

3. After firing an SCR, if the gate pulse is removed, the SCR current
(a) remains the same (b) reduces to zero
(c) rises up (d) rises a little and then falls to zero

4. A thyristor turned on by light irradiation is known as
(a) gate turn ON thyristor (b) LASCR
(c) DIACT (d) RIAC

5. The thyristors with slow turn OFF time are called
(a) converter-grade SCR (b) inverter-grade SCR
(c) chopper-grade SCR (d) all the above

6. The thyristors with fast turn OFF time are called
(a) converter-grade SCR (b) inverter-grade SCR
(c) chopper-grade SCR (d) all the above

7. ____ is used for protection of SCR against turn ON *dv/dt* and reverse recovery transients.
(a) Circuit breakers (b) Fast-acting current limiting fuses
(c) Snubber circuits (d) None of the above

8. GTO can be turned OFF by
(a) removing the supply (b) reverse bias
(c) applying negative gate current (d) reducing latching current

9. Which of the following statements is true?
(a) FET and BJT, both are unipolar (b) FET and BJT, both are bipolar
(c) FET is bipolar and BJT is unipolar (d) FET is unipolar and BJT is bipolar

10. An FET has
(a) very high input resistance (b) very low input resistance
(c) high connection emitter junction (d) forward-biased *PN* junction

11. The drain source voltage at which drain current becomes nearly constant is called
(a) barrier voltage (b) breakdown voltage
(c) pick-off-voltage (d) pinch-off-voltage

12. The main factor which makes a MOSFET likely to breakdown during normal handling is its
(a) very low gate capacitance (b) high leakage current
(c) high input resistance (d) both (a) and (c)

13. In an *N*-channel JFET,
(a) the current carriers are holes (b) the current carriers are electrons
(c) V_{GS} is positive (d) the input resistance is very low

14. The magnitude of the current source in the ac equivalent circuit of an FET depends on
(a) the dc supply voltage (b) V_{DS}
(c) externally drain resistance (d) transconductance and gate to source voltage

15. A CMOS amplifier, when compared to an *N*-channel MOSFET, has the advantage of
(a) higher cut-off frequency
(b) higher voltage gain
(c) higher current gain
(d) lower current drain from the power supply, thereby less dissipation.

16. A junction FET can be used as a voltage variable resistor
(a) at pinch-off condition (b) beyond pinch-off voltage
(c) well below pinch-off condition (d) for any value of V_{DS}

17. Which of the following devices is used in the microprocessors?
(a) JEET (b) BJT (c) MOSFET (d) CMOS

18. The MOSFET switch in its ON-state may be considered as equivalent to
(a) resistor (b) inductor (c) capacitor (d) battery

19. The pinch-off voltage for a *N*-channel JFET is 4 V. When $V_{GS} = 1$ V, the $|V_{DS(\min)}|$ at which the pinch-off occurs is equal to
(a) 3 V (b) 5 V (c) 4 V (d) 1 V

20. In an *N*-channel JFET, V_{GS} is held constant. V_{DS} is less than the breakdown voltage. As V_{DS} is increased,
(a) conducting cross-sectional area of the channel
(b) '*S*' decreases and '*J*' decreases; '*S*' and the channel current density '*J*' both increase
(c) '*S*' decreases and '*J*' increase
(d) '*S*' increases and '*J*' decreases

21. In MOSFET devices, the *N*-channel type is better than the *P*-channel in the following respects:
(a) It has better noise immunity (b) It is faster
(c) It is TTL compatible (d) It has better drive capability

22. The 'pinch-off' voltage of a JFET is 5.0 volt, its 'cut-off' voltage is
(a) $(5.0)\frac{1}{2}V$ (b) 2.5 V (c) 5.0 V (d) $(5.0)\frac{2}{3}V$

23. Which of the following effects can be caused by a rise in the temperature?
(a) Increase in MOSFET current (I_{DS}) (b) Increase in BJT current (I_C)
(c) Decrease in MOSFET current (I_{DS}) (d) Decrease in BJT current (I_C)

24. An *N*-channel JFET has $I_{DSS} = 2$ mA and $V_p = -4$V. Its transconductance g_m(in mA/V) for an applied GATE to source voltage V_{GS} of –2V is
(a) 0.25 (b) 0.5 (c) 0.75 (d) 1.0

25. MOSFET can be used as a
(a) current-controlled capacitor (b) voltage-controlled capacitor
(c) current-controlled inductor (d) voltage-controlled inductor

26. The effective channel length of a MOSFET in saturation decreases with increase in
(a) gate voltage (b) drain voltage (c) source voltage (d) body voltage

27. The drain of an *N*-channel MOSFET is shorted to the gate so that $V_{GS} = V_{DS}$. The threshold voltage (V_T) of MOSFET is 1 V. If the drain current I_D is 1 mA for $V_{GS} = 2V$, then for $V_{GS} = 3V$, I_D is
(a) 2 mA (b) 3 mA (c) 9 mA (d) 4 mA

28. In a CS amplifier with diode connected load, the input-output characteristics is relatively
(a) zero (b) constant (c) non linear (d) linear

29. The voltage gain of the CS amplifier if $R_D = 4\ \text{k}\Omega$, $\mu = 40$ and $r_d = 40\ \text{k}\Omega$ is
(a) –3.64 (b) 0.66 (c) –0.66 (d) 1.66

30. The voltage gain of a given common-source JFET amplifier does not depend on its
(a) input impedance (b) amplification factor
(c) dynamic drain resistance (d) drain load resistance

31. The voltage gain in CD amplifier depends on
(a) g_m and R_D (b) g_m and R_s (c) g_m (d) R_D

6 Amplifiers and Oscillators

6.1 INTRODUCTION

Feedback plays a very important role in electronic circuits and the basic parameters such as input impedance, current or voltage gains, and bandwidth may be altered considerably by the use of feedback for a given amplifier. In large-signal amplifiers and electronic measuring instruments, the major problem of distortion should be avoided as far as possible. Again, the gain must be independent of external factors such as variation in the voltage of the dc supply and the values of the circuit components. All this can be achieved by means of feedback. A portion of the output signal is taken from the output of the amplifier and is combined with the normal input signal and thereby, the feedback is accomplished.

Any circuit which is used to generate a periodic voltage without an ac input signal is called an oscillator. To generate the periodic voltage, the circuit is supplied with energy from a dc source. If the output voltage is a sine wave function of time, the oscillator is called a "sinusoidal" or "harmonic" oscillator. Positive feedback and negative resistance oscillators belong to this category. There is another category of oscillators which generate non-sinusoidal waveforms such as square, rectangular, triangular, or sawtooth waves. This chapter surveys methods of generating the sinusoidal waveforms.

6.2 CLASSIFICATION OF BASIC AMPLIFIERS

The basic amplifiers are normally classified into four broad categories, as voltage, current, transconductance, and transresistance, amplifiers based on the magnitudes of the input and output impedances of an amplifier, with respect to the source and load impedances. These basic amplifiers are used in feedback amplifiers.

➤ ***Voltage Amplifier*** Figure 6.1 shows a Thevenin's equivalent circuit of a voltage amplifier. If the amplifier input resistance R_i is large when compared to the source resistance R_s, then $V_i \approx V_s$. If the external load resistance R_L is large when compared to the output resistance R_o of the amplifier, then $V_o \approx A_v V_i \approx A_v V_s$, where A_v represents the open-circuit voltage gain with $R_L = \infty$. Such an amplifier provides a voltage output proportional to the voltage input, and the proportionality factor does not depend on the magnitudes of the source and load resistances. Such a circuit is called a voltage amplifier.

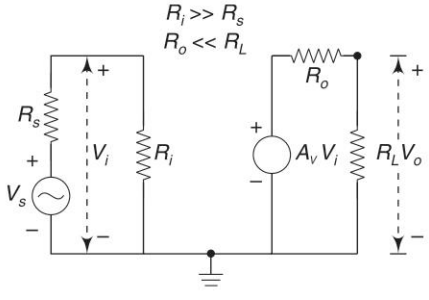


Fig. 6.1 *Voltage amplifier* $V_o \approx A_v V_s$

An ideal voltage amplifier must have infinite input resistance R_i and zero output resistance R_o. But for a practical voltage amplifier, $R_i >> R_s$ and $R_o << R_L$.

➤ ***Current Amplifier*** Figure 6.2 shows a Norton's equivalent circuit of current amplifier, in which $A_i \approx I_L/I_i$, with $R_L = 0$, represents the short-circuit current gain. An ideal current amplifier is defined as an amplifier which provides an output current proportional to the signal current and the proportionality factor is independent of R_s and R_L. An ideal current amplifier must have zero input resistance R_i and infinite output resistance R_o. In practice, the amplifier has low input resistance, and high output resistance, i.e., $R_i << R_s$ and $R_o >> R_L$.

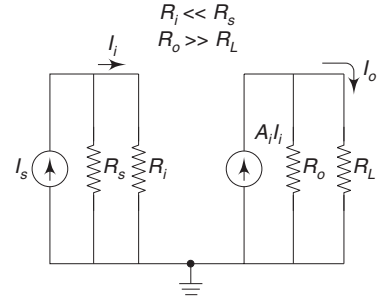


Fig. 6.2 *Current amplifier $I_L \approx A_iI_s$*

➤ ***Transconductance Amplifier*** Figure 6.3 shows the equivalent circuit of a transconductance amplifier, in which the input circuit is Thevenin and the output circuit is Norton. In an ideal transconductance amplifier, the output current is proportional to the signal voltage, independent of the magnitudes of R_s and R_L. An ideal amplifier must have an infinite input resistance R_i and infinite output resistance R_o. But a practical transconductance amplifier has a large input resistance $R_i >> R_s$ and high output resistance $R_o >> R_L$.

➤ ***Transresistance Amplifier*** Figure 6.4 shows the equivalent circuit of a transresistance amplifier, in which the input circuit is Norton and the output circuit is Thevenin and the output voltage V_o is proportional to the signal current I_s, independent of the magnitudes of R_s and R_L. Here, if $R_s >> R_i$, $I_i \approx I_s$ and if $R_o << R_L$, $V_o \approx R_mI_i \approx R_mI_s$. Note that $R_m = V_o/I_i$, with $R_L = \infty$ where R_m is the open-circuit transfer resistance. This amplifier is called a transresistance amplifier. For a practical transresistance amplifier, $R_i << R_s$ and $R_o << R_L$.

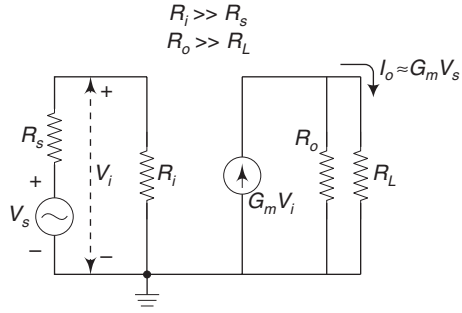


Fig. 6.3 *Transconductance amplifier*

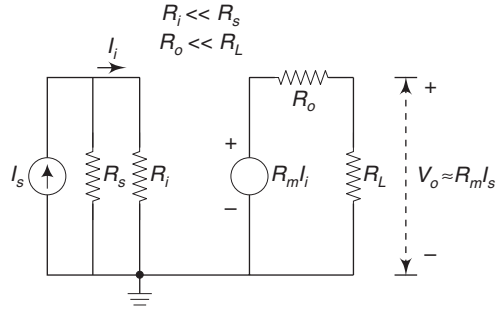


Fig. 6.4 *Transresistance amplifier*

The characteristics of the four ideal amplifier types are summarized in Table 6.1.

Table 6.1 *Characteristics of ideal basic amplifiers*

Properties of amplifier	Voltage amplifier	Current amplifier	Transconductance amplifier	Transresistance amplifier
R_i	∞	0	∞	0
R_o	0	∞	∞	0
Transfer gain	$V_o = A_vV_s$	$I_L = A_iI_S$	$I_L = G_mV_s$	$V_o = R_mI_s$

6.3 BASIC CONCEPT OF FEEDBACK

A block diagram of an amplifier with feedback is shown in Fig. 6.5. The output quantity (either voltage or current) is sampled by a suitable *sampler* which is of two types, namely, voltage sampler and current sampler, and fed to the *feedback network*. The output of feedback network, which has a fraction of the output signal, is combined with external source signal V_s through of a *mixer* and fed to the *basic amplifier*. Mixers, also known as comparators, are of two types, namely, series mixer and shunt mixer.

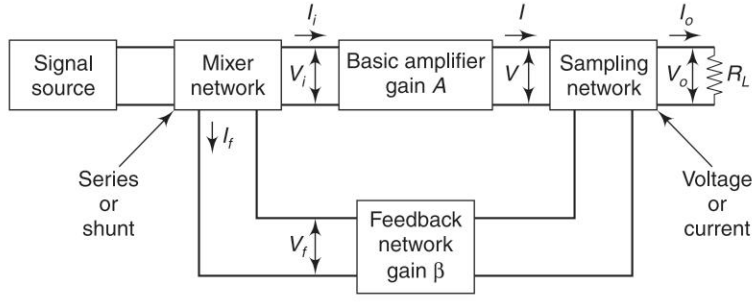


Fig. 6.5 *Block diagram of an amplifier with feedback*

A = gain of the basic amplifier = $\dfrac{V_o}{V_i}$

β = feedback ratio = $\dfrac{V_f}{V_o}$

A_f = gain of the feedback amplifier = $\dfrac{V_o}{V_s}$

V_s = ac signal in the input side (current or voltage)

V_f = feedback signal (current or voltage)

There are two types of feedback: (i) positive feedback, and (ii) negative feedback.

➤ ***Positive Feedback*** If the feedback signal V_f is in phase with the input signal V_s, then the net $V_i = V_s + V_f$. Hence, the input voltage applied to the basic amplifier is increased, thereby increasing V_o exponentially. This type of feedback is said to be positive or regenerative feedback. Gain of the amplifier with positive feedback is

$$A_f = \frac{V_o}{V_s} = \frac{V_o}{V_i - V_f}$$

$$= \frac{1}{\dfrac{V_i}{V_o} - \dfrac{V_f}{V_o}} = \frac{1}{\dfrac{1}{A} - \beta} = \frac{A}{1 - A\beta}$$

Here, $|A_f| > |A|$. The product of the open gain and the feedback factor is called the *loop gain*, i.e., loop gain = $A\beta$. If $|A\beta| = 1$, then $A_f = \infty$. Hence, the gain of the amplifier with positive feedback is infinite and the amplifier gives an ac output without an ac input signal. Thus, the amplifier acts as an oscillator.

The positive feedback increases the instability of an amplifier, reduces the bandwidth and increases the distortion and noise. The property of the positive feedback is utilized in oscillators.

➤ ***Negative Feedback*** If the feedback signal V_f is out of phase with the input signal V_s, then $V_i = V_s - V_f$. So the input voltage applied to the basic amplifier is decreased and correspondingly the output is decreased. Hence, the voltage gain is reduced. This type of feedback is known as negative or degenerative feedback. Gain of the amplifier with negative feedback is

$$A_f = \frac{V_o}{V_s} = \frac{V_o}{V_i + V_f} = \frac{1}{\frac{V_i}{V_o} + \frac{V_f}{V_o}} = \frac{1}{\frac{1}{A} + \beta} = \frac{A}{1 + A\beta}$$

Here, $|A_f| < |A|$. If $|A\beta| >> 1$, then $A_f = 1/\beta$, where β is a feedback ratio. Hence, the gain depends less on the operating potentials and the characteristics of the transistor or vacuum tube. The gain may be made to depend entirely on the feedback network. If the feedback network contains only stable passive elements, the gain of the amplifier using negative feedback is also stable.

The stabilization of the dc operating point of a transistor amplifier is accomplished by the use of negative feedback as far the dc potential is concerned and the operating point is kept constant in the case of change in temperature or a change in the h_{fe} or β of a transistor. Negative feedback is used to improve the performance of an electronic amplifier. Negative feedback always helps to increase the bandwidth, decrease distortion and noise, modify input and output resistances as desired. All the above advantages are obtained at the expense of reduction in voltage gain.

➤ ***Sampling Network*** There are two ways of sampling the signal at the output which is shown in Fig. 6.6(a) and (b). In Fig. 6.6(a), the output voltage is sampled by connecting the feedback network in shunt across the output. This type of connection at the output is referred to as voltage or node sampling. Another feedback connection which samples the output current is shown in Fig. 6.6(b), where the feedback network is connected in series with the output. This type of connection is referred to as current or loop sampling.

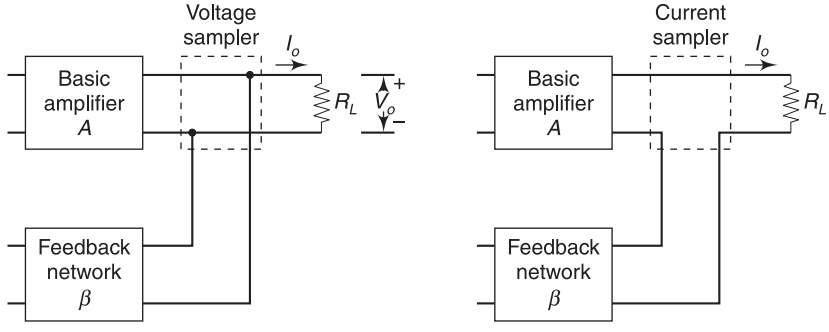


Fig. 6.6 *Feedback connections at the output of a basic amplifier*

➤ ***Feedback Network*** The block diagram of a feedback network shown in Fig. 6.5 is usually a passive two-port network which may contain resistors, capacitors, and inductors. Most often, it is simply a resistive configuration in amplifier circuits. It provides a reduced portion of the output as feedback signal to the input

mixer network and it is given as $V_f = \beta V_o$ where β is a feedback factor or feedback ratio which always lies between 0 and 1.

➤ ***Mixer Network*** Like sampling, there are two ways of mixing the feedback signal with the input signal. The two mixing blocks are shown in Fig. 6.7(a) and (b) at the input side of the amplifier. Figure 6.7(a) shows the series (loop) connection and Fig. 6.7(b) shows the shunt (node) connection at the input.

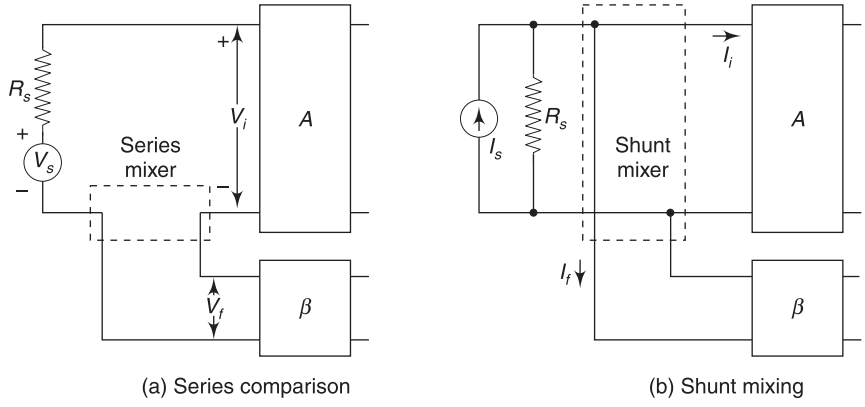


Fig. 6.7 *Feedback connections at the input of a basic amplifier*

➤ ***Transfer Ratio or Gain*** The symbol A shown in Fig. 6.5 represents the ratio of the output signal to the input signal of the basic amplifier. The transfer ratio V/V_i is the voltage amplification, or the voltage gain, A_V. Similarly, the transfer ratio I/I_i is the current amplification, or current gain, A_I for the amplifier. The ratio I/V_i of the basic amplifier is the transconductance G_M and V/I_i is the transresistance R_M.

Although G_M or R_M does not represent an amplification in the usual sense of the word, as the ratio of two signals shows one of these is a current and the other is a voltage signal. But it is convenient to refer to each of the four quantities A_V, A_I, G_M, and R_M as a transfer gain of the basic amplifier without feedback and to use the common symbol A to represent any one of these quantities. The symbol A_f is defined as the ratio of the output signal to the input signal of the amplifier and is called the transfer gain of the amplifier with feedback. Hence, A_f is used to represent any one of the four ratios $V_o/V_s \equiv A_{Vf}$, $I_o/I_s \equiv A_{If}$, $I_o/V_s \equiv G_{Mf}$ and $V_o/I_s \equiv R_{Mf}$.

Figure 6.8 shows the signal-flow diagram of a feedback amplifier in which quantity "X" represents either voltage or current signals. When the feedback signal X_f and the input signal X_i are out of phase, then the feedback is called negative feedback. In a negative feedback structure, the signal fedback to the input is out of phase with the input signal of the amplifier.

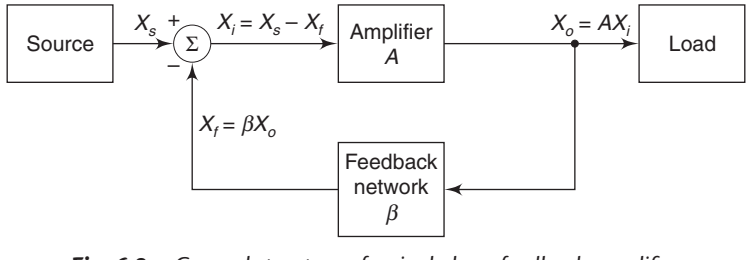


Fig. 6.8 *General structure of a single-loop feedback amplifier*

6.4 TRANSFER GAIN WITH FEEDBACK

Based on the type of sampling at the output side and the type of mixing to the input side, feedback amplifiers shown in Fig. 6.9, are classified into four topologies as

(1) voltage-series feedback or series shunt feedback
(2) current-series feedback or series series feedback
(3) current-shunt feedback or shunt series feedback
(4) voltage-shunt feedback or shunt shunt feedback

In Fig. 6.8, the source resistance R_s is considered to be part of the amplifier and the transfer gain $A(A_V, G_M, A_I, R_M)$ includes the effect of the loading of the β network (as well as R_L) upon the amplifier. The input signal X_s, the output signal X_o, the feedback signal X_f, and the difference signal X_d represent either a voltage or a current signal. These signals and the corresponding ratios A and β are summarized in Table 6.2.

Table 6.2 *Voltage and current signals in a feedback amplifier*

Signal or ratio	Voltage-series feedback	Current-series feedback	Current-shunt feedback	Voltage-shunt feedback
X_o	Voltage	Current	Current	Voltage
X_s, X_f, X_d	Voltage	Voltage	Current	Current
A	A_V	G_M	A_I	R_M
β	$\frac{V_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$	$\frac{I_f}{V_o}$

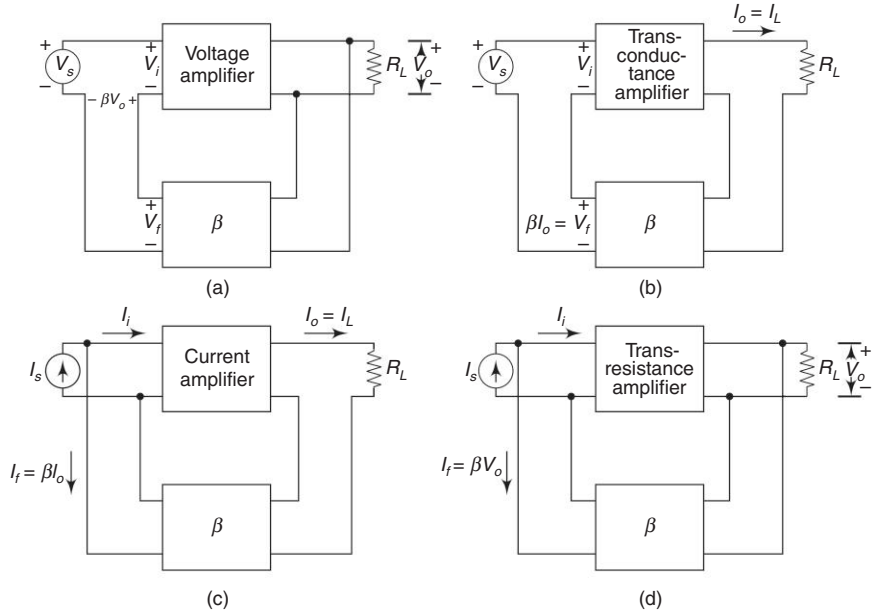


Fig. 6.9 *Feedback amplifier topologies: (a) Voltage amplifier with voltage-series feedback (b) Transconductance amplifier with current-series feedback (c) Current amplifier with current-shunt feedback (d) Transresistance amplifier with voltage-shunt feedback*

From Fig. 6.8, we know that

$$X_d = X_s - X_f = X_i$$

where X_d represents the difference between the applied input signal X_s and feedback signal X_f and it is called the error signal or comparison signal. The reverse transmission factor or feedback factor β is defined by

$$\beta = \frac{X_f}{X_o}$$

where the symbol X_o is the output voltage or the output current.

The transfer gain without feedback A is defined by

$$A = \frac{X_o}{X_i}$$

and the gain with feedback A_f is defined by

$$A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f} = \frac{X_o}{X_i + \beta X_o} = \frac{X_o}{X_i\,(1 + \beta X_o / X_i)}$$

$$A_f = \frac{A}{1 + \beta A}$$

Here, the symbol A represents open-loop gain or the transfer gain of the amplifier without feedback, which includes *the loading of the* β*-network*, R_L, R_s, and A_f represents the closed-loop gain or gain with feedback. If $|A_f| < |A|$, the feedback is termed as *negative,* or *degenerative* and if $|A_f| > |A|$, the feedback is termed *positive,* or *regenerative.* In the case of negative feedback, the gain of the basic amplifier with feedback is equal to the open-loop gain divided by the factor $(1 + \beta A)$.

6.5 GENERAL CHARACTERISTICS OF NEGATIVE FEEDBACK AMPLIFIERS

The positive feedback in an amplifier circuit results in oscillations as in various types of oscillators circuits. The negative feedback in amplifier circuit results in decreased voltage gain, noise, and distortion, but there will be an increase in bandwidth. In addition to these characteristics, input and output impedances get varied according to feedback connections.

Although there is a reduction in overall voltage gain, there are some improvements in using negative feedback in amplifier circuits as listed below:

1. Better stabilized voltage gain
2. Enhanced frequency response
3. Higher input impedance
4. Lower output impedance
5. Reduction in noise
6. Increase in linearity

The effects of negative feedback on amplifier characteristics according to the type of feedback connections can be found in Table 6.3.

The characteristics of negative feedback are discussed below in detail.

6.5.1 Desensitization or Stabilization of Gain

The variation due to aging, temperature, replacement, etc., of the circuit components and transistor or FET characteristics results in unstable amplifier transfer gain. The closed-loop gain of the amplifier with negative feedback is given by

$$A_f = \frac{A}{1 + \beta A}$$

Differentiating the above equation with respect to A, we have

$$\left|\frac{dA_f}{dA}\right| = \frac{(1 + \beta A)1 - \beta A}{(1 + \beta A)^2} = \frac{1}{(1 + \beta A)^2}$$

$$dA_f = \frac{dA}{(1 + \beta A)^2}$$

Dividing both sides by A_f, we get

$$\frac{dA_f}{A_f} = \frac{dA}{(1 + \beta A)^2} \times \frac{1}{A_f} = \frac{dA}{(1 + \beta A)^2} \times \frac{(1 + \beta A)}{A} = \frac{dA}{A} \times \frac{1}{(1 + \beta A)}$$

$$\frac{dA_f}{A_f} = \frac{dA/A}{(1 + \beta A)}$$

The term $\frac{dA_f}{A_f}$ represents the fractional change in amplifier voltage gain with feedback and $\frac{dA}{A}$ denotes the fractional change in voltage gain without feedback. The term $1/1 + A\beta$ is called *sensitivity*.

Therefore, the sensitivity is defined as the ratio of percentage change in voltage gain with feedback to the percentage change in voltage gain without feedback.

$$\text{Sensitivity} = \frac{\left(\frac{dA_f}{A_f}\right)}{\left(\frac{dA}{A}\right)} = \frac{1}{(1 + \beta A)}$$

For example, if the sensitivity is 0.1, then the percentage change in gain with feedback is one-tenth the percentage change in gain without feedback.

The reciprocal of the term sensitivity is called *desensitivity D*, or desensitivity $D = (1 + \beta A)$.

Hence, the transfer gain divided by desensitivity is called the closed-loop gain and it can be written as

$$A_f = \frac{A}{1 + \beta A} = \frac{A}{D}$$

In particular, if $|\beta A| >> 1$, then

$$A_f = \frac{A}{1+\beta A} \approx \frac{A}{\beta A} = \frac{1}{\beta}$$

Hence, the gain depends entirely on the feedback network. If the feedback network contains only stable passive elements, the improvement in stability may be high. Increase in stability shows that the gain is made insensitive to changes in transistor parameters. Since A represents either A_V, G_M, A_I, or R_M, then A_f represents the corresponding transfer gains with feedback: either A_{Vf}, G_{Mf}, A_{If} or R_{Mf}.

For voltage-series feedback, $A_{Vf} \approx 1/\beta$ shows that the voltage gain is stabilized. For current-series feedback, $G_{Mf} \approx 1/\beta$ $G_{Mf} \approx 1/\beta$, shows that the transconductance gain is desensitized. Similarly, the current gain is desensitized for current-shunt feedback ($A_{If} \approx 1/\beta$) and the transresistance gain is stabilized or desensitized for voltage-shunt feedback ($R_{Mf} \approx 1/\beta$).

EXAMPLE 6.1

An amplifier has an open-loop gain of 1000 and a feedback ratio of 0.04. If the open-loop gain changes by 10% due to temperature, find the percentage change in gain of the amplifier with feedback.

Solution Given $A = 1000$, $\beta = 0.04$ and $\frac{dA}{A} = 10$

We know that the percentage change in gain of the amplifier with feedback is

$$\frac{dA_f}{A_f} = \frac{dA}{A}\frac{1}{1+A\beta)} = 10 \times \frac{1}{1+1000\times 0.04} = 0.25\%$$

EXAMPLE 6.2

An amplifier has voltage gain with feedback of 100. If the gain without feedback changes by 20% and the gain with feedback should not vary more than 2%, determine the values of open-loop gain A and feedback ratio β.

Solution Given $A_f = 100$, $\frac{dA_f}{A_f} = 2\% = 0.02$ and $\frac{dA}{A} = 20\% = 0.2$

We know that $$\frac{dA_f}{A_f} = \frac{dA}{A}\frac{1}{(1+A\beta)}$$

$$0.02 = 0.2 \times \frac{1}{1+A\beta}$$

Therefore, $$(1+A\beta) = \frac{0.2}{0.02} = 10$$

Also, we know that the gain with feedback is

$$A_f = \frac{A}{1+A\beta}$$

i.e., $$100 = \frac{A}{10}$$

Therefore, $A = 1000$

$1 + A\beta = 10$; i.e., $A\beta = 9$

Therefore, $$\beta = \frac{9}{1000} = 0.009$$

6.5.2 Extension of Bandwidth

We know that the gain with feedback for an amplifier is given by

$$A_f = \frac{A}{1 + \beta A}$$

Using the above equation, we can write

$$A_{f\,\text{mid}} = \frac{A_{\text{mid}}}{1 + \beta A_{\text{mid}}}$$

$$A_{f\,\text{low}} = \frac{A_{\text{low}}}{1 + \beta A_{\text{low}}}$$

and $$A_{f\,\text{high}} = \frac{A_{\text{high}}}{1 + \beta\, A_{\text{high}}}$$

The effect of negative feedback on lower cut-off and upper cut-off frequencies of the amplifier is analyzed here.

➤ ***Lower Cut-off Frequency*** We know that the relation between gain at lower cut-off frequency and gain at mid frequency for an amplifier is given as

$$\frac{A_{\text{low}}}{A_{\text{mid}}} = \frac{1}{1 - j\left(\frac{f_L}{f}\right)}$$

Therefore, $$A_{\text{low}} = \frac{A_{\text{mid}}}{1 - j\left(\frac{f_L}{f}\right)}$$

Substituting A_{low} in the $A_{f\,\text{low}}$ equation, we get

$$A_{f\,\text{low}} = \frac{\frac{A_{\text{mid}}}{1 - j\left(\frac{f_L}{f}\right)}}{1 + \beta \frac{A_{\text{mid}}}{1 - j\left(\frac{f_L}{f}\right)}} = \frac{A_{\text{mid}}}{1 - j\left(\frac{f_L}{f}\right) + A_{\text{mid}}\beta} = \frac{A_{\text{mid}}}{(1 + A_{\text{mid}}\beta) - j\left(\frac{f_L}{f}\right)}$$

Dividing numerator and denominator by $(1 + A_{\text{mid}}.\beta)$, we have

$$A_{f\,\text{low}} = \frac{\dfrac{A_{\text{mid}}}{1 + A_{\text{mid}}\beta}}{1 - j\left[\dfrac{f_L}{(1 + A_{\text{mid}}\beta) f}\right]}$$

$$= \frac{A_{f\,\text{mid}}}{1 - j\left[\left(\dfrac{f_L}{(1 + A_{\text{mid}}\beta) f}\right)\right]}, \text{ since } A_{f\,\text{mid}} = \frac{A_{\text{mid}}}{1 + A_{\text{mid}}\beta}$$

Therefore, $$\frac{A_{f\,\text{low}}}{A_{f\,\text{mid}}} = \frac{1}{1 - j\left(\dfrac{f_{Lf}}{f}\right)}$$

where the lower cut-off frequency with feedback is given as

$$f_{Lf} = \frac{f_L}{1 + A_{\text{mid}}\beta}$$

From the above equation, we can say that lower cut-off frequency with feedback is less than the lower cut-off frequency without feedback by factor $(1 + A_{\text{mid}}\,\beta)$. Therefore, by introducing negative feedback, low-frequency response of the amplifier is improved.

➤ ***Upper Cut-off Frequency*** We know that the relation between gain at upper cut-off frequency and gain at mid frequency for an amplifier is given as

$$\frac{A_{\text{high}}}{A_{\text{mid}}} = \frac{1}{1 + j\left(\dfrac{f}{f_H}\right)}$$

$$A_{\text{high}} = \frac{A_{\text{mid}}}{1 + j\left(\dfrac{f}{f_H}\right)}$$

Substituting A_{high} in the $A_{f\,\text{high}}$ equation, we have

$$A_{f\text{high}} = \frac{\dfrac{A_{\text{mid}}}{1 + j\left(\dfrac{f}{f_H}\right)}}{1 + \beta\left[\dfrac{A_{\text{mid}}}{1 + j\left(\dfrac{f}{f_H}\right)}\right]} = \frac{A_{\text{mid}}}{1 + j\left(\dfrac{f}{f_H}\right) + A_{\text{mid}}\beta}$$

Dividing numerator and denominator by $(1 + A_{\text{mid}}\,\beta)$, we get

$$A_{f\,\text{high}} = \frac{\dfrac{A_{\text{mid}}}{1 + A_{\text{mid}}\beta}}{1 + j\left[\dfrac{f}{(1 + A_{\text{mid}}\beta) f_H}\right]}$$

$$A_{f\,\text{high}} = \frac{A_{f\,\text{mid}}}{1 + j\left[\dfrac{f}{(1 + A_{\text{mid}}\beta)\, f_H}\right]}, \text{ since } A_{f\,\text{mid}} = \frac{A_{\text{mid}}}{1 + A_{\text{mid}}\beta}$$

Therefore, $$\frac{A_{f\,\text{high}}}{A_{f\,\text{mid}}} = \frac{1}{1 + j\left(\dfrac{f}{f_{Hf}}\right)}$$

where the upper cut-off frequency with feedback is given as

$$f_{Hf} = (1 + A_{\text{mid}}\,\beta)\, f_H$$

From the above equation, we can say that upper cut-off frequency with feedback is greater than upper cut-off frequency without feedback by factor $(1 + A_{\text{mid}}\,\beta)$. Therefore, by introducing negative feedback, high-frequency response of the amplifier is improved.

The bandwidth of the amplifier without feedback is given as

$$BW = f_H - f_L$$

Therefore, the bandwidth of the amplifier with feedback can be written. or

$$BW_f = f_{Hf} - f_{Lf} = (1 + A_{\text{mid}}\beta)\, f_H - \frac{f_L}{(1 + A_{\text{mid}}\beta)}$$

or, it can also be written as

$$BW_f = BW(1 + A_{\text{mid}}\,\beta)$$

From the frequency-response graph shown in Fig. 6.10, it is very clear that $(f_{Hf} - f_{Lf}) > (f_H - f_L)$ and hence, the bandwidth of the amplifier with feedback is greater than the bandwidth of the amplifier without feedback. As the voltage gain of a feedback amplifier reduces by the factor $(1 + A\beta)$, its bandwidth increases by $(1 + A\beta)$. This shows that the product of voltage gain and bandwidth of an amplifier with feedback and without feedback remains the same, i.e., $A_f \times BW_f = A \times BW$.

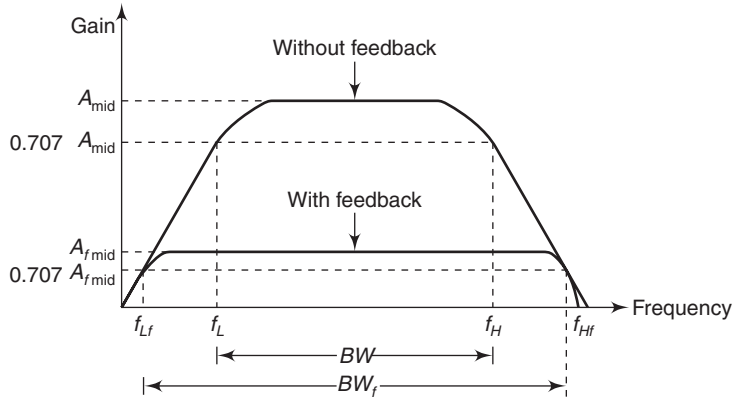


Fig. 6.10 *Effect of negative feedback on gain and bandwidth*

EXAMPLE 6.3

An amplifier has a midband gain of 125 and a bandwidth of 250 kHz. (a) If 4% negative feedback is introduced, find the new bandwidth and gain. (b) If the bandwidth is to restricted to 1 MHz, find the feedback ratio.

Solution Given $A = 125$, $BW = 250$ kHz, and $\beta = 4\% = 0.04$

(a) We know that $BW_f = (1 + A\beta)\, BW$

$$= (1 + 125 \times 0.04) \times 250 \times 10^3$$

$$= 1.5 \text{ MHz}$$

Gain with feedback, $A_f = \dfrac{A}{1 + A\beta} = \dfrac{125}{1 + 125 \times 0.04} = \dfrac{125}{6} = 20.83$

(b) $BW_f = (1 + A\beta')\, BW$

$$1 \times 10^6 = (1 + 125\, \beta') \times 250 \times 10^3$$

Therefore, $(1 + 125\, \beta') = \dfrac{1 \times 10^6}{250 \times 10^3} = 4$

i.e., $\beta' = \dfrac{3}{125} = 0.024 = 2.4\%$

EXAMPLE 6.4

An *RC* coupled amplifier has a mid-frequency gain of 200 and a frequency response from 100 Hz to 20 kHz. A negative feedback network with $\beta = 0.02$ is incorporated into the amplifier circuit. Determine the new system performance.

Solution

$$A_f = \frac{A}{1 + A\beta} = \frac{200}{1 + 200 \times 0.02} = 40$$

$$f_{Lf} = \frac{f_L}{1 + A\beta} = \frac{100}{1 + 200 \times 0.02} = 20 \text{ Hz}$$

$$f_{Hf} = f_H \times (1 + A\beta) = 20 \times 10^3 \times (1 + 200 \times 0.02) = 100 \text{ kHz}$$

$$BW_f = f_{Hf} - f_{Lf} = 100 \times 10^3 - 20 \approx 100 \text{ kHz}$$

$$A_f \times BW_f = 40 \times 100 \times 10^3 = 4000 \text{ kHz}$$

$$BW = f_H - f_L = 20 \times 10^3 - 100 \approx 20 \text{ kHz}$$

$$A \times BW = 200 \times 20 \times 10^3 = 4000 \text{ kHz}$$

This shows that the gain-bandwidth product of the amplifier with negative feedback is same as that of the gain-bandwidth product of the amplifier without feedback.

6.5.3 Noise Reduction

Negative feedback reduces the noise or interference in an amplifier, more precisely, by increasing the ratio of signal to noise, which is possible only under certain conditions. Consider the amplifier block shown in

Fig. 6.11(a) with input signal V_s, noise signal V_n and gain A_1. Assume that the noise is introduced at the input of the amplifier and the signal-to-noise ratio for this amplifier is given by $S/N = V_s/V_n$.

In Fig. 6.11(b), another amplifier stage with gain A_2, which does not suffer from the noise problem, is connected before the main amplifier A_1 and by applying negative feedback around the overall cascaded block, the overall gain is maintained constant. The output voltage of the circuit shown in Fig. 6.11(b) can be obtained by superposition and it is given by

$$V_o = V_s \frac{A_1 A_2}{1 + A_1 A_2 \beta} + V_n \frac{A_1}{1 + A_1 A_2 \beta}$$

Thus, the signal-to-noise ratio at the output becomes

$$\frac{S}{N} = \frac{V_s \dfrac{A_1 A_2}{1 + A_1 A_2 \beta}}{V_n \dfrac{A_1}{1 + A_1 A_2 \beta}} = \frac{V_s}{V_n} A_2$$

which is A_2 times higher than the original case. Hence, there is an improvement in signal-to-noise ratio (SNR), by connecting a noise-free amplifier before the noisy stage, with the application of negative feedback. Improvement in SNR results in reduction of noise.

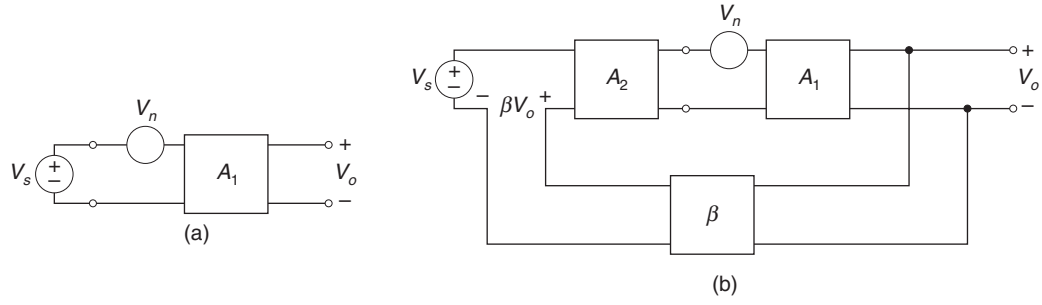


Fig. 6.11 *Noise reduction due to negative feedback*

6.5.4 Reduction in Nonlinear Distortion

The transfer characteristics of an amplifier shown in Fig. 6.12 indicates that it is piecewise linear, with the voltage gain changing from 1000 to 100 and then to 0. This nonlinear transfer characteristics of an amplifier generates a large amount of nonlinear distortion at the output.

This transfer characteristics can be considerably linearized (i.e., made less nonlinear) by applying negative feedback to the amplifier. As it is known that, negative feedback reduces the dependence of the overall closed-loop gain on the open-loop gain of the basic amplifier. Thus, large changes in open-loop gain (1000 to 100 in this case) results in much smaller changes in closed-loop gain.

The transfer characteristics of the closed-loop amplifier is shown in Fig. 6.12 as curve (b) in which a negative feedback with $\beta = 0.01$ is applied to the amplifier whose open-loop voltage transfer characteristic is indicated in Fig. 6.12 as curve (a). Here, the slope of the steepest segment is given by

$$A_{f1} = \frac{1000}{1 + 1000 \times 0.01} = 90.9$$

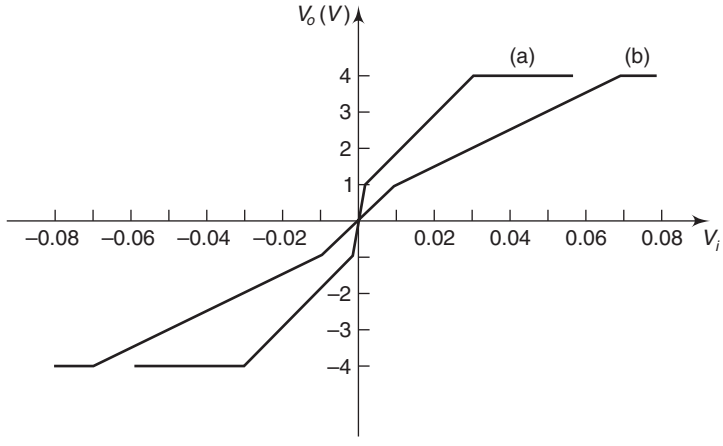


Fig. 6.12 *Transfer characteristics of feedback amplifier*

And the slope of the next segment is given by

$$A_{f2} = \frac{100}{1 + 100 \times 0.01} = 50$$

Thus, the order-of-magnitude change in slope with feedback as shown in (a) has been considerably reduced compared to the change in slope without feedback as shown in (b). This has been achieved at the expense of reduction in voltage gain. Thus, if the overall gain has to be restored, then a preamplifier should be added. This preamplifier should not present a severe nonlinear-distortion problem, since it deals with smaller signals.

Consider an amplifier with an open-loop voltage gain (A) and a total harmonic distortion without feedback (D). Then, due to introduction of negative feedback, with the feedback ratio (β), the distortion (D) is reduced by a factor of $1 + A\beta$ and the distortion with feedback (D_f) is given by

$$D_f = \frac{D}{1 + A\beta}$$

EXAMPLE 6.5

An amplifier has a voltage gain of 400, $f_1 = 50$ Hz, $f_2 = 200$ kHz and a distortion of 10% without feedback. Determine the amplifier voltage gain f_{1f}, f_{2f}, and D_f when a negative feedback is applied with feedback ratio of 0.01.

Solution Given $A = 400$, $f_1 = 50$ Hz, $f_2 = 200$ kHz, $D = 10\%$, and $\beta = 0.01$

We know that voltage gain with feedback

$$A_f = \frac{A}{1 + A\beta} = \frac{400}{1 + 400 \times 0.01} = 80$$

New lower 3 dB frequency,

$$f_{1f} = \frac{f_1}{1 + A\beta} = \frac{50}{1 + 400 \times 0.01} = 10 \text{ Hz}$$

New upper 3 dB frequency,

$$f_{2f} = (1 + A\beta) \times f_2 = (1 + 400 \times 0.01) \times 200 \times 10^3 = 1 \text{ MHz}$$

Distortion with feedback,

$$D_f = \frac{D}{1 + A\beta} = \frac{10}{5} = 2\%$$

6.6 EFFECT OF NEGATIVE FEEDBACK ON INPUT RESISTANCE

When the negative feedback signal is fed back to the input in series with the applied voltage, the input resistance is increased. Since the feedback voltage V_f opposes V_s, the input current I_i becomes less and the input resistance with feedback $R_{if} \equiv V_s/I_i$ is greater than the input resistance without feedback R_i. Hence, for voltage-series feedback and current-series feedback, $R_{if} = R_i\,(1 + \beta A) = R_i D$.

When the negative feedback signal is fed back to the input in shunt with the applied signal, the input resistance is decreased. Since $I_s = I_i + I_f$, then the source current I_s is increased and the input resistance with feedback $R_{if} \equiv V_i/I_s$ is smaller than the input resistance without feedback R_i. Hence, for voltage-shunt feedback and current-shunt feedback, $R_{if} = R_i/(1 + \beta A) = R_i/D$.

In other words, we can say that, in feedback amplifiers, series mixing at the input tends to increase the input resistance and shunt mixing tends to decrease the input resistance.

➤ ***Voltage-series Feedback*** The voltage-series feedback topology is shown in Fig. 6.13, with the amplifier input and output circuit replaced by its Thevenin's model. In this circuit, A_v represents the open-circuit voltage gain taking R_s into account. We have considered R_s to be part of the amplifier throughout the discussion of feedback amplifier. Here, the input impedance with feedback is given by $R_{if} = V_s/I_i$.

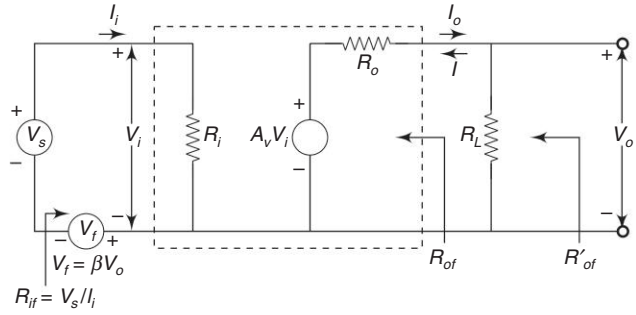


Fig. 6.13 *Voltage-series feedback circuit used for calculation of input and output resistances*

Applying KVL to the input side, we get

$$V_s = I_i R_i + V_f = I_i R_i + \beta V_o$$

The output voltage is written as

$$V_o = \frac{A_v V_i R_L}{R_o + R_L} = A_V V_i$$

where $A_V = \dfrac{V_o}{V_i} = \dfrac{A_v R_L}{R_o + R_L}$

Substituting the value of V_o in the above KVL equation, we get

$$V_s = I_i R_i + \beta A_v I_i R_i$$

Therefore,
$$R_{if} = \frac{V_s}{I_i} = R_i (1 + \beta A_v)$$

where A_v represents the open-circuit voltage gain without feedback and A_V indicates the voltage gain without feedback taking the load R_L into account. Therefore,

$$A_v = \lim_{R_L \to \infty} A_V$$

➤ ***Current-series Feedback*** The current-series feedback topology is shown in Fig. 6.14, with the amplifier input circuit represented by Thevenin's model and the output circuit by Norton's equivalent circuit. Here, the input impedance with feedback is given by $R_{if} = V_s / I_i$.

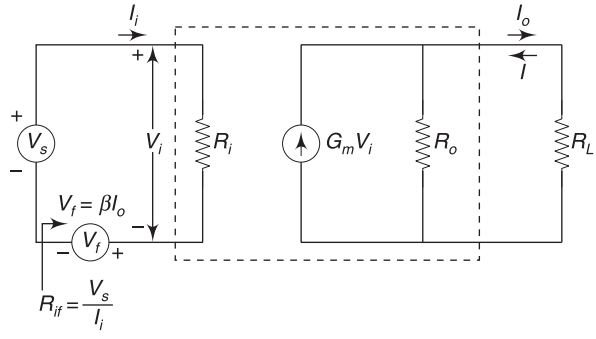


Fig. 6.14 *Current-series feedback circuit used for calculation of input and output resistances*

Applying KVL to the input side, we get

$$V_s = I_i R_i + V_f = I_i R_i + \beta I_o$$

The output current is written as

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i$$

where
$$G_M = \frac{I_o}{V_i} = \frac{G_m R_o}{R_o + R_L}$$

Substituting the value of I_o in the above KVL equation, we get

$$V_s = I_i R_i + \beta G_M I_i R_i$$

$$R_{if} = \frac{V_s}{I_i} = R_i (1 + \beta G_M)$$

where G_m represents the short-circuit transconductance without feedback and G_M indicates the transconductance without feedback taking the load R_L into account.

Therefore,
$$G_m = \lim_{R_L \to 0} G_M$$

➤ ***Current-shunt Feedback*** The current-shunt feedback topology is shown in Fig. 6.15, with the amplifier input and output circuits, replaced by its Norton's model.

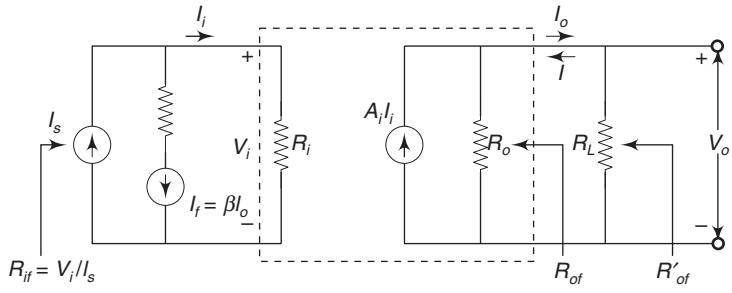


Fig. 6.15 *Current-shunt feedback circuit used for calculation of input and output resistances*

Applying KCL to the input side, we get

$$I_s = I_i + I_f = I_i + \beta I_o$$

The output current is written as

$$I_o = \frac{A_i I_i R_o}{R_o + R_L} = A_I I_i$$

where $A_I = \dfrac{I_o}{I_i} = \dfrac{A_i R_o}{R_o + R_L}$

Substituting the value of I_o in the above KCL equation, we get

$$I_s = I_i + \beta A_I I_i = (1 + \beta A_I)\, I_i$$

The input resistance with feedback is given as

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{(1 + \beta A_I)\, I_i} = \frac{R_i}{1 + \beta A_I}$$

where A_i represents the short-circuit current gain without feedback and A_I is the current gain without feedback taking the load R_L into account. Therefore,

$$A_i = \lim_{R_L \to 0} A_I$$

➤ ***Voltage-shunt Feedback*** The voltage-shunt feedback topology is shown in Fig. 6.16, with the amplifier input circuit represented by Norton's model and the output circuit by Thevenin's equivalent.

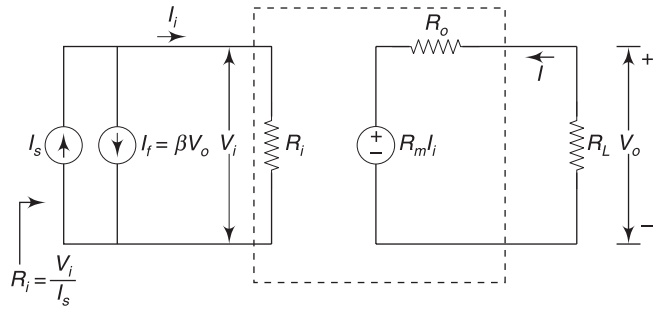


Fig. 6.16 *Voltage-shunt feedback circuit used for calculation of input and output resistances*

Applying KCL to the input side, we get

$$I_s = I_i + I_f = I_i + \beta V_o$$

The output voltage is written as

$$V_o = \frac{R_m I_i R_o}{R_o + R_L} = R_M I_i$$

where $R_M = \dfrac{V_o}{I_i} = \dfrac{R_m R_o}{R_o + R_L}$

Substituting the value of V_o in the above KCL equation, we get

$$I_s = I_i + \beta R_M I_i = (1 + \beta R_M)\, I_i$$

The input resistance with feedback is given as

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{(1 + \beta R_m) I_i} = \frac{R_i}{1 + \beta R_M}$$

where R_m represents the open-circuit transresistance without feedback and R_M is the transresistance without feedback taking the load R_L into account. Therefore,

$$R_m = \lim_{R_L \to \infty} R_M$$

6.7 EFFECT OF NEGATIVE FEEDBACK ON OUTPUT RESISTANCE

The negative feedback, which samples the output voltage, irrespective of how it is fed back to the input, decreases the output resistance. For example, if R_L increases, V_o increases. The effect of feeding this voltage to the input in the degenerative manner (negative feedback) causes V_o to increase. This increase in V_o is less than that of when there is no feedback and the output voltage tends to remain constant, as R_L changes, which means that $R_{of} << R_L$. Hence, sampling the output voltage reduces the output resistance.

Similarly, negative feedback, which samples the output current, will tend to hold this current constant. Hence, an output current source is created ($R_{of} >> R_L$), and it can be concluded that this type of current sampling increases the output resistance.

In other words, we can say that, in feedback amplifiers, voltage sampling at the output tends to decrease the output resistance ($R_{of} < R_o$) *and current sampling tends to increase the output resistance* ($R_{of} > R_o$).

➤ ***Voltage-series Feedback*** In voltage-series feedback topology shown in Fig. 6.13, the resistance with feedback R_{of} looking into the output terminals is obtained by disconnecting R_L (i.e., $R_L = \infty$) and by making the external source signal to zero (i.e., set $V_s = 0$). To find R_{of}, impress a voltage V across the output terminals and calculate the current I delivered by V. Then, $R_{of} = V/I$. In Fig. 6.13, V_o is replaced with V.

Applying KVL to the output side, we get

$$I = \frac{V - A_v V_i}{R_o}$$

The input voltage is written as

$$V_i = -V_f = -\beta V \quad (\text{with } V_s = 0)$$

Substituting V_i in the above KVL equation, we get

$$I = \frac{V + \beta A_v V}{R_o} = \frac{V(1 + \beta A_v)}{R_o}$$

The output resistance with feedback is given as

$$R_{of} = \frac{V}{I} = \frac{R_o}{1 + \beta A_v}$$

where A_v represents the open-circuit voltage gain without taking the load R_L into account.

The output resistance with feedback R'_{of} including R_L as part of the amplifier is given by

$$R'_{of} = R_{of} \| R_L$$

Therefore,

$$R'_{of} = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{R_o R_L}{(1 + \beta A_v)\left[\frac{R_o}{1 + \beta A_v} + R_L\right]} = \frac{R_o R_L}{R_o + R_L + \beta A_v R_L}$$

Dividing numerator and denominator by $(R_o + R_L)$, we get

$$R'_{of} = \frac{R_o R_L / (R_o + R_L)}{1 + \left[\beta A_v R_L / (R_o + R_L)\right]}$$

where $R'_o = \frac{R_o R_L}{R_o + R_L}$ and $A_V = \frac{A_v R_L}{R_o + R_L}$

$$R'_{of} = \frac{R'_o}{1 + \beta A_V}$$

where A_V indicates the open-circuit voltage gain taking the load R_L into account.

➤ ***Voltage-shunt Feedback*** The voltage-shunt feedback topology is shown in Fig. 6.16. For finding R_{of}, R_L is disconnected (i.e., $R_L = \infty$), the external source signal is made zero (i.e., set $I_s = 0$) and V_o is replaced with V.

Applying KVL to the output side, we get

$$I = \frac{V - R_m V_i}{R_o}$$

The input current is written as

$$I_i = -I_f = -\beta V \quad (\text{with } I_s = 0)$$

Substituting I_i in the above KVL equation, we get

$$I = \frac{V + \beta R_m V}{R_o} = \frac{V(1 + \beta R_m)}{R_o}$$

The output resistance with feedback is given as

$$R_{of} = \frac{V}{I} = \frac{R_o}{1 + \beta R_m}$$

where R_m represents the open-circuit transresistance without taking the load R_L into account.

The output resistance with feedback R'_{of} including R_L as part of the amplifier is given by

$$R'_{of} = R_{of} \| R_L$$

Therefore,
$$R'_{of} = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{\frac{R_o}{1+\beta R_m} \cdot R_L}{\frac{R_o}{1+\beta R_m} + R_L}$$

$$= \frac{R_o R_L}{R_o + R_L + \beta R_m R_L}$$

Dividing numerator and denominator by $(R_o + R_L)$, we get

$$R'_{of} = \frac{R_o R_L / (R_o + R_L)}{1 + \left[\beta R_m R_L / (R_o + R_L)\right]}$$

where $R'_o = \frac{R_o R_L}{R_o R_L}$ and $R_M = \frac{R_m R_L}{R_o + R_L}$

$$R'_{of} = \frac{R'_o}{1 + \beta R_M}$$

where R_M indicates the open-circuit transresistance taking the load R_L into account.

➤ ***Current-shunt Feedback*** The current-shunt feedback topology is shown in Fig. 6.15. For finding R_{of}, R_L is disconnected (i.e., $R_L = \infty$), the external source signal is made zero (i.e., set $I_S = 0$) and V_o is replaced with V.

Applying KCL to the output node, we get

$$I = \frac{V}{R_o} - A_i I_i$$

The input current is written as

$$I_i = -I_f = -\beta I_o = +\beta I \quad (\text{with } I_s = 0 \text{ and } I = -I_o)$$

Substituting I_i in the above KCL equation, we get

$$I = \frac{V}{R_o} - \beta A_i I$$

$$I(1 + \beta A_i) = \frac{V}{R_o}$$

The output resistance with feedback is given as

$$R_{of} = \frac{V}{I} = R_o (1 + \beta A_i)$$

where A_i represents the short-circuit current gain without taking the load R_L into account.

The output resistance with feedback R'_{of} including R_L as part of the amplifier is given by

$$R'_{of} = R_{of} \| R_L$$

Therefore, $$R'_{of} = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{R_o (1 + \beta A_i) R_L}{R_o (1 + \beta A_i) + R_L} = \frac{R_o R_L (1 + \beta A_i)}{R_o + R_L + \beta A_i R_o}$$

Dividing numerator and denominator by $(R_o + R_L)$, we get

$$R'_{of} = \frac{\frac{R_o R_L (1 + \beta A_i)}{R_o + R_L}}{1 + \frac{\beta A_i R_o}{R_o + R_L}} = R'_o \frac{1 + \beta A_i}{1 + \beta A_I}$$

where $R'_o = \frac{R_o R_L}{R_o + R_L}$ and $A_I = \frac{A_i R_o}{R_o + R_L}$

➤ *Current-series Feedback*

The current-series feedback topology is shown in Fig. 6.14. For finding R_{of}, R_L is disconnected (i.e., $R_L = \infty$), the external source signal is made zero (i.e., set $V_s = 0$) and V_o is replaced with V.

Applying KCL to the output node, we get

$$I = \frac{V}{R_o} - G_m V_i$$

The input voltage is written as

$$V_i = V_f = -\beta I_0 = \beta I \quad (\text{with } V_s = 0 \text{ and } I = -I_o)$$

Substituting V_i in the above KCL equation, we get

$$I = \frac{V}{R_o} - \beta G_m I$$

$$I(1 + \beta G_m) = \frac{V}{R_o}$$

The output resistance with feedback is given as

$$R_{of} = \frac{V}{I} = R_o (1 + \beta G_m)$$

where G_m represents the short-circuit transconductance without taking the load R_L into account.

The output resistance with feedback R'_{of} including R_L as part of the amplifier is given by

$$R'_{of} = R_{of} \| R_L$$

Therefore, $$R'_{of} = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{R_o (1 + \beta G_m) R_L}{(1 + \beta G_m) + R_L} = \frac{R_o R_L (1 + \beta G_m)}{R_o + R_L + \beta G_m R_o}$$

Dividing numerator and denominator by $(R_o + R_L)$, we get

$$R'_{of} = \frac{\frac{R_o R_L (1 + \beta G_m)}{R_o + R_L}}{1 + \frac{\beta G_m R_o}{R_o + R_L}} = R'_o \frac{1 + \beta G_m}{1 + \beta G_M}$$

where $R'_o = \dfrac{R_o R_L}{R_o + R_L}$ and $G_M = \dfrac{G_m R_o}{R_o + R_L}$

The characteristics of the four feedback topologies are summarized in Table 6.3.

Table 6.3 *Effect of negative feedback on amplifier characteristics*

Characteristic	Current-series	Voltage -series	Voltage-shunt	Current-shunt
Input resistance	Increases	Increases	Decreases	Decreases
Output resistance	Increases	Decreases	Decreases	Increases
Voltage gain	Decreases	Decreases	Decreases	Decreases
Bandwidth	Increases	Increases	Increases	Increases
Nonlinear distortion	Decreases	Decreases	Decreases	Decreases
Noise	Decreases	Decreases	Decreases	Decreases

EXAMPLE 6.6

A voltage-series negative feedback amplifier has a voltage gain without feedback of $A = 500$, input resistance $R_i = 3$ kΩ, output resistance $R_o = 20$ kΩ, and feedback ratio $\beta = 0.01$. Calculate the voltage gain A_f, input resistance R_{if} and output resistance R_{of} of the amplifier with feedback.

Solution Given $A = 500$, $R_i = 3$ kΩ, $R_o = 20$ kΩ, and $\beta = 0.01$

Voltage gain, $A_f = \dfrac{A}{1 + A\beta} = \dfrac{500}{1 + 500 \times 0.01} = \dfrac{500}{6} = 83.33$

Input resistance, $R_{if} = (1 + A\beta)\, R_i = (1 + 500 \times 0.01) \times 3 \times 10^3 = 18$ kΩ

Output resistance $R_{of} = \dfrac{R_o}{1 + A\beta} = \dfrac{20 \times 10^3}{(1 + 500 \times 0.01)} = 3.33$ kΩ

6.8 METHOD OF ANALYSIS OF FEEDBACK AMPLIFIERS

For analyzing the feedback amplifier, it is necessary to go through the following steps.

➤ *Step 1: Identify Topology (Type of Feedback)*

- **To find the type of sampling network**
  - (i) By shorting the output if feedback signal becomes zero, it is called "voltage sampling".
  - (ii) By opening the output loop if feedback signal becomes zero, it is called "current sampling".

- **To find the type of mixing network**
  - (i) If the feedback signal is subtracted from the externally applied signal as a voltage in the input loop, it is called "series mixing".
  - (ii) If the feedback signal is subtracted from the externally applied signal as a current in the loop, it is called "shunt mixing".

Thus, by finding the type of sampling network and mixing network, type of feedback amplifier can be determined. For example, if amplifier uses a voltage sampling and series mixing, then it is called a voltage-series amplifier.

➤ ***Step 2: To Find the Input Circuit***

(a) For voltage sampling, the output voltage is made zero by shorting the output.
(b) For current sampling, the output current is made zero by opening the output loop.

➤ ***Step 3: To Find the Output Circuit***

(a) For series mixing, the input current is made zero by opening the input loop.
(b) For shunt mixing, the input voltage is made zero by shorting the input.

▪ **Step 2 and Step 3** Ensure that the feedback is reduced to zero without altering the loading on the basic amplifier.

➤ ***Step 4:*** Optional. Replace each active device by its *h*-parameter model at low frequency.

➤ ***Step 5:*** Find, A, the open-loop gain (gain without feedback) of the amplifier.

➤ ***Step 6:*** Indicate X_f (feedback voltage or feedback current) and X_o (output voltage or output current) on the circuit and evaluate $\beta = X_f/X_o$.

➤ ***Step 7:*** From A and β, find D, A_f, R_{if}, R_{of}, and R'_{of}.

6.9 VOLTAGE-SERIES FEEDBACK AMPLIFIER

Three examples of the voltage-series topology, viz., (i) BJT common-collector amplifier (emitter follower), (ii) FET common-drain amplifier (source follower), and (iii) voltage-series feedback pair are discussed in this section.

6.9.1 Emitter Follower

Figure 6.17(a) shows the BJT emitter follower circuit. The feedback signal is the voltage V_f across R_E and the sampled signal is V_o across R_E. This configuration conforms to voltage-series feedback topology, as the sampled signal is taken directly from the output node and the feedback signal is applied in series with the external excitation. Using the analysis steps, approximate expressions for voltage gain, input resistance and output resistance with feedback are obtained.

Now the basic amplifier without feedback is drawn.

➤ ***To Find the Input Circuit*** Set $V_o = 0$, and Hence, V_s in series with R_s, appears between base B and emitter E.

➤ ***To Find the Output Circuit*** Set $I_i = I_b = 0$ (i.e., the input loop is opened), and hence, R_E appears only in the output loop.

Following the above rules, the circuit shown in Fig. 6.17(b) is obtained. Figure 6.17(c) shows the equivalent circuit after replacing the transistor by its low-frequency approximate *h*-parameter model. In the Fig. 6.17(c),

V_f and V_o are equal and hence, $\beta = V_f/V_o = 1$. This topology stabilizes the voltage gain. Since R_s is considered as part of the amplifier, then $V_i = V_s$, and the voltage gain without feedback is given by

$$A_V = \frac{V_o}{V_i} = \frac{h_{fe} I_b R_E}{V_s} = \frac{h_{fe} R_E}{R_s + h_{ie}}$$

where $V_s = I_b (R_s + h_{ie})$.

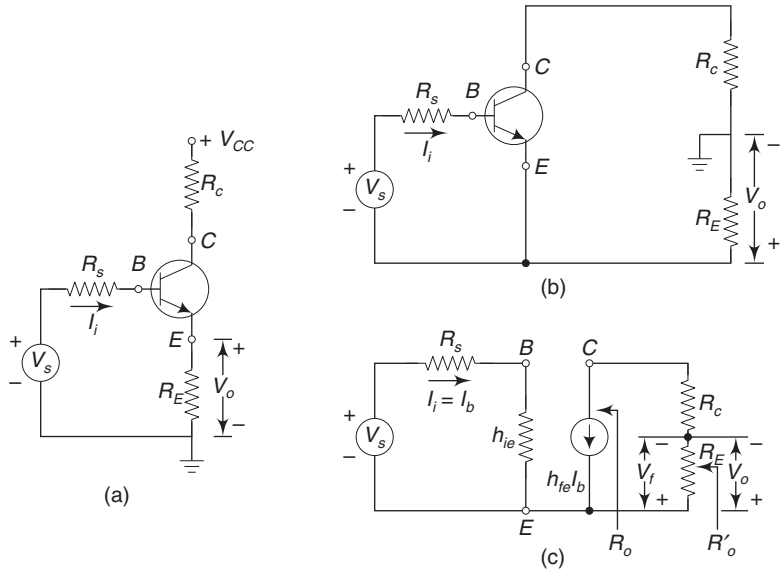


Fig. 6.17 *(a) BJT emitter follower (b) Amplifier without feedback (c) Low-frequency equivalent circuit*

The desensitivity is given by

$$D = 1 + \beta A_V = 1 + \frac{h_{fe} R_E}{R_s + h_{ie}} = \frac{R_s + h_{ie} + h_{fe} R_E}{R_s + h_{ie}}$$

where $\beta = \dfrac{V_f}{V_o} = 1$. Then, the voltage gain with feedback can be written as

$$A_{Vf} = \frac{A_V}{D} = \frac{h_{fe} R_E}{R_s + h_{ie} + h_{fe} R_E}$$

If $h_{fe} R_E >> R_s + h_{ie}$, then $A_{Vf} \approx 1$. This unity gain shows that it is an emitter-follower circuit.

From Fig. 6.17(c), the input resistance without feedback is given by

$$R_i = R_s + h_{ie}$$

Hence, for voltage-series feedback amplifier, the input resistance with feedback increases due to series mixing at the input and it is given by

$$R_{if} = R_i D = (R_s + h_{ie}) \times \frac{R_s + h_{ie} + h_{fe} R_E}{(R_s + h_{ie})} = R_s + h_{ie} + h_{fe} R_E$$

From Fig. 6.17(c), the output resistance of the amplifier with feedback, without considering the external load resistance ($R_L = R_E$) is given by

$$R_{of} = \frac{R_o}{1 + \beta A_v} = \frac{\infty}{\infty}$$

where $R_o = \infty$ and $A_v = \lim_{R_L \to \infty} A_V = \infty$. This indeterminacy can be resolved by first evaluating R'_{of} and then apply the limit $R_L \to \infty$.

The output resistance of the amplifier with feedback by considering the external load, can be written as

$$R'_{of} = \frac{R'_o}{D} = \frac{R_E(R_s + h_{ie})}{R_s + h_{ie} + h_{fe}R_E}$$

where $R'_o = R_L = R_E$.

$$R_{of} = \lim_{R_L \to \infty} R'_{of} = \frac{R_s + h_{ie}}{h_{fe}}$$

Hence, the feedback desensitizes voltage gain with respect to changes in h_{fe} and it increases the input resistance and decreases the output resistance for voltage-series feedback topology.

EXAMPLE 6.7

In the BJT emitter follower circuit shown in Fig. 6.17(a), the circuit-component values are R_s = 600 Ω, R_C = 4.7 kΩ, R_E = 2 kΩ, h_{fe} = 80, h_{ie} = 5 kΩ. Calculate A_{Vf}, R_{if}, R_{of}, and R'_{of}.

Solution

$$A_V = \frac{h_{fe}R_E}{R_s + h_{ie}} = \frac{80 \times 2 \times 10^3}{600 + 5 \times 10^3} = 28.57$$

The desensitivity is given by

$$D = 1 + \beta A_V = \frac{R_s + h_{ie} + h_{fe}R_E}{R_s + h_{ie}} = \frac{600 + 5 \times 10^3 + 80 \times 2 \times 10^3}{600 + 5 \times 10^3} = 29.57$$

where $\beta = \frac{V_f}{V_o} = 1$.

Then, the voltage gain with feedback can be written as

$$A_{Vf} = \frac{A_V}{D} = \frac{28.57}{29.57} = 0.966 \approx 1$$

This unity gain shows that it is an emitter-follower circuit.

From Fig. 6.17 (c), the input resistance without feedback is given by

$$R_i = R_s + h_{ie} = 600 + 5 \times 10^3 = 5.6 \text{ k}\Omega$$

Hence, for voltage-series feedback amplifier, the input resistance with feedback increases due to series mixing at the input and it is given by

$$R_{if} = R_i D = 5.6 \times 10^3 \times 29.57 = 165.59 \text{ k}\Omega$$

From Fig. 6.17(c), the output resistance of the amplifier with feedback, without considering the external load resistance ($R_L = R_E$) is given by

$$R_{of} = \frac{R_o}{1 + \beta A_v} = \frac{\infty}{\infty}$$

where $R_o = \infty$ and $A_v = \lim_{R_L \to \infty} A_V = \infty$. This indeterminacy can be resolved by first evaluating R'_{of} and then apply the limit $R_L \to \infty$.

The output resistance of the amplifier with feedback by considering the external load, can be written as

$$R'_{of} = \frac{R'_o}{D} = \frac{2 \times 10^3}{29.57} = 67.64\ \Omega$$

where $R'_o = R_L = R_E$.

This shows that the output resistance decreases due to voltage sampling at the output.

$$R_{of} = \lim_{R_L \to \infty} R'_{of} = \frac{600 + 5 \times 10^3}{80} = 70\ \Omega$$

6.9.2 FET Source Follower

Figure 6.18(a) shows the FET source follower circuit. The feedback signal is the voltage V_f across R_s and the sampled signal is the output voltage V_o across R_s. This configuration corresponds to voltage-series feedback topology, as the sampled signal is taken directly from the output node and the feedback signal is applied in series with the external excitation. Using the analysis steps, approximate expressions for voltage gain, input resistance, and output resistance with feedback are obtained.

Now the basic amplifier without feedback is drawn.

➤ ***To Find the Input Circuit*** Set $V_o = 0$ and hence, V_s appears directly between G and S at the input side.

➤ ***To Find the Output Circuit*** Set $I_i = 0$ (i.e., the input loop is opened), and hence, R_s appears only in output loop.

Figure 6.18(b) shows the basic amplifier without feedback and Fig. 6.18(c) shows equivalent circuit after replacing the FET by its low-frequency model. In Fig. 6.18(c), V_f and V_0 are equal and Hence, $\beta = V_f/V_o = 1$. This topology stabilizes the voltage gain.

From Fig. 6.18(c), the voltage gain without feedback is given by

$$A_V = \frac{V_o}{V_i} = \frac{g_m V_{gs} r_d R_s}{(r_d + R_s) V_s} = \frac{\mu R_s}{r_d + R_s}$$

where $\mu = g_m \times r_d$ and $V_s = V_{gs}$.

The desensitivity is given by $D = 1 + \beta A_V = 1 + \dfrac{\mu R_s}{r_d + R_s} = \dfrac{r_d + (1 + \mu) R_s}{r_d + R_s}$

where $\beta = 1$. Then, the voltage gain with feedback can be written as

$$A_{Vf} = \frac{A_V}{D} = \frac{\mu R_s}{r_d + (1 + \mu) R_s}$$

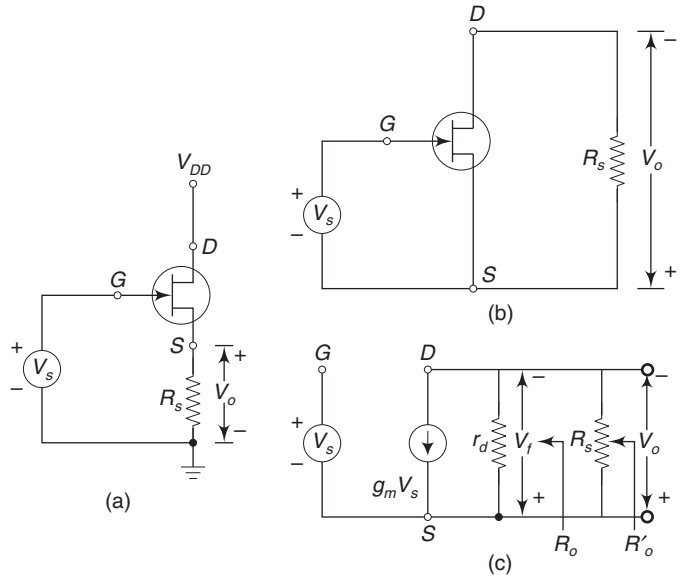


Fig. 6.18 *(a) FET source follower (b) Amplifier without feedback (c) Low-frequency equivalent circuit*

The input impedance of FET is infinite, i.e., $R_i = \infty$, and hence, $R_{if} = R_i D = \infty$. From Fig. 6.18(c), the output resistance of the amplifier with feedback without considering the external load resistance ($R_L = R_s$) is given by

$$R_{of} = \frac{R_o}{1 + \beta A_v} = \frac{r_d}{1 + \mu}$$

where $R_o = r_d$ and $A_v = \lim_{R_L \to \infty} A_V = \mu$

The output resistance of the amplifier with feedback by considering the external load, can be written as

$$R'_{of} = \frac{R'_o}{D} = \frac{R_s r_d}{R_s + r_d} \times \frac{r_d + R_s}{r_d + (\mu + 1) R_s} = \frac{R_s r_d}{r_d + (\mu + 1) R_s}$$

where $R'_o = R \parallel r_d$.

Note that the output resistance without load can also be obtained by, $R_{of} = \lim_{R_L \to \infty} R'_{of} = \frac{r_d}{1 + \mu}$.

EXAMPLE 6.8

For voltage-series feedback amplifier shown in Fig. 6.18 (a), R_s = 5 kΩ, r_d = 40 kΩ, μ = 40. Determine A_{Vf}, R_{if}, R_{of} and R'_{of}.

Solution The voltage gain without feedback is given by

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_s}{r_d + R_s} = \frac{40 \times 5 \times 10^3}{40 \times 10^3 + 5 \times 10^3} = 4.44$$

The desensitivity is given by

$$D = 1 + \beta A_V = 1 + 4.44 = 5.44$$

where $\beta = 1$.

Then, the voltage gain with feedback can be written as

$$A_{Vf} = \frac{A_V}{D} = \frac{4.44}{5.44} = 0.816$$

The input impedance of *FET* is infinite, i.e., $R_i = \infty$, and hence, $R_{if} = R_i D = \infty$.

The output resistance of the amplifier with feedback, without considering the external load resistance ($R_L = R_s$) is given by

$$R_{of} = \frac{R_o}{1 + \beta A_v} = \frac{r_d}{1 + \mu} = \frac{40 \times 10^3}{1 + 4} = 975\ \Omega$$

where $R_o = r_d$, and $A_v = \lim_{R_L \to \infty} A_V = \mu$.

The output resistance of the amplifier with feedback, by considering the external load, can be written as

$$R'_{of} = \frac{R'_o}{D} = \frac{R_s r_d}{R_s + r_d} \times \frac{1}{D} = \frac{5 \times 10^3 \times 40 \times 10^3}{5 \times 10^3 + 40 \times 10^3} \times \frac{1}{5.44} = \frac{4.44 \times 10^3}{5.44} = 816.2\ \Omega$$

where $R'_o = R_s \parallel r_d$.

6.9.3 Voltage-Series Feedback Pair

Figure 6.19 (a) shows two CE stages connected in cascade with voltage gains A_{V1} and A_{V2} respectively, in which the output of the second stage is returned through the feedback network $R_1 - R_2$ in opposition to the input signal V_s. As the sampled signal is taken directly from the output node and the feedback signal is applied in series with the external excitation, this is another case of voltage-series feedback topology.

Now, the basic amplifier without feedback is drawn.

➤ ***To Find the Input Circuit*** Set $V_o = 0$ and hence, R_2 appears in parallel with R_1 between the emitter of first transistor and ground.

➤ ***To Find the Output Circuit*** Set $I_i = 0$ and hence, R_1 is placed in series with R_2 between the collector of second transistor and ground.

Figure 6.19(b) shows equivalent circuit without external feedback, including the loading of R_2. This topology stabilizes the voltage gain.

From Fig. 6.19(b), the feedback factor is given by

$$\beta = \frac{V_f}{V_o} = \frac{R_1}{R_1 + R_2}$$

The circuit of Fig. 6.19(c) shows a two-stage CE amplifier, with voltage-series feedback, by connecting the second transistor collector to the first transistor emitter through the voltage divider resistors, R_1 and R_2. For this amplifier, the voltage gain A_{Vf} is given approximately by $1/\beta$, and is thus, stabilized against changes in temperature and replacement of transistors.

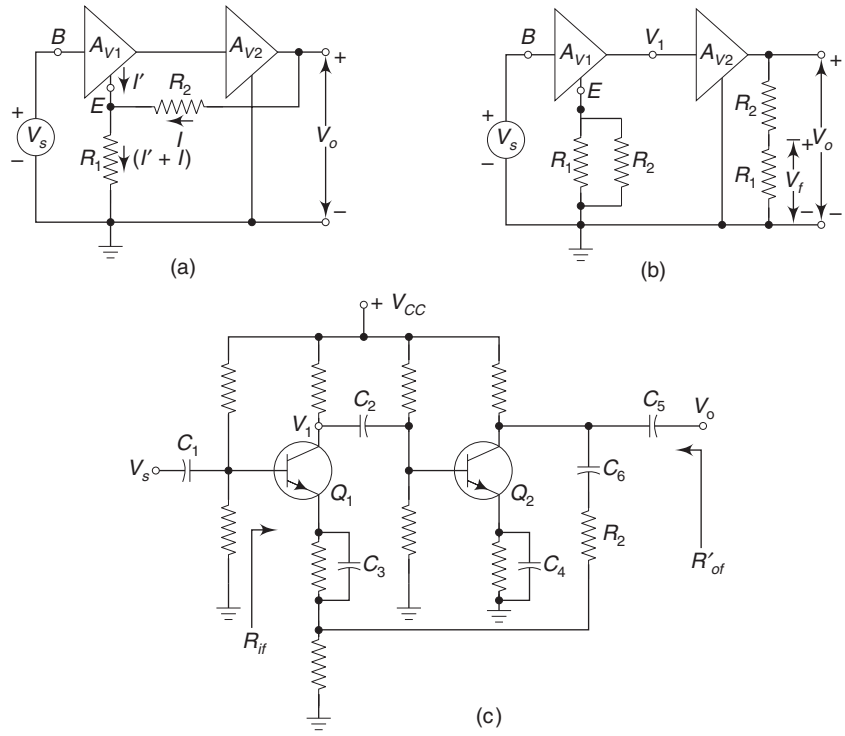


Fig. 6.19 *(a) Voltage-series feedback pair (b) Equivalent circuit, without feedback (c) Two-stage CE amplifier with voltage-series feedback*

EXAMPLE 6.9

Find the voltage gain, feedback factor, input resistance and output resistance of a series-shunt pair type two stage feedback amplifier using transistors with $h_{fe} = 90$ and $h_{ie} = 2$ kΩ, shown in Fig. 6.20.

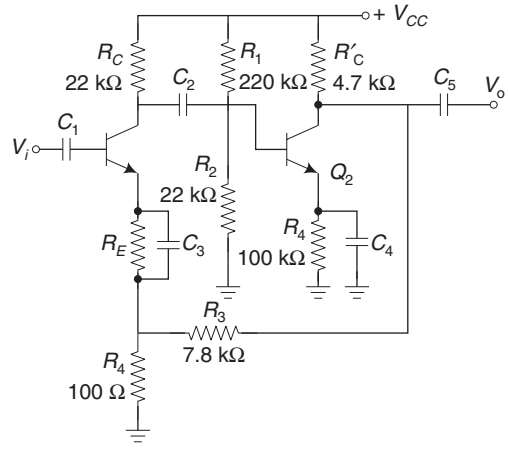


Fig. 6.20

Solution Given $h_{fe} = h_{fe1} = h_{fe2} = 99$, $h_{ie} = h_{ie1} = 2\ \text{k}\Omega$, $R_C = 22\ \text{k}\Omega$
$R_4 = 100\ \Omega$, $R_1 = 220\ \text{k}\Omega$, $R_2 = 22\ \text{k}\Omega$, $R'_C = 4.7\ \text{k}\Omega$ and $R_3 = 7.8\ \text{k}\Omega$.

(a) *To determine voltage gain:*

$$A_{V1} = -\frac{h_{fe} \times R_{o1}}{h_{ie}}$$

where $R_{o1} = R_C \parallel (R_1 \parallel R_2) \parallel h_{ie2}$

$$A_{V1} = 22 \times 10^3 \parallel (220 \times 10^3 \parallel 22 \times 10^3) \parallel 2 \times 10^3$$
$$= 1.67\ \text{k}\Omega$$

Therefore, $$A_{V1} = -\frac{99 \times 1.67 \times 10^3}{2 \times 10^3} = -82.7$$

$$A_{V2} = -\frac{h_{fe} \times R_{o2}}{h_{ie}}$$

where $R_{o2} = R'_C \parallel (R_3 + R_4) = 4.7 \times 10^3 \parallel (7.8 \times 10^3 + 100) = 2.95\ \text{k}\Omega$

Therefore, $$A_{V2} = -\frac{99 \times 2.95 \times 10^3}{2 \times 10^3} = -146$$

Overall gain of the cascaded amplifier without feedback

$$A_V = A_{V1} \times A_{V2} = (-82.7) \times (-146) = 13{,}155$$

(b) *Feedback factor:*

$$\beta = \frac{R_4}{R_3 + R_4} = \frac{100}{7.8 \times 10^3 + 100} = \frac{1}{79}$$

(c) *Input resistance with feedback:*

$$R_{if} = R_i\,(1 + \beta A_V), \text{ where } R_i = h_{ie1} = 2\ \text{k}\Omega$$

Therefore, $$R_{if} = 2 \times 10^3 \left(1 + \frac{1}{79} \times 13{,}155\right) = 335\ \text{k}\Omega$$

(d) *Output resistance with feedback:*

$$R_{of} = \frac{R_{o2}}{1 + \beta A_V}$$

where $R_{o2} = R'_C \parallel (R_3 + R_4) = 4.7 \times 10^3 \parallel (7.8 \times 10^3 + 100) = 2.95\ \text{k}\Omega$

Therefore, $$R_{of} = \frac{2.95 \times 10^3}{1 + \left(\frac{1}{79} \times 13{,}155\right)} = 17.61\ \Omega$$

(e) *Voltage gain with feedback:*

$$A_{Vf} = \frac{A_V}{1 + \beta A_V} = \frac{13{,}155}{1 + \left(\frac{1}{79} \times 13{,}155\right)} = 78.53$$

6.10 CURRENT-SERIES FEEDBACK AMPLIFIER

Two examples of current-series feedback topology: (i) common emitter amplifier with a resistor R_E in the emitter terminal, and (ii) FET common-source amplifier with a resistor R_s in the source lead are discussed in this section.

6.10.1 BJT CE Amplifier with Emitter Resistor R_E

Figure 6.21(a) shows a CE amplifier with emitter resistor R_E. The feedback signal is the voltage V_f across R_E and the sampled signal is the load current I_o. This configuration corresponds to current-series feedback topology, as the sampled signal is taken from the output loop and the feedback signal is applied in series with the external excitation.

To draw the basic amplifier without feedback as shown in Fig. 6.21(b), the input circuit of the amplifier is obtained by opening the output loop. Hence, R_E appears in the input side. Similarly, the output circuit is obtained by opening the input loop, and this place R_E again in the output side.

The resultant equivalent circuit is given in Fig.6.21(c) after replacing the transistor by its low-frequency h-parameter model. No ground can be indicated in this circuit because by doing so, would again couple the input to the output via R_E, i.e., it would reintroduce feedback, but taking the loading of the β network into account. This topology stabilizes the transconductance gain G_M. Since the feedback voltage V_f appears across R_E in the output circuit, then, from Fig. 6.21(c),

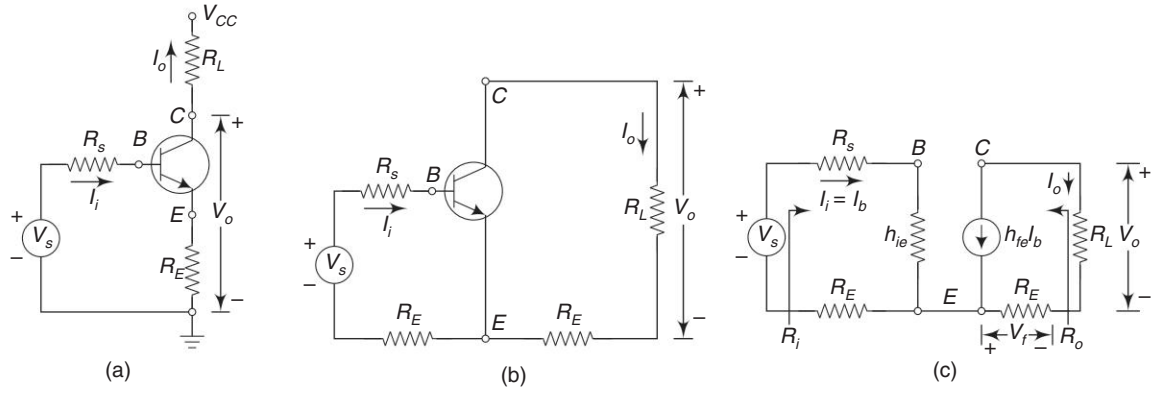


Fig. 6.21 *(a) CE amplifier with unbypassed emitter resistor R_E (b) Amplifier without feedback and (c) Low-frequency equivalent circuit*

$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_E}{I_o} = -R_E$$

Since the input signal V_t without feedback is equal to V_s, then the transconductance without feedback is given by

$$G_M = \frac{I_o}{V_i} = \frac{-h_{fe} I_b}{V_s} = \frac{-h_{fe}}{R_s + h_{ie} + R_E}$$

where $$V_s = I_b (R_s + h_{ie} + R_E)$$

The desensitivity is given by

$$D = 1 + \beta G_M = 1 + \frac{h_{fe} R_E}{R_s + h_{ie} + R_E} = \frac{R_s + h_{ie} + (1 + h_{fe}) R_E}{R_s + h_{ie} + R_E}$$

Then, the transconductance with feedback can be written as

$$G_{Mf} = \frac{G_M}{D} = \frac{-h_{fe}}{R_s + h_{ie} + (1 + h_{fe}) R_E}$$

Note that if $(1 + h_{fe})\, R_E >> R_s + h_{ie}$, and since $h_{fe} >> 1$, then $G_{Mf} \approx -1/R_E \approx 1/\beta$. If R_E is a stable resistor, the transconductance gain with feedback is stabilized (desensitized). The load current is given by

$$I_o = G_{Mf} V_s = \frac{-h_{fe} V_s}{R_s + h_{ie} + (1 + h_{fe}) R_E} \approx -\frac{V_s}{R_E}$$

Under the conditions, $(1 + h_{fe})\, R_E >> R_s + h_{ie}$ and $h_{fe} >> 1$, the load current is directly proportional to the input voltage, and this current depends only upon R_E and not upon any other circuit or transistor parameter. The voltage gain is given by

$$A_{Vf} = \frac{I_o R_L}{V_s} = G_{Mf} R_L = \frac{-h_{fe} R_L}{R_s + h_{ie} + (1 + h_{fe}) R_E}$$

From Fig. 6.21(c), the input resistance without feedback is given by

$$R_i = R_s + h_{ie} + R_E$$

Hence, for current-series feedback amplifier, the input resistance with feedback increases due to series mixing at the input and it is given by

$$R_{if} = R_i D = R_s + h_{ie} + (1 + h_{fe})\, R_E$$

Since R_E is considered to be part of the amplifier, it appears as a part of the input resistance. From Fig. 6.21(c), $R_0 = \infty$ and the output resistance of the amplifier with feedback, without considering the external load resistance is given by

$$R_{of} = R_o\, (1 + \beta G_m) = \infty$$

The output resistance of the amplifier with feedback, by considering the external load, can be written as

$$R'_{of} = R_L \parallel R_{of} = R_L$$

Alternatively, it can also be written as

$$R'_{of} = R'_o \frac{1 + \beta G_m}{1 + \beta G_M}$$

Since G_m represents the short-circuit transconductance, then $G_m = \lim_{R_L \to 0} G_M$. However, G_M is independent of R_L and hence, $G_m = G_M$ and $R'_{of} = R'_o = R_L$.

EXAMPLE 6.10

For current series feedback amplifier using BJT shown in Fig. 6.21(a), R_E = 1.2 kΩ, R_s = 1 kΩ, R_L = 2.2 kΩ, h_{ie} = 1.1 kΩ, h_{fe} = 50. Determine G_{Mf}, A_{Vf}, R_{if}, R_{of}, and R'_{of}.

Solution The transconductance without feedback is given by

$$G_M = \frac{-h_{fe}}{R_s + h_{ie} + R_E} = \frac{-50}{3.3 \times 10^3} = -0.015$$

The desensitivity is given by

$$D = 1 + \beta G_M = 1 + (-1.2 \times 10^3) \times (-0.015) = 19$$

where $\beta = \frac{V_f}{I_o} = -R_E$.

Then, the transconductance with feedback can be written as

$$G_{Mf} = \frac{G_M}{D} = \frac{-0.015}{19} = -0.789 \times 10^{-3}$$

The voltage gain is given by

$$A_{Vf} = \frac{I_0 R_L}{V_s} = G_{Mf} R_L = -0.789 \times 10^{-3} \times 2.2 \times 10^3 = -1.73$$

The input resistance without feedback is given by

$$R_i = R_s + h_{ie} + R_E = 3.3 \text{ k}\Omega$$

For current-series feedback amplifier, the input resistance with feedback increases due to series mixing at the input and it is given by

$$R_{if} = R_i D = 3.3 \times 10^3 \times 19 = 62.7 \text{ k}\Omega$$

For BJT, we know that, the output resistance, $R_0 = \infty$.

The output resistance of the amplifier with feedback, without considering the external load resistance is given by

$$R_{of} = R_o (1 + \beta G_m) = \infty$$

The output resistance of the amplifier with feedback by considering the external load, can be written as

$$R'_{of} = R_{of} \| R_L = \infty \| 2.2 \times 10^3 = 2.2 \text{ k}\Omega$$

Alternatively, it can also be written as

$$R'_{of} = R'_o \frac{1 + \beta G_m}{1 + \beta G_M} = 2.2 \text{ k}\Omega$$

Since G_m represents the short-circuit transconductance, then $G_m = \lim_{R_L \to 0} G_M$. However, G_M is independent of R_L and hence, $G_m = G_M$ and $R'_{of} = R'_o = R_L$.

6.10.2 FET CS Amplifier with Source Resistor R_s

Figure 6.22(a) shows a CS amplifier with source resistor R_s. Following the same procedure as we did for the BJT amplifier, the basic amplifier without feedback is drawn as shown in Fig. 6.22(b) and then the FET by its low-frequency model is replaced as shown in Fig. 6.22(c).

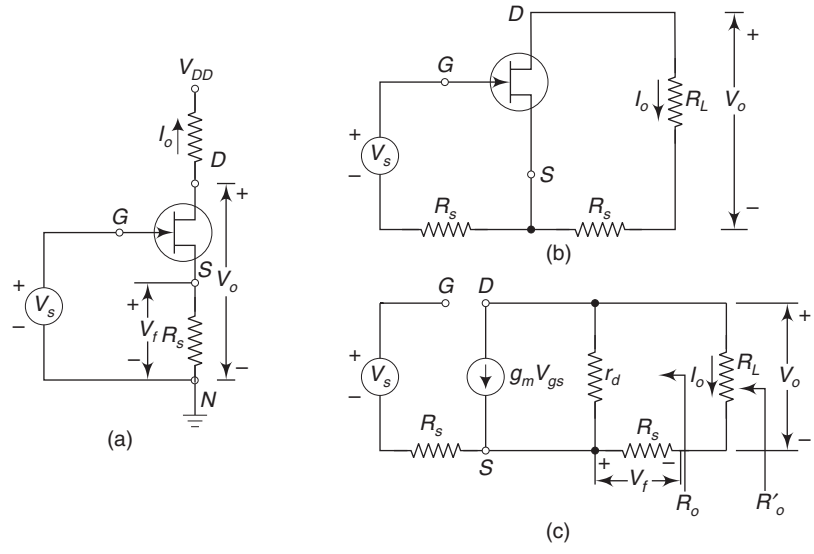


Fig. 6.22 *(a) FET amplifier with source resistor R_s (b) Amplifier without feedback (c) Low-frequency equivalent circuit*

Without feedback, $V_i = V_s$ and the transconductance without feedback is given by

$$G_M = \frac{I_o}{V_i} = \frac{I_o}{V_s} = \frac{-g_m V_{gs} r_d}{r_d + R_L + R_s} \times \frac{1}{V_s} = \frac{-\mu}{r_d + R_L + R_s}$$

where $\mu = g_m \times r_d$ and $V_s = V_{gs}$.

The desensitivity is given by

$$D = 1 + \beta G_M = 1 + \frac{\mu R_s}{r_d + R_L + R_s} = \frac{r_d + R_L + (\mu + 1) R_s}{r_d + R_L + R_s}$$

where $\beta = \dfrac{V_f}{I_o} = -R_s$.

Then, the transconductance with feedback can be written as

$$G_{Mf} = \frac{G_M}{D} = \frac{-\mu}{r_d + R_L + (\mu + 1) R_s}$$

Since $R_i = \infty$, then $R_{if} = R_i \times D = \infty$.

From Fig. 6.22(c), we see that, $R_o = r_d + R_s$.

To calculate R_{of}, we need G_m and it is obtained by, $G_m = \lim_{R_L \to 0} G_M$. Since β is independent of R_L, then

$$1 + \beta G_m = \lim_{R_L \to 0} D = \frac{r_d + (\mu + 1) R_s}{r_d + R_s}$$

The output resistance of the amplifier with feedback, without considering the external load resistance is given by

$$R_{of} = R_o\,(1 + \beta G_m) = (r_d + R_s)\,\frac{r_d + (\mu + 1)R_s}{r_d + R_s} = r_d + (\mu + 1)R_s$$

The output resistance of the amplifier with feedback, by considering the external load, can be written as

$$R'_{of} = R_{of} \parallel R_L = \frac{R_L \times (r_d + (\mu + 1)R_s)}{R_L + r_d + (\mu + 1)R_s}$$

The same result can also be obtained with $R'_o = R_o \parallel R_L = (r_d + R_s) \parallel R_L$. Thus,

$$\begin{aligned} R'_{of} &= R'_o\,\frac{1 + \beta G_m}{D} \\ &= \frac{(r_d + R_s)R_L}{r_d + R_L + R_s} \times \frac{r_d + (\mu + 1)R_s}{r_d + R_s} \times \frac{r_d + R_L + R_s}{r_d + R_L + (\mu + 1)R_s} \\ &= \frac{R_L \times (r_d + (\mu + 1)R_s)}{r_d + R_L + (\mu + 1)R_s} \end{aligned}$$

which is equivalent to R_L in parallel with R_{of}.

EXAMPLE 6.11

For current-series feedback amplifier using FET shown in Fig. 6.22(a), $R_s = 1$ kΩ, $R_L = 4.7$ kΩ, $r_d = 40$ kΩ, $\mu = 50$. Determine G_{Mf}, A_{Vf}, R_{if}, R_{of} and R'_{of}.

Solution The transconductance without feedback is given by

$$G_M = \frac{-\mu}{r_d + R_L + R_s} = \frac{-50}{45.7 \times 10^3} = -1.09 \times 10^{-3}$$

The desensitivity is given by

$$D = 1 + \beta G_M = 1 + (-1 \times 10^3) \times (-1.09 \times 10^{-3}) = 2.09$$

where $\beta = -R_s$.

Then, the transconductance with feedback can be written as

$$G_{Mf} = \frac{G_M}{D} = \frac{-1.09 \times 10^{-3}}{2.09} = -0.52 \times 10^{-3}$$

The voltage gain is given by

$$A_{Vf} = \frac{I_o R_L}{V_s} = G_{Mf} R_L = -0.52 \times 10^{-3} \times 4.7 \times 10^3 = -2.44$$

For FET, we know that, input resistance, $R_i = \infty$, then $R_{if} = R_i \times D = \infty$.

The output resistance, $R_o = r_d + R_s = 41$ kΩ

To calculate R_{of}, we need G_m and it is obtained by, $G_m = \lim_{R_L \to 0} G_M$. Since β is independent of R_L, then

$$1 + \beta G_m = \lim_{R_L \to 0} D = \frac{r_d + (\mu + 1)R_s}{r_d + R_s}$$

The output resistance of the amplifier with feedback, without considering the external load resistance is given by,

$$R_{of} = R_o\,(1 + \beta G_m)$$

$$= (r_d + R_s)\,\frac{r_d + (\mu + 1)\,R_s}{r_d + R_s} = r_d + (\mu + 1)\,R_s$$

$$= 40 \times 10^3 + (1 + 50) \times 1 \times 10^3 = 91\ \text{k}\Omega$$

The output resistance of the amplifier with feedback, by considering the external load, can be written as

$$R'_{of} = R_{of} \parallel R_L = 91\ \text{k}\Omega \parallel 4.7\ \text{k}\Omega = 4.47\ \text{k}\Omega.$$

6.11 CURRENT-SHUNT FEEDBACK AMPLIFIER

Figure 6.23(a) shows two CE amplifiers in cascade with feedback taken from the second transistor emitter to the first transistor base through the feedback resistor R'.

The output voltage of Q_1 ($V_{o1} \approx V_{i2}$) is much larger than V_{i1} because of its high-voltage gain and it is 180° out of phase with V_{i1}. Due to emitter-follower action, the voltage across emitter of Q_2 (V_{e2}) is only slightly smaller than V_{i2} and these voltages are in phase. Hence, V_{e2} is larger in magnitude than V_{i1} and is 180° out of phase with V_{i1}. This configuration corresponds to current-shunt topology, as the sampled signal is taken from the output loop and the feedback signal is connected directly to the input node. Using the analysis steps, approximate expressions for current gain, input resistance, output resistance, and the voltage gain with feedback are obtained.

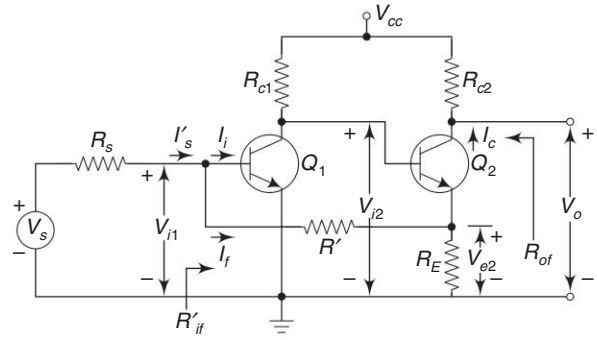


Fig. 6.23 (a) *Second transistor emitter to first transistor base feedback pair*

➤ ***To Draw the Basic Amplifier Without Feedback*** In Fig. 6.23(b), the input circuit of the amplifier is obtained by opening the output loop at the emitter of Q_2. This places R' in series with R_E from base to emitter of Q_1. The output circuit is obtained by shorting the input node (the base of Q_1). This places R' in parallel with R_E. In the circuit shown in Fig. 6.23(b), as the feedback signal is a current, the source is represented by a Norton's equivalent circuit with $I_s = V_s/R_s$.

From Fig. 6.23(a), neglecting the base current of Q_2 compared with the collector current and $V_{e2} >> V_{i1}$, the feedback current is given by

$$I_f = \frac{V_{i1} - V_{e2}}{R'} \approx \frac{V_{e2}}{R'} = \frac{(I_o - I_f)\,R_E}{R'}$$

Therefore,

$$I_f = \frac{R_E I_o}{R' + R_E} = \beta I_o$$

where $\beta = R_E/(R' + R_E)$. Since the feedback current is proportional to the output current, this

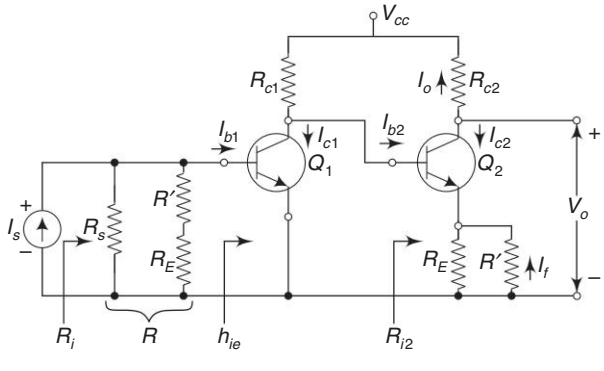


Fig. 6.23 (b) *Amplifier circuit without feedback*

circuit is an example of a current-shunt feedback amplifier. This topology stabilizes the transfer (current) gain. After replacing Q_1 and Q_2 by its low-frequency approximate h-parameter model, the transfer current gain without feedback is given by

$$A_I = \frac{-I_{c2}}{I_s} = \frac{-I_{c2}}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}} \frac{I_{b1}}{I_s}$$

where $\frac{-I_{c2}}{I_{b2}} = -h_{fe}, \frac{I_{c1}}{I_{b1}} = +h_{fe}, \frac{I_{b2}}{I_{b1}} = \frac{-R_{c1}}{R_{c1} + R_{i2}}$ and $\frac{I_{b1}}{I_s} = \frac{R}{R + h_{ie}}$

in which $R_{i2} = h_{ie} + (1 + h_{fe})\,(R_E \parallel R')$

$$R \equiv R_s \parallel (R' + R_E)$$

The desensitivity is given by

$$D = 1 + \beta A_I$$

where $\beta = R_E/(R' + R_E)$.

The current gain with feedback is given by

$$A_{If} = \frac{A_I}{D}$$

The voltage gain with feedback is written as

$$A_{Vf} = \frac{V_o}{V_s} = \frac{-I_{c2} R_{c2}}{I_s R_s} = \frac{A_{If} R_{c2}}{R_s} \approx \frac{R_{c2}}{\beta R_s}$$

where $A_{If} = \frac{1}{\beta}$ which shows the transfer current gain is stabilized. The input impedance without feedback seen by the current source is given by

$$R_i = R \parallel h_{ie}$$

Hence, for a current-shunt feedback amplifier, the input resistance with feedback decreases due to shunt mixing at the input, as seen by the current source and it is given by

$$R_{if} = \frac{R_i}{D}$$

The output resistance with feedback, without considering the load resistance R_{c2}, increases due to current sampling and it is given by

$$R_{of} = R_o\,(1 + \beta A_i) = \infty. \quad (\text{Since } h_{oe} = 0, \text{ then } R_o = \infty.)$$

From the A_I expression, we find that, it is independent of the load ($R_L = R_{c2}$).

Hence, $A_i = \lim_{R_{c2} \to 0} A_I = A_I$.

From Fig. 6.23(b), $R'_o = R_o \parallel R_{c2} = R_{c2}$. The output resistance with feedback, by considering the load resistance, can be written as

$$R'_{of} = R'_o \frac{1 + \beta A_i}{1 + \beta A_I} = R'_o = R_{c2}\,.$$

EXAMPLE 6.12

The circuit of Fig. 6.23(a) has the following parameters: R_{c1} = 3 kΩ, R_{c2} = 500 Ω, R_E = 50 Ω, $R' = R_s$ = 1.2 kΩ, h_{fe} = 50, h_{ie} = 1.1 kΩ, and $h_{re} = h_{oe} = 0$. Find A_{If}, A_{Vf}, R_{if}, R_{of}, and R'_{of}.

Solution Referring to Fig. 6.23(a), the current gain without feedback is given by

$$A_I = \frac{-I_{c2}}{I_s} = \frac{-I_{c2}}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}} \frac{I_{b1}}{I_s}$$

where $\frac{-I_{c2}}{I_{b2}} = -h_{fe} = -50, \ \frac{I_{c1}}{I_{b1}} = +h_{fe} = +50$

$$R_{i2} = h_{ie} + (1 + h_{fe})\,(R_E \parallel R')$$

$$= 1.14 + (51)\left(\frac{50 \times 1.2 \times 10^3}{1.25 \times 10^3}\right) = 3.55 \text{ k}\Omega$$

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1} + R_{i2}} = \frac{-3}{3 + 3.55} = -0.458$$

$$R \equiv R_s \parallel (R' + R_E)$$

$$= \frac{(1.2 \times 10^3)(1.25 \times 10^3)}{(1.2 + 1.25) \times 10^3} = 0.61 \text{ k}\Omega$$

$$\frac{I_{b1}}{I_s} = \frac{R}{R + h_{ie}} = \frac{0.61 \times 10^3}{(0.61 + 1.1) \times 10^3} = 0.358$$

Substituting all the above current ratio numerical values in A_I equation results in

$$A_I = (-50)\,(-0.458)\,(50)\,(0.358) = 410$$

The feedback factor is given by

$$\beta = \frac{R_E}{R' + R_E} = \frac{50}{1,250} = 0.04$$

The desensitivity is given by

$$D = 1 + \beta A_I = 1 + (0.040)\,(410) = 17.4$$

Current gain and voltage gain with feedback is given by

$$A_{If} = \frac{A_I}{D} = \frac{410}{17.4} = 23.6$$

$$A_{Vf} = \frac{V_o}{V_s} = \frac{-I_{c2} R_{c2}}{I_s R_s} = \frac{A_{If} R_{c2}}{R_s} = \frac{(23.6)(0.5)}{1.2} = 9.83$$

The approximate expression for voltage gain results in

$$A_{Vf} \approx \frac{R_{c2}}{\beta R_s} = \frac{0.5}{(0.04)(1.2)} = 10.4$$

which is in error by 6 percent with the actual value.

The input resistance without feedback, seen by the current source is

$$R_i = R \parallel h_{ie} = \frac{(0.61 \times 10^3)(1.1 \times 10^3)}{1.71 \times 10^3} = 0.394 \text{ k}\Omega$$

and the resistance R_{if} with feedback, seen by the current source is

$$R_{if} = \frac{R_i}{D} = \frac{394}{17.4} = 22.6\ \Omega$$

If R_{c2} is considered as an external load, then R_o is the resistance seen looking into the collector of Q_2. Since $h_{oe} = 0$, then $R_o = \infty$. The output resistance with feedback, without considering the load, is written as $R_{of} = R_o\,(1 + \beta A_i) = \infty$.

We know that, for current-shunt feedback, A_I is independent of the load ($R_L = R_{c2}$).

Hence, $A_i = \lim\limits_{R_{c2} \to 0} A_I = A_I$. Since $R'_o = R_o \parallel R_{c2} = R_{c2}$, the output resistance with feedback, by considering the load, $R'_{of} = R'_o \dfrac{1 + \beta A_i}{1 + \beta A_I} = R'_o = R'_{c2} = 500\ \Omega$.

6.12 VOLTAGE-SHUNT FEEDBACK AMPLIFIER

Figure 6.24(a) shows a common-emitter stage with a resistor R' connected from the output to the input. This configuration corresponds to voltage-shunt topology, as the sampled signal is taken directly from the output node and the feedback signal is connected directly to the input node. Using the analysis steps, approximate expressions for transresistance gain, input resistance, output resistance and the voltage gain with feedback are obtained.

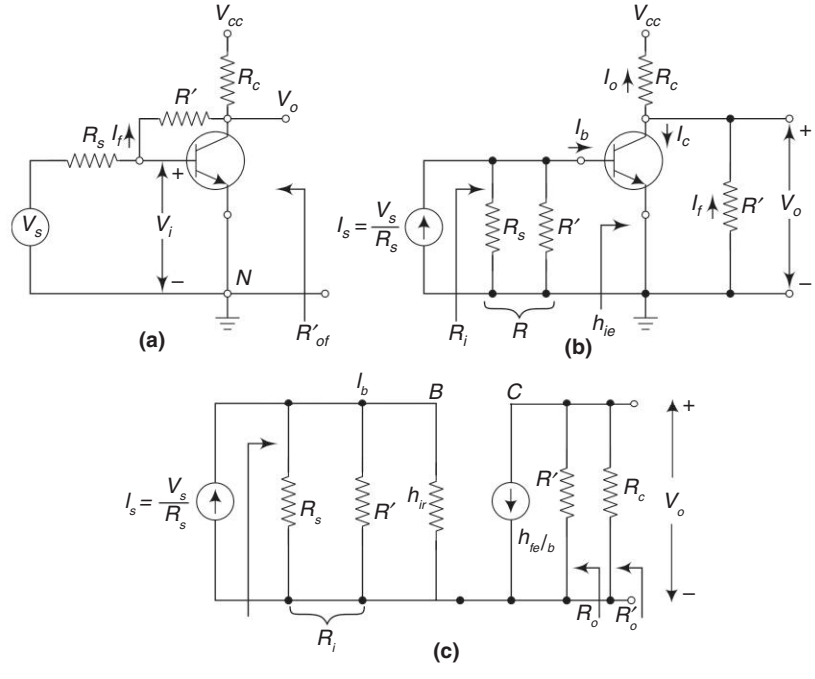


Fig. 6.24 *(a) Voltage-shunt feedback (b) The amplifier without feedback and (c) Low-frequency equivalent circuit model*

In Fig. 6.24(a), the output voltage V_o is much greater than the input voltage V_i and is 180° out of phase with V_i. Hence,

$$I_f = \frac{V_i - V_o}{R'} \approx \frac{V_o}{R'} = \beta V_o$$

where $\beta = \frac{I_f}{V_o} = -\frac{1}{R'}$.

As the feedback current is proportional to the output voltage, this circuit is an example of a voltage-shunt feedback amplifier. This topology stabilizes the transresistance gain R_M.

➤ ***To Draw the Basic Amplifier without Feedback*** The basic amplifier without feedback is shown in Fig. 6.24(b) and the input circuit of the amplifier without feedback is obtained by shorting the output node ($V_o = 0$). This results in R' connected between base and emitter of the transistor. The output circuit is found by shorting the input node ($V_i = 0$), thus, connecting R' from collector to emitter. The resultant equivalent circuit is given in Fig. 6.24(c) after replacing the transistor by its low frequency h-parameter model. As the feedback signal is current, the source is represented by a Norton's equivalent with $I_s = V_s/R_s$. The feedback signal is the current I_f flowing in the resistor R' which is in the output circuit. From Fig. 6.24(b),

$$\beta = \frac{I_f}{V_0} = -\frac{1}{R'}$$

The transresistance for the amplifier without feedback is given by

$$R_M = \frac{V_o}{I_i} = \frac{V_o}{I_s} = \frac{-I_c R'_s}{I_s} = \frac{-h_{fe} I_b R'_c}{I_s} = \frac{-h_{fe} R'_c R}{R + h_{ie}}$$

where $\frac{I_b}{I_s} = \frac{R}{R + h_{ie}}$, $R = R_s \parallel R' = \frac{R_s R'}{R_s + R'}$ and $R'_c = R_c \parallel R' = \frac{R' R_c}{R' + R_c}$

The desensitivity is given by

$$D = 1 + \beta R_M = 1 + \frac{h_{fe} R'_c R}{R'(R + h_{ie})} = \frac{R'(R + h_{ie}) + h_{fe} R'_c R}{R'(R + h_{ie})}$$

The transresistance with feedback is given by

$$R_{Mf} = \frac{R_M}{D} = \frac{-h_{fe} R'_c R R'}{R'(R + h_{ie}) + h_{fe} R'_c R}$$

The voltage gain with feedback can be written as

$$A_{Vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{R_{Mf}}{R_s}$$

From Fig. 6.24(c), $R_i = R \parallel h_{ie} = \frac{R h_{ie}}{R + h_{ie}}$

Hence, for voltage-shunt feedback amplifier, the input resistance with feedback decreases due to shunt mixing at the input and it is given by

$$R_{if} = \frac{R_i}{D} = \frac{R \parallel h_{ie}}{D}$$

Since $R_o = R'$, then $R_{of} = \dfrac{R_o}{1+\beta R_m}$ where $R_m = \lim\limits_{R_L \to \infty} R_M = \dfrac{-h_{fe}R'R}{R+h_{ie}}$

Therefore, $$1 + \beta R_m = 1 + \frac{h_{fe}R'R}{R'(R+h_{ie})} = \frac{R + h_{ie} + h_{fe}R}{R+h_{ie}} = \frac{h_{ie} + R(1+h_{fe})}{R+h_{ie}}$$

The output resistance with feedback, without considering the load resistance, decreases due to voltage sampling and it is given by

$$R_{of} = \frac{R_o}{1+\beta R_m} = \frac{R'(R+h_{ie})}{h_{ie} + R(1+h_{fe})}$$

From Fig. 6.24(c), $R'_o = R_o \parallel R_c = R' \parallel R_c = R'_c$. The output resistance with feedback, by considering the load resistance, can be written as

$$R'_{of} = \frac{R'_o}{D} = \frac{R'_o}{1+\beta R_M} = \frac{R'_c R'(R+h_{ie})}{R'(R+h_{ie}) + h_{fe}R'_c R}$$

Alternatively, it can also be written as

$$R'_{of} = R_{of} \parallel R_L = R_{of} \parallel R'_c$$

EXAMPLE 6.13

The circuit of Fig. 6.24(a) has the following parameters: $R_c = 4$ kΩ, $R' = 40$ kΩ, $R_s = 10$ kΩ, $h_{ie} = 1.1$ kΩ, $h_{fe} = 50$, and $h_{oe} = 0$. Find R_{Mf}, A_{Vf}, R_{if} and R'_{of}.

Solution Referring to Fig. 6.24, the transresistance gain without feedback is given by

$$R_M = \frac{V_o}{I_s} = \frac{-I_c R'_c}{I_s} = \frac{-h_{fe}I_b R'_c}{I_s} = \frac{-h_{fe}R'_c R}{R+h_{ie}}$$

where $$R'_c \equiv R_c \parallel R' = \frac{4\times10^3 \times 40\times10^3}{44\times10^3} = 3.64 \text{ kΩ}$$

and $$R = R_s \parallel R' = \frac{10\times10^3 \times 40\times10^3}{50\times10^3} = 8 \text{ kΩ}$$

Substituting the above values in R_M equation, we get

$$R_M = \frac{-h_{fe}R'_c R}{R+h_{ie}} = \frac{(-50)(3.64)(8)}{8+1.1} = -160 \text{ kΩ}$$

The feedback factor is given by

$$\beta = -\frac{1}{R'} = -\frac{1}{40\times10^3} = -0.025 \text{ mA/V}$$

The desensitivity is given by

$$D = 1 + \beta R_M = 1 + 0.025 \times 10^{-3} \times 160 \times 10^3 = 5$$

The transresistance gain and voltage gain with feedback are given by

$$R_{Mf} = \frac{R_M}{D} = \frac{-160 \times 10^3}{5} = -32 \text{ k}\Omega$$

$$A_{Vf} = \frac{V_0}{V_s} = \frac{V_0}{I_s R_s} = \frac{R_{Mf}}{R_s}$$

$$A_{Vf} = \frac{-32 \times 10^3}{10 \times 10^3} = -3.2$$

The input resistance without feedback is written as

$$R_i = \frac{Rh_{ie}}{R + h_{ie}} = \frac{(8 \times 10^3)(1.1 \times 10^3)}{9.1 \times 10^3} = 968\ \Omega$$

The input resistance with feedback is given by

$$R_{if} = \frac{R_i}{D} = \frac{968}{5} = 193\ \Omega$$

If R_c is an external load resistance, then the output resistance of the amplifier, without considering the load, is given by $R_o = R' = 40$ kΩ and the transresistance without load resistance is obtained by

$$R_m = \lim_{R_L \to \infty} R_M = \frac{-h_{fe} R' R}{R + h_{ie}}$$

$$= \frac{(-50)(40 \times 10^3)(8 \times 10^3)}{(8 + 1.1) \times 10^3} = -1760 \text{ k}\Omega$$

The output resistance with feedback is given by

$$R_{of} = \frac{R_o}{1 + \beta R_m} = \frac{40 \times 10^3}{1 + (0.025)(1760)} = 890\ \Omega$$

and

$$R'_{of} = R_{of} \parallel R_c$$

$$= \frac{(890)(4000)}{4890} = 728\ \Omega$$

Alternatively, R'_{of} can also be calculated as

$$R'_o = R_c \parallel R' = R'_c = 3.64 \text{ k}\Omega$$

and

$$R'_{of} = \frac{R'_o}{D} = \frac{3.64 \times 10^3}{5} = 728\ \Omega$$

EXAMPLE 6.14

Find R_m and R_{mf} using feedback principle for the circuit shown in Fig. 6.25. Assume and $h_{fe} = 50$ and $h_{ie} = 1.1$ kΩ.

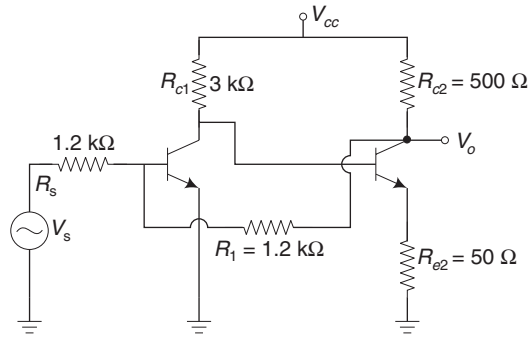


Fig. 6.25

Solution

$$R_{i2} = h_{ie2} + (1 + h_{fe2})\, R_{e2}$$
$$= 1.1 \times 10^3 + 51 \times 50 = 3.65\ \text{k}\Omega$$

We know that
$$R_m = \frac{V_o}{I_s} = \frac{V_o}{I_{b2}} \cdot \frac{I_{b2}}{I_{c1}} \cdot \frac{I_{c1}}{I_{b1}} \cdot \frac{I_{b1}}{I_s}$$

$$\frac{V_o}{I_{b2}} = \frac{-h_{fe} I_{b2} (R_{c2} \parallel R_1)}{I_{b2}}$$
$$= -50(0.5 \times 10^3 \parallel 1.2 \times 10^3) = -17.6 \times 10^3$$

$$\frac{I_{c1}}{I_{b1}} = h_{fe} = 50$$

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1} + R_{i2}} = \frac{-3 \times 10^3}{3 \times 10^3 + 3.65 \times 10^3} = -0.451$$

$$\frac{I_{b1}}{I_s} = \frac{(R_s \parallel R_1)}{(R_s \parallel R_i) + R_{i1}}$$
$$= \frac{(1.2 \times 10^3 \parallel 12 \times 10^3)}{(1.2 \times 10^3 \parallel 1.2 \times 10^3) + 1.1 \times 10^3} = 0.353$$

where $R_{i1} = h_{ie} = 1.1\ \text{k}\Omega$.

$$R_m = -17.6 \times 10^3 \times (-0.451) \times 50 \times 0.353 = 139.79\ \text{k}\Omega$$

$$\beta = \frac{I_f}{V_o} = \frac{1}{R_1} = \frac{1}{1.2 \times 10^3} = 0.833 \times 10^{-3}$$

$$R_{mf} = \frac{R_m}{1 + \beta R_m} = \frac{139.79 \times 10^3}{1 + 139.79 \times 10^3 \times 0.833 \times 10^{-3}} = 1.19\ \text{k}\Omega$$

or,
$$R_{mf} \approx \frac{1}{\beta} \approx \frac{1}{0.833 \times 10^{-3}} \approx 1.2\ \text{k}\Omega$$

6.13 CLASSIFICATION OF OSCILLATORS

Oscillators are classified in the following different ways.

1. According to the waveforms generated:
   (a) Sinusoidal oscillator
   (b) Relaxation oscillator

➤ ***Sinusoidal Oscillator*** This generates sinusoidal voltages or currents as shown in Fig. 6.26(a).

➤ ***Relaxation Oscillator*** This generates voltages or currents which vary abruptly one or more times in a cycle of oscillation as shown in Fig. 6.26(b) to 6.26(d).

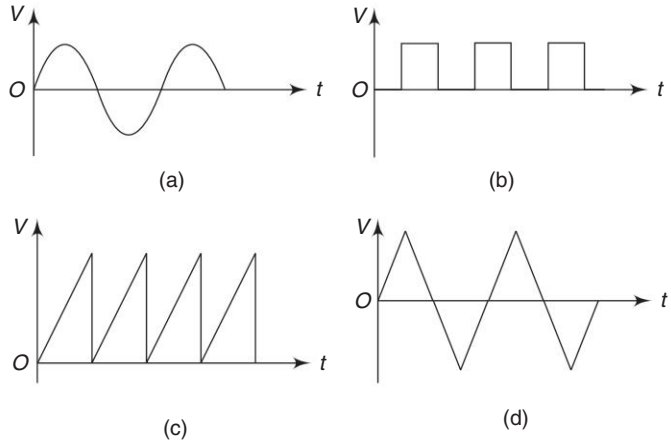


Fig. 6.26 *Waveforms generated by oscillators: (a) Sinusoidal (b) Square (c) Sawtooth (d) Triangular*

2. According to the fundamental mechanisms involved:
   (a) Negative resistance oscillators
   (b) Feedback oscillators

➤ ***Negative Resistance Oscillator*** This uses negative resistance of the amplifying device to neutralize the positive resistance of the oscillator.

➤ ***Feedback Oscillator*** This uses positive feedback in the feedback amplifier to satisfy the Barkhausen criterion.

3. According to the frequency generated:
   (a) Audio Frequency Oscillator (AFO): up to 20 kHz
   (b) Radio Frequency Oscillator (RFO): 20 kHz to 30 MHz
   (c) Very High Frequency (VHF) oscillator: 30 MHz to 300 MHz
   (d) Ultra High Frequency (UHF) oscillator: 300 MHz to 3 GHz
   (e) Microwave frequency oscillator: above 3 GHz
4. According to the type of circuit used, sine-wave oscillators may be classified as
   (a) *LC* tuned oscillator
   (b) *RC* phase-shift oscillator

6.14 CONDITIONS FOR OSCILLATION

Mechanism for Start of Oscillations

The oscillator circuit is set into oscillations by a random variation caused in the base current due to noise component or a small variation in the dc power supply. The noise components, i.e., extremely small random electrical voltages and currents are always present in any conductor, tube or transistor. Even when no external signal is applied, the ever-present noise will cause some small signal at the output of the amplifier. When the amplifier is tuned at a particular frequency f_o, the output signal caused by noise signals will be predominantly at f_o. If a small fraction (β) of the output signal is fed back to the input with proper phase relation, then this feedback signal will be amplified by the amplifier. If the amplifier has a gain of more than $1/\beta$, then the output increases and thereby the feed back signal becomes larger. This process continues and the output goes on increasing. But as the signal level increases, the gain of the amplifier decreases and at a particular value of output, the gain of the amplifier is reduced exactly equal to $1/\beta$. Then the output voltage remains constant at frequency f_o, called *frequency of oscillation*.

The essential conditions for maintaining oscillations are

1. $|A\beta| = 1$, i.e., the magnitude of loop gain must be unity.
2. The total phase-shift around the closed loop is zero or 360 degrees.

➤ ***Amplitude Stability of Oscillators*** As soon as the oscillations are initiated, they quickly grow in size till the amplitude becomes great enough to introduce nonlinear effects which reduce the amplification of the system. Then the equilibrium is established at an amplitude where the amplification of the loop from base to collector and back to base has dropped to exactly unity. If there was no such amplitude limiting, the amplitude of oscillation would build up to infinity. Thus, nonlinear action establishes the equilibrium amplitude in an oscillator.

➤ ***Practical Considerations*** The condition $|A\beta| = 1$ gives a single and precise value of $A\beta$ which should be set throughout the operation of the oscillator circuit. But in practice, as transistor characteristics and performance of other circuit components change with time, $|A\beta|$ will become greater or less than unity. Hence, in all practical circuits $|A\beta|$ should be set greater than unity so that the amplitude of oscillation will continue to increase without limit but such an increase in amplitude is limited by the onset of the nonlinearity of operation in the active devices associated with the amplifier as shown in Fig. 6.27. In this circuit, $A\beta$ is larger than unity for positive feedback. This onset of nonlinearity is an essential feature of all practical oscillators.

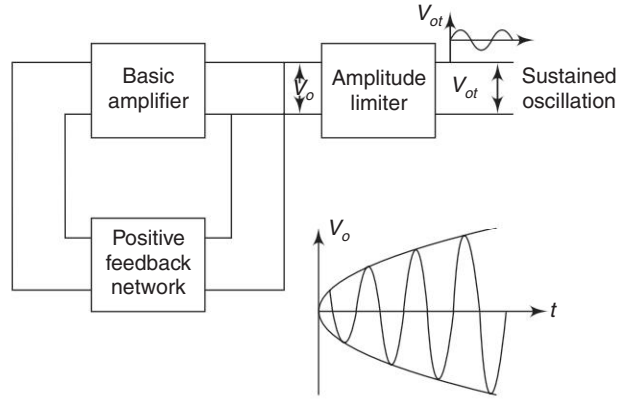


Fig. 6.27 *Block diagram of an oscillator*

6.15 *RC* PHASE SHIFT OSCILLATOR

6.15.1 *RC* Oscillators

All the oscillators using tuned *LC* circuits operate well at high frequencies. At low frequencies, as the inductors and capacitors required for the time circuit would be very bulky, *RC* oscillators are found to be more suitable. Two important *RC* oscillators are (i) *RC* phase-shift oscillator, and (ii) Wien-bridge oscillator.

➤ ***RC Phase-Shift Oscillator using BJT with Cascade Connection of High-Pass Filter (Phase-lead RC Network)*** In a BJT-based *RC* phase-shift oscillator using phase-lead *RC* network shown in Fig. 6.28(a), BJT is used as an active element of the amplifier. Here, the output of the feedback network is loaded appreciably by the relatively low resistance of the transistor. Thus, the resistance R of the feedback network is in parallel with the low input resistance h_{ie} of the transistor, which reduces the effective value of R in the last section of the feedback network. The feedback signal is coupled through the feedback resistor R_3 in series with the amplifier stage input resistor. In order to make the three sections identical, R_3 is chosen as $R_3 = R - R_i$ where R_i is the input impedance of the circuit.

The BJT amplifier provides a phase-shift of 180° and the feedback *RC* network provides the remaining 180° phase-shift to obtain a total phase-shift of 360° around the loop. Hence, each *RC* section is designed so as to provide a phase-shift of 60° at the desired frequency of oscillation.

The small-signal ac equivalent model is shown in Fig. 6.28(b). Simplifying this circuit by replacing the current source to voltage source, the simplified small-signal ac equivalent model is obtained as shown in Fig. 6.28(c).

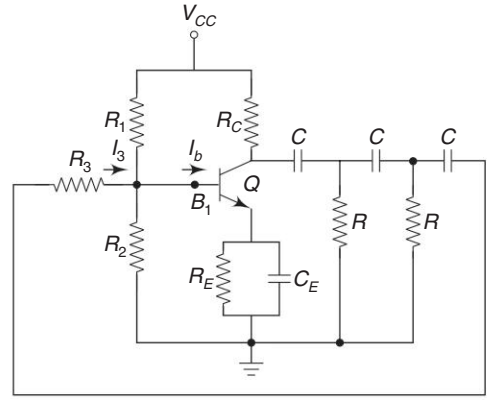


Fig. 6.28 (a) *BJT-based RC phase-shift oscillator*

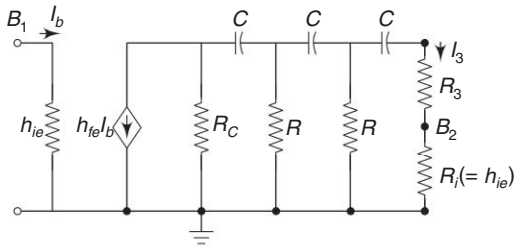


Fig. 6.28(b) *Small-signal ac equivalent model using h-parameters*

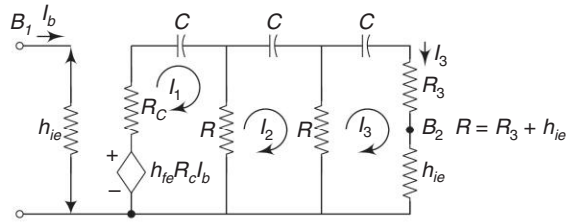


Fig. 6.28(c) *Simplified small-signal ac equivalent model*

Applying KVL, we get

$$I_1\left(R_C + R + \frac{1}{j\omega C}\right) - I_2 R = -h_{fe}R_C I_b$$

$$-I_1 R + I_2\left(2R + \frac{1}{j\omega C}\right) - I_3 R = 0$$

$$-I_2R + I_3\left(2R + \frac{1}{j\omega C}\right) = 0$$

Let $\alpha = \dfrac{1}{\omega RC}$ and $k = \dfrac{R_C}{R}$

Upon solving the above equations, we get

$$I_2 = I_3\,(2 - j\alpha)$$

and

$$I_1 = I_3\,(3 - \alpha^2 - j4\alpha)$$

Substituting the above I_1 and I_2 equations in the first KVL equation, we get loop gain I_3/I_b as

$$\frac{I_3}{I_b} = \frac{-h_{fe}k}{1 + 3k - (5 + k)\alpha^2 - j[(6 + 4k)\,\alpha - \alpha^3]}$$

Since the loop gain is a real quantity, we have

$$(6 + 4k)\,\alpha - \alpha^3 = 0$$

$$\alpha^2 = 6 + 4k$$

The frequency of oscillation f_o is given by

$$f_o = \frac{1}{2\pi RC\sqrt{6 + 4k}}$$

At this frequency, the loop gain I_3/I_b becomes

$$\frac{I_3}{I_b} = \frac{h_{fe}k}{4k^2 + 23\,k + 29}$$

We know that for sustained oscillation, $I_3/I_b > 1$.

Therefore, $h_{fe} > 4k + 23 + \dfrac{29}{k}$ (6.1)

- **To Determine the Value of *k* with Minimum h_{fe}**

$$\frac{dh_{fe}}{dk} = 4 - \frac{29}{k^2} = 0$$

$$k = \left(\frac{29}{4}\right)^{1/2} = 2.7$$

Therefore, $(h_{fe})_{\min} = 4(2.7) + 23 + \dfrac{29}{(2.7)} = 44.5$ (6.2)

Hence, it is understood that the value of h_{fe} for a transistor must be at least 45 for the circuit to oscillate.

EXAMPLE 6.15

In an *RC* phase-shift oscillator, if $R_1 = R_2 = R_3 = 200$ kΩ and $C_1 = C_2 = C_3 = 100$ pF. Find the frequency of oscillations.

Solution The frequency of an *RC* phase-shift oscillator is given by

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

$$= \frac{1}{2\pi \times 200 \times 10^3 \times 100 \times 10^{-12}\sqrt{6}} = 3.248 \text{ kHz}$$

EXAMPLE 6.16

Determine the frequency of oscillations when a *RC* phase-shift oscillator has $R = 10$ kΩ, $C = 0.01$ μF and $R_C = 2.2$ kΩ. Also, find the minimum current gain needed for this purpose.

Solution The frequency of oscillations of a *RC* phase-shift oscillator is

$$f_o = \frac{1}{2\pi RC\sqrt{6 + \left(\frac{4R_C}{R}\right)}}$$

Substituting the given values, we get

$$f_o = \frac{1}{2 \times 3.142 \times 10 \times 10^3 \times 0.01 \times 10^{-6}\sqrt{6 + \frac{4 \times 2.2 \times 10^3}{10 \times 10^3}}} = 607 \text{ Hz}$$

For sustained oscillations, the minimum value of current gain h_{fe} is

$$h_{fe} > 23 + \frac{29}{k} + 4k, \text{ where } k = \frac{4R_C}{R}$$

$$h_{fe} > 23 + 29\frac{R}{R_C} + \frac{4R_C}{R}$$

$$= 23 + 29 \times \frac{10}{2.2} + 4 \times \frac{2.2}{10} = 155.6$$

EXAMPLE 6.17

Find the capacitor C and h_{fe} for the transistor to provide a resonating frequency of 10 kHz of a transistorized phase-shift oscillator. Assume $R_1 = 25$ kΩ, $R_2 = 60$ kΩ, $R_C = 40$ kΩ, $R = 7.1$ kΩ and $h_{ie} = 1.8$ kΩ.

Solution For a phase-shift oscillator,

$f_o = 10$ kHz, $R_1 = 25$ kΩ, $R_2 = 60$ kΩ, $R_C = 40$ kΩ, $R = 7.1$ kΩ, $h_{ie} = 1.8$ kΩ

(i) To find capacitance, C

Frequency of oscillation is

$$f_o = \frac{1}{2\pi RC\sqrt{6 + 5k}}, \text{ where } k = \frac{R_C}{R}$$

$$C = \frac{1}{2\pi f_o R\sqrt{6 + \frac{4R_C}{R}}}$$

$$= \frac{1}{2\pi \times 10 \times 10^3 \times 7.1 \times 10^3 \sqrt{6 + \frac{4 \times 40 \times 10^3}{7.1 \times 10^3}}} = 0.41 \text{ nF}$$

(ii) To find h_{fe}

We know that $h_{fe} \geq 23 + 29 \frac{R}{R_C} + 4 \frac{R_C}{R}$

$$\geq 23 + 29 \frac{7.1 \times 10^3}{40 \times 10^3} + 4 \times \frac{40 \times 10^3}{7.1 \times 10^3}$$

$$\geq 23 + 5.1475 + 22.53 = 50.67$$

Therefore, $h_{fe} \geq 50.67$

➤ ***RC Phase-Shift Oscillator using Cascade Connection of Low-Pass Filter (Phase-Lag RC Network)*** Figure 6.29(a) shows the *RC* phase-shift oscillator using cascade connection of low-pass filters. There are three *RC* networks with the output of the last section returned to the input. In this oscillator, the required phase-shift of 180° is obtained by using *RC* network. In practice, the resistor *R* of the last section is adjusted in such a way that the total phase-shift produced by the cascade connection of *RC* network is exactly equal to 180°. The transistor in the amplifier circuit gives a phase-shift of another 180°. Hence, the total phase-shift around the circuit is 360°, i.e., 0°.

From Fig. 6.29(b), we can write the following three equations.

$$-\frac{I_1}{j\omega C} + \left(R + \frac{2}{j\omega C}\right) I_2 - \frac{I_3}{j\omega C} = 0 \tag{6.3}$$

$$-\frac{1}{j\omega C} I_2 + \left(R + \frac{2}{j\omega C}\right) I_3 - \frac{1}{j\omega C} I_4 = 0 \tag{6.4}$$

$$-\frac{1}{j\omega C} I_3 + \left(R + \frac{1}{j\omega C}\right) I_4 = 0 \tag{6.5}$$

From Eq. (6.5), the value of I_3 becomes

$$I_3 = I_4 (1 + j\omega RC) \tag{6.6}$$

Substituting Eq. (6.6) into Eq. (6.4), we get

$$-\frac{1}{j\omega C} I_2 + (1 + j\omega RC)\left(R + \frac{2}{j\omega C}\right) I_4 - \frac{1}{j\omega C} I_4 = 0$$

$$-I_2 + (3j\omega RC + 1 - \omega^2 R^2 C^2)\, I_4 = 0$$

Therefore,

$$I_2 = (3j\omega RC + 1 - \omega^2 R^2 C^2)\, I_4 \tag{6.7}$$

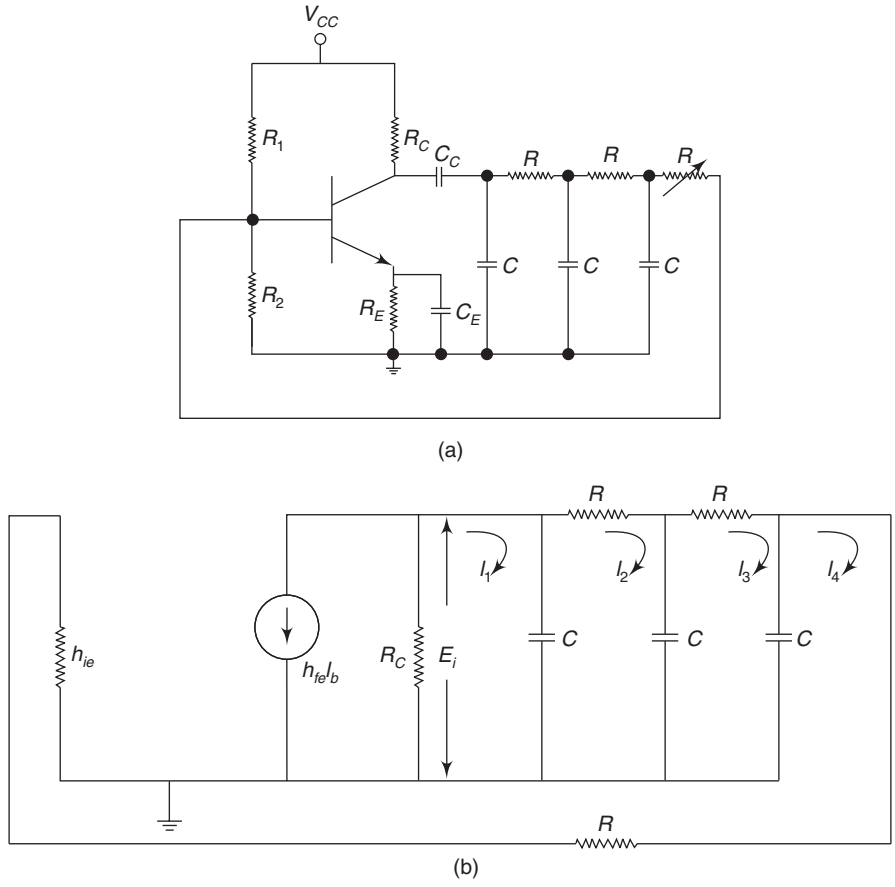


Fig. 6.29 *(a) RC phase-shift oscillator circuit using cascade connection of low-pass filters (b) Its equivalent circuit*

By substituting the values of I_2 and I_3 into Eq. (6.3), we get

$$I_4\left(6R - \omega^2 R^2 C^2 + \frac{1}{j\omega C} + 5\ j\omega CR^2\right) = \frac{I_1}{j\omega C} = 0$$

Therefore,

$$I_4 = \frac{I_1}{1 - 5\omega^2 R^2 C^2 + j\omega RC\,(6 - \omega^2\, R^2\, C^2)}$$

$$= \frac{I_1}{1 - 5\alpha^2 + j\alpha\,(6 - \alpha^2)} \text{ where } \alpha = \omega RC$$

Hence,
$$\beta = \frac{I_4}{I_1} = \frac{1}{1 - 5\alpha^2 + j\alpha\,(6 - \alpha^2)} \tag{6.8}$$

To determine the frequency of oscillation, the imaginary part is equated to zero, i.e.,

$$\alpha(6 - \alpha^2) = 0$$

Therefore, $\alpha = \sqrt{6};\ \omega CR = \sqrt{6}$

Hence, the frequency of oscillation is

$$f_o = \frac{\sqrt{6}}{2\pi RC}$$

By substituting the values of f_o into Eq. (6.8), we get

$$\beta = \frac{1}{1 - 30 - j\sqrt{6}\,(6 - 6)} = \frac{1}{29}$$

or $$|\beta| = \frac{1}{29}$$

Thus, sustained oscillation is obtained by having the gain of transistor amplifier greater than 29 and frequency of oscillation may be varied by changing the value of impedance element in the phase-shifting network.

➤ ***Analysis of Oscillator using Cascade Connection of One RC and One CR Filters*** A two stage oscillator uses the phase-shifting network is shown in Fig. 6.30.

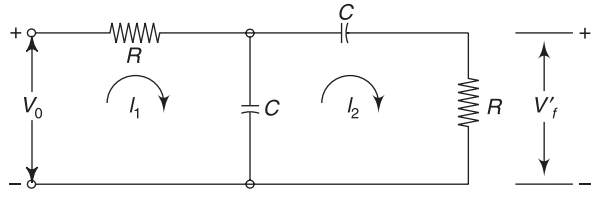


Fig. 6.30 *Cascade connection of one RC and one CR filters*

From Fig. 6.30, we can write the following three equations using Kirchhoff's voltage law,

$$I_1\left[R + \frac{1}{j\omega C}\right] - I_2\frac{1}{j\omega C} = V_o$$

$$I_2\left[\frac{2}{j\omega C} + R\right] - I_1\frac{1}{j\omega C} = 0$$

$$I_2 R = V'_f$$

Solving the above simultaneous equations, we get the feedback factor (β) of the network given by

$$\beta = \frac{V_o}{V'_f} = \frac{1}{3 + j\left(\omega RC - \dfrac{1}{\omega RC}\right)}$$

Here the oscillator oscillates when $\omega_o RC - \dfrac{1}{\omega_0 RC} = 0$.

i.e., $$\omega_o RC = \frac{1}{\omega_o RC}$$

$$2\pi f_o RC = \frac{1}{2\pi f_o RC}$$

$$f_o = \frac{1}{2\pi RC}$$

Therefore, the frequency of oscillation is $f_o = \frac{1}{2\pi RC}$.

At frequency of oscillation, $|\beta| = \frac{V_o}{V_f'} = \frac{1}{3}$.

As $|A\beta|$ should not be less than unity, it is necessary that the amplifier gain $|A|$ must be greater than three for the operation of the oscillator.

EXAMPLE 6.18

Find the value of C in a RC phase-shift oscillator using a BJT designed for a frequency of 1 kHz having value of R is 10 kΩ.

Solution The frequency of the RC phase-shift oscillator is given by

Hence, $$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

$$C = \frac{1}{2\pi f_o R\sqrt{6}} = \frac{1}{2\pi \times 1\times 10^3 \times 10\times 10^3 \times \sqrt{6}} = \frac{1}{15.386\times 10^7} = 6.5 \text{ nF}$$

EXAMPLE 6.19

Design an RC phase-shift oscillator to generate a 5 kHz sine wave with 20 V peak to peak amplitude. Draw the designed circuit. Assume $h_{fe} = 150$.

Solution Refer to Fig. 6.31.

Given $f_o = 5$ kHz, $V_{CC} = 20$ V, $h_{fe} = 150$,

$R_E = 1\ k\Omega$, and $C_E = 100$ μF.

Let $$V_{CE} = \frac{V_{CC}}{2} = 10 \text{ V and } V_E = \frac{V_{CC}}{10} = 2 \text{ V}$$

$$I_C \approx I_E = \frac{V_E}{R_E} = \frac{2}{1\times 10^3} = 2 \text{ mA}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{20-10}{2\times 10^{-3}} = 5 \text{ kΩ}$$

$$I_B = \frac{I_C}{h_{fe}} = \frac{2\times 10^{-3}}{150} = 13.33 \text{ μA}$$

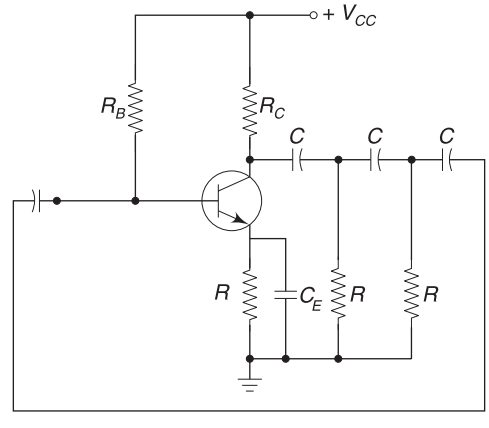


Fig. 6.31

$$R_B = \frac{V_{CC} - 0.6}{I_B} = \frac{20 - 0.6}{13.33 \times 10^{-6}} = 1.45 \text{ M}\Omega$$

$$R_i = R_B \parallel h_{ie}$$

$$h_{ie} = \frac{\eta V_T}{I_B} = \frac{2 \times 26 \times 10^{-3}}{6.67 \times 10^{-6}} = 7.79 \text{ k}\Omega$$

$$R_i = 1.45 \text{ M}\Omega \parallel 7.79 \text{ k}\Omega \approx 7.75 \text{ k}\Omega$$

$$R \approx R_i = 7.75 \text{ k}\Omega$$

$$k = \frac{R_C}{R} = \frac{5 \times 10^3}{7.75 \times 10^3} = 0.65$$

$$f_o = \frac{1}{2\pi RC\sqrt{4k + 6}}$$

$$5 \times 10^3 = \frac{1}{2\pi \times 7.75 \times 10^3 \times C \times \sqrt{4 \times 0.65 + 6}}$$

Therefore, $$C = \frac{1}{2\pi \times 5 \times 10^3 \times 7.75 \times 10^3 \times 2.93} = 1.4 \text{ nF}$$

6.15.2 *RC* PHASE-SHIFT OSCILLATOR USING FET

In this oscillator, the required phase shift of 180° in the feedback loop from output to input is obtained by using *R* and *C* components instead of tank circuit.

Figure 6.32(a) shows the circuit of a FET-based *RC* phase-shift oscillator using cascade connection of high-pass filter, i.e., phase-lead *RC* network. The FET amplifier is self-biased with a capacitor-bypassed source resistor and a drain resistor. The feedback network consists of three cascaded *RC* sections. Here, a common-source amplifier is followed by three sections of phase-lead network and the feedback voltage V_f available at the output of the last *RC* section of the feedback network is fed to the gate as the input.

The phase-shift, Φ, given by each *RC* section is $\Phi = \tan^{-1}\left(\frac{1}{\omega CR}\right)$.

If *R* is made zero, then Φ will become 90°. But making $R = 0$ is impracticable because if *R* is zero, then the voltage across it will become zero. Therefore, in practice, the value of *R* is adjusted such that Φ becomes 60°.

If the values of *R* and *C* are so chosen, for the given frequency f_o, the phase-shift of each *RC* section is 60°. Thus, such a *RC* ladder network produces a total phase-shift of 180° between its input and output voltages for the given frequency. Therefore, at the specific

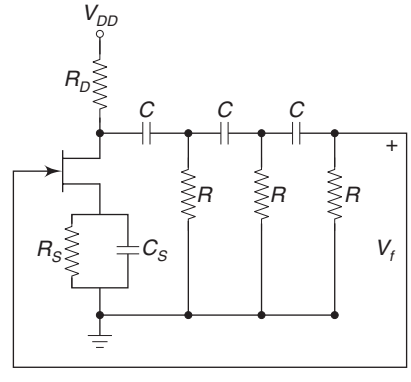


Fig. 6.32(a) *RC phase-shift oscillator using FET*

frequency f_o, the total phase-shift from the base of the transistor around the circuit and back to the base will be exactly 360° or 0°, thereby satisfying Barkhausen condition for oscillation.

The loop gain $A\beta$ can be computed using the ac equivalent circuit shown in Fig. 6.32(b). Here, let us assume that the input impedance of the FET amplifier stage is infinite.

Figure 6.32(b) is further simplified. Here, the current source is replaced by the equivalent voltage source $g_m R'_D V_i$, where $R'_D = r_d \parallel R_D$. Also, it is assumed that the feedback network does not load the amplifier as $R >> R'_D$ and hence, R'_D is neglected in Fig. 6.32(c).

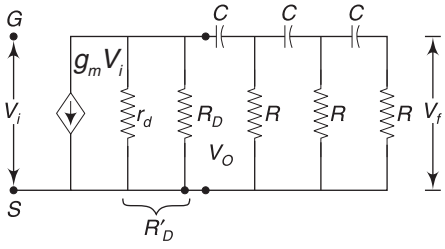


Fig. 6.32 (b) *Small-signal ac equivalent*

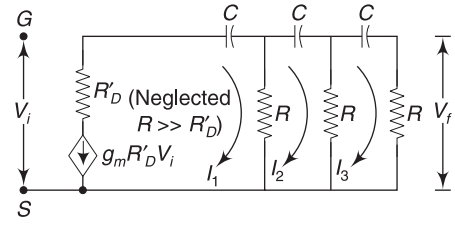


Fig. 6.32 (c) *Simplified small-signal ac equivalent model*

Applying KVL, we have

$$I_1\left(R + \frac{1}{j\omega C}\right) - I_2 R = -g_m R'_D V_i$$

$$-I_1 R + I_2\left(2R + \frac{1}{j\omega C}\right) - I_3 R = 0$$

$$-I_2 R + I_3\left(2R + \frac{1}{j\omega C}\right) - I_3 R = 0$$

Substituting $\alpha = \dfrac{1}{\omega RC}$ and writing I_2 in terms of I_3, we get

$$I_2 = I_3 (2 - j\alpha)$$

Substituting the above expression in the second KVL equation and writing I_1 in terms of I_3, we get

$$I_1 = I_3 (3 - 4j\alpha - \alpha^2)$$

Substituting the above I_1 and I_2 equations in the first KVL equation, we get

$$I_3[(3 - 4j\alpha - \alpha^2)(1 - j\alpha)] - I_3 (2 - j\alpha) = \frac{-g_m R'_D V_i}{R}$$

$$I_3 = \frac{-g_m R'_D V_i}{R[(1 - 5\alpha^2) + j(\alpha^3 - 6\alpha)]}$$

We know that

$$V_f = I_3 R = \frac{-g_m R'_D V_i}{(1 - 5\alpha^2) + j(\alpha^3 - 6\alpha)}$$

Therefore, the loop gain $A\beta$ can be written as

$$A\beta = \frac{V_f}{V_i} = \frac{-g_m R'_D}{(1 - 5\alpha^2) + j(\alpha^3 - 6\alpha)}$$

where $$\alpha = \frac{1}{\omega RC}$$

Since the loop gain is a real quantity, we have

$$\alpha^3 - 6\alpha = 0$$

$$\alpha^2 = 6$$

$$\omega^2 R^2 C^2 = \frac{1}{6}$$

Therefore, the frequency of oscillation becomes

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

and the loop gain $|A\beta|$ becomes

$$|A\beta| = \frac{g_m R'_D}{29}$$

We know that for sustained oscillation, $|A\beta| > 1$ and, hence,

$$g_m R'_D > 29$$

The voltage gain of the FET amplifier is given by

$$|A| > g_m R'_D$$

Therefore, $$|A| > 29 \text{ and } \beta = \frac{1}{29}$$

Hence, the gain of the FET amplifier gate must be at least 29 to sustain oscillations.

The *RC* phase-shift oscillator is suitable for audio frequencies only. Its main drawbacks are that the three capacitors or resistors should be changed simultaneously to change the frequency of oscillation and it is difficult to control the amplitude of oscillation without affecting the frequency of oscillation.

6.16 WIEN-BRIDGE OSCILLATOR

Figure 6.33(a) shows the circuit of a Wien-bridge oscillator. The circuit consists of a two-stage *RC* coupled amplifier which provides a phase-shift of 360° or 0°. A balanced bridge is used as the feedback network which has no need to provide any additional phase-shift. The feedback network consists of a lead-lag network ($R_1 - C_1$ and $R_2 - C_2$) and a voltage divider ($R_3 - R_4$). The lead-lag network provides a positive feedback to the input of the first stage and the voltage divider provides a negative feedback to the emitter of Q_1.

If the bridge is balanced, $$\frac{R_3}{R_4} = \frac{R_1 - jX_{C1}}{\left[\frac{R_2(-jX_{C2})}{R_2 - jX_{C2}}\right]} \tag{6.9}$$

where X_{C1} and X_{C2} are the reactances of the capacitors.

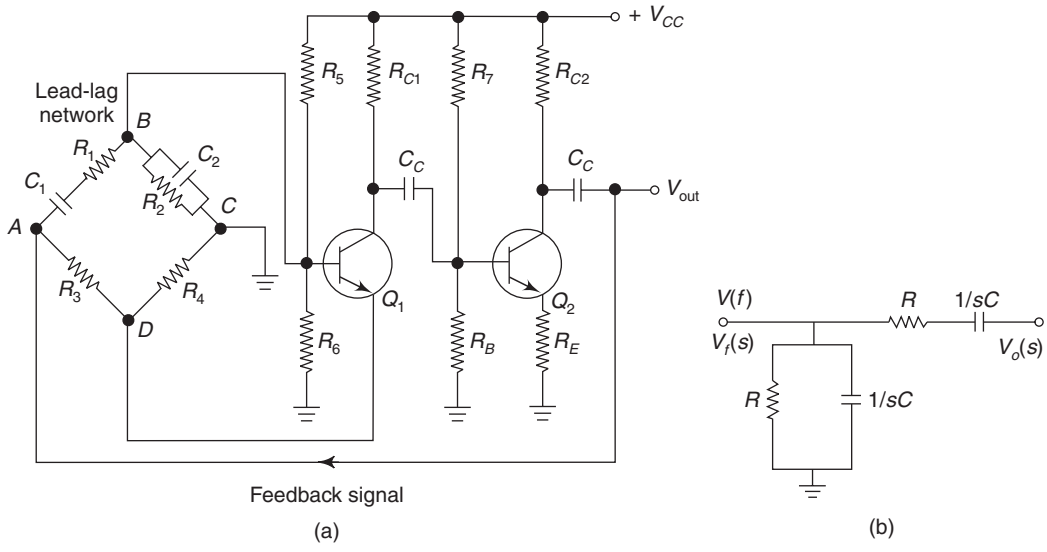


Fig. 6.33 *(a) Wien-bridge oscillator and (b) Feedback circuit*

Simplifying Eq. (6.9) and equating the real and imaginary parts on both sides, we get the frequency of oscillation as,

$$f_o = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

$$= \frac{1}{2\pi RC}, \text{ if } R_1 = R_2 = R \text{ and } C_1 = C_2 = C.$$

The ratio of R_3 to R_4 being greater than 2 will provide a sufficient gain for the circuit to oscillate at the desired frequency. This oscillator is used in commercial audio-signal generators.

➤ *To Determine the Gain of a Wien-Bridge Oscillator using a BJT Amplifier*

Assume that $R_1 = R_2 = R$ and $C_1 = C_2 = C$

Then the feedback circuit is as shown in Fig. 6.34(b).

Therefore,
$$V_f(s) = V_o(s)\frac{R \parallel \frac{1}{sC}}{R + \frac{1}{sC} + R \parallel \frac{1}{sC}}$$

$$V_f(s) = V_o(s)\frac{\frac{R}{1+sRC}}{R + \frac{1}{sC} + \frac{R}{1+sRC}}$$

$$= V_o(s)\frac{sRC}{s^2R^2C^2 + 3sRC + 1}$$

Hence, the feedback factor is

$$\beta = \frac{V_f(s)}{V_o(s)} = \frac{sRC}{s^2R^2C^2 + 3\,sRC + 1}$$

We know that $A\beta = 1$

Therefore, the gain of the amplifier,

$$A = \frac{1}{\beta} = \frac{s^2R^2C^2 + 3sRC + 1}{sRC}$$

Substituting $s = j\omega_o$, where the frequency of oscillation $f_o = \frac{1}{2\pi RC}$, i.e., $\omega_o = \frac{1}{RC}$, in the above equation and simplifying, we get $A = 3$. Hence, the gain of the Wien-bridge oscillator using a BJT amplifier is at least equal to 3 for oscillations to occur.

EXAMPLE 6.20

In a Wien-bridge oscillator, if the value of R is 100 kΩ, and frequency of oscillation is 10 kHz, find the value of the capacitor C.

Solution The operating frequency of a Wien-bridge oscillator is given by

$$f_o = \frac{1}{2\pi RC}$$

Therefore, $$C = \frac{1}{2\pi Rf_o} = \frac{1}{2\pi \times 100 \times 10^3 \times 10 \times 10^3} = 159 \text{ pF}$$

EXAMPLE 6.21

Design an oscillator with network in the feedback path of the amplifier shown in Fig. 6.34(a) to generate a sine wave of 2 kHz.

Solution Refer to Fig. 6.34(b).

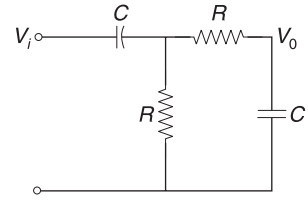


Fig. 6.34(a)

Applying KVL to the loop-1, we get

$$I_1\left(R - \frac{j}{\omega C}\right) - I_2R = V_i$$

$$I_1R\left(1 - \frac{j}{\omega RC}\right) - I_2R = V_i$$

Letting $\alpha = \frac{1}{\omega RC}$, we get

$$I_1(1 - j\alpha) - I_2 = \frac{V_i}{R} \qquad (1)$$

Applying KVL to the loop-2, we get

$$-I_1R + I_2\left(2R - \frac{j}{\omega C}\right) = 0$$

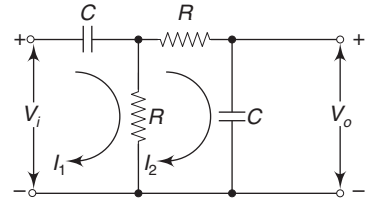


Fig. 6.34(b)

$$I_1 = I_2(2 - j\alpha) \quad (2)$$

Substituting Eq. (2) in Eq. (1), we get

$$I_2(2 - j\alpha)(1 - j\alpha) - I_2 = \frac{V_i}{R}$$

$$I_2(2 - 2j\alpha - j\alpha - \alpha^2 - 1) = \frac{V_i}{R}$$

$$\frac{I_2}{V_i} = \frac{1}{R[(1 - \alpha^2) - j3\alpha]}$$

The loop gain is given by

$$\beta = \frac{V_o}{V_i} = \frac{I_2 \times \left(-\frac{j}{\omega C}\right)}{V_i} = \frac{-j}{\omega CR[(1 - \alpha^2) - j3\alpha]} = \frac{-j\alpha}{(1 - \alpha^2) - j3\alpha}$$

Dividing both numerator and denominator by $j\alpha$, we get

$$\beta = \frac{\alpha^2}{j\alpha[(1 - \alpha^2) - j3\alpha]} = \frac{\alpha}{3\alpha + j(1 - \alpha^2)}$$

At frequency of oscillation, $(1 - \alpha^2) = 0$

Therefore, $\alpha = 1$

Hence, $$\frac{1}{\omega_o RC} = \frac{1}{2\pi f_o RC} = 1$$

$$f_o = \frac{1}{2\pi RC}$$

Equating the imaginary part of β to zero, we get

$$\beta = \frac{1}{3}$$

To obtain sustained oscillations, $|A\beta| \geq 1$

Therefore, $|A| \geq \frac{1}{|\beta|} \geq 3$

Given, $f_o = 2$ kHz

Here, $$f_o = \frac{1}{2\pi RC}$$

Let $C = 0.01$ μF

$$2 \times 10^3 = \frac{1}{2\pi R \times 10^{-8}}$$

Therefore, $R = 7.957$ kΩ

As the feedback network shown in Fig. 6.34(a) is a lead-lag network which introduces 0° phase-shift, the amplifier in the forward path should be a two-stage amplifier as shown in Fig. 6.34(c) to obtain overall phase-shift of 0°.

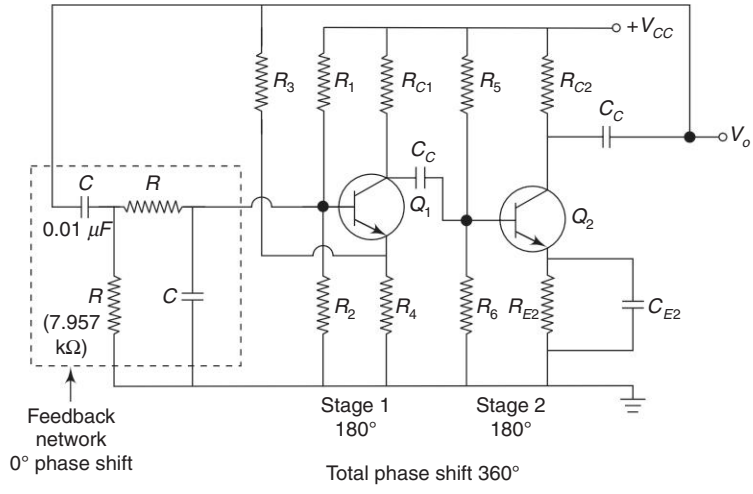


Fig. 6.34(c)

6.17 CRYSTAL OSCILLATORS

Figure 6.35 shows a crystal-controlled oscillator circuit. Here, it is a Colpitts crystal oscillator in which the inductor is replaced by the crystal. In this type, a piezoelectric crystal, usually quartz, is used as a resonant circuit replacing an *LC* circuit.

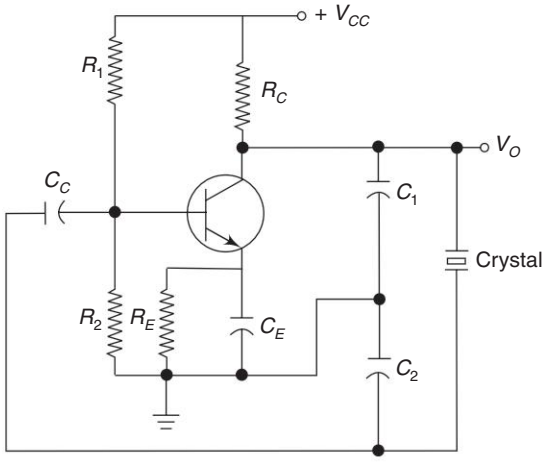


Fig. 6.35 *Colpitts crystal oscillator*

The crystal is a thin slice of piezoelectric material, such as quartz, tourmaline, and rochelle salt, which exhibit a property called *piezoelectric effect*. The piezoelectric effect represents the characteristics that the crystal reacts to any mechanical stress by producing an electric charge; in the reverse effect, an electric field results in mechanical strain.

➤ ***Quartz Crystal Construction*** In order to obtain high degree of frequency stability, crystal oscillators are essentially used. Generally, the crystal is a ground wafer of translucent quartz or tourmaline stone placed between two metal plates and housed in a stamp-sized package. There are two different methods of cutting this crystal wafer from the crude quartz. The method of cutting determines the natural resonant frequency and temperature coefficient of the crystal. When the wafer is cut in such a way that

its flat surfaces are perpendicular to its electrical axis (*X*-axis), it is called an *X-cut crystal* as shown in Fig. 6.36(b). When the wafer is cut in such a way that its flat surfaces are perpendicular to its mechanical axis (*Y*-axis), it is called *Y-cut crystal* as shown in Fig. 6.36(c).

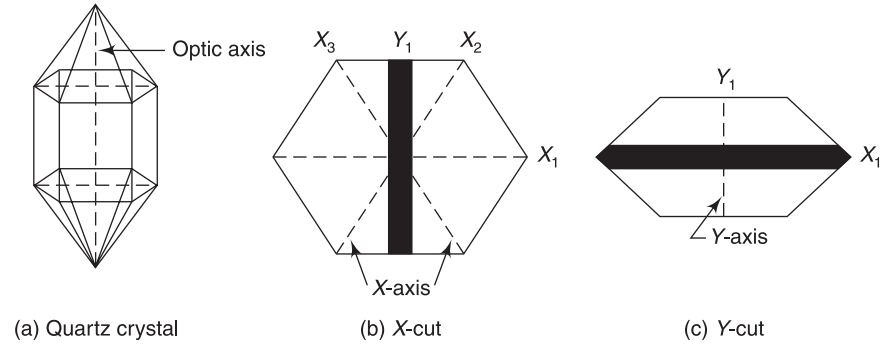


Fig. 6.36 *Piezoelectric crystal*

If an alternating voltage is applied, then the crystal wafer is set into vibration. The frequency of vibration equal to the resonant frequency of the crystal is determined by its structural characteristics. If the frequency of the applied ac voltage is equal to the natural resonant frequency of the crystal, then the maximum amplitude of vibration will be obtained. In general, the frequency of vibration is inversely proportional to the thickness (*l*) of the crystal.

The frequency of vibration is $f = \frac{P}{2l}\sqrt{\frac{Y}{\rho}}$

where Y is the Young's modulus, ρ is the density of the material and, $P = 1, 2, 3, \ldots$

The crystal is suitably cut and polished to vibrate at a certain frequency and mounted between two metal plates as shown in Fig. 6.37(a). The equivalent circuit of the crystal is shown in Fig. 6.37(b). The ratio of C_p to C_s may be several hundred or more so that series resonance frequency is very close to parallel resonant frequency. The resonant frequency is inversely proportional to the thickness of the crystal. Resonant frequencies from 0.5 MHz to 30 MHz can be obtained.

The reactance function shown in Fig. 6.37(c) is

$$jX = \frac{1}{j\omega C_p} \cdot \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

neglecting R. Here, $\omega_s^2 = \frac{1}{LC_s}$ is the series resonant frequency and

$$\omega_p^2 = \frac{1}{L\left(\frac{1}{C_s} + \frac{1}{C_p}\right)}$$

is the parallel resonant frequency. Since $C_p >> C_s$, $\omega_p \cong \omega_s$. For $\omega_s < \omega < \omega_p$, the reactance is inductive and for ω out of the above range, it is capacitive.

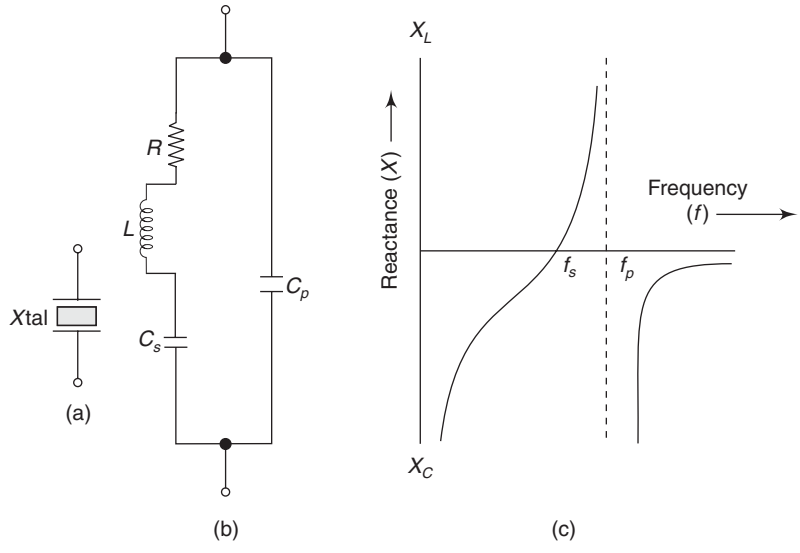


Fig. 6.37 *A Piezoelectric crystal: (a) Symbol (b) Electrical equivalent circuit (c) The reactance function when R = 0*

For a crystal Hartley oscillator, the capacitors C_1 and C_2 shown in Fig. 6.35 are replaced with inductors L_1 and L_2 respectively, so that the reactance of the crystal is capacitive. Hence, its oscillation frequency is $\dfrac{1}{2\pi\sqrt{(L_1 + L_2)C}}$.

The advantage of the crystal is its very high Q as a resonant circuit, which results in good frequency stability for the oscillator. However, since the resonant frequencies of the crystals are temperature dependent, it is necessary to enclose the crystal in a temperature-controlled oven to achieve the frequency stability of the order of 1 part in 10^{10}.

EXAMPLE 6.22

A crystal has the following parameters: $L = 0.5$ H, $C_s = 0.06$ pF, $C_p = 1$pF, and $R = 5$ kΩ. Find the series and parallel resonant frequencies and Q-factor of the crystal.

Solution (a) The series resonant frequency of the crystal is

$$f_s = \frac{1}{2\pi\sqrt{LC_s}} = \frac{1}{2\pi\sqrt{0.5 \times 0.06 \times 10^{-12}}} = 918.9 \text{ kHz}$$

Q-factor of the crystal at $f_s = \dfrac{\omega_s L}{R} = \dfrac{2\pi f_s L}{R}$

$$= \frac{2\pi \times 918.9 \times 10^3 \times 0.5}{5 \times 10^3} = 577$$

(b) The parallel resonant frequency of the crystal is

$$f_p = \frac{1}{2\pi}\sqrt{\frac{C_s + C_p}{LC_s C_p}}$$

$$= \frac{1}{2\pi}\sqrt{\frac{1.06\times10^{-12}}{0.5\times0.06\times10^{-12}\times1\times10^{-12}}} = 946 \text{ kHz}$$

Q-factor of the crystal at $f_p = \frac{\omega_p L}{R} = \frac{2\pi f_p L}{R}$

$$= \frac{2\pi\times946\times10^3\times0.5}{5\times10^3} = 594$$

EXAMPLE 6.23

A certain X-cut quartz crystal resonates at 500 kHz. It has an equivalent inductance of 4.2 H and an equivalent capacitance of 0.03 pF. If its equivalent resistance is 500 Ω, calculate its Q-factor.

Solution

$$Q = \frac{\omega L}{R} = \frac{2\pi fL}{R} = \frac{2\pi\times500\times10^3\times4.2}{500} = 26,376$$

6.17.1 Miller Crystal Oscillator

The Miller crystal controlled oscillator circuit is shown in Fig. 6.38. The crystal has two resonant frequencies. In between the series resonant frequency and parallel resonant frequency, the reactance of the crystal becomes inductive and hence, the crystal can be used as an inductor. One of the inductors in Hartley Oscillator is replaced by the crystal, which acts as an inductor when the frequency is greater than the series resonant frequency. The inter-electrode capacitance of the transistor acts as a capacitor to generate oscillations in the circuit.

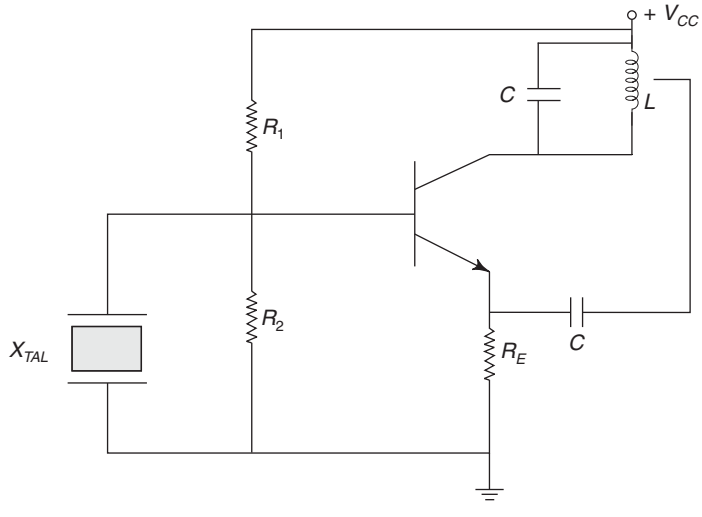


Fig. 6.38 *Miller crystal oscillator*

6.17.2 Pierce Crystal Oscillator

The transistor Pierce crystal oscillator is shown in Fig. 6.39. Here the crystal is connected as a series element in the feedback path from the collector to the base. The resistors, R_1, R_2, and R_E provide the necessary dc bias to the transistor and C_E is an emitter by pass capacitor. The Radio Frequency (RF) choke coil provides dc bias while decoupling any ac signal on the power lines from affecting the output signal. The coupling capacitor C blocks any dc between collector and base, and has negligible impedance at the operating frequency of the oscillator.

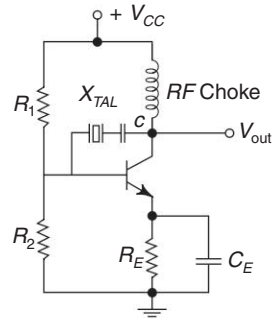


Fig. 6.39 *Pierce crystal oscillator*

The frequency of oscillation set by the series resonant frequency of the crystal is given by,

$$f_o = \frac{1}{2\pi\sqrt{LC_s}}$$

The main advantage of the Pierce crystal oscillator is its simplicity.

6.18 FREQUENCY STABILITY OF OSCILLATORS

The frequency stability of an oscillator is a measure of its ability to maintain the required frequency as precisely as possible over as long a time interval as possible. The accuracy of frequency calibration required may be anywhere between 10^{-2} and 10^{-10}. The main drawback in transistor oscillators is that the frequency of oscillation is not stable during a long time operation. The following are the factors which contribute to the change in frequency.

1. Due to change in temperature, the values of the frequency-determining components, viz., resistor, inductor and capacitor change.
2. Due to variation in the power supply, unstable transistor parameters, change in climatic conditions and aging.
3. The effective resistance of the tank circuit is changed when the load is connected.
4. Due to variation in biasing conditions and loading conditions.

The variation of frequency with temperature is given by

$$S_{\omega,T} = \frac{\Delta\omega/\omega_o}{\Delta T/T_o} \text{ ppmc (parts per million per °C)}$$

where ω_o, T_o are the desired frequency of oscillation and the operating temperature respectively. In the absence of automatic temperature control, the effect of temperature on the resonant LC circuit can be reduced by selecting an inductance L with positive temperature coefficient and a capacitance C with negative temperature coefficient.

The loading effect may be minimized if the oscillator is coupled to the load loosely or by a circuit with high input resistance and low output resistance properties. The frequency stability is defined as

$$S_\omega = \frac{d\theta}{d\omega}$$

where $d\theta$ is the phase-shift introduced for a small frequency change in nominal frequency f_o.

The circuit giving the larger value of $\frac{d\theta}{d\omega}$ has the more stable oscillator frequency. If the Q is infinite (an ideal inductor with zero series resistance), this phase change in phase is abrupt, $\frac{d\theta}{d\omega} \to \infty$ because the phase changes abruptly from $-90°$ to $+90°$.

For tuned oscillators, S_ω is directly proportional to the Q of a tuned circuit. A frequency stability of one part in 10^4 can be achieved with *LC* circuits. For *LC* oscillators, a tuned circuit must be lightly loaded to preserve high Q value.

As piezoelectric crystals have high Q values of the order of 10^5, they can be used as parallel resonant circuits in oscillators to get very high frequency stability of 1 ppm (part per million).

REVIEW QUESTIONS

1. What do you understand by feedback in amplifiers? Explain the terms *feedback factor* and *open-loop gain*.
2. What are the types of feedback?
3. Explain the term *negative feedback* in amplifiers.
4. What are the disadvantages of negative feedback?
5. When will a negative feedback amplifier circuit be unstable?
6. Compare the negative feedback and positive feedback.
7. Explain with circuit diagram a negative feedback amplifier and obtain expression for its closed-loop gain.
8. An amplifier with stage gain 200 is provided with negative feedback of feedback ratio 0.05. Find the new gain. [*Ans.* 18.8]
9. An amplifier has an open-loop gain of 90. When a negative feedback of feedback factor 0.6 is applied to it, calculate the overall gain. [*Ans.* 1.64]
10. An amplifier has a gain of 300. When negative feedback is applied, the gain is reduced to 240. Find the feedback ratio. [*Ans.* 1/1200]
11. An amplifier requires an input signal of 60 mV to produce a certain output. With a negative feedback to get the same output, the required input signal is 0.5 V. The voltage gain with feedback is 90. Find the open-loop gain and feedback factor. [*Ans.* 750, 0.88]
12. The open-loop gain of an amplifier is 50 and its bandwidth is 20 kHz. When a negative feedback is applied, the bandwidth is increased to 25 kHz (by 5 kHz). What will be the required feedback ratio? [*Ans.* 0.005]
13. A negative feedback of 0.0005 is applied to an amplifier whose open-loop gain is 60 dB. If the open-loop gain gets reduced by 12%, how much the overall gain gets altered? [*Ans.* 2%]
14. Enumerate the effects of negative feedback on the various characteristics of the amplifier.
15. How does negative feedback reduce distortion in an amplifier?
16. The distortion in an amplifier is found to be 3% when the feedback ratio of a negative feedback amplifier is 0.04. When the feedback is removed, the distortion becomes 15%. Find the open-loop gain and closed-loop gain. [*Ans.* 100; 20]
17. If negative feedback with a feedback factor β of 0.01 is introduced into an amplifier with a gain of 200 and a bandwidth of 6 MHz, obtain the resulting bandwidth of the feedback amplifier. [*Ans.* $BW_f = 18$ MHz]
18. If non-linear distortion in a negative feedback amplifier with an open-loop gain of 100 is reduced from 40% to 10%. Find feedback β of the amplifier. [*Ans.* $\beta = 0.03$]

19. The β and the open-loop gain of an amplifier are 10% and 80 respectively. By how much % does the closed-loop gain change if the open-loop gain increases by 25%?

[*Ans.* % change in closed-loop gain = 12.51%]

20. An amplifier has a gain of 50 with negative feedback. For a specified output voltage, if the input required is 0.1 V without feedback and 0.8 V with feedback, compute β and open-loop gain.

[*Ans.* $\beta = 0.0175$ and $A = 400$]

21. Describe with necessary derivations, the effect of negative feedback on the bandwidth and distortion in an amplifier.

22. What are the different types of negative feedback? Explain how the input and output impedances of an amplifier are affected by the different types of negative feedback.

23. Explain negative feedback with the help of the emitter follower as an example. Why is the emitter follower called so?

24. Explain what type of feedback has been used in an emitter follower circuit.

25. What is the effect of a voltage-series negative feedback in the following performance measures of a BJT amplifier: (i) Input resistance (ii) Output resistance (iii) Bandwidth (iv) Distortion and noise (v) Gain stability.

26. What type of input terminal connections should be used to have a large input impedance?

27. What is the sensitivity of an amplifier?

28. An amplifier with 2.5 kΩ input resistance and 50 kΩ output resistance has a voltage gain of 100. The amplifier is now modified to provide 5% negative voltage feedback in series with the input. Calculate (i) the voltage gain (ii) the input resistance, and (iii) the output resistance with feedback.

[*Ans.* 16.67; 15 kΩ; 8.3 kΩ]

29. An RC coupled amplifier has a voltage gain of 1000, f_1 = 50 Hz, f_2 = 200 kHz, and a distortion of 5%, without feedback. Find the amplifier voltage gain, f_{1f}, f_{2f} and distortion when a negative feedback is applied with feedback ratio of 0.01. [*Ans.* $A_f = 90.9$; $f_{1f} = 4.5$ Hz; $f_{2f} = 2.2$ MHz; $D_f = 0.45\%$]

30. The open-loop voltage gain of an amplifier is 50. Its input impedance is 1 kΩ. What will be the input impedance where a negative feedback of 10% is applied to the amplifier? [*Ans.* 6 kΩ]

31. The open-loop gain of an amplifier is 50 and its output impedance is 40 kΩ. When a negative feedback is applied, the output impedance becomes 6.666 kΩ. Find the feedback factor. [*Ans.* 0.1]

32. An amplifier has a voltage gain of 200, before negative feedback is applied. When negative feedback with $\beta = 0.25$ is applied, the nominal gain changes by 10%. Find the percentage change in the overall gain. [*Ans.* 0.19%]

33. The open-loop gain of an amplifier is 50 dB. A negative feedback of feedback factor 0.004 is applied to it. If the open-loop gain is thereby reduced by 10%. Find the change in the overall gain. [*Ans.* 0.0044]

34. In the BJT emitter follower circuit shown in Fig. 6.17(a), the circuit component values are R_s = 500 Ω, R_c = 1 kΩ, R_E = 2 kΩ, h_{fe} = 100, h_{ie} = 1.1 kΩ. Calculate A_{Vf}, R_{if}, R_{of} and R'_{of}.

35. For voltage-series feedback amplifier shown in Fig. 6.18(a), R_s = 2.55 kΩ, r_d = 20 kΩ, μ = 50. Determine A_{vf}, R_{if}, R_{of} and R'_{of}.

36. For current-series feedback amplifier using BJT shown in Fig. 6.21(a), R_E = 2 kΩ, R_s = 1.2 kΩ, R_L = 2.2 kΩ, h_{ie} = 2.2 kΩ, h_{fe} = 100. Determine $G_{Mf}A_{Vf}$, R_{if}, R_{of} and R'_{of}.

37. For current series feedback amplifier using FET shown in Fig. 6.22(a), R_s = 1.5 kΩ, R_L = 5 kΩ, r_d = 20 kΩ, μ = 40. Determine G_{Mf}, A_{Vf}, R_{if}, R_{of} and R'_{of}.

38. The circuit of Fig. 6.23(a) has the following parameters: R_{c1} = 2 kΩ, R_{c2} = 1 kΩ, R_E = 100 Ω, $R' = R_s$ = 1.2 kΩ, h_{fe} = 100, h_{ie} = 2.2 kΩ, and $h_{re} = h_{oe} = 0$. Find A_{If}, A_{Vf}, R_{if}, R_{of} and R'_{of}.

39. The circuit of Fig. 6.24(a) has the following parameters: R_c = 2 kΩ, R' = 20 kΩ, R_s = 5 kΩ, h_{ie} = 2.2 kΩ, h_{fe} = 100, and $h_{oe} = 0$. Find R_{Mf}, A_{Vf}, R_{if} and R'_{0f}.

40. Explain the main difference between an amplifier and an oscillator.

41. What are the constituent parts of an oscillator?

42. State and briefly explain Barkhausen criterion for oscillation.

43. Describe the construction of phase-shift oscillator and explain its working.

44. Derive the expression for the frequency of oscillation and the minimum gain required for sustained oscillations of the *RC* phase-shift oscillator.

45. Why do we need three *RC* networks for a phase-shift oscillator? Can it be two or four?

46. What are the merits and demerits of a phase-shift oscillator?

47. In an *RC* phase-shift oscillator, if its frequency of oscillation is 955 Hz and $R_1 = R_2 = R_3 = 680\ \text{k}\Omega$, find the value of capacitors. [*Ans.* 100 pF]

48. Draw the circuit diagram of Wien-bridge oscillator and briefly explain its operation.

49. In the Wien-bridge oscillator, if the *RC* network consists of resistors of 200 kΩ and the capacitors of 300 pF, find its frequency of oscillation. [*Ans.* 2.653 kHz]

50. A Wien-bridge oscillator has a frequency of 500 kHz. If the value of *C* is 1000 pF, determine the value of *R*. [*Ans.* 318.3 kΩ]

51. Draw the equivalent circuit of a quartz crystal.

42. What makes the quartz produce stable oscillations?

53. A crystal has the following parameters: $L = 0.33$ H, $C_S = 0.065$ pF, $C_P = 1.0$ pF, and $R = 5.5\ \text{k}\Omega$. Find the series resonant frequency and *Q*-factor of the crystal. [*Ans.* 1.09 MHz, 411]

54. What is the advantageous feature of a crystal oscillator?

55. What are the factors which affect the frequency stability of an oscillator?

56. Explain the working of a Miller crystal oscillator.

57. Show that the gain of Wien-bridge oscillator using BJT amplifier must be at least 3 for the oscillations to occur.

58. Explain the working of a Pierce crystal oscillator.

OBJECTIVE-TYPE QUESTIONS

1. In a positive feedback amplifier, the phase difference between input signal and feedback signal is
(a) 0º (b) 180º (c) 270º (d) 90º

2. In a negative feedback amplifier, the bandwidth is given by
(a) BW $(1+A\beta)$ (b) BW/ $(1+A\beta)$ (c) BW$(1-A\beta)$ (d) BW/ $(1-A\beta)$

3. In a negative feedback amplifier, the stability changes by a factor of
(a) $A\beta$ (b) $A+\beta$ (c) $(1+A\beta)$ (d) $(1-A\beta)$

4. A series-derived, shunt-fed feedback amplifier is otherwise called a _____ feedback amplifier.
(a) voltage-series (b) voltage-shunt (c) current-series (d) current-shunt

5. The Nyquist criterion for stability states that an amplifier is unstable if the Nyquist curve encloses the _____ point.
(a) $1+j0$ (b) $-1+j0$ (c) $0+j0$ (d) $0-j1$

6. The input impedance Z_i and the output impedance Z_0 of an ideal transconductance (voltage controlled–current source) amplifier are
(a) $Z_i = 0, Z_0 = 0$ (b) $Z_i = 0, Z_0 = \infty$ (c) $Z_i = \infty, Z_0 = 0$ (d) $Z_i = \infty, Z_0 = \infty$

7. In a negative feedback amplifier using voltage series (i.e., voltage sampling, series mixing) feedback,
(a) R_i decreases and R_0 decreases (b) R_i decreases and R_0 increases
(c) R_i increases and R_0 decreases (d) R_i increases and R_0 increases
(R_i and R_0 denote the input and output resistances respectively)

8. Voltage-series feedback (also called series-shunt feedback) results in
(a) increase in both input and output impedances
(b) decrease in both input and output impedances
(c) increase in input impedance and decrease in output impedance.
(d) decrease in input impedance and increase in output impedance.

9. In a shunt-shunt negative feedback amplifier, as compared to the basic amplifier
(a) both input and output impedances, decrease
(b) input impedance decreases but output impedance increases
(c) input impedance increases but output impedance decreases
(d) both input and output impedances increase

10. The effect of current-shunt feedback in an amplifier is to
(a) increase the input resistance and decrease the output resistance.
(b) increase both input and output resistances
(c) decrease both input and output resistances
(d) decrease the input resistance and increase the output resistance

11. Consider the following:
1. Oscillator 2. Emitter follower 3. Cascaded amplifier 4. Power amplifier
Which of these use feedback amplifiers?
(a) 1 and 2 (b) 1 and 3 (c) 2 and 4 (d) 3 and 4

12. If an amplifier with gain of –1000 and feedback of $b = -0.1$ has a gain change of 20% due to temperature, then change in gain of the feedback amplifier would be
(a) 10% (b) 5 % (c) 0.2 % (d) 0.01 %

13. The feedback amplifier shown in the figure has

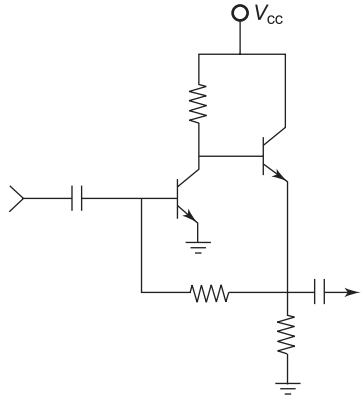


Fig. 6.40

(a) current-series feedback with large input impedance and large output impedance
(b) voltage-series feedback with large input impedance and low output impedance
(c) voltage-shunt feedback with low input impedance and low output impedance
(d) current-shunt feedback with low input impedance and output impedance

14. To obtain very high input and output impedances in a feedback amplifier, the amplifier configuration mostly used is
(a) voltage-series (b) current-series (c) voltage-shunt (d) current-shunt

15. Negative feedback in an amplifier
(a) reduces gain (b) increases frequency and phase distortions
(c) reduces bandwidth (d) increases noise

16. An amplifier has an open-loop gain of 100, an input impedance of 1 kΩ, and an output impedance of 100 Ω. A feedback network with a feedback factor of 0.99 is connected to the amplifier in a voltage series feedback mode. The new input and output impedances, respectively, are
(a) 10 Ω and 1 Ω (b) 10 Ω and 10 Ω
(c) 100 kΩ and 1 Ω (d) 100 kΩ and 1 kΩ

17. An amplifier without feedback has a voltage gain of 50, input resistance of 1 kΩ and output resistance of 2.5 kΩ. The input resistance of the current-shunt negative feedback amplifier using the above amplifier with a feedback factor of 0.2 is
(a) 1/11 kΩ (b) 1/5 kΩ (c) 5 kΩ (d) 11 kΩ

18. The value of β and amplification factor with feedback in order of oscillations to occur if $A = 40$ without feedback is
(a) 0.025, 20 (b) 0.025, ∞ (c) 0, ∞ (d) 0, 20

19. In a common-emitter amplifier, the unbypassed emitter resistance provides
(a) Voltage-shunt feedback (b) Current-series feedback
(c) Voltage-series feedback (d) Current-shunt feedback

20. The essential conditions for sustained oscillation are
(a) $|A\beta| = 1$ and $\angle A\beta = 0$ (b) $|A\beta| < 1$ and $\angle A\beta = 0$
(c) $|A\beta| > 1$ and $\angle A\beta = 0$ (d) $|A\beta| < 1$ and $\angle A\beta = 180°$

21. For a stable oscillator, the Barkhausen criterion is
(a) $A\beta = 0$ (b) $|A\beta| = 1$
(c) $-A\beta = 1$ (d) $A = \dfrac{1}{\sqrt{\beta}}$

22. In an *RC* phase-shift oscillator, oscillations will occur if the voltage gain of its internal amplifier is
(a) unity (b) less than unity (c) around 3 (d) more than 29

23. In an *RC* phase-shift oscillator, the frequency of oscillations is
(a) $\dfrac{1}{2\pi\sqrt{RC}}$ (b) $\dfrac{1}{2\pi RC\sqrt{6}}$ (c) $\dfrac{2\pi}{\sqrt{RC}}$ (d) $2\pi\sqrt{RC}$

24. The phase shift of each *RC* network of an *RC* phase-shift oscillator is
(a) 60° (b) 90° (c) 180° (d) 360°

25. To generate a 1 kHz signal, the most suitable circuit is
(a) Hartley oscillator (b) Colpitts oscillator
(c) tuned collector oscillator (d) Wien-bridge oscillator

26. The crystal oscillator frequency is very stable due to
(a) rigidity of crystal (b) size of crystal
(c) structure of crystal (d) high *Q* of the crystal

27. A crystal oscillator is used because
(a) it gives high output voltage
(b) it works at high efficiency
(c) the frequency of oscillations remains substantially constant
(d) it requires very low dc supply voltage

28. A Wien-bridge oscillator has $R_1 = R_2 = 220$ kΩ and $C_1 = C_2 = 250$ pF. The frequency of oscillations will be nearly
(a) 0.89kHz (b) 1.89 kHz (c) 2.89 kHz (d) 3.89 kHz

29. The main advantage of using crystal oscillators is
(a) high-frequency stability (b) suitability for low voltages
(c) high efficiency (d) high output voltage

30. In a piezoelectric crystal oscillator, the oscillation or tuning frequency is linearly proportional to the
(a) mass of the crystal
(b) square root of the mass of the crystal
(c) square of the mass of the crystal
(d) inverse of the square root of the mass of the crystal

31. Which one of the following oscillators is well suited for the generation of a wide range audio-frequency sine waves?

(a) *RC* phase-shift oscillator
(b) Wien-bridge oscillator
(c) Colpitts oscillator
(d) Harley oscillator

32. The configuration of the Fig. 15.33 is a

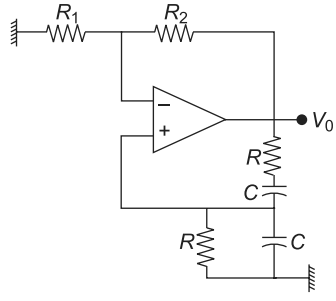


Fig. 6.41

(a) precision integrator
(b) Hartley oscillator
(c) Butterworth high-pass filter
(d) Wien-bridge oscillator

33. For the *RC* phase-shift oscillator shown in the figure, the frequency of oscillations is

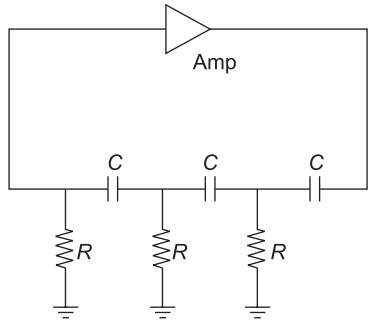


Fig. 6.42

(a) $\frac{1}{(2\pi\sqrt{6RC})}$ (b) $\frac{1}{(2\pi RC)}$ (c) $\frac{1}{(\sqrt{6}RC)}$ (d) $\frac{1}{\sqrt{6}(2\pi RC)}$

APPENDIX
A

Probable Values of General Physical Constants

Constant	Symbol	Value
Electronic charge	q	1.602×10^{-19} C
1 electron volt	eV	1.602×10^{-19} Joules
Electronic mass	m	9.109×10^{-31} kg
Ratio of charge to mass of an electron	q/m	1.759×10^{11} C/kg
Planck's constant	h	6.626×10^{-34} J-s
Boltzmann constant	k	8.620×10^{-5} eV/°K
Velocity of light	c	2.998×10^{8} m/s
Acceleration of gravity	g	9.807 m/s^2
Permeability of free space	μ_0	1.257×10^{-6} H/m
Permittivity of free space	ε_0	8.854×10^{-12} F/m
1 joule	J	6.25×10^{18} eV

APPENDIX
B

Conversion Factors and Prefixes

Constant	Value
1 ampere (A)	1 C/s
1 angstrom unit (Å)	10^{-10} m = 10^{-8} cm
1 coulomb (C)	1 A–s
1 farad (F)	1 C/V
1 henry (H)	1 V–s/A
1 hertz (Hz)	1 cycle/s
1 lumen	0.0016 W (at 0.55 μ m)
1 mil	10^{-3} inch = 25 μ m
1 micron	1 μ m = 10^{-6} m
1 newton (N)	1 kg = m/s^2
1 Volt (V)	1 W/A
1 watt (W)	1 J/s
1 weber (Wb)	1 V–s
1 weber per square meter (Wb/m^2)	10^4 gauss
1 tesla (T)	1 Wb/m^2