Basic Electrical and Electronics Engineering-II

WBUT–2016

Fifth Edition

About the Authors

Abhijit Chakrabarti, PhD (Technology), is former Vice Chairman and Chairman (acting) of West Bengal State Council of Higher Education, West Bengal. He is also the Professor and former HOD of the Department of Electrical Engineering, Indian Institute of Engineering, Science and Technology Shibpur, Howrah, West Bengal. He has also served as the former Vice Chancellor of Jadavpur University, Kolkata. He has nearly eight years of industrial experience and around twenty-five years of teaching and research experience. He is a fellow of the Institution of Engineers (India) and has published/presented 129 research papers in international and national journals and conferences including IEEE Transaction, Elsevier, etc. He has published numerous books on Electrical Engineering. Professor Chakrabarti is the recipient of Pandit Madan Mohan Malviya award and the Power Medal, Merit and Best Paper awards (twice) from Central Electricity Authority, India, and an International Conference, China. His areas of interest include power systems, electric circuits, and power electronics and drives.

Sudipta Debnath, PhD in (Engineering), is the Associate Professor, Department of Electrical Engineering, Jadavpur University, Kolkata. She has received the Career Award from AICTE, Govt. of India, and Young Scientist recognition from DST, Govt. of India. She is also the recipient of a certificate of merit from Institution of Engineers, India. She has published/presented 35 research papers in international and national journals and conferences. She has nearly one year of industrial experience and 18 years of teaching and research experience. Her areas of interest include power systems, electrical machines and soft computing techniques.

Soumitra Kumar Mandal is Professor at National Institute of Technical Teachers' Training and Research, Kolkata. He obtained a BE (Electrical Engineering) from Bengal Engineering College, Shibpur, Calcutta University, and an MTech (Electrical Engineering) with specialisation in Power Electronics from Institute of Technology, Banaras Hindu University, Varanasi. Thereafter, he obtained a PhD degree from Punjab University, Chandigarh. He started his career as a lecturer of Electrical Engineering, SSGM College of Engineering, Shegaon. After that he joined as a lecturer at Punjab Engineering College, Chandigarh, and served there from March 1999 to January 2004. From February 2004, he joined National Institute of Technical Teachers' Training and Research, Kolkata, and is presently the Professor in Electrical Engineering. He is also a life member of ISTE and a member of IE. Throughout his academic career, he has published about twenty research papers in national and international journals and presented many papers in national and international conferences. His research interests are in the field of computer controlled drives, microprocessor and microcontroller-based system design, embedded system design and neuro-fuzzy computing.

Basic Electrical and Electronics Engineering-II

WBUT–2016

Fifth Edition

Part I: Electrical Engineering-II

Authored by

Abhijit Chakrabarti

Professor and Former HOD, Department of Electrical Engineering
Indian Institute of Engineering Science and Technology Shibpur, Howrah, West Bengal
and
Former Vice Chancellor, Jadavpur University, Kolkata
Former Vice Chairman and Chairman (acting)
West Bengal State Council of Higher Education, Kolkata

Sudipta Debnath

Associate Professor Department of Electrical Engineering
Jadavpur University, Kolkata

Part II: Electronics Engineering-II

Authored by

Soumitra Kumar Mandal

Professor
National Institute of Technical Teachers' Training and Research
Kolkata

McGraw Hill Education (India) Private Limited

NEW DELHI

McGraw Hill Education Offices

New Delhi New York St Louis San Francisco Auckland Bogotá Caracas
Kuala Lumpur Lisbon London Madrid Mexico City Milan Montreal
San Juan Santiago Singapore Sydney Tokyo Toronto

McGraw Hill Education (India) Private Limited

Published by McGraw Hill Education (India) Private Limited,
P-24, Green Park Extension, New Delhi 110 016.

Basic Electrical and Electronics Engineering-II, 5e (WBUT–2016)

Print Edition:

ISBN-13: 978-93-85880-91-9
ISBN-10: 93-85880-91-8

Managing Director: *Kaushik Bellani*
Director—Product (Higher Education and Professional): *Vibha Mahajan*

Manager—Product Development: *Koyel Ghosh*
Specialist—Product Development: *Piyali Chatterjee*
Head—Production (Higher Education and Professional): *Satinder S Baveja*
Senior Production Executive: *Jagriti Kundu*
Senior Graphic Designer—Cover: *Meenu Raghav*
AGM—Product Management (Higher Education and Professional): *Shalini Jha*
Manager—Product Management: *Ritwick Dutta*

General Manager—Production: *Rajender P Ghansela*
Manager—Production: *Reji Kumar*

Typeset at Tej Composers, WZ-391, Madipur, New Delhi 110063 and printed at

Cover:

Visit us at: www.mheducation.co.in

CONTENTS

PREFACE

Basic Electrical Engineering and Basic Electronics Engineering are the two fundamental subjects of most engineering disciplines. It is extremely important to ensure that the fundamentals of these two courses are well understood by all engineering students since these subjects have applications in all streams. Though numerous textbooks on these two subjects are already available, we felt that there was still a need for another book which would present the basics of Electrical and Electronics Engineering in a comprehensive manner. It is also true that there is hardly any comprehensive textbook available on this subject that precisely covers the prescribed syllabus of WBUT. Moreover, following the new syllabus framed by West Bengal University of Technology (WBUT), there was a need to bring out a textbook that would cover the entire syllabus of Basic Electrical and Electronics Engineering-II. An attempt has, therefore, been made to present an exhaustive material in the form of a textbook to the students studying basic electrical and electronics engineering in WBUT. We hope that after going through this book, the undergraduate engineering students of WBUT will find that their learning and understanding of the subject, Basic Electrical and Electronics Engineering, has increased progressively.

Our main aim was to equip the students with the fundamental knowledge of Electrical and Electronics Engineering, the theory backed up by illustrative solved problems. We have emphasized on building of fundamental concepts, mathematical derivations coupled with applications and solutions of problems. We have attempted to keep the language in the textbook as lucid as possible. Relevant examples have been selected to supplement the theory so that students have a thorough idea of the applicability of the theoretical concepts. The salient features of this book are as follows:

- Coverage and chapter organization as per the syllabus of WBUT
- Important statements and key terms highlighted within the topics for better clarity
- Individual topics are very well supported by the solved examples
- Single book containing the fundamentals of both electrical and electronics engineering
- Stepwise explanation of theories and derivations along with relevant examples
- Diagrammatic and elaborate representation of circuits and phasors
- Numerous solved examples and adequate exercise problems for practice
- Solutions of WBUT previous year questions from 2003–2015 incorporated within the book appropriately.

- Pedagogy includes:
  - *–507 Solved Examples*
  - *–347 Practice Questions with Answers*
  - *–224 Multiple Choice Questions*
  - *–589 Illustrations*

The book comprises 12 chapters designed as per WBUT syllabus. The first six chapters deal with the fundamentals of basic electrical engineering, and the next six chapters deal with the fundamentals of basic electronics engineering.

Part I is organized in six chapters as follows:
Chapter 1 deals with electrostatics with emphasis on Coulomb's law, Gauss's law, electric field intensity and capacitance.
Chapter 2 introduces dc machines and presents the concepts of magnetic flux, equivalent circuit, back emf, armature windings, speed-torque characteristics and applications of dc machines.
Chapter 3 describes single-phase transformers, their construction, operation, regulation and efficiency.
Chapters 4 and 5 introduce three-phase systems and three-phase induction motors respectively.
Chapter 6 presents the structure of a power system with special emphasis on distribution and representation.

The second part of Basic Electrical and Electronics Engineering is written as a first course of electronics, incorporating both analog and digital electronics devices and circuits. This part of the book allows students to achieve an enhanced level of understanding within the prescribed period and helps them develop a strong foundation for other electronics specialized courses. The principles of operation of various devices are explained properly, and examples and solved problems ranging from simple to complex have been incorporated. After studying this book, we are sure students can perform better in semesters as well as in competitive examinations.

Part II aims to provide working knowledge about analog and digital logic elements and the expertise required to develop analog and digital systems. This part covers the following areas: field effect transistors, feedback amplifier and oscillators, operational amplifier, number system, and Boolean algebra.

Part II is organized into six chapters as explained below:
Chapter 1 describes the basic concept of field effect transistors, JFET structure and its characteristics, MOSFET structure and characteristics, depletion and enhancement-type MOSFET, common source, common gate and common drain configuration of FET, and basic principles of CMOS.
Chapter 2 presents the basic concept of positive and negative feedback amplifiers, classification of amplifiers, different topologies of feedback amplifiers, and properties of feedback amplifiers.
Chapter 3 describes the basic concept of oscillators, Barkhausen criteria, classification of oscillators, phase-shift oscillation, Wein bridge oscillator, tuned collector oscillator, LC oscillators, Colpitts, Hartley and crystal oscillators.

Chapter 4 is related to operational amplifiers. The integrated circuits, ideal OP-AMP, equivalent circuit of OP-AMP, difference amplifier, configuration of OP-AMP, characteristics, frequency response and stability of OP-AMP and the concept of virtual ground are discussed elaborately in this chapter.
Chapter 5 deals with design and implementation of analog circuits using an operational amplifier. The application of operational amplifiers in adder, subtractor, voltage-to-current converter, current-to-voltage converter, multiplier, voltage follower, integrator, differentiator, logarithmic amplifier, multiplier, divider and Schmitt trigger are incorporated in this chapter.
Chapter 6 provides the basic concepts of number systems, binary arithmetic, BCD codes, Boolean algebra and various logic operations. The correlation between Boolean expressions and implementation using logic gates is explained. The operation of logic gates with logic diagrams, De Morgan's theorems, and simplification of logic circuits are also incorporated.

Care has been taken regarding the chronology of presentations, mathematical treatments and in representing the theory in a lucid manner. Each chapter has sufficient number of theoretical questions and unsolved problems with hints and answers. For the benefit of students, we have also included answers of questions and detailed solutions of problems from question papers of WBUT.

Acknowledgements

A number of experts took pains to provide valuable feedback on various chapters of the book. Our heartfelt gratitude goes out to those whose names are given below:

Sayantan Chakraborty	*Dr. Sudhir Chandra Sur Degree Engineering College, Kolkata*
Chandra Monli Gupta	*Adamas Institute of Technology, Kolkata*
Subhra Mukherjee	*Narula Institute of Technology, Kolkata*
Goutam Das	*Haldia Institute of Technology, Medinipur*
Chameli Sarkar	*Sir J C Bose School of Engineering, Nadia*
Rabindranath Shaw	*Brainware Institute of Technology, Kolkata*
D Lahiri	*Techno India Group, Kolkata*
G S Taki	*Institute of Engineering and Management (IEM), Kolkata*
Sudip Dogra	*Meghnad Saha Institute of Technology, Kolkata*
Shila Ghosh	*B P Poddar Institute of Management and Technology, Kolkata*
Asim Kar	*Academy of Technology, Kolkata*
Sucharita Ghosh	*Future Institute of Engineering and Management, Kolkata*

We acknowledge the assistance and encouragement of all our colleagues and staff.

Soumitra Kumar Mandal would like to acknowledge the sincere cooperation and inspiration that he received from Dr Gurnam Singh, PEC, Chandigarh; Dr S Chatterjee, NITTTR, Chandigarh; Dr S K Bhattachariya, Director NITTTR, Kolkata; Prof. Amitabha Sinha, Director School of IT, WBUT; Dr P Shyam, Bengal Engineering College, Shibpur; Dr P Sarkar, Professor and Head, Electrical Engineering; Dr S Chattopadhay, Associate Professor; and Dr S Pal, Assistant Professor, NITTTR, Kolkata. He is also thankful to other staff of Electrical Engineering—Mr A K Das, Mr N K Sarkar, Mr S Roy Choudhury, and Mr Surojit Mallick—who helped him complete the manuscript of this book.

We are also very thankful to our family members for their continuous support, encouragement and patience throughout the writing of the manuscript of this book.

We express sincere gratitude to the entire team of McGraw Hill Education (India) in bringing out this book in a very short time. We will be extremely thankful to the readers for their constructive suggestions and views to enhance the utility of this book.

Abhijit Chakrabarti
Sudipta Debnath
Soumitra Kumar Mandal

Publisher's Note

Remember to write to us. We look forward to receiving your feedback, comments and ideas to enhance the quality of this book. You can reach us at *info.india@mheducation.com*. Kindly mention the title and the author's name as the subject. In case you spot piracy of this book, please do let us know.

ROADMAP TO THE SYLLABUS

BASIC ELECTRICAL AND ELECTRONICS ENGINEERING-II

This text is suitable for the Paper Code ES201.

PART I: BASIC ELECTRICAL ENGINEERING-II

Electrostatics: Coulomb's law; Electric field intensity; Electric field due to a group of charges; Continuous charge distribution; Electric flux; Flux density; Electric potential; Potential difference; Gauss's law; Proof of Gauss's law and its applications to electric field and potential calculation; Capacitor; Capacitance of parallel plate capacitor; Spherical capacitor; Isolated spheres; Concentric conductors; Parallel conductors; Energy stored in a capacitor

Go to *CHAPTER 1:* **ELECTROSTATICS**

DC Machines: Construction; Basic concepts of winding (lap and wave); dc generator—principle of operation, emf equation, characteristics (open circuit, load); dc motors—principle of operation; speed–torque characteristics (shunt and series machine); Starting (by 3-point starter); Speed control (armature voltage and field control)

Go to *CHAPTER 2:* **DC MACHINES**

Single-phase Transformer: Core and shell-type construction; emf equation; No-load and on-load operation; Phasor diagram and equivalent circuit; Losses of a transformer; Open and short-circuit tests; Regulation and efficiency calculation

Go to *CHAPTER 3:* **SINGLE-PHASE TRANSFORMER**

Three-phase Induction Motor: Types; Construction; Production of rotating field; Principle of operation; Equivalent circuit and phasor diagram; Rating; Torque–

speed characteristics (qualitative only); Starter for squirrel-cage and wound-rotor induction motor; Brief introduction of speed control of three-phase induction motor (voltage control; frequency control; resistance control)

Go to *CHAPTER 5:* **THREE-PHASE INDUCTION MOTORS**

General Structure of Electrical Power System: Power generation to distribution through overhead lines and underground cables with single lone diagram

Go to *CHAPTER 6:* **STRUCTURE OF A POWER SYSTEM**

Three-phase System: Voltages of three balanced phase systems; Delta and star connection; Relationship between line and phase quantities; Phasor diagrams; Power measurement by two-wattmeter method

Go to *CHAPTER 4:* **THREE-PHASE SYSTEM**

PART II: BASIC ELECTRONICS ENGINEERING-II

Field Effect Transistors: Concept of field Effect Transistors (channel width modulation); Gate isolation types; JFET structure and characteristics; MOSFET structure and characteristics; Depletion and enhancement types; CS, CT, CD configurations; CMOS: basic principles

Go to *CHAPTER 1:* **FIELD EFFECT TRANSISTORS**

Feedback Amplifiers and Oscillators: Concept (block diagram); Properties; Positive and negative feed back; Loop gain; Open loop gain; Feedback factors; Topologies of feedback amplifier; Effect of feedback on gain; Output impedance; Input impedance; Sensitivities (qualitative); Bandwidth stability; Effect of positive feedback—instability and oscillation; condition of oscillation; Barkhausen criteria

Go to *CHAPTER 2:* **FEEDBACK AMPLIFIER**
CHAPTER 3: **OSCILLATORS**

Operational Amplifier: Introduction to integrated circuits; Operational amplified and its terminal properties; Application of operational amplifier; Inverting and non-inverting mode of operation; Voltage summing and difference; Constant gain multiplier; Voltage follower; Comparator; Integrator; Differentiator; Schmitt trigger; Logarithmic amplifier

Go to *CHAPTER 4:* **OPERATIONAL AMPLIFIER**
CHAPTER 5: **APPLICATIONS OF OPERATIONAL AMPLIFIERS**

Introduction to Digital Electronics: Introduction to binary number; Basic Boolean algebra; Logic gates; and function realization with OP-AMPs

Go to *CHAPTER 6:* **NUMBER SYSTEM, BOOLEAN ALGEBRA AND LOGIC CIRCUITS**

1 ELECTROSTATICS

1.1 INTRODUCTION

In *electrostatics* we deal with static electricity (i.e, when charges are at rest). The knowledge of electrostatics is important in electrical engineering as we frequently come across the design process of electrical insulations and performance of various equipment, cables and overhead lines when subjected to electric stress. Natural phenomenon like lightning is very much related to electrostatic processes and laws. Electrostatics finds extensive applications in extra high voltage systems (ehv) in transmission engineering. *Capacitors* play a vital role in different spheres of electrical engineering as well as electronics engineering. The performance of a capacitor can be best analysed and it can be properly designed with knowledge in electrostatics.

1.2 COULOMB'S LAW

Coulomb's first law states that like charges repel each other while opposite charges attract each other. *Coulomb's second law* states that the force of attraction between two opposite charges or force of repulsion between two like charges is

(a) directly proportional to the product of the charges, the distance between them being same;
(b) inversely proportional to the square of the straight distance between them, magnitude of the charges being constant.

If we assume the charges to be of magnitude (Q) and (q) separated by a straight distance x, then from Coulomb's second law we can write

$F \propto Q \times q/x^2$, (F) being the force of repulsion if both charges are alike or force of attraction if the charges have opposite polarity. The force (F) is measured in Newtons when the magnitude of the charges are expressed in Coulombs and the distance in meters.

$$\therefore \qquad F = K\frac{Q \cdot q}{x^2} \tag{1.1}$$

(K) being constant of variation and in SI unit (K) in vacuum is given by $1/4\pi\varepsilon_o$; otherwise $K = 1/4\pi\varepsilon$, when the charges are placed in any other medium other than vacuum or space.

$$\therefore \qquad F = \frac{Q \cdot q}{4\pi\varepsilon x^2} \tag{1.2}$$

In electrical engineering we term this ε as permittivity of the medium in which charges are placed. It is known as absolute permittivity and is represented as

$$\varepsilon = \varepsilon_o \times \varepsilon_r \tag{1.3}$$

where (ε_o) is the *permittivity* of space while (ε_r) is the *relative permittivity* of the medium where the charges are placed.
In SI unit,

$$\varepsilon_o = 8.854 \times 10^{-12} \text{ Farad/metre}$$

$$\therefore \qquad \frac{1}{4\pi\varepsilon_o} = \frac{1}{4\pi \times 8.854 \times 10^{-12}} = 9 \times 10^9$$

Thus, Coulomb's law can be written as

$$F = 9 \times 10^9 \, \frac{Q \times q}{\varepsilon_r x^2}. \tag{1.4a}$$

When the charges are placed in vacuum (or space),

$$F = 9 \times 10^9 \, \frac{Q \cdot q}{x^2}. \tag{1.4b}$$

If $Q = q = 1$ Coulomb and $x = 1$ metre, from Coulombs law, $F = 9 \times 10^9$ Newtons (in space). This gives rise to the definition of *unit charge* (i.e. 1 Coulomb) which means that it is such a charge which when placed at one metre apart from another similar charge experiences a force of 9×10^9 Newton in vacuum.

1.3 PERMITTIVITY

Permittivity of a medium is basically that property of the medium which permits electric flux to pass through it. If the permittivity is more it means that the medium allows more flux to pass through it and hence this medium is more susceptible to the electric field.

Absolute permittivity (ε) is the ratio of electric flux density in a dielectric medium to the corresponding electric field strength and is expressed as Farad/meter.

i.e $$\varepsilon = \frac{\delta}{E} \text{ F/m} \tag{1.5}$$

where δ is electric flux density and E is the strength of the field.

Also, $\varepsilon = \varepsilon_o \times \varepsilon_r$, where ε_o is the permittivity of free space (8.854×10^{-12} F/m) and (ε_r) is the relative permittivity of a dielectric medium. It is defined as the ratio of flux densities of the dielectric medium to that in vacuum produced by the same electric field strength.

$$[e_r = \frac{\delta}{\delta_o} = \frac{(\varepsilon E)}{(\varepsilon_o E)} = \frac{\varepsilon}{\varepsilon_o}$$

$$\therefore \qquad \varepsilon = \varepsilon_r \times \varepsilon_0]$$

Relative permittivity of space is 1 while that of air is 1.0006. In practice, we assume ε_r of vacuum and air as 1. Commonly used dielectric medium have permittivity between 2 and 10.

1.4 ELECTRIC FLUX AND FLUX DENSITY

Electric flux represents the total number of lines of force in any electric field. It is the lines of force coming out of a positive charge of one coulomb. Electric flux is often represented by symbol ψ or ϕ and expressed in Coulombs.

Electric flux density (often represented by the sysmbol δ) may be defined as the flux per unit area, measured at right angles to the direction of electric flux. Its unit is Coulomb per sq. metre.

i.e., $d = \frac{\phi}{A}$ e/m^2, where A represents the area in m^2.

1.5 ELECTRIC POTENTIAL AND POTENTIAL DIFFERENCE

The *electric potential* at any point in an electric field is defined as the work done in joules in moving a unit positive charge from infinity (i.e., from zero potential) to that point against the electric field.

$$\therefore \qquad \text{Electric potential} = \frac{\text{Work done}}{\text{Electric charge}}$$

or
$$V = \frac{W}{Q} \tag{1.6}$$

When W is expressed in joules, Q in coulombs, V is expressed in volts. Then the electric potential at a particular point in an electric field is one volt provided one joule of work is done in moving a unit positive charge from zero potential to that point against the field.

In electrical engineering we are more interested in measuring the potential difference between two points in a field than to know the absolute value of the electric potential at any point s in the field. The *potential difference (p.d.)* is the work done in joule in moving a unit positive charge from the point of lower potential to higher potential within the field.

The potential difference is obviously measured in volts and the p.d. of one volt means one joule of work is done in bringing a unit positive charge from the point of lower potential to the point of higher potential within the electric field.

1.6 EXPRESSION FOR POTENTIAL AT A POINT WITHIN AN ELECTRIC FIELD

Let us consider two positive charges, the first one having a charge of Q coulombs while the second one is a unit positive charge. Both the charges are assumed to be placed in space at a straight distance x metres between them. From Coulomb's law we can express the force of repulsion between these two charges as

$F = \dfrac{Q \times 1}{(4\pi\varepsilon_o)x^2}$; ε_o being the permittivity of space.

The work done dW in moving the unit charge towards the charge Q for a small distance dx metre will be given as

$$dW = \left[\frac{Q}{(4\pi\varepsilon_o)x^2}(-dx)\right] \text{ joule}$$

Work done is negative as the charge is moved against a repulsive force and against the direction of the field.

In order to find the total work done in moving the unit positive charge from infinity to any point d metres away from the charge Q against the field, we will integrate the expression of dW obtained within the limit of integral ∞ to d.

$$\therefore \qquad W = \int_{\infty}^{d} \frac{Q(-dx)}{(4\pi\varepsilon_o)x^2} = \frac{-Q}{4\pi\varepsilon_o}\left[-\frac{1}{x}\right]_{\infty}^{d} = \frac{Q}{(4\pi\varepsilon_o)\cdot d} \text{ joules.}$$

Thus, from definition we can write the potential at a point d metres away from the charge Q is simply $\left(\dfrac{Q}{4\pi\varepsilon_o \cdot d}\right)$ volts.

$$\therefore \qquad V = \frac{Q}{(4\pi\varepsilon_o)\cdot d} \text{ volts} \tag{1.7a}$$

If the analysis be performed assuming the surrounding medium as a dielectric of relative permitivity ε_r, we can modify the expression for potential at distance d away from Q as

$$V = \frac{Q}{4\pi\varepsilon_o\varepsilon_r \cdot d} \text{ volts} \tag{1.7b}$$

If we consider an isolated sphere of radius R placed in space and having +ve charge Q coulombs uniformly distributed over its surface, the potential at the surface of the sphere would be

$$V = \frac{Q}{4\pi\varepsilon_o R} \tag{1.8}$$

[the charge on the sphere would act as a concentrated charge at the centre O of the sphere.]

The potential will remain constant for the space between O and R in the sphere and will be same as the potential V at the surface of the sphere. The surface of the sphere would be termed as equipotential surface and electric lines of force always cross such a equipotential surface normally. If we assume a point P outside the sphere at distance D from the centre of the sphere, we would have the potential of $V_P = Q/(4\pi\varepsilon_0 D)$ at that point outside the sphere.

1.7 ELECTRIC FIELD INTENSITY

The *intensity of the electric field* at a point is defined as the mechanical force per unit charge placed at that point. The direction of the intensity is same as direction of the force exerted on a positive charge.

Thus, if F be the force experienced by a test charge q placed at a point in an electric field, the intensity E at that point is given by

$$E = \frac{F}{q}. \tag{1.9}$$

E is expressed in newton per coulomb or in volt/metre (V/m). Frequently the term *electric field strength* is also used instead of the term electric field intensity.

Let us assume a positive point charge $+Q$ is placed at a point M and a test charge $+q$ is placed at point N, as shown in Fig. 1.1.

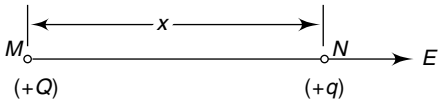


Fig. 1.1 ***A (+ve) charge (+Q) placed in an electric field***

The force F experienced by q is given by

$$F = \frac{Qq}{4\pi\varepsilon_o x^2}.$$

Since intensity E is given by F/q, we can write

$$E = \frac{Q}{4\pi\varepsilon_o x^2}. \tag{1.10}$$

The direction of E is towards the point charge or away from it according as the charge is negative or positive.

1.8 ELECTRIC FIELD INTENSITY AND POTENTIAL OF ISOLATED POINT CHARGE (Q)

Figure 1.2 represents an isolated point charge $+q$ placed in space. We are to find the field intensity and potential at point P.

Fig. 1.2 ***An isolated point charge (+q) placed in space***

To find intensity:
By definition of electric field intensity, the intensity at a point is given by (in vector form)

$$E = \frac{1}{4\pi\varepsilon_o} \times \frac{q}{r^2} \tag{1.11a}$$

where q = positive point charge
r = distance between $+q$ and point P and
ε_0 = permittivity of space

To find potential:
By definition of potental at a point P,

$$V = -\int_{\infty}^{r} |\vec{E}|\, dr = -\int_{\infty}^{r} \frac{1}{4\pi\varepsilon_o}\left(\frac{q}{r^2}\right) dr = -\left[-\frac{1}{4\pi\varepsilon_o}\left(\frac{q}{r}\right) - 0\right] = \frac{q}{4\pi\varepsilon_o r}$$

$$\therefore \qquad V = \frac{q}{4\pi\varepsilon_o r}. \tag{1.11b}$$

1.9 POTENTIAL DUE TO A GROUP OF CHARGES

The potential at a point due to a number of charges can be determined by algebraically adding the potential at that point due to each one of the charges. Let q_1, q_2, q_3, … be the charges at distances r_1, r_2, r_3 … respectively from a given point P at which we are required to find the resultant of the above charges. The resultant potential (V) is then given by

$$V = \frac{q_1}{4\pi\varepsilon_0\varepsilon_r r_1} + \frac{q_2}{4\pi\varepsilon_0\varepsilon_r r_2} + \frac{q_3}{4\pi\varepsilon_0\varepsilon_r r_3} + \ldots$$

or,
$$V = \frac{q}{4\pi\varepsilon_0\varepsilon_r}\left[\frac{1}{r_1} + \frac{1}{r_2} + \frac{1}{r_3} + \ldots\right] \tag{1.12}$$

(assuming $q_1 = q_2 = q_3 = \ldots = q$)

1.10 ELECTRIC FIELD INTENSITY AND POTENTIAL GRADIENT

Electric field strength E due to a point charge at any point in the vicinity of the charge is defined as the force experienced by a unit positive charge placed at that point within the field (Fig. 1.3). It is expressed in Newton/Coulomb (or volt/meter). If this force is stronger, the electric field strength is more. We also can state that the work done in moving a unit positive charge through a small distance dx meters in the direction of the field is given by

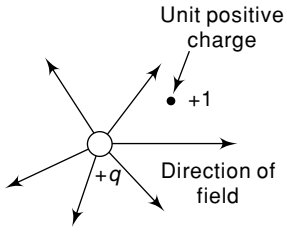


Fig. 1.3 ***A unit (+ve) charge in a field***

(dW) = force × displacement of the charge
= $E \times dx$ joules, where E is expressed in Newton/Coulomb.

Obviously this work done would be equal to the "drop" or reduction in potential as this time the unit positive charge is moved along the direction of the field and the work done would consequently be positive.

Then we can write $dV = E \times dx$

or
$$E = \frac{dV}{dx} \tag{1.13}$$

(dV/dx) is known as the *potential gradient* and is thus the drop in potential per meter in the direction of the field. It is expressed as volt/meter. We thus find that the electric field strength and potential gradient being same, both are expressed in volt/meter.

1.11 RELATION BETWEEN ELECTRIC FLUX DENSITY AND ELECTRIC FIELD INTENSITY

We have just derived

or
$$E = \frac{Q}{4\pi\varepsilon_0\varepsilon_r r^2} = \frac{Q}{4\pi\varepsilon r^2}$$

i.e.,
$$\varepsilon E = \frac{Q}{4\pi r^2}$$

The quantity εE has dimensions of charge per unit area and is equivalent to electric flux density (d).

$\therefore$
$$d = \varepsilon E = \frac{Q}{4\pi r^2} \tag{1.14}$$

1.12 ELECTRIC POTENTIAL ENERGY

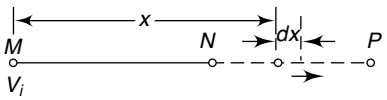


Fig. 1.4 ***A system of two charges***

Let us consider a system of two charges Q_1 and Q_2. Suppose Q_1 is a fixed charge at a point M while the charge Q_2 is taken from a point N to a point P along the line MNP (Fig. 1.4).

Let distance $MN = x_1$, while distance $MP = x_2$. We consider a small displacement of charge Q_2. Its distance from M then changes to $(x + dx)$. The electric force on Q_2 is given by

$$F = \frac{Q_1 Q_2}{4\pi\varepsilon_o x^2}, \text{ in direction } M \text{ to } N.$$

[We assume the medium in which the charges are placed in space and hence $\varepsilon_r = 1$]

The work done by the force in making small displacement dx by the charge is

$$dW = \frac{Q_1 Q_2}{4\pi\varepsilon_o x^2} \cdot dr$$

[$\because$ Work done = force × displacement]
The total work done as Q_2 moves from N to P is thus

$$W = \int_{x_1}^{x_2} \frac{Q_1 Q_2}{4\pi\varepsilon_o x^2} \cdot dx$$

$$= \frac{Q_1 Q_2}{4\pi\varepsilon_o}\left[\frac{1}{x_1} - \frac{1}{x_2}\right] \text{ joule} \tag{1.15}$$

[Charges are expressed in Coulomb and distance in metres]
[It may be noted here that no work is done by the electric force on the charge Q_1 as it remains fixed.]
The change in potential energy is thus

$$u(x_2) - u(x_1) = -W = -\frac{Q_1 Q_2}{4\pi\varepsilon_o}\left[\frac{1}{x_1} - \frac{1}{x_2}\right]$$

$$= \frac{Q_1 Q_2}{4\pi\varepsilon_o}\left[\frac{1}{x_2} - \frac{1}{x_1}\right] \tag{1.16}$$

[We define *change in electric potential energy* of the system as negative of work done by the electric force.]

If one charge is placed at infinity, its potential is zero and consequently $u(\infty) = 0$.

The potential energy, when the separation is x, can be obtained as

$$U(x) = u(x) - u(\infty)$$

$$= \frac{Q_1 Q_2}{4\pi\varepsilon_o}\left(\frac{1}{x} - \frac{1}{\infty}\right) = \frac{Q_1 Q_2}{4\pi\varepsilon_o x} \tag{1.17}$$

The equations derived here assume that one of the charges is fixed and the other is moving. However, the potential energy depends essentially on the separation between charges and is independent of the spatial location of the charged particles.

1.13 RELATION BETWEEN ELECTRIC FIELD STRENGTH AND POTENTIAL

Let us suppose the electric field at a point n due to a charge distribution is E, while the electric potential at the same point is V. Let us assume the point charge of strength q is moved slightly from the point x to $(x + dx)$. The force on the charge is $F = q \times E$, while the work done is

$$dW = F(-dx) = qE(-dx)$$

[In article 1.8, we have assumed dx in the direction of the field, i.e. from +q towards infinity. If any charge is moved against the field, dx becomes –ve.] The change in potential energy due to this displacement is

$$du = +dW = -q \times E \times dx.$$

The change in potential is $dV = \dfrac{du}{q}$ i.e. $dV = -E\,dx$.

[If the test charge is moved along the field, $dV = E \times dx$ (as shown in article 1.8).]

Integrating between x_1 and x_2, we get

$V_2 - V_1 = -\int_{x_1}^{x_2} E dx$, where V_2 and V_1 are the potentials at x_2 and x_1 respectively.

If we select point x_1 as reference having zero potential, we can write $V(r) = -\int_{\infty}^{x} E \cdot dx$, where x is distance equal to x_2.

1.14 ELECTRIC FIELD INSIDE A CONDUCTOR

When there is no electric field around a conductor the conduction electrons are almost uniformly distributed within the conductor. In any small volume of the conductor the number of electrons is equal to the number of proton in the nuclei of each atom of the conductor. The net charge in the volume is then zero. Next we suppose that an electric field E is created in the direction left to right across the conductor. This field will exert a force on the free electrons in the atoms of the conductor from right to left. The free electron then move towards the left and consequently the number of electrons in the left will increase while the number of electrons in the right decreases. The left side of the conductor then becomes negatively charged while the right side is positively charged. The electron continue to drift towards the left. The result is the creation of an electric field of strength $E¢$ within the conductor in the direction opposite to the applied field. With passage of time a situation comes when the field E' inside the conductor is equal to the magnitude of the external field E. The net electric field inside the conductor is zero. Then a steady state is reached when some positive and negative charges appear at the surface of the conductor while there is no electric field inside the plate. Thus there is no electric field inside the conductor when it is subjected to an external electric field. The redistribution of electrons take place in such a way that charges remain at the surface of the conductor only.

It may be recalled here from the basic concepts of physics that in conductors there is always existence of free electrons while in insulators all atomic electrons are tightly bound to their respective nuclei. When insulators are placed in an electric field they may slightly shift their parent position but cannot drift from their parent atoms and hence cannot move long distance. These materials are then said to act as dielectrics. If the external field is strengthened further, a time will come when the bonding of the electron with their nuclei may break causing them to drift apart. We call this phenomenon as breakdown of dielectric medium.

1.15 CONTINUOUS CHARGE DISTRIBUTION

It is impractical to work in terms of discrete charges and we need to work with continuous charge distributions. It is impractical to specify the charge distribution on the surface of a charged conductor in terms of the locations of the microscopic charged constituents. It is more logical to consider an area element ΔS on the surface of the conductor (which is very small on the macroscopic scale but large enough to include a very large number of electrons) and specify the charge ΔQ on that element. The surface charge density can be defined as

$$\delta = \frac{\Delta Q}{\Delta S}$$

The unit of δ is C/m^2. The surface charge density δ ignores the quantisation of charge and the discontinuity in charge distribution at the microscopic level. δ represents the macroscopic surface charge density which is a smoothed average of the microscopic charge density over an area element ΔS which is large microscopically but small macroscopically.

Similarly, we can define linear charge density λ and volume charge density ρ.

$$\lambda = \frac{\Delta Q}{\Delta l}$$

where Δl is a small line element of wire on the macroscopic scale which, however, includes a large number of microscopic charged constituents and ΔQ is the charge contained in that line element. The unit for λ is c/m.

Now,
$$\rho = \frac{\Delta Q}{\Delta V}$$

where ΔQ is the charge included in the macroscopically small volume element ΔV that includes a large number of microscopic charged constituents. Unit of ρ is c/m^3.

Now, suppose a continuous charge distribution in space has a charge density ρ. The charge distribution is divided into small volume elements of size ΔV. The charge in volume element ΔV is $\rho \Delta V$. Then the electric field at any general point P due to the charge $\rho \Delta V$ is given by Coulomb's law:

$$\Delta E = \frac{\rho \Delta V}{4\pi \varepsilon_o r^2}$$

where r is the distance between the charge element and P. By the Superposition principle, the total electric field due to the charge distribution is obtained by adding over electric fields due to different volume elements:

$$E = \frac{1}{4\pi \varepsilon_o} \sum_{\Delta V} \frac{\rho \Delta V}{r^2}$$

By using Coulomb's law and the Superposition principle, electric field can be determined for any charge distribution, discrete or continuous, or part discrete and part continuous.

1.16 GAUSS'S LAW AND ITS DERIVATION

Statement of Gauss's Law The flux of the net electric field through a closed surface is equal to the net charge enclosed by the surface divided by ε_o.

i.e., $$\oint E \cdot ds = \frac{q_{in}}{\varepsilon_o} \tag{1.18}$$

where $\oint E \cdot ds$ represents the flux ϕ through a closed surface and q_{in} is the net charge enclosed by the surface through which the flux passes.

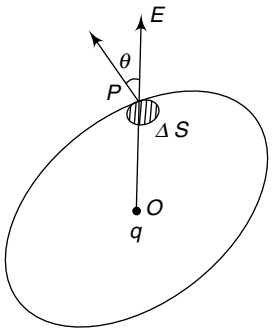


Fig. 1.5 ***A charge (q) placed inside a closed surface***

Derivation of Gauss's Law from Coulomb's Law
Let us suppose that a charge q is placed at a point O inside a closed surface (Fig. 1.5). We assume a point P on the surface and consider a small area Ds on the surface around P.

Let OP = x.

The electric field at point P due to the charge q is given by, $E = q/4\pi\varepsilon_o \cdot x^2$, directed along the line OP.

Let us suppose this line OP makes an angle (θ) with the outward normal to the surface Δs. The flux of the electric field through Δs is given by

$$\begin{aligned} Df &= E\,\Delta s \cos q \\ &= \frac{q}{4\pi\varepsilon_o x^2} \cdot \Delta s \cos q \\ &= \frac{q}{4\pi\varepsilon_o} \cdot \Delta s \end{aligned}$$

where $\Delta\sigma = \dfrac{\Delta s \cdot \cos\theta}{x^2}$ [Actually ($\Delta\sigma$) is the solid angle subtended by (Δs) at O]

$$\therefore \qquad f = \sum \frac{q}{4\pi\varepsilon_o} \cdot Ds = \frac{q}{4\pi\varepsilon_o} \sum \Delta\sigma$$

We can see that [S(Ds)] represents the sum that is actually the total solid angles subtended by a closed surface at O. Obviously this total solid angle is 4p.

$\therefore$ the total flux of the electric field due to the internal charge q through the closed surface is

$$f = \frac{q}{4\pi\varepsilon_o} \cdot 4\pi = \frac{q}{\varepsilon_o}$$

$\because$ $\phi \equiv \oint E \cdot ds$, hence we have

$$\oint E \cdot ds = \frac{q_{in}}{\varepsilon_o} \text{ (proof of Gauss's law)} \tag{1.19}$$

where, $\frac{q_{in}}{\varepsilon_o} = \sum \frac{q_i}{\varepsilon_o}$ (i.e. the sum of all charges $q_1, q_2, \ldots, q_i, \ldots q_n$ located in the said closed surface. We do not consider external charges as the solid angle (Ds) subtended by a closed surface at any external point is zero, then f becomes zero.

1.17 APPLICATIONS OF GAUSS'S LAW

The electric field for symmetric charge configurations can be obtained in a simple way using Gauss's law. This can be understood by considering the following cases

1.17.1 Field due to an Infinitely Long Straight Uniformly Charged Wire

Consider an infinitely long thin straight wire with uniform linear charge density λ. To calculate the field, imagine a cylindrical Gaussian surface with radius r as shown in Fig. 1.6. The wire is obviously an axis of symmetry. Since the field is everywhere radial, flux through the two ends of the cylindrical Gaussian surface is zero. At the cylindrical part of the surface, E is normal to the surface at every point and its magnitude is constant, since it depends only on r. The surface area of the curved part is $2\pi rl$, where l is the length of the cylinder.

Flux through the Gaussian surface

= Flux through the curved cylindrical part of the surface

$= E \times 2\pi rl$

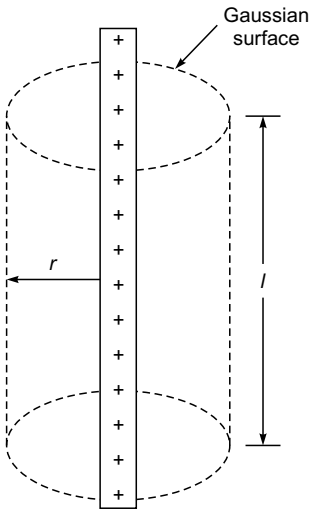


Fig. 1.6 *Gaussian surface for a long thin wire of uniform linear charge density*

The surface includes charge equal to λl where λ is the linear charge density in the wire in c/m. According to Gauss's law,

$$E \times 2\pi rl = \lambda l/\varepsilon_o$$

or

$$E = \frac{l}{2\pi\varepsilon_o r} \tag{1.20}$$

It may be noted that though only the charge enclosed by the surface (λl) was included above, the electric field E is due to the charge on the entire wire. Also, we have to assume that the wire is infinitely long. Otherwise, we cannot take E to be normal to the curved part of the cylindrical Gaussian surface. Equation (1.20) is approximately true for an electric field around the control portions of a long wire, where the end effects may be ignored.

1.17.2 Field due to a Uniformly Charged Infinite Plane Sheet

Let δ be the uniform surface charge density of an infinite plane sheet as shown in Fig. 1.7. By symmetry, the electric field will not depend on y and z coordinates and its direction at every point must be parallel to the x-direction.

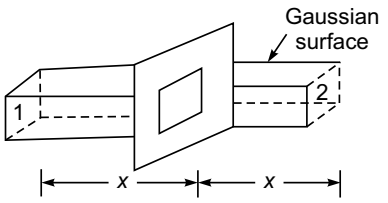


Fig. 1.7 *Gaussian surface for a uniformly charged infinte plane sheet*

We consider a Gaussian surface to be a rectangular parallelpiped of cross-sectional area A as shown in Fig. 1.7. Only two faces 1 and 2 will contribute to the flux; electric field lines are parallel to the other faces and they, therefore, do not contribute to the total flux.

The unit vector normal to the surface 1 is in the $-x$ direction, whereas the unit vector normal to the surface 2 is in the $+x$ direction. Hence, $E \cdot \Delta S$ through both the surfaces are equal. Therefore, the net flux through the Gaussian surface is $2EA$. The charge enclosed by the closed surface is δA. Hence, by Gauss's law,

$$2EA = \delta A/\varepsilon_o$$

or,
$$E = \frac{\delta}{2\varepsilon_o}$$

E is directed away from the plate if δ is positive and toward the plate if δ is negative. E is independent of x.

1.17.3 Field due to Uniformly Charged Thin Spherical Shell

Let δ be the uniform surface charge density of a thin spherical shell of radius R. The field at any point P, outside or inside can depend only on r, where r is the radial distance (from the centre of the shell to the point) and must be radial.

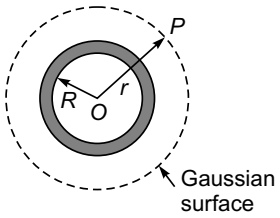


Fig. 1.8(a) *Gaussian surface for point outside the shell*

(a) Field Outside the Shell First, we consider the point P outside the shell. To calculate E at the point P, consider the Gaussian surface to be a sphere of radius r and with centre O, passing through P as shown in Fig. 1.8 (a). All points on this sphere are equivalent relative to the given charged configuration. The electric field at each point on the Gaussian surface has the same magnitude E and same direction. Hence, E and ΔS at every point are parallel and flux through each element is $E\Delta S$. Hence, total flux through the Gaussian surface is $E \times 4\pi r^2$.

By Gauss's law,

$$E \times 4\pi r^2 = \frac{\delta}{\varepsilon_o}\ 4\pi R^2$$

or,
$$E = \frac{\delta R^2}{\varepsilon_o r^2} = \frac{Q}{4\pi\varepsilon_o r^2}$$

where $Q = 4\pi R^2\delta$ is the total charge on the spherical shell.

The electric field is directed outward if $Q > 0$ and inward if $Q < 0$. Thus, for all points outside the shell, the field due to a uniformly charged shell is as if the entire charge of the shell is concentrated at the centre.

(b) Field Inside the Shell Here, we consider the point P inside the shell as shown in Fig. 1.8(b). The Gaussian surface is again a sphere through P centred at 0. The flux through the Gaussian surface is $E \times 4\pi r^2$. But in this case, the Gaussian surface encloses no charge. Hence, Gauss's law gives

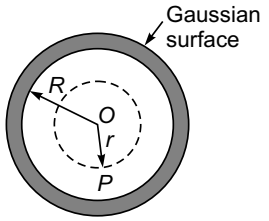


Fig. 1.8(b) ***Gaussain surface for point inside the shell***

$$E \times 4\pi r^2 = 0$$

or
$$E = 0$$

Hence, the field due to a uniformly charged thin shell is zero at all points inside the shell.

1.1 Three equal charges, each of magnitude 3.0×10^{-6}C, are placed at three corners of a right-angled triangle of sides 3 cm, 4 cm and 5 cm. Find the force on the charge at the right-angle corner.

Solution

Force on A due to B (Fig. 1.9)

$$(= F_1) = \frac{(3.0\times10^{-6})(3.0\times10^{-6})}{4\pi\varepsilon_o(4\times10^{-2})^2}$$

$$= 9 \times 10^9 \times 9.0 \times 10^{-12} \times \frac{1}{16\times10^{-4}}$$

$$= 5.0625 \times 10^1 = 50.625 \text{ N}.$$

This force acts along BA. Similarly, force on A due to C is, $F_2 = 90\ N$ in direction CA.

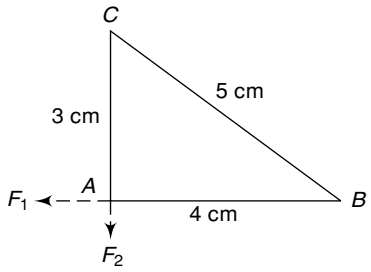


Fig. 1.9 ***Right-angled triangle of Ex. 1.1***

$\therefore$ Net electric force $= F = \sqrt{F_1^2 + F_2^2}$

$$= \sqrt{(50.625)^2 + (90)^2}$$

$$= 103.261 \text{ N}.$$

The resultant makes an angle of q with BA where $\tan q = \frac{90}{50.625} = 1.778$.

1.2 A charge Q is divided between two point charges. What should be the values of the charges on the objects so that the force between them is maximum?

Solution

Let charge on the objects be q and $(Q - q)$.

$$\therefore \text{ force between them } (= F) = \frac{q(Q-q)}{4\pi\varepsilon_o d^2} \tag{i}$$

where d is the distance between them.

For maximum F, numerator of (i) is maximum. Let $q(Q - q) = y$.

$\therefore$ y should be maximum.

Differentiating y w.r.t. (q) we get

$$\frac{dy}{dq} = Q - 2q.$$

Equating to zero (to get the maxima of y), $Q - 2q = 0$ or $q = Q/2$.

Thus, the charge should be equally distributed between the objects.

1.3 An infinite number of charges each equal to Q coulomb are placed along the x-axis at $x = 1$, $x = 2$, $x = 8$,… and so on. Find the potential and the electric field at the point $(x = 0)$ due to these charges. What will be the potential and electric field if, in the above setup, the consecutive charges have opposite signs?

Solution

Refering to Fig. 1.10, the potential at $x = 0$ due to this set of charges is given by

$$V = \frac{1}{4\pi\varepsilon_o}\left(\frac{q}{1}+\frac{q}{2}+\frac{q}{4}+\frac{q}{8}+\ldots\right)$$

$$= \frac{q}{4\pi\varepsilon_o}\left(1+\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\ldots\right)$$

$$= \frac{q}{4\pi\varepsilon_o}\times\frac{1}{1-1/2} = \frac{2q}{4\pi\varepsilon_o}$$

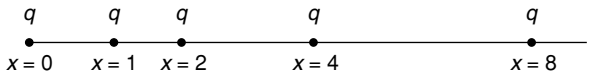


Fig. 1.10 ***Infinite number of charges placed along x-axis (Ex. 1.3)***

Since the point charges are along the same straight line, the intensities at $x = 0$ are also along the x-axis.

$$E = \frac{1}{4\pi\varepsilon_o}\left[\frac{q}{1^2}+\frac{q}{2^2}+\frac{q}{4^2}+\frac{q}{8^2}+\ldots\right]$$

$$= \frac{q}{4\pi\varepsilon_o}\left[1+\frac{1}{4}+\frac{1}{16}+\frac{1}{64}+\ldots\right]$$

$$= \frac{1}{4\pi\varepsilon_o}\left\{\frac{q}{1-1/4}\right\} = \frac{1}{4\pi\varepsilon_o}\times\frac{4q}{3} = \frac{q}{3\pi\varepsilon_o}$$

If the consecutive charges are of opposite sign, the potential at $x = 0$ is

$$V = \frac{1}{4\pi\varepsilon_o}\left(\frac{q}{1} - \frac{q}{2} + \frac{q}{4} - \frac{q}{8} + \frac{q}{16} - \frac{q}{32} + \ldots\right)$$

$$= \frac{q}{4\pi\varepsilon_o}\left\{\left(1 + \frac{1}{4} + \frac{1}{16} + \ldots\right) - \left(\frac{1}{2} + \frac{1}{8} + \frac{1}{32} + \ldots\right)\right\}$$

$$= \frac{q}{4\pi\varepsilon_o}\left\{\frac{1}{1-1/4} - \frac{1}{2} \times \frac{1}{1-1/4}\right\} = \frac{q}{4\pi\varepsilon_o}\left[\frac{4}{3} - \frac{2}{3}\right]$$

$$= \frac{q}{6\pi\varepsilon_o}$$

$\therefore$ $$V = \frac{1}{4\pi\varepsilon_o}\left(\frac{2q}{3}\right)$$

The electric field intensity at $x = 0$ is

$$E = \frac{1}{4\pi\varepsilon_o}\left\{\frac{q}{(1)^2} - \frac{q}{(2)^2} + \frac{q}{(4)^2} - \frac{q}{(16)^2} \ldots\right\}$$

$$= \frac{q}{4\pi\varepsilon_o}\left\{\left(1 + \frac{1}{16} + \frac{1}{256} + \ldots\right) - \left(\frac{1}{4} + \frac{1}{64} + \frac{1}{1024} + \ldots\right)\right\}$$

$$= \frac{q}{4\pi\varepsilon_o}\left\{\frac{1}{1-1/16} - \frac{1}{4} \times \frac{1}{1-1/16}\right\}$$

$$= \frac{q}{4\pi\varepsilon_o}\left\{\frac{16}{15} - \frac{1}{4} \times \frac{16}{15}\right\}$$

$$= \frac{1}{4\pi\varepsilon_o}\left(\frac{4q}{5}\right)$$

1.4 Some equipotential surfaces are shown in Fig. 1.11(a) and 1.11(b). What are the magnitudes and directions of the electric field intensity for these two figures?

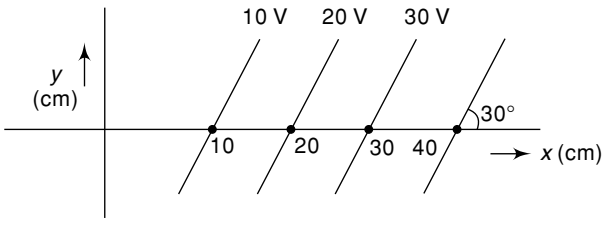


Fig. 1.11(a) *Equipotential surfaces (linear)*

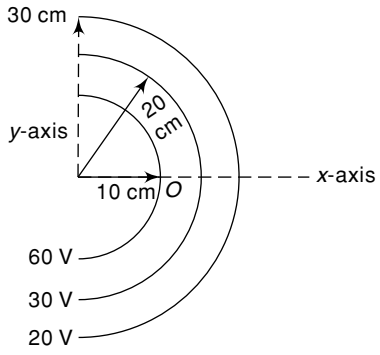


Fig. 1.11(b) ***Equipotential surfaces (circular)***

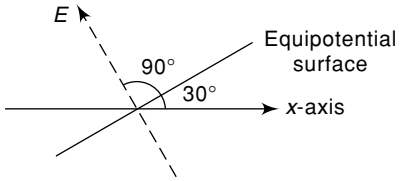


Fig. 1.11(c) ***Direction of field of equipotential surfaces shown in Fig. 1.18***

Solution

We know electric field is normal to the equipotential surface in the direction of the decreasing potential.

Thus for the equipotential surfaces of Fig. 1.11(a), the field will be at an angle making an angle 120° to the x-axis (Fig. 1.11(c)).

Magnitude of the electric field in this case is

$$E\cos 120° = -\frac{(20-10)}{(20-10)10^{-2}}\left[\because E = -\frac{dv}{dx}\right]$$

or $$E'\left(-\frac{1}{2}\right) = -\frac{10}{0.10}$$

$\therefore$ $$E = 200 \text{ V/m}.$$

In Fig. 1.11(b), direction of electric field will be radially outward, similar to a point charge kept at centre, i.e. $V = \frac{Kq}{r}$, (r) being the radius.

When $$V = 60 \text{ V},$$

$$60 = \frac{Kq}{(0.1)}$$

$\therefore$ $$Kq = 6.$$

Then, potential at any distance from the centre is

$$V(r) = \frac{6}{r}\left[\because V = \frac{Kq}{r}\right]$$

Hence $$E = -\frac{dv}{dr} = \left(\frac{6}{r^2}\right) \text{ V/m}$$

1.5 A square frame of edge 20 cm is placed with its positive normal making an angle of 60° with a uniform electric field of 10 V/m. Find the flux of the electric field through the surface bounded by the frame.

Solution

The situation is displayed in Fig. 1.12. The surface considered is plane and the electric field is uniform. The flux is

$$\Delta f = E\,\Delta S \cos 60°$$

$$= (10 \text{ V/m})\left(20 \times 20 \times \frac{1}{2} \times 10^{-4} \text{ m}^2\right)$$

$$= 0.2 \text{ V.m.}$$

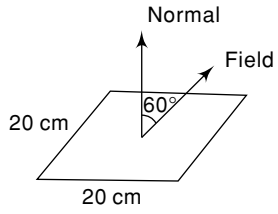


Fig. 1.12 ***Situation of the square of Ex. 1.5***

1.6 A charge q is placed at the centre of a sphere (Fig. 1.13). Taking the outward normal as positive, find the flux of the electric field through the surface of the sphere due to the enclosed charge.

Solution

The electric field here is radially outward and has the magnitude $q/4\pi\varepsilon_o r^2$, (r) being the radius of the sphere. As the positive normal is outward, $Q = 0$ and the flux through this part is

$$Df = \bar{E}\ DS = \frac{q}{4\pi\varepsilon_o r^2} \times \Delta S.$$

Summing over all the parts of the spherical surface,

$$f = \sum \Delta\phi = \frac{q}{4\pi\varepsilon_o r^2} \sum \Delta S = \frac{q}{4\pi\varepsilon_o r^2} \cdot 4\pi r^2$$

$$= \frac{q}{\varepsilon_o}.$$

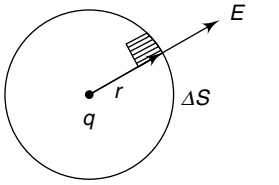


Fig. 1.13 ***(+q) charge is placed at the centre of a sphere (Ex. 1.6)***

1.18 CAPACITOR AND CAPACITANCE

A combination of two conductors placed close to each other and separated by a dielectric medium forms a *capacitor*. One of the conductors is given a positive charge (+Q) while the other one is charged by the same amount of negative charge (–Q). The conductor with (+Q) charge is called the *positive plate* while that with (–Q) charge is known as the *negative plate*. The charge stored in the positive or in the negative plate is the charge on the capacitor [note that the total charge on the capacitor is (+Q + (–Q)) zero]. The potential difference (V) between the plates is called the *potential of the capacitor*. If the positive plate has a potential V(+) while the negative plate has a potential V(–), then (V) = V(+) – V(–).

For any given capacitor, the charge Q on the capacitor is proportional to the p.d. (V) between the plates-

i.e. $Q \propto V$

or $Q = CV.$ (1.21)

The constant of proportionality being C, it is called *capacitance* of the capacitor. It depends on the shape, size and geometrical spacing of the conductors as well as the medium between them.

In *SI* system, capacitance is expressed in coulomb/volt and is termed as *Farad*. Since Farad is a large unit by magnitude, in electrical engineering frequently *microfarad* (10^{-6} F) or μF is used.

If $Q = 1$, $V = 1$, then $C = 1$F, i.e. the capacitor is one Farad if it requires a charge of one coulomb when the potential difference is one volt across its plates. It may be noted here that when the capacitor is fully 'charged' i.e., if it is full to its capacity of containing charges across a voltage source, then the p.d. across its plates is always equal to the magnitude of the voltage source.

1.18.1 Series and Parallel Connection of Capacitors

(a) Capacitors in Series Let us assume three capacitors of capacitances (C_1), (C_2) and (C_3) are connected in series across a dc supply of potential difference (V) through a switch K(Fig. 1.14). On closing the switch, the capacitors get charged and at steady state the p.d. across (C_1), (C_2) and (C_3) are (V_1), (V_2) and (V_3) respectively while the charge in each capacitor is (Q) (since the capacitors are connected in series, same charging current would flow resulting in accumulation of charge (Q) in each capacitor).

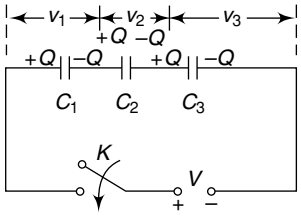


Fig. 1.14 ***Capacitors in series connection***

Obviously,

$$V_1 = \frac{Q}{C_1}; \quad V_2 = \frac{Q}{C_2}; \quad V_3 = \frac{Q}{C_3}$$

Since $V = V_1 + V_2 + V_3$, we can write

$$\frac{Q}{C} = \frac{Q}{C_1} + \frac{Q}{C_2} + \frac{Q}{C_3}$$

or $\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$ [(C) being the hypothetical capacitance equivalent to three capacitances (C_1), (C_2) and (C_3) in series].

$\therefore$ for n number of capacitances in series,

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \ldots + \frac{1}{C_n} \tag{1.22}$$

Thus we can conclude that for series connection of capacitance across a voltage source, the charge on each capacitor being same while the voltages vary. Also, the sum of individual voltage drops across each capacitor gives the total supply voltage. *The reciprocal of the equivalent capacitance of the series combination is equal to the sum of the reciprocals of the capacitances of the individual capacitors*.

(b) Capacitors in Parallel In this arrangement (Fig. 1.15) on closing K, charges Q_1, Q_2 and Q_3 would accumalate in capacitances C_1, C_2 and C_3 during steady state while the voltage will remain V across each capacitors in the parallel combination. Obviously,

$$Q = Q_1 + Q_2 + Q_3,$$

where Q is the total charge drained from the source.

or $$CV = C_1V + C_2V + C_3V$$

[(C) is assumed to be the equivalent hypothetical capacitance of this parallel combination of capacitance]

i.e., $$C = C_1 + C_2 + C_3 \qquad (1.23)$$

Generalising for n number of capacitances

Thus, in case of parallel combination of capacitances (where voltage across each capacitance remain the same but the capacitors share the charge depending on the value of their capacitance), *the equivalent capacitance is equal to the sum of their individual capacitance*.

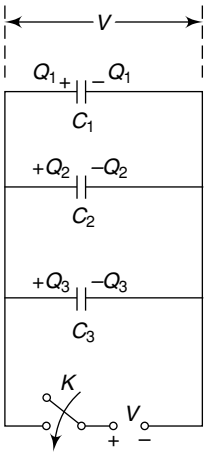


Fig. 1.15 ***Capacitors in parallel connection***

1.18.2 Concept of Dielectric Strength

Dielectric strength is the potential gradient required to cause breakdown of a dielectric medium. It is usually expressed in megavolts/millimetre (MV/mm). Dielectric strength depends on the moisture content, carbon content or presence of other impurity and thickness of the medium. With pressure of moisture and other impurities, dielectric strength drops while with increase of thickness the dielectric strength increases.

1.19 TYPES OF CAPACITORS COMMONLY USED

Depending or the nature of dielectric medium the following types of capacitors are usually available:

(a) Air Capacitors These have two sets of metal foils (aluminium or brass) and the inbetween medium is ordinary air. These capacitors are used in voltage ranges 100 V to 3000 V and the capacity varies up to 500 μF.

(b) Paper Capacitors These have a pair of elongated foil of metal (aluminium or copper or tin) interrelated with oil impregnated paper. Multiple layers of foils with paper is available. They can be used in the range of 100 V to 100 KV and is applicable for both AC and DC circuits. The capacitances are small and is usually in the range of pF.

(c) Mica Capacitors These consist of a series of aluminuim or tin foils separated by very thin layers of mica sheets. Usually multiple sheets are used and alternate plates are connected to each other. These capacitors are used in the range of 100–500 V and the capacitances in the range of pF to μF. These capacitors can be used in AC circuits.

(d) Ceramic Capacitors These capacitors are made of discs of ceramic material and the parallel facing surfaces are coated with silver. They have application in the range of a few volts to 3000 volts and the capacitances are from low values of pF to low values of μF. They are extensively used in AC and DC circuit.

(e) Electrolytic Capacitors Usually, aluminium foils or cylinders are used as electrodes while electrolytes like porous paper, plastic, aluminium oxide, tantalum powder, etc. are used as dielectric. These capacitors are used in DC circuits and applicable in the range of 1 V to 1 kV. The range of capacitances are usually from 1pF to even Farad.

1.20 CAPACITANCE OF A PARALLEL-PLATE CAPACITOR

Let us consider two identical plates A and B are kept in close proximity and parallel to each other and separated by a dielectric medium of thickness (x) metre and relative permittivity (ε_r) (Fig. 1.16). Let us connect the parallel plates with a potential difference (V) volts and we assume (Q) coulombs of charge is accumulated by the parallel plate combination acting on a parallel plate capacitor. The electric flux is ψ is due to (Q) coulombs and the area of each plate is considered to be (A) square metres.

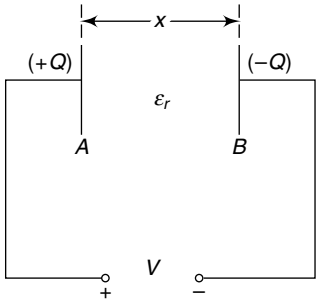


Fig. 1.16 ***Parallel-plate capacitor***

Since the charge Q is distributed uniformly over each plate, the electric field between the plates is nearly uniform. Let δ represent the electric flux density while E the intensity (or the potential gradient) and C the capacitance in Farads for this parallel plate capacitor.

Here

$$\delta = \frac{\psi}{A} = \frac{Q}{A} \text{ coulomb/square metre.}$$

But $$E = \frac{V}{x}, \; V \text{ being the potential;}$$

also, $$\frac{\delta}{E} = \varepsilon \text{ [see equation (1.5)]}$$

or $$\frac{Q/A}{V/x} = \varepsilon = \varepsilon_o \times \varepsilon_r$$

$\therefore$ $$\frac{Q}{V} = C = \frac{\varepsilon_o \varepsilon_r \times A}{x} \text{ Farad.} \qquad (1.24a)$$

If the dielectric medium of the capacitance is vacuum, $\varepsilon_r = 1$ and hence

$$C = \frac{\varepsilon_o A}{x} \tag{1.24b}$$

Hence, we find capacitance C of a parallel plate capacitor becomes

(i) proportional to the area of the plate,
(ii) inversely proportional to the distance of separation (x) between plates, and
(iii) directly proportional to the relative permittivity of the medium of separation of plates.

1.21 CAPACITANCE OF A MULTI-PLATE CAPACITOR

We just obtained the capacitance of a parallel plate capacitor having only two plates held in parallel. If there are n number of parallel plates, each being identical to the other and alternate plates being connected to the same polarity of the supply potential (Fig. 1.17). We can say that there are $(n - 1)$ space between n number of parallel plates. Thus the capacitor is equivalent to $(n - 1)$ number of parallel plate capacitor consisting of two parallel plates.

$\therefore$ Total capacitance C of multiple parallel plate capacitor (containing n number of plates)

$= (n - 1) \times$ capacitance of one pair of plates

$$= (n - 1) \times \frac{\varepsilon_o \varepsilon_r A}{x} \text{ Farad} \tag{1.25}$$

where ε_o = absolute permittivity of space,
ε_r = relative permittivity of dielectric medium,
x = thickness of dielectric medium between any two parallel plates in metres, and
A = area of each plate in m^2.

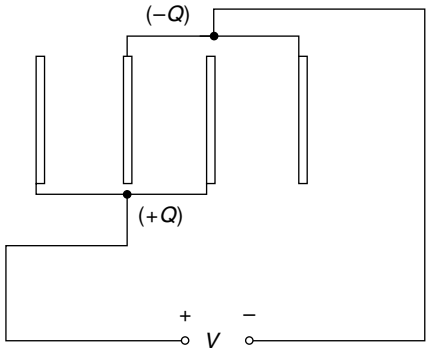


Fig. 1.17 *Alternate plates of a parallel-plate capacitor being connected to same polarity*

1.22 CAPACITANCE OF A PARALLEL-PLATE CAPACITOR WITH COMPOSITE DIELECTRICS

Let us assume a parallel plate capacitor with two different dielectrics having relative permittivities ε_{r_1} and ε_{r_2}. The separation of plates are x_1 and x_2 metres, as shown in Fig. 1.18. The plates are of identical cross-sectional area (A) square metre and the charge accumulated in the capacitor is Q coulombs when a p.d. of (V) volts is applied across the capacitor terminals.

Electric flux density is given by

$$d = \frac{\psi}{A} = \frac{Q}{A} \text{ coulomb/m}^2.$$

Since $\varepsilon = \frac{\delta}{E}$, E being the electric field intensity, we can write

$$\varepsilon_1 = \frac{\delta}{E_1} \text{ and } e_2 = \frac{\delta}{E_2}$$

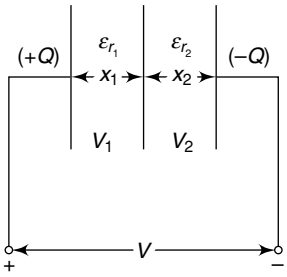


Fig. 1.18 ***Parallel-plate capacitor with composite dielectric***

i.e. $$E_1 = \frac{\delta}{\varepsilon_1} = \frac{\delta}{\varepsilon_o \varepsilon_{r_1}}$$

and $$E_2 = \frac{\delta}{\varepsilon_2} = \frac{\delta}{\varepsilon_o \varepsilon_{r_2}}.$$

If V_1 and V_2 be the p.d. across the respective dielectrics, we can write

$$V = V_1 + V_2$$

$$= E_1 x_1 + E_2 x_2 \left[\because \text{Intensity } E = \frac{\text{Potential } (V)}{\text{Distance } (x)} \right]$$

$$= \frac{\delta}{\varepsilon_o \varepsilon_{r_1}} \cdot x_1 + \frac{\delta}{\varepsilon_o \varepsilon_{r_2}} \cdot x_2$$

$$= \frac{\delta}{\varepsilon_o} \left[\frac{x_1}{\varepsilon_{r_1}} + \frac{x_2}{\varepsilon_{r_2}} \right]$$

$$= \frac{Q}{\varepsilon_o A} \left[\frac{x_1}{\varepsilon_{r_1}} + \frac{x_2}{\varepsilon_{r_2}} \right]$$

$$\therefore \text{ Capacitance } (C) = \frac{Q}{V} = \frac{Q}{\frac{Q}{\varepsilon_o A} \left[\frac{x_1}{\varepsilon_{r_1}} + \frac{x_2}{\varepsilon_{r_2}} \right]}$$

or $$C = \frac{\varepsilon_o A}{\left[\frac{x_1}{\varepsilon_{r_1}} + \frac{x_2}{\varepsilon_{r_2}} \right]} \text{ Farad} \qquad (1.26a)$$

i.e. $$C = \frac{\varepsilon_o A}{\sum \frac{x}{\varepsilon_r}}, \text{ for more number of dielectrics.} \qquad (1.26b)$$

1.23 CAPACITANCE OF AN ISOLATED SPHERE

We have seen earlier that in case of an isolated sphere, charged with Q coulombs of electricity, the potential at the surface is given by

$$V = \frac{Q}{4\pi\varepsilon_o R},$$

R being the radius of the sphere. V being expressed in volts, we can find the capacitance of this sphere as

$$C = \frac{Q}{V} = 4\pi\varepsilon_o R \text{ Farad.}$$

If the medium within the sphere is filled up with a dielectric medium of relative permittivity ε_r, we can modify this expression of capacitance as

$$C = 4\pi\,\varepsilon_o\,\varepsilon_r\,R \text{ Farad.} \tag{1.27}$$

1.24 CAPACITANCE OF CONCENTRIC SPHERES

A pair of concentric sphere S_1 and S_2 of radii R_1 and R_2 metres, separated by a dielectric medium of permittivity ε_r forms a spherical capacitance. We will consider two cases of this spherical capacitor.

Case-A

S_2 (the outer sphere) is earthed Let the inner sphere S_1 be charged by $(+Q)$ coulomb of charge. It will induce $(-Q)$ coulomb charge at the inner surface of S_2 and $(+Q)$ coulomb charge at the outer surface of S_2. But as the outer surface of S_2 is earthed, this $(+Q)$ charge at the outer surface of S_2 will escape (e_1) to the earth (Fig. 1.19).

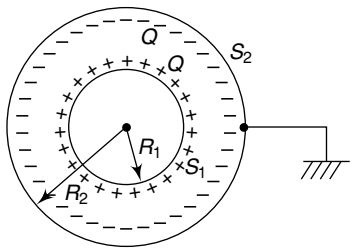


Fig. 1.19 *Charge distribution of concentric spheres (outer sphere earthed)*

$\therefore$ surface potential of S_1 is given by

$$V_{S_1} = \frac{+Q}{4\pi\varepsilon_o\,\varepsilon_r\,R_1},$$

while surface potential at the inner surface of S_2 is given by $V_{S_2} = \dfrac{-Q}{4\pi\varepsilon_o\,\varepsilon_r\,R_2}$.

$\therefore$ potential difference between S_1 and S_2 is

$$V = V_{S_1} - V_{S_2}$$

$$= \frac{Q}{4\pi\varepsilon_o\,\varepsilon_r}\left[\frac{1}{R_1} - \frac{1}{R_2}\right] = \frac{Q}{4\pi\varepsilon_o\,\varepsilon_r} \times \frac{R_2 - R_1}{R_1 R_2}$$

Then, $$C = \frac{Q}{V} = \frac{Q}{\frac{Q}{4\pi\varepsilon_o \varepsilon_r} \times \frac{R_2 - R_1}{R_2 R_1}}$$

$$= 4\pi\varepsilon_o\varepsilon_r \Big/ \left(\frac{R_2 - R_1}{R_2 R_1}\right) \text{ Farad} \tag{1.28}$$

Case-B

S_1(the inner sphere) earthed This time the outer sphere S_2 is given a charge of $(+Q)$ coulomb. This charge is uniformly distributed in the outer and inner surface of S_2; we assume $(+Q_2)$ charge remain at the outer surface while $(+Q_1)$ at the inner surface of S_2. The charge $(+Q_1)$ at the inner surface of S_2 would induce a charge of $(-Q_1)$ coulomb on the outer surface of S_1; $(+Q_1)$ charge induced in the inner surface of S_1 would pass to the earth as the inner surface of S_1 is earthed (Fig. 1.20).

The system is now composed of two subsystems of capacitors as described below:

(i) Capacitor formed by inner surface of S_2 and outer surface of S_1 and is similar to the case we described in case A

$\therefore$ Its capacitance,

$$C_1 = 4\pi\varepsilon_o\varepsilon_r\left[\frac{1}{R_2} - \frac{1}{R_1}\right]^{-1}$$

$$= 4\pi\varepsilon_o\varepsilon_r \Big/ \left(\frac{R_1 - R_2}{R_2 R_1}\right)$$

(ii) Capacitor formed by the outer surface of outer sphere S_2 and earth with air as dielectric.

$\therefore$ its capacitance, $C_2 = 4\pi\varepsilon_o\varepsilon_r R_2$

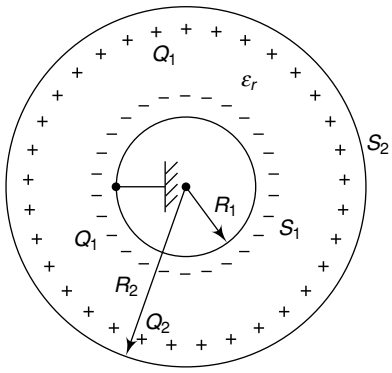


Fig. 1.20 ***Charge distribution of concentric spheres (inner sphere earthed)***

Since these two subsystems of capacitors are electrically parallel, we can find the total capacitance (C) as

$$C = C_1 + C_2$$

$$= 4\pi\varepsilon_o\varepsilon_r\left[\frac{R_1 - R_2}{R_1 + R_2}\right]^{-1} + 4p\varepsilon_o R_2$$

$$= 4\pi\varepsilon_o\left[\varepsilon_r \cdot \left(\frac{R_1 - R_2}{R_1 + R_2}\right)^{-1} + R_2\right] \text{ Farad} \tag{1.29}$$

1.25 CAPACITANCE OF A PARALLEL-PLATE CAPACITOR WHEN AN UNCHARGED METAL SLAB IS INTRODUCED BETWEEN PLATES

Let us consider each parallel plate has area of A m^2 and the distance between them is x m, the dielectric medium being air. If the charge retained by the capacitor is Q coulombs, the charge density d is given by

$$d = \frac{Q}{A} \text{ C/m}^2.$$

Also $$C = \frac{\varepsilon_o A}{x} \text{ Farad}$$

And, $$\varepsilon = \frac{\delta}{E}, (E) \text{ being the field intensity}$$

$$\therefore \quad E = \frac{\delta}{\varepsilon_o} = \frac{Q}{\varepsilon_o A}; \varepsilon_o \text{ being the permittivity of air medium}$$

When an uncharged metal plate of thickness a ($a < b$) is inserted between the plates, equal and opposite charges are induced on the slab (Fig. 1.21) and the net charge on the slab is equal to zero. Thus, the electric field inside the slab is zero. Then electric field would act in the distance $(x - a)$ m.

However, p.d. $(V) = E \times$ Distance

In our case, $V = E \times (x - a) = \frac{Q}{\varepsilon_o A} \times (x - a)$

Thus, the new capacitance C' is given by

$$C' = \frac{Q}{V} = \frac{\varepsilon_o A}{(x - a)} \text{ Farad} \qquad (1.30)$$

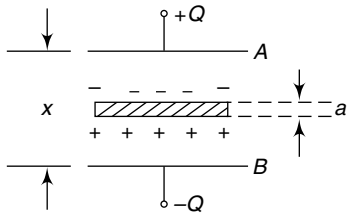


Fig. 1.21 *Parallel plate capacitor with uncharged metal plate in between*

1.7 Find the equivalent capacitance of the network shown in Fig. 1.19 connected across terminals a and b.

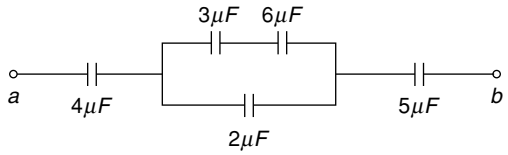


Fig. 1.22 *Capacitance configuration of Ex. 1.17*

Solution

The capacitors of 3 μF and 6 μF are connected in series. Hence, their equivalent capacitance

$$C_1 = \frac{1}{\frac{1}{3} + \frac{1}{6}} = \frac{6}{2 + 1} = 2 \text{ μF}$$

However, C_1 and 2 μF are in parallel, therefore their equivalent capacitance $C_2 = C_1 + 2 = 2 + 2 = 4$ μF.

Thus the network of capacitors reduces to that as shown in Fig. 1.22(a).

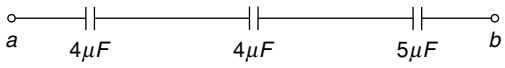


Fig. 1.22(a) *Reduced network of capacitors*

If C_{eq} be the equivalent capacitance of the new network configuration then,

$$\frac{1}{C_{eq}} = \frac{1}{4}+\frac{1}{4}+\frac{1}{5}=\frac{5+5+4}{20}=\frac{14}{20}\,\mu F$$

Hence, $C_{eq} = \frac{20}{14}\ \mu F = 1.43\ \mu F.$

1.8 Find the equivalent capacitance of the system of capacitances shown in Fig. 1.23.

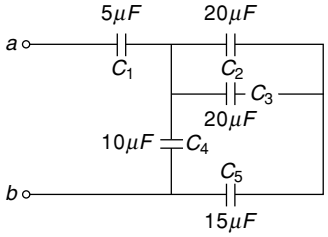


Fig. 1.23 *Capacitor configuration of Ex. 1.8*

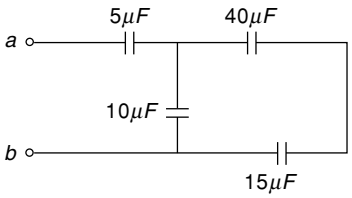


Fig. 1.23(a) *Reduced network*

Solution

The capacitors C_2 and C_3 (20 μF each) are conected in parallel. Hence, their equivalent capacitance is 20 + 20 = 40 μF. The network is shown in Fig. 1.23a.

40 μF and 15 mF are connected in series. Hence their equivalent capacitance is $\frac{40\times15}{40+15}$ i.e 10.91 μF.

Thus, 10 μF and 10.91 μF are connected in parallel. Their equivalent capacitance is 10 + 10.91 = 20.91 μF. The corresponding network is shown in Fig. 1.23(b).

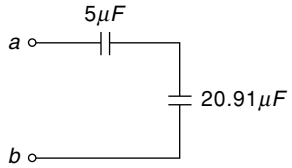


Fig. 1.23(b) *Equivalent network of capacitances of Ex. 1.8*

Hence, the equivalent capacitance of the system is

$$C_{eq} = \frac{5\times20.91}{5+20.91}\ \mu F, \text{ i.e } 4.035\ \mu F$$

1.9 A 50 mF capacitor is initially charged to accumulate 100 m coulomb of charge. One uncharged capacitor of 200 μF is connected across it in parallel. How much charge will be transferred?

Solution

Let V be the voltage across the capacitors connected in parallel. We know that $V = Q/C$, where Q is the charge in coulomb and C is the capacitance in Farad.

Hence, $Q_1/C_1 = Q_2/C_2$, where Q_1 is the charge of capacitor C_1 and Q_2 is the charge of capacitor C_2. Voltage across the parallel combination of C_1 and C_2 remain the same.

Therefore, $$\frac{Q_1}{Q_2} = \frac{C_1}{C_2}=\frac{50}{200}=\frac{1}{4} \quad \text{(i)}$$

Again, Total charge = Initial charge accumulated by C only = 100 μ Coulumb.

Hence, $Q_1 + Q_2 = 100$ (ii)

Solving equations (i) and (ii)

$$Q_1 + 4Q_1 = 100\ \mu C$$

or $$Q_1 = 20\ \mu C \text{ and } Q_2 = 80\ \mu C$$

Therefore 80 μC charge will be transferred from C_1 to C_2.

1.10 Find the equivalent capacitance across terminals *x*-*y* in Fig. 1.24. Also find the time to charge the capacitances by a direct current of 10A.

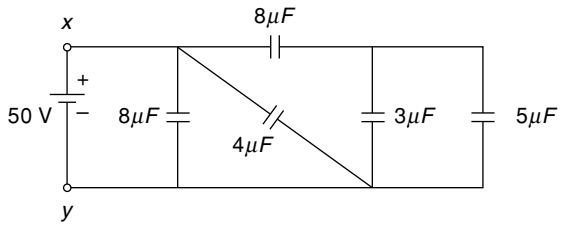


Fig. 1.24 *Network of capacitances of Ex. 1.10*

Solution

Equivalent capacitance of 3 μF and 5 μF is (3 + 5)μF, i.e 8 μF

The equivalent capacitance of two 8 μF capacitors in series is 8 × 8/8 + 8 μF, i.e 4 μF. The equivalent capacitance of two 4 μF capacitors in parallel is (4 + 4) μF, i.e 8 μF. Here we find two 8 μF capacitors are in parallel with the voltage source.

Hence the equivalent capacitance of the circuit across terminals (*x* – *y*) is (8 + 8) μF, i.e 16 μF.

Now, charge = $50 \times 16 \times 10^{-6}$ coulomb

$= 800 \times 10^{-6}$ coulomb

If *t* be the charging time and *i* be the current then

$$i \times t = 800 \times 10^{-6} \quad [\because\ Q = i \times t]$$

or $$t = \frac{800 \times 10^{-6}}{10} \text{ s} = 80\mu \text{ second.}$$

1.11 A voltage of 90V dc is applied across two capacitors in series having capacitances of 50 μF and 25 μF. Find the voltage drop across each capacitor. What is the charge in coulomb in each capacitor?

Solution

Since the capacitors are in series, same charge *Q* is flowing across each of them.

Hence $Q = C_1V_1 = C_2V_2$, where C_1 and V_1 are the capacitance and voltage across one capacitor and C_2 and V_2 are the capacitance and voltage across the other.

Therefore, $50V_1 = 25V_2$ or, $V_2 = 2V_1$ (i)

Again $V_1 + V_2 = 90$ (ii)

Solving equations (i) and (ii), $V_1 + 2V_1 = 90$

or $V_1 = 30$ and $V_2 = 60$.

Hence voltage drop across the capacitors are 30 V and 60 V.

Since both the capacitors are in series

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \quad \text{or} \quad C = \frac{C_1 C_2}{C_1 + C_2} = \frac{50 \times 10^{-6} \times 25 \times 10^{-6}}{50 \times 10^{-6} + 25 \times 10^{-6}}$$

$$= 16.67 \ \mu\text{F}.$$

The charge supplied by the dc source is

$$Q = CV = 16.67 \times 10^{-6} \times 90 \ ; \ 1500 \ \mu\text{C}.$$

In series combination, each capacitor has equal charge and this charge equals the charge supplied by the dc source.

$\therefore$ each capacitor would retain a 1500 μC charge in fully charged condition.

1.12 Calculate the capacitance of a parallel plate capacitor having 20 cm × 20 cm square plates separated by a distance of 1.0 mm. Assume the dielectric medium to be air with permittivity of 8.85×10^{-12} F/m.

Solution

$$C = \frac{\varepsilon_o A}{x}, \text{ for parallel plate capacitor}$$

$$= \frac{8.85 \times 10^{-12} \times 400 \times 10^{-4}}{1 \times 10^{-3}}$$

$$= 3.54 \times 10^{-10} \text{ F} = 354 \text{ pF}.$$

1.13 In Fig. 1.25, a voltage source is connected across a combination of capacitances at terminals $(x - y)$. Find the current supplied by the battery to charge this combination if the time taken to charge is 50 m sec.

[$C_1 = C_2 = C_3 = 10$ μF

$V = 100$ V]

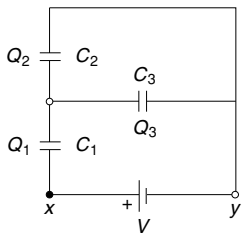


Fig. 1.25 ***Capacitance configuration (Ex. 1.13)***

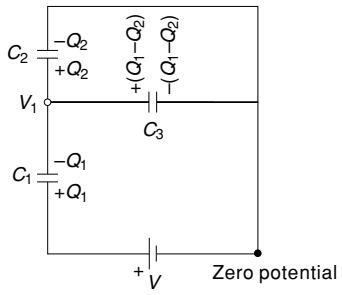


Fig. 1.25(a) ***Voltage-charge distribution***

Solution

Let us redraw the diagram with voltage and charge distribution (Fig. 1.25a)

Here

$$Q_1 = C_1(V - V_1) \quad \text{(i)}$$

$$Q_2 = C_2 V_1 \quad \text{(ii)}$$

$$(Q_1 - Q_2) = C_3 V_1 \quad \text{(iii)}$$

From equations (ii) and (iii)

$$Q_1 = (C_2 + C_3)V_1$$

i.e.

$$V_1 = \frac{Q_1}{C_2 + C_3} \quad \text{(iv)}$$

From (i), $\frac{Q_1}{C_1} = V - V_1$ (v)

Adding (iv) and (v),

$$V = \frac{Q_1}{C_2 + C_3} + \frac{Q_1}{C_1}$$

or $$V = \frac{(C_1 + C_2 + C_3)Q_1}{C_1(C_2 + C_3)}$$

$$\therefore \quad C \text{ (equivalent capacitance)} = \frac{Q_1}{V} = \frac{C_1(C_2 + C_3)}{C_1 + C_2 + C_3}$$

$$= \frac{10 \times 10^{-6}(10 + 10)10^{-6}}{(10 + 10 + 10)10^{-6}}$$

$$= 6.67 \times 10^{-6}\ \mu\text{F}$$

Hence, Q = charge drawn from source

$= CV = 6.67 \times 10^{-6} \times 100 = 6.67 \times 10^{-4}$ coulombs

Also, Charge = Current × Time

$$\therefore \quad \text{Current } (I) = \frac{\text{Charge}}{\text{Time}} = \frac{6.67 \times 10^{-4}}{50 \times 10^{-3}} = 13.34 \text{ mA.}$$

1.14 What is the capacitance across *AD* in Fig. 1.26?

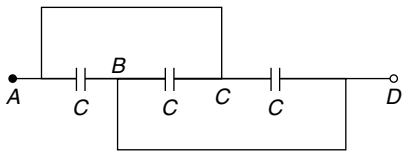


Fig. 1.26 ***Capacitance configuration (Ex. 1.14)***

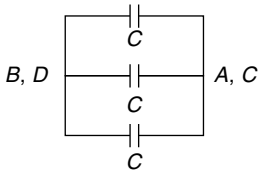


Fig. 1.26(a) ***Reduced network (Ex. 1.14)***

Solution

Observation reveals that *B* and *D* are electrically same points while *A* and *C* are electrically same points. The given figure then reduces as shown in Fig. 1.26a. Thus the equivalent capacitance of this parallel combination becomes 3C.

1.15 If capacitance between adjacent parallel plates be *C*, find the total capacitance in the system shown in Fig. 1.27.

Solution

Let us redraw the circuit in a conventional form (Fig. 1.27(a)).

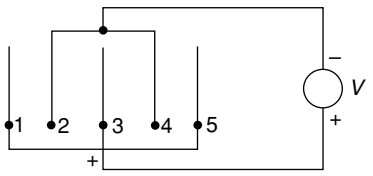


Fig. 1.27 ***Circuit of Ex. 1.15***

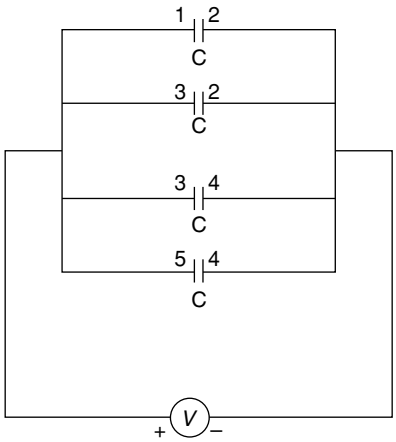


Fig. 1.27(a) ***Equivalent circuit of Fig. 1.27***

Hence we find that the plate pairs are in parallel and hence the net capacitance is 4C.

1.16 Show that if a dielectric of thickness t and with the same area as the plates of parallel plate capacitor is introduced, the capacitor would then have the capacitance

$$C = \frac{\varepsilon_o A}{\left[d - t + \frac{t}{\varepsilon_r}\right]}$$

Solution

Let us suppose that we have a parallel plate capacitor with air as the dielectric medium and capacitance C. Obviously, $C = \varepsilon_o A/d$, (d) being the separation between the plates.

Next we imagine that the capacitor is filled up by another dielectric of dielectric strength ε_r replacing the air medium (Fig. 1.28). Let C' be the new capacitance.

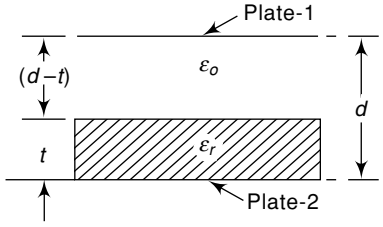


Fig. 1.28 ***Parallel-plate capacitor with two dielectric media***

$$C' = \frac{\varepsilon_o \varepsilon_r A}{d} = \frac{\varepsilon_o A}{d/\varepsilon_r}$$

Now, if the two capacitances are supposed to be equal then we find that d/ε_r replaces d in the original expression when air was the dielectric medium.

Thus d distance between the plates with air as the dielectric medium is equivalent to distance d/ε_r in air medium.

Therefore, if a dielectric of thickness t is introduced then it being equivalent to t/ε_r of air medium, the effective air distance between the plate is $(d - t + t/\varepsilon_r)$.

$$\therefore \qquad C = \frac{\varepsilon_o A}{d - t + (t/\varepsilon_r)}.$$

[Also, the problem may be solved in another way:
C_1 is the capacitance with ε_o.

$$\therefore \qquad C_1 = \frac{\varepsilon_o A}{d - t}$$

C_2 is the capacitance with ε_r.

$$\therefore \qquad C_2 = \frac{\varepsilon_r \varepsilon_o A}{t}.$$

Since C_1 and C_2 are in series

$$C = \frac{C_1 C_2}{C_1 + C_2} = \frac{\varepsilon_o A/d - t \times \varepsilon_r \varepsilon_o A/t}{\varepsilon_o A/d - t + \varepsilon_r \varepsilon_o A/t}$$

$$= \frac{\varepsilon_o^2 \varepsilon_r A^2}{\varepsilon_o A(t + d\varepsilon_r - t\varepsilon_r)} = \frac{\varepsilon_o A}{\left(d - t + \frac{t}{\varepsilon_r}\right)}.$$

We have obtained same result using the previous method.]

1.17 The space between two plates of a parallel plate capacitor C is filled up with three different dielectric slabs of identical size as shown in Fig. 1.29. If the dielectric constants of the three slabs be ε_1, ε_2, and ε_3, find the new value of the capacitance. The plate cross-sectional area is A and the separation is d.

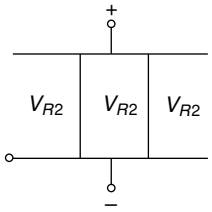


Fig. 1.29 *Capacitor of Ex. 1.17*

Solution

Let us consider each 1/3 assembly as separate capacitors C_1, C_2 and C_3.

$$C_1 = \frac{\varepsilon_1 (A/3)}{d}; \quad C_2 = \frac{\varepsilon_2 (A/3)}{d}; \quad C_3 = \frac{\varepsilon_3 (A/3)}{d}$$

As the three capacitors are in parallel (the +ve plates are joined together for all capacitors as well as the negative plates are also connected together),

$$C_{eq} = C_1 + C_2 + C_3 = \frac{A}{3d} (\varepsilon_1 + \varepsilon_2 + \varepsilon_3).$$

1.26 EXPRESSION OF INSTANTANEOUS CURRENT AND VOLTAGE IN A CAPACITOR

The instantaneous current in a capacitor is given by

$$i = \frac{dq}{dt} = \frac{d}{dt}(Cv) = C\frac{dv}{dt}. \tag{1.31a}$$

Thus, the voltage across the capacitor being constant, current through it is zero. This means, on application of dc voltage across the capacitor and with no initial charge the capacitor first acts as short circuit but as soon as it accumulates full charge, it behaves like an open circuit.

Also, from above

$$dv = \frac{1}{C} \times i \times dt$$

or $$\int_{v_o}^{v_f} dv = \frac{1}{C}\int_{o}^{t} i \cdot dt \quad [v_o = \text{initial voltage in the capacitor, if any and } v_f = \text{the final voltage in the capacitor}]$$

or $$v_f - v_o = \frac{1}{C}\int_{o}^{t} i \cdot dt$$

$$\therefore \quad v_f = \frac{1}{C}\int_{o}^{t} i \cdot dt + v_o \tag{1.31b}$$

[Normally, $v_o = 0$ and hence $v_f = v_C = \frac{1}{C}\int_{o}^{t} i\,dt$]

1.27 CHARGING AND DISCHARGING OF CAPACITANCE

(a) Charging

Let a dc voltage V be applied (at $t = 0$) by closing a switch S in a series RC circuit (Fig. 1.30). The capacitor being charged, at $t > 0$, the charging current becomes i. We can write

$$Ri + \frac{1}{C}\int_{o}^{t} i\,dt = V \tag{1.32}$$

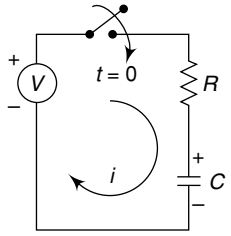


Fig. 1.30 ***Charging and discharging of capacitor***

[$\because$ drop across the resistor = Ri and the drop across (C) is obtained from the instantaneous current (i) given by

$$i = C\frac{dv}{dt}$$

i.e. $$v = \frac{1}{C}\int i\,dt\ ]$$

It may be noted here that as the charging gets started, upper plate of (C) will start accumulating +ve charges while the lower plate accumulates –ve charge. Differentiation of equation 1.32 results

$$R\frac{di}{dt} + \frac{i}{C} = 0 \tag{1.32a}$$

or $$\frac{di}{i} = -\frac{1}{RC}dt$$

Integrating both sides

$$\log_e i = -\frac{t}{RC} + K_1, \text{ where } K_1 \text{ is a constant}$$

or $$\log_e \frac{i}{K_2} = \log_e e^{-t/RC} \quad (\text{where } K_1 = \log_e K_2)$$

or $$i = K_2 e^{-t/RC} \tag{1.32b}$$

With application of voltage and assuming no initial charge across the capacitor, the capacitor will not produce any voltage across it but acts as a short circuit causing the circuit current to be (V/R).

i.e. at $$t = 0^+, i(0^+) = \frac{V}{R}$$

Hence, from equation (1.32) at $t = 0^+$

$$\frac{V}{R} = K$$

Finally, we then obtain, $$i = \frac{V}{R} e^{-t/RC} \tag{1.33}$$

It may be observed that the charging current is a decaying function, the plot being shown in Fig. 1.30(a). As the capacitor is getting charged, the charging current dies out.

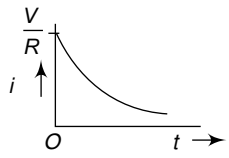


Fig. 1.30(a) *Profile of current in RC charging circuit*

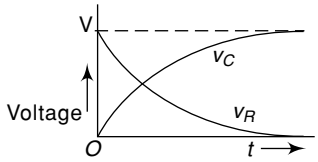


Fig. 1.30(b) *Profiles of v_R and v_C in RC charging circuit*

The corresponding voltage drops across the resistor and capacitor can be obtained as follows:

$$v_R = iR = V e^{-t/RC} \tag{1.34}$$

and $$v_C = \frac{1}{C}\int i\, dt = \frac{1}{C}\int_o^t \frac{V}{R} e^{-\frac{t}{RC}} dt$$

$$= V(1 - e^{-t/RC}) \tag{1.35}$$

Observing equations (1.34) and (1.35), it reveals that (v_R) is a decaying function while (v_C) is an exponentially rising function [profiles of (v_R) and (v_C) are shown in Fig. 1.30(b)]. The steady state voltage across capacitor is V volts.

The time constant is obtained by substituting $t = RC$ which gives $v_C = V(1 - 0.368) = 0.632V$, i.e the item by which the capacitor attains 63.2% of steady state voltage.

The instantaneous powers are given by

$$p_R = iv_R = \frac{V^2}{R} e^{-2t/RC}$$

and

$$p_C = iv_C = \frac{V^2}{R}\left(e^{-t/RC} - e^{-2t/RC}\right)$$

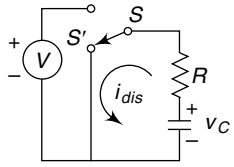


Fig. 1.31 *Discharging in RC series circuit*

(b) Discharging

Let us now study the discharging case when the switch S is thrown to a contact S' such that the R-C circuit is shorted and the voltage source is withdrawn (Fig. 1.31). Here we can write

$$Ri + \frac{1}{C}\int i\,dt = 0 \tag{1.36}$$

Differentiating equation (1.36), we get

$$R\frac{di}{dt} + \frac{i}{C} = 0 \tag{1.37}$$

Solution of equation (1.37) is

$$i = K'e^{-t/RC} \tag{1.38}$$

where K' is a constant.

However at $t = 0^+$, the voltage across the capacitor will start discharging current through the resistor in opposite direction to the original current (shown by i_{dis} in Fig. 1.31). Hence the direction of i during discharge is negative and its magnitude is given by (V/R).

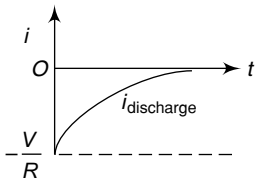


Fig. 1.31(a) *Current decay transient in RC discharging circuit*

Hence from equation (1.38) we get

$$-\frac{V}{R} = K'(\text{at } t = 0^+)$$

The complete solution is then

$$i = -\frac{V}{R}e^{-t/RC} \tag{1.39}$$

The decay transient is plotted in Fig. 1.31(a).
The corresponding transient voltages are given by

$$\left.\begin{aligned} &v_R\,(\text{voltage drop across } R) = iR = -Ve^{-t/RC} \\ \text{and}\quad &v_C\,(\text{voltage drop across } C) = \frac{1}{C}\int i\,dt = Ve^{-t/RC} \end{aligned}\right\} \tag{1.40}$$

Obviously, $v_R + v_C = 0$

Figure 1.31(b) represents the profiles of v_R and v_C with t. In the discharging circuit, the time constant is given by the product of R and C such that $v_C = Ve^{-1}$ $= 0.369V$; $0.37V$, i.e. the time by which the capacitor discharges to 37% of its initial voltage.

The instantaneous powers are given by

$$p_R = v_R\, i = \frac{V^2}{R} e^{-2t/RC} \quad \left.\right\} \qquad (1.41)$$

and $$p_C = v_C\, i = -\frac{V^2}{R} e^{-2t/RC} \quad \left.\right\}$$

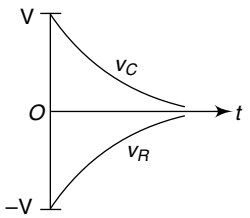


Fig. 1.31(b) *v_R and v_C in RC discharging circuit*

[The charge stored in the capacitor during charging is given by $q = Cv_C = CV\left(1 - e^{-t/RC}\right)$ or $q = Q\left(1 - e^{-t/RC}\right)$ while that during discharging is given by $q = Cv_C = CVe^{-t/RC}$ coulombs or, $q = Qe^{-t/RC}$].

1.18 Calculate the time taken by the capacitor of 1 mF and in series with a 1 μΩ. resistance to be charged upto 80% of the final value.

Solution

The time constant T is given by

$$T = RC = 1 \times 10^6 \times 10^{-6} = 1 \text{ sec.}$$

The charging of capacitor is expressed by the following equation

$$q = Q_o\left(1 - e^{-t/RC}\right).$$

Here $q = 0.8\ Q_o$; $R = 1$ sec.

$$\therefore \qquad 0.8 = 1 - e^{-t} \quad \text{or, } e^{-t} = 0.2$$

Hence $t = 1.61$ sec.

1.19 A dc constant voltage source feeds a resistance of 2000 kW in series with a 5 μF capacitor. Find the time taken for the capacitor when the charge retained will be decayed to 50% of the initial value, the voltage source being short circuited.

Solution

Time constant $T = RC = 2 \times 10^6 \times 5 \times 10^{-6} = 10$ sec.

The decaying condition is represented by the following expression

$$q = Q_o\, e^{-t/T}$$

However, $q = 0.5\ Q_o$,

$$\therefore \qquad 0.5\ Q_o = Q_o\, e^{-t/T}$$

or $$0.5 = e^{-t/T} = e^{-t/T}$$

or $$-t/10 = \log_e (0.5)$$

or $$t = 6.938$$

1.20 In Fig. 1.32 the switch K is closed. Find the time when the current from the battery reaches to 500 mA.

[R_x = 50 W; R_y = 70W; C = 100 μF]

Solution

Let current through R_x be I_x and through C be I_y after switch K is closed.

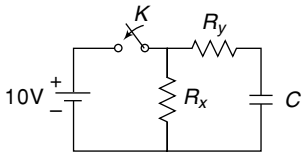
$$I_x = \frac{10}{50} = 0.2A = 200 \text{ mA}$$

However $I = I_x + I_y$

[I being the current from the supply]

or $500 = 200 + I_y$ [$\because$ supply current is 500 mA]

$I_y = 300$ mA



[$R_x = 50\ \Omega$; $R_y = 70\ \Omega$; $C = 100\ \mu$F]

Fig. 1.32 ***Circuit of Ex. 1.20***

But $I_y = \frac{V}{R_y} e^{-t/T}$ [$T = RC = 70 \times 100 \times 10^{-6} = 0.007$ sec]

or $0.3 = \frac{10}{70} e^{-t/0.007}$

or $-\frac{t}{0.007} = \log_e (2.1)$

$t = 5.2$ m-sec.

This is the time required when the d.c. source current flow will be 500 mA.

1.21 A 10 µF capacitor is initially charged to 100 volts dc. It is then discharged through a resistance of (R) ohms for 20 seconds when the p.d. across the capacitor is 50 V. Calculate the value of (R).

Solution

In the discharging condition of the capacitor,

$$q = Q_0 e^{-t/RC} \quad \text{or} \quad v = V_0 e^{-t/RL}$$

As per the question capacitor p.d. gets discharged to 50 V from the initial p.d. of 100 V.

$\therefore \quad v = 0.5V_0$

Hence we obtain, $0.5 = e^{-t/R \times 10 \times 10^{-6}}$

or $\log_e 0.5 = -\frac{t}{R \times 10^{-5}} = -\frac{20}{R \times 10^{-5}}$

or $-0.7 = -\frac{20}{R \times 10^{-5}}$

$\therefore \quad R = 28.86 \times 10^5$ W $= 2.86$ MΩ.

1.22 A resistance R and 5µF capacitor are connected in series across a 100 V d.c. supply. Calculate the value of R such that the voltage across the capacitor becomes 50 V in 5 sec after the circuit is switched on.

Solution

In case of charging

$$q = Q_0\left(1 - e^{-t/T}\right) \quad [T = RC = (5 \times 10^{-6}\ R) \text{ sec.}]$$

or $v = V_0\left(1 - e^{-t/T}\right)$

As per the question, the p.d. across the capacitor is 50 V within 5 sec.

$\therefore \quad v = 0.5\ V_0$ [V_0 = final p.d. in steady state = 100 V]

and $t = 5$ sec.

$\therefore \quad 0.5 = 1 - e^{(-5)/(5\times10^{-6})R}$ or, $-0.5 = -e^{-10^6/R}$

$R = 1.44\ \text{M}\Omega$

1.23 The 10 μF capacitor in *RC* circuit of Fig. 1.33 has initial charge of 100 μ*C* with polarities as shown in Fig. 1.51. At $t = 0$, the switch being closed, a dc voltage of 100 V is applied. Find the expression for the current.

Solution

In the charging case

$$100 = 500 \times i + \frac{1}{10\times10^{-6}}\int i\,dt$$

or $$0 = 500\frac{di}{dt} + \frac{i}{C}$$

or $$\frac{di}{i} = -\frac{1}{500\,C}dt$$

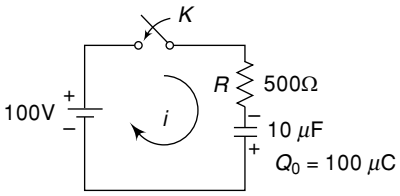


Fig. 1.33 *Circuit of Ex. 1.23*

or $i = Ke^{-200\,t}$, where K is constant.

However, due to initial charge of 100 μC in the polarity shown, the equivalent voltage becomes

$$V_o = \frac{q_o}{C} = \frac{100\times10^{-6}}{10\times10^{-6}} = 10\ \text{V}$$

This 10 V also sends current in the direction of i.
Hence at $t = 0$

$$i_0 = (V + V_o)/R = \frac{110}{500} = 0.22\ \text{A}$$

Thus at $t = 0$, $0.22 = Ke^{-200\times0}$

or $K = 0.22$

Thus, the expression for current becomes

$$i = 0.22\ e^{-200t}\ \text{A}.$$

1.28 ENERGY STORED IN A CAPACITOR

A capacitor never dissipates energy and only stores it when the capacitor is assumed to be ideal. It can store finite amount of energy, even if the steady state current through it is zero. A capacitor discharges its energy when connected in a circuit having resistances.

The power absorbed by the capacitor is given by

$$p = v \times i = v \times C \times \frac{dv}{dt}$$

$\therefore$ energy stored by the capacitor is

$$W = \int_o^t p\,dt = \int_o^v v \cdot C \cdot \frac{dv}{dt}\cdot dt$$

$$= \frac{1}{2}Cv^2 \qquad (1.42)$$

The energy stored by the capacitor is then (½) Cv^2 Joules.

$$\left[\text{Also,} \qquad W = \frac{1}{2}Cv^2 = \frac{1}{2}C \cdot \frac{Q^2}{C^2} = \frac{Q^2}{2C}\right] \tag{1.43}$$

W is always expressed in joules.

1.24 A parallel plate capacitor of plate area A and plate separation d is charged to a potential difference V and then the battery is disconnected. A slab of dielectric constant e is then inserted between the plates so as to fill the space between the plates. If Q, E and W denote respectively, the magnitude of charge on each plate, the electric field between the plates (after the slab is inserted), and the work done on the system, show that in the process of inserting the slab the work done is given by

$$W = \frac{\varepsilon_o A V^2}{2d}\left(1 - \frac{1}{\varepsilon}\right)$$

Solution

Let us assume that the capacitor retain charge Q when charged to voltage V at the initial condition. This charge will remain same even when the slab is inserted; however, the electric field intensity will reduce by a factor e.

$$\therefore \qquad Q = CV = \varepsilon_o \frac{AV}{d}\,;\; E \text{ (field intensity)} = \frac{V}{\varepsilon d}$$

Energy of the system before dielectric e is inserted,

$$W_1 = \frac{1}{2}\frac{Q^2}{C} = \frac{\varepsilon_o^2 A^2 V^2}{2d^2} \times \frac{d}{\varepsilon_o A} \qquad \left[\because \text{from above } C = \frac{\varepsilon_o A}{d}\right]$$

$$= \frac{\varepsilon_o A V^2}{2d}$$

After insertion of dielectric,

$$W_2 = \frac{1}{2}\frac{Q^2}{C_1}, \quad \text{where } C_1 = \varepsilon_o \frac{\varepsilon A}{d}$$

$$= \frac{1}{2}\frac{\varepsilon_o^2 A^2 V^2}{2d^2} \times \frac{d}{\varepsilon_o \varepsilon A} = \frac{\varepsilon_o A V^2}{2\varepsilon d}$$

$$\therefore \qquad W_1 - W_2 = \frac{\varepsilon_o A V^2}{2d}\left(1 - \frac{1}{\varepsilon}\right).$$

1.25 A capacitor of capacitance C is fully charged by a 220 V supply. It is then discharged through a small resistance embedded in a thermally insulated block of specific heat 2.5×10^2 J kg^{-1} K^{-1} and of 0.2 kg mass. If the temperature of the block rises by 1 K, find the value of C.

Solution

Energy stored in the capacitor is

$$W = \frac{1}{2}CV^2 = \frac{1}{2} \times C \times (220)^2 \text{ Joule}$$

Energy supplied as heat in the block is obtained as

$$H = m\ s\ t$$

where H = heat,

m = mass,

s = specific heat, and

t = temperature rise.

Here $H = 0.2 \times 2.5 \times 10^2 \times 1$ Joule = 50 Joule

In a thermally insulated system,

$$W = H$$

$$\therefore \quad \frac{1}{2} \times C \times (220)^2 = 50$$

$$\therefore \quad C = \frac{50}{(220)^2} \times 2 = 2066\ \mu\text{F}.$$

1.29 CAPACITANCE OF TWO CO-AXIAL CYLINDERS

Figure 1.34 represents two co-axial cylinders of radii R_1 and R_2 ($R_2 > R_1$). Let $+Q$ be the charge per metre length at inside surface of the outer cylinder (assuming the outer surface of the outer cylinder earthed); by electrostatic induction, $-Q$ charge per metre is induced at the outer surface of the inner cylinder.

Let us assume another imaginary co-axial cylinder having radius x and length one metre between the two given cylinders. Let ε_r be the permittivity of medium inbetween the two cylinders of radii R_1 and R_2.

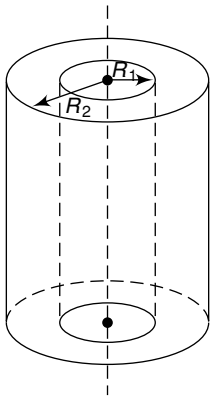


Fig. 1.34 *Co-axial cylinders*

Electric flux density (d) on the surface of the imaginary cylinder is then given by

$$d = \frac{\psi}{A} = \frac{Q}{A} = \frac{Q}{2\pi x \times 1}\ \text{C/m}^2$$

[$\because$ Curved surface area of a cylinder is $2\pi rl$ and here $r = x$; $l = 1$ m; we express Q in columb while x and R in metre]

$\therefore$ Electric field intensity is obtained as

$$E = \frac{\delta}{\varepsilon_o \varepsilon_r}\ \text{V/m} = \frac{Q}{2\pi\varepsilon_o \varepsilon_r x}\ \text{V/m}$$

Since $dV = E\ dx$, we can write,

$$\int_O^V dV = \int_{R_1}^{R_2} E\ dx$$

or

$$V = \int_{R_1}^{R_2} \frac{Q}{2\pi\varepsilon_o \varepsilon_r x} \cdot dx = \frac{Q}{2\pi\varepsilon_o \varepsilon_r} \int_{R_1}^{R_2} \frac{1}{x}\ dx$$

$$= \frac{Q}{2\pi\varepsilon_o\varepsilon_r}\left|\ln x\right|_{R_1}^{R_2}$$

$$= \frac{Q}{2\pi\varepsilon_o\varepsilon_r}\ln(Q_2/Q_1)$$

Since Capacitance, $C = Q/V$, we have

$$C = \frac{Q}{(Q/2\pi\varepsilon_o\varepsilon_r)\ln(R_2/R_1)}$$

$$= \frac{2\pi\varepsilon_o\varepsilon_r}{\ln(R_2/R_1)}\text{ F/m}$$

$\left[\text{for length } L \text{ metre, the capacitance is given by } C = \dfrac{2\pi\varepsilon_o\varepsilon_r}{\ln(R_2/R_1)}\text{ F}\right]$

ADDITIONAL EXAMPLES

1.26 Three concentric thin spherical shells A, B, C of radii r_1, r_2, r_3 are kept as shown in Fig. (1.35i). Shells A and C are given charges q and $-q$ respectively, shell B is earthed. Find charges appearing on the surfaces of B and C.

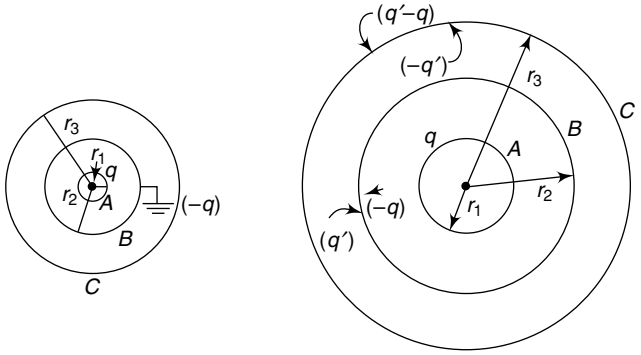


Fig. 1.35 ***Three concentric spherical shells (Ex. 1.26)***

Solution

Inner surface of B (by Gauss's law) must have charge $-q$. Let the outer surface of B have charge q'. The Inner surface of C must have change $-q'$ from Gauss's law. As net charge on C must be $-q$, its outer surface should have a charge $(q' - q)$. The charge distribution is shown in Fig. (1.35ii).

Potential at B due to charge q on $A = \dfrac{q}{4\pi\varepsilon_o r_2}$

due to charge $-q$ on the inner surface of $B = \dfrac{-q}{4\pi\varepsilon_o r_2}$

due to charge q' on outer surface of $B = \dfrac{q'}{4\pi\varepsilon_o r_2}$

due to charge $-q'$, on inner surface of $C = \dfrac{-q'}{4\pi\varepsilon_o r_3}$

and due to charge $(q' - q)$ on outer surface of $C = \dfrac{q'-q}{4\pi\varepsilon_o r_3}$.

Net potential on B is obtained adding all the potentials at B. We then obtain

$$V_B = \frac{q'}{4\pi\varepsilon_o r_2} - \frac{q}{4\pi\varepsilon_o r_3}.$$

But $V_B = 0$ as B is earthed.

$$\therefore \qquad q' = \frac{r_2}{r_3} q.$$

The final charge distribution is shown in Fig. 1.35a.

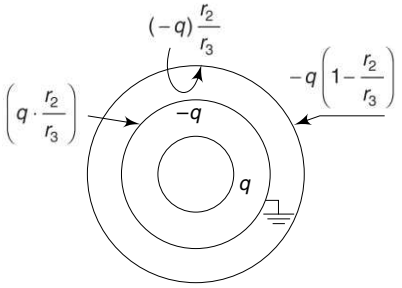


Fig. 1.35a *Final charge distribution*

1.27 There are two thin wire rings, each of radius R, whose axes coincide. The charges of the rings are $(+Q)$ and $(-Q)$. Find the potential difference between the centres of the rings separated by a distance a.

Solution

The arrangement of the rings are shown in Fig. 1.36. The potential at point 1 is given by V_1 = potential at 1 due to ring 1 + potential at 1 due to the ring 2;

i.e., $$V_1 = \frac{Q}{4\pi\varepsilon_o R} + \frac{-Q}{4\pi\varepsilon_o (R^2 + a^2)^{1/2}}.$$

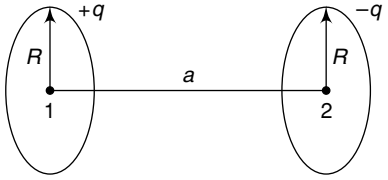


Fig. 1.36 *Arrangement of rings in Ex. 1.27*

Similarly, the potential at point 2 is

$$V_2 = \frac{-Q}{4\pi\varepsilon_o R} + \frac{Q}{4\pi\varepsilon_o (R^2 + a^2)^{1/2}}$$

$$\therefore \qquad V = V_1 - V_2 = \mathrm{D}V = 2\left(\frac{Q}{4\pi\varepsilon_o R} + \frac{-Q}{4\pi\varepsilon_o (R^2 + a^2)^{1/2}}\right)$$

$$= \frac{Q}{2\pi\varepsilon_o R}\left[1 - \frac{1}{\sqrt{1 + (a/R)^2}}\right]$$

1.28 Three point charges q, $2q$ and $8q$ are to be placed on a 9 cm long straight line. Find the position where the charges should be placed such that the potential energy of this system is minimum. In this situation, what is the electric field at the position of the charge q due to the other two charges?

Solution

Let charges q, $2q$ and $8q$ be placed along a straight line of length 9 cm or 0.09 m with distance between the charges q and $2q$ being x metres. Then distance between $2q$ and $8q$ would be $(0.09 - x)$m. Thus the potential energy u of the system is given by

$$u = \frac{1}{4\pi\varepsilon_o}\left[\frac{q\cdot 2q}{x} + \frac{2q\cdot 8q}{(0.09-x)} + \frac{q\cdot 8q}{0.09}\right] = 9 \times 10^9 \times 2q^2\left[\frac{1}{x} + \frac{8}{0.09-x} + \frac{4}{0.09}\right]$$

u to be minimum,

$$\frac{du}{dx} = 0, \text{ i.e } 0 = -\frac{1}{x^2} + \frac{8}{(0.09-x)^2}.$$

This, gives $$x^2 = \frac{(0.09-x)^2}{8}$$

or $$2\sqrt{2}\,x = \pm(0.09 - x)$$

or $$2\sqrt{2}\,x \pm x = \pm 0.09$$

$$\therefore \quad x(\text{minimum}) = \frac{0.09}{2\sqrt{2}+1} = 0.0235 \text{ m.}$$

Again, with E_1 and E_2 as the electric fields at the position of charge q due to charge $2q$ and $8q$ respectively,

$$E_1 = \frac{1}{4\pi\varepsilon_o}\times\frac{2q}{x^2} \quad \text{and} \quad E_2 = \frac{1}{4\pi\varepsilon_o}\cdot\frac{8q}{(0.09)^2}$$

The electric field at q due to the other two charges is $(E_1 + E_2)$

$$\therefore \quad E_1 + E_2 = \frac{1}{4\pi\varepsilon_o}\left[\frac{2q}{(0.0235)^2} + \frac{8q}{(0.09)^2}\right]$$

$$= 9 \times 10^9 \times 2q\left[\frac{1}{(0.0235)^2} + \frac{4}{(0.09)^2}\right]$$

$$= 4.15 \times 10^{13}\, q \text{ N/C.}$$

1.29 Find the value of the capacitance C if the equivalent capacitance between points X and Y is to be 1 μF. All capacitances are in μF in Fig. 1.37.

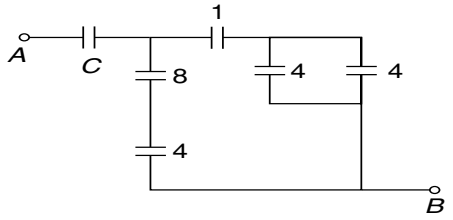


Fig. 1.37 ***Capacitance configuration (Ex. 1.29)***

Solution

The series combination of capacitances 6 and 12 is $6 \times 12/\ 6 + 12$ i.e. 4 μF. The parallel combination of 2 and 2 is (2 + 2), i.e. 4 μF. Figure 1.37 is reduced to Fig. 1.37a.
The parallel combination of 4 and 4 is 8 μF in Fig. 1.38a, while the series combination of 8 and 4 is $8 \times 4/8 + 4$, i.e. 8/3 μF. We can reduce Fig. 1.37a further to Fig. 1.37b.

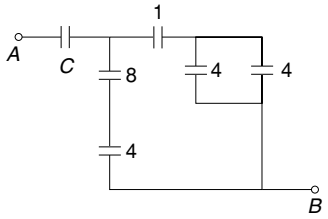


Fig. 1.37a ***Partly reduced network of Fig. 1.37***

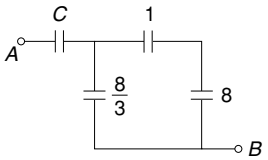


Fig. 1.37b ***Further network reduction of Fig. 1.37a***

The series combination of 1 and 8 yield $1 \times 8/1 + 8$, i.e. 8/9 μF and this 8/9 μF is in parallel to 8/3 μF in Fig. 1.37b. The equivalent capacitance is then (8/9 + 8/3) i.e., 32/9 μF. Thus finally we reduce the network of Fig. 1.37b to Fig. 1.37c, where C is in series with 32/9 μF. By the given question,

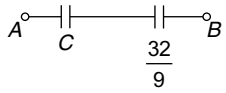


Fig. 1.37c ***Finally reduced network of Fig. 1.37b***

$$1 = \frac{1}{C} + \frac{9}{32}$$

$$\therefore \quad C = \frac{32}{23} = 1.39 \text{ μF}.$$

1.30 In Fig. 1.38, C = 9F; C_1 = 6F. Find the equivalent capacitance across (a – b).

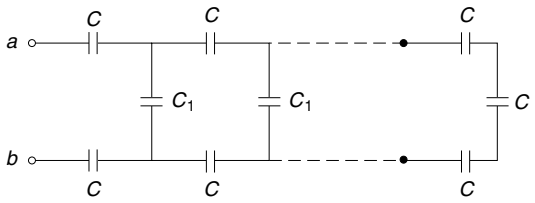


Fig. 1.38 ***Capacitance configuration (Ex. 1.30)***

Solution

We may note that the last three capacitors are all C, i.e. all are 9F each. Since they are in series, the net capacitance of these three capacitors is 3F. This 3F equivalent capacitor is in parallel to C_1 of the previous loop (Fig. 1.38a). Thus parallel combination of C_1(6F) and C_q(3F) gives C_{q1} = 9F.

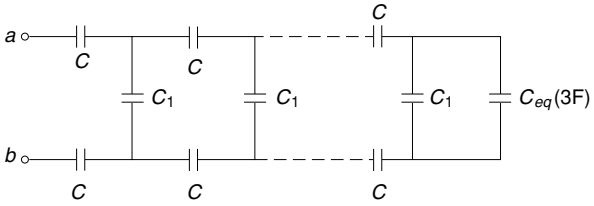


Fig. 1.38a ***Reduced network of Fig. 1.38***

Thus in this loop, there are again two capacitors of C Farad (9F) each in series with C_{q1}. The net capacitance of this loop again becomes 3F. This process continues and finally we come to the first loop while the same result is obtained.

$\therefore$ equivalent capacitance across *ab* becomes 3F (Fig. 1.38b).

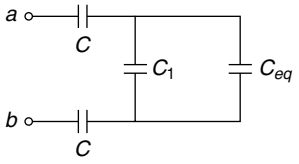


Fig. 1.38b ***Finally reduced network of Ex. 1.30***

1.31 Find the equivalent capacitance across XY (Fig. 1.39).

Solution

Each vertical column is having equivalent capacitance of

$$C_1 = 1\text{F}$$

$$C_2 = \frac{1}{2}\text{F}$$

$$C_3 = \frac{1}{4}\text{F}$$

$$C_4 = \frac{1}{8}\text{F}$$

and so on.

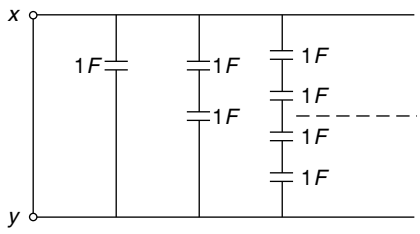


Fig. 1.39 ***Capacitance network of Ex. 1.31***

It may be noticed that all these capacitors C_1, C_2, … are in parallel (Fig. 1.34a).

$$\therefore \quad C = C_1 + C_2 + C_3 + \ldots$$

$$= 1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \ldots$$

= 2[Q it is a geometric series whose sum is 2]

$$\therefore \quad C = 2 \text{ F}.$$

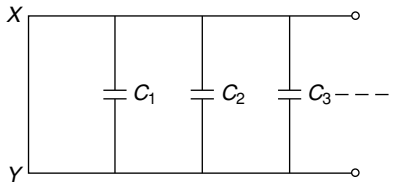


Fig. 1.39a ***Equivalent network of Fig. 1.39***

1.32 In the network of Fig. 1.40, find the capacitance between points x and y. Also find the charges on the three capacitors. Assuming the potential of y to be zero, find the potential at z.

Solution

Equivalent capacitance of 12 μF and 6 μF capacitors (being joined in series) is $12 \times 6/12 + 6 = 4$ μF (C_x), across XY.

This equivalent capacitance C_x is in parallel to the 2 μF capacitor. The final equivalent capacitance C is then

$$C = C_x + 2 = 6\ \mu\text{F}.$$

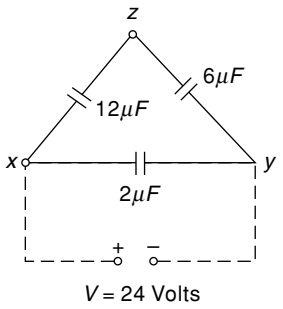


Fig. 1.40 ***Circuit of Ex. 1.32***

C is the net capacitance between x and y points. The charge supplied by the battery is then

$$Q = CV = 6\ \mu\text{F} \times 24\ \text{V}$$

$$= 144\ \mu\text{C}$$

[$\because$ Voltage across the equivalent capacitance C is 24 V]

Since the p.d. across the 2 μF capacitor is 24 V hence charge on the 2 μF capacitor is

$$2\ \mu F \times 24\ V = 48\ \mu C.$$

The charge on each of the 12 and 6 μF capacitors is then (144 μC – 48 μC), i.e. 96 μC. ∴ Drop across the 6 μF capacitor is obtained as 96 μC/6 μF = 16 Volts. Observation reveals that this 16 V drop is actually the potential V_{zy} (i.e. $V_z - V_y$). Since V_y is zero, hence $V_{zy} = V_z = 16$ V. Then potential at z with respect to y is 16 V.

1.33 The plates of a parallel plate air capacitor of a capacitance C consists of two circular plates, each of 10 cm radius and placed 0.2 cm apart. The capacitor is charged to 100 V and connected across an electrostatic voltmeter. The space between the plates is then filled up by a dielectric medium so that the capacitance of the parallel plate capacitor becomes $4.5C$ and the voltmeter now reads 25 V. What is the capacitance of the electrostatic voltmeter?

Solution

Let V be the p.d. across the combination (condenser C in parallel to capacitance C' of voltmeter). Since C and C' are in parallel (Fig. 1.41),

$$Q = CV + C'V = (C + C')V$$

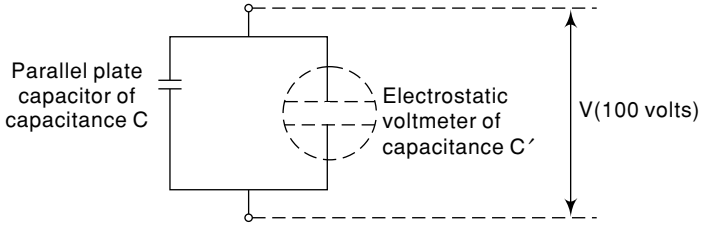


Fig. 1.41 ***Circuit of Ex. 1.33***

Let us now replace the air medium of C and fill it by a dielectric medium such that the new capacitance is $4.5C$.

Total charge remaining the same we can now write

$4.5C\ V_1 + C'V_1 = Q = (C + C')\ V$

[V_1 is the new voltage across the capacitor]

or $(4.5C + C')\ V_1 = (C + C')\ V$.

$$\therefore \quad \frac{4.5C + C'}{C + C'} = \frac{V}{V_1} = \frac{100}{25} = 4$$

$$\therefore \quad C' = \frac{C}{6} \text{ (on simplification).}$$

Now $$C = \frac{\varepsilon_o A}{x}, \text{ where } A = pr^2$$

Here, $$C = \frac{8.85 \times 10^{-12} \times \pi \times (10 \times 10^{-2})^2}{0.2 \times 10^{-2}}$$

$$= \frac{8.85 \times \pi \times 10^{-14}}{0.2 \times 10^{-2}}$$

$$= 1.39 \times 10^{-10}\ F$$

Hence $C' = \dfrac{C}{6} = 2.32 \times 10^{-11}$ F.

1.34 In Fig. 1.42, find the p.d. between (x-y) and (x-z) in steady state. Figures shown against capacitances are in μF.

Solution

At steady state all the capacitors are fully charged and no current passes through the circuit. Thus points y and z are at some potential as points a and b respectively.

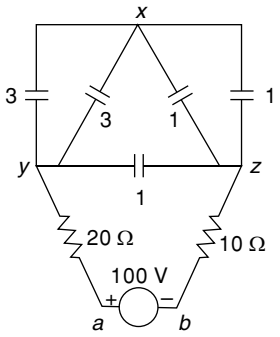


Fig. 1.42 *Network of Ex. 1.34*

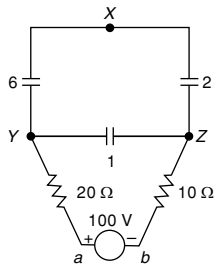


Fig. 1.42a *Reduced network of Fig. 1.42*

Figure 1.42a shows the reduced network where both 3 μF capacitors at the left hand side are replaced by their equivalent capacitance as well as two 1 μF capacitors at the right hand side of Fig. 1.42 are also replaced by their equivalent capacitance.

Further reduction of the network (shown in Fig. 1.42a) is possible (Fig. 1.42b).

We thus find the 3/2 μF equivalent capacitor is placed in parallel to the 1 μF capacitor. The charge retained by each of them will be different. We find that charge retained by the 3/2 μF equivalent capacitance is

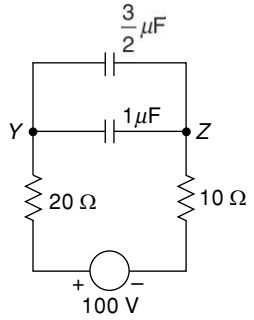


Fig. 1.42b *Final reduced network of Fig. 1.42a*

$$Q = CV = \frac{3}{2} \times 10^{-6} \times 100 = 150\ \mu C.$$

If we go back to the capacitor configuration of Fig. 1.37a, we find this 150 μC charge will be retained by capacitors 6 μF and 2 μF. Thus, the p.d. between x and y is actually the drop across the 6 μF capacitor.

$$\therefore \quad V_{x\text{-}y} = \frac{Q}{C} = \frac{150 \times 10^{-6}}{6 \times 10^{-6}} = 25 \text{ V}.$$

Similarly, p.d. at $x - z$ will be the drop across the 2 μF capacitor

$$\text{i.e.} \quad V_{x\text{-}z} = \frac{150 \times 10^{-6}}{2 \times 10^{-6}} = 75 \text{ V}.$$

[Check that, $V_{x\text{-}y} + V_{x\text{-}z} = V$.]

1.35 Three plates are held parallel to a common plate (Fig. 1.43). A is the area in m^2 for each of the three parallel plates, while d metre is the distance between each pair of plates. What is the equivalent capacitance?

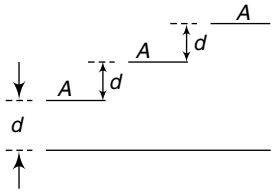


Fig. 1.43 *Three plates parallel to a common plate*

Solution

Each of the three plates form a parallel plate capacitance with the common plate (the bottom most plate). Also by virtue of their placement and configuration, these capacitances are parallel.

$\therefore$ Equivalent capacitance

$$C = C_1 + C_2 + C_3$$

$$= \frac{\varepsilon_o A}{d} + \frac{\varepsilon_o A}{2d} + \frac{\varepsilon_o A}{3d}$$

$$= \frac{\varepsilon_o A}{d}\left[1 + \frac{1}{2} + \frac{1}{3}\right] = \frac{11}{6} \times \frac{\varepsilon_o A}{d}$$

Hence, equivalent capacitance is $\frac{11}{6}\frac{\varepsilon_o A}{d}$.

1.36 Figure 1.44 represents a capacitive ladder network. Obtain equivalent capacitance across $(x - y)$.

Solution

As the capacitive ladder network is infinitely long, the capacitance of the ladder to the right of points M and N is the same as that of the ladder to the right of the points $(x - y)$.

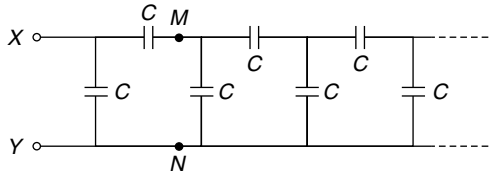


Fig. 1.44 *A capacitive ladder network*

Let the equivalent capacitance of the network to the right of $M - N$ be C_1. We must draw the reduced network (Fig. 1.44a).

The equivalent capacitance between $x - y$ is

$$C_{x-y} = C + \frac{CC_1}{C + C_1}$$

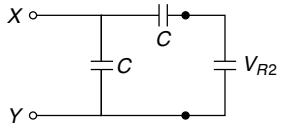


Fig. 1.44a *Reduced network of Fig. 1.44*

However, the ladder is symmetric and hence all the loops are identical to the adjacent loop. Hence the equivalent capacitance of the ladder is also C_1, i.e. $C_{x-y} = C_1$.

$$\therefore \qquad C_1 = C + \frac{CC_1}{C + C_1}$$

or $$C_1^2 - CC_1 - C^2 = 0$$

$$\therefore \qquad C_1 = \frac{C + \sqrt{C^2 + 4C^2}}{2} = \frac{1+\sqrt{5}}{2} C \qquad \text{[negative sign is neglected]}$$

1.37 A 5 μF capacitor is initially charged with 500 μC. At $t = 0$, the switch K is closed (Fig. 1.45). Determine the voltage drop across the resistor at $t < T$ and $t = \infty$.

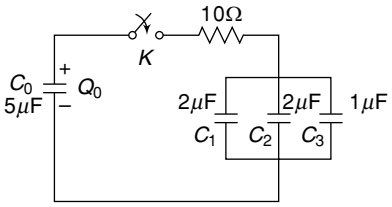


Fig. 1.45 *Circuit of Ex. 1.37*

Solution

The equivalent capacitance of bank of parallel capacitances is 5μF. As soon as K is closed, the equivalent 5μF capacitor is in series with C_0 and the net capacitance becomes 2.5 μF.

$\therefore$ T(time constant) = $R\ C_{\text{net}} = 10 \times 2.5 \times 10^{-6} = 25\mu$ sec.

The initial voltage V_0 across capacitor C_o is given by

$$V_0 = \frac{Q_0}{C_0} = \frac{500\,\mu C}{5 \times 10^{-6}} = 100 \text{ V}$$

With closing of K, capacitor C_0 will start discharging, however at $t = 0^+$, there will be no voltage across C_1, C_2 or C_3.

Thus, the entire voltage drop will be across R only (v_R) at $t = 0^+$ time.

i.e. $$v_R = V_0 \text{ (decaying)}$$

$$= V_0 e^{-t/RC} = 100\, e^{-t/25 \times 10^{-6}}$$

$$= 100\, e^{-4 \times 10^4\, t} \text{ V}$$

At $t = \infty$, v_R becomes zero.

[It is also evident that in steady state ($t = \infty$), the charge of C_0 will be distributed through C_1, C_2 and C_3 and no current will flow through the circuit. Hence, $i = 0$, $v_R = i_R = 0$].

1.38 In Fig. 1.46, a capacitor of capacitance C is charged to a voltage V_0 (dc) and is allowed to discharge through a resistance R while charging another capacitor of capacitance αC. Determine the final voltage at terminals $(a - b)$ under steady-state condition.

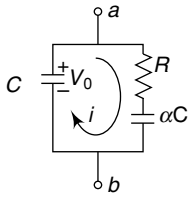


Fig. 1.46 *Circuit of Ex. 1.38*

Solution

Let V_f be the final voltage appearing across $(a - b)$ after discharging of C charging αC through R.

Equating the charge of the two capacitors

$$V_f(aC) = V_0 C - V_f C$$

or $$V_f(1 + a) = V_0$$

$$\therefore \qquad V_f = \frac{V_0}{1+\alpha}$$

[It may be noted that the final voltage across $(a - b)$ is independent of R].

1.39 In Example 1.38, what fraction of the energy originally stored is lost?

Solution

Initial energy = $\frac{1}{2}CV_o^2$ [the proof is furnished in Article 1.28]

Final energy = $\frac{1}{2}(\alpha C)V_f^2 + \frac{1}{2}CV_f^2 = \frac{1}{2}CV_f^2(1+\alpha)$

$$= \frac{1}{2}(1+\alpha)C\left(\frac{V_o}{1+\alpha}\right)^2 = \frac{1}{2}\frac{V_o^2 C}{(1+\alpha)}$$ [Q $V_f = \frac{V_o}{1+\alpha}$, as described in Ex. 1.38]

Hence, loss in energy = initial energy – final energy

$$= \frac{1}{2}CV_o^2 - \frac{1}{2}CV_o^2 \cdot \frac{1}{\alpha+1}$$

$$= \frac{1}{2}CV_o^2\left[1 - \frac{1}{\alpha+1}\right] = \frac{1}{2}CV_o^2 \cdot \frac{\alpha}{\alpha+1}$$

[It may be noted that this loss of energy is due to presence of resistance *R*. However, the energy loss expression is independent of *R*].

1.40 A 10F capacitance is charged to 5 V and is isolated. It is then connected in parallel to a 40 F capacitor. What is the decrease in total energy of the system?

Solution

$$Q_1 = C_1V_1 = 10 \times 5 = 50 \text{ C}$$

$$W_1 = \frac{1}{2}C_1V_1^2 = \frac{1}{2} \times 10 \times (5)^2 = 125 \text{ J}$$

Next, with parallel combination of 10 F and 40 F, the equivalent capacitance of the system becomes 50 F.

$\therefore$ W_2 (final energy when both the capacitors are connected in parallel)

$$= \frac{1}{2}CV^2 = \frac{1}{2}\cdot\frac{Q^2}{C} = \frac{1}{2}\times(50)^2 \times \frac{1}{50} = 25 \text{ J}$$

Thus, the decrease in total energy of the system is (125 J – 25 J), i.e. 100 J.

1.41 An uncharged capacitor is connected to a battery. Show that half the energy supplied by the battery is lost as heat while charging the capacitor.

Solution

The charge required by the capacitor is $Q = CV$ while the work done by the battery is

$$W = Q \times V$$

The capacitor would store energy of $1/2CV^2$.

However, $\frac{1}{2}CV^2 \circ \frac{1}{2}QV$.

Then the remaining energy is $\left(QV - \frac{1}{2}QV\right)$

i.e. $1/2QV$ is lost as heat. Then half the energy supplied by the battery is lost as heat.

1.42 A 1.0 μF parallel plate capacitor with air in dielectric medium is charged to 200 V at steady state. Assuming the distance between the two parallel plates to be 1.0 cm, find

(i) the electric stress on dielectric

(ii) the electric stress on plate surface and electric flux density

(iii) the charges on the plate.

(iv) if the dielectric medium of air is replaced by another dielectric medium of permittivity 4, recalculate the answers for (i) , (ii) and (iii).

Solution

(i) $E = \dfrac{V}{x}$ V/m [E = electric stress on dielectric i.e. field intensity]

$$= \frac{200}{1\times10^{-2}} = 20 \text{ kV/m}$$

(ii) Electric stress on plate surface will also be 20 kV/m while the flux density is given by

$$\delta = \varepsilon_o \times E = 8.854 \times 10^{-12} \times 20 \times 10^3$$
$$= 1.771 \times 10^{-7} \text{ C/sq. m.}$$

(iii) $Q = CV$; Q is the charge on the plate
$= 1 \times 10^{-6} \times 200 = 200$ µC.

(iv) If the air medium is replaced by another medium of permittivity 4, we can obtain the new values of E, δ and Q as follows:

$$C_{\text{new}} = \frac{\varepsilon_o \varepsilon_r A}{x}$$

$$= \varepsilon_r \times \frac{\varepsilon_o A}{x} = e_r \times 1 \times 10^{-6}$$

[Q original capacitance of the given capacitor with air on dielectric medium is given as 1 µF.]

$\therefore \quad C_{\text{new}} = 4 \times 1 \times 10^{-6} = 4$ µF

Also, $E_{\text{new}} = \dfrac{V}{x} = \dfrac{200}{1\times10^{-2}} = 20$ kV/m [distance x remains same]

$$\delta_{\text{new}} = \varepsilon_o \varepsilon_r E = 8.854 \times 10^{-12} \times 4 \times 20 \times 10^3$$
$$= 7.1 \times 10^{-7} \text{ C/m}^2$$

The new charge accumulation is

$$Q_{\text{new}} = C_{\text{new}} \times V = 4 \times 10^{-6} \times 200$$
$$= 8 \times 10^{-4} \text{ Coulomb.}$$

1.43 Two capacitors C_1 and C_2 are placed in (i) Series and (ii) Parallel. If $C_1 = 100$ µF; $C_2 = 50$ µF, find the maximum energy stored when a 220 dc supply is applied across the combination.

Solution

If C is the equivalent capacitance, for series connection of C_1 and C_2,

$$C = \frac{C_1 C_2}{C_1 + C_2} = \frac{100 \times 50}{100 + 50} = 33.33 \text{ µF.}$$

$\therefore$ Maximum energy stored is $\dfrac{1}{2} CV^2$, i.e. $\dfrac{1}{2} \times 33.333 \times 10^{-6} \times (220)^2$ i.e. 0.807 J.

When the capacitors are in parallel, $C = C_1 + C_2 = 150$ µF

\ Maximum energy stored is

$$\frac{1}{2} \times 150 \times 10^{-6} \times (220)^2 \text{ i.e. } 3.63 \text{ J.}$$

[It may be observed here that capacitor conserves maximum energy when they are in parallel configuration.]

1.44 Find the equivalent capacitance between *A* and *B* in Fig. 1.47. Assume the capacitances are equal to each other and having a value of 2 μF each.

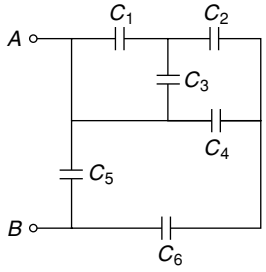
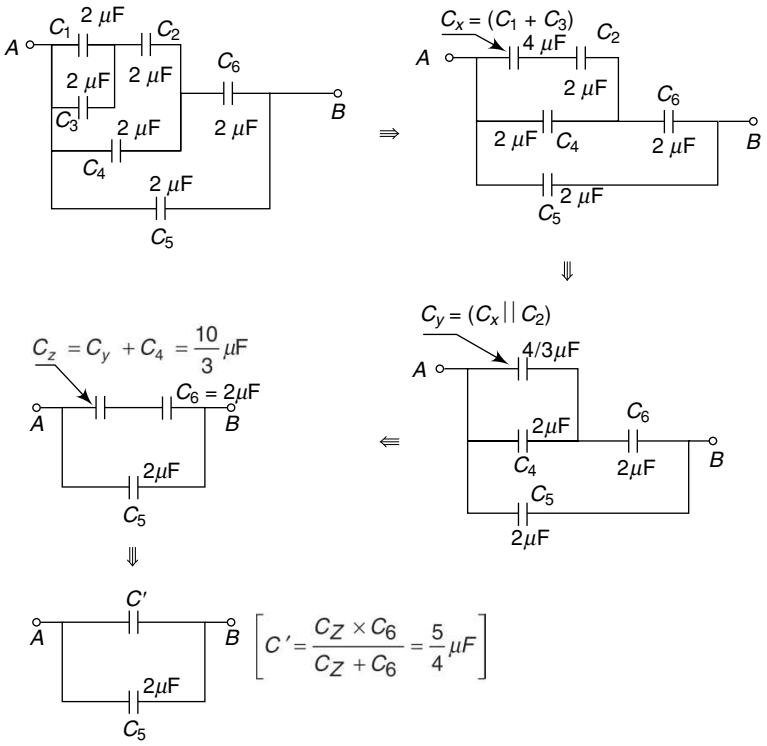


Fig. 1.47 *Capacitance configuration of Ex. 1.44*

Solution

We can reduce the given circuit as shown in Fig. 1.47(a).



$$\left[C' = \frac{C_Z \times C_6}{C_Z + C_6} = \frac{5}{4}\mu F\right]$$

Fig. 1.47a *Circuit reduction for Ex. 1.44*

Finally we obtain

$$C = C' \| C_5 = C' + C_5 = \frac{5}{4} + 2 = \frac{13}{4} \text{ mF}$$

1.45 In Fig. 1.48, if $C_1 = C_2 = C_3 = C_4 = \ldots = C_{12} = 1$ F, and $V = 10$ V, find the charge supplied by the battery. If the charging current drawn from the battery is 10 A, how much time would the battery take to charge the capacitor cube? What is the energy stored in the capacitances of the cube?

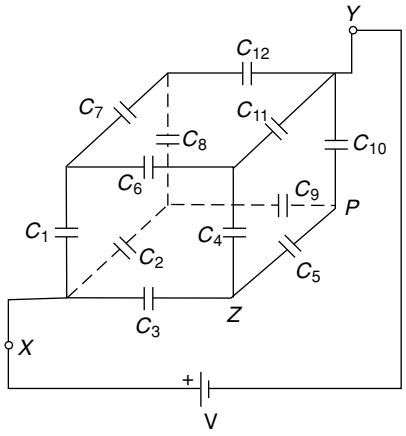


Fig. 1.48 ***Cube of Ex. 1.45***

Solution

Let us assume Q be the charge entering terminal x from the battery to the cube. Obviously, capacitance C_1, C_2 and C_3 would store charges $Q/3$, $Q/3$ and $Q/3$. Since charge (Q) leaves out terminal y hence charge on capacitors C_{10}, C_{11} and C_{12} must also be $\left(\frac{Q}{3}\right)$ each. On the other hand since C_3 is connected to C_4 and C_5 at terminal z, hence C_4 and C_5 should have a total charge equal to that stored in C_3. Hence, we can say since C_3 stores $\left(\frac{Q}{3}\right)$, hence C_4 and C_5 would individually have $\left(\frac{Q}{6}\right)$ each.

Following charging current path in the cube from x to y we find

$$V_{xy} = V_x - V_y = (V_x - V_z) + (V_z - V_p) + (V_p - V_y)$$

$$= V_{xz} + V_{zp} + V_{py} = \frac{Q/3}{C} + \frac{Q/6}{C} + \frac{Q/3}{C}$$

$$= \frac{5Q}{6C} \quad [\text{Q } C_1 = C_2 = C_3 = \ldots = C_{12} = C]$$

or $$\frac{Q}{C_{eq}} = \frac{5Q}{6C}$$

$$C_{eq} = \frac{6}{5}C = \frac{6}{5}\text{F} \quad [\text{Q } C = 1 \text{ F}]$$

Hence, charge stored in the cube is

$$Q = C_{eq} \times V = \frac{6}{5} \times 10 = 12 \text{ Coulomb.}$$

The battery supplies 12 coulomb of electricity. Also Q = Charging current × Time.

$$\therefore \quad \text{Time} = \frac{Q}{I_{ch}} = \frac{12}{10} = 1.2 \text{ sec.}$$

Energy stored in the capacitor cube

$$= \frac{1}{2}\frac{Q^2}{C_{eq}} = \frac{(12)^2}{2 \times 6/5} = 60 \text{ J.}$$

1.46 A parallel-plate capacitor has plate area of 0.1 m^2 and plate separation 0.015 cm. The dielectric medium between the plates has relative permittivity 3. The capacitors retain a charge of 1.0 μC when placed across a dc voltage source. Find the flux density, electric field strength and voltage across the plates. Assume ε_o, the permittivity space as 8.854×10^{-12} F/m.

Solution

Given:

$$A = 0.1 \text{ m}^2; x = 0.015 \text{ cm} = 0.015 \times 10^{-2} \text{ m}$$
$$\varepsilon_r = 3; Q = 1.0 \text{ μC}.$$
$$\varepsilon_o = 8.854 \times 10^{-12} \text{ F/m}$$

$\therefore$ for the given parallel-plate capacitor,

$$C = \frac{\varepsilon_o \varepsilon A}{x} = \frac{8.854 \times 10^{-12} \times 3 \times 0.1}{0.015 \times 10^{-2}}$$
$$= 0.01771 \text{ μF}.$$

Flux density is obtained identical to charge density.

$$\therefore \quad d = \frac{Q}{A} = \frac{1.0 \times 10^{-6}}{0.1} = 10 \text{ μC/m}^2.$$

Field strength (E) is obtained as

$$E = \frac{\delta}{\varepsilon_o \varepsilon_r} = \frac{10 \times 10^{-6}}{8.854 \times 10^{-12} \times 3}$$
$$= 37.65 \times 10^4 \text{ V/m}.$$

The p.d. across plates is formed as

$$V = \frac{Q}{C} = \frac{1 \times 10^{-6}}{0.01771 \times 10^{-6}} = 56.47 \text{ V}.$$

1.47 A 20 μF capacitor is charged to 100 V and then discharged through a resistor of 10 kW. Find (i) initial value of current, (ii) value of current when t = time constant, and (iii) rate at which current begins to decrease.

Solution

(i) As soon as the capacitor is switched to the discharging charging circuit having a series resistance 10 kW, the initial value of discharging current would be

$$I = \frac{100}{10^4} = 0.01 \text{ A}$$

(ii) While discharging

$$i = Ie^{-t/RC};$$

at t = time constant (RC),

$$i = Ie^{-t/t} = I \times \frac{1}{e}.$$

Here, $i = 0.01 \times \frac{1}{e} = 0.00368$ A

(iii) Normally, the time constant is RC in the discharging circuit and hence $RC = 10^4 \times 20 \times 10^{-6} = 0.2$ sec.

$$i = I \times e^{-t/RC} = 0.01 \times e^{-\frac{t}{0.2}}$$
$$= 0.01\ e^{-5t}$$

$$\therefore \quad \frac{di}{dt} \text{ (= rate of discharging)}$$
$$= 0.01(-5)e^{-5t} = -0.05e^{-5t} \text{ A/s.}$$

1.48 Two metal plates form a parallel-plate capacitor with an in-between metal plate of the same material. There are two dielectric medium K_1 and K_2 having relative permittivity ε_{r_1} and ε_{r_2} respectively as shown in figure (Fig. 1.49). If the metal plate is removed find the work done in slowly removing the plate when a p.d. of (V) volts is applied across the capacitors.

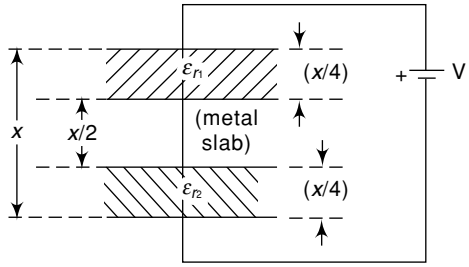


Fig. 1.49 ***A parallel-plate capacitor (Ex. 1.48)***

Solution

From the given (Fig. 1.49) it is evident that the capacitor consists of two series capacitors C_1 and C_2 when C_1 is formed with ε_{r_1} while C_2 is formed with ε_{r_2}.

$$\therefore \quad C_1 = \frac{\varepsilon_o \varepsilon_{r_1} A}{(x/4)}; \quad C_2 = \frac{\varepsilon_o \varepsilon_{r_2} A}{(x/4)}$$

and
$$C_{eq} = \left(\frac{1}{C_1} + \frac{1}{C_2}\right)^{-1} = \left(\frac{x}{4\varepsilon_o \varepsilon_{r_1} A} + \frac{x}{4\varepsilon_o \varepsilon_{r_2} A}\right)^{-1}$$
$$= \frac{4\varepsilon_o A}{x}\left[\frac{\varepsilon_{r_1} \times \varepsilon_{r_2}}{\varepsilon_{r_1} + \varepsilon_{r_2}}\right]$$

$$\therefore \text{ Energy stored } (E_1) = \frac{1}{2} C_{eq} V^2 = \frac{1}{2} \times \frac{4\varepsilon_o A}{x}\left[\frac{\varepsilon_{r_1} \times \varepsilon_{r_2}}{\varepsilon_{r_1} + \varepsilon_{r_2}}\right] V^2$$

When the metal slab is removed, there are now three capacitors formed, the first one is C_1 as it was, the second one is with dielectric medium air C_A (as the metal slab is removed, the space between ε_{r_1} and ε_{r_2} is now air) and the third one is C_2 as it was and now, C_A $= \frac{\varepsilon_o A}{x/2} = \frac{2\varepsilon_o A}{x}$.

$$\therefore \quad C'_{eq} = \left(\frac{1}{C_1} + \frac{1}{C_A} + \frac{1}{C_2}\right)^{-1} \text{ i.e., } \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_A}\right)^{-1}$$
$$= \left(\frac{x}{4\varepsilon_o \varepsilon_{r_1} A} + \frac{x}{4\varepsilon_o \varepsilon_{r_2} A} + \frac{x}{2\varepsilon_o A}\right)^{-1}$$

$$= \frac{4\varepsilon_o A}{x}\left[\frac{1}{\varepsilon_{r_1}} + \frac{1}{\varepsilon_{r_2}} + 2\right]^{-1}$$

$$= \frac{4\varepsilon_o A}{x}\left[\frac{\varepsilon_{r_1} + \varepsilon_{r_2} + 2\varepsilon_{r_1}\varepsilon_{r_2}}{\varepsilon_{r_1}\varepsilon_{r_2}}\right]^{-1}$$

$$= \frac{4\varepsilon_o A}{x}\left[\frac{\varepsilon_{r_1}\varepsilon_{r_2}}{\varepsilon_{r_1} + \varepsilon_{r_2} + 2\varepsilon_{r_1}\varepsilon_{r_2}}\right]$$

$\therefore$ Energy stored $(E_2) = \frac{1}{2} C'_{eq} V^2$

$$= \frac{1}{2} \times \frac{4\varepsilon_o A}{x}\left[\frac{\varepsilon_{r_1}\varepsilon_{r_2}}{\varepsilon_{r_1} + \varepsilon_{r_2} + 2\varepsilon_{r_1}\varepsilon_{r_2}}\right] \cdot V^2 .$$

Since work done (ΔE) is given by $(\Delta E = E_1 - E_2)$ and this represents the work done to remove the metal slab.

$$\therefore \qquad \Delta E = E_1 - E_2 = \frac{1}{2} V^2 \times \frac{4\varepsilon_o A}{x}\left[\frac{\varepsilon_{r_1}\varepsilon_{r_2}}{\varepsilon_{r_1} + \varepsilon_{r_2}} - \frac{\varepsilon_{r_1}\varepsilon_{r_2}}{\varepsilon_{r_1} + \varepsilon_{r_2} + 2\varepsilon_{r_1}\varepsilon_{r_2}}\right]$$

$$= V^2 \cdot \frac{2\varepsilon_o A \varepsilon_{r_1}\varepsilon_{r_2}}{x}\left[\frac{1}{\varepsilon_{r_1} + \varepsilon_{r_2}} - \frac{1}{\varepsilon_{r_1} + \varepsilon_{r_2} + 2\varepsilon_{r_1}\varepsilon_{r_2}}\right]$$

$$= V^2 \cdot \frac{2\varepsilon_o A \varepsilon_{r_1}\varepsilon_{r_2}}{x}\left[\frac{2\varepsilon_{r_1}\varepsilon_{r_2}}{(\varepsilon_{r_1} + \varepsilon_{r_2})(\varepsilon_{r_1} + \varepsilon_{r_2} + 2\varepsilon_{r_1}\varepsilon_{r_2})}\right]$$

$$= \frac{4\varepsilon_o A V^2 \varepsilon_{r_1}^2 \varepsilon_{r_2}^2}{x(\varepsilon_{r_1} + \varepsilon_{r_2})(\varepsilon_{r_1} + \varepsilon_{r_2} + 2\varepsilon_{r_1}\varepsilon_{r_2})} \text{ Joules.}$$

This is the work done in removing the metal slab from the capacitor.

1.49 Three delta connected capacitors are set to form a unit as shown in Fig. 1.50. It is required to transform the delta unit to equivalent star. Find these star capacitances for equal capacitances between similar terminals in both the connections.

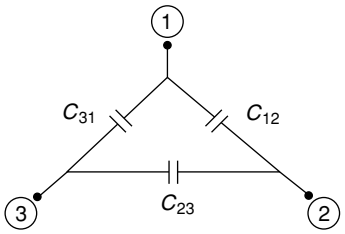


Fig. 1.50 *Delta-connected capacitors (Ex. 1.49)*

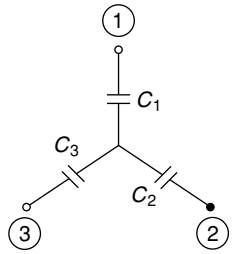


Fig. 1.50a *Equivalent star connection of delta-connected capacitors in Ex. 1.49*

Solution

Figure 1.50a represent the equivalent star capacitances provided net capacitances between terminals ① – ②, ② – ③, ③ – ① remain same for both the configurations. Capacitances between ① and ②, in star connection is $\left(\frac{C_1 C_2}{C_1 + C_2}\right)$ while that between ① and ②, in delta connection is $\left(C_{12} + \frac{C_{23} C_{31}}{C_{23} + C_{31}}\right)$.

For equal capacitance between similar terminals,

$$\frac{C_1 C_2}{C_1 + C_2} = \frac{C_{23} C_{31}}{C_{23} + C_{31}} + C_{12} = \frac{C_{23} C_{31} + C_{12} C_{23} + C_{31} C_{12}}{C_{23} + C_{31}}$$

or $$\frac{C_1 + C_2}{C_1 C_2} = \frac{C_{23} + C_{31}}{C_{23} C_{31} + C_{12} C_{23} + C_{31} C_{12}} = \frac{C_{23} + C_{31}}{\Delta} \quad \text{(i)}$$

where $D = C_{12}\ C_{31} + C_{23}\ C_{31} + C_{12}\ C_{23}$

Similarly, capacitance between ① and ③ in star connection is $\left(\frac{C_2 C_3}{C_2 + C_3}\right)$ while that in delta connection is

$$\frac{C_{31} C_{12}}{C_{31} + C_{12}} + C_{23}$$

By the same reasoning,

$$\frac{C_2 C_3}{C_2 + C_3} = C_{23} + \frac{C_{31} C_{12}}{C_{31} + C_{12}}$$

or $$\frac{C_2 + C_3}{C_2 C_3} = \frac{C_{31} + C_{12}}{\Delta} \quad \text{(ii)}$$

Also, capacitance between ③ and ① in star connection is $\frac{C_3 C_1}{C_3 + C_1}$ and that between ③ and ① in delta connection is $\frac{C_{12} C_{23}}{C_{12} + C_{23}} + C_{31}$.

$\because$ $$\frac{C_3 C_1}{C_3 + C_1} = \frac{C_{12} C_{23}}{C_{12} + C_{23}} + C_{31}, \text{ we can write}$$

$$\frac{C_3 + C_1}{C_3 C_1} = \frac{C_{12} + C_{23}}{\Delta} \quad \text{(iii)}$$

Adding (i) and (ii), we have

$$\frac{C_1 + C_2}{C_1 C_2} + \frac{C_2 + C_3}{C_2 C_3} = \frac{C_{23} + C_{31}}{\Delta} + \frac{C_{31} + C_{12}}{\Delta}$$

or, $$\frac{C_1C_3 + C_2C_3 + C_1C_2 + C_1C_3}{C_1C_2C_3} = \frac{C_{23} + C_{31} + C_{31} + C_{12}}{\Delta} \quad \text{(iv)}$$

Subtracting (iii) from (iv), we have

$$\frac{C_1C_3 + C_2C_3 + C_1C_2 + C_1C_3 - C_2C_3 - C_2C_1}{C_1C_2C_3}$$

$$= \frac{C_{23} + C_{31} + C_{31} + C_{12} - C_{12} - C_{23}}{\Delta}$$

or $$\frac{2C_1C_3}{C_1C_2C_3} = \frac{2C_{31}}{\Delta}$$

or $$\frac{1}{C_2} = \frac{C_{31}}{\Delta}, \quad C_2 = \frac{\Delta}{C_{31}}$$

$$\therefore \quad C_2 = \frac{C_{12}C_{31} + C_{23}C_{12} + C_{31}C_{23}}{C_{31}} \quad \text{(iva)}$$

$$= C_{12} + C_{23} + \frac{C_{23}C_{12}}{C_{31}} \quad \text{(ivb)}$$

Similarly,

$$C_1 = C_{31} + C_{12} + \frac{C_{31}C_{12}}{C_{23}} \quad \text{(ivc)}$$

and $$C_3 = C_{23} + C_{31} + \frac{C_{23}C_{31}}{C_{12}} \quad \text{(ivd)}$$

1.50 Three star-connected capacitances C_1, C_2 and C_3 are to be transformed to delta. Show that for equal capacitances between similar terminals in both connections,

$$C_{12} = \frac{C_1C_2}{C_1 + C_2 + C_3}$$

$$C_{23} = \frac{C_2C_3}{C_1 + C_2 + C_3}$$

$$C_{31} = \frac{C_3C_1}{C_1 + C_2 + C_3}$$

Solution

With reference to Fig. 1.51 and Fig. 1.51a, we have found out in the previous example that for capacitance between identical terminals being same for both star and delta, delta capacitances can be successfully converted to star where

$$C_1 = C_{12} + C_{31} + \frac{C_{12}C_{31}}{C_{23}} = \frac{C_{12}C_{23} + C_{23}C_{31} + C_{31}C_{12}}{C_{23}}$$

$$= \frac{\Delta}{C_{23}} \quad \text{(i)}$$

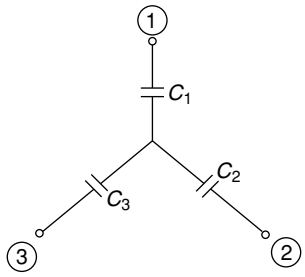


Fig. 1.51 ***Star-connected capacitors (Ex. 1.50)***

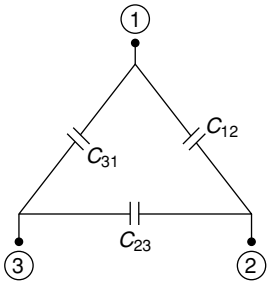


Fig. 1.51a ***Equivalent delta-connected capacitors of Ex. 1.50***

$$C_2 = C_{23} + C_{12} + \frac{C_{23}C_{12}}{C_{31}} = \frac{\Delta}{C_{31}} \tag{ii}$$

$$C_3 = C_{31} + C_{23} + \frac{C_{31}C_{23}}{C_{12}} = \frac{\Delta}{C_{12}} \tag{iii}$$

Multiplying equations (i) and (ii), (ii) and (iii) and (iii) and (i), we have

$$C_1\ C_2 = \frac{\Delta^2}{C_{23}C_{31}} \tag{iv}$$

$$C_2\ C_3 = \frac{\Delta^2}{C_{31}C_{12}} \tag{v}$$

$$C_3\ C_1 = \frac{\Delta^2}{C_{12}C_{23}} \tag{vi}$$

Inverting and adding equations (iv), (v) and (vi),

$$\frac{1}{C_1C_2} + \frac{1}{C_2C_3} + \frac{1}{C_3C_1} = \frac{C_{12}C_{23} + C_{31}C_{12} + C_{23}C_{31}}{\Delta^2}$$

or $$\frac{C_3 + C_1 + C_2}{C_1C_2C_3} = \frac{\Delta}{\Delta^2} = \frac{1}{\Delta}$$

or $$\frac{C_1C_2C_3}{C_1 + C_2 + C_3} = \text{D}$$

or $$\frac{\Delta}{C_3} = \frac{C_1C_2}{C_1 + C_2 + C_3} \tag{vii}$$

However, we have proved earlier in the preceding example

$$C_3 = C_{23} + C_{31} + \frac{C_{23}C_{31}}{C_{12}} = \frac{C_{23}C_{12} + C_{31}C_{12} + C_{23}C_{31}}{C_{12}}$$

$$= \frac{\Delta}{C_{12}}$$

$\therefore$ From equation (iii), using $C_3 = \dfrac{\Delta}{C_{12}}$, we can write

$$\frac{\Delta}{C_3} = C_{12} = \frac{C_1 C_2}{C_1 + C_2 + C_3}$$

Similarly, $$C_{23} = \frac{C_2 C_3}{C_1 + C_2 + C_3}$$

and $$C_{31} = \frac{C_3 C_1}{C_1 + C_2 + C_3}$$

1.51 A 8 μF capacitor is connected in series with a 0.5 MΩ resistor across a 200 V dc supply. Calculate (i) the time constant during charging of the capacitor, (ii) the initial charging current, (iii) the time taken for the p.d. across the capacitor to grow to 160 V and (iv) the current and the p.d. across the capacitor in 4 sec after it is connected to the supply.

Solution

(i) Time constant = $RC = 0.5 \times 10^6 \times 8 \times 10^{-6} = 4.0$ sec.

(ii) $I = \dfrac{V}{R} = \dfrac{200}{0.5 \times 10^6} = 0.4$ mA

[capacitor acts as short circuit as soon as voltage is applied and hence initial charging current is (V/R)]

(iii) $\because \quad v_C = V\left(1 - e^{-t/RC}\right)$, [refer text]

Here, $160 = 200\ (1 - e^{-t/4})$

i.e. $\dfrac{160}{200} = 1 - e^{-t/4}$ or, $0.2 = e^{-t/4}$

or, $\log_{10} 0.2 = -\dfrac{t}{4} \log_{10} e$

$\therefore \quad t = 6.438$ sec.

(iv) $i = Ie^{-t/RC}$
$= (0.4 \times 10^{-3})e^{-t/4}$
$= (0.4 \times 10^{-3})0.3679$
$= 0.147$ mA

$v = V(1 - e^{-t/RC})$
$= 200(1 - e^{-4/4})$
$= 126.40$ V.

EXERCISES

Short- and Long-Answer-Type Questions

1. State and explain Coulomb's law in Electrostatics and hence define "Coulomb", the unit for electric charge.
2. What is permittivity? What do you mean by relative permittivity of a medium? Why it does not have any unit?

3. Define electric potential and potential difference with their units. Find an expression for potential at a point within an electric field. What is equipotential surface?
4. What is meant by electric field intensity? Discuss the various factors upon which it depends.
5. Find the expression of electric field intensity and electric potential of an isolated point charge in vector form.
6. Define potential gradient. What is its unit? Why do we say electric field intensity and potential gradient both are expressed in volt/m?
7. Derive an expression of potential energy in an electric field.
8. Find a relationship between electric field strength and electric potential.
9. State Gauss' Law and derive it from Coulomb's law.
10. What do you mean by electric dipole? Obtain an expression of electric field and potential due to a dipole at an axial point.
11. (a) Define electric capacitance and derive an expression for the capacitance of a parallel-plate capacitor.
    (b) Discuss the various factors upon which the value of capacitance of parallel plate capacitor depends.
12. State the factors on which the capacitance of a condenser would depend.
13. Derive expression for the equivalent capacitance for a number of capacitors connected in (i) series, and (ii) parallel.
14. Derive the expression of capacitance of a parallel-plate capacitor with (i) uniform dielectric medium, and (ii) compound dielectric medium.
15. How would you find capacitance of multiplate capacitors?
16. Find the capacitors of an isolated sphere.
17. Derive the expression to find capacitance of concentric spheres.
18. How do you find the capacitance of a parallel plate capacitor if a metal plate (uncharged) is introduced within the parallel plates?
19. Derive an expression for the energy stored in a condenser charged to a potential.
20. Explain charging and discharging of a capacitor alongwith necessary derivation when the capacitor is connected across a dc voltage source and when discharging from steady state with resistance in series in both the cases.
21. What is the potential at $x = 0$ due to these charges in Fig. 1.52?

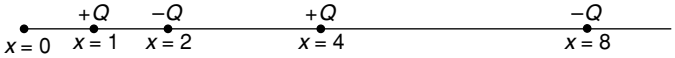


Fig. 1.52

$\rightarrow$ ***x metre*** $+Q$ at $x = 1, 4, 16, \ldots$
$-Q$ at $x = 2, 8, 32, \ldots$

$\left(Ans: V = \dfrac{Q}{6\pi\varepsilon_o} \right)$

[Hint: Potential V_1 at $x = 0$ due to +ve charges is given by

$$V_1 = \frac{Q}{4\pi\varepsilon_o(1)} + \frac{Q}{4\pi\varepsilon_o(4)} + \frac{Q}{4\pi\varepsilon_o(16)} + \ldots$$

$$= \frac{Q}{4\pi\varepsilon_o}\left(1+\frac{1}{4}+\frac{1}{16}+\ldots\right)=\frac{Q}{4\pi\varepsilon_o}\left[\frac{1}{1-1/4}\right]$$

$$= \frac{Q}{3\pi\varepsilon_o}$$

Potential V_2 at $x = 0$ due to –ve charges is given by

$$V_2 = \frac{-Q}{4\pi\varepsilon_o(2)}+\frac{-Q}{4\pi\varepsilon_o(8)}+\frac{-Q}{4\pi\varepsilon_o(32)}+\ldots$$

$$= \frac{-Q}{4\pi\varepsilon_o}\left[\frac{1}{2}+\frac{1}{8}+\frac{1}{32}+\ldots\right]=\frac{-Q}{6\pi\varepsilon_o}$$

$$\therefore \qquad V = V_1 + V_2 = \frac{Q}{6\pi\varepsilon_o}\Bigg]$$

22. Find the potential and field intensity at $x = 0$ due to these set of charges (Fig. 1.53); x represents the distance from origin in x-axis. Q is magnitude of charge.

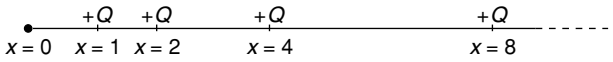


Fig. 1.53

$$\left(Ans: V = \frac{Q}{2\pi\varepsilon_o}; \frac{Q}{3\pi\varepsilon_o}\right)$$

[Hint:

$$V = \frac{Q}{4\pi\varepsilon_o}\left[1+\frac{1}{2}+\frac{1}{4}+\ldots\right]=\frac{Q}{4\pi\varepsilon_o}\times 2=\frac{Q}{2\pi\varepsilon_o}$$

$$E = \frac{Q}{4\pi\varepsilon_o x^2}=\frac{Q}{4\pi\varepsilon_o}\left[1+\frac{1}{2^2}+\frac{1}{4^2}+\ldots\right]$$

$$= \frac{Q}{4\pi\varepsilon_o}\left(1+\frac{1}{4}+\frac{1}{16}+\ldots\right)=\frac{4Q}{3}\times\frac{1}{4\pi\varepsilon_o}=\frac{Q}{3\pi\varepsilon_o}\Bigg]$$

23. Three point charges $4q$, Q and q are placed in a straight line of length l at point of distance 0, $l/2$ and l from origin respectively. The net force on charge q is zero. What is the value of Q?

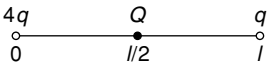


Fig. 1.54

[*Ans:* $Q = -q$]

[Hint: With ref. to Fig. 1.54, the net force on q is zero when

$$\frac{4q\times q}{4\pi\varepsilon_o\times(l)^2}+\frac{Q\times q}{4\pi\varepsilon_o(l/2)^2}=0$$

i.e $4q^2 + 4Qq = 0$

i.e $Q = -q$]

24. Eight charged drops of a fluid carry a charge of 10^{-4} μC each. Each drop has a diameter of 2 mm. If they merge together to form a single drop, find the potential of the merged big drop. (*Ans:* 3.6 kV)

[Hint: Total charge of 8 drops = 8×10^{-4} μC (=q)

Potential due to a charge 'q' is given by.

$V = \dfrac{1}{4\pi\varepsilon_o} \times \dfrac{q}{R}$, where R is the radius of the big drop and q is its charge.

Since the single big drop is equivalent to eight drops, assuming all drops to be perfect spheres,

$$8 \times \frac{4}{3} p\, r^3 \times r = \frac{4}{3} p\, R^3 \times r,$$

ρ being the density of the fluid and $\dfrac{4}{3}\pi r^3$ is the volume of each small drop.

$\therefore$ We have $8r^3 = R^3$

or $R = 2r$.

$$\therefore \quad V = \frac{1}{4\pi \times 8.854 \times 10^{-12}} \times \frac{8 \times 10^{-4} \times 10^{-6}}{2 \times 10^{-3}} = 3600 \text{ V} \Bigg]$$

25. Show that when a dielectric slab of thickness t and permittivity ε_r is inserted between two fixed charges Q_1 and Q_2, the force of repulsion between them is given by

$$F = \frac{1}{4\pi\varepsilon_o} \cdot \frac{Q_1 Q_2}{(d - t + \sqrt{\varepsilon_r}\, t)^2}$$

and hence find the dielectric constant of the slab, if on interposing another slab of same material of thickness (d/2) the force of repulsion reduceds in the ratio (9/4). Assume the distance between the fixed charges to be d.

(*Ans:* $\varepsilon_r = 4$)

$$\Bigg[\text{Hint: } F = \frac{1}{4\pi\varepsilon_o \varepsilon_r} \times \frac{Q_1 Q_2}{d^2}$$

Let us assume that when the same two charges are placed d' apart in air, same force of repulsion arises between them.

$$\therefore \quad F = \frac{1}{4\pi\varepsilon_o} \times \frac{Q_1 Q_2}{d'^2}$$

Then, $e_r d^2 = d'^2$ i.e., $d' = \sqrt{\varepsilon_r} \cdot d$

Then, d of medium is equivalent to d' of air

i.e., $\sqrt{\varepsilon_r} \cdot d$ in air.

$\therefore$ Effective air separation is $(d - t + \sqrt{\varepsilon_r} \cdot t)$

$$F = \frac{1}{4\pi\varepsilon_o} \times \frac{Q_1 Q_2}{(d - t + \sqrt{\varepsilon_r} \cdot t)^2}$$

Substituting $t = d/2$, $F' = \dfrac{1}{4\pi\varepsilon_o} \times \dfrac{Q_1 Q_2}{\left(d - \dfrac{d}{2} + \sqrt{\varepsilon_r} \cdot \dfrac{d}{2}\right)^2}$

$$= \frac{1}{4\pi\varepsilon_o} \times \frac{4 Q_1 Q_2}{(1 + \sqrt{\varepsilon_r})^2 \, d^2}$$

Force in air is $F = \dfrac{1}{4\pi\varepsilon_o} \times \dfrac{Q_1 Q_2}{d^2}$

$\therefore$ $F'/F = \dfrac{4}{(1 + \sqrt{\varepsilon_r})^2}$. But it is given $F'/F = 4/9$

$\therefore$ $\dfrac{4}{(1 + \sqrt{\varepsilon_r})^2} = \dfrac{4}{9} \therefore \sqrt{\varepsilon_r} = 2$]

26. If the capacitance between two successive plates is 0.5C (Fig. 1.55), find the capacitance of the equivalent system between points P and Q.

(*Ans:* 1.5 C)

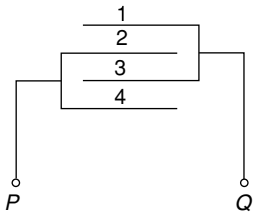


Fig. 1.55

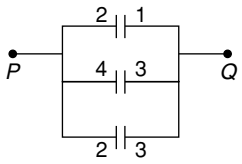


Fig. 1.55a

[Hint: The four plates form three capacitors (Fig. 1.55a)
$\therefore$ $C_{eq} = 0.5C + 0.5C + 0.5C = 1.5C$]

27. Two capacitors are once connected in parallel and then in series. If the equivalent capacitance in the two cases be 10F and 2.1F respectively, find the capacitance of each of the capacitors.

[Hint: $C_1 + C_2 = 10$; $\dfrac{C_1 C_2}{C_1 + C_2} = 2.1$

Solving, $C_1 = 7$F, $C_2 = 3$ F]

28. Two dielectrics of equal size are introduced inside a parallel plate capacitor as shown in Fig. 1.56. How does the effective capacitance charge?

(*Ans:* Increase by $\dfrac{\varepsilon_1 + \varepsilon_2}{2}$)

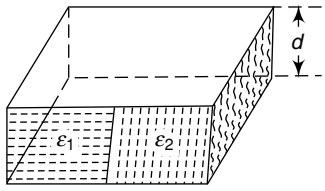


Fig. 1.56

[Hint: With introduction of two dielectrics two parallel capacitors are formed.

$$C_{eq} = \frac{\varepsilon_o \varepsilon_1 (A/2)}{d} + \frac{\varepsilon_o \varepsilon_2 (A/2)}{d} = \frac{\varepsilon_o A}{d}\left(\frac{\varepsilon_1 + \varepsilon_2}{2}\right)$$

while without these dielectrics it was $\frac{\varepsilon_o A}{d}$, assuming the area of plates to be A.

$$\therefore \quad \text{Ratio} = \frac{\frac{\varepsilon_o A}{d}\left(\frac{\varepsilon_1 + \varepsilon_2}{2}\right)}{\frac{\varepsilon_o A}{d}} = \frac{\frac{\varepsilon_1 + \varepsilon_2}{2}}{1}$$

$\because$ ε_1 and ε_2 are both more than 1, hence the new capacitance is increased by $\frac{\varepsilon_1 + \varepsilon_2}{2}$ times].

29. Find the charge drawn from the battery at steady state when K is closed. Assume $C_1 = C_2 = C$.

(Fig. 1.57) $\left(Ans: \frac{1}{2}CV\right)$

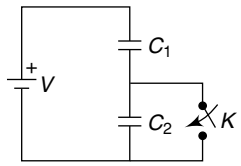


Fig. 1.57

[Hint: K open:

$$Q = C_{eq} \times V = \frac{C}{2} \times V$$

Next K closed; C_2 gets shorted. Charge is now drawn by C_1 only.

$$Q' = CV$$

$$Q' - Q = \frac{1}{2}CV$$

This is the amount of charge drawn with K closed].

30. If each of the capacitances is C, find the equivalent capacitance between A and B (Fig. 1.58).

(*Ans:* 2C)

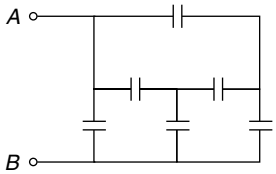


Fig. 1.58

[Hint: The given circuit can be redrawn as shown below:

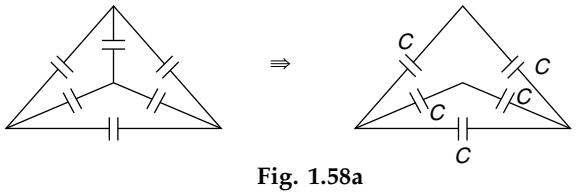


Fig. 1.58a

One capacitor may be deleted from star as no charge will flow through it since p.d. will be same across it. This simplifies the figure and we find net capacitance 2C. The problem can also be solved using (Y – D) conversion].

31. Derive an expression for the capacitance of a cylindrical capacitor of internal radius R_1 and external radius R_2. Assume appropriate length.
Solution: Let us consider an imaginary co-axial cylinder of radius n m and length 1 m between the two given cylinders. (WBUT 2008)

Area of curved surface $A = 2\pi n$ m^2

$$\text{Flux density } D = \frac{Q}{A} = \frac{Q}{2\pi n} \text{ C/m}^2$$

$$\text{Electric intensity } E = \frac{D}{\epsilon_o \epsilon_r} = \frac{Q}{2\pi \epsilon_o \epsilon_r x} \text{ V/m}$$

$$\text{Now } dV = Edx$$

$$V = \int_{R_2}^{R_1} \frac{Q dn}{2n\epsilon_o \epsilon_r n} = \frac{Q}{2n\epsilon_o \epsilon_r} l_n \frac{R_1}{R_2}$$

$$C = \frac{Q}{V} = \frac{2n\epsilon_o \epsilon_r}{\ln \frac{R_1}{R_2}} \text{ F/m}$$

$$\text{The capacitance for 1 m length is } \frac{2\pi \epsilon_o \epsilon_r l}{\ln \frac{R_1}{R_2}} \text{ F}$$

UNIVERSITY QUESTIONS WITH ANSWERS

Long-Answer-Type Question

1. Derive an expression for capacitance of a cylindrical capacitor, assuming grounded outer surface. (WBUT 2012)
Solution: Refer Article 1.29.
2. Deduce an expression showing the relation between electric field strength and potential. (WBUT 2013)
Solution: Refer Article 1.13.
3. (a) State and prove Gauss's law [WBUT 2013]
Solution: Refer Article 1.16.
(b) What is meant by potential and potential difference?
Solution: Refer Article 1.5. [WBUT 2013]
(c) Deduce an expression for electric field intensity due to an isolated point charge + q. [WBUT 2013]
Solution: Refer Article 1.7.

Multiple Choice Questions

1. In SI unit the permittivity of space t_o is
(a) 8.584×10^{-12} F/m (b) 8.854×10^{-10} F/m
(c) 8.854×10^{12} F/m (d) 88.54×10^{-12} F/m
Answer: (a) 8.584×10^{-12} F/m

2. If two static changes having megnitude of 1.0 coulomb (each) are placed at 1 m apart in space, the force of electrostatics developed is
   (a) 90×10^{10} Newtons (b) 9×10^{9} Newtons
   (c) 0.9×10^{9} Newtons (d) 0
   Answer: (b) 9×10^{9} Newtons
3. Potential gradient can be expressed as
   (a) KV × cm (b) KV/m
   (c) KV (d) KV/km
   Answer: (b) KV/m
4. The net electric field inside a conductor is
   (a) infinity (b) equal to charge per unit length
   (c) Zero (d) none of these
   Answer: (c) Zero
5. Unit of capacitance is Farad. In SI system Farad can be expressed as
   (a) Volt/m (b) Ampere/Volt
   (c) Coulomb/Volt (d) Volt/Coulomb
   Answer: (c) Coulomb/Volt
6. In two capacitors of 2F and 10 F are in series, the net capacitance is
   (a) 12 F (b) 1.67 F
   (c) 8 F (d) 20 F
   Answer: (b) 1.67 F
7. If three capacitors having capacitances of 1F are in parallel across the voltage source of 10 V, the net capacitance of the circuit is
   (a) 3 F (b) 1/3 F
   (c) 0 F (d) 9 F
   Answer: (a) 3 F
8. If the dielectric medium of a parallel plate capacitor is vacuum, the capacitance (C) is given by
   (a) $C = \dfrac{\epsilon_0\, d}{A}$ (b) $C = \dfrac{1}{\epsilon_0}\dfrac{A}{d}$
   (c) $C = \dfrac{\epsilon_0\, A}{d}$ (d) $C = \dfrac{\epsilon_0}{Ad}$
   where A is the area of each plate and d the vertical separation between the plates.
   Answer: (c) $C = \dfrac{\epsilon_0\, A}{d}$
9. The magnitude of cepacitance of an isolated sphere is
   (a) inversely proportional to its radius
   (b) directly proportional to its radius
   (c) directly proportional to square of its radius
   (d) has no relation with its radius
   Answer: (b) directly proportional to its radius
10. Time constant of a RC series circuit is given by
    (a) R/C (b) $\dfrac{1}{RC}$

(c) $\frac{C}{R}$ (d) RC

Answer: (d) RC

11. Energy stored in a capacitor is given by

(a) $\frac{Q}{2C}$ (b) $\frac{1}{2} \cdot \frac{V^2}{C}$

(c) $\frac{Q^2}{2C}$ (d) $\frac{Q}{V}$

Answer: (c) $\frac{Q^2}{2C}$

12. A 10 V dc source is directly applied across a capacitor. At steady state the current passing through the capacitor is

(a) Infinity (b) Very high

(c) Zero (d) Oscillating

Answer: (c) Zero

13. If two static charges having magnitude 1 coulomb each are placed at 1 m apart in space, the electrostatic force developed between the charges is (WBUT 2012)

(a) 90×10^{10} newtons (b) 9×10^9 newtons

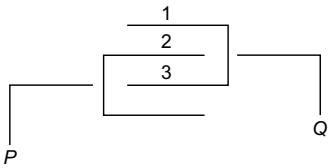
(c) 0.9×10^9 newtons (d) 0

Answer: (b) 9×10^9 newtons

14. If the capacitance between the two successive plates is 0.5 C as shown in Fig. 1.59, the value of capacitance of the equivalent system between P and Q is (WBUT 2013)

(a) 1 C (b) 0.5 C

(c) 1.5 C (d) 2 C



Answer: (c) 1.5 C (Hint: 4 plates form 3 capacitors in parallel)

15. The dielectric strength of an insulating material is expressed in (WBUT 2014)

(a) μF/m (b) kV/m

(c) kV/μF (d) none of them

Answer: (b) kV/m

16. When the plate area of a parallel-plate capacitor is increased keeping the capacitor voltage constant, the force between the plates (WBUT 2014)

(a) increases

(b) decreases

(c) remains constant

(d) may increase or decrease depending on the metal

Answer: (a) increases

2 DC MACHINES

2.1 INTRODUCTION

There are two types of *direct current* (dc) machines, the dc generator and the dc motor. The dc generator converts mechanical energy into electrical energy while the dc motor converts electrical energy into mechanical energy. The dc generator is based on the principle that when a conductor is rotated in a constant unidirectional field, a voltage will be induced in the conductor. The dc motor is based on the principle that when a current carrying conductor is placed in a magnetic field a mechanical force is exerted on the conductor. DC generator operation thus follows Fleming's right hand rule while dc motor operation follows Fleming's left hand rule.

2.2 PRINCIPAL PARTS OF A DC MACHINE

1. Magnetic field system
2. Armature
3. Commutator and brushgear.

2.2.1 Magnetic Field System

The *magnetic field system* is usually the stationary part of the machine. It produces the main magnetic field flux. The outer frame (or *yoke*) is a hollow cylinder of cast steel or rolled steel. Even number of poles (say 2, 4, 6 …) are bolted to the yoke. The poles project inwards and they are called *salient poles.* The purpose of the yoke is to support the pole cores and to act as a protective cover to the machine. It also forms a part of the magnetic circuit. Each pole core has a *pole shoe* having a curved surface to support the field coils and to increase the cross-sectional area of the magnetic circuit reducing its reluctance.

The pole cores are made of sheet steel laminations and these laminations are insulated from each other but riveted together. The poles are laminated to reduce eddy-current loss in the fields.

Each pole core has one or more field coils (windings) placed over it and are connected in series with one another such that when the current flows through the coils, alternate north and south poles are produced in the direction of rotation.

2.2.2 Armature

The rotating part of the dc machine is usually called the *armature*. The armature consists of a shaft upon which a laminated cylinder (called armature core) is mounted. The armature core has grooves (or slots) on its outer surface. The laminations are insulated from each other but tightly clamped together. In small machines the laminations may be keyed directly to the shaft. In large machines the laminations are mounted on a special frame. The purpose of using laminations is to reduce eddy-current loss in the armature core.

Insulated conductors (usually copper) are placed in the slots of the armature core and are fastened round the core to prevent them flying under centrifugal forces when the armature rotates. The conductors are suitably connected and this arrangement of conductors is called *armature winding*. Two types of windings are used; *wave* and *lap*. In wave winding the number of parallel paths of armature winding is two and in lap winding the number of parallel paths is equal to the number of poles.

2.2.3 Commutator and Brushgear

Alternating voltage is produced in the coil rotating in a magnetic field. In order to obtain direct current in the external circuit, a *commutator* is used. The commutator that rotates with the armature is made from a number of wedge-shaped hard-drawn copper bars or *segments* insulated from each other as well as from the shaft. The segments form a ring around the shaft of the armature. Each commutator segment is connected to the ends of the armature coils.

Current is collected from the armature winding by means of two or more *carbon brushes* mounted on the commutator. Each brush is supported by a metal holder called *brush holder*. The pressure exerted by the brushes on the commutator can be adjusted through this brush holder and is maintained at a constant value by means of springs. Current produced in the armature winding is passed to the commutator and then to the external circuit through brushes.

2.3 MAGNETIC FLUX PATH IN A DC GENERATOR

The magnetic circuit of a four-pole dc generator is shown in Fig. 2.1. The dotted lines indicate the main flux paths.

2.4 EQUIVALENT CIRCUIT OF A DC MACHINE

The armature of a dc generator can be represented by an equivalent electric circuit. Here E is the generated voltage, R_a is the armature resistance, and V_b is the brush contact voltage drop. The equivalent circuit of the armature of a dc generator is shown in Fig. 2.2(a), while that of a dc motor is shown in Fig. 2.2(b) (In case of dc motor E is the back emf).

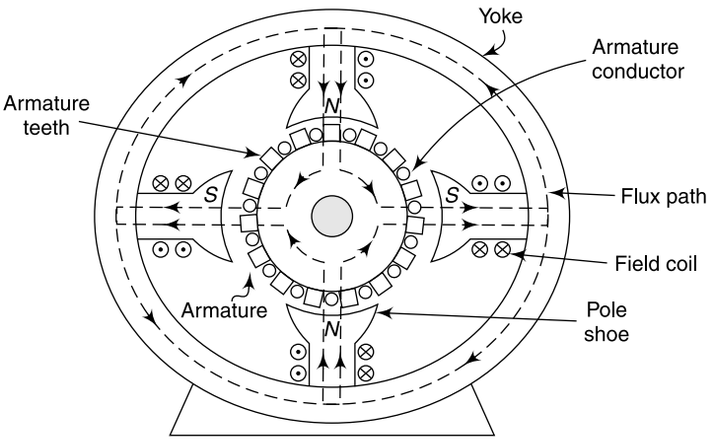
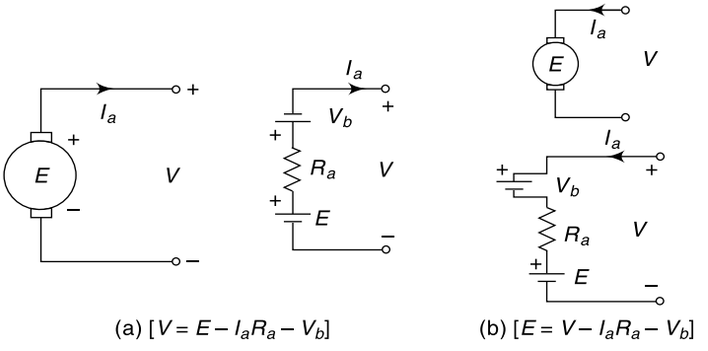


Fig. 2.1 *Magnetic flux path of a four pole dc generator*



(a) $[V = E - I_a R_a - V_b]$ (b) $[E = V - I_a R_a - V_b]$

Fig. 2.2 *Equivalent circuits of the armature (a) dc generator (b) dc motor*

2.5 DIFFERENT TYPES OF EXCITATIONS IN DC MACHINE

There are, in general, two methods of exciting the field windings of dc machines.

(a) Separate excitation
(b) Self-excitation.

2.5.1 Separate Excitation

The separately excited field winding consists of several hundred turns of fine wire and is connected to a separate or external dc source as shown in Fig. 2.3(a). The voltage of the external dc source has no relation with the armature voltage, i.e field winding energised from a separate source can be designed for any suitable voltage.

2.5.2 Self-excitation

When the field winding is excited by its own armature the machine is called a

self-excited dc machine. In these machines the field poles must have residual magnetism. A self-excited dc machine can be classified as follows:

(a) ***Shunt Excitation*** [Fig. 2.3 (b)]. Here field excitation is obtained from the armature voltage. The shunt field excitation ampere turns (AT) is obtained by having a large number of field turns with a small field current. For a generator, shunt excitation is a type of self-excitation when the field winding resistance is high but field exciting current is low.

(b) ***Series Excitation*** [Fig. 2.3 (c)]; The field is wound with a few turns of wire (of low resistance) and is excited in series from the armature current. This excitation varies with the load (current).

(c) ***Compound Excitation*** [Fig. 2.3 (d) and (e)]; Both shunt and series fields are employed in this method.

If the shunt field is connected in parallel with the armature alone the machine is called a *short shunt compound* machine [Fig. 2.3(d)] and if the shunt field is connected in parallel with both the armature and series field the machine is called a *long shunt compound* machine [Fig. 2.3(e)].

If the magnetic flux produced by the shunt field winding aids the flux produced by the series field winding the machine is *cumulatively compounded*. On the other hand, if the series field flux opposes the shunt field flux, the machine is said to be *differentially compounded*.

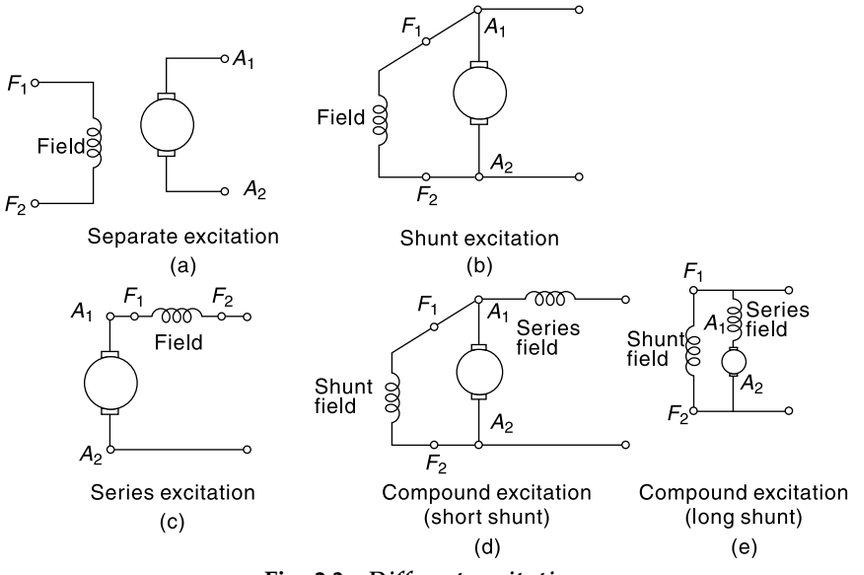


Fig. 2.3 ***Different excitations***

Depending upon the number of turns of the series field three types of compound generators can be obtained.

(a) ***Overcompounded Generator*** The generated voltage increases as the load increases.

(b) ***Level or Flat Compounded Generator*** The no load voltage is same as that of the full load voltage.

(c) ***Undercompounded Generator*** The generated voltage decreases as the load increases.

2.6 PROCESS OF VOLTAGE BUILD UP IN A SELF-EXCITED GENERATOR

Figure 2.4 shows the process of voltage build-up in a self-excited shunt generator. The line *OA* has a slope equal to the shunt field resistance R_{sh}. When the armature of the machine is rotated, a small voltage *OB* is generated due to residual magnetism in the field poles. This voltage causes field current *OC* to flow. This current *OC* increases the field flux and generates voltage *OD* which in turn results in field current *OE* which will generate a still higher voltage. This process goes on and the generated voltage continues to increase. This process continues till point *P* is reached where the generated voltage is equal to $I_{sh}\ R_{sh}$, I_{sh} being the shunt field current. If the resistance of shunt field be such that R_{sh} is equal to the slope of the line *OA′* (which is tangent to the curve *BP*) the generated voltage would remain at value *OB* only, so no voltage will build up. The value of R_{sh} corresponding to slope of the line *OA′* is known as *critical field resistance*. The voltage build up is possible only if R_{sh} is less than critical value. If the speed of the generator is decreased the slope of the curve is lower. Hence for each value of R_{sh} there is a value of critical speed. If speed is less than critical speed, no voltage build up will occur.

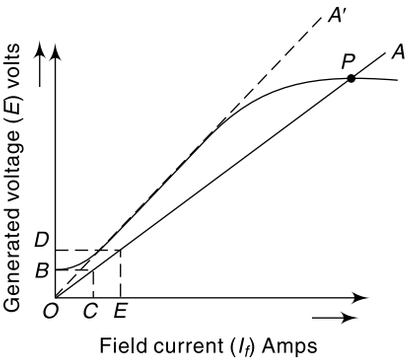


Fig. 2.4 ***Voltage build up in a self-excited generator***

The connections of the field circuit should be such that field current strengthens the residual flux. If the connections are such that field current decreases the residual flux voltage will not build up.

For series generator the resistance of the load should be less than critical resistance and load should be connected so that the load current exists. Then only voltage will build up.

Hence the *conditions for voltage build up in self-excited generators* are:

(a) Residual magnetism must be present
(b) Field winding should be properly connected so that field current strengthens the residual magnetism.
(c) The resistance of the field should be less than the critical resistance
(d) The speed of the machine should be higher than the critical speed.
(e) For series generator load should be connected and resistance of load should be less than critical resistance.

2.7 EMF EQUATION OF A DC MACHINE

As the armature of a dc machine rotates, a voltage is generated in its coils. In case of a generator, the emf of rotation E_r is called the generated emf E_g (or armature emf) and $E_r = E_g$. The direction (polarity) of dynamically induced emf can be determmed by Fleming's right hand rule.

In case of a motor, the emf of rotation E_r is known as back emf E_b (or counter emf), and $E_r = E_b$. The expression, however, is the same for both conditions of operation, whether generating or motoring; only the polarity is reversed if the rotation of the machine is in the same direction in both the modes.

Let ϕ = Useful flux per pole in webers (Wb)
P = Total number of poles
Z = Total number of conductors in the armature
n = Speed of rotation of armature in revolutions per second (rps)
A = Number of parallel paths in the armature between brushes of opposite polarity

$\therefore \quad \frac{Z}{A}$ = Number of armature conductors in series for each parallel path

Since the flux per pole is (ϕ), each conductor cuts a flux ($P\phi$) in one revolution. Generated voltage per conductor

$$= \frac{\text{Flux cut per revolution in Wb}}{\text{Time taken for one revolution in seconds}}$$

Since n revolutions are made in one second, one revolution will be made in $1/n$ second. Therefore, the time for one revolution of the armature is $1/n$ second.

The average voltage generated per conductor $= \frac{P\phi}{1/n} = nP\phi$ V.

The generated voltage E is determined by the number of armature conductors in series in any one path between the brushes. Therefore, the total voltage generated is obtained as

E = (average voltage per conductor) × (number of conductors in series per path)

i.e. $E = nP\phi \times Z/A$

$$E = \frac{nP\phi Z}{A} = \frac{P\phi ZN}{60\,A} \quad [N = \text{rpm}]. \tag{2.1}$$

Equation (2.1) is called the *emf equation of a dc machine*.

2.8 TYPES OF WINDINGS

Armature coils can be connected to the commutator to form either lap on wave windings.

Lap Winding

The ends of each armature coil are connected to adjacent segments on the commutators so that the total number of parallel paths (A) is equal to the total number of poles P. Thus for lap winding, $A = P$.

Wave Winding

In this winding, the ends of each of the armature coils is connected to the armature segement some distance apart, and only two parallel paths are provided between the positive and negative brushes. Thus, for wave winding $A = 2$.

In general, lap winding is used in low-voltage, high-current machines and winding is used in high-voltage, low-current machines.

2.1 The armature of a 4-pole 230 V wave wound generator has 400 conductors and runs at 400 rpm. Calculate the useful flux per pole.

Solution

Number of poles $P = 4$;
emf $E = 230$ V
Number of conductors $Z = 400$
$N = 400$ rpm.

As the machine is wave wound the number of parallel paths $A = 2$

$\because \quad E = \dfrac{P\phi ZN}{60\,A}$, where ϕ is flux per pole

$\therefore \quad \phi = \dfrac{60\,AE}{P\,Z\,N} = \dfrac{60 \times 2 \times 230}{4 \times 400 \times 400} = 0.043$ Wb.

2.2 A 6-pole lap wound dc generator has 250 armature conductors, a flux of 0.04 Wb per pole and runs at 1200 rpm. Find the generated emf.

Solution

Number of poles $(P) = 6$.

As the machine is lap wound the number of parallel paths, $A\ (= P) = 6$ Also, number of armature conductors $(Z) = 250$

Flux per pole, $\phi = 0.04$ Wb
Speed, $N = 1200$ rpm.

So, generated emf $E = \dfrac{P\,\phi\,ZN}{60\,A} = \dfrac{6 \times 0.04 \times 250 \times 1200}{60 \times 6} = 200$ V

2.3 An 8-pole lap wound dc generator has 1000 armature conductors, flux of 20 m Wb per pole and emf generated is 400 V. What is the speed of the machine?

Solution

Number of poles $(P) = 8$

$\therefore$ Number of parallel paths $A = P = 8$

Number of armature conductors $(Z) = 1000$;

Flux per pole $(\phi) = 20$ m Wb $= 0.02$ Wb

Emf generated $(E) = 400$ V $= \dfrac{P\,\phi\,ZN}{60\,A}$

where N is the speed of the machine in rpm.

$\therefore \qquad N = \dfrac{60\,A \times 400}{P\,\phi\,Z} = \dfrac{60 \times 8 \times 400}{8 \times 0.02 \times 1000} = 1200$ rpm.

2.4 A 4-pole generator with 400 armature conductors has a useful flux of 0.04 Wb per pole. What is the emf produced if the machine is wave wound and runs at 1200 rpm? What must be the speed at which the machine should be driven to generate the same emf if the machine is lap wound?

Solution

$$P = 4 \; ; \; Z = 400 \; ; \; \phi = 0.04 \text{ Wb} \; ; \; N = 1200 \text{ rpm.}$$

So, $$\text{emf } (E) = \frac{P \phi ZN}{60 A} = \frac{4 \times 0.04 \times 400 \times 1200}{60 \times 2} = 640 \text{ V (For wave wound } A = 2).$$

For lap wound $A = P = 4$. If N_1 be the new speed then

$$N_1 = \frac{60 AE}{P\phi Z} = \frac{60 \times 4 \times 640}{4 \times 0.04 \times 400} = 2400 \text{ rpm.}$$

2.5 An 8-pole dc generator has 96 slots and 16 conductors per slot. The flux per pole is 40 m Wb and the speed is 960 rpm. Find the emf produced if the machine is (a) wave wound, (b) lap wound.

Solution

Given $P = 8 \; ; \; Z = 96 \times 16 = 1536 \; ; \; \phi = 0.04 \text{ Wb} \; ; \; N = 960$

(a) $A = 2$ (in wave wound)

$$E = \frac{P\phi ZN}{60 A} = \frac{8 \times 0.04 \times 1536 \times 960}{60 \times 2} = 3932.16 \text{ V.}$$

(b) $A = P = 8$ (in lap wound)

$$E = \frac{3932.16 \times 2}{8} = 983.04 \text{ V.}$$

2.6 A 4-pole wave wound dc generator has 220 coils of 10 turns each. The speed is 400 rpm and resistance of each turn is 0.02 Ω. Find the emf produced and the resistance of armature winding if the flux per pole is 0.05 Wb.

Solution

$$P = 4 \; ; \text{ Total no. of turns} = 220 \times 10 = 2200$$

One turn consists of two conductors. Therefore, total number of conductors (Z) = $2 \times 2200 = 4400$.

Also. $\phi = 0.05$ Wb ; $N = 400$ rpm ; $A = 2$

Emf produced $$E = \frac{P\phi ZN}{60 A} = \frac{4 \times 0.05 \times 4400 \times 400}{60 \times 2} = 2933.33 \text{ V}$$

As the number of parallel paths is 2, so conductors per path is $\frac{4400}{2} = 2200$ or turns per path is $\frac{2200}{2} = 1100$.

$\therefore$ Armature resistance per path is $0.02 \times 1100 = 22$ Ω.

The total resistance of armature winding is thus $\frac{22}{2} = 11$ Ω.

2.9 ARMATURE REACTION

When the current flows in the armature conductors, it produces a magnetic field surrounding the conductors. This armature flux reacts with the main flux. The effect of armature flux on the main field flux is called *armature reaction*. The armature flux has two effects on the main flux:

1. It distorts the main flux.
2. It weakens the main flux.

Figure 2.5 shows a 2-pole dc generator rotating in a clockwise direction where the brushes are placed in the *geometrical neutral plane* (GNP). The currents in the conductors under the influence of North Pole (i.e alone GNP) carry currents inwards while those under the influence of South Pole (i.e below GNP) carry currents outwards. The direction of the flux due to the armature conductors in the upper and lower half of armature is shown by dotted lines. The resultant flux lies along GNP which is shown by *OA* while *OB* represents the main field flux. The net flux is shown by *OP*. The *magnetic neutral plane* (MNP) coincides with GNP in the absence of armature flux. When armature flux is present, MNP shifts from GNP in the direction of rotation. To facilitate commutator action it is essential to place the brushes along MNP. Figure 2.6 shows brushes placed along MNP. Armature mmf *OA* can be split into two components *OC* and *OD*. The component *OC* is in opposition with the main field flux and called the demagnetising component and *OD* is called the cross-magnetising component. Thus, armature reaction distorts the main field flux by its cross-magnetising flux *OD* and demagnetising flux *OC*.

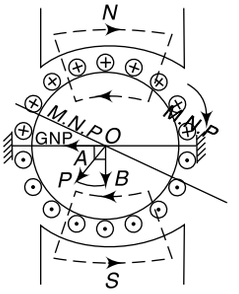


Fig. 2.5 ***Two-pole dc generator with brushes in GNP***

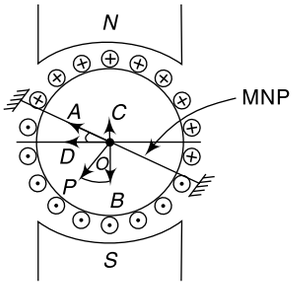


Fig. 2.6 ***Two-pole dc generator with brushes at MNP***

2.9.1 Method of Improving Armature Reaction (Compensating Winding)

The demagnetising effect of armature reaction has a detrimental effect on the operation of dc motors whenever there is a sudden change in load. This causes a sudden change in flux/pole resulting in induction of large static emf which can short-circuit the complete commutator (known as *flashover*). Armature reaction AT (Ampere-turns) in dc machines can be compensated by placing a compensating winding in the pole faces with its axis along the brush axis and excited by the armature current in series connection (Fig. 2.7) so that it causes cancellation of armature reaction AT at all values of armature current.

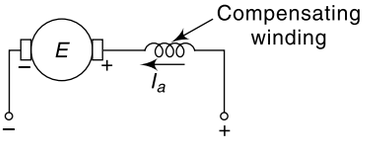


Fig. 2.7 ***Compensating winding (dc motor)***

2.10 COMMUTATION

Commutation is the process of producing a unidirectional or direct current from the alternating current generated in the armature coils.

The currents generated in the armature conductors of a dc generator are alternating. These currents flow in one direction when the armature conductors are under north pole and in the opposite direction when they are under south pole.

As conductors move out of the influence of the north pole and enter south pole, the current in them is reversed. When a brush spans two commutator segments, the winding element connected to those segements is short-circuited. During the period of short circuit of an armature coil by a brush the current in the coil must be reversed and also brought up to its full value in the reversed direction. The time of short-circuit is called the *period of commutation*. The inductive nature of the coil opposes the reversal of current from $(+I)$ to $(-I)$. If t is the time of short-circuit and L is the inductance of the coil, then the average induced voltage in the coil is

$$e_L = -L\frac{di}{dt} = \frac{-L}{t}\ [-I - (+I)] = \frac{2LI}{t}.$$

This induced voltage is called the *reactance voltage*. The sudden reversal of current as the brush leaves the segment may form an arc causing sparking at the commutator and the brush.

2.10.1 Methods of Improving Commutation

The main cause of sparking at the commutator being the reactance voltage, it can be minimised by the following methods:

(a) Use of High Resistance Carbon Brushes (use of high contact resistance carbon brushes increases the circuit resistance of coils undergoing commutation. Thus the reactance voltage is reduced.)

(b) Use of Interpoles (To reduce sparking at the commutator, small auxiliary poles called *interpoles* are provided in the machine. These are narrow cross-section poles with small cross-sectional area placed in-between the main poles. The interpoles are also called *commutating poles* (or *compoles*). The interpoles are wound with a small number of bigger cross-section conductor turns and are connected in series with the armature. Flux is produced in these poles only when current flows in the armature circuit. The flow of current in the interpole winding is such that the polarity of an interpole in a dc generator is the same as that of the next pole ahead, in the direction of rotation. In a dc motor, the polarity of an interpole is opposite to that of the next main pole in the direction of rotation.

2.11 CHARACTERISTICS OF DC GENERATORS

2.11.1 OCC (Open Circuit Characteristics) of DC Shunt Generator

Figure 2.8(a) shows a dc shunt generator on an open circuit being run at speed n rpm by means of a primemover. The field excitation is varied by regulating the resistance placed in the field circuit. The open circuit characteristic (OCC) so obtained is shown in Fig. 2.8(b). The OCC at any other speed would be a scaled version of the original OCC at rated speed (as $V_{OC} \equiv E_g \propto \omega_n$).

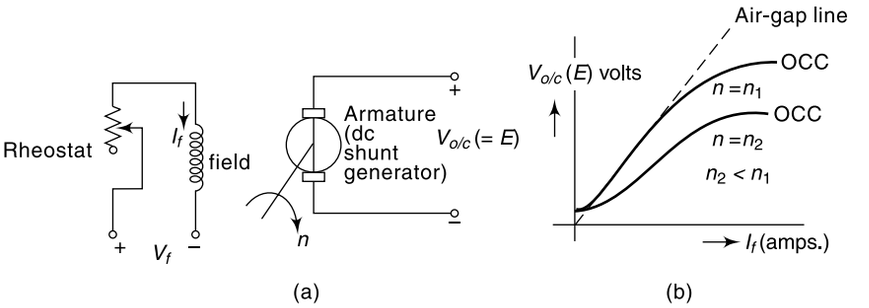


Fig. 2.8 *Open circuit characteristic of a dc generator*

2.11.2 Load Characteristics of DC Shunt Generator

The terminal voltage V versus armature current I_a characteristic is called the *internal characteristic* of a dc shunt generator and is drawn in Fig. 2.9. The load characteristic of a dc generator is called the *external characteristic*. It will only be slightly shifted from the internal characteristic as $I_L = I_a - I_f$. I_f (field current) is usually very small.

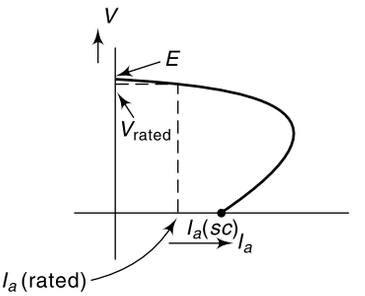


Fig. 2.9 ***Internal characterstic of dc shunt generator [terminal voltage V = Induced voltage E – drop within the armature]***

2.11.3 Characteristics of Other Generators

Figure 2.10 (a) shows a series generator with its external characteristic shown in Fig. 2.10(b). The external characteristic of a long shunt compound generator and its connection diagram are drawn in Fig. 2.11(a) and 2.11(b). The characteristic is a combination of the characteristics of shunt and series generators. Series winding turns can be so adjusted that the *OC* (open circuit) voltage equals the full load voltage. The generator is then known as level compound dc generator.

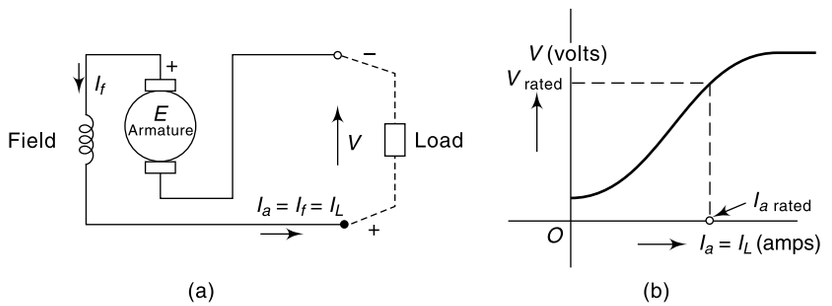


Fig. 2.10 *External characteristic of a dc generator (series)*

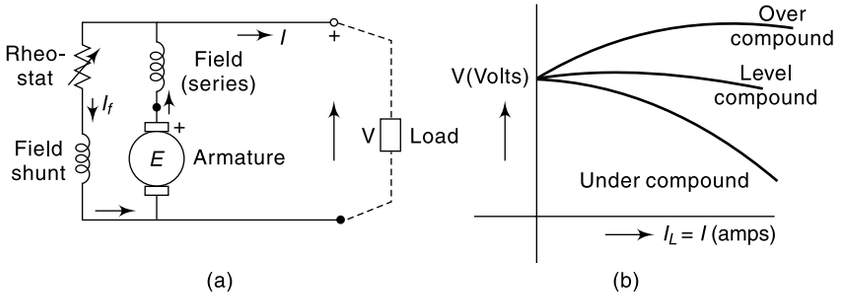


Fig. 2.11 *External characteristic of a dc generator (compound)*

2.7 A shunt wound dc generator has an induced voltage of 200 V. The terminal voltage is 180 V. Find the load current if the field and armature resistances are 100 Ω and 0.1 Ω respectively.

Solution

The shunt wound machine is shown in Fig. 2.12.

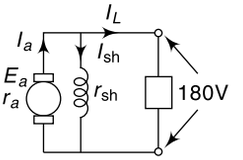


Fig. 2.12 ***A shunt wound a dc generator (Ex. 4.7)***

Induced emf E_a = 200 V

Terminals voltage V_t = 180 V

Shunt field resistance r_{sh} = 100 Ω

Armature resistance r_a = 0.1 Ω

$$\text{Field current } (I_{sh}) = \frac{V_t}{r_{sh}} = \frac{180}{100} = 1.8 \text{ A}$$

$$E_a = V_t + I_a r_a$$

where I_a is the armature current

or $$I_a = \frac{E_a - V_t}{r_a} = \frac{200 - 180}{0.1} = 200 \text{ A}$$

$\therefore$ Load current $I_L = I_a - I_{sh} = 200 - 1.8$ A $= 198.2$ A.

2.8 A 4-pole dc shunt generator having a field and armature resistance of 100 Ω and 0.2 Ω respectively supplies parallel connected 100 number of 200 V, 40 W lamps. Calculate the armature currents and generated emf. Allow 1 V per brush as brush contact drop.

Solution

Given $P = 4$; $r_{sh} = 100$ Ω and $r_a = 0.2$ Ω

Current drawn by each lamp $= \frac{40}{200}$ A

Total load current $I_L = 100 \times \frac{40}{200} = 20$ A

Since $V = 200$ V

$\therefore$ $$I_{sh} = \frac{200}{100} = 2 \text{ A}$$

Armature current $(I_a) = I_L + I_{sh} = 20 + 2 = 22$ A

Generated emf $(E) = V + I_a r_a$ + Brush drop

$= 200 + 22 \times 0.2 + 2 \times 1$

$= 200 + 4.4 + 2 = 206.4$ V.

2.9 A dc shunt generator has an induced voltage of 220 V on open circuit. When the machine is on load the voltage is 200 V. Find the load current if the field resistance is 100 Ω and armature resistance is 0.2 Ω.

Solution

Open circuit voltage $E = 220$ V
Terminal voltage $V = 200$ V
If I_a is be the armature current

$E = V + I_a r_a$, where r_a is the armature resistance.

$$\therefore \quad I_a = \frac{E - V}{r_a} = \frac{220 - 200}{0.2} \text{A} = \frac{20}{0.2} \text{A} = 100 \text{ A}$$

Field current $I_{sh} = \dfrac{V}{r_{sh}}$, where r_{sh} is the field resistance.

$$\therefore \quad I_{sh} = \frac{200}{100} = 2 \text{ A}.$$

The load current $I_L = I_a - I_{sh} = 100 - 2 = 98$ A.

2.10 A series generator delivers a load current of 50 A at 400 V and has armature and series field resistance of 0.05 Ω and 0.04 Ω respectively. Find the induced emf in the armature if the brush contact drop is 1 V per brush.

Solution

In a series generator (shown in Fig. 2.13), Load current = Armature current

$I_a = 50$ A, $V = 400$ V,
$r_a = 0.05$ Ω and $r_{se} = 0.04$ Ω,

Hence emf $= V + I_a r_a + I_a r_{se}$ + Brush drop
$= 400 + 50 \times 0.05 + 50 \times 0.04 + 2 \times 1$
$= 406.5$ V

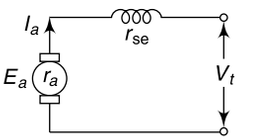


Fig. 2.13 ***A series generator (Ex. 4.10)***

2.11 A long shunt compound wound dc generator delivers a load-current of 100 A at 400 V. The armature, series and shunt field resistances are 0.04 Ω, 0.02 Ω and 200 Ω respectively. Find the armature current and the generated emf.

Solution

Referring to Fig. 2.14

$I_L = 100$ A, $V = 400$ V, $r_a = 0.04$ Ω,
$r_{se} = 0.02$ Ω and $r_{sh} = 200$ Ω.

$$\therefore \quad I_{sh} = \frac{400}{200} = 2 \text{ A}$$

and $I_a = I_L + I_{sh} = 100 + 2 = 102$ A.

Generated emf $E = V + I_a(r_a + r_{se})$
$= 400 + 102\ (0.04 + 0.02)$
$= 400 + 102 \times 0.06 = 406.12$ V.

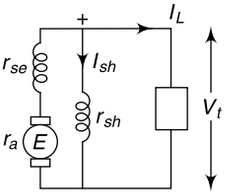


Fig. 2.14 ***A long shunt compound generator (Ex. 4.11)***

2.12 Solve Example 2.11 assuming the machine as short shunt compound.

Solution

Referring to Fig. 2.15,

$I_L = 100$ A

Voltage across shunt field winding
$= 400 + I_L r_{se}$
$= 400 + 100 \times 0.02 = 402$ V

Hence, $I_{sh} = \dfrac{402}{200} = 2.01$ A

and $I_a = I_L + I_{sh} = 100 + 2.01 = 102.01$ A

$E = 402 + I_a r_a$
$= 402 + 102.01 \times 0.04 = 406.08$ V.

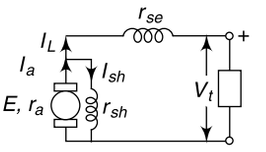


Fig. 2.15 *A short shunt compound generator*

2.12 PRINCIPLE OF OPERATION OF A DC MOTOR

When a current-carrying conductor is placed in a magnetic field, a force is produced in it. The direction of the force is obtained from Fleming's left hand rule. Let us consider one such conductor is placed in a slot of armature and it is acted upon by the magnetic field developed from a north pole of the motor. By applying Flemming's left-hand rule it can be found that the conductor has a tendency to move to the left-hand side from its axis. Since the conductor is in a slot on the circumference of the rotor, the force acts in a tangential direction to the rotor creating a torque on the rotor. Similar torques will be produced for all the rotor conductors if we assume these conductors are placed in successive slots. The rotor being free to move it then starts rotating in the anticlockwise direction. (left hand side from its axis).

2.13 BACK EMF

When the dc motor armature rotates, its conductors cut the magnetic flux. The emf of rotation E_r is then induced in them. In a motor, this emf of rotation is known as *back emf* (or *counter emf*). The back emf opposes the applied voltage. Since the back emf is induced due to generator action its magnitude is, therefore, obtained from the same expression as that for the generated emf in a dc generator.

$$E_b = \frac{NP\Phi Z}{60\,A}$$ N being the rpm, (E_b) is the back emf ($E_b = E_r$).

Here other symbols have their usual meanings.

2.14 TORQUE EQUATION OF A DC MOTOR

The expression for torque T is same for the generator and the motor. It can be deduced as follows:

The voltage equation of a dc motor is given by

$$V = E_b + I_a R_a \tag{2.2}$$

Multiplying both the sides of Eq. (2.2) by I_a we obtain

$$VI_a = E_b I_a + I_a^2 R_a. \tag{2.3}$$

However, VI_a = electrical power input to the armature

and $I_a^2 R_a$ = copper loss in the armature.

Since Input = Output + Losses, (2.4)

comparison of Eqns (2.3) and (2.4) shows that

$E_b I_a$ = electrical equivalent of gross mechanical power
[developed by the armature (electromagnetic power)]

Let T = average electromagnetic torque developed by the armature in newton metres (Nm)

$\because$ Mechanical power developed by the armature is given by,

$$P_m = \omega T = 2\pi nT \qquad [n \text{ is the speed in r.p.s i.e., } (N/60)].$$

$$\therefore \quad P_m = E_b I_a = \omega T = 2\pi nT$$

But $$E_b = \frac{nP\phi Z}{A}$$

$$\therefore \quad \frac{nP\Phi Z}{A} I_a = 2\pi nT$$

or $$T = \frac{1}{2\pi} \cdot \phi Z I_a \cdot \frac{P}{A} \text{ Nm} = 0.159\ \phi\ Z\ I_a \left(\frac{P}{A}\right) \text{ Nm}$$

and $$T = \frac{PZ}{2\pi A} \Phi\ I_a = \frac{E_b I_a}{2\pi n} = \frac{E_b I_a}{2\pi N} \times 60 \qquad (2.5)$$

Equation (2.5) is called the *torque equation* of a dc motor.

For a given dc machine, P, Z and A are constant, therefore $\left(\frac{PZ}{2\pi A}\right)$ is also a constant.

Let $$\frac{PZ}{2\pi A} = k$$

$$\therefore \quad T = k\ \phi\ I_a$$

or $$T \propto \phi\ I_a \qquad (2.6a)$$

Also $$2\pi nT = E_b I_a$$

$$\therefore \quad T = \frac{1}{2\pi} \cdot \frac{E_b I_a}{n} \text{ Nm} = 0.159\ \frac{E_b I_a}{n} \text{ Nm.} \qquad (2.6b)$$

Hence the torque developed by a dc motor is directly proportional to the product of flux per pole and armature current.

2.14.1 Torque Current Characteristic of a Shunt Motor

From the torque expression, we have

$$T \propto \phi I_a.$$

If the effect of armature reaction is neglected, ϕ is nearly constant and we can write

$$T \propto I_a.$$

The graph between T and I_a is thus a straight line passing through the origin (Fig. 2.16). In the high current region, due to saturation of the core, the $T - I_a$ characteristic loses linearity.

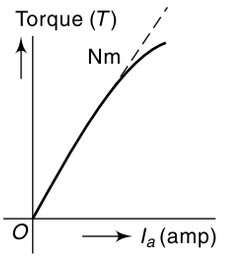


Fig. 2.16 ***Torque current characteristic of dc shunt motor***

2.14.2 Torque Current Characteristic of a Series Motor

$$T \propto \phi\ I_a$$

In series motor, before saturation $\phi \propto I_a$ and hence at rated loads,

$$T \propto I_a^2 \qquad (2.7)$$

The above equation shows that the torque/armature current T/I_a curve of a series motor will be parabolic. When the iron core becomes magnetically saturated, ϕ becomes almost constant, so that at heavy loads

$$T \propto I_a. \tag{2.8}$$

Equations (2.7) and (2.8) shows that the T/I_a characteristic is a parabolic one at light or rated loads and straight line at heavy load. Thus, the torque/current characteristic of a dc series motor is initially parabolic and finally becomes linear when the load current becomes large. This characteristic, up to the rated loading of the motor, is shown in Fig. 2.17.

The characteristic relating the net torque or useful torque T_r to the armature current is parallel to the T/I_a characteristic, but is slightly below it. The difference between the two curves is due to friction and windage losses.

Since the $T - I_a$ characteristic of a dc series motor is parabolic hence the starting torque is high for the motor for a definite starting current. This property is used in traction motors, cranes and hoists where the dc motor is to start with full load. High starting torque (being proportional to square of starting current) helps to overcome the initial inertia of the load and the dc series motor speeds up smoothy with heavy load on it.

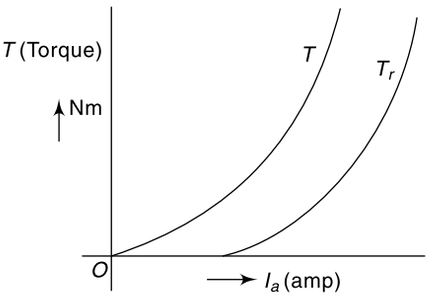


Fig. 2.17 ***Torque current characteristic of a dc series motor (up to rated loads)***

2.14.3 Torque Current Characterstic of a Compound Motor

A compound motor has both shunt and series field windings, so its characteristics are intermediate between the shunt and series motors. The cumulative compound motor is generally used in practice. The torque armature current characteristics are shown in Fig. 2.18.

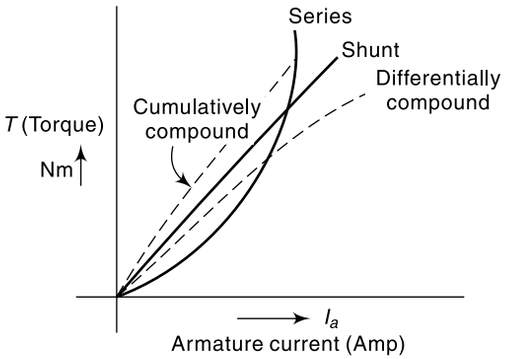


Fig. 2.18 ***Torque current characteristic of compound motor***

2.13 A 400 V, 6-pole shunt motor has a two-circuit armature winding with 250 conductors. The armature resistance is 0.3 Ω, field resistance 200 Ω and flux per pole is 0.04 Wb. Find the speed and the electromagnetic torque developed if the motor draws 10 A from the supply.

Solution

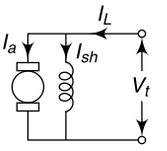


Fig. 2.19 ***A 400 V, 6-pole dc shunt motor (Ex. 4.13)***

Given $P = 6$, $Z = 250$, $r_a = 0.3\ \Omega$, $A = 2$

and $r_{sh} = 200\ \Omega$

Also, $\phi = 0.04$ Wb, $I_L = 10$ A and $V = 400$ V

$$\therefore \quad I_{sh} = \frac{400}{200} = 2\text{A} \quad \text{(from Fig. 2.19)}$$

$$I_a = I_L - I_{sh} = 10 - 2 = 8 \text{ A}$$

Back emf $E_b = V_t - I_a r_a = 400 - 8 \times 0.3 = 397.6$ V

i.e $$E_b = 397.6 = \frac{P\phi ZN}{60\,A}$$ where (N) is the speed in rpm

$$\therefore \quad N = \frac{60 \times 2 \times 397.6}{6 \times 0.04 \times 250} = 795 \text{ rpm}$$

Electromagnetic power $P_e = E_b I_a = 397.6 \times 8 = 3180.8$ W.

Electromagnetic torque $T_e = \dfrac{E_b I_a}{\omega}$, where ω is the angular velocity

But $$\omega = 2\pi \frac{N}{60} \text{ rad/s} = \frac{2\pi \times 795}{60} \text{ rad/s} = 83.21 \text{ rad/s}$$

$$\therefore \quad T_e = \frac{397.6 \times 8}{83.21} \text{ Nm} = 38.23 \text{ Nm.}$$

2.14 An 8-pole, 400 V shunt motor has 960 wave connected armature conductors. The full load armature current is 40 A and the flux per pole is 0.02 Wb. The armature resistance is 0.1 Ω and the contact drop is 1 V per brush. Calculate the full load speed of the motor.

Solution

Given $P = 8$, $V = 400$ V, $Z = 960$, $I_a = 40$ A $\phi = 0.02$ Wb,
$r_a = 0.1\ \Omega$ and $A = 2$. Also total brush drop $= 2 \times 1 = 2$ V

Back emf $E_b = V - I_a r_a$ – brush drop $= 400 - 40 \times 0.1 - 2 = 394$ V

Again, $$E_b = \frac{P\phi ZN}{60\,A}$$, where (N) is the full load speed

$$\therefore \quad N = \frac{60\,A\,E_b}{P\phi Z} = \frac{60 \times 2 \times 394}{8 \times 0.02 \times 960} \text{ r.p.m} = 308 \text{ rpm.}$$

2.15 A 42 kW, 400 V dc shunt motor has a rated armature current of 100 A at 1500 rpm. The resistance of armature is 0.2 Ω. Find (i) the internal torque developed and (ii) the internal torque if the field current is reduced to 0.9 times of its original value.

Solution

Given, $V = 400$ V, $I_a = 100$ A, $N = 1500$ r.p.m and $r_a = 0.2\ \Omega$

Back emf $E_b = V - I_a r_a = 400 - 100 \times 0.2 = 400 - 20 = 380$ V

(i) Internal torque developed

$$T_e = \frac{E_b I_a}{\omega}, \quad \text{where} \quad \omega = \frac{2\pi N}{60} \text{ rad/s} = \text{angular speed}$$

$$\therefore \quad T_e = \frac{E_b\, I_a}{2\pi N} \times 60 = \frac{380 \times 100}{2\pi \times 1500} \times 60 \text{ Nm} = 242 \text{ Nm}.$$

(ii) If the field current I_f is reduced to 0.9 times of its original value then ϕ is also reduced by 0.9 times of its previous values (as $\phi \propto I_f$).

$E_b \propto \phi$, if N is constant; hence E_b is also reduced by 0.9 times from its previous value.

Thus, the internal terque (T_e) = 0.9 × 242 = 217.8 Nm.

2.16 A 400 V, 10 kW series motor drives a fan when running at 800 rpm. The motor draws 50 A from the supply. The resistance of the armature and series field are 0.2 Ω and 0.1 Ω respectively. Determine the electromagnetic torque developed by the motor.

Solution

Terminal voltage V = 400 V
Armature current I_a = 50 A
Armature resistance r_a = 0.2 Ω
Series field resistance r_{se} = 0.1 Ω

Back emf $E_b = V - I_a(r_a + r_{se}) = 400 - 50(0.2 + 0.1) = 385$ V

Now, Speed N = 800 rpm.

∴ The electromagnetic torque developed is

$$T_e = \frac{E_b\, I_a}{\frac{2\pi N}{60}} = \frac{385 \times 50}{2\pi \times 800} \times 60 = 230 \text{ Nm}.$$

2.17 A four-pole series motor has 944 wave connected armature conductors. At a certain load the flux per pole is 34.6 m Wb and the total mechanical power developed is 4 kW. Calculate the line current taken by the motor and the speed at which it will run with the applied voltage of 500 V. The total motor resistance is 3 Ω.

Solution

Here $P = 4$, $Z = 944$, $A = 2$ and $\phi = 0.0346$ Wb

Power developed is 4 kW i.e 4000 W

If E_b be the back emf and I_a be the armature current,

$$E_b\, I_a = 4000$$

Now, V = 500 V and r = 3 Ω where (r) is the motor circuit resistance.

$$\therefore \quad E_b = V - I_a r = 500 - I_a \times 3$$

$$\text{or} \quad E_b = 500 - 3 \times \frac{4000}{E_b}$$

$$\text{or} \quad E_b^2 = 500\, E_b - 12000$$

$$\text{or} \quad E_b^2 - 500\, E_b + 12000 = 0$$

$$E_b = 25.28 \text{ V or, } E_b = 474.72 \text{ V}$$

$$\text{If} \quad E_b = 25.28 \text{ V}, \; I_a = \frac{4000}{25.28} \text{ A} = 158.22 \text{ A}$$

$$\text{If} \quad E_b = 474.72 \text{ V}, \; I_a = \frac{4000}{474.72} \text{ A} = 8.43 \text{ A}.$$

If I_a is very large the armature of the machine will be damaged. So, I_a is not equal to 158.22 A and the feasible value is I_a = 8.43 A and E_b = 474.72 V.

If N be the speed, we can write

$$E_b = 474.72 = \frac{P\phi ZN}{60\,\text{A}}$$

$$\therefore \quad N = \frac{60 \times 2 \times 474.72}{4 \times 0.0346 \times 944} \text{ rpm} = 436 \text{ rpm.}$$

2.18 A dc series motor has an armature resistance of 0.03 Ω and series field resistance of 0.04 Ω. The motor is connected to a 400 V supply. The line current is 20 A when the speed of the machine is 1000 rpm. Find the speed of the machine when the line current is 50 A and the excitation is increased by 20%.

Solution

Given, $r_a = 0.03\ \Omega$, $r_{se} = 0.04\ \Omega$, $V = 400$ V, $I_{L_1} = I_{a_1} = 20$ A

and $N_1 = 1000$ rpm.

When line current is 50 A (i.e $I_{L_2} = I_{a_2} = 50$ A), we assume speed is N_2.

If ϕ be the flux when speed is 1000 rpm, the flux becomes (1.2 ϕ) as this time excitation is increased by 20%.

We know $E_b \propto \phi N$

$$\therefore \quad \frac{E_{b_1}}{E_{b_2}} = \frac{\phi\, N_1}{1.2\,\phi\, N_2}$$

However, $E_{b_1} = V - I_{a_1}(r_a + r_{se}) = 400 - 20(0.03 + 0.04) = 398.6$ V

and $E_{b_2} = 400 - 50(0.03 + 0.04) = 396.5$ V

$$\therefore \quad N_2 = \frac{N_1\, E_{b_2}}{1.2\, E_{b_1}} = \frac{1000 \times 396.5}{1.2 \times 398.6} = 829 \text{ rpm.}$$

2.15 SPEED EQUATION OF A DC MOTOR

The emf equation of a dc machine is given by

We have, $$E = \frac{N P\phi Z}{60\ \text{A}}$$

or $$N = \frac{60\ \text{A}}{PZ}\frac{E}{\phi}$$

Therefore, $$N = \frac{E}{K\phi}$$

where $$K = \frac{PZ}{60\ \text{A}}\ .$$

This equation shows that *the speed of a dc machine is directly proportional to the emf of rotation E and is inversely proportional to flux per pole* ϕ. Since the expression for emf of rotation applies equally to motors and generators, it gives the speed for both motors and generators.

If the suffixes 1 and 2 denote the initial and final values, we can write

$$N_1 = \frac{E_1}{k\phi_1}$$

$$N_2 = \frac{E_2}{k\phi_2}$$

$$\therefore \quad \frac{N_2}{N_1} = \frac{E_2}{E_1} \times \frac{\phi_1}{\phi_2}$$

For dc shunt motor, $\phi_1 = \phi_2$ for rated load conditions. Thus for such a motor we can write

$$\frac{N_2}{N_1} = \frac{E_{b\,2}}{E_{b\,1}}$$

2.16 SPEED REGULATION OF DC MOTOR

The *speed regulation* is defined as the change in speed from no load N_{nl} to full load N_{fl} expressed as a fraction or a percentage of the full load speed. It can be written as:

$$\text{Per unit speed regulation} = \frac{N_{\text{nl}} - N_{\text{fl}}}{N_{\text{fl}}}$$

$$\therefore \quad \text{Per cent speed regulation} = \frac{N_{\text{nl}} - N_{\text{fl}}}{N_{\text{fl}}} \times 100.$$

A motor which has a nearly constant speed at all loads is said to have a good speed regulation.

2.17 SPEED VS. ARMATURE CURRENT CHARACTERISTIC OF DC MOTOR (N/I_a CHARACTERISTICS)

2.17.1 Shunt Motor

In a shunt motor, $I_{\text{sh}} = V/R_{\text{sh}}$. If V is constant I_{sh} will also remain constant. Hence the flux is constant at no load. The flux decreases slightly due to armature reaction. If the effect of armature reaction is neglected, the flux ϕ will remain constant. The motor speed being given by

$$N \propto \frac{V - I_a R_a}{\phi} \quad \left(= \frac{E_b}{K\phi}\right)$$

For ϕ remaining constant, the speed can be written as

$$N \propto V - I_a R_a$$

This is an equation of a straight line with a negative slope. That is, *the speed N of the shunt motor decreases linearly with the increase in armature current* as shown in Fig. 2.20.

Since $I_a R_a$ at full load is very small compared to V, the drop in speed from no load to full load is very small in well designed machines. The decrease in speed is partially neutralized by a reduction in ϕ due to armature reaction. Hence for all practical purposes *the shunt motor may be taken as a constant-speed motor*.

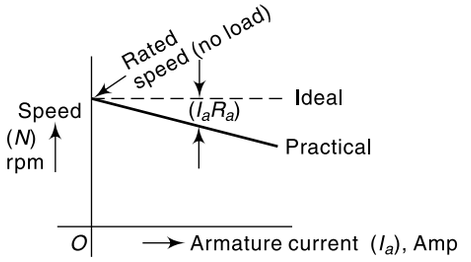


Fig. 2.20 ***Speed vs current characteristic of a dc shunt motor***

2.17.2 Series Motor

The motor speed N for a series motor is given by

$$N \propto \frac{V - I_a (R_a + R_{se})}{\phi} \quad \left(= \frac{E_b}{K\phi}\right)$$

At low values of I_a, the voltage drop $[I_a (R_a + R_{se})]$ is negligibly small in comparison with V

$$\therefore \qquad N \propto \frac{V}{\phi}$$

Since V is constant,

$$N \propto \frac{1}{\phi}$$

In a series motor, the field flux ϕ is produced by the armature current flowing in the field winding so that $\phi \propto I_a$. Hence the series motor is a variable flux machine.

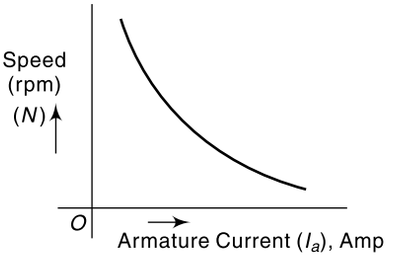


Fig. 2.21 ***Speed vs current characteristic of a dc series motor***

Also,

$$N \propto \frac{1}{I_a}$$

Thus, for *the series motor, the speed is inversely proportional to the armature (load) current*. The speed-load characteristic is a rectangular hyperbola as shown in Fig. 2.21.

The speed equation shows that when the load decreases, the speed will be very large. Therefore at no load (or at light loads) there is a possibility of dangerously high speed, which may damage the series motor due to large centrifugal forces. Hence a series motor should never be run unloaded. It should always be coupled to a mechanical load either directly or through gearing. It should not be coupled by belt, which may slip at any time making the armature unloaded. With the increase in armature current (i.e the field current) the flux also increases and therefore the speed is reduced.

2.17.3 Compound Motor

The speed-armature current characteristics are shown in Fig. 2.22. In differentially compound motor, because of weakening of field, speed increases with increase in armature current while in cummulatively compound, the speed drops because of increase of field flux with armature current.

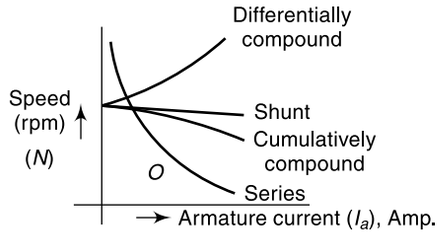


Fig. 2.22 *Speed vs current characteristic of a dc compound motor*

2.18 SPEED TORQUE CHARACTERISTIC OF DC MOTORS

2.18.1 Shunt Motor

Since the torque is proportional to armature current in a dc shunt motor the speed torque characteristic of such a motor will be identical to the speed armature current characteristic. The speed torque characteristic of the shunt motor is shown in Fig. 2.23.

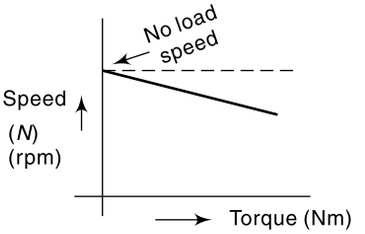


Fig. 2.23 *Speed torque characteristic of a dc shunt motor*

2.18.2 Series Motor

The speed/torque characteristic of a dc series motor can be derived from its speed/armature current N/I_a and torque/armature current T/I_a characteristics. The characteristic (Fig. 2.24) shows that the dc series motor has a high torque at a low speed and a low torque at a high speed. Hence the speed of the dc series motor changes considerably with increasing load. It is a very useful characteristic for traction purposes, hoists and lifts where at low speeds a high starting torque is required to accelerate large masses.

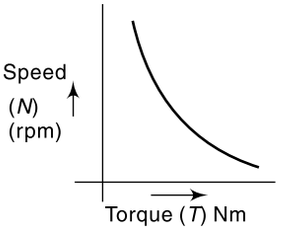


Fig. 2.24 *Speed torque characteristic of a dc series motor*

2.18.3 Compound Motor

Figure 2.25 shows the speed-torque (N/T) characteristic of a dc compound motor. A compound motor has a high starting torque together with a safe no-load speed. These factors make it suitable for use with heavy intermittent loads such as lifts, hoists etc.

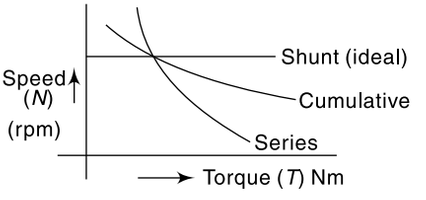


Fig. 2.25 *Speed torque characteristic of a dc compound motor*

2.19 Find the no load and full load speeds of a 220 V, four-pole shunt motor having following data flux 0.04 *Wb*, armature resistance 0.04 Ω, 160 armature conductors, wave connection, full load line current 95 A, no load line current 9 A, field resistance 44 Ω.

Solution

Here $P = 4$, $V = 220$ V, $\phi = 0.04$ *Wb*, $r_a = 0.04\ \Omega$ $Z = 160$ and $A = 2$.

Also, $r_{sh} = 44\ \Omega$ and $I_{sh} = \dfrac{220}{44}\text{A} = 5$ A.

Under full load condition

$$I_{Lfl} = 95 \text{ A}$$

$$\therefore \quad I_{afl} = 95 - 5 = 90 \text{ A}$$

$$E_{bfl} = 220 - 90 \times 0.04 = 216.4 \text{ V}.$$

Under no load condition

$$I_{LO} = 9 \text{ A}$$

$$\therefore \quad I_{ao} = 9 - 5 = 4 \text{ A}$$

and $$E_{bo} = 220 - 4 \times 0.04 = 219.84 \text{ V}.$$

Now, $$E_{bo} = \frac{P\phi ZN_o}{60\text{ A}} \quad \text{or} \quad N_o = \frac{60\,AE_{b_o}}{P\phi Z} = \frac{60 \times 2 \times 219.84}{4 \times 0.04 \times 160} = 1030.5 \text{ rpm}$$

Also $$E_{bfl} = \frac{P\phi ZN_{fl}}{60\text{ A}} \quad \text{or} \quad N_{fl} = \frac{60 \times 2 \times 216.4}{4 \times 0.04 \times 160} = 1014 \text{ rpm}.$$

Hence the no load and full load speeds are 1030.5 rpm and 1014 rpm.

2.20 A 220 V series motor runs at 400 rpm and takes a line current of 50 A. Find the speed and percentage change in torque if the load is reduced so that the motor takes 20 A. The armature and the field circuit resistance is 0.5 Ω. Assume that the flux is proportional to the field current.

Solution

Given $V = 220$V, $N_1 = 400$ r.p.m, $I_{L_1} = I_{a_1} = 50$ A

$(r_a + r_{se}) = 0.5\ \Omega$, $I_{L2} = I_{a2} = 20$ A.

Let the torque when line current is 50A be T_{e1} and when the line current is 20 A the torque be T_{e2}

Now $$E_{b_1} = V - I_{a1}(r_a + r_{se}) = 220 - 50(0.5) = 195 \text{ V}$$

and $$E_{b_2} = V - I_{a2}(r_a + r_{se}) = 220 - 20(0.5) = 210 \text{ V}$$

Also, $$\frac{E_{b_1}}{E_{b_2}} = \frac{\phi_2 N_1}{\phi_2 N_2} = \frac{I_{a_1} N_1}{I_{a_2} N_2} \quad (\because \phi \propto I_a)$$

or $$N_2 = \frac{E_{b_2}}{E_{b_1}} \times \frac{I_{a_1}}{I_{a_2}} N_1 = \frac{210}{195} \times \frac{50}{20} \times 400 = 1077 \text{ rpm}$$

$$\frac{T_{e_2}}{T_{e_1}} = \frac{\phi_2 I_{a_2}}{\phi_1 I_{a_1}} = \frac{I_{a_2}^2}{I_{a_1}^2} \quad (\because \phi \propto I_a)$$

or $$\frac{T_{e_2}}{T_{e_1}} = \left(\frac{20}{50}\right)^2 = \frac{4}{25}.$$

Percentage change in torque is $\left(1 - \dfrac{4}{25}\right) \times 100\%$ or, 84%

2.19 SPEED CONTROL OF DC MOTORS

The speed of a dc motor is given by the relationship

$$N = \frac{V - I_a R_a}{K\phi}$$

This speed is thus dependent upon the supply voltage V, the armature circuit resistance R_a, and the field flux ϕ, which is produced by the field current. Thus there are two general methods of speed control of dc motors:

(i) Variation of resistance in the armature circuit. This method is called armature resistance control.

(ii) Variation of field flux (ϕ). This method is called field resistance control.

2.19.1 Armature Resistance Control

In this method a variable series resistor R_e is connected in series with the armature circuit. Figure 2.26 shows the method of connection for a shunt motor. The field is directly connected across the supply and therefore the flux (ϕ) is not affected by variation of R_e.

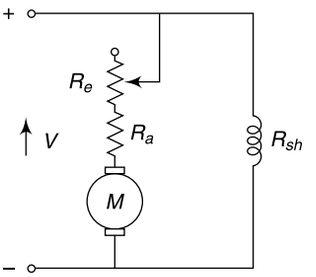


Fig. 2.26 *Speed control of a dc shunt motor by armature resistance control*

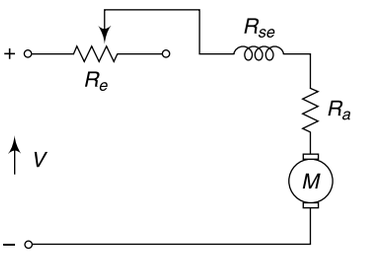


Fig. 2.27 *Speed control of a dc series motor by armature resistance control*

Figure 2.27 shows the method of connection of external resistance R_e in the armature circuit of a d.c series motor.

Figures 2.28(a) and (b) show typical speed/current characteristics for shunt and series motors respectively. In both the cases the motor runs at a lower speed as the value of R_e is increased. R_e carries full armature current hence R_e should be designed to carry continuously the full armature current. The main disadvantages of armature control are as under:

(a) A large amount of power is wasted in the external resistance (R_e).

(b) Speed control is limited to give speeds below rated and increase of speed is not possible by this method.

(c) For a given value of the external resistance the speed reduction is not constant but varies with the motor load.

This method can only be used for small dc motors.

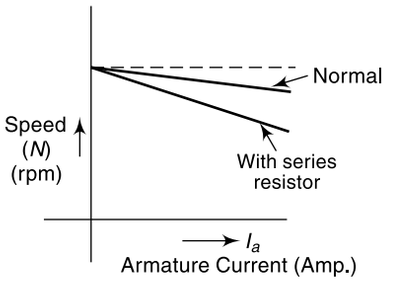


Fig. 2.28(a) *Speed current characteristic for shunt motor*

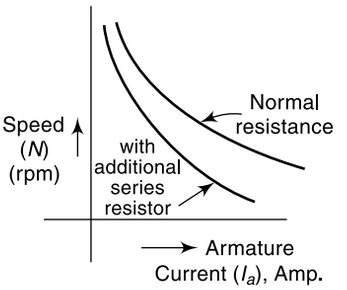


Fig. 2.28(b) *Speed current characteristic for series motor*

2.19.2 Variation of Field Flux (ϕ)

The flux in the dc motor being produced by the field current, control of speed is possible by field current variation. In the shunt motor, field current control is acheived by connecting a variable resistor R_C in series with the shunt field winding as shown in Fig. 2.29. The resistor R_C is called the shunt *field regulator*.

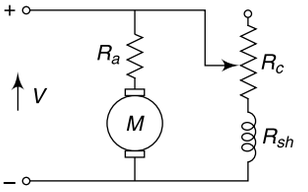


Fig. 2.29 *Speed control of dc shunt motor by field flux control*

The connection of R_C in the field reduces the field current which in turn reduces the flux ϕ. The reduction in flux will result in an increase in the speed. This method of speed control is used to give motor speeds above normal speed. The variation of field current in a series motor is done by any one of the following methods:

(a) A variable resistance R_d is connected in parallel with the series field winding as shown in Fig. 2.30. The parallel resistor is called the *diverter*. A portion of the main current is diverted through R_d, thus the diverter reduces the current flowing through the field winding. This reduces the flux and increases the speed.

(b) The second method uses a tapped field control as shown in Fig. 2.31.

Here the ampere-turns are varied by varying the number of field turns. This arrangement is used in electric traction.

Figures 2.32(a) and (b) show the typical speed/torque curves for shunt and

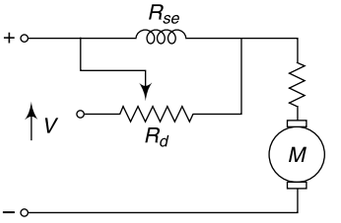


Fig. 2.30 *Speed control of dc series motor by using diverter in the field circuit*

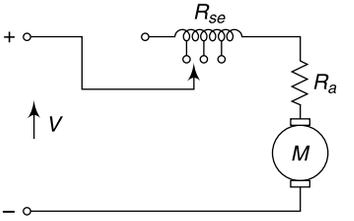


Fig. 2.31 *Speed control of dc series motor by using tapped field control*

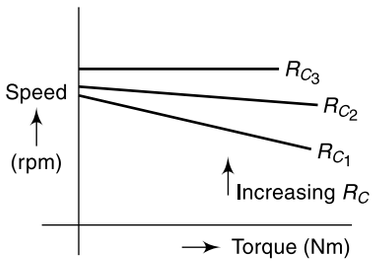


Fig. 2.32(a) ***Speed torque characteristic of a shunt motor***

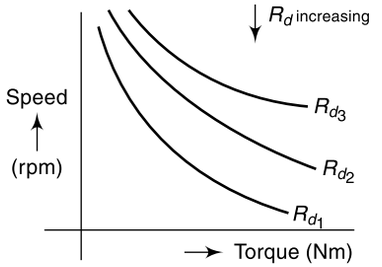


Fig. 2.32(b) ***Speed torque characteristic of a series motor***

series motors respectively, whose speeds are controlled by the variation of the field flux.

The advantages of field control are that this method is easy and convenient and since the shunt field current I_{sh} is very small, the power loss in the shunt field is also small.

2.21 A shunt wound motor with an armature resistance of 0.2 Ω is connected across a 400 V supply. The armature current is 40 A and the speed of the motor is 1000 rpm. Calculate the additional resistance which should be connected in series with the armature to reduce its speed to 700 rpm. Assume that the armature current remains the same.

Solution

Here $r_a = 0.2\ \Omega$, $V = 400$ V, $I_a = 40$ A and $N_1 = 1000$ rpm.

Let the additional resistance connected in series with armature R and $N_2 = 700$ rpm.

$$E_{b1} = V - I_a r_a = 400 - 40 \times 0.2 = 392 \text{ V}$$

$$E_{b2} = V - I_a(r_a + R) = 400 - 40\ (0.2 + R)$$

Now for shunt motor $E_b \propto N$ (as ϕ is constant).

Hence $$\frac{E_{b_1}}{E_{b_2}} = \frac{N_1}{N_2} = \frac{1000}{700}$$

or $$E_{b_2} = \frac{7}{10} E_{b_1} = \frac{7 \times 392}{10} = 274.4 \text{ V}$$

$\therefore$ $$274.4 = 400 - 40(0.2 + R)$$

or $$8 + 40R = 400 - 274.4 = 125.6 \text{ V}$$

or $$R = 2.94\ \Omega$$

2.22 A series wound dc motor runs at 500 rpm and is connected across 220 V supply. The line current is 10 A and armature circuit resistance is 0.6 Ω. Find the resistance to be inserted in series to reduce the speed of the machine to 400 rpm assuming torque to vary as the square of the speed.

Solution

Given $N_1 = 500$ rpm, $V = 220$ V, $I_{a1} = 10$ A, $(r_a + r_{se}) = 0.6\ \Omega$

$N_2 = 400$ r.p.m and $T_e \propto N^2$

$$E_{b_1} = V - I_{a_1}(r_a + r_{se}) = 220 - 10 \times 0.6 = 214 \text{ V}$$

$$E_{b_2} = V - I_{a_2}(0.6 + R)$$

where R is the resistance to be inserted in series with the armature.

Now, for series motor $T_e \propto I_a^2$.

Hence $$\frac{T_{e_1}}{T_{e_2}} = \frac{I_{a_1}^2}{I_{a_2}^2} = \frac{N_1^2}{N_2^2} = \frac{(500)^2}{(400)^2} = \frac{25}{16}$$

or $$I_{a_2} = \sqrt{\frac{16}{25}}\ I_{a_1} = \frac{4}{5} I_{a_1} = 0.8\ I_{a1} = 0.8 \times 10 = 8\ \text{A}$$

and $$\frac{E_{b_1}}{E_{b_2}} = \frac{\phi_1 N_1}{\phi_2 N_2} = \frac{I_{a_1} N_1}{I_{a_2} N_2} \quad (\because \text{in series motor } \phi \propto I_a)$$

or $$\frac{214}{220 - 8\,(0.6 + R)} = \frac{10 \times 500}{8 \times 400}$$

or $(220 - 4.8 - 8R)50 = 32 \times 214 = 6848$

or $215.2 - 8R = 136.96$

or $R = 9.78\ \Omega$.

2.23 A 220 V series motor takes 10 A and runs at 600 rpm. The total resistance is 0.8 Ω. At what speed will it run, when a 5 Ω resistance is connected in series, the motor taking the same current at the same supply voltage.

Solution

Here, $V = 220$ V, $I_a = 10$ A, $N_1 = 600$ r.p.m, $r_a = 0.8\ \Omega$

$R = 5\ \Omega$; $E_1 = V - I_a r_a = 220 - 10 \times 0.8 = 212$ V

$E_2 = V - I_a(r_a + R) = 220 - 10(0.8 + 5) = 220 - 58 = 162$ V

Let the speed be N_2 when 5 Ω resistor is added.

$$\therefore \quad \frac{E_1}{E_2} = \frac{\phi_1 N_1}{\phi_2 N_2} = \frac{N_1}{N_2} \quad (\text{As } I_a \text{ remains same})$$

or $$N_2 = \frac{E_2}{E_1}\ N_1 = \frac{162}{212} \times 600 = 458\ \text{rpm}.$$

2.24 A 500 V dc shunt motor runs at 250 rpm at rated full load condition and takes an armature current of 200 A. The armature resistance is 0.12 Ω. Find the speed of the motor when the field circuit resistance is increased such that the flux is reduced to 80% of the normal value and the motor is loaded for an armature current of 100A.

Solution

Given, $V = 500$ V, $N_1 = 250$ rpm. $I_a = 200$ A and $r_a = 0.12\ \Omega$

$E_{b_1} = V - I_a r_a = 500 - 200 \times 0.12 = 476$ V

Let initial flux be ϕ.

When armature current I_a' is 100 A, the flux $\phi' = 0.8\ \phi$, and the speed is N, we have

$E_{b2} = V - I_a' r_a = 500 - 100 \times 0.12 = 488$ V

$$\because \quad \frac{E_{b_1}}{E_{b_2}} = \frac{\phi N_1}{\phi' N_2} \quad \text{or,} \quad N_2 = \frac{E_{b_2}}{E_{b_1}} \frac{\phi}{\phi'}\ N_1 = \frac{488}{476} \times \frac{\phi}{0.8\,\phi} \times 250$$

$$\therefore \quad N_2 = 320\ \text{rpm}.$$

2.25 A dc shunt machine connected to a 400 V mains has an armature and field circuit resistance of 0.2 Ω and 250 Ω respectively. Find the ratio of the speed when the machine acts as a generator to the speed when the machine acts as a motor, if the line current in each case is 100 A.

Solution

Given $V = 400$ V, $r_a = 0.2\ \Omega$, $r_{sh} = 250\ \Omega$, $I_L = 100$ A

Also, $$I_{sh} = \frac{400}{250} = 1.6 \text{ A}$$

When the machine acts as a generator

$$I_{a_1} = 100 + 1.6 = 101.6 \text{ A} \quad [\because I_{a(gen)} = I_L + I_f]$$

$$E_1 = V + I_{a_1} r_a = 400 + 101.6 \times 0.2 = 420.32 \text{ V}$$

Let the speed of the generator be N_1 when the machine acts as a motor.

$$I_{a_2} = 100 - 1.6 = 98.4 \text{ A} \quad [I_{a\,(\text{motor})} = I_L - I_f]$$

So, $E_2 = V - I_{a_2} r_a = 400 - 98.4 \times 0.2 = 380.32$ V

$$\therefore \quad \frac{E_1}{E_2} = \frac{\phi_1 N_1}{\phi_2 N_2} = \frac{N_1}{N_2} \quad \text{(As flux is constant)}$$

or $$\frac{N_1}{N_2} = \frac{420.32}{380.32} = 1.105.$$

2.20 LOSSES IN A DC MACHINE

There are three types of major losses in a dc machine.

(a) Copper Losses There are two types of copper losses. One is *armature copper loss* and the other is *field copper loss*. Armature copper loss = $I_a^2 r_a$, where I_a is the armature current and r_a is the armature resistance.

Field copper loss = Shunt field copper loss + Series field copper loss.

$= I_{sh}^2 r_{sh} + I_{se}^2 r_{se}$, where I_{sh} and I_{se} are the shunt and series field current, r_{sh} and r_{se} are the shunt and series field resistance.

Brush contact loss is due to resistance of the brush contact. It is included in armature copper losses.

(b) Iron Losses (Core or Magnetic Losses) These losses occur in the armature and field core. They are of two types—*hysteresis loss* and *eddy current loss*. Hysteresis loss = $K_h B_m^{1.6} f$ and Eddy current loss = $K_B B_m^2 f$ where B_m = maximum flux density, f = frequency of magnetic reversal and K_h and K_e are constants.

(c) Mechanical Losses These losses consist of bearing frictional and windage loss.

In a medium-size motor, armature copper losses are about 30% to 40% of the total full load losses and field copper losses are about 20% to 30% of total full load losses. Iron losses are about 20% and mechanical losses are about 5 to 10% of the total full load losses. For small motors mechanical losses are comparable with full load losses while for larger motors, mechanical losses may be neglected.

Iron losses and mechanical losses are constant for a particular machine and they are together known as *no load rotational losses.*

Besides the above three types of losses there is an additional loss known as stray load loss. All the losses which do not belong to any of the above categories may be included in this group. In most machines stray load loss is taken as 1% of the rated output of the machine and is usually neglected.

Efficiency of dc Machines

$$\text{Efficiency } \eta = 1 - \frac{\text{Losses}}{\text{Input}} \quad \left[\because \eta = \frac{\text{Output}}{\text{Input}} = \frac{\text{Input} - \text{Losses}}{\text{Input}}\right]$$

For a generator, $\eta_g = 1 - \dfrac{\text{losses}}{VI_L + \text{losses}}$, where V is the terminal voltage and I_L is the line current; $V I_L$ is the output power.

For a motor, $\eta_m = 1 - \dfrac{\text{losses}}{V I_L}$; here VI_L is the input power. η may also be expressed in %, if multiplied by 100.

Condition for Maximum Efficiency for a dc Generator

$$\eta_g = \frac{V I_L}{V I_L + I_a^2 r_a + V_f I_f + W_o}$$

Now, $V_f I_f + W_o$ = constant (= C) and as (I_f) is negligible so $I_L = I_a$.

Here, $V I_L$ = output power

$I_a^2 r_a$ = armature copper loss

$V_f I_f$ = shunt field copper loss

W_o = No load rotational loss.

So, $$\eta_g = \frac{V I_L}{V I_L + I_L^2 r_a + C}.$$

Maximum efficiency occurs when

$$\frac{d\eta_g}{dI_L} = \frac{(V I_L + I_L^2 r_a + C) V - V I_L (V + 2 I_L r_a)}{(V I_L + I_L^2 r_a + C)^2} = 0$$

or $$V I_L + I_L^2 r_a + C = V I_L + 2 I_L^2 r_a$$

or $$C = I_L^2 r_a .$$

Hence, constant loss = variable armature circuit loss. Hence a generator has maximum efficiency when variable loss equals constant loss.

The load current at maximum efficiency is given by

$$I_L = \sqrt{\frac{\text{constant loss}}{r_a}} .$$

2.26 A 480 V, 20 kW shunt motor takes 2.5 A when running at no load. Taking the armature resistance to be 0.6 Ω, field resistance to be 800 Ω and brush drop 2 V, find the full load efficiency.

Solution

Here, $V = 480$ V, $P = 20 \times 10^3$ W, $I_L = 2.5$ A (no load), $r_a = 0.6$ A, $r_{sh} = 800\ \Omega$

$$\therefore \qquad I_{sh} = \frac{V}{r_{sh}} = \frac{480}{800} = 0.6 \text{ A}$$

Input power at no load = VI_L (no load) = $480 \times 2.5 = 1200$ W

Field copper loss = $I_{sh}^2 r_{sh} = (0.6)^2 \times 800 = 288$ W.

Armature current (no load)

$$I_a = I_L - I_{sh} = 2.5 - 0.6 = 1.9 \text{ A}.$$

Armature copper loss (no load) = $I_a^2 r_a = (1.9)^2 \times 0.6 = 2.166$ W

Brush contact loss = $2 \times I_a = 3.8$ W

So, (Core loss + Frictional losses) = $1200 - 288 - 2.166 - 3.8 = 906.034$ W

Under full load condition,

$$I_L = \frac{20 \times 10^3}{480} = 41.67 \text{ A}$$

$$\therefore \qquad I_a = I_L \text{ (full load)} - I_{sh} = 41.67 - 0.6 = 41.07 \text{ A}$$

Armature copper loss at full load = $(41.07)^2 \times 0.6 = 1012.05$ W

Total losses = $1012.05 + 288 + 906.034 + 2 \times 41.07 = 2288.22$ W

Hence, full load efficiency $= \dfrac{\text{Input} - \text{Loss}}{\text{Input}}$

$$= 1 - \frac{\text{Loss}}{\text{Input}} = 1 - \frac{2288.22}{20{,}000} = 0.8855 \text{ or, } 88.55\%.$$

2.27 A 100 kW, 220V dc shunt generator has the following data:

Armature resistance = 0.1 Ω
Mechanical loss = 5 kW
Iron losses = 5 kW
Shunt field resistance = 220 Ω
Brush contact drop = 1 V per brush
Stray losses are 1% of output.

Find the efficiency at full load. Also find the input torque if the speed is 1000 rpm.

Solution

Given, Output = 100 W
Terminal voltage = 220 V

Line current $I_L = \dfrac{100 \times 10^3}{220} = 454.54$ A

Field current $I_{sh} = \dfrac{220}{220} = 1$ A

Armature current $I_a = I_L + I_{sh} = 454.54 + 1 = 455.54$ A

Field copper loss

$$I_{sh}^2 r_{sh} = 1^2 \times 220 = 220 \text{ W}$$

Armature copper loss

$$I_a^2 r_a = (455.54)^2 \times 0.1 = 20751.67 \text{ W}$$

Brush contact loss = $1 \times 2 \times 455.54 = 911.08$ W

Mechanical loss = 5000 W.

Iron loss = 5000 W

Stray losses = $0.01 \times 100 \times 10^3 = 1000$ W

Total loss = 220 + 20751.67 + 911.08 + 5000 + 5000 + 1000
= 32882.75 W = 32.88 kW

Input power = Output + Loss = (100 + 32.88) kW = 132.88 kW

$$\therefore \quad \text{Efficiency} = \frac{\text{Output}}{\text{Input}} \times 100\% = \frac{100}{132.88} \times 100\% = 75.25\%$$

Speed = 1000 rpm

$$\because \quad \text{Angular velocity } \omega = \frac{2\pi \times 1000}{60} \text{ rad/s} = 104.67 \text{ rad/s}$$

$$\text{Input torque} = \frac{\text{Input power}}{\omega} = \frac{132.88 \times 10^3}{104.67} \text{ Nm} = 1269.51 \text{ Nm.}$$

2.28 A 400 V shunt motor with armature and field resistance of 0.1 Ω and 200 Ω takes no load current of 10 A at 1500 rpm. If full load current is 100 A find the speed and output torque at full load. Assume that the mechanical losses are same at no load and full load.

Solution

Given, $V = 400$ V, $r_a = 0.1$ Ω, $r_{sh} = 200$ Ω

At no load

$I_{L_1} = 10$ A

$N_1 = 1500$ rpm

$$I_{sh} = \frac{V}{r_{sh}} = \frac{400}{200} = 2 \text{ A}$$

$$\therefore \quad I_{a_1} = I_{L_1} - I_{sh} = 10 - 2 = 8 \text{ A}$$

Armature copper loss = $(8)^2 \times 0.1 = 6.4$ W [at no load]

Back emf $E_{b_1} = V - I_{a_1} r_a = 400 - 8 \times 0.1 = 399.2$ V

Input power at no load = $400 \times 10 = 4000$ W (= total loss)

So, constant losses (i.e mechanical loss + core loss + shunt field copper loss) = 4000 – 6.4 = 3993.6 W

At full load,

$I_{L_2} = 100$ A

Hence, $I_{a_2} = 100 - 2 = 98$ A

Armature copper loss is $(98)^2 \times 0.1 = 960.4$ W (at full load)

Back emf $(E_{b_2}) = 400 - 98 \times 0.1 = 390.2$ W

If N_2 be the speed at full load

$$\frac{E_{b_1}}{E_{b_2}} = \frac{N_1}{N_2}$$

or $$N_2 = \frac{E_{b_2}}{E_{b_1}} N_1 = \frac{390.2}{399.2} \times 1500 = 1466 \text{ rpm}$$

Input power at full load = $100 \times 400 = 40000$ W

$\therefore$ Total loss = 3993.6 + 960.4 = 4954 W (at full load)

Output power = Input power – Loss = 40,000 – 4954 = 35046 W (at full load)

Angular velocity $\omega = \frac{2\pi N_2}{60} = \frac{2\pi \times 1466}{60}$ rad/s = 153.44 rad/s

Output torque at full load = $\frac{35046}{153.44}$ Nm = 228.4 Nm

$\left[\because \quad T_{\text{output}} = \frac{P(\text{output})}{\omega}\right]$.

2.29 A 400 V dc shunt motor runs at 1000 rpm and takes an input of 1500 W under no load condition. The armature and shunt field resistance are 0.3 Ω and 200 Ω respectively. Find the efficiency when the machine is used as a generator supplying 100 A at 400 V.

Solution

For motor at no load,

Input power = 1500 W

Line current = $\frac{1500}{400}$ = 3.75 A [no load]

Shunt field current = $\frac{400}{200}$ = 2 A

Hence, armature current I_a = 3.75 – 2 = 1.75 A,

Armature copper loss = $(1.75)^2 \times 0.3$ = 0.9187 W [no load]

Constant loss = Mechanical loss + core loss + Shunt field copper loss

= 1500 – 0.9187 = 1499.08 W

For generator, output = 100 × 400 = 40,000 W

Line current = 100 A

Armature current = 100 + 2 = 102 A

Armature copper loss = $(102)^2 \times 0.3$ = 3121.2 W

So, total loss= 3121.2 + 1499.08 = 4620.28 W

Efficiency = $\frac{\text{Output}}{\text{Output + Loss}} = \frac{40{,}000}{40{,}000 + 4620.28} = \times 100\% = 89.65\%$.

2.30 A 200 V dc shunt generator runs at 1000 rpm at no load taking an input of 700 W. The armature resistance is 0.2 Ω and the shunt field current is 2A. Find the line current at which maximum efficiency occurs. Also find the value of maximum efficiency.

Solution

At no load, Input power = 700 W

Line current = $\frac{700}{200}$ = 3.5 A (no load).

Shunt field current = 2 A.

Hence, armature current at no load = 3.5 + 2 = 5.5 A

Armature copper loss at no load = $(5.5)^2 \times 0.2$ = 6.05 W

Constant loss = 700 – 6.05 = 693.95 W.

Maximum efficiency occurs when constant loss = variable loss.

In shunt machines variable loss is the armature copper loss.

If I_a be the armature current at which maximum efficiency occurs, then

$$I_a^2 \times 0.2 = 693.95$$

or $$I_a = \sqrt{\frac{693.05}{0.2}} = 58.9 \text{ A}$$

$\therefore$ The line current at which maximum efficiency occurs is (58.9 – 2) = 56.9 A.
Output power = 56.90 × 200 = 11380 W;
Total losses = 693.95 × 2 = 1387.9 W ($\because$ constant loss = variable loss
hence total loss = 2 × constant loss)

$$\therefore \text{ Efficiency} = \frac{11380}{11380+1387.9} \times 100\% = 89.13\%.$$

2.31 A 1500 kW, 550 V, 16-pole series generator runs at 150 rpm. What must be the useful flux per pole if there are 2500 lap connected armature conductors and full load copper losses are 25 kW?

Solution

In a series generator,

Line current = Armature current

Hence, $$I_a = \frac{1500 \times 10^3}{550} \text{ A} = 2727.27 \text{ A}$$

Now, copper loss = $I_a^2 r_a = 25 \times 10^3$ W

$$\therefore \quad r_a = \frac{25 \times 10^3}{(2727.27)^2} = 0.00336\ \Omega$$

Generated emf $E = V + I_a r_a = 550 + 2727.27 \times 0.00336 = 559.167$ V.
If ϕ be the flux per pole, we can write

$$559.167 = \frac{P\phi ZN}{60\text{ A}} = \frac{16\,\phi \times 2500 \times 150}{60 \times 16} = 6250\,\phi$$

$$\therefore \quad \phi = 0.08947 \text{ Wb.}$$

2.21 DC MOTOR STARTING

The armature current of a motor is given by

$$I_{as} = \frac{V - E_b}{R_a}$$

Thus, I_a depends upon E_b and R_a when V is kept constant. When a motor is first switched on, the armature is stationary so the back emf E_b is zero ($\because$ $E_b \propto$ speed).

The initial starting armature current I_a is given by

$$I_{as} = \frac{V - 0}{R_a} = \frac{V}{R_a}.$$

Since the armature resistance of a motor is very small, generally less than one ohm, therefore the starting armature current I_{as} would be very large. For example, if a motor with armature resistance of 0.2 Ω is connected directly to a 230 V supply, then

$$I_{as} = \frac{V}{R_a} = \frac{230}{0.2} = 1150 \text{ A}$$

This large current would damage the brushes, commutator, or windings. Also it may damage supply installation.

As the motor speed increases, the back emf increases and the difference ($V - E_b$) goes on decreasing. This results in the gradual decrease of I_{as} until the motor

attains its stable rated speed and the corresponding back emf. Under this condition the armature current reaches its desired rated value. Thus, it is found that the back emf helps the armature resistance in limiting the current through the armature.

Since the starting current is very large, at the time of starting of dc motors (except very small motor) an extra resistance must be connected in series with the armature. This would limit the initial current to a safe value until the motor has built up the stable speed and back emf E_b.

This external starting resistance is basically known as the *starter resistance.*

The series resistance is divided into sections which are cut out one by one as the speed of the motor increases and the back emf builds up. When the speed of the motor attains its normal value, the extra resistance is completely cut out.

2.21.1 Three-point Starter

A three-point starter connected to a dc shunt motor is shown in Fig. 2.33. As only three terminals, i.e. *L*, *A* and *F* are available from the starter it is called a three-point starter. The terminal *L* of the starter is connected to the supply terminal, *A* to the armature and *F* to the field terminal.

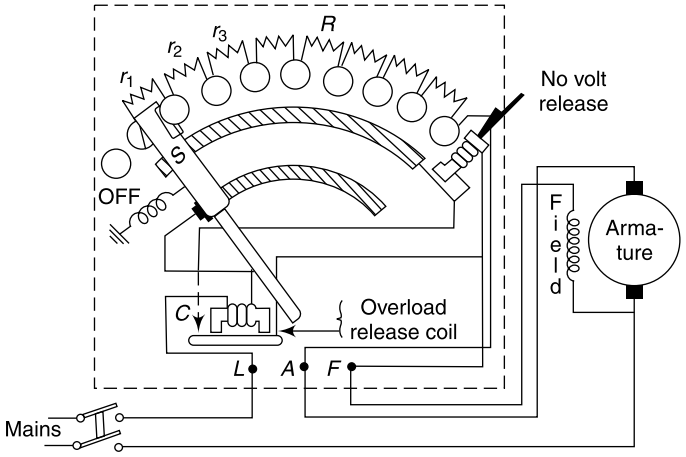


Fig. 2.33 ***Three-point starter for a dc shunt motor***

When the motor is at rest the starter handle *S* is kept in the "OFF" position by a spring and motor is disconnected from the supply. When the motor is to be started the handle is moved to stud 1. The shunt field and the holding coil gets the supply and entire starting resistance is connected in series with the armature. The armature starts rotating and the handle is gradually moved through all the studs until it touches the holding magnet. The holding magnet is called the *no volt release* or *low voltage release coil*. In case of power failure the holding coil gets demagnetized and the handle is brought back to "OFF" position by a spring action. Again, if by any chance the shunt field winding gets open circuited the holding magnet gets demagnetized and starter handle returns to the "OFF" position.

There is another coil called *overload release coil* which protects the motor against excessive load current. When armature current exceeds a particular value the overload release coil attracts the soft iron armature and as a result the no volt release coil gets short circuited. The starter is pulled back to the "OFF" position by the spring action as the holding coil gets demagnetized. The motor is thus automatically switched off.

2.22 REVERSAL OF ROTATION OF DC MOTOR

The direction of rotation of a dc motor can be reversed by reversing the connections of either the field winding or the armature but not both.

It is to be noted that in order to reverse the direction of rotation of a compound motor the reversal of the field connections involves both shunt and series windings.

2.23 DC MACHINE APPLICATIONS

Applications of a dc machine are discussed as follows.

2.23.1 Generator Applications

DC generaters are nowadays used in dynamometers (for measuring torque etc.), for welding purpose, as control type dc generator for closed loop systems, permanent magnet dc generators, etc. Separately excited dc generators are used (a) to serve as an excitation source for large alternators in power generating stations (b) to serve as control generator in Ward-Leonard system of speed control and (c) to serve as auxiliary and emergency power supplies.

2.23.2 Motor Applications

When constant speed service at low speed is required in industries shunt motors are used. When driven load requires a wide range of speed control dc shunt motor is used, e.g. in lathes.

Since series motor have high starting torque it is best suited for driving hoists, trains, cranes, etc. They are widely used in all types of electric vehicles, electric trains, street cars, battery powered portable tools, etc.

Compound motors are used in rolling mill drive, punching press, planning or miling machine. When the supply voltage across the motor terminals is likely to vary considerably such as in traction motors, compound motors are preferred.

As separately excited dc motors are easily adaptable to a wide range of speed and torque control, in high power applications these are widely used in steel and aluminium rolling mills and Ward Leonard method of speed control. In low power applications separately excited dc motor finds use as control motor.

ADDITIONAL EXAMPLES

2.32 A 4-pole dc armature wave winding has 294 conductors;
(i) What flux per pole is necessary to generate 230 V when rotating at 1500 rpm?
(ii) What is the electromagnetic torque at this flux when the rated armature current of 120 A is flowing?

Solution

Here, $P = 4$, $A = 2$ and $Z = 294$

(i) $E = 230$ V, $N = 1500$ rpm

$$E = \frac{P\phi ZN}{60\,\text{A}}$$

$$\text{or} \quad \phi = \frac{60\,AE}{PZN} = \frac{60 \times 2 \times 230}{4 \times 294 \times 1500} = 0.0156 \text{ Wb.}$$

(ii) $I_a = 120$ A

$$T_e = K\phi I_a = \frac{PZ}{2\pi A}\,\phi\, I_a = \frac{4 \times 294}{2\pi \times 2} \times 0.0156 \times 120 \text{ Nm} = 175.276 \text{ Nm.}$$

2.33 A dc machine is generating 125 V while delivering 8 A to a load. If its armature circuit resistance is 1.35 Ω, what voltage must be generated internally in the armature?

Solution

Here, $V = 125$ V, $I_L = 8$ A, $r_a = 1.35\ \Omega$

$\therefore$ $E = V + I_a r_a = 125 + 8 \times 1.35 = (125 + 10.8)\text{V} = 135.8$ V.

2.34 A shunt motor has a rated armature current 50A when connected to 200 V. The rated speed is 1000 rpm and armature resistance is 0.1 Ω. Find the speed if total torque is reduced to 70% of that at rated load and a 3Ω resistance is inserted in series with the armature.

Solution

Given, $I_{a_1} = 50$ A, $V = 200$ V, $N_1 = 1000$ rpm,
$r_a = 0.1\ \Omega$, $T_{e2} = 0.7\ T_{e1}$

As $T_e \propto \phi\, I_a$

So $I_{a_2} = 0.7\ I_{a1}$ (ϕ = constant for shunt motor)

or $I_{a_2} = 0.7 \times 50 = 35$ A

$E_{b_1} = V - I_{a1}\, r_a = 200 - 50 \times 0.1 = 195$ V

$E_{b_2} = V - I_{a2}(r_a + 3) = 200 - 35(0.1 + 3) = 200 - 35 \times 3.1 = 91.5$ V

Since $\frac{E_{b_1}}{E_{b_2}} = \frac{N_1}{N_2}$ (As ϕ = constant)

So $N_2 = \frac{E_{b_2}}{E_{b_1}} N_1 = \frac{91.5}{195} \times 1000 = 469$ rpm.

2.35 A dc series motor drives a load whose torque varies as cube of the speed. The armature and series field resistance together is 2 Ω. The line current is 10 A when connected to a 400 V supply and the speed is 1500 rpm. Find the resistance to be connected in series with the armature to reduce the speed to 1000 rpm.

Solution

$$T_e \propto I_a^2 \text{ (in series motor)}$$

Here, $T_e \propto N^3$. So, $I_a^2 \propto N^3$

Also, $r_a + r_{se} = 2\ \Omega$

$I_{L1} = 10$ A $= (I_{a1})$, $V = 400$ V and $N_1 = 1500$ rpm

When resistance R is connected in series with armature, let speed $N_2 = 1000$ rpm and armature current is I_{a2}

$$\frac{I_{a1}^2}{I_{a2}^2} = \frac{N_1^3}{N_2^3} = \frac{(1500)^3}{(1000)^3}$$

or $$I_{a2} = \left(\frac{1000}{1500}\right)^3 \times (10)^2$$

$\therefore$ $$I_{a2}^2 = 5.44 \text{ A}$$

$$E_{b_2} = V - I_{a_2}(r_a + r_{se} + R) = 400 - 5.44\ (2 + R)$$

Now, $$E_{b_1} = V - I_{a_1}(r_a + r_{se}) = 400 - 10 \times 2 = 380 \text{ V}$$

Again $$\frac{E_{b_1}}{E_{b_2}} = \frac{I_{a_1} N_1}{I_{a_2} N_2} \quad \text{(for series motor)}$$

Here, $$E_{b_2} = \frac{I_{a_2} N_2}{I_{a_1} N_1} \times 380 = \frac{5.44 \times 1000}{10 \times 1500} \times 380 = 137.897 \text{ V}$$

$\therefore$ $400 - 5.44(2 + R) = 137.897$

or $R = 46.18\ \Omega$.

2.36 A 50 kW, 400 V dc shunt generator has field and armature resistance of 200 Ω and 0.1 Ω respectively. The full load speed is 1000 rpm. Find the speed of the machine when running as a motor and taking 50 kW from a 400 V supply. Assume brush contact drop of 1 V per brush.

Solution

Here, $r_{sh} = 200\ \Omega$ and $r_a = 0.1\ \Omega$

For dc shunt generator

$$I_{sh} = (V/R_{sh}) = \frac{400}{200} \text{A} = 2\text{A}$$

$$I_L = \frac{\text{Power output}}{\text{Terminal voltage}} = \frac{50 \times 10^3}{400} = 125 \text{ A}.$$

$\therefore$ $$I_a = (I_L + I_{sh}) = (125 + 2) \text{ A} = 127 \text{ A}$$

$$E_g = V + I_a r_a = 400 + 127 \times 0.1 = 412.7 \text{ V}.$$

Similarly, for a dc shunt motor,

$$I_L = \frac{50 \times 10^3}{400} \text{A} = 125 \text{ A}$$

$$I_{sh} = \frac{400}{200} \text{A} = 2 \text{ A}, \ I_a = (125 - 2)\text{A} = 123 \text{ A}$$

$\therefore$ $$E_b = V - I_a r_a = 400 - 123 \times 0.1 = 387.7 \text{ V}.$$

If speed of the motor is N_2 then comparing the two cases of operation we have

$$\frac{E_g}{E_b} = \frac{1000}{N_2}$$

or $$N_2 = 1000 \times \frac{387.7}{412.7} = 939 \text{ rpm.}$$

2.37 A dc motor takes an armature current of 100 A at 230 V. The armature resistance is 0.03 Ω. The total number of lap connected armature conductors is 500 and the number of poles is 4. The flux per pole is 0.03 Wb. Find the speed and torque.

Solution

Here, $I_a = 100$ A, $V = 230$ V, $r_a = 0.03$ Ω

$A = P = 4$, $Z = 500$ and $\phi = 0.03$ Wb

$\therefore$ $E_b = V - I_a r_a = 230 - 100 \times 0.03 = 227$ V

Also, $$E_b = \frac{P\phi ZN}{60\,A}$$

or $$N = \frac{60\,AE_b}{P\phi Z} = \frac{60 \times 227}{0.03 \times 500} = 908 \text{ rpm} \quad (\because A = P)$$

$\therefore$ $$T_e = \frac{E_b I_a}{\omega} = \frac{227 \times 100}{\frac{2\pi \times 908}{60}} = 238.85 \text{ Nm.}$$

2.38 A 50 kW belt driven shunt generator is running at 300 rpm and delivers rated load to a 250 V bus bar. The armature and shunt field resistances are 0.025 Ω and 50 Ω respectively. Suddenly the belt breaks and the machine continues to run as a motor taking 5 kW from bus bars. Find the speed of the motor allowing brush drop of 1 V per brush.

Solution

When the machine acts as a generator, we have

$P = 50{,}000$ W, $N_1 = 300$ rpm, $V = 250$ V, $r_a = 0.025$ Ω and $r_{sh} = 50$ Ω.

$\therefore$ $$I_L = \frac{P}{V} = \frac{50000}{250}\text{A} = 200 \text{ A}$$

$$I_{sh} = \frac{V}{r_{sh}} = \frac{250}{50}\text{A} = 5 \text{ A}$$

$$I_a = (I_L + I_{sh}) = (200 + 5)\text{A} = 205 \text{ A}$$

$$E_1 = V + I_a r_a + 2 \times 1 = (250 + 205 \times 0.025 + 2)$$

$$E_1 = 257.125 \text{ V.}$$

When the machine acts as a motor, we have

$$I_L = \frac{5000}{250}\text{A} = 20 \text{ A}$$

$$I_a = (20 - 5) \text{ A} = 15 \text{ A}$$

$$E_2 = 250 - 15 \times 0.025 - 2 = 247.625 \text{ V.}$$

If N_2 be the speed of the motor

$$N_2 = \frac{E_2}{E_1} N_1 = \frac{247.625}{257.125} \times 300 \text{ rpm} = 289 \text{ rpm.}$$

2.39 A 600 V dc motor drives a 60 kW load 700 rpm. The shunt field resistance is 100 Ω and armature resistance is 0.16 Ω. If the motor efficiency is 85%, calculate the speed at no load and speed regulation.

Solution

Output = 60000 W, V = 600, N_1 = 700 rpm, r_{sh} = 100 Ω,
r_a = 0.16 Ω, η = 0.85.

$$\text{Input power} = \frac{\text{Output power}}{\text{Efficiency}} = \frac{60000}{0.85} = 70588 \text{ W}$$

$$\therefore \quad I_L = \frac{\text{Input power}}{\text{Terminal voltage}} = \frac{70588}{600} = 117.65 \text{ A};$$

$$I_{sh} = \frac{V}{r_{sh}} = \frac{600}{100} \text{A} = 6 \text{ A}$$

$$I_a = I_L - I_{sh} \text{ (for motor)} = 117.65 - 6 = 111.65 \text{ A}$$

Also, $E_{b_1} = V - I_a r_a = 600 - 111.65 \times 0.16 = 582.136$ V

At no load,

$$E_{b_2} = V = 600 \text{ V}$$

It no load speed is N_2 then

$$N_2 = N_1 \frac{E_{b_2}}{E_{b_1}} = 700 \times \frac{600}{582.136} \text{ rpm} = 721 \text{ rpm}.$$

$$\text{Speed regulation} = \frac{721 - 700}{700} \times 100\% = 3\%.$$

2.40 A 200 V shunt motor has r_a = 0.1 Ω, r_{sh} = 240 Ω and rotational loss is 236 W. On full load the line current is 9.8 A with the motor running at 1450 rpm. Find (i) the mechanical power developed (ii) power output (iii) load torque and (iv) full load efficiency.

Solution

Here, V = 200 V, r_a = 0.1 Ω, r_{sh} = 240 Ω, I_{fl} = 9.8 A
N_{fl} = 1450 rpm. Rotational loss = 236 W

$$\therefore \quad I_{sh} = \frac{V}{r_{sh}} = \frac{200}{240} = 0.833 \text{ A}$$

and $I_a = (I_{fl} - I_{sh}) = 9.8 - 0.833 = 8.97$ A

Also, $E_b = V - I_a r_a = 200 - 8.97 \times 0.1 = 199$ V

(i) Mechanical power developed is $E_b I_a = 199 \times 8.97 = 1785$ W = 1.785 kW.

(ii) Power output = 1785.9 – 236 1549 W = 1.55 kW.

(iii) $$\text{Load torque} = \frac{\text{Power output}}{\omega} = \frac{1549 \times 60}{2\pi \times 1450} = 10.2 \text{ Nm}.$$

(iv) $$\text{Full load efficiency} = \frac{\text{Output}}{\text{Input}} = \frac{1549}{200 \times 9.8} = 0.791 = 79.1\%.$$

2.41 A dc series motor runs at 1500 rpm and takes 100 A from 400 V supply. The combined resistance of the armature and field is 0.5 Ω. If an additional resistance of 5 Ω is inserted in series with the armature circuit, find the motor speed if the electromagnetic torque is proportional to the square of the speed.

Solution

N = 1500 rpm; $I_a = I_L$ = 100 A; V = 400 V;

$(r_a + r_{se})$ = 0.5 Ω

$T_e \propto \phi I_a$

As $\phi \propto I_a$,

$T_e \propto I_a^2$

Again $T_e \propto N^2$

Hence, $I_a \propto N$

$\therefore$ $I_a = KN$ (K being a consant)

or, $$K = \frac{100}{1500} = \frac{1}{15}$$

Now, $E_{b_1} = V - I_a(r_a + r_{se}) = 400 - 100 \times 0.5 = 350$ V

and $E_{b_2} = V - I_{a2}(r_a + r_{se} + 5) = 400 - I_{a2}(5.5)$

If the speed is N when 5 Ω resistor is connected, then we can write

$$\frac{E_{b_1}}{E_{b_2}} = \frac{N_1}{N_2} \quad \text{or,} \quad \frac{350}{400 - 5.5I_{a2}} = \frac{1500}{N} \qquad \begin{bmatrix} N_1 = \text{initial speed} \\ = 1500 \text{ rpm} \\ N_2 \equiv N \end{bmatrix}$$

or, $350\,N = 600{,}000 - 5.5 \times K \times N \times 1500$.

or, $N \quad 667$ rpm.

2.42 A dc shunt motor runs at 750 rpm from 250 V supply and takes a full load line current of 60 A. Its armature and field resistances are 0.4 Ω and 125 Ω respectively. Assuming 2 V brush drop calculate no load speed for a no load line current of 6 A and the resistance to be added series with the armature circuit to reduce the full load speed to 600 rpm.

Solution

Given, N_{fl} = 750 rpm; V = 250 V; I_{fl} = 60 A

r_a = 0.4 Ω, r_{sh} = 125 Ω

I_{nl} = 6 A

$$I_{a\text{fl}} = 60 - \frac{250}{125} = 58 \text{ A} \quad \left[\because I_{afl} = \left(I_{fl} - \frac{V}{r_{\text{sh}}}\right)\right]$$

$E_{b\text{fl}} = 250 - 58 \times 0.4 - 2 = 224.8$ V $[\because E_{bfl} = V - I_{afl} \times r_a]$

$$I_{anl} = 6 - \frac{250}{125} = 4 \text{ A} \quad \left[\because I_{anl} = I_{nl} - I_{\text{sh}} = I_{nl} - \frac{V}{r_{\text{sh}}}\right]$$

$E_{bnl} = 250 - 4 \times 0.4 - 2 = 246.4$ V $[\because E_{bnl} = V - I_{anl} \times r_a - \text{brush drop}]$

[Suffix *nl* stands for no load parameters while suffix *fl* stands for full load parameters]

If N be the no load speed then we have

$$N = N_{\text{fl}} \times \frac{E_{bnl}}{E_{bfl}} = 750 \times \frac{246.4}{224.8} = 822 \text{ rpm}$$

If R be the resistance connected in series with the armature circuit then we can write,

$$E_b = [250 - I_a(0.4 + R) - 2] \text{ and } N' = 600 \text{ rpm}$$

or $$E_b = [248 - 60(0.4 + R)] = 224 - 60\,R.$$

$$\therefore \quad \frac{224 - 60R}{246.4} = \frac{600}{822} \quad \left[\because \frac{E_b}{E_{bnl}} = \frac{N'}{N}\right]$$

or $$224 - 60\,R = 179.85$$

or $$R = 0.736\ \Omega.$$

2.43 A 25 H.P., 240 V, 1000 rpm, 4-pole dc shunt motor has 1000 conductors arranged in 2 parallel paths. The armature circuit resistance is 0.3 Ω, field current and line current are 2 A and 100 A respectively. Find (i) flux per pole, (ii) torque developed, (iii) rotational losses, (iv) total losses expressing as a percentage of power.

Solution

Output power $P = 25$ H.P. $= 25 \times 735.5$ W $= 18387.5$ W

$V = 240$ V, $N = 1000$ rpm, $P = 4$, $Z = 1000$,

$A = 2$, $r_a = 0.3\ \Omega$, $I_{sh} = 2$ A, $I_L = 100$ A,

$I_a = I_L - I_{sh} = 100 - 2 = 98$ A

and $E_b = V - I_a\, r_a = 240 - 98 \times 0.3 = 210.6$ V

(i) Also $E_b = \dfrac{P\phi ZN}{60\,A}$ where ϕ = flux per pole

$$\text{or } \phi = \frac{60\,AE_b}{PZN} = \frac{60 \times 2 \times 210.6}{4 \times 1000 \times 1000} = 0.0063 \text{ Wb.}$$

(ii) $T_e = \dfrac{P\phi ZI_a}{2\pi A}$ Nm $= \dfrac{4 \times 0.0063 \times 1000 \times 98}{2\pi \times 2} = 196.62$ Nm.

(iii) Power developed by the motor $(= E_b\, I_a) = 210.6 \times 98 = 20638.8$ W

Rotational losses $= E_bI_a$ – output power $= 20638.8 - 18387.5 = 2251.3$ W

(iv) Armature copper loss $(= I_a^2\, r_a) = (98)^2 \times 0.3 = 2881.2$ W

Field copper loss $(= V\, I_{sh}) = 240 \times 2 = 480$ W

Total losses $= (2881.2 + 480 + 2251.3)$W $= 5612.5$ W

$$\therefore \quad \% \text{ loss} = \frac{5612.5}{18387.5} \times 100\% = 30.52\%.$$

2.44 A 220 V shunt motor takes 10.25 A on full load. The armature resistance is 0.8 Ω and the field resistance is 880 Ω. The losses due to friction, windage and the iron amount to 150 W. Find the output power and the efficiency of the motor on full load.

Solution

Motor input on full load $= 220 \times 10.25 = 2255$ W

Field current $= \dfrac{220}{880} = 0.25$ A

Armature current $= 10.25$ A $- 0.25$ A $= 10$ A

Armature copper loss $= (10)^2 \times 0.8 = 80$ W

Field copper loss $= (0.25)^2 \times 880 = 55$ W

Total loss = total copper loss + friction, windage and iron loss

$= (80 + 55 + 150) = 285$ W

Output power = Input – Loss = 2255 – 285 = 1970 W

$$\text{Efficiency} = \frac{\text{Output}}{\text{Input}} \times 100\% = \frac{1970}{2255} \times 100\% = 87.36\%.$$

2.45 A dc shunt motor has an armature resistance of 0.9 Ω and takes an armature current of 18A from 230 V dc mains. Calculate the power output and overall efficiency of the motor if the rotational losses are measured to be 112 W and the shunt field resistance is 300 Ω.

Solution

Armature current = 18 A

$$\text{Field current} = \frac{230}{300} = 0.767 \text{ A}$$

Line current = 18.767 A

Armature copper loss = $(18)^2 \times 0.9 = 291.6$ W

Field copper loss = $(0.767)^2 \times 300 = 176.48$ W

Total losses = 291.6 + 176.48 + 112 = 580.08 W

Output power = Input power – Loss = $18.767 \times 230 - 580.08 = 3736.33$ W = 3.74 kW.

$$\text{Overall efficiency} = \frac{\text{Output}}{\text{Input}} \times 100\% = \frac{3736.33}{18.767 \times 230} \times 100\% = 86.56\%.$$

2.46 A dc shunt motor running at 1200 rpm has armature resistance of 0.15 Ω. The current taken by the armature is 60 A when the applied voltage is 220 V. If the load is increased by 30% find the variation in the speed.

Solution

Given $r_a = 0.15$ Ω

When speed $N_1 = 1200$ rpm the back emf is

$$E_{b_1} = 220 - 60 \times 0.15 = 211 \text{ V}.$$

Let the output power be P_1.

If the load is increased by 30% the output power $P_2 = 1.3\ P_1$ and let the back emf and speed be E_{b_2} and N_2 respectively

We have, $E_{b_2}\ I_{a_2} = 1.3\ E_{b_1}\ I_{a_1} = 1.3 \times 211 \times 60 = 16458$ W

Now $$E_{b_2} = 220 - I_{a2} \times 0.15 = 220 - 0.15 \times \frac{16458}{E_{b_2}}$$

or $$E_{b2}^2 = 220\ E_{b_2} - 2468.7 \text{ or } E_{b2}^2 - 220\ E_{b_2} + 2468.7 = 0$$

or $$E_{b_2} = \frac{220 \pm \sqrt{48400 - 9874.8}}{2} = \frac{220 \pm 196}{2}$$

or $$E_{b_2} = 208.14 \text{ V}.$$

$$\text{Speed} = \frac{208.14}{211} \times 1200 = 1184 \text{ rpm}.$$

2.47 A 230 V, 10 kW shunt motor with a stated full load efficiency of 85% runs at a speed of 1000 rpm. At what speed should the motor be driven if it is used as a generator to supply an emergency lighting load at 230 V? The armature resistance is 0.2 Ω and the field resistance is 115 Ω. Find the kW rating of the machine under this condition. Assume that the line current is same in both the cases.

Solution

$$\text{Output} = 10 \text{ kW} = 10{,}000 \text{ W}$$

$$\text{Input} = \frac{10000}{0.85} = 11764.7 \text{ W}$$

$$\text{Shunt field current} = \frac{230}{115} \text{A} = 2\text{A} \ (= I_{\text{sh}}).$$

$$\text{Full load line current} = \frac{11764.7}{230} \text{A} = 51.15 \text{ A} \ (= I_{fl}).$$

When the machine runs as a motor

Armature current $[(I_{a(m)}) = I_{fl} - I_{\text{sh}})] = 51.15 - 2 = 49.15$ A

Back emf $[(E_{b(m)}) = V - I_{a(m)} \times r_a] = 230 - 49.15 \times 0.2 = 220.17$ V

When used as a generator,

Armature current $[I_{a(g)} = I_{fl} + I_{\text{sh}}] = 51.15 + 2 = 53.15$ A

Generated emf $[E_{b(g)} = V + I_{a(g)} \times r_a] = 230 + 53.15 \times 0.2 = 240.63$ V.

If N_g be the speed of the generator then

$$N_g = 1000 \times \frac{240.63}{220.17} = 1093 \text{ rpm} \left[\because \frac{N_g}{N_m} = \frac{E_{b(g)}}{E_{b(m)}}\right]$$

Rating of the machine $(V \times I_{fl} \times 10^{-3}) = \frac{230 \times 51.15}{1000}$ kW = 11.76 kW.

EXERCISES

Short- and Long-Answer-Type Questions

1. Draw a neat sketch of a dc machine showing different parts. State the function of each part.
2. Derive the emf equation of a dc generator.
3. What are the different types of dc generators according to the ways in which fields are excited. Show the connection diagram of each type.
4. Distinguish between
   (i) self-excited and separately excited dc machines
   (ii) lap connected and wave connected dc machines
   (iii) cumulatively wound and differentially wound dc machines.
   (iv) long shunt and short shunt dc machines.
5. What is armature reaction? Describe the effects of armature reaction on the operation of dc machines. How is the armature reaction minimised?
6. What is commutation in a dc machine? Describe the various methods of improving commutation.
7. Describe the process of voltage build up in a self-excited dc machine. What are the conditions for voltage build up in a dc machine?
8. Draw the external characteristics of various types of dc generators.
9. What is meant by back emf? Explain the principle of torque production in a dc motor.
10. Derive the equation of torque for a dc motor.
11. Describe in details the methods of speed control of dc shunt motor.

12. What is the necessity of a starter in a dc motor? Explain with the help of a neat sketch the principle of operation of a three-point starter. What are the functions of no volt and overload release coils?
13. Draw and explain the speed current, torque current and speed torque characteristics of (i) a dc shunt motor (ii) a dc series motor.
14. What are the losses that occurs in dc machines? Derive the condition for maximum efficiency in a dc generator.
15. A 4-pole dc generator has 51 slots and each slot contains 20 conductors. The machine has a useful flux of 0.007 Wb and runs at 1500 rpm. Find the induced emf if the machine is wave wound. [*Ans.* 357 V]
16. A dc generator has an armature emf of 100 V when the useful flux per pole is 20 m Wb and the speed is 800 rpm. Calculate the generated emf with the same flux and a speed of 1000 rpm. [*Ans.* 125 V]
17. A short shunt compound dc generator delivers 100 A to a load at 250 V. The generator has shunt field, series field and armature resistance of 130 Ω, 0.1 Ω and 0.1 Ω respectively. Calculate the generated voltage. Assume 1 V drop per brush. [*Ans.* 272.2 V]
18. The armature of an 8-pole dc machine has a wave winding containing 664 conductors. Calculate the generated emf when the flux per pole is 0.08 Wb and the speed is 210 rpm. At what speed should the armature be driven to generate 500 V, if the flux per pole is made 0.06 Wb?
[*Ans.* 743.7 V, 188 rpm]
19. A 4-pole, 220 V, dc shunt generator has an armature resistance of 1 Ω, shunt field resistance of 220 Ω. The generator supplies power to a 10 Ω resistor. Calculate the generated emf of the generator if the load voltage is to be maintained at 220 V. Assume brush contact drop = 2 V.
[*Ans.* 245 V]

[*Hint:* Generated emf, $E = 220 + I_a r_a + 2$

$$I_L = \frac{220}{10}\text{ A} = 22\text{ A}$$

$$I_{sh} = \frac{220}{220}\text{ A} = 1\text{ A}$$

$$I_a = 22 + 1 = 23\text{ A}$$

$\therefore$ $E = 220 + 23 \times 1 + 2 = 245\text{ V}$]

20. A 4 pole, 220 V, dc shunt motor has armature and shunt field resistances of 0.2 Ω and 220 Ω respectively. It takes 20 A at 220 V from a source while running at a speed of 1000 rpm. Find the (i) field current, (ii) armature current (iii) back emf (iv) torque developed.
[*Ans.* 1 A; 19 A; 216.2 V; 39.25 Nm]

[*Hint:* (i) Field current $I_{sh} = \frac{220}{220}\text{ A} = 1\text{ A}$

(ii) Armature current $I_a = 20 - 1 = 19\text{ A}$

(iii) Back emf $E_b = 220 - 19 \times 0.2 = 216.2$ V

(iv) Torque $T = \dfrac{E_b I_a}{\omega} = \dfrac{216.2 \times 19}{\dfrac{2\pi \times 1000}{60}}$ Nm = 39.246 Nm]

21. A 400 V shunt generator has a full load current of 200 A, its armature resistance is 0.06 Ω and field resistance 100 Ω, the stray losses are 2000 Watts. Find the input H.P. of the generator. [*Ans.* 117.06 HP]
22. A 100 kW, 460 V shunt generator was run as a motor on no load at its rated voltage and speed. The total current drawn was 9.8 A including shunt current of 2.7 A. The resistance of the armature circuit was 0.11 Ω. Calculate the efficiencies (i) at full load and (ii) at half load.

[*Ans.* 91.3% and 89.7%]

23. A 220 V, dc shunt motor at no load takes a current of 2.5 A. The resistance of the armature and shunt field are 0.8 Ω and 200 Ω respectively. Estimate the efficiency of the motor when the input current is 20 A. [*Ans.* 81%]
24. A shunt motor runs at 500 rpm on a 200 V circuit. Its armature resistance is 0.5 Ω and the current taken is 30 A, in addition to field current. What resistance must be placed in series in order that the speed may be reduced to 300 rpm, the current in the armature remaining the same? [*Ans.* 2.466 Ω]
25. A 120 V dc shunt motor having an armature circuit resistance of 0.2 Ω and field circuit resistance of 60 Ω, draws a line current of 40 A at full load. The brush voltage drop is 3 V and rated full load speed is 1800 rpm. Calculate (i) the speed at half load (ii) the speed at 125% of full load.

[*Ans.* 1867 rpm, 1766 rpm]

[*Hint:* $I_L = 40$ A

$I_{sh} = \dfrac{120}{60}$ A = 2 A $\quad \therefore I_a = 40 - 2 = 38$ A

At full load $E_{b_1} = 120 - 38 \times 0.2 - 3 = 109.4$ V

(i) At half load $I_L = \dfrac{1}{2} \times 40$ A = 20 A and $I_a = 18$ A

$E_{b_2} = 120 - 18 \times 0.2 - 3 = 113.4$ V

Speed $N_2 = N_1 \dfrac{E_{b_2}}{E_{b_1}} = 1800 \times \dfrac{113.4}{109.4} = 1866$ rpm.

(ii) $I_L = 1.25 \times 40 = 50$ A and $I_a = 50 - 2 = 48$ A

$E_{b_3} = 120 - 48 \times 0.2 - 3 = 107.4$ V

$N_3 = 1800 \times \dfrac{107.4}{109.4} = 1767$ rpm].

26. A 4-pole 240 V dc shunt motor has armature and shunt field resistance of 0.24 Ω and 240 Ω respectively. It takes 20 A from a 240 V dc supply while running at a speed of 1000 rpm. Find the (i) field current, (ii) armature current, (iii) back emf and (iv) torque developed in Nm.

[*Ans.* 1 A; 19 A; 235.44 V; 42.74 Nm]

[*Hint:* (i) Field current, $I_{sh} = \frac{240}{240}$ A $= 1$ A

(ii) Armature current, $I_a = 20 - 1 = 19$ A

(iii) Back emf, $E_b = 240 - 19 \times 0.24 = 235.44$ V

(iv) Torque $T = \frac{E_b I_a}{\omega} = \frac{235.44 \times 19}{2\pi \times \frac{1000}{60}}$ Nm = 42.74 Nm]

27. A 220 V separately excited dc machine has an armature resistance of 0.4 Ω. If the load current is 20 A, find the induced emf when the machine operates (i) as a generator (ii) as a motor. [*Ans*. 228 V; 212 V]
[*Hint:* (i) $E = 220 + 20 \times 0.4 = 228$ V
(i) $E = 220 - 20 \times 0.4 = 212$ V]
28. Find no load and full load speeds of a 220 V, 4 pole shunt motor having following data:
Flux 0.04 m Wb, armature resistance 0.04 Ω, 160 armature conductors, wave connection, full load line current 95 A, no load line current 9 A, field resistance 44 Ω. [*Ans.* 1030.5 rpm, 1014.4 rpm]

MULTIPLE CHOICE QUESTIONS

1. The regulation of a separately excited dc shunt generator is approximately
(a) Zero
(b) infinity
(c) equal to the value of that for a dc series generator
(d) none of these
Answer: (a) Zero
2. If a dc series motor is started at no load, the speed will be
(a) rated value (b) too low
(c) too high (d) fluctuating
Answer: (c) too high
3. The speed of a dc shunt motor car be raised above its rated value by
(a) inserting a resistance in the connective circuit
(b) inserting a resistance in the field circuit
(c) applying a reduced voltage
(d) inserting a capacitor in the armature circuit
Answer: (b) inserting a resistance in the field circuit
4. The mechanical power developed by the armature of a dc motor is given by
(a) $E_b I_L$ (b) VI_L
(c) $E_b I_a$ (d) VI_d
Answer: (c) $E_b I_a$
5. The direction of EMF generated in a dc generator can be determined from
(a) Lenz's law
(b) Kirchhoff's Law
(c) Fleming's Left-hand rule

(d) Fleming's right-hand rule

Answer: (d) Fleming's right-hand rule

6. In a dc series motor the torque developed at 5 A is 15 Nm. If the hand current is doubled, the new torque is
   (a) 45 Nm (b) 15 Nm
   (c) 60 Nm (d) 30 Nm
   Answer: (c) 60 Nm
7. The output power is maximum for a dc motor when
   (a) $E_b = V/2$ (b) $E = 0.5\ I_a\ r_a$
   (c) $E_b = V$ (d) $E_b = I_a\ r_a$
   Answer: (a) $E_b = V/2$
8. The commutator of a dc machine acts as a
   (a) full wave rectifier (b) half wave rectifier
   (c) controlled full wave rectifier (d) none of these
   Answer: (a) full wave rectifier
9. The number of parallel paths in wave-connected armature winding of a dc machine is equal to
   (a) number of poles (b) half the number of poles
   (c) two (d) four
   Answer: (c) two
10. The dc motor needs a starter during starting to control
    (a) speed (b) current
    (c) voltage (d) flux
    Answer: (b) current
11. Direction of a dc shunt motor can be reversed by interchanging the
    (a) supply terminals
    (b) shunt field and armature terminals
    (c) shunt field or armature terminals
    (d) none of these
    Answer: (c) shunt field or armature terminals
12. In traction, the type of dc motor used is
    (a) shunt (b) separately excited
    (c) series
    Answer: (c) series

UNIVERSITY QUESTIONS WITH ANSWERS

Long-Answer Type Questions

1. (a) Deduce the emf equation of a dc generator. (WBUT 2013, 2014)
   Answer: Article 2.7

   (b) What do you mean by back emf?
   Answer: Article 2.13

   (c) A 4 pole 220 V, dc shunt motor has armature and shunt field resistances of 0.2 Ω and 220 Ω respectively. It takes 20 A at 220 V from a source while running at a speed of 1000 rpm. Find (i) field current, (ii) armature current, (iii) back of emf, and (iv) torque developed.
   (WBUT 2004)

Answer: Given, $V = 220$ V $\quad r_a = 0.2\ \Omega \quad r_{sh} = 220\ \Omega$
$I_L = 20$ A $\quad N = 1000$ rpm

(i) Field current $\frac{V}{r_{sh}} = \frac{220}{220} = 1$ A

(ii) Armature current $(I_a) = I_L - I_{sh} = 20 - 1 = 19$ A

(iii) Back emf $(E_b) = V - I_a r_a = 220 - 19 \times 0.2 = 216.2$ V

(iv) Torque developed $(T) = \frac{E_b l_a}{w} = \frac{216.2 \times 19}{2\pi \times \frac{1000}{60}} = 39.25$ Nm

2. (a) Deduce the e.m.f equation of a dc generator.

Answer: Article 2.7.

(b) A 120 V dc shunt motor having an armature circuit resistance of 0.2 Ω and field circuit resistance of 60 Ω, draws a line current of 40 A at full load. The brush voltage drop is 3 V and rated full load speed is 1800 rpm calculate. (WBUT 2005, 2014)

(i) the speed at half load

(ii) the speed at 125 % of full load.

Answer: Armature circuit resistance $(r_a) = 0.2\ \Omega$
Field circuit resistance $(r_{sh}) = 60\ \Omega$
Full load line current $(I_{Lfl}) = 40$ A

Shunt field current $(I_{sh}) = \frac{120}{60} = 2$ A

Armature current at full load $(I_{afl}) = 40 - 2 = 38$ A

$\therefore$ Back emf at full load $(E_{bfl}) = 120 - 38 \times 0.2 - 3 = 109.4$ V

Full load speed $(N_{fl}) = 1800$ rpm.

(i) At half load line current $(I_{L1}) = \frac{1}{2} \times 40 = 20$ A

$\therefore$ Armature current $(I_{a1}) = 20 - 2 = 18$ A

Back emf at half load $(E_{b1}) = 120 - 18 \times 0.2 - 3 = 113.4$ V

If N_1 be the speed at half load then

$$\frac{E_{b_1}}{Eb_{fl}} = \frac{N_1}{N_{fl}} \qquad [\because \text{for shunt motor flux is constant}]$$

$$\therefore \quad N_1 = \frac{N_{fl}\, E_{b_1}}{E_{b\,fl}} = \frac{1800 \times 113.4}{109.4} = 1866 \text{ r.p.m}$$

(ii) At 125 % of full load line current $(I_{L2}) = 1.25 \times 40 = 50$ A

$\therefore$ Armature current $(I_{a2}) = 50 - 2 = 48$ A

Back emf at 125 % full load $(E_{b2}) = 120 - 48 \times 0.2 - 3 = 107.4$ V

If N_2 be the speed at 125% of full load then

$$N_2 = \frac{N_{fl}\, E_{b_2}}{E_{b\,fl}} = \frac{1800 \times 107.4}{109.4} = 1767 \text{ r.p.m}$$

3. (a) Derive the emf equation of a dc generator. Explain all the symbols with their units.

Answer: Article 2.7.

(b) A 4 pole 240 V dc shunt motor has armature and shunt field resistance of 0.24 Ω and 240 Ω respectively. It takes 20 A from a 240 V dc supply while running at a speed of 1000 rpm. Find (i) field current (ii) armature current (iii) back emf and (iv) torque developed in Nm.

(WBUT 2006)

Answer: Supply voltage (V) = 240 V
Armature resistance (r_a) = 0.24 Ω
Shunt field resistance (r_{sh}) = 240 Ω
Line current (I_L) = 20 A
Speed (N) = 1000 rpm.

(i) Field current $(I_f) = \dfrac{240}{240} = 1$ A

(ii) Armature current $(I_a) = I_L - I_f = 20 - 1 = 19$ A

(iii) Back emf $(E_b) = V - I_a r_a$
$= 240 - 19 \times 0.24$
$= 235.44$ V

(iv) Torque developed $(T) = \dfrac{E_b l_a}{w}$

$= \dfrac{E_b l_a}{\dfrac{2\pi N}{60}}$

$= \dfrac{235.44 \times 19}{\dfrac{2\pi \times 1000}{60}}$

$= 42.74$ Nm

4. (a) Deduce the e.m.f equation of dc generator.

Answer: Article 2.7.

(b) A 4 pole, 220 V dc shunt motor has armature and shunt field resistance of 0.2 Ω and 220 Ω respectively. It takes 20 A 220 V from the source while running at a speed of 1000 r.p.m. Find

(i) field current (ii) armature current
(iii) back emf (iv) torque developed

Answer: Given $P = 4$, $V = 220$ V, $I_L = 20$ A, $r_a = 0.2$ Ω and $r_{sh} = 220$ Ω.

(WBUT 2007)

(i) field current $(I_{sh}) = \dfrac{V}{r_{sh}} = \dfrac{220}{220} = 1$ A

(ii) $I_a = I_L - I_{sh} = 20 - 1 = 19$ A

(iii) $E_b = V - I_a r_a = 220 - 19 \times 0.2 = 216.2$ V

(iv) $T = \dfrac{E_b I_a}{\omega} = \dfrac{216 \times 19}{2\pi \dfrac{1000}{60}} = 39.21$ Nm

5. (a) Deduce the expression for the voltage generated by a dc generator.
Solution: Refer Article 2.7.

(b) An 8 pole lap connected armature has 40 slots with 12 conductors per slot, generates a voltage of 500 volts. Determine the speed at which it is running if the flux per pole is 50 m Wb. Also calculate the terminal voltage at full load of 20 A if the armature resistance is 0.5 Ω and the machine is running as shunt generator having a shunt field resistance of 250 Ω. (WBUT 2008)

Solution: No. of poles $P = 8$
Total no. of conductors $Z = 12 \times 40 = 480$
General voltage $E = 500$ V
Flux per pole $\phi = 50 \times 10^{-3}$ Wb
If N be the speed in rpm then

$$E = \frac{P\phi ZN}{60\,A} \quad \text{where } A \text{ is the number of parallel paths and } A = P$$

$$\therefore \quad N = \frac{60AE}{P\phi Z} = \frac{60 \times 8 \times 500}{8 \times 50 \times 10^{-3} \times 480} = 1250 \text{ rpm}$$

Load current $I_L = 20$ A
Armature resistance $r_a = 0.5\ \Omega$
Shunt field resistance $r_{sh} = 250\ \Omega$

$$\therefore \text{ Shunt field current } I_{sh} = \frac{500}{250} = 2 \text{ A}$$

Armature current $I_a = I_L + I_{sh} = 20 + 2 = 22$ A
Terminal voltage $V_L = E - I_a r_a$
$= 500 - 22 \times 0.5$
$= 489$ V

6. (a) Derive the expression for emf in a dc generator.
Solution: Refer Article 2.7.

(b) Write a short note on back emf.
Solution: Refer Article 2.13.

(c) A 4-pole shunt generator supplies 80 A at a terminal voltage of 400 V. If a armature resistance is 0.4 Ω and shunt field resistance is 80 Ω, find the generated emf. Take voltage drop per brush as 1 V. (WBUT 2008)

Solution: $P = 4$
$I_L = 80$ A
$V = 400$ V $\quad r_a = 0.4\ \Omega \quad r_{sh} = 80\ \Omega$

$$I_{sh} = \frac{400}{80}$$

Generated emf $E = V + Ia\ ra + 1 \text{ x } 2$
$= 400 + 85 \text{ x } 0.4 + 1 \text{ x } 2$
$= 436$ V

7. (a) Give the expression for the torque developed in a dc motor.
Solution: Refer Article 2.14

(b) A 4-pole, 240 V dc shunt motor has armature and shunt field resistances of 0.24 Ω and 240 Ω respectively. It takes 20 A at 240 V while running at a speed of 1000 rpm. Find (i) field current, (ii) armature current, (iii) back e.m.f, and (iv) torque developed. (WBUT 2009)

sd_n

$V = 240$ V

r_a 0.24 Ω

$r_{sh} = 240$ Ω

$I_L = 20$ A

$N = 1000$ r.p.m.

(i) Field current $= \dfrac{240}{240} = 1$ A

(ii) Armature current = 20 – 1 = 19

(iii) Back emf = $240 - 19 \times 0.2$
$= 235.44$ V

(iv) Torque developed $= \dfrac{235.44 \times 19}{2\pi \times \dfrac{1000}{60}}$

$= 42.72$ Nm

8. Derive the expression of torque of a dc series motor. (WBUT 2012)

Solution: Refer Articles 2.14 and 2.14.2.

9. (a) Explain the open circuit characteristics (OCC) of a DC generator. (WBUT 2012)

Solution: Refer Article 2.11.1.

(b) An 8-pole, 400 V shunt motor has 960 wave connected armature conductors. The full load armature current is 40 A and flux per pole is 0.02 Wb. The armature resistance is 0.1 Ω and the contact drop is 1 V per brush. Calculate the full load speed of the motor. (WBUT 2012)

Solution:

$P = 8$
$V = 400$
$Z = 960$
$A = 2$
$I_a = 40$ A
$\phi = 0.02$ wb
$r_a = 0.1$ Ω

$$E = \frac{P\phi Z N}{60\text{ A}} = \frac{8 \times 0.02 \times 960 \times N}{60 \times 2} = V - I_a r_a - \text{brush contact drop}$$

$$= 400 - 40 \times 0.1 - 2 = 394 \text{ V}$$

$$N = \frac{394 \times 60 \times 2}{8 \times 0.02 \times 960} = 308 \text{ rpm}$$

(c) Why starter is needed to start a dc motor?

Solution: Refer Article 2.21.

10. Draw and explain speed-torque characteristics of a (i) dc shunt motor, and (ii) dc series motor. [WBUT 2013]

Solution: Refer Article 2.18.

11. A shunt motor has a rated armature current of 40 A when connected to 200 V. The rated speed of the motor is 1000 rpm. The armature resistance is 0.2 ohm. Find the speed of the motor if the total torque is reduced to 70% of that at rated load and a 3-ohm resistance is inserted in series with the armature. [WBUT 2013]

    Solution: Refer Example 2.34.

12. Explain how the speed of a dc shunt motor can be controlled by flux control method. [WBUT 2014]

    Solution: Refer Article 2.19.2

Multiple Choice Question

1. If a dc series motor is started at no load, the speed will be (WBUT 2012)

    (a) rated speed (b) zero
    (c) very high (d) half of the rated speed

    Answer: (c) very high

2. A series motor will run at very high speed when (WBUT 2013)

    (a) load is increased (b) field is opened
    (c) the armature is opened (d) the load is removed

    Answer: (d) the load is removed

3. A series motor drawing armature current I_a is operated under saturated condition. The torque will be proportional to (WBUT 2014)

    (a) $1/I_a$ (b) $1/I_a^2$
    (c) I_a^2 (d) I_a

    Answer: (d) I_a

4. The dc motor used for traction purpose is (WBUT 2014)

    (a) shunt (b) series
    (c) compound (d) none of these

    Answer: (b) series

3 SINGLE PHASE TRANSFORMER

3.1 DEFINITION

A transformer may be defined as a static electric device that transfers electrical energy from one circuit to another circuit at the same frequency but with changed voltage (or current or both) through a magnetic circuit.

3.2 CONSTRUCTION OF SINGLE-PHASE TRANSFORMERS

A single-phase transformer consists of primary and secondary windings placed on a *magnetic core*. The magnetic core is a stack of thin silicon steel laminations (CRGO steel). The laminations reduce eddy current loss and silicon steel reduces hysteresis loss. There are two general types of transformers, *core type* and *shell type*.

In core type transformers, the windings surround a considerable part of the steel core. The core consists of two vertical legs (or *limbs*) and the horizontal portions (called *yokes*) as shown in Fig. 3.1. For reduction of the leakage flux half of each winding is placed on each leg of the core. The low voltage winding is placed usually adjacent to the steel core and high voltage is placed outside in order to minimise the amount of insulation required.

In shell type transformers the steel core surrounds a major part of the winding as shown in Fig. 3.2. The low voltage and high voltage windings are wound over the central limb and are *interleaved* (or) *sandwiched*. The shell type transformer requires more conductor material as compared to core type transformer.

In core type transformers the flux has a single path around the legs whereas in shell type transformers the flux in the central limb divides equally and returns through the outer two legs. Concentric coils are used for core type transformers and interleaved (or sandwiched) coils are used for shell type transformers.

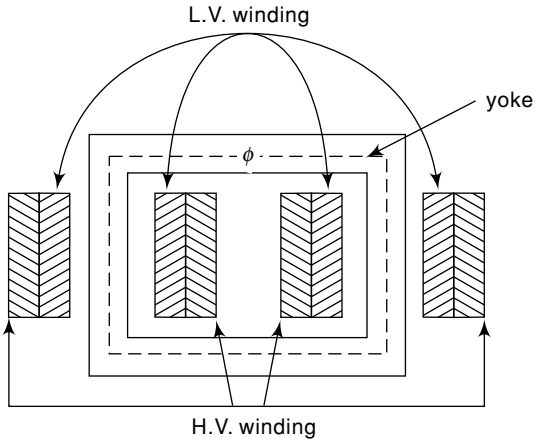


Fig. 3.1 *Core type transformer*

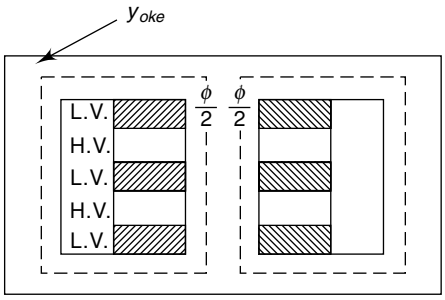


Fig. 3.2 *Shell type transformer*

3.3 PRINCIPLE OF OPERATION

When alternating voltage V_1 is applied to the primary winding of a transformer a current (termed as exciting current, I_ϕ) flows through it as shown in Fig. 3.3. The exciting current produces an alternating flux (ϕ) in the core, which links with both the winding (primary and secondary). According to Faraday's laws of electromagnetic induction, the flux will cause self-induced emf E_1 in the primary and mutually induced emf E_2 in the secondary winding. But according to Lenz's law primary induced emf will oppose the applied voltage and in magnitude this primary induced emf is (almost) equal to the applied voltage. Therefore, in brief we can say emf induced in the primary winding is equal and opposite to the applied voltage.*

When a load is connected to the secondary side, current will start flowing in the secondary winding. Voltage induced in the secondary winding is responsible to deliver power to the load connected to it. In this way power is transferred from one circuit (primary) to another (secondary) winding through a magnetic circuit by electromagnetic induction. This is the working principle of the transformer.

*If all the losses are neglected, the transformer is said to be ideal and hence for open circuited secondary, we can write $|V_1| = |E_1|$; $|V_2| = |E_2|$.

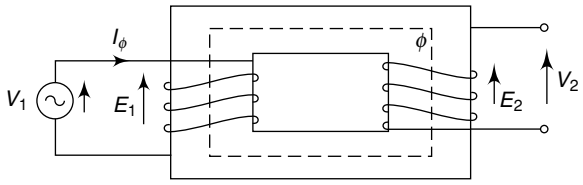


Fig. 3.3 ***Schematic diagram of single phase transformer***

The induced emf in the secondary E_2 is also in phase opposition to the applied voltage V_1 at primary. If the secondary is open circuited, terminal voltage V_2 at the secondary is equal in magnitude and in phase with the induced emf at secondary.

3.4 EMF EQUATION

Since the applied voltage is sinusoidal at the primary, the flux produced by the exciting current is also sinusoidal (asuming $\phi \propto I$).

Thus core flux is given by $\phi = \phi_{\max} \sin \omega t$. If the coil has N turns then instantaneous value of the induced emf e is given by

$$e = -N\frac{d\phi}{dt}$$

or $$e = -N\frac{d}{dt}(\phi_{\max} \sin \omega t)$$

or $$e = -2\pi f\, \phi_{max}\, N \cos \omega t \qquad (\because \quad \omega = 2\pi f)$$

The maximum value of the induced emf will be obtained when (cos ωt) is 1.

i.e . $$E_{\max} = 2\pi f\, \phi_{\max}\, N \text{ V} \qquad (3.1)$$

Dividing both sides of equation (3.1) by $\sqrt{2}$, we have

$$\frac{E_{\max}}{\sqrt{2}} = \frac{2\pi}{\sqrt{2}} \phi_{\max} f N$$

or $$E_{\text{rms}} = 4.44\, \phi_{\max} f N. \qquad (3.2)$$

If N_1 be the primary number of turns, then the rms values of induced voltage at primary is given by

$$E_1 = 4.44\, \phi_{\max} f N_1. \qquad (3.2a)$$

(As the induced voltage in the primary winding is equal and opposite to the applied voltage, so $V_1 = 4.44\, \phi_{\max} f N_1$).

Similarly, the rms value of the induced emf at secondary is obtained as

$$E_2 = 4.44\, \phi_{\max} f N_2 \text{ volt} \qquad (3.2b)$$

Thus for a single phase *ideal* transformer, the expressions for the induced voltages at the primary as well as at the secondary windings can be obtained from Eqns (3.2a) and (3.2b).

3.5 TRANSFORMATION RATIO (OR TURNS RATIO)

Let N_1 = Number of turns in the primary winding
N_2 = Number of turns in the secondary winding
E_1 = RMS value of the primary induced emf
E_2 = RMS value of the secondary induced emf.

Using the emf equation, we can write

$$E_1 = 4.44\, f\, N_1\, \phi_m \text{ and } E_2 = 4.44\, f\, N_2\, \phi_m$$

$$\therefore \quad \frac{E_1}{E_2} = \frac{N_1}{N_2} \tag{3.3}$$

Thus the ratio of primary voltage to secondary voltage is same as the ratio of primary winding turns to the secondary winding turns. The ratio N_1/N_2 is known as the *transformation ratio* (or *turns ratio*). It is usually denoted by K). By selecting this ratio properly, transformation can be done from any input voltage to any convenient output voltage. There can be two cases:

(a) If $N_1 > N_2$, then $E_2 < E_1$; the transformer is known as a *step-down* transformer ($k > 1$).

(b) If $N_2 > N_1$, then $E_2 > E_1$; the transformer is known as a *step-up* transformer ($k < 1$).

Let us again consider a two-winding transformer. In the process of transforming electrical power from one voltage to the other, there occurs some losses in the transformer. These losses are actually very small as compared to the total amount of power handled by the transformer. If we neglect these losses for the time being, we must have the same power (volt-ampere) in the primary and in the secondary winding. If I_1 and I_2 are the currents in the primary and secondary windings of an ideal transformer (i.e having no losses), we should have

$$E_1 I_1 = E_2 I_2$$

[$E_1 I_1$ and $E_2 I_2$ are the primary and secondary powers (voltamperes)]

or

$$\frac{I_1}{I_2} = \frac{E_2}{E_1} = \frac{N_2}{N_1} = \frac{1}{K} \quad \left(= \frac{V_2}{V_1}\right) \tag{3.4}$$

Thus we find that *the current is transformed in the reverse ratio of the voltage*. If a transformer steps up the voltage, it steps down the current. If it steps down the voltage, it steps up the current.

3.6 IMPEDANCE TRANSFORMATION

In Fig. 3.4 an impedance Z_2 is connected across the secondary winding at its output. The primary winding is connected to a voltage source V_1. The number of turns in the two windings are assumed to be N_1 and N_2. Induced emfs E_1 and E_2 are in phase opposition to V_1. Since V_2 is the secondary terminal voltage, it is also in the opposite phase of V_1.

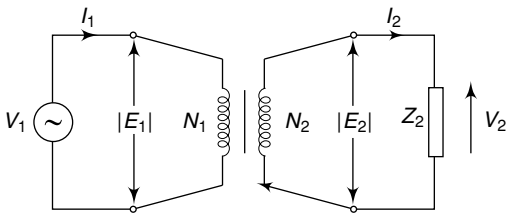


Fig. 3.4 *Schematic diagram of two-winding transformers*

Assuming the transformer to be ideal,

$$\frac{V_1}{V_2} = \frac{E_1}{E_2} = \frac{N_1}{N_2} = K \quad \text{(turns-ratio).}$$

The impedance Z_2', as seen from the input side, can be obtained by dividing voltage V_1 by I_1. Thus, we can write

$$Z_2' = \frac{V_1}{I_1} = \frac{V_1 \times (V_2 I_2)}{I_1 \times (V_2 I_2)}$$

$$= \left(\frac{V_1}{V_2}\right) \times \left(\frac{I_2}{I_1}\right) \times \left(\frac{V_2}{I_2}\right) = K \times K \times Z_2 = K^2 Z_2 \text{ i.e,}$$

$$\frac{Z_2'}{Z_2} = K^2. \tag{3.5}$$

Therefore, *impedance transformation ratio is equal to the square of turns ratio*. Referring to the primary or secondary side, this transferred impedance is known as the *equivalent impedance* on that side. In an ideal transformer thus we can note the following.

- Voltages are transformed in the direct ratio of turns. ($V_1/V_2 = K$)
- Currents are transformed in the inverse ratio of turns. ($I_1/I_2 = 1/K$)
- Volt-amperes of two sides are equal. ($V_1 I_1 = V_2 I_2$)
- Impedances are transformed in proportion to the square of turns-ratio. $\left(Z_2' = K^2 Z_2 \; ; Z_1' = \frac{1}{K^2} \times Z_1\right)$

3.1 Find the cross-sectional area of the core of a 10 turns transformer for a voltage of 50 V at 50 Hz. The flux density is 0.9 Wb/m^2.

Solution

Number of turns $N = 10$
Voltage $E = 50$ V
Frequency $f = 50$ Hz
Flux density $B = 0.9$ Wb/m^2.
If A be the cross-sectional area then
Flux $\phi = (0.9A)$ Wb
$\because$ $E = 4.44\ \phi f N$,
Here, $E = 4.44 \times 0.9\ A \times 50 \times 10 = 50$
Hence, $A = \dfrac{50}{4.44 \times 0.9 \times 500}$ m^2 = 0.025 m^2.

3.2 A single-phase transformer has 400 primary and 1000 secondary turns. The net cross sectional area of the core is 60 cm^2. The primary winding is connected to a 500 V supply. Find the (i) peak value of the core flux density and the (ii) emf induced in the secondary winding.

Solution

$N_1 = 400 \quad N_2 = 1000$
$A = 60$ cm^2 = 0.006 m^2
$E_1 = 500$ V (given)

$\because$ $E_1 = 4.44\ \phi_m f N_1$,

So $\phi_m = \dfrac{500}{4.44 \times 50 \times 400} = 0.0056$ Wb.

(i) Peak value of core flux density $= \dfrac{0.0056}{0.006}$ Wb/m^2 = 0.938 Wb/m^2.

(ii) Emf induced in the secondary $E_2 = 4.44\ \phi_m f N_2$
$= 4.44 \times 0.0056 \times 50 \times 1000$ V = 1243.2 V.

3.3 The primary winding of a 50 Hz transformer is supplied from a 440 V, 50 Hz source and has 200 turns. Find the (i) peak value of flux (ii) voltage induced in the secondary winding if it has 50 turns.

Solution

$f = 50$ Hz
$E_1 = 440$ V
$N_1 = 200$.

(i) If ϕ_m is the peak value of flux then
$E_1 = 4.44\ f\ \phi_m\ N_1$
or $\phi_m = \dfrac{440}{4.44 \times 50 \times 200}$ Wb = 0.0099 Wb.

(ii) $N_2 = 50$
Voltage induced in the secondary
$E_2 = 4.44\ f\ \phi_m\ N_2 = 4.44 \times 50 \times 0.0099 \times 50$ V = 110 V.

3.4 A 200 kVA single-phase transformer has 1000 turns in the primary and 600 turns on the secondary. The primary winding is supplied from a 440 V, 50 Hz source. Find the (i) secondary voltage at no load and (ii) primary and secondary currents at the full load.

Solution

Let primary and secondary currents at full load be I_1 and I_2.

Primary kVA = Secondary kVA = 200
$\therefore$ $E_1 I_1 = E_2 I_2 = 200 \times 10^3$ VA
$N_1 = 1000$; $N_2 = 600$
$E_1 = 440$ V.

(i) Now, $\dfrac{E_1}{E_2} = \dfrac{N_1}{N_2}$ or, $E_2 = \dfrac{E_1 N_2}{N_1} = 440 \times \dfrac{600}{1000} = 264$ V.

(ii) $I_1 = \dfrac{200 \times 10^3}{E_1} = \dfrac{200 \times 10^3}{440}$ A = 454.54 A.

$I_2 = \dfrac{200 \times 10^3}{E_2} = \dfrac{200 \times 10^3}{264}$ A = 757.57 A.

3.5 The emf per turn for a single-phase 440/220 V, 50 Hz transformer is approximately 15 V. Find (i) the number of primary and secondary turns and (ii) the net cross sectional area of the core, for a maximum flux density of 1 Wb/m^2.

Solution

$E_1 = 440$ V
$E_2 = 220$ V
$f = 50$ Hz.
Voltage per turn = 15 V.

(i) If N_1 and N_2 be the number of turns in the primary and secondary respectively,

$$\frac{E_1}{N_1} = \frac{E_2}{N_2} = 15$$

$$\therefore \quad N_1 = \frac{E_1}{15} = \frac{440}{15} = 29.33.$$

As the number of turns cannot be a fraction so N_1 is taken as 30.

$$\therefore \quad \text{voltage per turn} = \frac{440}{30} = 14.67 \text{ V}$$

$$\text{Also,} \quad N_2 = \frac{E_2}{E_1} N_1 = \frac{220}{440} \times 30 = 15$$

(ii) Flux density $B_m = 1$ Wb/m^2 (given).

If A be the cross-sectional area then, $\frac{E_1}{N_1} = 4.44(B_{mr}A)f$, i.e. $4.44\ B_m A\ f = 14.67$

$$\therefore \quad A = \frac{14.67}{4.44 \times 1 \times 50} \text{ m}^2 = 0.066 \text{ m}^2.$$

3.6 A 400/50 V, 60 Hz step down transformer is to be operated at 50 Hz. Find (i) the highest safe input voltage and (ii) transformation ratio in both frequency applications.

Solution

$E_1 = 400$ V
$E_2 = 50$ V
$f = 60$ Hz

$\because \quad E_1 = 4.44\ \phi_m f N_1,$

$$\therefore \quad 4.44\ \phi_m N_1 = \frac{400}{60} = 6.67.$$

(i) If E_1' be the highest safe input at 50 Hz;

$E_1' = 4.44\ \phi_m N_1 \times 50 = 6.67 \times 50 = 333.5$ V.

(ii) Transformation ratio at 60 Hz

$$\frac{E_1}{E_2} = \frac{400}{50} = 8$$

At 50 Hz, the secondary induced emf is given by

$$E_2' = \frac{N_2}{N_1} E_1' = \frac{N_2}{N_1} \times E_1'$$

$$\text{Now,} \quad \frac{N_2}{N_1} = \frac{E_2}{E_1} = \frac{50}{400} = \frac{1}{8}$$

$$\text{So,} \quad E_2' = \frac{1}{8} E_1'$$

$$\text{or} \quad \frac{E_1'}{E_2'} = 8.$$

Transformation ratio at 50 Hz is also 8.

3.7 A 200/50 V, 50 Hz transformer has a core area of 100 cm^2. The maximum value of the flux density is 1 Wb/m^2. Assuming 9% loss of area due to laminations, find the primary and secondary number of turns and transformation ratio.

Solution

$$A = 100 \times 10^{-4} \text{ m}^2 = 0.01 \text{ m}^2$$
$$E_1 = 200 \text{ V}; \quad E_2 = 50 \text{ V}; \quad B_m = 1 \text{ Wb/m}^2$$

Assuming 9% loss of area, net area of core = $0.01 \times 0.09 \text{ m}^2 = 0.0091 \text{ m}^2$

Primary turns $N_1 = \dfrac{E_1}{4.44 f B_m A} = \dfrac{200}{4.44 \times 50 \times 1 \times 0.0091} = 99$

Secondary turns $N_2 = \dfrac{E_2}{E_1} N_1 = \dfrac{50}{200} \times 99 \simeq 25$

Transformation ratio $\dfrac{E_1}{E_2} = \dfrac{N_1}{N_2} = \dfrac{100}{25} = 4.$

3.8 A 1000 kVA transformer has primary and secondary turns of 400 and 100 respectively and induced voltage in the secondary is 1000 V. Find (i) the primary volt (ii) the primary and secondary full load current and (iii) the secondary current when 100 kW load at 0.8 p.f. is connected at the output.

Solution

Given: kVA = 1000
$N_1 = 400$
$N_2 = 100$
$E_2 = 1000.$

(i) Primary voltage $E_1 = \dfrac{N_1}{N_2} E_2 = \dfrac{400}{100} \times 1000 = 4000$ V.

(ii) Primary full load current $I_1 = \dfrac{VA}{E_1} = \dfrac{1000 \times 10^3}{4000} = 250$ A

Secondary full load current $I_2 = I_1 \times \dfrac{N_1}{N_2} = 250 \times \dfrac{400}{100} = 1000$ A.

(iii) Secondary current at 100 kW and 0.8 p.f. load

$$I_2 = \frac{100 \times 10^3}{0.8 \times 1000} = 125 \text{ A}.$$

3.7 NO LOAD OPERATION OF A TRANSFORMER

A transformer is said to be on no load, if its primary winding is connected to an ac supply source and the secondary is open. The instantaneous flux (ϕ) linking with both the windings is given as $\phi = \phi_m \sin \omega t$.

Therefore, the induced emf in primary winding is given as

$$E_1 = -N_1 \frac{d\phi}{dt} = -N_1 \frac{d}{dt}(\phi_m \sin \omega t)$$
$$= -N_1 \omega \phi_m \cos \omega t = N_1 \omega \phi_m \sin\left(\omega t - \frac{\pi}{2}\right)$$

Similarly, the induced emf in the secondary winding is given as

$$E_2 = N_2 \omega \phi_m \sin\left(\omega t - \frac{\pi}{2}\right)$$

We consider the transformer to be ideal (i.e there are no voltage drops in the windings). E_1 and E_2 are in phase opposition to V_1.
It is thus evident that

- The induced emfs in primary and secondary windings (E_1 and E_2) lag behind the main flux ϕ by an angle $\pi/2$, and E_1 and E_2 are in the same phase with each other [as shown in the phasor diagram (Fig. 3.5)].
- Applied voltage to the primary winding V_1, leads the main flux ϕ by an angle $\pi/2$. Also it is in phase opposition to the induced emfs in the primary winding and secondary winding in ideal transformers. In ideal transformers there is no voltage drop in the secondary winding and hence $|V_2| = |E_2|$.

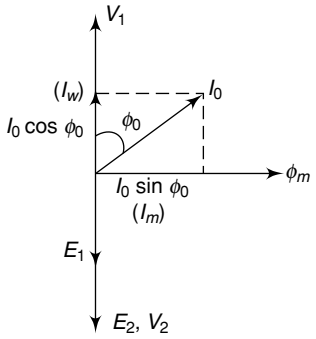


Fig. 3.5 ***Phasor diagram under no load condition ($N_2 > N_1$)***

- *The no load current* or exciting current I_o lags behind the applied voltage by an angle ϕ_o. It has two components I_m and I_w. The magnetising component I_m is in phase with the main flux ϕ, whereas, the other component I_w is in phase with the applied voltage. (This current is required to meet the hysteresis and eddy-current losses occurring in the core.)

  Thus, from the phasor diagram of Fig. 3.5, we have

$$I_o = \sqrt{I_m^2 + I_w^2} \; ; \; I_w = I_o \cos \phi_o, \; I_m = I_o \sin \phi_o$$

  and $\phi_o = \tan^{-1} \dfrac{I_m}{I_w}$. (In practice, ϕ_o is close to 90° and is called *no load power factor angle*.)

When a transformer is connected to a supply, there actually occurs eddy-current loss and hysteresis loss in the iron-core and appear as heat. This power is taken from the ac supply at primary.

The no load current component I_m is used in magnetizing the core. (There is no power loss due to this current). The current I_m lags behind the applied voltage V_1 by $\pi/2$. The product of I_m and V_1 does not represent active power. This product is called the *reactive power*. Therefore, the input active power at no-load is

$$P_o = V_1 I_w = V_1 I_o \cos \phi_o \qquad (3.6)$$

and, the reactive power is

$$W_o = V_1 I_m = V_1 I_o \sin \phi_o. \qquad (3.7)$$

3.8 WORKING OF A TRANSFORMER ON LOAD

When the transformer is loaded, load current I_2 flows in the secondary winding. Secondary number of turns being N_2, the secondary ampere- turns is $I_2 N_2$; it sets up flux ϕ_2 in the core, which opposes the flux ϕ already set up by the no load current. As a result the flux linking with primary is reduced. The difference between applied voltage and induced voltage in the primary will however exist

resulting in additional current in the primary (say of magnitude I_1'). The primary turns being N_1 these additional ampere-turns is $I_1' N_1$ and will produce flux ϕ_1 in the opposite direction of ϕ_2 (i.e. in the same direction of the original flux ϕ). Magnetic equilibrium will be achieved when $\phi_1 = \phi_2$, thus leaving behind the initial flux ϕ. Therefore from the above discussion it is evident that when a transformer is loaded the secondary ampere-turns necessitates the production of additional primary ampere-turns, which is equal in magnitude, to the secondary ampere-turns, but opposite in direction (Ref. Fig. 3.6).

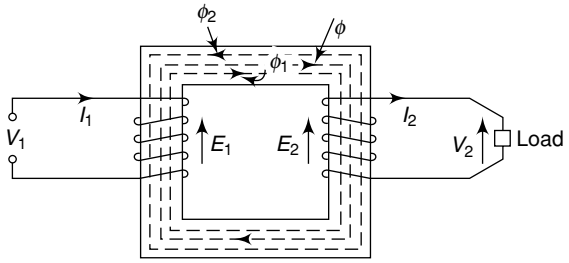


Fig. 3.6 ***Transformer under load***

The phasor diagram of the transformer on load can be drawn for different types of loadings and is explained below.

The no load phasor diagram is drawn and discussed earlier. Let us now consider load current I_2 while the load is of inductive nature. I_2 will be lagging the secondary voltage (i.e. E_2 or V_2). When there is no voltage drop in the transformer (transformer being ideal) then $|V_2| = |E_2|$. To counter balance the secondary ampere-turns additional primary current I_2' will flow and will be 180° out of phase of I_2. The total primary current I_1 is the phasor sum of the no load current I_o and of the additional primary current I_2'. Complete phasor diagram of the transformer on load for inductive load has been shown in Fig. 3.7(b). Figure 3.7(a) and (c) represent phasor diagrams no load when load is having unity power factor and leading power factor respectively.

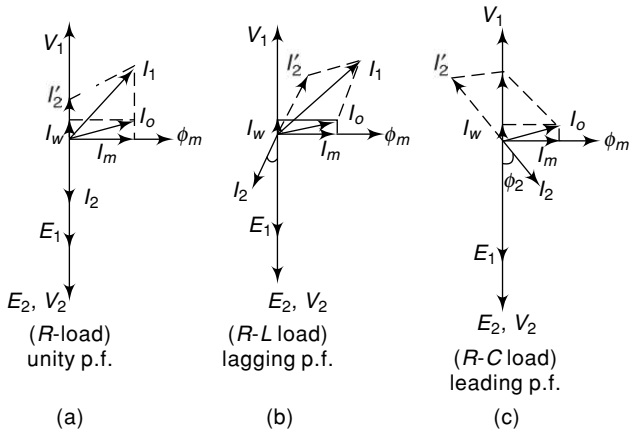


Fig. 3.7 ***Transformer phasor diagram at different p.f. neglecting transformer internal voltage drop ($N_2 > N_1$)***

Figure 3.8(a) shows the phasor diagram of a transformer under lagging load power factor and considering internal voltage drop (the transformer is now not an ideal one). The voltage $(-E_1)$ has been replaced by V_1' for convenience. Alternatively V_1' may be treated as a voltage drop in the primary in the direction of flow of primary current. The primary current I_1 flows through primary resistance R_1 and primary leakage reactance X_1. Hence primary voltage is given as

$$V_1 = V_1' + I_1(R_1 + jX_1), \text{ where } V_1' \text{ is } (-E_1).$$

Similary, $E_2 = V_2 + I_2(R_2 + jX_2)$ where R_2 and X_2 are the resistance and leakage reactance of the secondary side of the transformer.

Here, V_1 = the supply voltage (input voltage at primary)
E_1 = the induced voltage at primary
$V_1' = -E_1$ (phasor E_1 reserved to the primary side in the phasor diagram)
I_o = the no load (magnetising) current at primary $(= I_w + I_m)$
E_2 = the secondary induced voltage
V_2 = the output voltage, i.e. terminal voltage at the secondary
I_2 = the secondary load current
ϕ = the p.f. angle
I_2' = the referred secondary current to primary.

Figures 3.8(b) and 3.8(c) represent the phasor diagrams of the transformer (not an ideal one) operating with unity power factor and leading power factor respectively.

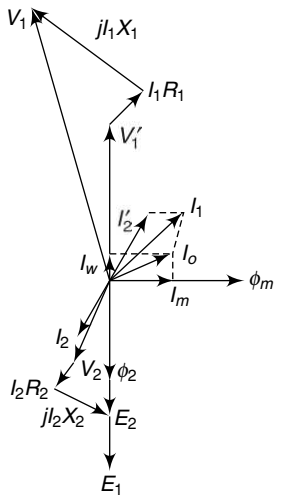


Fig. 3.8(a) ***Exact phasor diagram for lagging power factor I_1 = (primary current); R_1, X_1 and R_2, X_2 = primary and secondary winding resistance and reactances.***

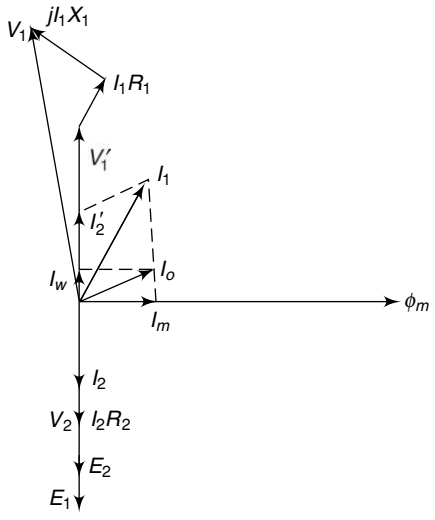


Fig. 3.8(b) ***Exact transformer phasor diagram for unity power factor [I_2 and V_2 in phase]***

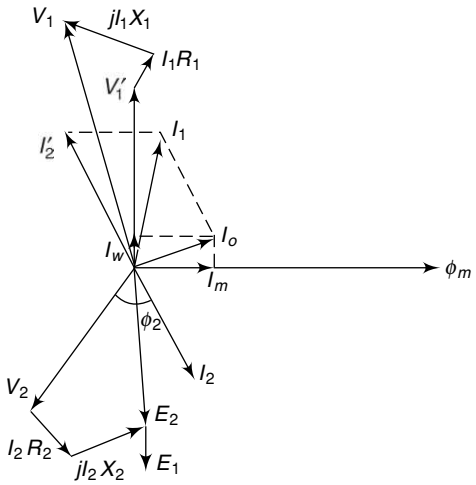


Fig. 3.8(c) ***Exact transformer phasor diagram for leading power factor [I_2 leads V_2]***

3.9 EQUIVALENT CIRCUIT OF TRANSFORMER

Though the ideal transformer winding does not have any resistance, in actual practice, there is always some resistance of the windings. This causes a voltage drop. The resistance of the primary winding is represented by R_1 and that of the secondary by R_2.

The actual transformer has another deviation from the ideal transformer. Not all of the flux produced by the primary winding links with the secondary winding in the actual transformer. Similarly, not all of the flux produced by the secondary winding links with the primary winding. The difference between the total flux linking with the primary winding and the mutual flux ϕ linking with both windings is called the *primary leakage flux*. Similarly, the *secondary leakage flux* can also be expressed.

We can write Kirchhoff's voltage equations for the primary and secondary sides of the transformer (Fig. 3.9) as

$$V_1 = I_1R_1 + jI_1 X_1 - E_1 = I_1(R_1 + jX_1) - E_1 \tag{3.8}$$

and

$$E_2 = I_2R_2 + jI_2 X_2 + V_2 = I_2(R_2 + jX_2) + V_2. \tag{3.9}$$

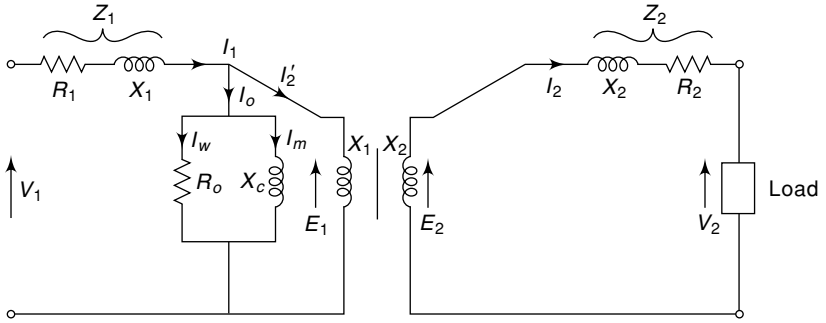


Fig. 3.9 ***Equivalent circuit of transformer***

The equivalent circuit gives the interpretation of the above equations. Further, we know the primary current I_1 is composed of two currents I_2' and I_o. Also, the current I_o consists of two components, I_m and I_w. Therefore, the current I_o can be considered to be split into two parallel branches. The current I_w accounts for the core-loss, and hence is shown to flow through resistance R_o. The current I_m represents the magnetising current and is shown to flow through a pure reactance X_o. This branch consisting of the parallel R_o and X_o is called the *magnetising branch* of the transformer.

Using the impedance transformation, we can draw the simplified equivalent circuit of a transformer, as referred to the primary side only or to the secondary side only.

We have seen earlier that an impedance connected across the secondary appears as K^2 times, when referred to the primary. (Here, $K = N_1/N_2$, where K is the transformation ratio). Therefore to simplify the equivalent circuit of Fig. 6.9, we can transfer the resistance R_2 and the reactance X_2 to the primary side, by simply multiplying each of them by K^2. The total resistance and the total reactance in the primary side then becomes

$$R_{o1} = R_1 + K^2R_2 \quad \text{and} \quad X_{o1} = X_1 + K^2X_2$$

where $R_2' = K^2R_2$ and $X_2' = K^2X_2$.

The equivalent circuit of the transformer now simply reduces to the one as shown in Fig. 3.10(a).

Here,
$$I_2' = \frac{1}{K} I_2$$
$$V_2' = KV_2$$
$$R_{o1} = R_1 + X_2'$$
$$R_2' = K^2R_2$$
$$X_{o1} = X_1 + X_2'$$
$$X_2' = K^2X_2$$
$$I_1 = I_o + I_2'.$$

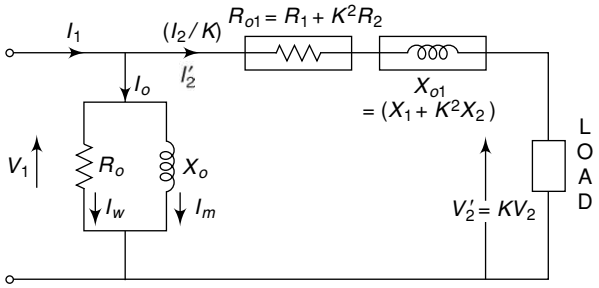


Fig. 3.10(a) ***Equivalent circuit of transformer referred to primary***

Similarly, the equivalent circuit as referred to secondary side can also be drawn. But in this case the equivalent resistance and reactance as referred to secondary side will be

$$R_{o2} = R_2 + (1/K^2)R_1 \text{ and } X_{o2} = X_2 + (1/K^2)X_1.$$

The equivalent circuit referred to the secondary is shown in Fig. 3.10(b). Here R_o' and X_o' represent the core resistance and the magnetizing reactance referred to the secondary.

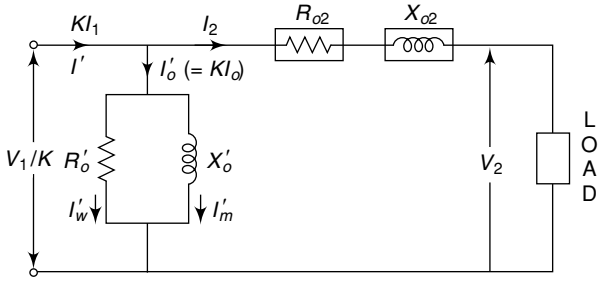


Fig. 3.10(b) *Equivalent circuit of transformer referred to secondary*

3.10 APPROXIMATE EQUIVALENT CIRCUIT

Since in a transformer the magnitude of I_o is very low (1 – 3% of the full load current), we can neglect the magnetising branch for simplicity. The equivalent circuit neglecting the magnetising branch is called the approximate equivalent circuit (Fig. 3.10(c) and Fig. 3.10(d)).

$$R_{o2} = R_2 + \frac{1}{K^2} R_1 \; ; \; R_{01} = R_1 + K^2 R_2$$

$$X_{o2} = X_2 + \frac{1}{K^2} X_1 \; ; \; X_{01} = X_1 + K^2 X_2$$

$$V_1' = \frac{1}{K} V_1 ; \; V_2' = KV_2$$

$$I_1' = KI_1 ; \; I_2' = (I_2/K)$$

$$I_o' = KI_o$$

$$R_o' = \frac{1}{K^2} R_o$$

$$X_o' = \frac{1}{K^2} X_o$$

$$KI_1 = I_1' = KI_o + I_2$$

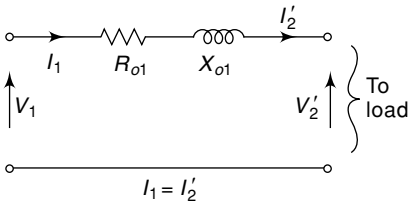


Fig. 3.10(c) *Approximate equivalent circuit of transformer referred to as primary*

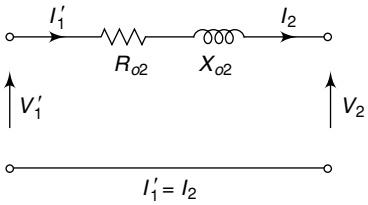


Fig. 3.10(d) *Approximate equivalent circuit of transformer referred to as secondary*

3.11 REGULATION OF A TRANSFORMER

The *regulation* of a transformer (generally expressed as percentage regulation) may be defined as

$$\left[\frac{\text{Secondary no load voltage} - \text{Secondary full load voltage}}{\text{Secondary no load voltage}}\right] \times 100$$

If E_2 = the secondary no load voltage

V_2 = the terminal voltage at secondary

$$\text{then percentage regulation} = \frac{E_2 - V_2}{E_2} \times 100 \tag{3.10}$$

Therefore percentage regulation of a transformer is defined as the *percentage decrease in the terminal voltage of the transformer from no-load to full load condition at a constant applied voltage*.

3.11.1 Expression for Regulation

Let us consider the equivalent circuit of the transformer referred to the secondary (as shown in Fig. 3.11)

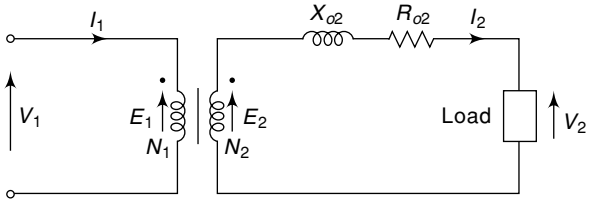


Fig. 3.11 ***Approximate equivalent circuit of transformer referred to as secondary***

When the load is connected to the secondary side, current I_2 will start flowing. Depending upon the nature of the load, current I_2 may be lagging the voltage V_2 for inductive load, in phase of the voltage V_2 for resistive load and leading the voltage V_2 for capacitive load.

Hence on the basis of the above current-voltage phasor relation, the load has a lagging power factor, a unity power factor and a leading power factor respectively. Expressions for regulation in each case will be as discussed below.

(i) Lagging power factor The phasor diagram of the transformer referred to as the secondary, when supplying a load of lagging power factor load, has been shown in Fig. 3.12, where,

E_2 = the no load voltage

V_2 = the load voltage

I_2R_{o2} = the resistive drop referred to secondary

I_2X_{o2} = the reactive drop referred to secondary

and θ_2 = the angle between V_2 and I_2 i.e. cos θ_2 is p.f. of the load.

$[Oa = V_2;\ ab = I_2R_{o2} \cos \theta_2;\ bc \simeq I_2 X_{o2} \sin \theta_2;\ cd = (I_2 X_{o2}) \cos \theta_2 - I_2R_{o2} \sin \theta_2]$

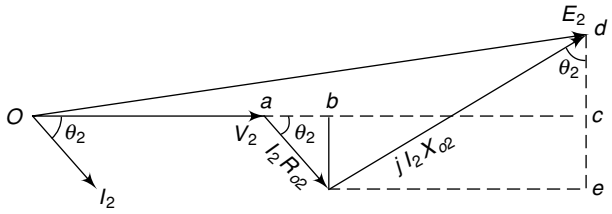


Fig. 3.12 ***Phasor diagram of a transformer on lagging load, referred to as secondary***

From Fig. 3.12

$$E_2^2 = (Oc)^2 + (cd)^2 = (Oa + ab + bc)^2 + (cd)^2$$
$$= (V_2 + I_2 R_{o2} \cos \theta_2 + I_2 X_{o2} \sin \theta_2)^2$$
$$+ (I_2 X_{o2} \cos \theta_2 - I_2 R_{o2} \sin \theta_2)^2$$

where I_2 is the secondary current lagging V_2 by angle θ_2.

As $(I_2 X_{o2} \cos \theta_2 - I_2 R_{o2} \sin \theta_2)$ is very small (being the difference of two quantities) it can easily be neglected.

Hence $$E_2 \simeq V_2 + I_2 R_{o2} \cos \theta_2 + I_2 X_{o2} \sin \theta_2$$

or $$E_2 - V_2 = (I_2 R_{o2} \cos \theta_2 + I_2 X_{o2} \sin \theta_2). \quad (3.11)$$

$$\text{Percentage voltage regulation} = \frac{E_2 - V_2}{E_2} \times 100\%$$

$$= \left(\frac{I_2 R_{o2}}{E_2} \cos \theta_2 + \frac{I_2 X_{o2}}{E_2} \sin \theta_2 \right) \times 100\% \quad (3.12)$$

$$= (R_{\text{p.u}} \cos \theta_2 + X_{\text{p.u}} \sin \theta_2) \times 100\% \quad (3.13)$$

where $(R_{\text{p.u}})$ and $(X_{\text{p.u}})$ are the total p.u resistance and reactance respectively

$$\left[R_{\text{p.u.}} = \frac{I_2 R_{o2}}{E_2}; X_{\text{p.u.}} = \frac{I_2 X_{o2}}{E_2} \right]$$

(ii) Unity power factor Phasor diagram at unity p.f. has been shown in Fig. 3.13. From Fig. 3.13 we have

$$E_2^2 = (V_2 + I_2 R_{o2})^2 + (I_2 X_{o2})^2 \quad (3.14)$$

If the second term is neglected

$$E_2 = V_2 + I_2 R_{o2} \quad (3.15)$$

{The second term $(I_2 X_{02})$ is neglected as it does not contribute much in changing the magnitude of V_2. On the other hand, it is responsible for the phase shift between E_2 and V_2 . Hence we can reasonably neglect $(I_2 X_{02})$}.

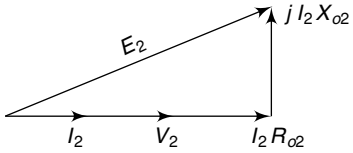


Fig. 3.13 ***Phasor diagram of the transformer for unity p.f. load***

Hence percentage voltage regulation $= \frac{E_2 - V_2}{E_2} \times 100\%$

$$= \frac{I_2 R_{o2}}{E_2} \times 100\%$$
$$= R_{\text{p.u}} \times 100\% \quad (3.16)$$

(iii) Leading power factor For leading power factor (cos θ_2),

$$I_2 = I_2 \cos \theta_2 + j\, I_2 \sin \theta_2$$

$$E_2 = V_2 + I_2 Z_{o2} = V_2 + j.0 + (I_2 \cos \theta_2 + jI_2 \sin \theta_2)\,(R_{o2} + j\, X_{o2})$$

or $$E_2 = V_2 + \mathrm{I}_2 R_{o2} \cos \theta_2 - I_2 X_{o2} \sin \theta_2 + j(I_2 R_{o2} \sin \theta_2 + I_2 X_{o2} \cos \theta_2)$$

Hence $$E_2^2 = (V_2 + I_2 R_{o2} \cos \theta_2 - I_2 X_{o2} \sin \theta_2)^2 + (I_2 R_{o2} \sin \theta_2 + I_2 X_{o2} \cos \theta_2)^2.$$

The phasor diagram is shown in Fig. 3.14.

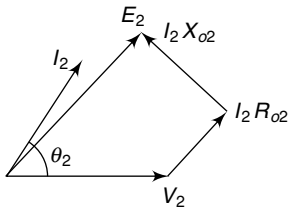


Fig. 3.14 ***Phasor diagram of transformer for leading power factor load***

Now ($I_2 R_{o2} \sin \theta_2 + I_2 X_{o2} \cos \theta_2$) is very small compared to ($V_2 + I_2 R_{o2} \cos \theta_2 - I_2 X_{o2} \sin \theta_2$). Hence ($I_2 R_{o2} \sin \theta_2 + I_2 X_{o2} \cos \theta_2$) is neglected.

$\therefore\ E_2 = V_2 + I_2 R_{o2} \cos \theta_2 - I_2 X_{o2} \sin \theta_2$

or $E_2 - V_2 = I_2 R_{o2} \cos \theta_2 - I_2 X_{o2} \sin \theta_2$ (3.17)

Percentage voltage regulation is

$$\frac{E_2 - V_2}{E_2} \times 100\% = \left(\frac{I_2 R_{o2}}{E_2} \cos \theta_2 - \frac{I_2 X_{o2}}{E_2} \sin \theta_2 \right) \times 100\% \qquad (3.18)$$

$$= (R_{\text{p.u}} \cos \theta_2 - X_{\text{p.u}} \sin \theta_2) \times 100\% \qquad (3.19)$$

3.12 CONDITION FOR ZERO (MINIMUM) REGULATION

We can use the expression of regulation to find the condition for which the regulation is zero. We can write at zero regulation,

$$I_2 R_{o2} \cos \theta_2 + I_2 X_{o2} \sin \theta_2 = 0$$

or $$\tan \theta_2 = -\frac{R_{o2}}{X_{o2}}. \qquad (3.20)$$

The negative sign in the above condition indicates that zero regulation is possible at a leading power factor. Also, if the transformer is not loaded at all, $E_2 = V_2$ and this also gives zero regulation. Thus the regulation is zero if the transformer is open circuited or operated at a leading p.f. so that $\theta_2 = \tan^{-1} \frac{R_{o2}}{X_{o2}}$.

Also from the expression of regulation, it is evident that for a leading power factor load if the magnitude of θ_2 is high, the magnitude of ($I_2 X_{o2} \sin \theta_2$) would become more than that of ($I_2 R_{o2} \cos \theta_2$). The regulation then may become negative. It means, on increasing the load the terminal voltage increases at leading power factor operation of the transformer.

3.12.1 Condition for Maximum Regulation

We can derive the condition for maximum regulation using the expression for regulation. The regulation will be maximum if the differentiation of regulation with respect to phase angle θ_2 is equal to zero. That is

$$\frac{d}{d\theta_2} = (I_2 R_{o2} \cos \theta_2 + I_2 X_{o2} \sin \theta_2) = 0$$

or $$- I_2 R_{o2} \sin \theta_2 + I_2 X_{o2} \cos \theta_2 = 0$$

or $$\tan \theta_2 = \frac{X_{o2}}{R_{o2}}. \qquad (3.21)$$

Hence maximum regulation occurs only at lagging power factor and when $\theta_2 = \tan^{-1} \frac{X_{o2}}{R_{o2}}$.

3.9 A single-phase transformer has 200 and 100 turns respectively in its secondary and primary windings. The resistance of the primary winding is 0.05 Ω and that of the secondary is 0.3 Ω. Find the resistance of (i) the primary winding referred to the secondary, (ii) the secondary winding referred to the primary. Also find the equivalent resistance of the transformer referred to the primary.

Solution

Number of turns of primary winding $N_1 = 100$
Number of turns of secondary winding $N_2 = 200$
Resistance of primary winding $R_1 = 0.05\ \Omega$
Resistance of secondary winding $R_1 = 0.3\ \Omega$

(i) Resistance of primary winding referred to secondary

$$= R_1' = R_1 \left(\frac{N_2}{N_1}\right)^2 = 0.05 \times \left(\frac{200}{100}\right)^2 = 0.05 \times 4 = 0.2\ \Omega.$$

(ii) Resistance of secondary winding referred to primary

$$R_2' = R_2 \times \left(\frac{N_1}{N_2}\right)^2 = 0.3 \times \left(\frac{100}{200}\right)^2 = \frac{0.3}{4}\ \Omega = 0.075\ \Omega$$

Equivalent resistance of the transformer referred to the primary

$$R_{01} = R_1 + R_2' = 0.05 + 0.075 = 0.125\ \Omega.$$

[Also, $R_{02} = R_2 + R_1' = 0.3 + 0.2 = 0.5\ \Omega$].

3.10 A 20 kVA, 1000/200 V single-phase transformer has a primary resistance of 1 Ω and a secondary resistance of 0.2 Ω. Find the equivalent resistance of the transformer referred to the secondary and the total resistance drop on full load.

Solution

If N_1 and N_2 be the number of turns of the primary and secondary winding then $\frac{N_1}{N_2} = \frac{1000}{200}$.

Resistance of the primary winding $R_1 = 1\ \Omega$.
Resistance of the secondary winding $R_2 = 0.2\ \Omega$.
Total equivalent resistance in terms of the secondary winding is $(R_1' + R_2)$

i.e. $$R_{o2} = R_1 \left(\frac{N_2}{N_1}\right)^2 + R_2 = 1 \times \left(\frac{200}{1000}\right)^2 + 0.2 = 0.04 + 0.2 = 0.24\ \Omega.$$

Full load secondary current

$$I_2 = \frac{20 \times 10^3}{200} = 100 \text{ A.}$$

Total resistance drop on full load = $I_2 R_{o2} = 100 \times 0.24 = 24$ V.

3.11 A single-phase transformer has turns ratio of 8. The resistances of the high voltage and low voltage windings are 1.5 Ω and 0.05 Ω respectively and the reactances are 10 Ω and 0.5 Ω respectively. Find (i) the voltage to be applied to the high voltage side to obtain a full load current of 100 A on the low voltage winding on short circuit and (ii) the power factor on short circuit.

Solution

If N_H and N_L be the number of turns on the high voltage and low voltage windings then $\frac{N_H}{N_L} = 8$ (given).

Resistance of high voltage winding $R_H = 1.5$ Ω
Resistance of low voltage winding $R_L = 0.05$ Ω
Reactance of high voltage winding $X_H = 10$ Ω
Reactance of low voltage winding $X_L = 0.5$ Ω
Full load current on the low voltage side = 100 A.

$\therefore$ full load current on the high voltage side $= 100 \times \frac{N_L}{N_H} = \frac{100}{8} = 12.5$ A.

Equivalent impedance referred to the high voltage side

$$= (R_H + R_L') + j(X_H + X_L')$$
$$= \{1.5 + 0.05(8)^2\} + j\{10 + 0.5(8)^2\} = 4.7 + j42 = 42.26\angle 83.6° \text{ Ω.}$$

(i) The voltage to be applied to the high voltage side to obtain full load current is 12.5 × 42.26 = 528.25 V

(ii) Power factor on short circuit is cos 83.6° = 0.111.

3.12 A 6600/440 V, 50 Hz single-phase transformer has high voltage and low voltage winding resistances of 0.5 Ω and 0.0007 Ω respectively and reactances of 2 Ω and 0.001 Ω respectively. Find the current and the input power when the high voltage winding is connected to a 220 V 50 Hz supply, the low voltage being short circuited.

Solution

$$\frac{N_H}{N_L} = \frac{6600}{440}, \qquad R_H = 0.5 \text{ Ω}, \qquad R_L = 0.0007 \text{ Ω},$$
$$X_H = 2 \text{ Ω}, \qquad X_L = 0.001 \text{ Ω}.$$

Equivalent impedance referred to the high voltage side

$$Z_{eH} = R_H + R_L\left(\frac{N_H}{N_L}\right)^2 + j\left\{X_H + X_L\left(\frac{N_H}{N_L}\right)^2\right\}$$
$$= 0.5 + 0.0007\left(\frac{6600}{440}\right)^2 + j\left\{2 + 0.001\left(\frac{6600}{440}\right)^2\right\}$$
$$= 0.6575 + j2.225 = 2.32\angle 73.54° \text{ Ω.}$$

$\therefore$ Current in the high voltage side when low voltage is short circuited is $\frac{220}{2.32}$ A = 94.83 A.

Input power = 220 × 94.83 cos 73.54° = 5911 W = 5.91 kW.

3.13 The equivalent impedance of a 10 kVA, 220/440 V, single-phase, 50 Hz transformer referred to the low voltage side is $(0.2 + j0.5)\ \Omega$. The core loss resistance and magnetizing reactance are 100 Ω and 150 Ω respectively, both referred to the low voltage side. If the high voltage current is 20 A at a lagging p.f. of 0.8 find the low voltage input current and the high voltage terminal voltage.

Solution

$$\left.\begin{aligned} R_{OL} &= 0.2\ \Omega \\ X_{OL} &= 0.5\ \Omega \end{aligned}\right\} \text{[Low voltage side resistance and reactance]}$$

$$\left.\begin{aligned} R_O &= 100\ \Omega \\ X_O &= 150\ \Omega \end{aligned}\right\} \text{[Magnetizing branch resistance and reactance at low voltage side]}$$

$\therefore \quad Z_{OL} = 0.5385\angle 68.2°\ \Omega.$

High voltage current $(I_H) = 20\angle -\cos^{-1}0.8 = 20\angle -36.86°$ V

The high voltage current referred to low voltage side $= I'_H = 20 \times \dfrac{440}{220} = 40$ A.

$$\text{The no load component of current } (I_O) = \frac{220}{100} - j\frac{220}{150}$$
$$= (2.2 - j1.47) \text{ A}$$
$$\text{Input current on the low voltage side} = 40(0.8 - j0.6) + 2.2 - j1.47$$
$$= 34.2 - j25.47$$
$$= 42.64\angle -36.67° \text{ A.}$$
$$\text{High voltage side terminal voltage } (V_2) = \{220 - 42.64\angle -36.67°(0.2 + j0.5)\}\frac{440}{220}$$
$$= \{220 - 42.64(0.8 - j0.6)(0.2 + j0.5)\}\frac{440}{220}$$
$$= \{220 - 42.64(0.46 + j0.28)\}\frac{440}{220}$$
$$= (200.38 - j11.94\} \times 2 = 401.47\angle -3.41° \text{ V.}$$

3.14 A 500 kVA, single-phase, 2000/200 V, 50 Hz. transformer has a high voltage resistance 0.2 Ω and a leakage reactance of 0.4 Ω. The low voltage winding resistance is 0.002 Ω and the leakage reactance is 0.008 Ω. Find (i) the equivalent winding resistance and reactance referred to the high voltage side and the low voltage side, (ii) the equivalent resistance and equivalent reactance drops in volts and in percent of the rated winding voltages expressed in terms of high voltage quantities.

Solution

(i) Equivalent winding resistance referred to the high voltage side

$$R_{o1} = R_1 + R_2\left(\frac{N_1}{N_2}\right)^2 = 0.2 + 0.002 \times \left(\frac{2000}{200}\right)^2 = 0.2 + 0.2 = 0.4\ \Omega.$$

Equivalent reactance referred to the high voltage side

$$X_{o1} = X_1 + X_2\left(\frac{N_1}{N_2}\right)^2 = 0.4 + 0.008 \times \left(\frac{2000}{200}\right)^2 = 0.4 + 0.8 = 1.2\ \Omega.$$

Equivalent resistance referred to low voltage side

$$R_{o2} = R_2 + R_1\left(\frac{N_2}{N_1}\right)^2 = 0.002 + 0.2 \times \left(\frac{200}{2000}\right)^2 = 0.002 + 0.002 = 0.004\ \Omega.$$

Equivalent reactance referred to low voltage side

$$X_{o2} = X_2 + X_1\left(\frac{N_2}{N_1}\right)^2 = 0.008 + 0.4 \times \left(\frac{200}{2000}\right)^2 = 0.008 + 0.004 = 0.012\ \Omega.$$

(ii) Equivalent resistance drop referred to the high voltage side $= I_1 R_{o1} = \dfrac{500 \times 10^3}{2000} \times 0.4 = 250 \times 0.4 = 100$ V.

Percent equivalent resistance drop $= \dfrac{I_1 R_{o1}}{V_1} \times 100\% = \dfrac{100}{2000} \times 100\% = 5\%$.

Equivalent reactance drop referred to the low voltage side

$$I_1 X_{o1} = \frac{500 \times 10^3}{2000} \times 1.2 = 250 \times 1.2 = 300\ \text{V}$$

Percent equivalent reactance drop

$$\frac{I_1 X_{o1}}{V_1} \times 100\% = \frac{300}{2000} \times 100\% = 15\%.$$

3.15 A 5 kVA 440/220 V single-phase transformer has a primary and secondary winding resistance of 2 Ω and 0.8 Ω respectively. The primary and secondary reactances are 10 Ω and 1.5 Ω respectively. Find the secondary terminal voltage at full load, 0.8 p.f. lagging.

Solution

If V_2 be the secondary terminal voltage at full load and E_2 the secondary terminal voltage at no load then

$$E_2 = V_2 + I_2 R_{o_2} \cos\theta_2 + I_2 X_{o_2} \sin\theta_2$$

or $$V_2 = E_2 - I_2 R_{o2}(0.8) - I_2 X_{o2}(0.6)$$

$$R_{o2} = 2 \times \left(\frac{220}{440}\right)^2 + 0.8 = 0.5 + 0.8 = 1.3\ \Omega$$

$$X_{o2} = 10 \times \left(\frac{220}{440}\right)^2 + 1.5 = 2.5 + 1.5 = 4\ \Omega$$

$$I_2 = \frac{5 \times 10^3}{220} = 22.73\ \text{A}.$$

$\therefore$ $$V_2 = 220 - 22.73(1.3 \times 0.8 + 4 \times 0.6) = 220 - 22.73 \times 3.44 = 141.8\ \text{V}.$$

3.16 A 220/1100 V single phase transformer has a resistance of 0.6 Ω and leakage reactance of 1.5 Ω both referred to the high voltage side. Find the p.f. at which regulation is zero. The full load primary current is 30 A.

Solution

Full load secondary current $I_2 = 30 \times \dfrac{220}{1100} = 6$ A

$$R_{\text{p.u}} = \frac{I_2 R_{o2}}{E_2} = \frac{6 \times 0.6}{1100} = 0.0033$$

$$X_{\text{p.u}} = \frac{I_2 X_{o2}}{E_2} = \frac{6 \times 1.5}{1100} = 0.0082$$

Voltage regulation is ($R_{p.u}$ cos θ_2 + $X_{p.u}$ sin θ_2), where (cos θ_2) is the lagging p.f.
Hence, 0.0033 cos θ_2 + 0.0082 sin θ_2 = 0
or, tan θ_2 = –0.4024
i.e., cos θ_2 = 0.93 and the negative sign indicates leading p.f.
The regulation is zero at 0.93 p.f. leading.

3.17 A 40 kVA, 2500/500 V single phase transformer has the following parameters: R_1 = 8 Ω, R_2 = 0.5 Ω, X_1 = 20 Ω, X_2 = 0.8 Ω. Find the voltage regulation and the secondary terminal voltage at full load for a p.f. of 0.8 lagging. The primary voltage is held constant at 2500 V.

Solution

Equivalent resistance referred to low voltage side

$$R_{o2} = 0.5 + 8 \times \left(\frac{500}{2500}\right)^2 = 0.5 + 0.32 = 0.82\ \Omega$$

Equivalent reactance referred to low voltage side

$$X_{o2} = 0.8 + 20 \times \left(\frac{500}{2500}\right)^2 = 0.8 + 0.8 = 1.6\ \Omega$$

Full load secondary current $I_2 = \dfrac{40 \times 10^3}{500} = 80$ A

Voltage regulation = ($I_2\ R_{o2}$ cos θ_2 + $I_2\ X_{o2}$ sin θ_2)/E_2

$$= \frac{80}{500}\{0.82 \times (0.8) + 1.6 \times (0.6)\}$$

$$= \frac{129.28}{500} = 0.258 \text{ or } 25.8\%.$$

If V_2 be the secondary terminal voltage then

$$\frac{E_2 - V_2}{E_2} = 0.258 \quad \text{or,} \quad V_2 = (1 - 0.258)\ 500 = 371 \text{ V.}$$

3.18 A 2000/400 V single phase transformer has an equivalent resistance of 0.03 p.u. and an equivalent reactance of 0.08 p.u. Find the full load voltage regulation at 0.8 p.f. lag if the primary voltage is 1500 V. Find also the secondary terminal voltage at full load.

Solution

$$\text{Voltage regulation} = \frac{E_2 - V_2}{E_2} = R_{p.u.} \cos \theta_2 + X_{p.u.} \sin \theta_2$$

or,
$$\frac{E_2 - V_2}{E_2} = 0.03 \times 0.8 + 0.08 \times 0.6 = 0.072$$

So, voltage regulation is 0.072 or, 7.2%.

When primary voltage is 1500 V secondary voltage is $1500 \times \dfrac{400}{2000} = 300$ V at no load or, E_2 = 300 V. Hence, secondary terminal voltage $V_2 = E_2(1 - 0.072) = 300 \times 0.928 = 278.4$ V.

3.13 LOSSES AND EFFICIENCY OF TRANSFORMER

Like any other machine, the *efficiency* of a transformer is defined as

$$\eta = \frac{\text{Power output}}{\text{Power input}}$$

$$= \frac{\text{Power output}}{\text{Power output + Power losses in the transformer}}$$

To find the efficiency, we are to know various types of losses. There are two types of losses in a transformer:

(a) *Copper losses* (or I^2R *losses* or *ohmic losses*) in the primary and secondary windings.

(b) *Iron losses* (or *core losses*) in the core. This again has two components:

(i) *hysteresis losses* and (ii) *eddy current losses*.

The copper losses (P_C) also have two components: (i) the primary winding copper loss, and (ii) the secondary winding copper loss.

$$\therefore \quad \text{Copper losses, } (P_C) = I_1^2 R_1 + I_2^2 R_2$$

$$= I_1^2 R_1 + I_1^2 R_2' = I_1^2 R_{o_1}$$

Also,
$$P_C = I_2^2 R_2 + I_2^2 R_1' = I_2^2 R_{o_2} \tag{3.22}$$

(For correct determination of copper losses, the winding resistance should be determined at the operating temperature of windings.)

When alternating current flows through the windings, the core material undergoes cyclic processes of magnetisation and demagnetisation.

This process is called *hysteresis*.

The hysteresis losses (in watts) is given as,

$$P_h = K_h B_m^n f v \tag{3.23}$$

where, K_h = hysteresis coefficient whose value depends upon the material (K_h is 0.025 for cast steel, 0.001 for silicon steel and 0.0001 for permalloy)

B_m = maximum flux density (in tesla)

n = a constant, $1.5 \le n \le 2.5$ depending upon the material

f = frequency (in hertz)

v = volume of the core material (in m^3)

The eddy currents are the circulating currents set up in the core. These are produced due to magnetic flux being cut by the core. The loss due to these eddy currents is called *eddy current losses*. This loss (in watts) is given by

$$P_e = K_e B_m^2 f^2 t^2 v \tag{3.24}$$

where K_e = constant dependent upon the material

t = thickness of laminations (in metre)

A comparison of the expressions of hysteresis and eddy current losses reveals that the eddy-current loss varies as the square of the frequency, whereas the hysteresis loss varies directly with the frequency. The hysteresis losses can be minimised by selecting suitable ferromagnetic material for the core. The eddy-current losses can be minimised by using thin laminations in building the core.

The total iron losses (P_i) is given as

$$P_i = P_h + P_e$$

The efficiency of the transformer in thus given as

$$\eta = \frac{\text{Power output}}{\text{Power input}} = \frac{P_o}{P_o + P_c + P_i}$$

$$= \frac{V_2 I_2 \cos \phi_2}{V_2 I_2 \cos \theta_2 + I_2^2 R_{02} + P_i} \tag{3.25}$$

3.14 CONDITION FOR MAXIMUM EFFICIENCY

Dividing the numerator and denominator in the above expression of efficiency by (I_2), we get

$$\eta = \frac{V_2 \cos \theta_2}{V_2 \cos \theta_2 + I_2 R_{02} + P_i / I_2}$$

The transformer being operating at constant terminal voltage and constant power factor, we know the value of (I_2) at which the efficiency is maximum. Obviously, the efficiency will be maximum when ($I_2 R_{o2} + P_i/I_2$) is a minimum. (η) is maximum when its first derivative with respect to I_2 is zero.

i.e, $$\frac{d}{dI_2}\left(I_2 R_{02} + \frac{P_i}{I_2}\right) = 0$$

or $$R_{o_2} - \frac{P_i}{I_2^2} = 0$$

or $$I_2^2 R_{o_2} = P_i \tag{3.26}$$

Thus, the efficiency at a given terminal voltage and load power factor is maximum for such a load current (I_2) which makes copper losses equal to the constant iron losses.

3.15 EXPRESSION FOR LOAD AT WHICH EFFICIENCY IS MAXIMUM

Let I_{2fl} = Full load secondary current
I_{2m} = secondary current when efficiency is maximum
R_{o2} = equivalent resistance referred to the secondary
P_i = core loss

Full load copper losses = $I_{2\,fl}^2 R_{o\,2} = P_{cfl}$

Copper losses (when efficiency is maximum) are, $I_{2m}^2 R_{o\,2}$ $(= P_{cfl})$

So, $$I_{2m}^2 = \frac{P_C}{R_{o\,2}} = \frac{I_{2fl}^2 P_C}{I_{2\,fl}^2 R_{o\,2}} = \frac{I_{2\,fl}^2 P_C}{P_{cfl}}$$

or, $$I_{2m} = I_{2\,fl}\sqrt{\frac{P_C}{P_{cfl}}} = I_{2\,fl}\sqrt{\frac{P_i}{P_{cfl}}} \tag{3.27}$$

Current at maximum efficiency = current at full load $\times \left(\sqrt{\dfrac{\text{Core loss}}{\text{Full load copper loss}}} \right)$

Now, $$V_2 I_{2m} = V_2 I_{2fl} \sqrt{\frac{P_C}{P_{cfl}}} = I_{2fl} \sqrt{\frac{P_i}{P_{cfl}}} \tag{3.28}$$

or, (VA) output at maximum efficiency

$$= \text{full load } (VA) \text{ output} \times \sqrt{\frac{\text{Core loss}}{\text{Full load copper loss}}}$$

Hence, if the maximum efficiency occurs at n times the full load, then $n = \sqrt{(P_C / P_{cfl})}$. (3.28a)

Maximum efficiency $= \dfrac{nV_2 I_{fl} \cos\theta_2}{nV_2 I_{fl} \cos\theta_2 + 2P_C}$, where $(\cos\theta_2)$ is the load p.f.

3.19 In a 25 kVA, 2000/200 V transformer the iron and full load copper losses are 350 W and 400 W respectively. Find the efficiency at unity p.f. at (a) full load (b) half load. Determine the load for maximum efficiency.

Solution

$$\text{Efficiency} = \frac{\text{Output}}{\text{Input}} = \frac{\text{Output}}{\text{Output} + \text{Losses}}$$

(a) At full load and unity p.f.

$$\text{Output} = 25 \times 10^3 \times 1 = 25 \times 10^3 \text{ W}$$

$$\text{Losses} = 350 + 400 = 750 \text{ W}$$

$$\therefore \quad \text{efficiency} = \frac{25{,}000}{25{,}000 + 750} \simeq 0.97 \text{ or } 97\%$$

(b) At half load and unity p.f.

$$\text{Output} = 25 \times 10^3 \times \frac{1}{2} = 12.5 \times 10^3 \text{ W}$$

$$\text{Iron losses} = 350 \text{ W}$$

$$\text{Copper losses} = \left(\frac{1}{2}\right)^2 \times 400 = 100 \text{ W}$$

$$\text{Total losses} = 450 \text{ W}$$

$$\text{Efficiency} = \frac{12500}{12500 + 450} = 0.965 \text{ or } 96.5\%$$

If maximum efficiency occurs when load is (x) times the full load then copper losses $= (x^2 \times 400)$ W

As core losses = copper losses, under maximum efficiency condition then $(x^2 \times 400) = 350$, or $(x) = \sqrt{\dfrac{35}{40}} = 0.935$

Hence, load for maximum efficiency $= 0.935 \times 25$ kVA $= 23.375$ kVA.

3.20 Find the efficiency of a 150 kVA transformer at 25% full load at 0.8 p.f. lagging if copper losses are 1600 W at full load and iron losses are 1400 W.

Solution

Output at 25% full load and 0.8 p.f. lagging is

$150 \times 10^3 \times 0.25 \times 0.8 = 30{,}000$ W

Copper losses = $1600 \times (0.25)^2$ W = 100 W

Iron losses = 1400 W

Total losses = (100 + 1400) W = 1500 W

$$\therefore \quad \text{Efficiency} = \frac{\text{Output}}{\text{Output + Losses}} = \frac{30{,}000}{30{,}000 + 1500} = 0.9524 \text{ or } 95.24\%.$$

3.21 The efficiency of a 10 kVA, 2000/400 V single phase transformer at unity p.f. is 97% at rated load and also at half rated load. Determine the transformer core losses and ohmic losses.

Solution

$$\text{Efficiency} = \frac{\text{Output}}{\text{Input}} = \frac{(\text{Input} - \text{Loss})}{\text{Input}} = 1 - \frac{\text{Losses}}{\text{Input}}$$

At full load,

$$0.97 = 1 - \frac{\text{Core losses + Copper losses}}{\text{Output + Core losses + Copper losses}}$$

or $$0.97 = 1 - \frac{P_C + P_{cu}}{10 \times 10^3 \times 1 + P_c + P_{cu}}$$

or $$\frac{P_c + P_{cu}}{10000 + P_c + P_{cu}} = 0.03$$

or $$P_c + P_{cu} = 309.278 \text{ W}. \qquad \text{(i)}$$

At half load,

$$0.97 = 1 - \frac{P_c + \frac{1}{4}P_{cu}}{10 \times 10^3 \times \frac{1}{2} + P_c + \frac{1}{4}P_{cu}}$$

or $$P_c + \frac{1}{4}P_{cu} = 150 + 0.03\left(P_c + \frac{1}{4}P_{cu}\right)$$

or $$P_c + \frac{1}{4}P_{cu} = \frac{150}{0.97} = 154.639 \text{ W}. \qquad \text{(ii)}$$

Solving Eqs (i) and (ii)

$$P_{cu} = 206.185 \text{ W}$$

and $$P_c = 103.1 \text{ W}.$$

3.22 A 20 kVA, 2000/220 V single-phase transformer has a primary resistance of 2.1 Ω and a secondary resistance of 0.026 Ω. If the total iron loss is 200 W find the efficiency on (i) full load and at a p.f. of 0.5 (lagging); (ii) half load and a p.f. of 0.8 (leading).

Solution

Iron losses = 200 W

$$\text{Full load primary current} = \frac{20{,}000}{2000} = 10 \text{ A}$$

$$\text{Full load secondary current} = \frac{20{,}000}{220} = 90.91 \text{ A}$$

Total copper losses at full load = $I_1^2 R_1 + I_2^2 R_2$
$= (10)^2 \times 2.1 + (90.91)^2 \times 0.026$
$= 210 + 214.88 = 424.88$ W.

(i) Output at full load and 0.5 p.f. lag $= 20 \times 10^3 \times 0.5 = 10{,}000$ W
Input = Output + Iron losses + Copper losses
$= 10{,}000 + 200 + 424.88 = 10{,}624.88$ W.

So, efficiency $= \dfrac{\text{Output}}{\text{Input}} = \dfrac{10{,}000}{10{,}624.88} = 0.941 = 94.1\%$.

(ii) Output at half load at 0.8 p.f. leading $= 20 \times 10^3 \times \dfrac{1}{2} \times 0.8 = 8000$ W.

Copper loss at half load $= 424.88 \times \left(\dfrac{1}{2}\right)^2 = 106.22$ W

Input $= 8000 + 106.22 + 200 = 8306.22$ W

Efficiency $= \dfrac{8000}{8306.22} = 0.963 = 96.3\%$.

3.23 The primary resistance of a 440/110 V single-phase transformer is 0.28 Ω and the secondary resistance is 0.018 Ω. If the iron losses is measured to be 160 W when the rated primary voltage is applied, find the kW loading to give maximum efficiency at unity p.f.

Solution

Let at (x) times the full load the efficiency is maximum. If P_{cu} is the copper losses at full load, then $x^2 P_{cu} = 160$, as copper losses = iron losses when efficiency is maximum.

Now ($x^2 I_2^2 R_{o_2}$) = 160 where I_2 is the full load secondary current and R_{o2} is the equivalent resistance referred to secondary.

Now $R_{o2} = R_1 \left(\dfrac{N_2}{N_1}\right)^2 + R_2 = 0.28 \times \left(\dfrac{110}{440}\right)^2 + 0.018$
$= 0.0175 + 0.018 = 0.0355\ \Omega$

$\therefore \quad xI_2 = \sqrt{\dfrac{160}{0.0355}}\ \text{A} = 67.13\ \text{A}$

The loading at unity p.f. is $= \dfrac{110 \times 67.13 \times 1}{10^3} = 7.38$ kW.

3.24 A single-phase transformer supplies a load of 20 kVA at a p.f. of 0.81 (lagging). The iron loss of the transformer is 200 W and the copper losses at this load is 180 W. Calculate (i) the efficiency (ii) if the load is now changed to 30 kVA at a p.f. of 0.91 (lagging), calculate the new efficiency.

Solution

Iron loss = 200 W
Copper loss at a load of 20 kVA is = 180 W.

(i) Output of 0.81 p.f. (lag) $= 20 \times 10^3 \times 0.81 = 16200$ W
Total losses = 200 + 180 = 380 W
Input = Output + Losses = 16200 + 380 = 16580 W

Efficiency $= \dfrac{\text{Output}}{\text{Input}} = \dfrac{16200}{16580} = 0.977 = 97.7\%$.

(b) New load is 30 kVA at 0.91 p.f. (lag)
Output = $30 \times 10^3 \times 0.91 = 27300$ W

Copper losses at a load of 30 kVA is, $P_{cu} = 180 \times \left(\frac{30}{20}\right)^2 = 180 \times \frac{9}{4} = 405$ W

Input = Output + Losses = 27300 + 200 + 405 = 27905 W

Efficiency = $\frac{27300}{27905} = 0.978 = 97.8\%$

3.25 The ohmic resistance of the primary and secondary windings of a 27.5 kVA, 450/112 V single-phase transformer are 0.055 Ω and 0.00325 Ω respectively. At the rated supply voltage the iron losses are 170 W. Calculate (i) the full load efficiency at a p.f. of 0.8 lagging, (ii) the kVA output at which efficiency is a maximum at a p.f. of 0.8 (lagging), (iii) the value of maximum efficiency at a p.f. of 0.8 (lagging).

Solution

Full load primary current $I_1 = \frac{27.5 \times 10^3}{450} = 61.1$ A.

Full load secondary current $I_2 = \frac{27.5 \times 10^3}{112} = 245.53$ A.

Primary copper losses at full load = $(61.1)^2 \times 0.055 = 205.326$ W.
Secondary copper losses at full load = $(245.53)^2 \times 0.00325 = 195.93$ W.
Total copper losses at full load = (205.326 + 195.93) W = 401.26 W.
Iron losses = 170 W.

(i) Full load efficiency at a p.f. of 0.8 lag

$$= \frac{\text{Output}}{\text{Output + Total Losses}} = \frac{27.5 \times 10^3 \times 0.8}{27.5 \times 10^3 \times 0.8 + 401.26 + 170} \simeq 0.975 = 97.5\%.$$

(ii) Let maximum efficiency occurs when load is (x) times the full load. As core losses = copper losses under this condition,
$\therefore\ x^2 \times 401.26 = 170$ or, $x = 0.65$
kVA output under this condition is = $0.65 \times 27.5 \simeq 17.9$.

(iii) Maximum efficiency = $\frac{17.9 \times 10^3 \times 0.8}{17.9 \times 10^3 \times 0.8 + 170 + (0.65)^2 \times 401.25}$

$= \frac{14320}{14659.5} = 0.9768 = 97.68\%$.

3.16 TESTING OF TRANSFORMERS

The efficiency and regulation of a transformer are calculated by two types of tests, called *open circuit test* and *short circuit test*.

3.16.1 Open Circuit Test

This test is performed to measure the iron losses. The no-load current components I_w and I_m are measured from the open circuit test. From these, R_o (core loss resistance) and X_o (magnetizing reactance) parameters of equivalent circuit can be calculated.

One of the windings of a transformer is open-circuited. The rated voltage at rated frequency is applied to the other winding. Generally the HT side is kept open-circuited and the rated voltage is fed to the LT winding.

The connections are made as shown in Fig. 3.15. The rated voltage is supplied through an auto-transformer (also called *variac*). The readings of the wattmeter, voltmeter and ammeter are noted. Let W_o, V_1 and I_o be their readings. Since the secondary is open circuited a very small current called the no load current flows in the primary. The ammeter reads no load current I_o. As I_o is very small so the ohmic loss which is proportional to the square of the current can be neglected.

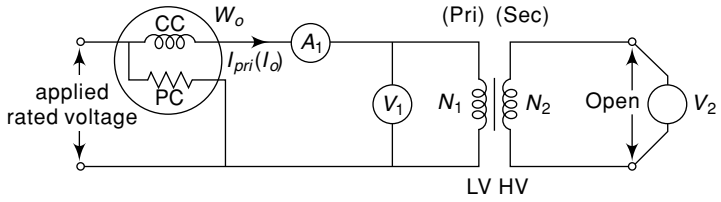


Fig. 3.15 ***Circuit diagram for open circuit test***

So, Iron losses, $$P_i = W_o - \frac{V_1^2}{r_p} - I_o^2 r_1 \tag{3.29}$$

where r_p = resistance of potential circuit of wattmeter
r_1 = resistance of transformer winding connected to supply.

Since the terms V_1^2/r_p and $I_o^2 r_1$ are very small, the wattmeter reading W_o can be assumed to give the iron losses.

If I_w and I_m be the core loss component and magnetizing component of the no load current I_o and cos θ_o is the no load power factor, then

$$P_i = \mathrm{W}_o = V_1 I_o \cos \theta_o$$

or $$\cos \theta_o = \frac{W_o}{V_1 I_o} \tag{3.30}$$

$\therefore$ $I_w = I_o \cos \theta_o$ and $I_m = I_o \sin \theta_o$

$$R_o = \frac{V_1}{I_w} \quad \text{and} \quad X_o = \frac{V_1}{I_m}.$$

3.16.2 Short Circuit Test

This test is carried out to determine the equivalent resistance and the leakage reactance of the transformer. The connections are made as shown in the Fig. 3.16. The LT winding is short-circuited. A low voltage is applied to HT side using an auto-transformer. This voltage is adjusted in such a way that the full-load current flows through the HT and LT windings. Since low voltage is applied the iron loss which is proportional to the square of the applied voltage is negligibly small as compared to the copper loss. Therefore, the wattmeter reading gives the copper loss. Let the various readings be W_{sc}, V_{sc} and I_{sc}. Then

$$R_{OH} = W_{sc} / I_{sc}^2 \tag{3.31a}$$

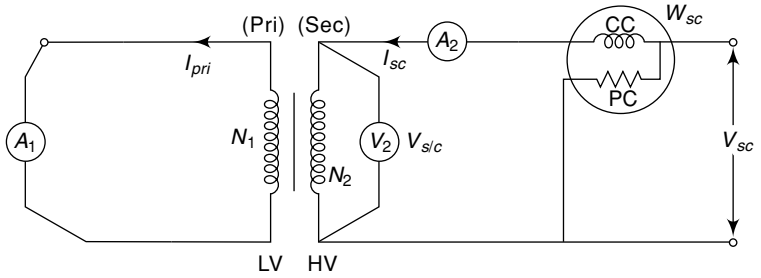


Fig. 3.16 *Circuit diagram for short circuit test.*

$$Z_{OH} = V_{sc}/I_{sc} \tag{3.31b}$$

$$X_{OH} = \sqrt{(Z_{oH})^2 - (R_{oH})^2} \tag{3.31c}$$

where, R_{OH} is the equivalent resistance, (X_{OH}) is the equivalent leakage reactance and Z_{OH} is the equivalent impedance referred to the h.v. winding. These parameters refer to the winding on which measurements are made, i.e. h.v. side. From these, the various parameters as referred to other winding i.e. l.v. winding can be calculated.

3.26 Calculate the values of R_o, X_o, R_1 and X_1 in the diagram shown in Fig. 3.17 of a single-phase 8 kVA, 22/440 V, 50 Hz transformer of which the following are the test results:

Open circuit test
220 V, 0.9 A, 90 W on the low voltage side.

Short circuit test
20 V, 15 A, 100 W on the high voltage side.

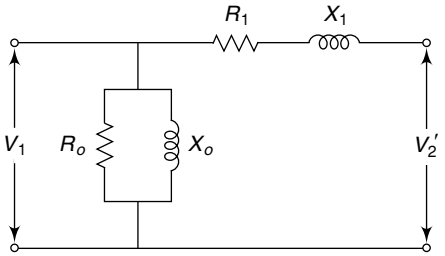


Fig. 3.17 *Circuit diagram for Example 3.26*

Solution

From the open circuit test data,

No load p.f. $\cos\theta_o = \dfrac{90}{220 \times 0.9} = 0.4545$

$\therefore \quad \sin\theta_o = 0.89$

Core loss resistance $R_o = \dfrac{V_1}{I_o \cos\theta_o} = \dfrac{220}{0.9 \times 0.4545}\ \Omega = 537.83\ \Omega$

Magnetizing reactance $X_o = \dfrac{V_1}{I_o \sin\theta_o} = \dfrac{220}{0.9 \times 0.89} = 274.65\ \Omega$

From short circuit test data,

$$R_{OH} = R_{o2} = \frac{100}{(15)^2}\ \Omega = 0.444\ \Omega$$

$$Z_{OH} = Z_{o2} = \frac{20}{15}\ \Omega = 1.33\ \Omega$$

where R_{o2} and Z_{o2} are the equivalent resistance and impedance referred to the high voltage side.

Hence, $X_{OH} = X_{o2} = \sqrt{(1.33)^2 - (0.44)^2} = 1.255\ \Omega$

Figure 3.17 shows the equivalent resistance R_1 and reactance X_1 referred to the low voltage side or primary side.

Hence, $R_1 = 0.444 \times \left(\frac{220}{440}\right)^2 = 0.111\ \Omega$

and $X_1 = 1.257 \times \left(\frac{220}{440}\right)^2 = 0.314\ \Omega$

Also $R_O = 537.83\ \Omega$ and $X_O = 274.65\ \Omega$.

3.27 Short circuit test performed on the h.v. side of a 100 kVA, 6600/440 V, single-phase transformer yields the following results: 100 V, 6 A, 200 W. If the low voltage side is delivering full load current at 0.8 p.f. lag and at 440 V find the voltage applied to the high voltage side.

Solution

From the short circuit test results

$$R_{O1} = \frac{200}{(6)^2}\ \Omega = 5.55\ \Omega$$

$$Z_{O1} = \frac{100}{6}\Omega = 16.67\ \Omega$$

$$X_{O1} = \sqrt{Z_{0_1}^2 - R_{0_1}^2} = 15.72\ \Omega$$

Secondary rated current $I_2 = \frac{100 \times 10^3}{440}$ A = 227.27 A.

If E_2 and V_2 be the secondary terminal voltage under no load and full load condition then

$$E_2 - V_2 = I_2 R_{O2} \cos \theta_2 + I_2 X_{O2} \sin \theta_2$$

Now, $R_{o2} = R_{O1} \times \left(\frac{440}{6600}\right)^2 = 5.55 \times \left(\frac{2}{30}\right)^2 = 0.0247\ \Omega$

and $X_{o2} = X_{O1} \times \left(\frac{440}{6600}\right)^2 = 15.71 \times \left(\frac{2}{30}\right)^2 = 0.0699\ \Omega$

Hence $(E_2 - V_2) = 227.27\ (0.0247 \times 0.8 + 0.0698 \times 0.6)$ 14 V.

For $V_2 = 440$ V, $(E_2) = V_2 + 14 = 454$ V

Hence the voltage applied to the h.v. side is $\left(454 \times \frac{6600}{440}\right) = 6810$ V.

3.28 A 8 kVA, 440/2000 V, 50 Hz single-phase transformer gave the following test results:

No load test: 440 V, 0.8 A, 80 W.

Short circuit test: 50 V, 3 A, 20 W.

Calculate (i) the magnetizing current and the component corresponding to iron losses at normal voltage and frequency, (ii) the efficiency on full load at unity p.f., (iii) the secondary terminal voltage on full load at unity p.f.

Solution

(i) From no load test data,

No load p.f. $(\cos \theta_o) = \frac{80}{440 \times 0.8} = 0.227$

Iron loss component current = 0.8 (cos θ_o) = 0.8 × 0.227 = 0.182 A
Magnetising current = 0.8 (sin θ_o) = 0.8 × 0.974 = 0.779 A.

(ii) Iron loss = 80 W
As the secondary side is the h.v. side so a short circuit test is performed on the secondary side.

Rated current of the h.v. side $I_2 = \dfrac{8000}{2000} = 4$ A.

When current is 3 A the wattmeter reading is 20 W.
So, if rated current of 4 A flows through the high voltage winding the wattmeter reading = $20 \times \left(\dfrac{4}{3}\right)^2 = 35.55$ W.

So rated copper losses = 35.55 W.

Efficiency on full load at unity p.f. = $\dfrac{8 \times 10^3 \times 1}{8 \times 10^3 \times 1 + 35.55 + 80} = 0.9858$ or 98.58%.

(iii) From short circuit test data,

$$R_{O2} = \frac{20}{(3)^2} = 2.22\ \Omega,\ (Z_{O2}) = \frac{50}{3} = 16.67\ \Omega$$

and $(X_{O2}) = \sqrt{(16.67)^2 - (2.22)^2} = 16.52\ \Omega$.

If V_2 be the terminal voltage then,
$E_2 - V_2 = I_2 R_{O2} \cos \theta_2 + I_2 X_{O2} \sin \theta_2$, where E_2 is the secondary voltage under no load condition and cos θ_2 is the load p.f. which is unity in this case.

$\therefore$ $(2000 - V_2) = 4(2.22 \times 1 + 16.52 \times 0)$

or $(V_2) = 2000 - 8.88 = 1991.12$ V.

3.29 The following results were obtained in tests on a 50 kVA, single-phase, 3300/400 V transformer.
Open circuit test: 3300 V, 430 W
Short circuit test: 124 V, 15.3 A, 535 W.
(supply given on h.v. side)
Calculate (i) the efficiency at full load and half full load both at 0.707 p.f. lagging, (ii) the regulation at full load for p.f. of 0.707 (lagging and leading) and (iii) full load terminal voltage under the condition of 0.707 p.f. (lagging).

Solution

For short circuit test data,

$$Z_{O1} = \frac{124}{15.3}\ \Omega = 8.10\ \Omega,\ R_{O1} = \frac{535}{(15.3)^2}\ \Omega = 2.285\ \Omega$$

$$X_{O1} = \sqrt{(8.1)^2 - (2.285)^2} = 7.77\ \Omega$$

(i) Rated current on the h.v. side = $\dfrac{50{,}000}{3300}$ A = 15.15 A

So, rated copper loss = $535 \times \left(\dfrac{15.15}{15.3}\right)^2 = 524.56$ W

Iron loss = 430 W
Efficiency at full load and 0.707 p.f. lagging

$$= \frac{50 \times 10^3 \times 0.707}{50 \times 10^3 \times 0.707 + 524.56 + 430} = 0.9735 \text{ or } 97.35\%.$$

Efficiency at half load and 0.707 p.f. lagging is

$$= \frac{50\times10^3\times0.707\times\frac{1}{2}}{50\times10^3\times(0.707)\times\frac{1}{2}+\left(\frac{1}{2}\right)^2\times524.56+430} = 0.9623 \text{ or } 96.23\%.$$

(ii) Voltage regulation at full load and 0.707 lagging p.f. is

$$= \frac{I_1 R_{01}\cos\theta + I_1 X_{01}\sin\theta}{E_1} = \frac{15.15\,(2.285\times0.707+7.77\times0.707)}{3300}$$

$$= 0.0326 = 3.26\%$$

Voltage regulation at full load and 0.707 p.f. leading

$$= \frac{I_1 R_{01}\cos\theta - I_1 X_{01}\sin\theta}{E_1} = \frac{15.15\,(2.285\times0.707-7.77\times0.707)}{3300}$$

$$= (-0.0178) \text{ or } (-1.78\%).$$

(iii) If V_2 is the terminal voltage at 0.707 p.f. lagging

$$\left[\frac{400-V_2}{400}\right] = 0.0326 \text{ or, } V_2 = 400\ (1-0.0326)\ \text{V} = 386.96\ \text{V}.$$

3.17 SINGLE-PHASE AUTO TRANSFORMER

An auto transformer is a single winding transformer in which a part of the winding is common to both the high voltage and low voltage side. Figure 6.18 shows a step down auto transformer. The primary winding AB has N_1 number of turns and the secondary winding BC has N_2 number of turns. The winding BC is common to both the primary and secondary. The induced emf in the primary winding AB is E_1 and in the secondary winding BC is E_2. Hence $\frac{E_1}{E_2}=\frac{N_1}{N_2} = K$, where K is the turns ratio. The input current is I_1 and the load current is I_2. The mmfs I_1N_1 and I_2N_2 will be equal and opposite. If terminal C is a sliding contact, the output voltage V_2 can be varied. The voltampere delivered to the load $V_2 I_2 = V_2 I_1 + V_2(I_2 - I_1)$. $(V_2\ I_1)$ is the voltamperes transferred conductively to the load through winding AC and $V_2(I_2 - I_1)$ is the voltamperes transferred inductively to the load through winding BC which represents the rating of the equivalent two winding transformer.

Hence,
$$\frac{\text{Output VA of auto transformer}}{\text{Output VA of equivalent a two-winding transformer}}$$

$$= \frac{V_2 I_2}{V_2\,(I_2 - I_1)} = \frac{a}{a-1} \tag{3.32}$$

Figure 3.19 represents a step up auto transformer. Here input voltampere $V_1 I_1 = V_1 I_2 + V_1(I_1 - I_2)$.

Hence
$$\frac{\text{Output VA of auto transformer}}{\text{Output VA of equivalent two winding transformer}}$$

$$= \frac{V_1 I_1}{V_1(I_1 - I_2)} = \frac{a}{a-1} \tag{3.33}$$

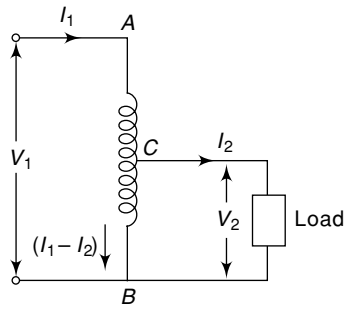


Fig. 3.18 *Step down auto transformer*

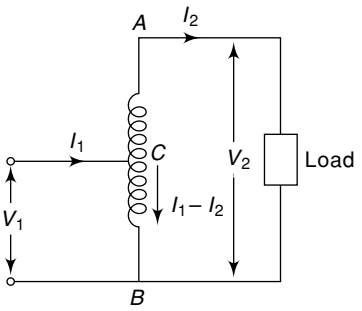


Fig. 3.19 *Step up auto transformer*

3.17.1 Adavantages of an Auto Transformer

(a) For the same capacity and voltage ratio, an auto transformer requires less winding material than a two-winding transformer. Hence there is saving in copper.
(b) An auto transformer is smaller in size and cheaper than a two winding transformer of same output.
(c) An auto transformer has higher efficiency since core loss and ohmic losses are smaller.
(d) Voltage regulation of an auto transformer is better because of reduced voltage drops in the resistance and ractance.
(e) An auto transformer has variable output voltage when a sliding contact is used for the secondary.

3.17.2 Disadvantages of an Auto Transformer

(a) There is direct connection between the high voltage and low voltage side. If there is an open circuit in the winding *BC* (Fig. 6.18) the full primary voltage would be applied to the secondary. This high voltage may cause serious damage to the equipments connected on the secondary side.
(b) The short circuit current is larger for an auto transformer due to reduced internal impedance.

3.17.3 Applications of Auto Transformers

(a) Auto transformers are used for obtaining continuously variable ac voltage.
(b) They are used for interconnections of power systems of different voltage levels.
(c) They are applied for boosting of ac mains voltage by a small amount.
(d) Auto transformers are used for starting the induction motors and synchronous motors.

3.18 TRANSFORMER COOLING

The core and copper losses cause heating of transformers. It is necessary to ensure that the temperature of the transformer does not exceed the maximum

value, otherwise it may cause damage to the insulation. The following are the methods for cooling these type of transformers.

(a) Air Natural Cooling Small transformers up to 25 kVA are cooled by natural circulation of air surrounding it.

(b) Air Blast Cooling In this type of cooling continuous blast of filtered air is forced through the core and windings for better cooling.

(c) Oil Natural Cooling A majority of transformers have their core and windings immeresed in oil. Oil is a good insulating material and provides better heat dissipation than air. Oil immersed transformers are enclosed in sheet steel tank. The heat produced in the transformer is passed to the oil. The oil is heated and it becomes lighter and rises to the top and its place is taken by cool air from the bottom of the tank.

The heat of the air is transferred to the tank by natural circulation of air. The heat is then transferred to the surrounding atmosphere.

(d) Oil Blast Cooling Here forced air is passed over cooling elements of transformer immersed in oil.

(e) Forced Oil and Forced Air Cooling Heated oil is taken from the top of the transformer tank to a cooling plant. Cooled oil is then circulated through the bottom of the tank.

(f) Forced Oil and Water Cooling In this type of cooling metallic tubes are situated inside the tank, below the oil level. Water is circulated through these tubes to extract heat from the oil.

3.19 CONSERVATOR AND BREATHER

A *conservator* is an air tight metallic drum supported on a transformer top cover. It takes up the expansion of oil with changes in temperature. When the oil is cold the tank is filled with oil. When the temperature of the oil rises, the oil expands and the expansion is taken up in the conservator. When the transformer cools, the level of oil goes down and the air is drawn in. The incoming air is passed through a device called breather for extracting moisture. A *breather* consists of a small vessel which contains a drying agent like silica gel or calcium chloride.

3.20 DISTRIBUTION TRANSFORMERS AND POWER TRANSFORMERS

Distribution transformers are used to step down the transmission voltage to a lower value suitable for distribution. They are kept in operation all 24 hours in a day whether they carry any load or not. They have better voltage regulation and small leakage reactance.

Power transformers are used in generating stations or substations at each end of transmission line for steping up or steping down the voltage. They are put in service during load periods and are disconnected during light load periods. They have greater leakage reactance and have maximum efficiency at or near full load.

3.21 NAME PLATE AND RATINGS

The specifications of transformers are given by BIS (Bureau of Indian Standard) 2026. As per this standard every transformer must be provided with the following specifications:

Type (power, distribution, auto, etc.), year of mannufacture, number of phases, rated kVA, rated frequency, rated voltage of each winding, connection symbol, percent impedance voltage at rated current, type of cooling, total mass, mass and volume of insulating oil.

3.22 ALL-DAY EFFICIENCY

It is usual for the primary of a transformer to be connected permanently to the supply and for the switching of load to be carried out in the secondary circuit. Since the copper loss varies with load but iron loss is constant and the efficiency depending on loading and losses vary througout the day. For transformers which are continuously excited but supply loads only intermittently, a low iron loss is particularly desirable, but a low copper loss is specially important where the load factor is high. Again for a transformer working on full load for greater part of the day, maximum efficiency should be arranged to occur some where around the full load value but for a transformer whose full load value may be supplied for only 1/4 of the day and the unit is only lightly loaded for the rest of the time, it would be desirable to arrange maximum efficiency to occur at about 1/2 full load value.

Considering the above factors the efficiency of a transformer is better estimated on an energy rather than a power ratio and thus we have the term "all day efficiency".

$$\text{All-day efficiency} = \frac{\text{Output in kWh for 24 hr.}}{\text{Input in kWh for 24 hr.}} \tag{3.34}$$

ADDITIONAL EXAMPLES

3.30 The core of a single-phase 3300/440 V, 50 Hz transformer is of square cross-section, each side being 140 mm. If the maximum flux density in the core is not to exceed 1*T*, find the number of turns required for each winding.

Solution

$$\text{Flux} = \text{Flux density} \times \text{Area}$$
$$= 1 \times (140 \times 10^{-3})^2 = 0.0196 \text{ Wb.}$$

If N_1 and N_2 be the number of turns of the primary and secondary windings respectively then,

$$3300 = 4.44 \times 0.0196 \times 50 \times N_1 \quad (\because E_1 = 4.44\ \phi_m f N_1)$$

or $$N_1 = 758.4 \quad \text{or,} \quad 758 \text{ (say)}$$

As $$\frac{N_1}{N_2} = \frac{E_1}{E_2}$$

So, $N_2 = N_1 \frac{E_2}{E_1} = 758 \times \frac{440}{3300} = 101.$

3.31 For the no load test on a transformer, the ammeter was found to read 0.18 A and the wattmeter 12 W. The reading on the primary voltmeter was 400 V and on the secondary voltmeter was 240 V. Calculate the magnetizing component of the no load current, the iron loss component and the transformation ratio.

Solution

Core loss or iron loss component of no load current $I_C = \dfrac{12}{400} = 0.03$ A.

No load current = 0.18 A

So magnetizing component of no load current = $\sqrt{(0.18)^2 - (0.03)^2} = 0.178$ A.

Transformation ratio = $\dfrac{400}{240} = \dfrac{5}{3} = 1.67{:}1$.

3.32 A single-phase transformer with a ratio of 440/200 V takes a no load current of 8 A at a p.f. of 0.25 (lagging). If the secondary supplies a current 220 A at a p.f. of 0.8 (lagging), estimate the current taken by the primary from the supply.

Solution

Secondary load current $I_2 = 220$ A

$\therefore$ load component of the primary current ($= I_1'$) $= I_2 \times \dfrac{N_2}{N_1} = 220 \times \dfrac{200}{440} = 100$ A.

No load component of the primary current $I_o = 8$ A.

Referring to Fig. 3.20, the horizontal and vertical components of I_1' are (I_1' sin θ) and (I_1' cos θ), where cos $\theta = 0.8$. Similarly, the horizontal and vertical components of I_o are (I_o sin θ_o) and (I_o cos θ_o) where cos $\theta_o = 0.25$. So, the horizontal component of the primary current

$= (I_1'$ sin $\theta + I_o$ sin $\theta_o)$

i.e. $I_{1H} = 100 \sin(\cos^{-1} 0.8) + 8 \sin(\cos^{-1} 0.25)$

$= 67.75$ A

Vertical component of the primary current

$I_{1V} = (I_1'$ cos $\theta + I_o$ cos $\theta_o)$

$= 100 \times 0.8 + 8 \times 0.25 = 82$ A.

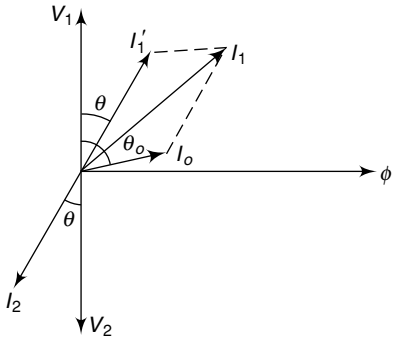


Fig. 3.20 ***Plot for Example 6.31***

So the total primary current $I_1 = \sqrt{(82)^2 + (67.75)^2} = 106.37$ A.

3.33 A 6600/440 V single-phase transformer has a primary resistance of 140 Ω and a secondary resistance of 0.25 Ω. Calculate the equivalent resistances referred to the secondary winding and primary winding respectively.

Solution

Primary resistance $R_1 = 140$ Ω

Secondary resistance $R_2 = 0.25$ Ω

Secondary resistance referred to primary $R_2' = 0.25 \times \left(\dfrac{N_1}{N_2}\right)^2$

$= 0.25 \times \left(\dfrac{6600}{440}\right)^2 = 56.25$ Ω.

So, equivalent resistance referred to primary

$$R_{o1} = r_1 + r_2' = 140 + 56.25 = 196.25\ \Omega$$

Now, primary resistance referred to secondary $R_1' = 140 \times \left(\frac{N_2}{N_1}\right)^2$

$$= 140 \times \left(\frac{440}{6600}\right)^2 = 0.6222\ \Omega.$$

So, equivalent resistance referred to secondary

$$R_{o2} = R_1' + R_2 = 0.622 + 0.25 = 0.872\ \Omega.$$

3.34 A 17.5 kVA, 460/115 V single-phase, 50 Hz transformer has primary and secondary resistances of 0.36 Ω and 0.02 Ω respectively and the leakage reactances of these windings are 0.82 Ω and 0.06 Ω respectively. Determine the voltage to be applied to the primary to obtain full load current with the secondary winding short circuited. Neglect the magnetizing current.

Full load primary current $I_1 = \frac{17500}{460} = 38.04$ A

$R_1 = 0.36\ \Omega$ and $R_2 = 0.02\ \Omega$

$X_1 = 0.82\ \Omega$ and $X_2 = 0.06\ \Omega$.

Equivalent resistance referred to the primary

$$R_{o1} = R_1 + R_2' = 0.36 + 0.02 \left(\frac{460}{115}\right)^2 = 0.68\ \Omega.$$

Equivalent reactance referred to the primary

$$X_{O1} = X_1 + X_2' = 0.82 + 0.06 \times \left(\frac{460}{115}\right)^2 = 1.78\ \Omega.$$

Equivalent impedance referred to the primary

$$Z_{O1} = \sqrt{(0.68)^2 + (1.78)^2} = 1.905\ \Omega.$$

As the secondary is short circuited the voltage applied to the primary to obtain full load current $= I_1 Z_{O1}$

$$= (38.04 \times 1.905) = 72.47\ \text{V}.$$

3.35 A transformer has 4% resistance and 6% reactance drop. Find the voltage regulation at full load (a) 0.8 p.f. lagging (b) 0.8 p.f. leading and (c) unity p.f.

Solution

(a) Regulation at 0.8 p.f. lagging $= R_{\text{p.u}} \cos \theta_2 + X_{\text{p.u}} \sin \theta_2$
$= 0.04 \times 0.8 + 0.06 \times 0.6$
$= 0.032 + 0.036 = 0.068$ or 6.8%.

(b) Regulation at 0.8 p.f leading $= R_{\text{p.u}} \cos \theta_2 - X_{\text{p.u}} \sin \theta_2$
$= 0.04 \times 0.8 - 0.06 \times 0.6$
$= 0.032 - 0.036 = -0.004$ or –0.4%.

(c) Regulation at unity p.f $(= R_{\text{p.u}} \cos \theta_2) = 0.04 \times 1 = 0.04$ or 4%.

3.36 A 10 kVA, 440/200 V, 50 Hz single phase transformer requires 100 V on h.v. side to circulate full load current with l.v. short circuited. The power input is 200 W. Find the maximum possible voltage regulation and p.f. at which it occurs. Also find the secondary terminal voltage under this condition.

Solution

Full load h.v. current = $\frac{10\times10^3}{440}$ A = 22.73 A.

Power input = 200 W = $(22.73)^2\ R_{o1}$

Hence R_{o_1} = 0.387 Ω.

Also $Z_{o_1} = \frac{100}{22.73}\ \Omega = 4.4\ \Omega$, hence $X_{o_1} = \sqrt{Z_{o1}^2 - R_{o1}^2}$ = 4.38 Ω.

Voltage regulation is ($R_{\text{p.u.}} \cos\theta_2 + R_{\text{p.u.}} \sin\theta_2$). Maximum voltage regulation occurs when

$$\frac{d}{d\theta_2}(R_{\text{p.u.}} \cos\theta_2 + X_{\text{p.u.}} \sin\theta_2) = 0$$

or, $$-R_{\text{p.u.}} \sin\theta_2 + X_{\text{p.u.}} \cos\theta_2 = 0$$

or, $$\tan\theta_2 = \frac{X_{\text{p.u.}}}{R_{\text{p.u.}}}$$

Now $$R_{\text{p.u.}} = \frac{0.387\times22.73}{440} = 0.02$$

and $$X_{\text{p.u.}} = \frac{4.38\times22.73}{440} = 0.226$$

Hence, $$\tan\theta_2 = \frac{0.226}{0.02} = 11.31$$ or, cos θ_2 is 0.088

i.e., Power factor is 0.088 lagging.

Hence maximum voltage regulation $= 0.02\times0.088 + 0.226\times0.996 = 0.227$ p.u. or, 22.7%.

If (V_2) be the terminal voltage then

$$1 - \frac{V_2}{E_2} = 0.227$$

or, $$V_2 = (1 - 0.227)\times200 = 154.6\ \text{V}$$

3.37 A 20 kVA, 2000/220 V single-phase transformer has a primary resistance of 2.1 Ω and a secondary resistance of 0.026 Ω. If the total iron loss equals 200 W, find the efficiency on (i) full load and at a p.f of 0.5 lagging (ii) half load and a p.f of 0.8 leading.

Solution

Iron loss = 200 W

Secondary current = $\frac{20\times10^3}{220}$ = 90.91 A

Equivalent resistance referred to the secondary

$$= 2.1\times\left(\frac{220}{2000}\right)^2 + 0.026 = 0.0514\ \Omega$$

Total copper losses = $(90.91)^2\times0.0514$ = 424.8 W

$$\text{Efficiency} = \frac{\text{Output}}{\text{Input}} = \frac{\text{Output}}{\text{Output + Losses}}$$

(i) Efficiency at full load and 0.5 lagging p.f.

$$= \frac{20\times10^3\times0.5}{20\times10^3\times0.5 + 200 + 424.8}\times100\% = 94.12\%.$$

(ii) Efficiency at half load and p.f. 0.8 leading

$$= \frac{20\times10^3\times0.8\times\frac{1}{2}}{20\times10^3\times0.8\times\frac{1}{2}+200+424.8\times\left(\frac{1}{2}\right)^2}\times 100\% = 96.3\%.$$

3.38 The primary resistance of a 440/110 V single-phase transformer is 0.28 Ω and the secondary resistance is 0.018 Ω. If the iron loss is measured to be 160 W when rated voltage is applied, find the kW loading to give maximum effeciency at unity p.f.

Solution

Iron loss = 160 W

For maximum efficiency, iron loss = Copper loss

So, $(I_2^2 R_{O2}) = 160$, where I_2 = Secondary full load current

and R_{O2} is the equivalent resistance referred to the secondary

Now, $R_{O2} = 0.28 \times \left(\frac{110}{440}\right)^2 + 0.018 = 0.0355\ \Omega$

So, $(I_2^2 \times 0.0355) = 160$ or, $I_2 = 67.13$ A

So, kW rating at unity p.f. $= \frac{V_2 I_2 \times 1}{10^3} = \frac{110\times67.13}{10^3} = 7.38.$

3.39 The core of a single-phase transformer has a cross-sectional area of 15000 mm^2 and the windings are chosen to operate the iron at a maximum flux density of 1.1 T from a 50 Hz. supply. If the secondary winding consists of 66 turns estimate the kVA output if the winding is connected to a load of 6 Ω impedance value.

Solution

Area $A = 15{,}000\ \text{mm}^2 = 0.015$ sqm

Flux density $B_m = 1.1\ \text{Wb/m}^2$

$f = 50$ Hz.

$N_2 = 66$

$E_2 = 4.44\ \phi_m f N_2 = 4.44\ B_m\ A f N_2$

$= 4.44 \times 1.1 \times 0.015 \times 50 \times 66 = 241.758$ V.

If load is 6 Ω the current $(I_2) = \frac{241.758}{6}$ A = 40.3 A

kVA output $= \left(\frac{E_2 I_2}{10^3}\right) = \frac{241.758\times40.3}{10^3} = 9.743.$

3.40 A 440/220 V single-phase transformer has a primary resistance of 0.29 Ω and a secondary resistance of 0.025 Ω. The corresponding reactance values are 0.44 Ω and 0.04 Ω. Estimate the primary current which would flow if a short circuit was to occur across the secondary terminals.

Solution

$$R_{O1} = 0.29 + 0.025 \times \left(\frac{440}{220}\right)^2 = 0.39\ \Omega$$

$$X_{O1} = 0.44 + 0.04 \times \left(\frac{440}{220}\right)^2 = 0.6\ \Omega$$

$$Z_{O1} = \sqrt{(0.39)^2 + (0.6)^2} = 0.7156\ \Omega$$

So, if a short circuit occurs across the secondary terminals

$$= \frac{440}{0.7156}\ \text{A} = 614.87\ \text{A}.$$

3.41 A 660/220 V single-phase transformer has a primary resistance of 0.3 Ω and a secondary resistance of 0.035 Ω. The corresponding reactance values are 0.5 Ω and 0.06 Ω. Estimate the percentage regulation for a secondary load current of 50 A at a p.f. of 0.8 (lagging).

Solution

$$R_{O2} = 0.3 \times \left(\frac{220}{660}\right)^2 + 0.035 = 0.0683\ \Omega$$

$$X_{O2} = 0.5 \times \left(\frac{220}{660}\right)^2 + 0.06 = 0.1155\ \Omega$$

$$\text{Voltage regulation} = \frac{I_2 R_{O2} \cos\theta_1 + I_1 X_{O2} \sin\theta_2}{E_2}$$

$$= \frac{50}{220}\{0.0683 \times 0.8 + 0.1155 \times 0.6\} = 0.028 \text{ or, } 2.8\%.$$

3.42 A 20 kVA, 2000/220 V, single-phase transformer has a primary resistance of 2.1 Ω and a secondary resistance of 0.026 Ω. The corresponding leakage reactances are 2.5 Ω and 0.03 Ω. Estimate the regulation at full load under p.f. conditions of (i) unity, (ii) 0.5 lagging and (iii) 0.5 leading.

Solution

$$I_2 = \frac{20 \times 10^3}{220} = 90.91\ \text{A}$$

$$R_{O2} = 2.1 \times \left(\frac{220}{2000}\right)^2 + 0.026 = 0.0514\ \Omega$$

$$X_{O2} = 2.5 \times \left(\frac{220}{2000}\right)^2 + 0.03 = 0.06025\ \Omega$$

(i) Voltage regulation at unity p.f. $= \frac{I_2}{E_2}\{R_{O2} \cos\theta_2 + X_{O2} \sin\theta_2\}$

$$= \frac{90.91}{220} \times 0.0514 \times 1 = 0.0212 \text{ or } 2.12\%.$$

(ii) Regulation at (0.5 lagging) p.f. $= \frac{90.91}{220}\{0.0514 \times 0.5 + 0.06025 \sin(\cos^{-1} 0.5)\}$

$$= 0.322 \text{ or } 3.22\%.$$

(iii) Regulation at (0.5 leading) p.f. $= \frac{90.91}{220}\{0.0514 \times 0.5 - 0.06025 \sin(\cos^{-1} 0.5)\}$

$$= (-0.0109) \text{ or, } (-1.09\%).$$

3.43 A single-phase transformer is designed to operate at 2 V per turn and turns ratio of 3:1. If the secondary winding is to supply a load of 8 kVA at 80 V, find (i) the primary supply voltage, (ii) the number of turns on each winding and (c) the current in each winding.

Solution

$$\frac{N_1}{N_2} = \frac{3}{1} = \frac{E_1}{E_2}$$

$$\frac{E_1}{N_1} = \frac{E_2}{N_2} = 2$$

$$E_2 = 80 \text{ V}$$

where N_1 and N_2 are the number of turns of the primary and secondary windings respectively.

(i) So, $E_1 = 3 \times 80 = 240$ V
Primary voltage = 240 V.

(ii) Now, $\left(\frac{E_1}{N_1}\right) = 2$

So, $(N_1) = \frac{E_1}{2} = \frac{240}{2} = 120$

Again, $(N_2) = \frac{E_2}{2} = \frac{80}{2} = 40.$

(iii) Secondary current = $\frac{8000}{80} = 100$ A ($\because$ load is 8 kVA)

Primary current = $\frac{8000}{240} = 33.33$ A.

3.44 A single-phase step down transformer has the following particulars: Turns ratio 4:1, no load current 5 A at 0.3 p.f. lagging. Secondary voltage 110 V. Secondary load 10 kVA at 0.8 p.f. (lagging). Find (i) the primary voltage, neglecting the internal voltage drop, (ii) the secondary current on load, (iii) the primary current and (iv) the primary p.f.

Solution

$$\left(\frac{N_1}{N_2}\right) = \frac{4}{1} = \frac{E_1}{E_2}$$

$$E_2 = 110 \text{ V}$$

(a) $\therefore \quad E_1 = 4 \times 110 = 440$ V.

(b) Secondary load current $(I_2) = \frac{10{,}000}{110} = 90.91$ A.

(c) If (I_1') is the load component of the primary current then from $I_1' N_1 = I_2 N_2$ or,

$$I_1' = I_2 \frac{N_2}{N_1} = 90.91 \times \frac{1}{4} = 22.73 \text{ A}$$

if I_1 is the primary current then,

$I_1 \cos \theta_1 = I_o \cos \theta_o + I_1' \cos \theta$, where I_o and I_1' the no load and load component of primary current, $\cos \theta_o$ and $\cos \theta$ are the no load p.f. and secondary load p.f. respectively.

So, $I_1 \cos \theta_1 = 5 \times 0.3 + 22.73 \times 0.8 = 19.684$ A.

Again, $I_2 \sin \theta_1 = 5 \sin(\cos^{-1} 0.3) + 22.73 \sin(\cos^{-1} 0.8)$
$= 18.4$ A

$\therefore \quad I_1 = \sqrt{(19.684)^2 + (18.4)^2} = 26.94$ A.

$\therefore$ Primary current is 26.94 A

(d) Primary p.f. = $\cos \theta = \dfrac{I_1 \cos \theta_1}{I_1} = \dfrac{19.68}{26.94} = 0.73$ lagging.

3.45 A 6.6 kV, 50 Hz single-phase transformer with a transformation ratio (1:0.06) takes a no load current of 0.7 A and a full load current of 7.827 A when the secondary is loaded to 120 A at a p.f. of 0.8 lagging. What is the no load p.f.?

Solution

$I_2 = 120$ A

Load p.f. ($\cos \theta = 0.8$ lagging or, $\theta = \cos^{-1} 0.8 = 36.87°$

$$\frac{N_1}{N_2} = \frac{1}{0.06}$$

No load primary current $I_o = 0.7$ A

Load component of primary current $(= I_1')= I_2 \dfrac{N_2}{N_1} = 120 \times 0.06 = 7.2$ A

Full load primary current $I_1 = 7.827$ A

Let no load p.f. angle be θ_o

Referring to Fig. 6.31

$$I_1^2 = I_0^2 + I_1'^2 + 2 I_O I_1' \cos(\theta_o - \theta)$$

or $$\cos(\theta_o - \theta) = \frac{(7.827)^2 - (0.7)^2 - (7.2)^2}{2 \times 0.7 \times 7.2} = 0.886$$

or $$(\theta_o - \theta) = \cos^{-1} 0.886 = 27.625°$$

or $$\theta_o = 27.625° + 36.87° = 64.495°.$$

3.46 A 1 kVA single-phase transformer has an iron loss of 20 W and a full load copper loss of 40 W. Calculate its efficiency on full load output at a p.f. of (0.8) lagging.

Solution

Efficiency on full load at 0.8 p.f. lagging

$$= \frac{\text{Output}}{\text{Output + Loss}} = \frac{1000 \times 0.8}{1000 \times 0.8 + 20 + 40} \times 100\% = 93\%.$$

3.47 A 25 kVA, 440/110V, 50 Hz single-phase step down transformer is designed to work with 1.5 V per turn with a flux density not exceeding 1.35 T. Calculate (i) the required number of turns on the primary and secondary windings respectively, (ii) the cross-sectional area of the iron core and (iii) the secondary current.

Solution

$$\frac{E_1}{N_1} = \frac{E_2}{N_2} = 1.5$$

$B_m = 1.35$ Wb/m^2

$E_1 = 440$ V and $E_2 = 110$ V

(i) $$N_1 = \frac{E_1}{1.5} = \frac{440}{1.5} = 293$$

As $$\frac{E_1}{E_2} = \frac{N_1}{N_2}$$

So, $$N_2 = \frac{E_2}{E_1} \times N_1 = \frac{110}{440} \times 293 = 73$$

Here (N_1) and (N_2) are the number of turns of the primary and secondary windings respectively.

(ii) $E_1 = 4.44\ B_m\ AfN_1$, where A is the cross-sectional area of the iron core.

Here, $$A = \frac{440}{4.44 \times 1.35 \times 50 \times 293} \text{ sqm} = 0.005 \text{ sqm.}$$

3.48 The diagram in Fig. 3.21 shows the equivalent circuit for a single-phase transformer. The ratio of secondary to primary turns is 15. Find the (i) secondary terminal voltage, (ii) the primary current and (iii) efficiency.

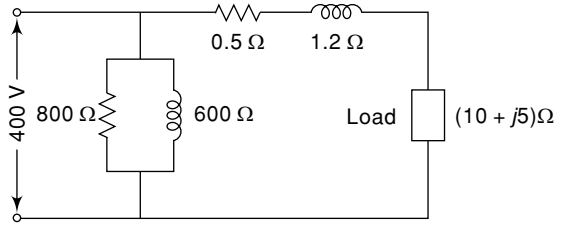


Fig. 3.21 *Circuit diagram for Example 6.48*

Solution

Load impedance = $10 + j5 = 11.18\angle 26.56°\ \Omega$

Total series impedance = $(0.5 + 10) + j(1.2 + 5) = 10.5 + j\ 6.2 = 12.194\angle 30.56°\ \Omega$

Load current, $$I_2 = \frac{400}{12.194\angle 30.56°} \text{ A} = 32.8\angle -30.56° \text{ A}$$

(i) Secondary terminal voltage = $I_2 \times 11.18\angle 26.56° = 366.7$ V.

(ii) Magnetising current = $\frac{400}{800} - j\frac{400}{600} = 0.5 - j0.667 = 0.833\angle -53.14°$ A.

Hence primary current = load current + magnetising current

$= 32.8\angle -30.56° + 0.5 - j0.667$

$= (28.74 - j17.34) = 33.57\angle -31.1°$.

(iii) Input = $(VI \cos \theta) = 400 \times 33.57 \cos (31.1°) = 11497.95$ W.

Total losses = Iron losses + Copper losses

$= 400 \times 0.833 \cos 53.14° + (33.57)^2 \times 0.5 = 763.34$ W

$$\text{Efficiency} = \left(1 - \frac{\text{Loss}}{\text{Input}}\right) = 1 - \frac{763.34}{11497.95} = 0.9336 \text{ or } 93.36\%.$$

3.49 A 50 kVA, 3.3 kV/230 V single-phase transformer has an impedance of 4.2% and a copper loss of 1.8% at full load. Calculate the ohmic value of resistance, reactance and impedance referred to the primary side. Estimate the primary short circuit current, assuming the supply voltage to be maintained.

Solution

Primary full load current = $\frac{50,000}{3300}$ A = 15.15 A

Now, $\frac{4.2}{100} = \frac{I_1 Z_{o1}}{V_1}$

or $0.042 = \frac{15.15\, Z_{o1}}{3300}$

or $Z_{o1} = 9.148\ \Omega$

where Z_{o1} = equivalent impedance referred to the primary.

Again, $0.018 = \frac{I_1^2 R_{o1}}{V_1 I_1} = \frac{I_1 R_{o1}}{V_1} = \frac{15.15\, R_{o1}}{3300}$

or $R_{o1} = 3.92\ \Omega$,

where R_{o1} = equivalent resistance referred to the primary.

$\therefore$ equivalent reactance referred to the primary = $\sqrt{(9.148)^2 - (3.92)^2}\ \Omega = 8.26\ \Omega$.

Under short circuit condition, the primary current = $\left(\frac{V_1}{Z_{o1}}\right) = \frac{3300}{9.148}$ A = 360.73 A.

3.50 A 50 kVA, 440/110 V single-phase transformer has an iron loss of 250 W. With the secondary windings short circuited full load currents flow in the windings when 25 V is applied to the primary, and the power input being 500 W. For this transformer determine (i) the percentage voltage regulation at full load, 0.8 p.f. lagging, (ii) the fraction of full load at which the efficiency is maximum.

Solution

Iron loss = 250 W.

Full load primary current = $\frac{50,000}{440}$ A = 113.63 A.

Full load secondary current = $\frac{50,000}{110}$ A = 454.52 A.

Total impedance referred to the primary $Z_{o1} = \frac{25}{113.63}\ \Omega = 0.22\ \Omega$.

Primary input = $(113.63)^2 \times R_{o1} = 500$, where R_{o1} = equivalent resistance referred to the primary.

So $R_{o1} = \frac{500}{(113.63)^2}\ \Omega = 0.0387\ \Omega$

Now $X_{o1} = \sqrt{(0.22)^2 - (0.0387)^2}\ \Omega = 0.2165\ \Omega$.

If R_{o2} and X_{o2} be the equivalent resistance and reactance referred to the secondary then

$$R_{o2} = (0.0387) \times \left(\frac{110}{440}\right)^2 \Omega = 0.0024\ \Omega$$

$$X_{o2} = (0.2165) \times \left(\frac{110}{440}\right)^2 \Omega = 0.0135\ \Omega$$

(i) Voltage regulation at full load and 0.8 p.f. lagging

$$= \frac{I_2 R_{o_2} \cos\theta_2 + I_2 X_{o_2} \sin\theta_2}{E_2}$$

$$= \frac{454.52}{110}\{0.0024 \times 0.8 + 0.0135 \times 0.6\} = 0.0414 \text{ or } 4.14\%$$

(ii) Let x be the fraction of full load at which efficiency is maximum. For maximum efficiency, core losses = copper losses

$\therefore \quad x^2 I_2^2 R_{o2} = 250$ or, $\quad x^2 = \dfrac{250}{(454.52)^2 \times 0.0024} = 0.504$

or $\quad x^2 = 0.71.$

$\therefore$ Efficiency is maximum when the load is 0.71 times the full load.

3.51 The maximum efficiency of a 100 kVA, single-phase transformer is 95% and occurs at 90% of full load at 0.85 p.f. If the leakage impedance of the transformer is 5%, find the voltage regulation at rated load 0.8 p.f. lagging.

Solution

Output at maximum efficiency = $100 \times 0.9 \times 0.85 = 76.5$ kW

$$\text{Efficiency} = (0.95) = \frac{\text{Output}}{\text{Output} + \text{Losses}} = \frac{76.5}{76.5 + \text{Losses}}$$

$$\therefore \quad \text{Losses} = \left[\frac{76.5}{0.95} - 76.5\right] = 4.026 \text{ kW}$$

At maximum efficiency core losses = copper losses

$\therefore$ Core losses = copper losses = 2.013 kW

2.013 kW is the copper losses at 90% of full load.

$$\text{So full load ohmic losses} = 2.013 \times \left(\frac{1}{0.9}\right)^2 = 2.485 \text{ kW}$$

If I_2 be the full load secondary current,

$(I_2^2 R_{O2}) = 2485$, where R_{O2} is the equivalent resistance referred to as the secondary

$$\therefore \quad I_2 V_2 \left(\frac{I_2 R_{O2}}{V_2}\right) = 2485$$

or $\quad 100 \times 10^3 \times R_{\text{P.u}} = 2485$, where $R_{\text{p.u.}}$ is the p.u resistance

or $\quad R_{\text{P.u}} = 0.02485$

Now $\quad Z_{\text{P.u}} = 0.05$

$$\therefore \quad X_{\text{P.u}} = \sqrt{(0.05)^2 - (0.02485)^2} = 0.04339$$

Voltage regulation $= (R_{\text{P.u}} \cos\theta_2 + X_{\text{P.u}} \sin\theta_2) = 0.02485 \times 0.8 + 0.04339 \times 0.6$

$= 0.0459$ or, 4.59%.

3.52 When an open circuit test is made on the primary of a transformer at 440 V and 50 Hz, the iron loss is 2.5 kW. When the test is repeated at 220 V and 25 Hz, the corresponding loss is measured to be 850 W. Determine the hysteresis and eddy current loss at normal voltage and frequency.

Solution

Hysteresis loss, $H \propto f$ and eddy current loss, $E \propto f^2$, where f is the frequency.

At $H = K_1 f$ and $(E) = K_2 f^2$

At 50 Hz iron loss = 2500 W

As iron loss = $H + E$

$\therefore \quad 2500 = K_1 50 + K_2 (50)^2$

or $\quad 2500\ K_2 + 50\ K_1 = 2500$

or $\quad 50\ K_2 + K_1 = 50$

Again at 25 Hz iron loss = 850 W

$\therefore \quad 850 = K_1\ 25 + K_2 (25)^2$

or $\quad K_1 + 25\ K_2 = 34$

Solving the above two equations

$$(50 - 25) K_2 = 50 - 34$$

or $$K_2 = \frac{16}{25} = 0.64$$

and $$K_1 = 50 - 50 \times 0.64 = 18.$$

At 50 Hz, hysteresis loss = $18 \times 50 = 900$ W

and eddy current loss = $0.64 \times (50)^2 = 1600$ W.

3.53 The following results were obtained in tests on a 50 kVA, single-phase, 3300/400 V transformer.

Open Circuit Test:

Primary voltage 3300 V, Secondary voltage 400 V, Input Power 430 W.

Short Circuit Test:

Reduced voltage on primary (124 V) to give full secondary current, primary current is 15.3 A and input power 535 W.

Calculate

(i) The efficiency at half load at 0.707 p.f. lagging.

(ii) The regulation and terminal voltage at full load for p.f. 0.707 leading.

Solution

From open circuit test iron losses = 430 W.

From short circuit test copper losses = 535 W.

Under short circuit test applied voltage = 124 V

and primary current = 15.3 A.

Hence equivalent impedance referred to the primary winding

$$Z_{O1} = \frac{124}{15.3}\ \Omega = 8.1\ \Omega$$

Equivalent impedance referred to the secondary winding

$$Z_{O2} = Z_{O1} \times \left(\frac{N_2}{N_1}\right)^2 = 8.1 \times \left(\frac{400}{3300}\right)^2 = 0.119\ \Omega$$

If I_1 is the primary current and R_{O1} is the equivalent resistance referred to the primary then

$$I_1^2 R_{O1} = 535$$

or $$R_{O1} = \frac{535}{(15.3)^2} = 2.285\ \Omega.$$

Hence equivalent resistance referred to secondary is

$$R_{O2} = 2.285 \times \left(\frac{400}{3300}\right)^2 = 0.03357\ \Omega$$

$$X_{O2} = \sqrt{(0.119)^2 - (0.03357)^2} = 0.114\ \Omega.$$

Full load secondary current $I_2 = \dfrac{50 \times 10^3}{400}$ A = 125 A

(i) Efficiency at $\left(\frac{1}{2}\right)$ load at 0.707 p.f. lagging

$$= \frac{50 \times 10^3 \times \frac{1}{2} \times 0.707}{50 \times 10^3 \times \frac{1}{2} \times 0.707 + 430 + \left(\frac{1}{2}\right)^2 \times 535} \times 100\% = 96.91\%.$$

(ii) Regulation at full load for p.f. 0.707 leading

$$= \frac{I_2}{E_2}\{R_{O2} \cos\ \theta_2 - X_{O2} \sin\ \theta_2\}$$

$$= \frac{125}{400}\{0.03357 \times 0.707 - 0.114 \times 0.707\} = -0.0178 \text{ or, } -1.78\%$$

Again, $\left[1 - \dfrac{V_2}{E_2}\right] = (-0.0178)$, where (V_2) is the terminal voltage.

Hence, $V_2 = (1 + 0.0178)\ E_2 = 1.0178 \times 400 = 407.12$ V.

3.54 A 17.5 kVA, 450/121 V, 50 Hz single-phase transformer gave the following data on test:

Open circuit test (OCT)*:* 450 V, 1.5 A, 115 W

Short circuit test (SCT)*:* 15.75 V, 38.9 A, 312 W.

Estimate the voltage on the secondary terminals and the efficiency of the transformer when supplying full load current, at a p.f. of (0.8) lagging, from the secondary side. Assume the input voltage to be maintained at 450 V.

Solution

Full load primary current = $\dfrac{17500}{450}$ A = 38.89 A

Full load secondary current = $\dfrac{17500}{121}$ A = 144.63 A

As 450 V is the applied voltage in OCT so this test has been performed on the h.v. side and as the current in the SCT is 38.9 A which the rated primary or low voltage current so this test has also been performed on the l.v. side.

From short circuit test data,

$$R_{o1} = \frac{312}{(38.9)^2}\ \Omega = 0.206\ \Omega,$$

$$Z_{O1} = \frac{15.75}{38.9}\ \Omega = 0.405$$

and $$X_{O1} = \sqrt{(0.405)^2 - (0.206)^2} = 0.3487\ \Omega.$$

$\therefore$ $$R_{O2} = 0.206 \times \left(\frac{121}{450}\right)^2 = 0.0149\ \Omega$$

and $X_{O2} = 0.3487 \times \left(\frac{121}{450}\right)^2 = 0.0252\ \Omega.$

If V_2 be the secondary terminal voltage then

$[121 - V_2] = 144.63(0.0149 \times 0.8 + 0.0252 \times 0.6) = 3.91$

or $V_2 = 117.09$ V.

From OCT, iron loss = 115 W

From SCT, full load copper loss = 312

So efficiency at full load and 0.8 p.f. lagging

$$= \frac{17.5 \times 10^3 \times 0.8}{17.5 \times 10^3 \times 0.8 + 115 + 312} = 0.97 \text{ or } 97\%.$$

3.55 A 11,000 V, 500 Hz transformer has a flux density of 1.2 Wb/m^2 at rated voltage and frequency. Now all the linear dimensions of the core are doubled; primary and secondary turns are halved and the new transformer is energised from 22000 V, 50 Hz supply. Both the transformers have the same core material and the same lamination thickness. Calculate the flux density for the new transformer.

Solution

$$V = \sqrt{2}\ \pi f B_m AN$$

$$\frac{V_1}{V_2} = \frac{11{,}000}{22{,}000} = \frac{50 \times 1.2\ AN}{50 \times B_{m_2} \times 2^2\ A \times \frac{1}{2}N}$$

or $$\frac{1}{2} = \frac{1.2}{B_{m_2} \times 2} \text{ or, } B_{m_2} = \frac{1.2 \times 2}{2} = 1.2.$$

So the flux density of the new transformer = 1.2 Wb/m^2.

3.56 The daily variation of load on a 100 kVA transformer is as follows:

8 a.m. to 1 p.m.:	65 kW, 45 KVAR
1 p.m .to 7 p.m.:	80 kW, 50 KVAR
7 p.m. to 2 a.m.:	30 kW, 30 KVAR
2 a.m. to 8 a.m.:	No load

The transformer has a no load core loss of 270 W and a full load ohmic loss of 1200 W. Determine the all day efficiency of the transformer.

Solution

From 8 a.m. to 1 p.m.,

$$\text{kVA} = \sqrt{(65)^2 + (45)^2} \quad 79$$

$$\text{Ohmic loss} = \left(\frac{79}{100}\right)^2 \times 1200 = 749 \text{ W}$$

Energy lost as ohmic loss = $\frac{749 \times 5}{10^3}$ kWh = 3.745 kWh.

From 1 p.m. to 6 p.m.,

$$\text{kVA} = \sqrt{(80)^2 + (50)^2} = 94.34$$

$$\text{Ohmic loss} = \left(\frac{94.34}{100}\right)^2 \times 1200 = 1068 \text{ W}$$

Energy lost as ohmic loss = $\frac{1068 \times 6}{10^3}$ kWh = 6.408 kWh.

From 7 p.m. to 2 a.m.,

$$\text{kVA} = \sqrt{(30)^2 + (30)^2} = 42.426$$

$$\text{Ohmic loss} = \left(\frac{42.426}{100}\right)^2 \times 1200 = 216$$

Energy lost as ohmic loss = $\frac{216 \times 7}{10^3}$ kWh = 1.51 kWh

Daily energy lost as ohmic losses = (3.745 + 6.408 + 1.512) kWh = 11.665 kWh

Daily energy lost as core loss = $\frac{24 \times 270}{10^3}$ kWh = 6.48 kWh

Total energy loss = (11.665 + 6.48) kWh = 18.145 kWh

Daily kWh output = 65 × 5 + 80 × 6 + 30 × 7 + 0 = 1015 kWh

All day efficiency = $\frac{\text{Energy output}}{\text{Energy output + Energy loss}} = \frac{1015}{1015 + 18.145} \times 100\% = 98.24\%$.

3.57 A 100 kVA, 2400/240 V, 50 Hz single-phase transformer has an exciting current of 0.64 A and a core loss of 700 W, when its high voltage side is energised at rated voltage and frequency. Calculate the two components of the exciting current.

Solution

Exciting current I_e = 0.64 A

Core loss = ($V_1 I_e \cos \theta_o$) = 700 W, where $\cos \theta_o$ is the no load p.f. and V_1 is the voltage of the primary winding.

So, $\cos \theta_o = \frac{700}{2400 \times 0.64} = 0.456$

The core loss component of exciting current

$= I_e \cos \theta_o = 0.64 \times 0.456 = 0.292$ A.

The magnetizing component of exciting current

$= I_e \sin \theta_o = 0.64 \times \sin (\cos^{-1} 0.456) = 0.569$ A.

3.58 In no load test of a single-phase transformer the following test data were obtained:

Primary voltage = 220 V

Secondary voltage = 110 V

Primary current = 0.5 A

Power input 30 = W.

Find the turns ratio, magnetising component of no load current, loss component of no load current and the iron loss. Resistance of primary winding is 0.6 Ω.

Solution

$$\text{Turns ratio} = \left(\frac{N_1}{N_2}\right) = \frac{V_1}{V_2} = \frac{220}{110} = 2$$

No load current I_o = 0.5 A

Power at no load ($V_1 I_o \cos \theta_o$) = 30 W.

Hence, $I_o \cos \theta_o = \frac{30}{220}$ = 0.136 A, i.e loss component of no load current is 0.136 A.

Hence, $\cos \theta_o$ = 0.272, i.e. $\sin \theta_o$ = 0.962

Magnetising component of no load current is

$I_o \sin \theta_o = 0.5 \times 0.962 = 0.481$ A

Iron loss = Input power – Ohmic loss in primary winding

$= (30 - (0.5)^2 \times 0.6) = 29.85$ W.

3.59 A transformer has its maximum efficiency of 0.975 at 20 kVA at unity p.f. During the day it is loaded as follows:

10 hr: 3 kW at 0.6 p.f.

8 hr: 10 kW at 0.8 p.f.

6 hr: 20 kW at 0.9 p.f.

Find the all day efficiency.

Solution

kWh output = $(10 \times 3) + (8 \times 10) + (6 \times 20) = 30 + 80 + 120 = 230$ kWh

As maximum efficiency is 0.975 so total losses under this condition is $[1 - 0.975] = 0.025$ of output power.

At unity p.f. output power = $20 \times 1 = 20$ kW

Hence losses = $0.025 \times 20{,}000 = 500$ W

$\therefore$ core losses = copper losses = $\frac{500}{2}$ W = 250 W

As core loss is constant for all p.f. so total core losses in 24 hr.

$$= \frac{250 \times 24}{10^3} \text{ kWh} = 6 \text{ kWh}$$

For the first 10 hr.

$$\text{kVA load} = \frac{3}{0.6} = 5$$

$$\text{Total copper losses} = 10 \times \left(\frac{5}{20}\right)^2 \times \frac{250}{1000} \text{ kWh} = 0.156 \text{ kWh}$$

For the next 8 hr.

$$\text{kVA load} = \frac{10}{0.8} = 12.5$$

$$\text{Total copper losses} = 8 \times \left(\frac{12.5}{20}\right)^2 \times \frac{250}{1000} \text{ kWh} = 0.781 \text{ kWh.}$$

For the last 6 hr.

$$\text{kVA load} = \frac{20}{0.9} = 22.22$$

$$\text{Total copper losses} = 6 \times \left(\frac{22.22}{20}\right)^2 \times \frac{250}{1000} \text{ kWh} = 1.85 \text{ kWh}$$

Total copper losses = $0.156 + 0.781 + 1.85 = 2.79$ kWh

Total loss = 6 kWh + 2.79 kWh = 8.79 kWh

$$\text{All day efficiency} = \frac{230}{230 + 8.79} = 0.963 \text{ or } 96.3\%.$$

3.60 A lighting transformer rated at 10 kVA has full load losses of 0.3 kW which is made up equally from the iron losses and the copper losses. The duty cycle consists of full load for 3 hours, half full load for 4 hours and no load for the remainder of a 24 hours period. If the load operates at unity power factor, calculate the all day efficiency.

Solution

The load operates at unity power factor.

For the first three hours,

$$\text{Energy output} = 10 \times 1 \times 3 \text{ kWh} = 30 \text{ kWh}$$

For the next four hours,

$$\text{Energy output} = \frac{1}{2} \times 10 \times 1 \times 4 = 20 \text{ kWh}$$

$$\text{Total energy output} = (30 + 20) \text{ kWh} = 50 \text{ kWh}$$

$$\text{Full load losses} = 0.3 \text{ kW}$$

$$\text{So, iron loss} = \left(\frac{0.3}{2}\right)\text{kW} = 0.15 \text{ kW}$$

$$\text{and full load copper loss} = \frac{0.3}{2} \text{ kW} = 0.15 \text{ kW}$$

$$\text{Iron loss energy} = (0.15 \times 24) = 3.6 \text{ kWh}$$

$$\text{Copper loss energy} = \left(0.15 \times 3 + \frac{0.15}{(2)^2} \times 4\right) \text{ kWh} = (0.45 + 0.15) \text{ kWh} = 0.6 \text{ kWh}$$

$$\text{Energy loss} = (3.6 + 0.6) \text{ kWh} = 4.2 \text{ kWh}$$

$$\therefore \quad \text{All day efficiency} = \frac{50}{50 + 4.2} = 0.922 \text{ or } 92.2\%.$$

EXERCISES

Short- and Long-Answer-Type Questions

1. Define a transformer. Discuss the principle of operation of a single phase transformer.
2. Distinguish between core type and shell type transformer. Why is the low voltage winding placed near the core? Why is the core of a transformer laminated?
3. Derive an expression for the emf induced in a transformer winding.
4. Define an ideal transformer. Draw and explain the no load phasor diagram of an ideal single phase transformer.
5. Draw the exact equivalent circuit of a transformer and describe briefly the various parameters involved in it.
6. Draw and explain the phasor diagram of a single-phase transformer under lagging p.f.
7. Define voltage regulation of a transformer. Develop an expression for calculating the voltage regulation of a two winding transformer under (i) lagging p.f., (ii) unity p.f. and (iii) leading p.f.
8. What are the different types of losses in a transformer? Write an expression for efficiency and develop a condition for maximum efficiency.
9. Explain why
   (i) the open circuit test on a transformer is conducted at a rated voltage,
   (ii) usually the low voltage winding is excited and the high voltage winding is open circuited for open circuit test,
   (iii) the open circuit test gives core loss and short circuit test gives copper loss,

(iv) usually low voltage winding is short circuited and high voltage winding is excited for the short circuit test.

10. Discuss about the Sumpner's test on single-phase transformer.
11. (i) Explain why parallel operation of transformer is necessary.
    (ii) State the essential and desirable conditions which would be satisfied before two single-phase transformers may be operated in parallel.
    (iii) Deduce expressions for the load shared by two transformers connected in parallel.
12. What is an auto transformer? State its merits and demerits over a two winding transformer. What are the applications of an auto transformer?
13. Discuss about the different types of cooling used in transformers. Distinguish between a power transformer and a distribution transformer.
14. Define all day efficiency of a single-phase transformer.
15. What are the advantages of a transformer bank of three single-phase transformers over a unit three-phase transformer of the same kVA rating? What are the distinguishing features of YY, YΔ, ΔY and ΔΔ three-phase connections?
16. The primary winding of a single phase transformer connected to a 500 V, 50 Hz supply takes 1.41 A and absorbs 125 W with the secondary winding open circuited. The secondary open circuit voltage is 250 V. When the secondary winding is short circuited and the primary is connected to a 250 V, 50 Hz supply, the primary current is 15.1 A and the power absorbed is 92 W. Determine the shunt and series components of the equivalent circuit.
    [*Ans:* $R_O = 2000\ \Omega$, $X_O = 360.32\ \Omega$, $r_{o1} = 0.403\ \Omega$, $x_{o1} = 16.06\ \Omega$]
17. A 1100/230 V, 150 kVA single-phase transformer has a core loss of 1.4 kW and a full load copper loss of 1.6 kW. Determine (i) the kVA load for maximum efficiency and (ii) the maximum efficiency at unity power factor load. [*Ans:* 140.312 kVA, 98.04%]
18. A 415/220 V transformer takes a no load current of 1 A and operates at a p.f. of 0.19 lagging when the secondary supplies a current of 100 A at 0.8 p.f. lagging; find the primary current. [*Ans.:* 53.27 A]

[*Hint:*

No load current, $I_o = 1$ A

No load power factor angle, $\theta_o = \cos^{-1} 0.19 = 79°$

Secondary current, $I_2 = 100$ A

Load power factor angle, $\theta_2 = \cos^{-1} 0.8 = 36.86°$

Load component of the primary current,

$$I_1' = I_2 \frac{N_2}{N_1} = 100 \times \frac{220}{415} \text{A} = 53 \text{ A}.$$

Vertical component of primary current I_1 is

$$I_1' \cos \theta_2 + I_o \cos \theta_o = 53 \times 0.8 + 1 \times 0.19 = 42.59 \text{ A}.$$

Horizontal component of primary current I_1 is

$$I_1' \sin \theta_2 + I_o \sin \theta_o = 53 \times 0.6 + 1 \times \cos 79° = 32 \text{ A}.$$

Hence $I_1 = \sqrt{(42.59)^2 + (32)^2} = 53.27$ A]

19. The following test data were obtained on a 20 kVA, 50 Hz; 1 ph, 2000/200 V transformer
No load test: 200 V, 1 A, 120 W
Short circuit test: 60 V, 10 A, 300 W
Find (i) efficiency of the transformer at 1/2 of the full load and 0.8 p.f. lagging.
(ii) maximum efficiency and the load at which it occurs.
[*Ans:* 97.62%; 63.2% of full load]

[*Hint:*
$P_c = 120$ W
$P_{cu} = 300$ W

(i) Efficiency $= \dfrac{20 \times 10^3 \times 0.8 \times \frac{1}{2}}{20 \times 10^3 \times 0.8 \times \frac{1}{2} + 120 + \left(\frac{1}{2}\right)^2 \times 300} \times 100\%$

$= 97.62\%$

(ii) If maximum efficiency occurs at x times the full load
$x^2 \times 300 = 120, \therefore x = 0.632$
Load at maximum efficiency is 20×0.632 kVA = 12.64 kVA
Maximum efficiency at 0.8 p.f. is

$$\frac{12.64 \times 10^3 \times 0.8}{12.64 \times 10^3 \times 0.8 + 2 \times 120} \times 100\% = 97.68\%]$$

20. A 100 kVA, single-phase transformer of ratio 10000/200 V requires 300 V at the high voltage winding to circulate full load current with low voltage winding short circuited. The intake power is then 1000 W. Calculate the % regulation and the secondary terminal voltage on full load at 0.8 p.f. lagging.
[*Ans:* 2.49%]

21. Calculate (i) full load efficiency at 0.8 p.f. and (ii) the approximate voltage at the secondary terminal at full load and power factor of 0.8 lag and 0.8 lead for a 4 kVA, 200/400 V, 50 Hz single-phase transformer with the following test results:
Open circuit test (L.T. side data) : 200 V, 0.8 A, 70 W
Short circuit test (H.T. side data) : 17.5 V, 9 A, 50 W
[*Ans:* 96.05%, 384 V, 406.12 V]

22. The primary and secondary winding resistances of a 30 kVA, 6000/230 V transformer are 10 Ω and 0.016 Ω respectively. The reactance of the transformer as referred to primary is 34 Ω. Calculate the regulation at full load 0.8 p.f. lagging. [*Ans:* 3.33%]

23. A single-phase 20 Hz transformer is required to step down 2200 V to 250 V. The cross-section of the core is 36 sq cm and the maximum value of the flux density is 6 Wb. Determine a suitable number of turns for each winding and the transformation ratio.

$\left[\textit{Ans}: 458, 52, \dfrac{1}{8.8} \right]$

24. A 20 kVA transformer has 400 turns on the primary and 40 turns on the secondary winding. The primary is connected to a 2 kV, 50 Hz. supply. Find the full load primary and secondary currents, secondary emf and the maximum flux in the core. Neglect leakage drop and no load primary current.
[*Ans:* $I_{fl} = 10$ A; $I_2 = 100$ A, $E_2 = 200$ V; $\phi_m = 22.5$ mwb]
[*Hints:*

$$\frac{N_1}{N_2} = \frac{400}{40},$$

$$I_1 = \frac{20}{2}\text{A} = 10 \text{ A}$$

$$I_2 = I_1 \times \frac{N_1}{N_2} = 10 \times \frac{400}{40} = 100 \text{ A}$$

Secondary emf $E_2 = E_1 \times \frac{N_2}{N_1} = 2 \times \frac{40}{400} = 0.2$ kV = 200 V

$$E_1 = 4.44 f N_1 \times \phi_m$$

$$\phi_m = \frac{2000}{4.44 \times 50 \times 400} \text{ wb} = 0.0225 \text{ wb}]$$

25. A 125 kVA transformer having a primary voltage of 2200 V at 50 Hz has 182 primary turns and 40 secondary turns. Neglecting losses calculate (i) full load primary and secondary currents and (ii) no load secondary induced emf. [*Ans:* 56.82 A, 258.52 A, 483.52 V]
26. The secondary windings of a 2 kVA, 2400/120 V, 50 Hz single phase transformer is short circuited and potential difference of 16.2 V produces a primary current of 6 A, the input being 33.5 W. Calculate the total primary impedance, resistance and reactance. [*Ans:* 2.7 Ω, 0.93 Ω, 2.54 Ω]
27. The open circuit and short circuit test data of a 5 kVA, 200/400 V, 50 Hz; 1 phase transformer are:
    (i) *O.C. test:* primary voltage = 200 V, $I = 0.75$ A, $W = 75$ W.
    (ii) *S.C. test:* primary voltage = 18 V, S.C. current on the secondary side = 12.5 A, $W = 60$ W.
    Find the parameters of the equivalent circuit.
    [*Ans.:* $R_o = 2133.33$ Ω; $X_o = 1232.66$ Ω,
    $r_e = 0.384$ Ω; $x_e = 1.39$ Ω
    (all quantities are referred to h.v. side)]
    [*Hint:*
    No load current, $I_0 = 0.75$ A
    Core loss component of current $I_C = \frac{75}{200} = 0.375$ A
    Magnetising component of current $I_\phi = \sqrt{(0.75)^2 - (0.375)^2} = 0.649$ A
    Parameters referred to h.v. side
    Core loss resistance $R_o = \frac{200}{0.375} \times \left(\frac{400}{200}\right)^2 = 2133.33$ Ω

Magnetising reactance $X_\phi = \frac{200}{0.649} \times \left(\frac{400}{200}\right)^2 = 1232.66\ \Omega$

Equivalent resistance $r_{eH} = \frac{60}{(12.5)^2}\Omega = 0.384\ \Omega$

Equivalent impedance $Z_{eH} = \frac{18}{12.5}\Omega = 1.44\ \Omega$

Equivalent reactance $x_{eH} = \sqrt{(1.44)^2 - (0.384)^2}\ \Omega = 1.388\ \Omega$]

28. A 10 kVA transformer is given an open circuit test from which the iron losses are found to be 160 W. A short circut test shows the copper losses to be 240 W with full load current flowing. Calculate the all day efficiency if it operates at unity p.f. for 6 hours per day on full load, 2 hours on half load and the remainder of the time on no load. [*Ans:* 92.85%]
29. A 20 kW lighting transformer of ordinary efficiency 95% is on full load for 6 hours per day. Find the all day efficiency if the full load losses are equally divided between copper and iron. [*Ans:* 88.39%]
30. A 100 kVA, 50 Hz, 440/11,000 V, 1-phase transformer has an efficiency of 98.5% when supplying full load current at 0.8 p.f. lagging and an efficiency of 99% when supplying half full load current at unity power factor. Find the core losses and copper losses corresponding to full load current.
[*Ans:* $P_i = 277.33$ W; $P_{cu} = 940.67$ W]

[*Hint:*
At 98.5% efficiency,
Output = 100×0.8 kW = 80 kW

Loss = $80 \times \frac{1 - 0.985}{0.985} = 1.218$ kW

If P_i and P_{cu} be the full load iron and copper losses then

$$P_i + P_{cu} = 1218$$

Again, $P_i + \frac{1}{4}(P_{cu}) = 100 \times 1 \times \frac{1 - 0.99}{0.99} \times 10^3 = 1010.$

Solving, $P_i = 277.33$ W and $P_{cu} = 940.67$ W]

MULTIPLE CHOICE QUESTIONS

1. If the full load copper loss of a transformer is 2000 W, its copper loss at 80% of full load is
   (i) 2000 W (ii) 500 W
   (iii) 80 W (iv) 1280 W
   Answers: (iv) 1280 W
2. For short circuit and oper circuit test of a transformer the intruments are connected in
   (i) l.v. side only
   (ii) h.v. side only
   (iii) l.v. and h.v. side respectively

(iv) h.v. and l.v. side respectively.

Answer: (iv) h.v. and l.v. side respectively.

3. The efficiency of a transformer is maximum when
   (i) copper losses are zero
   (ii) iron losses are zero
   (iii) coper losses are 50% of iron losses
   (iv) copper losses are equal to iron losses

   Answer: (iv) copper losses are equal to iron losses
4. Hysteresis hoss of a transformer can be reduced by using
   (i) laminated core (ii) silicon steel
   (iii) oil (iv) nature of dielectric

   Answer: (ii) silicon steel
5. The transformer core is laminated to reduce
   (i) copper loss (ii) eddy current loss
   (iii) hysteresis loss (iv) none of these

   Answer: (ii) eddy current loss
6. The regulation of a transformer is negative if the load at the secondary side is
   (i) resistive (ii) inductive
   (iii) capacitive (iv) resistive-inductive

   Answer: (iii) capacitive
7. Oil is used in transformer for the purpose of
   (i) cooling
   (ii) heating
   (iii) insulation and cooling medium
   (iv) insulation

   Answer: (iii) insulation and cooling medium
8. Iron loss of a transformer is 100 W at half full load. At full load the iron loss would be
   (i) 100 W (ii) 50 W
   (iii) 200 W (iv) 400 W

   Answer: (i) 100 W
9. Which of the following relation is true for an ideal transformer?

   (i) $\frac{V_1}{V_2} = \frac{E_2}{E_1} = \frac{I_1}{I_2}$ (ii) $\frac{V_1}{V_2} = \frac{I_2}{I_1} = \frac{E_1}{E_2}$

   (iii) $\frac{V_1}{V_2} = \frac{I_1}{I_2} = \frac{E_1}{E_2}$ (iv) $\frac{V_2}{V_1} = \frac{E_1}{E_2} = \frac{I_2}{I_1}$

   Answer: (ii) $\frac{V_1}{V_2} = \frac{I_2}{I_1} = \frac{E_1}{E_2}$
10. Eddy current loss in a transformer varies as
    (i) square of frequency (ii) reciprocal of frequency
    (iii) directly with frequency (iv) root of square frequency

    Answer: (i) square of frequency

11. Transformer core is made of
    (i) laminated steel (ii) solid steel
    (iii) lamineted copper sheets (iv) any non megnetic meterial
    Answer: (i) laminated steel
12. Hysteresis loss in a transfomer varies as
    (i) square of frequency (ii) square root of frequency
    (iii) frequency (iv) reciprocal of frequency
    Answer: (iii) frequency

UNIVERSITY QUESTIONS WITH ANSWERS

Long-Answer-Type Questions

1. (a) Prove that the efficiency of a transformer is maximum when iron loss is equal to copper loss.
   Answer: Article 3.14
   (b) Following test data were obtained on a 20 KVA, 50 Hz, 1 Phase, 2000/200 V transformer.
   No load test: 200 V, 1 A, 120 W.
   Short circuit test: 60 V, 10 A, 300 W.
   Find
   (i) the efficiency of the transformer at $\frac{1}{2}$ of the load and 0.8 p. f. lagging.
   (ii) maximum efficiency and the load at which it occurs.
   (WBUT 2004)

   Answer:
   From no load test rated core loss (P_C) = 120 W

   Rated current on the *h.v.* side = $\frac{20\times10^3}{2000} = 10\,\text{A}.$

   ∴ From short circuit test rated copper loss (P_{cu}) = 300 W.

   (i) Efficiency of the transformer at $\frac{1}{2}$ load and 0.8 p.f. lagging is

$$\frac{\frac{1}{2}(V_2 I_2 \cos\theta_2)}{\frac{1}{2}(V_2 I_2 \cos\theta_2) + P_C + \left(\frac{1}{2}\right)^2 P_{cu}}$$

$$= \frac{\frac{1}{2}\times 20\times10^3\times0.8}{\frac{1}{2}\times20\times10^3\times0.8+120+\frac{1}{4}\times300}$$

$$= 0.9762 \text{ or } 97.62\%$$

   (ii) Suppose at x fraction of load the efficiency is maximum. At maximum efficiency core loss is equal to the copper loss.

$\therefore\ P_c = x^2 P_{cu}$

or, $120 = x^2 \times 300$

or $x = 0.632$

Hence, copper loss at maximum efficiency is

$(0.632)^2 \times 300 = 120$ watts

$\therefore$ Maximum efficiency at 0.8 p.f. (η_{max})

$$= \frac{0.632 \times 20 \times 10^3 \times 0.8}{0.632 \times 20 \times 10^3 \times 0.8 + 120 + 120}$$

$= 0.9768$ or, 97.68%

2. (a) Draw the equivalent circuit of a single phase transformer referred to the primary. Also draw the phasor diagram for a lagging p.f. load.

Answer: Article 3.9 and Fig. 3.10 (WBUT 2005, 2013)
Article 3.8 and Fig. 3.8(a)

(b) A 100 kVA, 50 Hz, 440/11,000 V, single phase transformer has an efficiency of 98.5 % when supplying full load current at 0.8 p.f. lagging and an efficiency of 99 % when supplying half full load current at unity power factor. Find the core losses and the copper losses corresponding to full load current.

(WBUT 2005)

Answer: Efficiency at full load and at 0.8 p.f. lagging is 0.985.

If P_c and P_{cu} be the core loss and copper loss at full load respectively then

$$0.985 = \frac{100 \times 10^3 \times 0.8}{100 \times 10^3 \times 0.8 + P_c + P_{cu}}$$

$$\therefore \quad P_c + P_{cu} = \frac{80,000}{0.985} - 80,000 = 1218.27 \qquad (1)$$

Efficiency at half load and at unity p.f. is 0.99.

$$\therefore \quad 0.99 = \frac{100 \times 10^3 \times 1 \times \frac{1}{2}}{100 \times 10^3 \times 1 \times \frac{1}{2} + P_c + \left(\frac{1}{2}\right)^2 P_{cu}}$$

$$\text{or,} \quad P_c + \frac{1}{4} P_{cu} = \frac{50,000}{0.99} - 50,000$$

$$= 505.05 \qquad (2)$$

Solving equations (1) and (2)

$$\frac{3}{4} P_{cu} = 713.22$$

or, $P_{cu} = 950.96$ W and $P_c = 267.31$ W

Hence, the core losses and copper losses corresponding to full load current are 267.31 W and 950.96 W respectively.

3. Draw the schematic representations of a shell type transformer and a core type transformer. Which one of the two is suitable for use as a distribution transformer and why? (WBUT 2006)
Answer: Article 3.2.

Distribution transformers are placed at consumer premises with secondary directly connected to consumer terminals. Primary of distribution transformers are continuously energised and hence the core losses take place continuously. Therefore distribution transformers are designed to have very low value of core losses. Now as in the core type transformer the windings surround a considerable part of the core it requires less iron material in comparison with shell type transformer. Hence, core-type transformer is suitable for use as a distribution transformer in order to have reduced value for core losses.

4. (a) Explain with reasons as to why transformer core is made up of silicon steel laminations. (WBUT 2006)
Answer: Article 3.2.

(b) Draw the phasor diagram of a single-phase transformer for lagging power factor load. Level all the phasors.
Answer: Article 3.8.

(c) The open circuit and short circuit test data of a 5 kVA, 200/400 volt, 50 Hz. single-phase transformer are
(i) *O.C. test:* primary voltage = 200 volts, I = 0.75 A, *W* = 75 W.
(ii) *S.C test:* primary voltage = 18 volts, S.C current on the secondary side = 12.5 A, W = 60 W. Find the parameters of the equivalent circuit. (WBUT 2013)

Answer: As rated voltage of 200 V is applied on the low voltage side we get the rated core loss from open circuit test.
Hence, core loss (P_c) = 75 W

$$I_0 = 0.75 \text{ A}$$

$$\therefore \quad \text{No load power factor } (\cos \phi_0) = \frac{75}{200 \times 0.75} = 0.5$$

Core loss resistance referred to low voltage side

$$(R_{CL}) = \frac{200}{0.75 \times 0.5} = 533.33\ \Omega$$

Magnetizing reactance referred to low voltage side

$$(\text{X}\phi_L) = \frac{200}{0.75 \times \sin(\cos^{-1} 0.5)} = 307.92\ \Omega$$

Rated current on the *hv* side

$$(I_{\text{H}}) = \frac{5000}{400} = 12.5 \text{ A}$$

Since, the rated current of 12.5 A flows in the *hv* side during short circuit test hence we get rated copper loss from short-circuit test.

$\therefore$ Rated copper loss (P_{cu}) = 60 W

Hence, equivalent resistance referred to *hv* side

$$(r_{eH}) = \frac{60}{(12.5)^2} = 0.384\ \Omega$$

Equivalent impedance referred to *hv* side $(Z_{CH}) = \frac{18}{12.5} = 1.44\ \Omega$

$\therefore$ Equivalent reactance referred to *hv* side

$$(x_{eH}) = \sqrt{(1.44)^2 - (0.384)^2} = 1.3878\ \Omega.$$

Referring the core loss resistance and magnetizing reactance to the *hv* side

$$R_{CH} = 533.33 \times \left(\frac{400}{200}\right)^2 = 2133.32\ \Omega$$

$$X_{\phi H} = 307.92 \times \left(\frac{400}{200}\right)^2 = 1231.68\ \Omega$$

Hence, the parameters of the equivalent circuit referred to *hv* side are:

$$R_{CH} = 2133.32\ \Omega, \qquad X_{\phi H} = 1231.68\ \Omega,$$
$$r_{eH} = 0.384\ \Omega \quad \text{and} \quad x_{eH} = 1.3878\ \Omega.$$

5. A 20 KVA transformer has 400 turns on the primary and 40 turns on the secondary winding. The primary is connected to 440 V, 50 Hz supply. Find the full load primary and secondary current, secondary e.m.f and the maximum flux in the core. Neglect leakage drop and no load current.

(WBUT 2007)

Answer: Given $N_1 = 400$; $N_2 = 40$; $V_1 = 400$ V.

If V_2 be the secondary voltage then,

$$\frac{V_1}{V_2} = \frac{N_1}{N_2}$$

$\therefore \qquad V_2 = 400 \times \frac{40}{400} = 40$ V

Full load primary current $(I_1) = \frac{20 \times 10^3}{400} = 50$ A

Full load secondary current $(I_2) = \frac{20 \times 10^3}{40} = 500$ A

Neglecting leakage drop secondary e.m.f. $E_2 = V_2 = 40$ V

Now $E_2 = 4.44\, f\, \phi_m\, N_2$, where ϕ_m is the maximum flux in the core.

$$\therefore \qquad \phi_m = \frac{E_2}{4.44\, f N_2} = \frac{40}{4.44 \times 50 \times 40} = 0.0045 \text{ Wb}$$

$$= 4.5 \text{ mWb.}$$

6. A 75 kVA transformer has 500 turns primary and 100 turns secondary. The primary and secondary resistances are 0.4 ohms and 0.02 ohms respectively and the corresponding leakage reactances are 1.5 ohms and 0.045 ohms respectively. The supply voltage is 2200 volts. Calculate (i) the equivalent impedance referred to the primary (ii) the voltage regulation at power factor of 0.8 lagging. (WBUT 2007)

Answer: Given $N_1 = 500$ $N_2 = 100$
$r_1 = 0.4\ \Omega$ $r_2 = 0.02\ \Omega$
$x_1 = 1.5\ \Omega$ $x_2 = 0.045\ \Omega$
$V_1 = 2200$ V.

If V_2 be the secondary voltage then,

$$\frac{V_1}{V_2} = \frac{N_1}{N_2} = \frac{500}{100}$$

$$\therefore \quad V_2 = \frac{100}{500} \times 2200 = 440 \text{ V}$$

Equivalent resistance referred to the primary

$$r_{e1} = r_1 + r_2' = r_1 + r_2\left(\frac{N_1}{N_2}\right)^2 = 0.4 + 0.02 \times \left(\frac{500}{100}\right)^2$$
$$= 0.4 + 0.5 = 0.9\ \Omega.$$

Equivalent resistance referred to the secondary

$$x_{e1} = x_1 + x_2' = x_1 + x_2\left(\frac{N_1}{N_2}\right)^2 = 1.5 + 0.045 \times \left(\frac{500}{100}\right)^2$$
$$= 1.5 + 1.125 = 2.625\ \Omega.$$

(a) The equivalent impedance referred to the primary is

$$Z_{e1} = r_{e1} + j\, x_{e1} = 0.9 + j2.625\ \Omega$$

(b) Voltage regulation at p.f. of 0.8 lagging

$$\Delta V = \frac{I_2\, r_{e2} \cos\theta_2 + I_2\, X_{e2} \sin\theta_2}{E_2},$$

where r_{e2} and x_{e2} are the equivalent resistance and reactance referred to the secondary.

Here, $$r_{e2} = r_{e1} \times \left(\frac{N_2}{N_1}\right)^2 = 0.9 \times \left(\frac{100}{500}\right)^2 = 0.036\ \Omega$$

and $$x_{e2} = x_{e1} \times \left(\frac{N_2}{N_1}\right)^2 = 2.625 \times \left(\frac{100}{500}\right)^2 = 0.105\ \Omega$$

$$I_2 = \frac{75{,}000}{440} = 170.45 \text{ A}$$

∴ Voltage regulation

$$\Delta V = \frac{170.45 \times 0.036 \times 0.8 + 170.45 \times 0.105 \times 0.6}{440}$$

$$= 0.0355 \text{ or } 3.55\ \%$$

7. A 220/110 V transformer is having no load current of 0.9 A at 0.12 p.f. (lag) and a secondary current of 95 A at 0.27 p.f. (lag). Find its primary current. (WBUT 2008)

Solution: No load current $I_0 = 0.9$ A.

No load power factor angle $\theta_0 = \cos^{-1} 0.12 = 83.11°$

Secondary current $I_2 = 95$ A

Power factor angle $\theta_2 = \cos^{-1} 0.27 = 74.335°$

The phasor diagram is shown in Fig. 3.22.

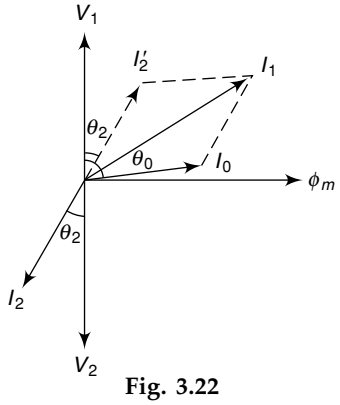


Fig. 3.22

The load component of primary current $I_2' = \frac{I_2 N_2}{N_1} = 95 \times \frac{110}{220} = 47.5$ A

Now primary current $\bar{I}_1 = \bar{I}_0 + \bar{I}_2'$ (pharor summation)

∴ Horizontal component of I_1 is

$$I_1 \cos\theta = I_2' \sin\theta_2 + I_0 \sin\theta_0$$
$$= 47.5 \sin 74.335° + 0.9 \times \sin 83.11°$$
$$= 45.736 + 0.893 = 46.63 \text{ A}$$

Vertical component of I_1 is

$$I_1 \sin\theta = I_2' \cos\theta_2 + I_0 \cos\theta_0 = 47.5 \times 0.27 + 0.9 \times 0.12$$
$$= 12.933$$

∴ Primary current $I_1 = \sqrt{(46.63)^2 + (12.933)^2} = 48.39$ A

8. (a) Prove that the efficiency of a transformer is maximum when iron loss is equal to copper loss.

Solution: Refer Article 3.14.

(b) Following test data were obtained on a 20 kVA, 50 Hz, 1 ph, 2000/200V transformer.

No load test: 200 V, 1 A, 120 W

Short circuit test: 60 V, 10 A, 300 W

Find (WBUT 2008)

(i) The efficiency of the transformer at $\frac{1}{2}$ of the full load and 0.8 p.f lagging.

(ii) Maximum efficiency and the load at which it occurs

Solution: Since, no load test is performed at rated voltage on low voltage side, the rated core loss P_c = 120 W

Now rated current at high voltage side is $\frac{20 \times 10^3}{2000}$ = 10 A.

Since, the short circuit test is performed at rated current on high voltage side the rated copper loss P_{cu} = 300 W

(i) Efficiency of transformer at half load and 0.8 p.f. lagging is

$$\frac{\frac{1}{2} V_2 I_2 \cos\theta_2}{\frac{1}{2} V_2 I_2 \cos\theta_2 + P_C + \left(\frac{1}{2}\right)^2 P_{cu}}$$

$$= \frac{\frac{1}{2} \times 20 \times 10^3 \times 0.8}{\frac{1}{2} \times 20 \times 10^3 \times 0.8 + 120 + \frac{1}{4} \times 300} = 0.9762 \text{ or } 97.62\ \%$$

(ii) Let at x fraction of load efficiency is maximum

$\therefore \quad x^2 P_{cu} = P_c$

or, $\quad x = \sqrt{\frac{P_c}{P_{cu}}} = \sqrt{\frac{120}{300}} = 0.632$

Maximum efficiency at 0.8 p.f. η_{max}

$$= \frac{0.632 \times 20 \times 10^3 \times 0.8}{0.632 \times 20 \times 10^3 \times 0.8 + 120 + 120}$$

$$= 0.9768 \text{ or } 97.68\ \%$$

Load at maximum efficiency is $0.632 \times 20 = 12.64$ kVA

(c) Explain the voltage regulation of a single phase transformer with the help of phasor diagram

Solution: Refer Article 6.11.

9. (a) Draw the equivalent circuit of a single-phase transformer. Draw teh phasor diagram.

Solution: Refer Article 3.9 and Article 3.8.

(b) Defined and derive the expression for the regulation of a single-phase transformer.

Solution: Refer Article 3.11.

(c) The primary and secondary windings of a 500 k VA transformer have resistance of 0.42 Ω and 0.0019 Ω respectively. The primary and secondary voltages are 11000 V and 415 V respectively and the core loss is 2.9 kW. Calculate the efficiency at (a) full load (b) half-load assuming the power factor of the load to be 0.8 lagging.

(WBUT 2009)

Solution:

Full-load primary current $I_1 = \dfrac{500 \times 10^3}{11,000} = 45.45\ A$

Full-load secondary current $I_2 = \dfrac{500 \times 10^3}{415} = 1204.82\ \text{A}$

Primary copper loss at full load = $(45.45)2 \times 0.42 = 867.595$ W
Secondary copper loss at full load = $(1204.82)2 \times 0.0019 = 2758.02$ W
Total copper losses at full load = 3625.615 W
(a) Full load efficiency at 0.8 pf lagging

$$= \frac{500 \times 10^3 \times 0.8}{500 \times 10^3 \times 0.8 + 2.9 \times 10^3 + 3625.615} \times 100\%$$

$$= 98.39\%$$

(b) Efficiency at half load and 0.8 pf lagging

$$= \frac{500 \times 10^3 \times 0.8 \times \frac{1}{2}}{500 \times 10^3 \times 0.8 \times \frac{1}{2} + 2.9 \times 10^3 + \left(\frac{1}{2}\right) \times 3625.615} \times 100\%$$

$$= 98.13\%$$

10. (a) Prove that the efficiency of the transformer is maximum when iron loss is equal to copper loss.
Refer Article 3.14.

(b) A 75 kVA transformer has 500 turns in the primary and 100 turns in the secondary The primary and secondary resistances are 0.4 Ω and 0.02 Ω respectively and corresponding leakage reactances are 1.5 Ω and 0.045 Ω respectively. The supply voltage is 6600 volts
Calculate,
(i) equivalent impedance referred to the primary
(ii) equivalent impedance referred to the secondary
(iii) the voltage regulation at power of 0.8 lagging. (WBUT 2009)

Solution

$N_1 = 500 \qquad N_2 = 100$
$r_1 = 0.4\Omega \quad r_2 = 0.02\Omega \quad x_1\ 1.5\Omega \quad x_2 = 0.045\Omega \quad V_1 = 6600\text{V}$
(i) equivalent impedance referred to the primary

$$Ze_1 = r_1 + jx_1 + r_2\left(\frac{N_1}{N_2}\right)^2 + j\,x_2\left(\frac{N_1}{N_2}\right)^2$$

$$= 0.4 + j1.5 + 0.02\left(\frac{500}{100}\right)^2\ j\,0.045\left(\frac{500}{100}\right)^2$$

$$= 0.9 + j\,2.625$$

(ii) Equivalent impedance reffered to secondary

$$Ze_2 = r_1 \left(\frac{N_2}{N_1}\right)^2 + jx_1 \left(\frac{N_2}{N_1}\right)^2 + r_2 + j\,x^2$$

$$= 0.4 \times \left(\frac{100}{500}\right)^2 + j1.5 \left(\frac{100}{500}\right)^2 + 0.02 + j\,0.045$$

$$= 0.036 + j\,0.105$$

(iii) Primary current $I = \dfrac{75,000}{6600} = 11.36$ A

Secondary current $I_2 = I_1 \dfrac{N_1}{N_2} = 11.36 \times \dfrac{500}{100} = 56.8$ A

Voltage regulation at power factor 0.8 lag is

$$\frac{I_2\, r_{e2} \cos\theta_2 + I_2\, x_{e2} \sin\theta_2}{E_2}$$

$$= \frac{56.8 \times 0.036 \times 0.8 + 56.8 \times 0.105 \times 0.6}{6600 \times \dfrac{100}{500}}$$

$$= \frac{5.214}{1320} = 0.00395 \text{ or } 0.395\ \%$$

11. Prove that the efficiency of transformer is maximum when iron loss is equal to copper loss. (WBUT 2012)

Solution: Refer Article 3.14.

12. (a) Explain the principle of operation of a transformer under loaded condition. (WBUT 2012)

Solution: Refer Article 3.8.

(b) A 200 kVA transformer has 400 turns on the primary and 40 turns on the secondary winding. The primary is connected to 2 kV, 50 Hz supply. Find the full load primary and secondary current, secondary *emf* and the maximum flux in the core. Neglect leakage drop and no-load primary current. (WBUT 2012)

Solution:

$N_1 = 400$

$N_2 = 40$

$V_1 = 2000$ V

$$\frac{V_1}{V_2} = \frac{N_1}{N_2}$$

or, $V_2 = \frac{N_2}{N_1} V_1 = \frac{40}{400} \times 2000 = 200$ V

kVA $= 200$

$$I_1 = \frac{200 \times 10^3}{2000} = 100 \text{ A}$$

$$I_2 = \frac{200 \times 10^3}{200} = 1000 \text{ A}$$

$E_1 = 4.44 f \phi_m N_1 = V_1$

$$\phi_m = \frac{V_1}{4.44 f N_1} = \frac{2000}{4.44 \times 50 \times 400} = 0.0225 \text{ wb} = 22.5 \text{ mwb}$$

13. (a) Explain why usually the low-voltage winding is excited and the high-voltage winding is open circuited for open-circuit test of a transformer? [WBUT 2013]

Solution: During open-circuit test of a transformer, the low-voltage winding is excited only for the sake of convenience. During open-circuit test, the rated voltage is applied to the primary of the transformer keeping the high-voltage side open circuited. As it is easy to apply rated voltage to the low-voltage side and also the instruments, i.e., voltmeter, ammeter and wattmeter, of corresponding ratings are readily available, open-circuit test is generally performed on the low-voltage side of the transformer.

(b) Why is the core of a transformer laminated? [WBUT 2013]

Solution: The core of a transformer is laminated to reduce the eddy-current loss.

14. Show that for a single-phase transformer, $E_P = 4.44 f \phi_m N_P$ where the symbols have their usual meanings. [WBUT 2014]

Solution: Refer Article 3.4.

15. (a) Draw the phasor diagram of a single-phase transformer under no-load condition. [WBUT 2014]

Solution: Refer Article 3.7.

(b) The efficiency at unity power factor of a 6600/384 V, 200 kVA single-phase transformer is 98%, both at full load and at half load. Calculate the full load Cu loss and core loss. [WBUT 2014]

Solution: Refer Example 3.21.

Multiple Choice Question

1. The regulation of a transformer is negative, if the load at the secondary side is (WBUT 2012)
   (a) resistive
   (b) inductive

(c) capacitive
(d) combination of resistive, inductive and capacitive

Answer: (c) capacitive

2. Iron loss of a transformer is 100 watts at half load. At full load, the iron loss would be (WBUT 2013)
   (a) 100 watts (b) 50 watts
   (c) 200 watts (d) 400 watts

   Answer: (a) 100 watts

3. In a transformer, the flux phasor
   (a) leads the induced emf by 90°
   (b) lags the induced emf by 90°
   (c) leads the induced emf by slightly less than 90°
   (d) lags the induced emf by slightly more than 90°

   Answer: (a) leads the induced emf by 90°

4. In a transformer, zero voltage regulation at full load is (WBUT 2014)
   (a) not possible
   (b) possible at unity power factor load
   (c) possible at leading power factor load
   (d) possible at lagging power factor load

   Answer: (c) possible at leading power factor load

5. Can a 50 Hz transformer be used for 25 Hz with input voltage rated for 50 Hz?
   (a) Yes, as V, I remains constant.
   (b) No, the flux is doubled which will drive the core to excessive saturation.
   (c) No, the current will become double.
   (d) Yes, at constant voltage, insulation will not be overstressed.

   Answer: (b) No, the flux is doubled which will drive the core to excessive saturation.

4 THREE-PHASE SYSTEM

4.1 THREE-PHASE ELECTRIC SYSTEM

A three-phase electric system may be considered as three separate single-phase systems displaced from each other by 120° [Fig. 4.1].

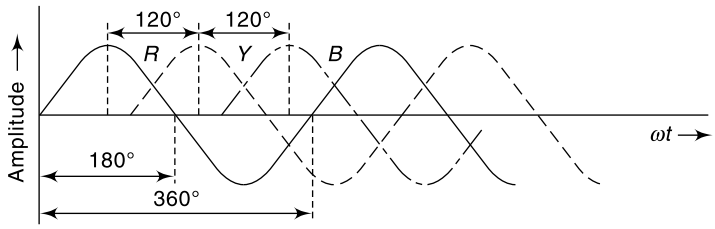


Fig. 4.1 *Graphical representation of a three-phase system*

4.2 ADVANTAGES OF A THREE-PHASE SYSTEM

The advantages of a three-phase system over a single-phase system are:

(a) The amount of conductor material required is less for three-phase system,
(b) domestic power and industrial/commercial power can be provided from the same source,
(c) voltage regulation of a three-phase system is better, and
(d) three-phase motors are self-starting while single-phase motors are not self-starting.

4.3 GENERATION OF THREE-PHASE BALANCED VOLTAGE

When three identical coils are placed with their axes at 120° displaced from each other and rotated in a uniform magnetic field, a sinusoidal voltage is generated across the coil. Figure 4.2 shows three sets of coils RR', YY' and BB' displaced from each other by 120° and rotating in an anticlockwise direction with angular

velocity ω in a uniform magnetic field. Since the three coils are identical the generated voltages have the same magnitude. The generated voltages in the coils are given by

$$v_R = V_m \sin \omega t$$
$$v_Y = V_m \sin (\omega t - 120°)$$
$$v_B = V_m \sin (\omega t - 240°)$$
$$= V_m \sin (\omega t + 120°).$$

[Here voltage generated in coil R is taken as reference. So v_Y lags v_R by 120° and v_B lags v_R by 240°.]

In polar form

$$v_R = |V| \angle 0°$$
$$v_Y = |V| \angle -120°$$
$$v_B = |V| \angle -240° = |V| \angle 120°.$$

The three phases may be numbered a, b, c or 1, 2, 3 or R, Y and B as customary and they may be given three colours—red, yellow and blue. The phase sequence is usually RYB. Vector rotation is usually anticlockwise.

The voltage waveform is shown in Fig. 4.1 and the phasor diagram is shown in Fig. 4.3. It can be shown that the phasor sum of three-phase emfs is zero.*

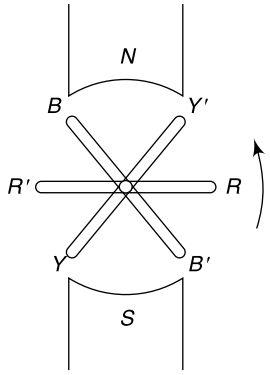


Fig. 4.2 *Three-phase emf generation*

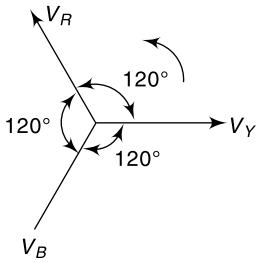


Fig. 4.3 *Vector representation of phase voltages*

4.4 INTERCONNECTION OF PHASES

If the three coils RR', YY' and BB' are not interconnected but kept separate as shown in Fig. 4.4 then each phase would require two conductors and so the total number of conductors would be six. This would make the whole system complicated. Hence the three phases are usually interconnected which results in substantial saving of copper.

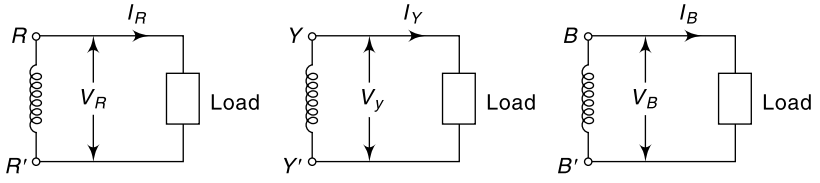


Fig. 4.4 *Three-phase coils not interconnected*

*Resultant instantaneous emf

$$= v_R + v_Y + v_B = V_m \sin \omega t + V_m \sin (\omega t - 120°) + V_m \sin (\omega t - 240°)$$
$$= V_m [\sin \omega t + 2 \sin (\omega t - 180°) \cos 60°]$$
$$= V_m [\sin \omega t - 2 \sin \omega t \times \frac{1}{2}] = 0.$$

The general methods of interconnections are
(a) *Star (or Y) connection*
(b) *Mesh or delta (Δ) connection.*

4.4.1 Star (or Y) Connection

Here the similar ends of the coils, i.e. either *a*, *b* and *c* are joined together (or *a′*, *b′* and *c′* are joined together) at point *N* known as "*neutral*" point or *star* point. In Fig. 4.5 a conductor is connected at point *N* which is known as the *neutral conductor*. Such a system is known as a *three-phase four wire* system.

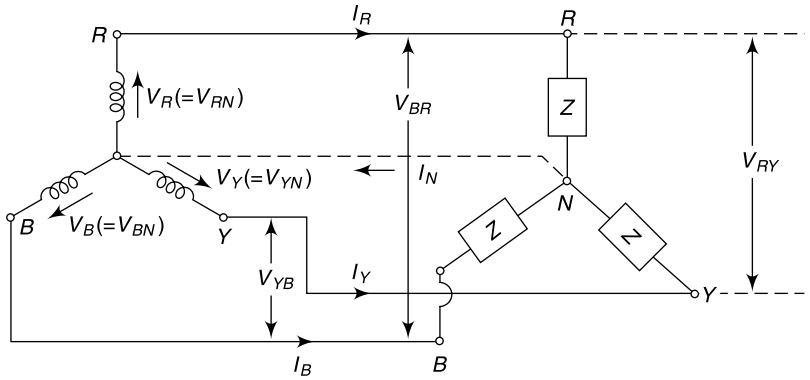


Fig. 4.5 ***Diagrammatic view of star connection***

If a balanced symmetrical load *Z* is connected across terminals *RY*, *YB* and *BR* then the currents in each phase will be exactly equal in magnitude but displaced 120° from each other (provided the supply voltage is balanced).
The resultant current is then given by

$$i_R + i_Y + i_B = I_m \sin \omega t + I_m \sin (\omega t - 120°) + I_m \sin (\omega t - 240°).$$

The current through the neutral in case of balanced load is zero
i.e. $I_N = I_R + I_Y + I_B = 0.$

The potential difference between any terminal and neutral gives the *phase voltage* and that between any two line terminals, i.e. *R*, *Y*, *B* gives the *line voltage*. In Fig. 4.5, V_R, V_Y and V_B are phase voltages of phases *R*, *Y* and *B* respectively while V_{RY}, V_{YB} and V_{BR} are the line voltages. If these voltages are equal in magnitude and displaced from each other by 120° (elect.) then they are called balanced voltages.

Relation between Line and Phase Voltages in Star Connection The potential difference between lines *R* and *Y* is

$$V_{RY} = V_R - V_Y \text{ (vector difference).}$$

V_{RY} can be found by compounding V_R and V_Y (reversed). Its value is given by the diagonal of the parallelogram of Fig. 4.6. Obviously, the angle between V_R and V_Y (reversed) is 60°.

Assuming $|V_R| = |V_Y| = |V_B| = |V_{Ph}|$(the phase emf),

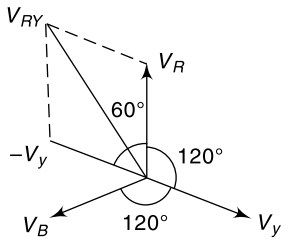


Fig. 4.6 ***Vectorial addition of phase voltages***

$$|V_{RY}| = \sqrt{V_R^2 + V_Y^2 + 2V_R V_Y \cos 60^\circ} = \sqrt{V_{\text{Ph}}^2 + V_{\text{Ph}}^2 + 2V_{\text{Ph}}^2 \times \frac{1}{2}}$$

$$= \sqrt{3}\, V_{\text{Ph}} \text{ (i.e., } \sqrt{3} \text{ times magnitude of } V_{\text{Ph}}).$$

Similarly, $V_{YB} = V_Y - V_B$ (vector difference)

$$= \sqrt{3}\, V_{\text{Ph}} \text{ and}$$

$$V_{BR} = V_B - V_R = \sqrt{3}\, V_{\text{Ph}}.$$

However, $|V_{RY}| = |V_{YB}| = |V_{BR}|$ = Line voltage $|V_L|$.

Hence in star connection

$$|V_L| = \sqrt{3}\, |V_{\text{Ph}}|. \qquad (4.1)$$

It may be noted from Fig. 4.7 that

(a) Line voltages are also 120° apart.
(b) Line voltages are 30° ahead of their respective phase voltages.
(c) The angle between the line currents and the corresponding line voltages is $(30^\circ + \theta)$ assuming current lagging by an angle θ° (for lagging loads)

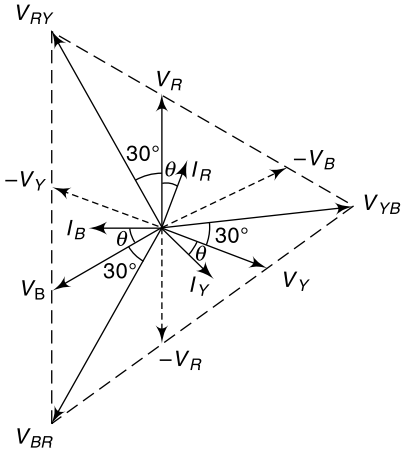


Fig. 4.7 ***Complete vector diagram for voltages in star connection***

Relation between Line and Phase Currents in Star Connection Observation of Fig. 4.5 reveals that each line is in series with its individual phase winding. Hence the line current in each line is the same as the current in the phase winding to which the line is connected.

Let current in line R be I_R, current in line Y be I_Y and current in line B be I_B.

Since $|I_R| = |I_Y| = |I_B| = |I_{\text{Ph}}|$ (say phase current), in star connection, *line current is same as the phase current* i.e. $|I_L| = |I_{\text{Ph}}|$.

Power in Star Connection The total *active* or *real power* P in the circuit is the sum of the three phase powers. Hence total active power

$$P = 3 \times \text{individual phase power} = 3V_{\text{Ph}} I_{\text{Ph}} \cos\theta$$

$$= 3 \times \frac{V_L}{\sqrt{3}} I_L \cos\theta$$

$$= \sqrt{3}\, V_L I_L \cos\theta \; [\because V_L = \sqrt{3}\, V_{\text{Ph}} \text{ and } I_L = I_{\text{Ph}}]. \qquad (4.2)$$

It should be noted that θ is the angle between phase voltage and phase current and V_L, I_L are magnitude vectors.

Similarly, total *reactive power* Q is given by $Q = \sqrt{3}\, V_L I_L \sin\theta$ (4.3)

[By convention reactive power of an inductive coil is taken as positive and that of a capacitor as negative]

S, the *total apparent power* or *complex power* of the three phases is

$$S = \sqrt{P^2 + Q^2} = \sqrt{3}\; V_L I_L. \qquad (4.4)$$

Also, $S = P + jQ.$ (4.4(a))

4.4.2 Delta (Δ) or Mesh Connection

In this configuration, the dissimilar ends of three phase windings are joined together, i.e. R is joined with Y', Y with B' and B with R' (or R is joined with B', B with Y' and Y with R'). In other words, the three windings are joined in series to form a closed mesh as shown in Fig. 4.8. The leads are taken out from the three junctions for external connection. If the system is balanced then the sum of the three voltages round the closed mesh is zero, hence no current (of fundamental frequency) can flow around the mesh when the terminals are open. At any instant, the emf of one phase is equal and opposite to the resultant of those in the other two phases. This type of connection is referred to as a three-phase, three-wire delta connection.

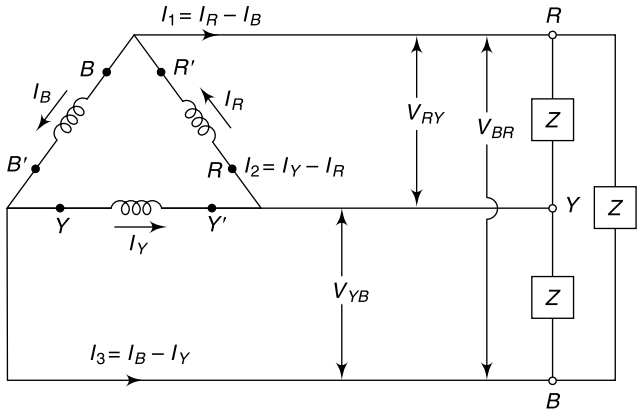


Fig. 4.8 *Delta connection*

Relation between Line Voltages and Phase Voltages in Delta Connection It is seen from Fig. 4.8 that there is only one phase winding completely included between any pair of terminals. Hence in Δ connection, the voltage between any pair of lines is equal to the corresponding phase voltage. Since the common phase sequence is RYB, V_{RY} leads V_{YB} by 120°, V_{YB} leads V_{BR} by 120° (as shown in Fig. 4.9).

If $|V_{RY}| = |V_{YB}| = |V_{BR}|$ = line voltage $|V_L|$, then it is seen that $|V_L| = |V_{\text{Ph}}|$.

Relation between Line Currents and Phase Currents in Delta Connection It is seen from Fig. 4.8 that current in each line is the vector difference of the two-phase currents flowing through that line (i.e. vector difference of corresponding phase currents).

Hence, Current in line R is $I_1 = I_R - I_B$
Current in line Y is $I_2 = I_Y - I_R$
Current in line B is $I_3 = I_B - I_Y$
} vector difference

Current in line R is found by compounding I_R and I_B (reversed) and its value is given by the diagonal of the parallelogram shown in Fig. 4.9. The angle between I_R and I_B (reversed) is 60°.

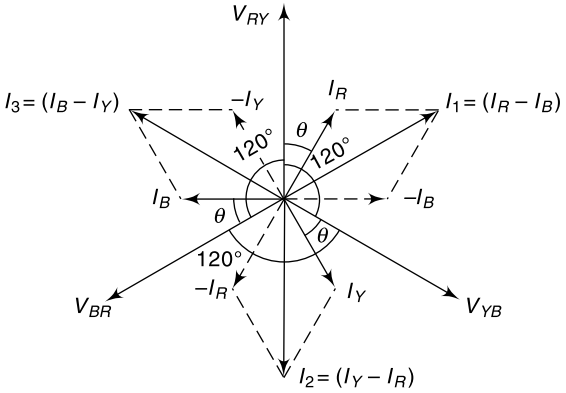


Fig. 4.9 ***Vector resolution of currents***

The current in line R is: $I_1 = \sqrt{I_R^2 + I_B^2 + 2 I_R I_B \cos 60°}$

$$= \sqrt{I_{\text{Ph}}^2 + I_{\text{Ph}}^2 + 2 I_{\text{Ph}}^2 \times \frac{1}{2}}$$

$= \sqrt{3}\, I_{\text{Ph}}$ (i.e., $\sqrt{3}$ times magnitude of phase current).

Current in line Y is: $I_2 = I_Y - I_R$ (vector difference) $= \sqrt{3}\, I_{\text{Ph}}$ and current in line B is: $I_3 = I_B - I_Y$ (vector difference) $= \sqrt{3}\, I_{\text{Ph}}$.

Assuming all the line currents are equal in magnitude,

$$[|I_1| = |I_2| = |I_3| = |I_L|]\ I_L = \sqrt{3}\, I_{\text{Ph}}. \tag{4.5}$$

With reference to Fig. 4.9 it should be noted that:

(a) line currents are 120° apart
(b) line currents are 30° behind the respective phase currents
(c) the angle between the line currents and corresponding line voltages is (30° + θ) with the current lagging by an angle θ.

Power in Delta Connection

Three-phase power

$P = 3 \times$ individual phase powers

$$= 3\, V_{\text{Ph}} I_{\text{Ph}} \cos\theta$$

$$= 3 V_L \frac{I_L}{\sqrt{3}} \cos\theta = \sqrt{3}\, V_L I_L \cos\theta \tag{4.6}$$

($\because$ $V_{\text{Ph}} = V_L$ and $I_L = \sqrt{3}\, I_{\text{Ph}}$)

[Here, V_{Ph}, I_{Ph}, V_L and I_L are magnitude of the respective phasors.]

Similarly, the total reactive power is given by

$$Q = \sqrt{3}\ V_L I_L \sin\theta \tag{4.7}$$

and the total apparent or complex power of the 3-phase delta circuit is given by

$$S = \sqrt{P^2 + Q^2} = \sqrt{3}\, V_L I_L \tag{4.8}$$

Also, $S = P + jQ$ [4.8(a)]

4.5 ONE-LINE EQUIVALENT CIRCUIT FOR BALANCED LOADS

We know that a set of three equal impedances in delta connection is equivalent to another set of three equal star connected impedances. Therefore, a more direct computation of the star circuit is possible for balanced three phase loads of either type.

The one line equivalent circuit is one phase of the three phase, four wire, star connected circuit in Fig. 4.10 except that a voltage is used which has the line to neutral magnitude and a zero phase angle. The line current calculated for this circuit has a phase angle with respect to the phase angle of zero on the voltage. Then the actual line currents I_R, I_Y and I_B will lead or lag their respective line to neutral voltages by this same phase angle.

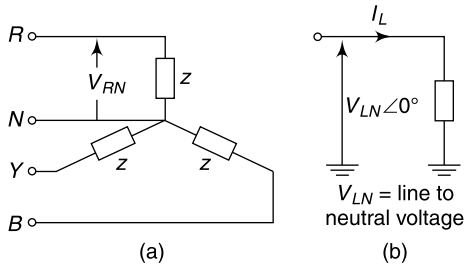


Fig. 4.10 *One line equivalent of one phase*

4.1 Three chokes each of resistance 40 Ω and reactance 30 Ω are connected in star to a 3-phase 440 V balanced supply. What is the line current and the total power dissipated?

Solution

Given, Resistance R = 40 Ω
Reactance X = 30 Ω.

$\therefore$ impedance $Z = \sqrt{R^2 + X^2} = \sqrt{(40)^2 + (30)^2} = 50\ \Omega$

Also, line voltage V_L = 440 V.

$\therefore$ In a star connected system

Phase voltage $$|V_{\text{Ph}}| = \frac{|V_L|}{\sqrt{3}} = \frac{440}{\sqrt{3}} = 254.04 \text{ V:}$$

phase current $$|I_{\text{Ph}}| = \frac{|V_{\text{Ph}}|}{|Z|} = \frac{254.04}{50} = 5.08 \text{ A.}$$

In a star connected system

Line current = Phase current = 5.08 A.

Total power dissipated is ($\sqrt{3}\ |V_L|\ |I_L| \cos\theta$), where

$$\cos\theta = \text{power factor} = \frac{|R|}{|Z|} = \frac{40}{50} = 0.8.$$

Hence total power dissipated is ($\sqrt{3} \times 440 \times 5.08 \times 0.8$) = 3094.18 W or 3.097 kW.

4.2 The load in each branch of a star connected three-phase circuit consists of 10 Ω resistance and 0.06 H inductance in series. The line voltage is 430 V. Calculate the phase voltage and the phase current.

Solution

Resistance $R = 10\ \Omega$

Reactance $X = \omega L = 2\pi fL = 2\pi \times 50 \times .06 = 18.85\ \Omega$

$\therefore$ Impedance $|Z| = \sqrt{R^2 + X^2} = \sqrt{(10)^2 + (18.85)^2} = 21.34\ \Omega$

Line voltage $|V_L| = 430$ V (given).

In a star connected system, line voltage = $\sqrt{3} \times$ phase voltage

So phase voltage $|V_{Ph}| = \dfrac{|V_L|}{\sqrt{3}} = \dfrac{430}{\sqrt{3}} = 248.27$ V

Phase current $|I_{Ph}| = \dfrac{|V_{Ph}|}{Z} = \dfrac{248.27}{21.34} = 11.63$ A.

4.3 Three similar coils each having series resistance of 20 Ω and capacitance 100 μF are connected in star to a 3-phase, 400 V, 50 Hz balanced supply. Find the line current, power factor, total kVA and total kW.

Solution

Resistance $R = 20\ \Omega$

Capacitance $C = 100 \times 10^{-6}$ F.

$\therefore$ Capacitive reactance $|X_C| = \dfrac{1}{\omega C} = \dfrac{1}{2\pi \times 50 \times 100 \times 10^{-6}} = \dfrac{100}{\pi}\ \Omega$

$= 31.83\ \Omega.$

Impedance $|Z| = \sqrt{R^2 + X_c^2}$

$= \sqrt{(20)^2 + (31.82)^2} = 37.59\ \Omega.$

Line voltage $|V_L| = 400$ V (given)

$\therefore$ Phase voltage is $|V_{Ph}| = \dfrac{|V_L|}{\sqrt{3}} = \dfrac{400}{\sqrt{3}} = 230.95$ V,

while, phase current $|I_{Ph}| = \dfrac{|V_{Ph}|}{Z} = \dfrac{230.95}{37.59} = 6.144$ A.

$\therefore$ Line current $|I_L| = |I_{Ph}| = 6.144$ A

Power factor $(\cos\theta) = \dfrac{R}{|Z|} = \dfrac{20}{37.59} = 0.53$

Total power $(\text{KVA}) = 3|V_{Ph}|\,|I_{Ph}| = (3 \times 230.95 \times 6.144 \times 10^{-3})$ kVA

$= 4.257$ kVA

Total active power $(\text{kW}) = 3|V_{Ph}|\,|I_{Ph}| \cos\theta$

$= (3 \times 230.95 \times 6.144 \times 0.53 \times 10^{-3})$ kW $= 2.256$ kW.

4.4 Each phase of a delta connected load comprises a resistor of 50 Ω and a series capacitor of 50 μF. Calculate the line and phase currents when the load is connected to a 440 V, 3 phase, 50 Hz supply.

Solution

Load resistance $R = 50\ \Omega$

Capacitive reactance $|X_C| = \frac{1}{\omega C} = \frac{1}{2\pi fc} = \frac{1}{2\pi \times 50 \times 50 \times 10^{-6}}$

$= 63.67\ \Omega.$

$\therefore$ Load impedance per phase $|Z| = \sqrt{R^2 + X_C^2} = 80.96\ \Omega.$

Phase current $|I_{Ph}| = \frac{|V_{Ph}|}{|Z|}$, where V_{Ph} is the phase voltage.

In delta connected system line voltage $|V_L|$ = phase voltage $|V_{Ph}|$

Here, $|V_{Ph}| = |V_L| = 440$ V

Therefore, $|I_{Ph}| = \frac{440}{80.96} = 5.434$ A.

In delta connected system line current $|I_L| = \sqrt{3}\, I_{Ph}$

$\therefore$ $|I_L| = \sqrt{3} \times 5.434 = 9.412$ A.

4.5 The load in each branch of a delta connected balanced three-phase circuit consists of an inductance of 0.0318 H in series with a resistance of 10 Ω. The line voltage is 400 V (balanced) at 50 Hz. Calculate the (i) line current and (ii) the total power in the circuit.

Solution

Inductive reactance $|X_L| = \omega L = 2\pi fL = 2\pi \times 50 \times 0.0318 = 10\ \Omega$

Resistance $R = 10\ \Omega$.

So load impedance, $|Z| = \sqrt{(10)^2 + (10)^2} = 14.14\ \Omega.$

Line voltage, $|V_L| = 400$ V (given)

$\therefore$ Phase voltage $|V_{Ph}| = |V_L| = 400$ V [$\because$ connection is delta]

Phase current $|I_{Ph}| = \frac{|V_{Ph}|}{|Z|} = \frac{400}{14.14}$ A $= 28.288$ A.

(i) Line current $|I_L| = \sqrt{3} \times$ phase current $= \sqrt{3} \times 28.29 = 49$ A.

(ii) Total power in the circuit $(P) = \sqrt{3}\, |V_L|\, |I_L| \cos\theta$

$\therefore$ $\cos\theta$ = power factor $= \frac{R}{|Z|} = \frac{10}{14.14} = 0.707.$

Also, total power in the circuit

$(P) = \sqrt{3} \times 400 \times 49 \times 0.707 = 24{,}000.37$ W $\quad 24$ kW.

4.6 A star connected three-phase load draws a current of 20 A at a lagging p.f. of 0.9 from a balanced 440 V, 50 Hz supply. Find the circuit elements in each phase if the elements are connected in series.

Solution

Line current, $|I_L| = 20$ A

Power factor, $\cos\theta = 0.9$ (lagging)

Line voltage = $|V_L| = 440$ V (given).

$\therefore$ Phase voltage, $|V_{Ph}| = \frac{|V_L|}{\sqrt{3}} = \frac{440}{\sqrt{3}}$ V.

As the power factor is lagging hence the circuit contains resistance R in series with inductance L.

If X_L be the inductive reactance and Z be the impedance then, $\frac{R}{|Z|} = 0.9$

and $$|Z| = \frac{|V_{Ph}|}{|I_{Ph}|} = \frac{\frac{440}{\sqrt{3}}}{|I_L|} = \frac{440}{\sqrt{3} \times 20} \ \Omega = 12.7\ \Omega$$

($|I_{Ph}| = |I_L|$ as the load is star connected).

$\therefore$ $$R = 12.7 \times 0.9 = 11.43\ \Omega$$

and $$|X_L| = \sqrt{Z^2 - R^2} = \sqrt{(12.7)^2 - (11.43)^2} = 5.536\ \Omega$$

Therefore, $$L = \frac{X_L}{\omega} = \frac{5.536}{2\pi f} = \frac{5.536}{2\pi \times 50} = 0.0176 \text{ H.}$$

The circuit elements are resistance of 11.43 Ω and inductor of 0.0176 H connected in series in each phase.

4.7 Three coils are connected in star to a balanced three-phase, 3-wire, 440 V, 50 Hz supply and takes a line current of 10 A at 0.9 p.f. lagging. Calculate the resistance and reactance of the coils assuming they are series connected in each phase. If the coils are delta connected to the same supply calculate the line current and the real power.

Solution

Line voltage $|V_L| = 440$ V

Line current $|I_L| = 10$ A

When the coils are star connected,

phase voltage $$|V_{Ph}| = \frac{|V_L|}{\sqrt{3}} = \frac{440}{\sqrt{3}} = 254 \text{ V,}$$

phase current $$|I_{Ph}| = |I_L| = 10 \text{ A}$$

If R, X and Z be the resistance, reactance and impedance respectively then,

$$|Z| = \frac{|V_{Ph}|}{|I_{Ph}|} = \frac{254}{10} = 25.4\ \Omega$$

$$\text{p.f.} = \cos\theta = 0.9 = \frac{|R|}{|Z|}.$$

So $$R = 25.4 \times 0.9 = 22.86\ \Omega.$$

Therefore, $$|X| = \sqrt{Z^2 - R^2} = \sqrt{(25.4)^2 - (22.8)^2}$$
$$= 11.19\ \Omega.$$

The resistance and reactance of the coil are 22.86 Ω and 11.9 Ω respectively.

Line voltage of supply system $|V_{L_1}| = \sqrt{3}\,|V_{Ph_1}|$

$= \sqrt{3} \times 230$ V

$= 398.36$ V (as it is star connected).

Line voltage of load $|V_{L_2}| = |V_{L_1}| = 398.36$ V

and phase voltage of load $|V_{Ph_2}| = |V_{L_2}| = 398.36$ V (as load is delta connected).

Hence phase current in load is given by $|I_{Ph_2}| = \frac{|V_{Ph_2}|}{Z}$

$= \frac{398.36}{10} = 39.8$ A.

Line current of load is obtained as $|L_{L_2}| = \sqrt{3}\,|I_{Ph_2}|$

$= \sqrt{3} \times 39.836 = 69$ A.

Now, when the coils are delta connected to the same supply

$$|V_L| = 440 \text{ V}, |Z| = 25.4\ \Omega \text{ and } (\cos\theta) = 0.9.$$

$$\text{Phase voltage } |V_{\text{Ph}}| = |V_L| = 440 \text{ V}$$

$$\text{Phase current } |I_{\text{Ph}}| = \frac{|V_{\text{Ph}}|}{|Z|} = \frac{440}{25.4} \text{ A} = 17.32 \text{ A}.$$

$$\text{Line current } |I_L| = \sqrt{3}\,|I_{\text{Ph}}| = \sqrt{3} \times 17.32 = 30 \text{ A}.$$

$$\text{Real power } (P) = \sqrt{3}\,|V_L|\,|I_L| \cos\theta$$

$$= \sqrt{3} \times 440 \times 30 \times 0.9 = 20576.32 \text{ W} = 20.577 \text{ kW}.$$

4.8 For a three-phase delta connected load, each phase of which has series resistance of 8 Ω and reactance of 6 Ω is supplied from a star connected balanced system having a phase voltage of 230 V. Calculate (a) magnitude of the phase current of the load and the supply system (b) active power taken by the load and the power factor of the load.

Solution

Impedance of load $|Z| = \sqrt{8^2 + 6^2} = 10\ \Omega$.

(The system is shown in Fig. 4.11).

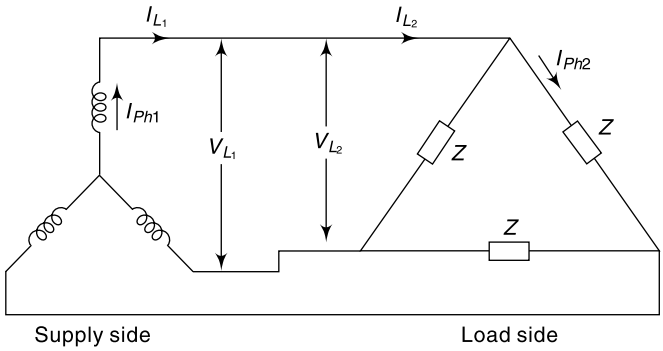


Fig. 4.11 *Circuit of Ex. 7.8 [Z = (8 + j6) Ω]*

Phase voltage of supply system $|V_{\text{Ph}_1}| = 230$ V.

(a) The line current of the supply system $|I_{L_1}| = |I_{L_2}| = \left(\frac{\sqrt{3} \times 230}{\sqrt{8^2 + 6^2}} \times \sqrt{3}\right) = 69\text{A}.$

(b) Power factor of the load is $\cos\theta = \frac{R}{|Z|} = \frac{8}{10} = 0.8$

Active power taken by the load $= \sqrt{3}\,|V_{L_2}|\,|I_{L_2}| \cos\theta$

$= \sqrt{3} \times 398.36 \times 69 \times 0.8$ W

$= 38086.88$ W $= 38.08$ kW.

4.9 A star connected load has an impedance of $(3 + j4)\ \Omega$ in each phase and is connected across a balanced 3-phase delta connected alternator having line voltage of 120 V. Obtain the line currents of both the load and generator.

Solution

For the load, $Z_{\text{Ph}} = 3 + j4 = 5\angle 53.13°\ \Omega$.

Magnitude of phase voltage $|V_{Ph}| = \dfrac{120}{\sqrt{3}} = 69.28$ V.

The line currents (as the load is star connected hence line and phase currents are equal) in phase R, Y and B of the load are

$$I_R = \frac{69.28}{5\angle 53.13^\circ}\angle 0^\circ = 13.86\angle -53.13^\circ \text{ A}$$

$$I_Y = \frac{69.28}{5\angle 53.13^\circ}\angle -120^\circ = 13.86\angle -173.13^\circ \text{ A}$$

and $$I_B = \frac{69.28}{5\angle 53.13^\circ}\angle -240^\circ = 13.86\angle 66.87^\circ \text{A}$$

As the star connected load is connected with the delta connected alternator hence the line current of the alternator is same as that of the line current of the load, i.e. $13.86\angle -53.13^\circ$ A, $13.86\angle -173.13^\circ$ A and $13.86\angle 66.87^\circ$ A.

4.10 A balanced star connected load has an impedance of $(2 + j3.46)\ \Omega$ between line and neutral. If the voltage across phase R be $20\angle 30^\circ$ volts, find current in phases Y and B. What is the voltage from line Y to neutral. Also obtain V_{RB}.

Solution

$$V_{RN} = 20\angle 30^\circ \text{ V}$$

$$Z_{ph} = 2 + j3.46 = 4\angle 60^\circ\ \Omega.$$

Hence $$I_{RN} = \frac{20\angle 30^\circ}{4\angle 60^\circ} \text{ A} = 5\angle -30^\circ \text{ A}.$$

If current in phase R is $5\angle -30^\circ$ A, currents in phases Y and B will be lagging by 120° and 240° respectively with respect to current in phase R.

Hence current in phase $Y = 5\angle(-30^\circ - 120^\circ)$ A $= 5\angle -150^\circ$ A

And current in phase $B = 5\angle(-30^\circ - 240^\circ) = 5\angle -270^\circ = 5\angle 90^\circ$ A.

Also, voltage across phase B is lagging with respect to phase R by 240°.

Hence $V_{BN} = 20\angle(30^\circ - 240^\circ) = 20\angle -210^\circ = 20\angle 150^\circ$ V.

Therefore, $$V_{RB} = V_{RN} - V_{BN} = 20\angle 30^\circ - 20\angle 150^\circ$$
$$= 20\{0.866 + j0.5 + 0.866 - j0.5\}$$
$$= 34.64\angle 0^\circ \text{ V}.$$

4.6 MEASUREMENT OF POWER IN A THREE-PHASE THREE-WIRE SYSTEM

Case (a): Star connected balanced load (with neutral point accessible). If a wattmeter W be connected with its current coil in one line and the voltage coil between that line and the neutral point, as shown in Fig. 4.12, the reading on the wattmeter gives the power per phase.

Therefore, total active power = 3 × wattmeter reading.

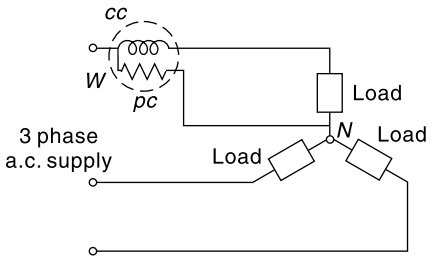


Fig. 4.12 *Measurement of power in a star connected balanced load*

Case (b): Balanced or unbalanced load (star or delta) The two wattmeter

method. Suppose the loads Z_1, Z_2 and Z_3 are connected in star as shown in Fig. 4.13. Current coils of the two wattmeters are connected in any two lines, say the 'red' and 'blue' lines, and the voltage circuits are connected between these lines and the yellow phase. Suppose v_{RN}, v_{YN} and v_{BN} be the instantaneous values of the potential differences across the loads, these p.d.s are assumed positive. Also suppose I_R, I_Y and I_B to be the corresponding instantaneous values of the line (and phase) currents.

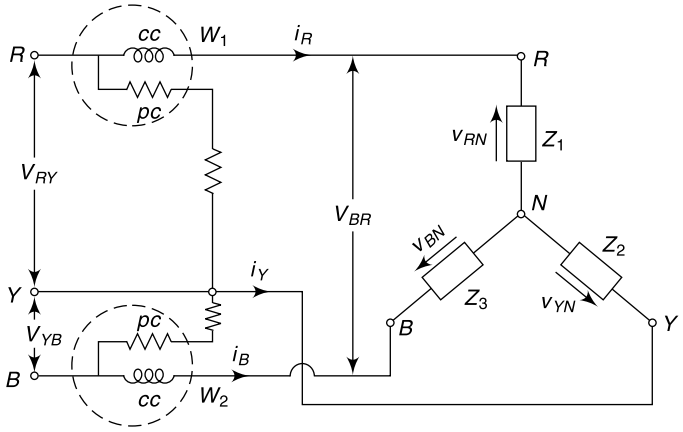


Fig. 4.13 ***Measurement of three-phase power by two wattmeters***

Therefore, instantaneous power in load $Z_1 = i_R \cdot v_{RN}$,
instantaneous power in load $Z_2 = i_Y \cdot v_{YN}$
instantaneous power in load $Z_3 = i_B \cdot v_{BN}$
Total instantaneous power $= i_R \cdot v_{RN} + i_Y \cdot v_{YN} + i_B \cdot v_{BN}$. (4.9)
From Fig. 4.13 it is seen that:
Instantaneous current through current coil of $W_1 = i_R$.
Instantaneous p.d. across voltage coil of $W_1 = v_{RN} - v_{YN}$.
Hence instantaneous power measured by W_1 is $i_R(v_{RN} - v_{YN})$.
Similarly, instantaneous power measured by W_2 is $i_B(v_{BN} - v_{YN})$.
Sum of the instantaneous powers of W_1 and W_2 being W,

$$W = i_R(v_{RN} - v_{YN}) + i_B(v_{BN} - v_{YN})$$
$$= i_R \cdot v_{RN} + i_B \cdot v_{BN} - (i_R + i_B)v_{YN} \quad (4.10)$$

From Kirchhoff's first law, the algebraic sum of the instantaneous current at N being zero,
we have $i_R + i_Y + i_B = 0$ or $i_R + i_B = -i_Y$
Therefore, sum of the instantaneous powers of W_1 and W_2 becomes

$$W = i_R \cdot v_{RN} + i_B \cdot v_{RN} + i_Y \cdot v_{YN}$$
$$= \text{total instantaneous power.} \quad (4.11)$$

Actually, the power measured by each wattmeter varies from instant to instant, but the inertia of the moving system causes the pointer to read the average value of the power. Hence the sum of the wattmeter readings gives the average value of the total power absorbed by the three phases.

Since the above proof does not assume a balanced load or sinusoidal waveforms, it follows that the sum of the two wattmeter readings gives the total power under all conditions. The above proof was derived for a star-connected load and it is a useful exercise to prove that the same conclusion holds for a delta connected load.

4.7 MEASUREMENT OF POWER FOR A THREE-PHASE SYSTEM USING TWO WATTMETERS (ASSUMING BALANCED LOAD AND SINUSOIDAL VOLTAGES AND CURRENTS)

Suppose Z in Fig. 4.13 represents three similar loads connected in star and let V_{RN}, V_{YN} and V_{BN} be the rms values of the voltages per phase. Since the voltages and currents are assumed sinusoidal, they can be represented by phasors as shown in Fig. 4.14, while the currents being assumed to lag by an angle θ behind the corresponding phase voltages.

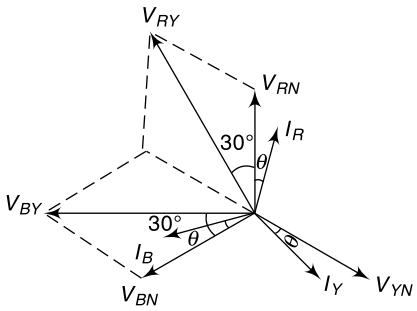


Fig. 4.14 *Phasor diagram for Fig. 4.13*

Current through current coil of W_1 is I_R and p.d. across voltage coil of W_1 is $V_{RN} - V_{YN} = V_{RY}$ (line voltage).

Phase difference between I_R and V_{RY} is $(30° + \theta)$.

Therefore, reading on $W_1 = I_R V_{RY} \cos (30° + \theta)$.

Current through current coil of W_2 is I_B.

P.d. across voltage coil of W_2 is $V_{BN} - V_{YN} = V_{BY}$.

Phase difference between I_B and $V_{BY} = (30° - \theta)$.

Therefore reading on W_2 is $I_B V_{BY} \cos (30° - \theta)$.

Since the load is balanced,

$$I_R = I_Y = I_B = I_L \text{ (numerically)}$$

and $$V_{RY} = V_{BY} = V_L \text{ (numerically)}$$

hence $$P_1 = I_L V_L \cos (30° + \theta) = W_1 \quad (4.12)$$

and $$P_2 = I_L V_L \cos (30° - \theta) = W_2 \quad (4.13)$$

$$\begin{aligned} P_1 + P_2 &= I_L V_L [\cos (30° + \theta) + \cos (30° - \theta)] \\ &= I_L V_L [\cos 30° \cos \theta - \sin 30° \sin \theta \\ &\qquad + \cos 30° \cos \theta + \sin 30° \sin \theta] \\ &= \sqrt{3}\, I_L V_L \cos \theta = W_1 + W_2. \end{aligned} \quad (4.14)$$

This is the expression deduced for the total power in a balanced 3-phase system. This is an alternative method of proving that the sum of the two wattmeter readings gives the total power, but it should be noted that this proof assumes a balanced load and sinusoidal voltages and currents.

From Eqs (4.12), (4.13) and (4.14), $P_2 - P_1 = I_L V_L \sin \theta$ and

$$\tan \theta = \frac{\sin \theta}{\cos \theta} = \sqrt{3}\,\frac{P_2 - P_1}{P_2 + P_1} = \sqrt{3}\,\frac{W_2 - W_1}{W_2 + W_1}. \quad (4.15)$$

From the above it may be noted that if $\theta = 0°$, $W_1 = W_2$; for $\theta < 60°$, both W_1 and W_2 are positive. On the other hand, if $\theta = 30°$, $W_2 = 0$; for $\theta > 60°$, W_1 becomes negative. In such a case, the connection of either the current coil on the voltage coil are made reverse and then the reading is recorded. Under this condition the sign of W_1 is taken as negative in the calculations.

4.8 UNBALANCED FOUR-WIRE STAR CONNECTED LOAD

With such a system the neutral conductor will carry current; also the voltage across each of the load impedances remains fixed with the same magnitude as the line to neutral voltage. The line currents are unequal and do not have a 120° phase difference.

4.9 UNBALANCED DELTA CONNECTED LOAD

If the three (line) voltages across the terminals of an unbalanced delta connected load are fixed, the voltage drop across each phase impedance is known. The currents in each phase can, therefore, be determined directly. The line currents can then be found from the phasor sum of the two component currents coming towards or flowing away from the line terminal. It will be noted that in this case (unlike with the balanced loads) the line currents will not be equal nor will they have a 120° phase difference.

4.10 UNBALANCED THREE-WIRE STAR CONNECTED LOAD

With such a system the common point O in Fig. 4.15 of the three load impedances will not be at the potential of the neutral and the voltages across the three impedances can vary considerably from line to neutral magnitude. (The displacement of O from N is known as the *displacement neutral voltage*).

There can be two approaches to the problem. The first is to determine with reference to Fig. 4.15 the three line currents I_A, I_B and I_C by writing the mesh currents (based on KVL) and then determining the voltages across the three impedances V_{AO}, V_{BO} and V_{CO} as the product of line current and the corresponding impedances (i.e. $V_{AO} = I_A Z$ etc.). The displacement neutral voltage V_{ON}, O being the common point of the impedances and N the neutral in Fig. 4.16, is then $V_{ON} = V_{OA} + V_{AN} = (V_{OB} + V_{BN} = V_{OC} + V_{CN})$, where V_{OA}, V_{OB} and V_{OC} have all been determined already and V_{AN}, V_{BN}, V_{CN} are known system phase voltages.

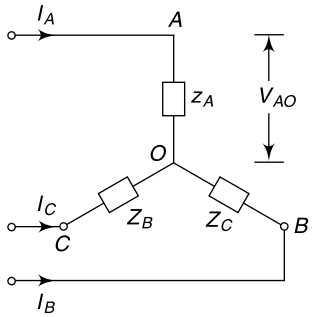


Fig. 4.15 ***Unbalanced three-wire star connected load***

The second is to obtain the displacement neutral voltage in the very beginning. For this we write line currents in terms of the load voltages and load admittances. Referring to Fig. 4.16 again,

$$I_A = V_{AO}Y_A,\ I_B = V_{BO}Y_B,\ I_C = V_{CO}Y_C \quad (4.16)$$

Applying Kirchhoff's current law at point O in Fig. 4.15 we may write

$$I_A + I_B + I_C = 0 \quad (4.17)$$

or $$V_{AO}Y_A + V_{BO}Y_B + V_{CO}Y_C = 0 \quad (4.18)$$

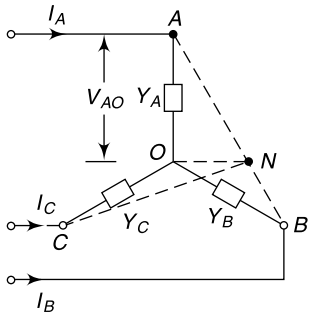


Fig. 4.16 ***Unbalanced three-wire star connected load***

Referring to Fig. 4.16 the voltages V_{AO}, V_{BO} and V_{CO} can be expressed in terms of their two component voltages, i.e.

$$\left.\begin{aligned} V_{AO} &= V_{AN} + V_{NO} \\ V_{BO} &= V_{BN} + V_{NO} \\ V_{CO} &= V_{CN} + V_{NO} \end{aligned}\right\} \quad \text{(all phasor additions)} \quad (4.19)$$

Substituting the expression of (4.19) in (4.18) we obtain

$$(V_{AN} + V_{NO})Y_A + (V_{BN} + V_{NO})Y_B + (V_{CN} + V_{NO})Y_C = 0 \quad (4.20)$$

from which, $$V_{ON} = \frac{V_{AN}Y_A + Y_{BN}Y_B + V_{CN}Y_C}{Y_A + Y_B + Y_C}. \quad (4.21)$$

The voltages V_{AN}, V_{BN} and V_{CN} in Eq. 4.21 are known voltages in a given problem and Y_A, Y_B and Y_C are also known as they are reciprocals of Z_A, Z_B and Z_C. Hence displacement neutral voltage may be computed.

The voltage across the impedances may then be easily obtained (e.g. $V_{AO} = V_{AN} + V_{NO}$, etc.). Finally the line currents may be obtained as product of voltage across admittance and the corresponding admittance (e.g. $I_A = V_{AO}Y_A$ etc.).

4.11 The phase voltage and current of a star connected load is 100 V and 10 A. The power factor of the load is 0.8 (lag). Assuming that the system is 3 wire, 3 phase and power is measured by two wattmeters, find the readings of the wattmeters.

Solution

Phase voltage $|V_{Ph}| = 100$ V.
Phase current $|I_{Ph}| = 10$ A.
As the load is star connected so,

line voltage $|V_L| = \sqrt{3}\,|V_{Ph}| = 173.2$ volts and
line current $|I_L| = |I_{Ph}| = 10$ A.
$\cos\theta$ (Power factor) = 0.8 (lag)
Power factor angle $\theta = \cos^{-1}0.8 = 36.87°$ (lag).
Reading of one wattmeter

$$W_1 = |V_L|\,|I_L| \cos(30° + \theta)$$
$$= 173.2 \times 10 \cos(30° + 36.87°) = 680.36 \text{ W}.$$

Reading of the other wattmeter

$$W_2 = |V_L|\,|I_L| \cos(30° - \theta)$$
$$= 173.2 \times 10 \cos(30° - 36.87°) = 1719.56 \text{ W}.$$

4.12 A three-phase 230 V load has a power factor of 0.4. Two wattmeters are connected to measure the power which shows the input to be 10 kW. Find the reading of each wattmeter.

Solution

Line voltage $|V_L| = 230$ V

Power factor angle $\theta = \cos^{-1}0.7 = 45.57°$

Input power = total power = 10 kW = 10,000 W

If W_1 and W_2 be the readings of the wattmeters then

$$W_1 + W_2 = 10{,}000 \quad \text{(i)}$$

Now $\sqrt{3}\,|V_L|\,|I_L| \cos\theta = 10{,}000$, where I_L is the line current

$$\therefore \quad |I_L| = \frac{10{,}000}{\sqrt{3}\times 230\times 0.7} = 35.86 \text{ A.}$$

Also, $W_1 - W_2 = |V_L|\,|I_L| \sin\theta = 230 \times 35.86 \sin 45.57° = 5889.8$ W. (ii)

Equating Eq. (i) and Eq. (ii)

$$W_1 = 7944.9 \text{ W} = 7.94 \text{ kW}$$

and $$W_2 = 2055.1 \text{ W} = 2.06 \text{ kW}.$$

4.13 In a balanced three-phase 200 V circuit, the line current is 115.5 A. When the power is measured by two wattmeter method one of the instruments reads 20 kW and the other zero. What is the power factor of the load?

Solution

Line voltage $|V_L| = 200$ V

Line current $|I_L| = 115.5$ A

1st wattmeter reading $W_1 = 20$ kW = 20,000 W

2nd wattmeter reading $W_2 = 0$

Now, $W_1 + W_2 = \sqrt{3}\,|V_L|\,|I_L| \cos\theta$, where $\cos\theta$ is the power factor

i.e., $$\cos\theta = \frac{W_1 + W_2}{\sqrt{3}V_L I_L} = \frac{20{,}000 + 0}{\sqrt{3}\times 200\times 115.5} = 0.5$$

4.14 Two wattmeters are connected to measure the input to a balanced three-phase circuit. The readings of the instruments are 2500 W and 500 W respectively. Find the power factor of the circuit when (a) both readings are positive and (b) when the later reading is obtained after reversing the current coil of the wattmeter.

Solution

(a) $W_1 = 2500$ W $\quad W_2 = 500$ W

If θ be the power factor angle

$$\tan\theta = \sqrt{3}\frac{W_1 - W_2}{W_1 + W_2} = \sqrt{3}\frac{2500 - 500}{2500 + 500} = 1.155$$

So power factor in first case, $\cos\theta = \cos(\tan^{-1} 1.155) = 0.655$.

(b) $W_1 = 2500$ W and $W_2 = -500$ W

Hence, $$\tan\theta = \sqrt{3}\frac{2500 - (-500)}{2500 + (-500)} = \sqrt{3}\frac{3000}{2000} = 2.598$$

Power factor in 2nd case, $\cos\theta = \cos(\tan^{-1} 2.598) = 0.359$.

4.15 Two wattmeters are connected to measure the input to a 400 V, three-phase delta connected motor whose output is 24.4 kW at a power factor of 0.4 (lag) and 80% efficiency. Find the resistance and reactance of the motor per phase and readings of each of the wattmeters.

Solution

Line voltage $|V_L| = 400$ V

$\therefore$ Phase voltage $|V_{Ph}| = |V_L| = 400$ V.

$$\left.\begin{aligned}\text{Output power} &= 24.4 \text{ kW}\\ \text{Efficiency} &= 80\% = 0.8\end{aligned}\right\} \text{(given)}$$

$$\therefore \quad \text{Input power} = \frac{\text{Output}}{\text{Effeciency}} = \frac{24.4}{0.8} = 30.5 \text{ kW}.$$

Also, power factor ($\cos\theta$) = 0.4 (lag).

If R, X and Z be the resistance, reactance and impedance per phase then we have

$$0.4 = \frac{|R|}{|Z|}$$

However, $\sqrt{3}\,|V_L|\,|I_L|\cos\theta = 30.5$ kW = 30,500 W where $|I_L|$ is the line current.

Hence, $$|I_L| = \frac{30{,}500}{\sqrt{3}\times 400\times 0.4} = 110.06 \text{ A}.$$

Phase current $$|I_{Ph}| = \frac{|I_L|}{\sqrt{3}} = \frac{110.06}{\sqrt{3}} = 63.543 \text{ A}.$$

and $$|Z| = \frac{|V_{Ph}|}{|I_{Ph}|} = \frac{400}{63.543}\ \Omega = 6.29\ \Omega$$

i.e. $$R = 0.4 \times 6.29\ \Omega = 2.52\ \Omega$$

and $$X = \sqrt{Z^2 - R^2} = 5.76\ \Omega.$$

If W_1 and W_2 are the readings of the two wattmeters then

$$W_1 + W_2 = 30{,}500 \qquad \text{(i)}$$

and $$W_1 - W_2 = |V_L|\,|I_L| \sin\theta = 400 \times 110.06 \sin(\cos^{-1} 0.4) = 40{,}348.66. \qquad \text{(ii)}$$

From equations (i) and (ii),

$$W_1 = 35424.33 \text{ W} = 35.42 \text{ kW}$$

and $$W_2 = -4924.33 \text{ W} = -4.924 \text{ kW}.$$

4.16 The input power to a three-phase motor is measured by two wattmeters both of which indicate 100 kW each. Find the power factor of the motor. If the power factor of the motor is changed to 0.75 leading find the readings of the two wattmeters, the input power remaining the same.

Solution

$$W_1 = 100 \text{ kW and } W_2 = 100 \text{ kW (given)}$$

Hence, $$\tan\theta = \sqrt{3}\frac{W_1 - W_2}{W_1 + W_2} = \sqrt{3} \times 0 = 0 \text{ i.e. } \theta = 0^\circ$$

$\therefore$ Power factor $\cos\theta = 1$

In the second case power factor becomes 0.75 i.e. $\cos\theta = 0.75$

Total power $W_1' + W_2' = 2 \times 100 = 200$ kW

Also, $W_1' - W_2' = \dfrac{(W_1' + W_2')\tan\theta}{\sqrt{3}} = \dfrac{200 \times 0.882}{\sqrt{3}}$ kW =101.84 kW

From above we get

$W_1' = 150.91$ kW and $W_2' = 49.09$ kW.

The readings of two wattmeters when the power factor of the motor is 0.75 leading are 150.91 kW and 49.09 kW.

4.17 The input power to a three-phase motor was measured by two wattmeters whose readings were 12 kW and –4 kW and the line voltage was 200 V. Calculate the power factor and the line current.

Solution

$W_1 = 12$ kW $\quad W_2 = -4$ kW

Line voltage $|V_L| = 200$ V

If θ be the power factor angle then

$$\tan\theta = \sqrt{3}\frac{W_1 - W_2}{W_1 + W_2} = \sqrt{3}\frac{12 - (-4)}{12 + (-4)} = \sqrt{3} \times \frac{16}{8} = 3.464.$$

So, power factor = $\cos\theta = \cos(\tan^{-1} 3.464) = 0.277$.

Now, $\sqrt{3}\,|V_L|\,|I_L| \cos\theta = W_1 + W_2 = 12 + (-4) = 8$ kW = 8000 W

where I_L is the line current.

So, $$|I_L| = \frac{8000}{\sqrt{3} \times 200 \times .277} = 83.37 \text{ A.}$$

4.18 Three coils each having resistance of 10 Ω and series reactance of 10 Ω are connected in star across a 400 V, three-phase line. Calculate the line current and readings on the two wattmeters which are connected to measure the total power.

Solution

$R = 10\ \Omega$, $X = 10\ \Omega$, Impedance $|Z| = \sqrt{R^2 + X^2} = 14.14\ \Omega$

Power factor $\cos\theta = \dfrac{|R|}{|Z|} = \dfrac{10}{14.14} = 0.707.$

Line voltage $|V_L| = 400$ V, phase voltage $|V_{Ph}| = \dfrac{|V_2|}{\sqrt{3}} = \dfrac{400}{\sqrt{3}} = 230.94$ V.

Phase current = $\dfrac{|V_{Ph}|}{|Z|} = \dfrac{230.94}{14.14} = 16.33$ A.

Line current $|I_L|$ = phase current = 16.33 A.

If W_1 and W_2 are the readings of the two wattmeters then

$$W_1 + W_2 = \sqrt{3}\,|V_L|\,|I_L| \cos\theta$$

$$= \sqrt{3} \times 400 \times 16.33 \times 0.707 = 7999 \text{ W} \quad 8 \text{ kW}$$

and $$W_1 - W_2 = |V_L||I_L| \sin\theta = 400 \times 16.33 \sin(\cos^{-1} 0.707)$$

$$= 4619.5 \text{ W} = 4.62 \text{ kW}$$

Hence, $W_1 = 6.31$ and $W_2 = 1.69$ kW.

ADDITIONAL EXAMPLES

4.19 A balanced three-phase delta connected load of 100 kW takes a lagging current of 50 A with a line voltage of 11 kV, 50 Hz. Find the circuit constants of the load per phase.

Solution

Total power = 100 kW (= 100,000 W).
Line current $|I_L|$ = 50 A
Line voltge $|V_L|$ = 11 kV (= 11,000 V).

As the system is delta connected,

$$\text{phase current } |I_{Ph}| = \frac{|I_L|}{\sqrt{3}} = \frac{50}{\sqrt{3}} \text{ A},$$

and phase voltage $|V_{Ph}| = (|V_L|) = 11{,}000$ V

$$\text{Impedance per phase } |Z| = \frac{|V_{Ph}|}{|I_{Ph}|} = \frac{11{,}000}{50/\sqrt{3}} = 381\ \Omega.$$

$P = \sqrt{3}\,|V_L|\,|I_L| \cos\theta = 100{,}000$ where ($\cos\theta$ = power factor)

i.e. $$\cos\theta = \frac{10{,}000}{\sqrt{3} \times 11{,}000 \times \frac{50}{\sqrt{3}}} = 0.0182.$$

Also, $|R|/|Z| = \cos\theta$

$\therefore$ $\dfrac{|R|}{|Z|} = 0.0182$, where R is the resistance per phase

So, $R = 6.93\ \Omega$.

If (X) be the reactance per phase then $|X| = \sqrt{Z^2 - R^2} = 380.94\ \Omega$.

As the current is lagging so the reactance is inductive in nature, i.e. inductance, $L = \dfrac{|X|}{\omega}$

$= \dfrac{380.94}{2\pi \times 50} = 1.213$ H.

We have assumed R and L to be series connected in each phase and the circuit constants of the load per phase are 6.93 Ω (resistor) and 1.213 H (inductor).

4.20 Three impedances Z_A, Z_B and Z_C are connected in star and are supplied from a 400 V, 50 Hz, three-phase ac source. Determine the line currents. Assume $Z_A = 5\angle 0°\ \Omega$, $Z_B = 40\angle 30°\ \Omega$ and $Z_C = 20\angle -30°\ \Omega$.

Solution

Referring to Fig. 4.17

$$I_A = \frac{V_{AN}}{Z_A} = \frac{(400/\sqrt{3})\angle 0°}{5\angle 0°} = 46.19\angle 0° \text{ A}$$

$$I_B = \frac{V_{BN}}{Z_B} = \frac{(400/\sqrt{3})\angle -120°}{40\angle 30°} = 5.77\angle -150° \text{ A}$$

$$I_C = \frac{V_{CN}}{Z_C} = \frac{(400/\sqrt{3})\angle -240°}{20\angle -30°}$$

$= 11.55\angle -210°$ A $= 11.55\angle 150°$ A.

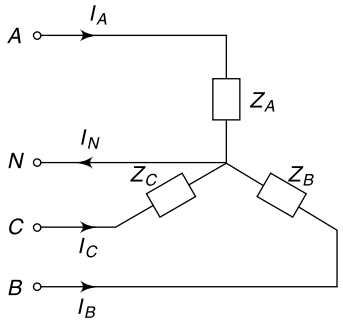


Fig. 4.17 *Circuit of Ex. 4.20*

4.21 A balanced star connected load with impedances of $2\angle -30°\ \Omega$ is supplied from a three-phase, 4-wire system, the voltages to neutral being $V_{AN} = 100\angle -90°$, $V_{BN} = 100\angle 30°$, $V_{CN} = 100\angle 150°$ V. Determine the current in the line conductors and the current in the neutral.

Solution

Referring to Fig. 4.18

$$I_A = \frac{V_{AN}}{Z} = \frac{100\angle -90°}{2\angle -30°} = 50\angle -60° \text{ A}$$

$$I_B = \frac{V_{BN}}{Z} = \frac{100\angle 30°}{2\angle -30°} = 50\angle 60° \text{ A}$$

$$I_C = \frac{V_{CN}}{Z} = \frac{100\angle 150°}{2\angle -30°} = 50\angle 180° \text{ A.}$$

$$I_N = (I_A + I_B + I_C) = 50(\angle -60° + \angle 60° + \angle 180°)$$
$$= 50(0.5 - j0.866 + 0.5 + j0.866 - 1) = 0 \text{ A.}$$

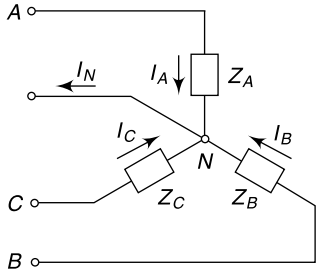


Fig. 4.18 ***Circuit of Ex. 4.21***

4.22 In a three-phase four-wire power distribution system phase B is open while currents through phase R and Y are $100\angle -30°$ and $50\angle 60°$. Find the current through the neutral connection.

Solution

The three-phase four-wire system is a star connected system with a neutral wire.

$$I_R = 100\angle -30° \text{ A}$$
$$I_Y = 50\angle 60° \text{ A.}$$

As B phase is open $I_B = 0$

Neutral current $I_N = (I_R + I_Y + I_B)$

$$= (100\angle -30° + 50\angle 60°)$$
$$= (86.6 - j50 + 25 + j43.3)$$
$$= +111.6 - j6.67 = 111.8\angle -3.42° \text{ A.}$$

4.23 Figure 4.18 shows a three-phase load connected in star. Here $I_A = 20\angle 100°$ A and $I_B = 10\angle -50°$ A. Find the voltage drops across the three impedances of Z_A, Z_B and Z_C where $Z_A = 6\angle 0°$, $Z_B = 6\angle 30°$ and $Z_C = 5\angle 45°$. Assume phasor sum of I_A, I_B and I_C as zero.

Solution

$$I_A = 20\angle 100° \text{ A}$$
$$I_B = 10\angle -50° \text{ A.}$$

$\therefore$ $I_A + I_B + I_C = 0$,

$$I_C = -(I_A + I_B) = -(20\angle 100° + 10\angle -50°$$
$$= -(-3.47 + j19.69 + 6.43 - j4.66)$$
$$= (-2.96 - j12.03) = 12.38\angle 76.18° \text{ A.}$$

Voltage drop across

$$Z_A = I_A Z_A = 20\angle 100° \times 6\angle 0° = 120\angle 100° \text{ V.}$$

Voltage drop across

$$Z_B = I_B Z_B = 10\angle -50° \times 6\angle 30° = 60\angle -20° \text{ V.}$$

Voltage drop across

$$Z_C = I_C Z_C = 12.38\angle 76.18° \times 5\angle 45° = 61.9\angle 121.18°.$$

4.24 The input power to a three-phase motor was measured by the two wattmeter method. The readings were 5.2 kW and 1.7 kW, the latter reading has been obtained after reversal

of current coil connections. The line voltage was 400 V. Calculate (a) the real power (b) the power factor and (c) the line current.

Solution

W_1 = 5.2 kW = 5200 W and W_2 = 1.7 kW = 1700 W.

As the reading of W_2 has been obtained after reversal of current coil so W_2 = –1700 W.

Line voltage (given) $|V_L|$ = 400 V

(a) Total power = $W_1 + W_2$ = (5200 – 1700) W = 3500 W = 3.5 kW.

(b) If θ be the power factor angle then

$$\tan\theta = \sqrt{3}\frac{W_1 - W_2}{W_1 + W_2} = \sqrt{3}\frac{5200 + 1700}{5200 - 1700} = \sqrt{3}\frac{6900}{3500} = 3.414$$

$\therefore$ Power factor

$(\cos\theta) = \cos(\tan^{-1} 3.414) = 0.28.$

(c) Total power = $W_1 + W_2 = \sqrt{3}\,|V_L|\,|I_L|\cos\theta$, where I_L is the line current.

$$\therefore \quad |I_L| = \frac{W_1 + W_2}{\sqrt{3}\,V_L\cos\theta} = \frac{3500}{\sqrt{3}\times 400\times .28} = 18 \text{ A.}$$

4.25 Three impedances each of resistance 10 Ω and series inductive reactance of 5 Ω are connected in (i) star (ii) in delta across a 3 phase 400 V supply. Find the line current in each case and the total power.

Solution

$|R|$ = 10 Ω, $|X|$ = 5 Ω, so impedance $|Z| = \sqrt{R^2 + X^2} = \sqrt{10^2 + 5^2} = 11.18$ Ω.

Line voltage $|V_L|$ = 400 V.

Power factor $\cos\theta = \dfrac{|R|}{|Z|} = \dfrac{10}{11.18} = 0.89.$

(i) In star connection

Phase voltage $|V_{Ph}| = \dfrac{|V_L|}{\sqrt{3}} = \dfrac{400}{\sqrt{3}} = 230.95$ V

and phase current $|I_{Ph}| = \dfrac{|V_{Ph}|}{|Z|} = \dfrac{230.95}{11.18} = 20.66$ A.

$\therefore$ Line current $|I_L|$ = phase current = 20.66 A.

Total power = $\sqrt{3}\,|V_L||I_L|\cos\theta = \sqrt{3}\times 400\times 20.66\times 0.89$

= 12739.16 Ω = 12.74 kW

(ii) In delta connection

Phase voltage $|V_{Ph}| = |V_L|$ = 400 V

So phase current $|I_{Ph}| = \dfrac{|V_{Ph}|}{Z} = \dfrac{400}{11.18} = 35.78$ A and

line current $|I_L| = \sqrt{3}\,|I_{Ph}| = \sqrt{3}\times 35.78 = 61.97$ A

Total power = $\sqrt{3}\,|V_L||I_L|\cos\theta = \sqrt{3}\times 400\times 61.97\times 0.89$

= 38210.206 W = 38.21 kW

It may be noted here that the arm impedances being same, a delta load consumes more real power than the equivalent star load.

4.26 A three-phase balanced voltage of 230 V is applied to a balanced delta connected load consisting of thirty 40 W lamps connected in parallel in each phase. Calculate the phase and line currents, phase voltages, power consumption of all lamps.

Solution

Line voltage $|V_L|$ = Phase voltage $|V_{Ph}|$ = 230 V ($\because$ the load is delta connected)

$\therefore$ $|V_{Ph}| = 230$ V

Power consumption of each lamp = 40 W.

$\therefore$ Total power consumption is $30 \times 40 = 1200$ W

If I_{Ph} be the phase current

$$|V_{Ph}||I_{Ph}| = 1200 \text{ W}$$

Hence $$I_{Ph} = \frac{1200}{230} = 5.2 \text{ A.}$$

Line current = $\sqrt{3}\, I_{Ph} = \sqrt{3} \times 5.2 \text{ A} = 9 \text{ A.}$

Power consumption of all lamps = 3×1200 W = 3600 W = 3.6 kW.

4.27 The load connected to a three-phase supply contains three similar impedances connected in star. The line currents are 50 A and the KVA and kW inputs are 50 and 27 respectively. Find the line and phase voltages, KVAR input and the resistance and reactance of each coil.

Solution

Line current $|I_L| = 50$ A

KVA = 50 and kW = 27

$\therefore$ $$\text{KVAR} = \sqrt{\text{KVA}^2 - \text{KW}^2} = \sqrt{(50)^2 - (27)^2} = 42.$$

As the load is star connected

Phase current $|I_{Ph}| = |I_L| = 50$ A.

If V_L be the line current and $\cos\theta$ be the power factor then

$$\sqrt{3}\,|V_L||I_L| \cos\theta = 27 \times 10^3$$

or $$\cos\theta = \frac{27000}{\sqrt{3} \times V_L I_L}$$

and $$\sqrt{3}\,|V_L||I_L| \sin\theta = 42 \times 10^3$$

or $$\sin\theta = \frac{42000}{\sqrt{3} V_L I_L}$$

$\therefore$ $$\tan\theta = \frac{42}{27} = \frac{X}{R},$$

where X and R are the reactance and resistance of the load.

or $$X = 1.56\, R.$$

Again $$\sqrt{3}\,|V_L||I_L| = 50 \times 10^3$$

or, $$|V_L| = \frac{50 \times 10^3}{\sqrt{3} \times 50} = 577.35 \text{ V}$$

Phase voltage $$|V_{Ph}| = \frac{|V_L|}{\sqrt{3}} = \frac{577.37}{\sqrt{3}} = 333.35 \text{ V}$$

If Z is the impedance per phase then

$$|Z| = \frac{|V_{Ph}|}{|I_{Ph}|} = \frac{333.35}{50} \ \Omega = 6.67\ \Omega$$

or $$R^2 + X^2 = (6.67)^2 = 44.49$$

or $$R^2 + (1.56\, R)^2 = 44.49$$

Hence $$R = 3.6\ \Omega$$

and $$X = 1.56\, R = 1.56 \times 3.6 = 5.61\ \Omega.$$

4.28 Three impedances Z_1, Z_2 and Z_3 are mesh connected to a symmetrical three-phase, 400 V, 50 Hz supply of phase sequence *RYB*. $Z_1 = (10 + j0)\ \Omega$ between *R* and *Y*, $Z_2 = (8 + j6)\ \Omega$ between *Y* and *B* and $Z_3 = (5 - j5)\ \Omega$ between *B* and *R*. Calculate the phase currents and total power consumed. Assume line voltages are balanced and separeted by 120° from each other.

Solution

$$Z_1 = 10 + j0 = 10\angle 0°\ \Omega$$
$$Z_2 = 8 + j6 = 10\angle 36.87°\ \Omega$$
and $$Z_3 = 5 - j5 = 7.07\angle -45°\ \Omega.$$

The corresponding circuit is shown in Fig. 4.19.

Line voltage $|V_L| = 400$ V $(=|V_{ph}|)$.

Phase current through Z_1 is $I_1 = \dfrac{400\angle 0°}{10\angle 0°}$ A

$= 40\angle 0°$ A.

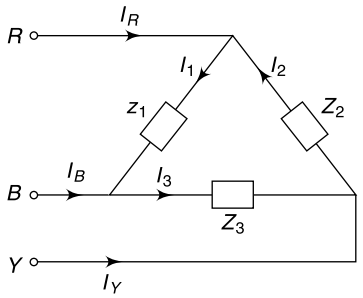


Fig. 4.19 ***Circuit of Ex. 4.28***

Phase current through Z_2 is $I_2 = \dfrac{400\angle -120°}{10\angle 36.87°}$ A $= 40\angle -156.87°$ A.

Phase current through Z_3 is $I_3 = \dfrac{400\angle -240°}{7.07\angle -45°}$ A $= 56.58\angle -195°$ A.

The angles of the currents are w.r.t. the corresponding line voltages.

The total power consumed = $400(40 + 40 \cos 36.87° + 56.58 \cos 45°) = 44.8$ kW.

4.29 A balanced delta connected load of $(4 + j3)\ \Omega$ per phase is connected to a three-phase, 230 V supply. Find the line current, p.f., reactive *VA* and total *VA*.

Solution

Impedance $Z = (4 + j3)\ \Omega = 5\angle 36.87°\ \Omega$.

Line voltage $|V_L|$ (= Phase voltage $|V_{Ph}|$) $= 230\angle 0°$ V.

Hence phase current $|I_{Ph}| = \dfrac{|V_{Ph}|}{|Z|} = \dfrac{230}{5}$ A $= 46$ A.

Line current $|I_L| = \sqrt{3}\,|I_{Ph}| = \sqrt{3} \times 46$ A $= 79.67$ A.

Power factor angle $\theta = 36.87°$ and power factor $\cos\theta = 0.8$.

Hence reactive $VA = \sqrt{3}\,|V_L||I_L| \sin\theta$

$= \sqrt{3} \times 230 \times 79.67 \sin 36.87°$

$= 19042.45$ VAR $= 19.042$ KVAR.

Total $VA = \sqrt{3}\,|V_L||I_L| = 31737.34$ VA $\quad 31.74$ KVA.

4.30 A three-phase 440 V supply feeds a balanced delta connected load. Given: $I_{ab} = 30\angle -30°$ w.r.t. V_{ab}. Find (i) the line current I_a and its phase angle w.r.t. V_{ab}, (ii) total power received by the load and (iii) the resistance per phase. The corresponding figure is given in Fig. 4.20.

Solution

(i) Line current $|I_L| = \sqrt{3} \times 30 = 51.96$ A.

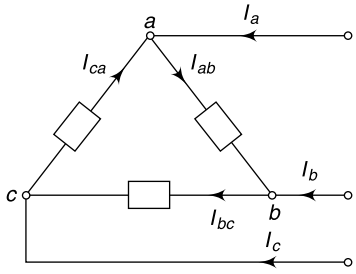


Fig. 4.20 ***Circuit of Ex. 4.30***

Referring to Fig. 4.21(a),
Line current $I_a = I_{ab} - I_{ca}$
$= 51.96\angle -(30° + 30°)$
$= 51.96\angle -60°$
Hence the phase angle of I_a w.r.t. V_{ab} is 60°.

(ii) Total power $= \sqrt{3}\,|V_L||I_L|\cos\theta$
$= \sqrt{3} \times 440 \times 51.96 \cos 30°$
$= 34292.6$ W
$= 34.29$ kW.

(iii) If R is resistance per phase then
$3I_{\text{Ph}}^2 R = 34292.6$
or $R = \dfrac{34292.6}{3 \times (30)^2}\ \Omega = 12.7\ \Omega.$

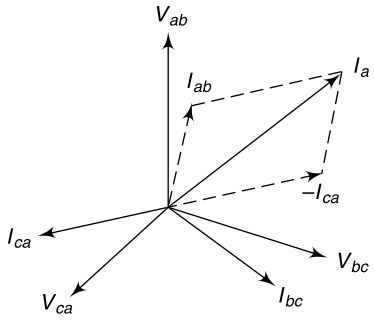


Fig. 4.20(a) ***Phasor diagram for Ex. 4.30***

4.31 A balanced 440 V, three-phase voltage is applied on an unbalanced star connected load. It is given that the supply voltage in phase R is $254\angle -30°$ V and the voltage drop across the load connected in phase R is $200\angle -15°$ V. Calculate the voltage between the star point of the load and the supply neutral. Also find the voltage across the loads in Y and B phases.

Solution

Line voltage of phase R is $V_R = \dfrac{440}{\sqrt{3}} = 254\angle -30°$ V (given)
Voltage drop in phase R is $200\angle -15°$ V.
Let N be the neutral point of the supply and N' be the star point of the load.
Hence $V_{RN} = 254\angle -30°$ volts and $V_{RN'} = 200\angle -15°$ V.
Therefore voltage between star point of load and supply neutral is

$$\begin{aligned} V_{N'N} = V_{RN} - V_{RN'} &= 254\angle -30° - 200\angle -15° \\ &= 220 - j127 - 193.2 + j51.76 \\ &= 26.8 - j75.24 = 79.87\angle -70.39° \text{ V.} \end{aligned}$$

Similarly, for phase Y, voltage across load is given by

$$\begin{aligned} V_{YN'} = V_{YN} - V_{N'N} &= 254\angle -30° - 120° - 79.87\angle -70.39° \\ &= -220 - j127 - 26.8 + j75.24 \\ &= -246.8 - j51.76 = 252.17\angle 168.16° \text{ V.} \end{aligned}$$

Also, voltage across load in phase B is

$$\begin{aligned} V_{BN'} = V_{BN} - V_{N'N} &= 254\angle -30° - 240° - 79.87\angle -70.39° \\ &= 330\angle 94.65° \text{ V.} \end{aligned}$$

4.32 Three impedances $Z_A = 4\angle 30°\ \Omega$, $Z_B = 5\angle -20°\ \Omega$ and $Z_C = 10\angle 0°\ \Omega$ are connected in star and are supplied from 50 V, 50 Hz; three-phase balanced source. Obtain line currents and power drawn by each impedance.

Solution

The line currents are

$$I_A = \frac{50\angle 0°}{\sqrt{3} \times 4\angle 30°} = 7.217\angle -30° \text{ A}$$

$$I_B = \frac{50\angle -120^\circ}{\sqrt{3}\times 5\angle -20^\circ} = 5.772\angle -100^\circ \text{ A}$$

and $$I_C = \frac{50\angle -240^\circ}{\sqrt{3}\times 10\angle 0^\circ} = 2.886\angle 120^\circ \text{ A.}$$

Power drawn by $Z_A = \frac{50}{\sqrt{3}} \times 7.217 \cos 30^\circ = 180.43$ W

Power drawn by $Z_B = \frac{50}{\sqrt{3}} \times 5.772 \cos 20^\circ = 156.57$ W

Power drawn by $Z_C = \frac{50}{\sqrt{3}} \times 2.886 \cos 0^\circ = 83.31$ W.

4.33 A balanced three-phase star connected load of 100 kW takes a leading current of 80 A when connected across a 4 kV, 50 Hz supply. Determine the circuit elements connected in series and power factor of the load.

Solution

Line voltage V_L = 4 kV = 4000 V. Hence phase voltage = $\frac{4000}{\sqrt{3}}$ V .

If I_L be the current (line current and phase current are same in star connected system) we can write,

$\sqrt{3}\, V_L I_L \cos\theta = 100 \times 10^3$, where $\cos\theta$ is the power factor angle of the load.

As $I_L = 80$ A,

Hence $$\cos\theta = \frac{100\times 10^3}{\sqrt{3}\times 4000\times 80} = 0.18 \text{ (as load current is leading)}$$

Now, impedance per phase $(Z_{\text{Ph}}) = \frac{\text{Phase voltage}}{\text{Phase current}} = \frac{4000}{\sqrt{3}\times 80}\ \Omega = 28.86\ \Omega.$

If R and X_C be the resistance and capacitive reactance connected in series,

$$\frac{R}{Z_{\text{Ph}}} = 0.18 \text{ or, } R = 0.18 \times 28.86 = 5.2\ \Omega.$$

$\therefore$ From $\sqrt{R^2 + X_C^2} = 28.86$, we have

$$X_C = \sqrt{(28.86)^2 - (5.2)^2} = 28.39\ \Omega.$$

Hence the resistance is 5.2 Ω and capacitive reactance is 28.39 Ω when the elements are connected in series and the power factor of the load is 0.18 lead.

4.34 A three-phase 440 V, 50 Hz line is connected to the identical capacitors connected in delta. If the line current is 10 A, fine the capacitance of each capacitor.

Solution

$$I_C = (I_{\text{Ph}}) = \frac{|I_L|}{\sqrt{3}} = \frac{10}{\sqrt{3}} = 5.774 \text{ A.}$$

V_C, the voltage across each capacitor is 440 V ($\because$ Δ connection, $|V_{\text{Ph}}| = |V_L| = |V_C|$)

$\therefore$ X_C (capacitive reactance of each capacitor) = $\frac{|V_C|}{|I_{\text{Ph}}|} = \frac{440}{5.774} = 76.20\ \Omega.$

The capacitance of each capacitor is

$$C = \frac{1}{\omega X_C} = \frac{1}{2 \times \pi \times 50 \times 76.20} = 41.79 \ \mu\text{F}.$$

4.35 An industry draws a total of 500 KVA from a balanced 3-phase supply of 3.3 kV ($L - L$) 50 Hz. If the plant power factor is 0.85 lagging, calculate the impedance of the plant (per phase), phase angle between the line to neutral voltage and the line current. Assume Y-connection of the load.

Solution

$$|V_{\text{Ph}}| = \frac{3300}{\sqrt{3}} = 1905.25 \text{ V}.$$

$$I_{\text{Ph}}(= I_L) = \frac{|S|/3}{|V_{\text{Ph}}|} = \frac{500 \times 10^3}{3 \times 1905.25} = 87.48 \text{ A}$$

$$\therefore \quad |Z_{\text{Ph}}| \text{ (impedance/branch)} = \frac{|V_{\text{Ph}}|}{|I_{\text{Ph}}|} = \frac{3300/\sqrt{3}}{87.48} = 21.78 \text{ ohm}.$$

Phase angle between V_{Ph} and the corresponding line current (= 87.48 A) is given by

$$\cos^{-1}(0.85) = 3178°.$$

Thus the line current lags the line voltage by 31.78°.

4.36 A 10 HP 415 V, 3 phase 50 Hz induction motor draws a full load current of 15 A at 0.8 p.f. (lag). Calculate the full load efficiency of the motor.

Solution

Output power being 10 HP, it is equivalent to 7460 W ($\because$ 1 HP = 746 W).

$$\text{Efficiency } \eta = \frac{\text{Output full load power}}{\text{Input power at full load}} \times 100$$

Hence, input power at full load is

$$S = \sqrt{3}\,|V_L||I_L| = \sqrt{3} \times 415 \times 15 = 10782.02 \text{ VA}$$

This is equivalent to input active power of (10782.02 × 0.8) or 8625.61 W (since p.f. is 0.8 and $P = VA$ power × p.f.)

$$\therefore \quad \eta = \frac{7460}{8625.61} \times 100 = 86.49\%.$$

Then we have obtained the efficiency of the motor at full load as 86.49% while full load input power is 8625.61 W and output power is 7460 W.

4.37 The power factor of each phase of a balanced star connected load is 0.6 lagging. If the impedance per phase is 5 Ω and the load is connected across a balanced 200 V 50 Hz source, find the apparent power drawn by the load.

Solution

$$|V_{\text{Ph}}| = \frac{200}{\sqrt{3}} = 115.47 \text{ V}$$

$$|I_{\text{Ph}}| = \frac{|V_{\text{Ph}}|}{|Z_{\text{Ph}}|} = \frac{115.47}{5} = 23.094 \text{ A}.$$

$$\phi = \cos^{-1}(0.6) = 53.13° \text{ (lag)}$$

$$\therefore \quad P = \sqrt{3}\,|V_L||I_L| \cos\phi = \sqrt{3} \times 200 \times 23.094 \times \cos 53.13° = 4800 \text{ W}$$

$[I_L = I_{\text{Ph}}$ and $V_{\text{Ph}} = \sqrt{3}\,V_L$ in Y-connection$]$

$$Q = \sqrt{3}\,|V_L||I_L| \sin\phi$$
$$= \sqrt{3} \times 200 \times 23.094 \times \sin(\cos^{-1} 0.6) = 6399.99 \text{ VAR.}$$
$$\therefore \quad |S| = \sqrt{P^2 + Q^2} = \sqrt{(4800)^2 + (6399.99)^2} = 7999.99 \text{ VA} \; (\; 8 \text{ KVA}).$$

4.38 A 440 V, three-phase, 50 Hz balanced source supplies electrical energy to the following three phase balanced loads:

(i) A 200 HP, three-phase 50 Hz induction motor operating at 94% efficiency and 0.88 p.f. (lag).
(ii) A 50 kW three-phase electric heating element.
(iii) A mixed load of 40 kW (three-phase) operating at 0.7 lagging p.f.

Obtain

(a) the total load in kW supplied by source
(b) the total KVAR supplied by the source
(c) the total apparent power
(d) the line current.

Solution

(a) *Real power*

(i) For motor: $P_M = \dfrac{\text{HP} \times 746}{\text{Efficiency}} = \dfrac{200 \times 746}{0.94} \times 10^{-3} = 158.72$ kW

(ii) For heater: $P_H = 50$ kW.

(iii) For mixed load: $P_X = 40$ kW.

$\therefore$ Total real power supplied = 158.72 + 50 + 40
= 248.72 kW (3-phase).

(b) For motor: $\phi_m = \cos^{-1} 0.88 = 28.36°$

However, $\tan\phi_m = \dfrac{Q_m}{P_m}$ [Q_m = reactive power input to motor, P_m = real power input to motor]

or $Q_M = P_m \tan\phi_m = 158.72 \tan 28.36° = 85.68$ KVAR.

For heating load, $\phi_H = 0$ [as heater is a pure resistive load]

Hence $Q_H = 0$

For mixed load:

$$\phi_X = \cos^{-1}(0.70) = 45.57° \text{ (lag)}$$
$$\therefore \quad Q_X = P_X \tan\phi_X = 40 \tan 45.57° = 40.81 \text{ KVAR.}$$

Thus we find total KVAR supplied

$$(Q) = 85.68 + 0 + 40.81 = 126.49 \text{ KVAR}$$

(c) Total apparent power $|S|$ is given by

$$|S| = \sqrt{P^2 + Q^2} = \sqrt{248.72^2 + 126.49^2} = 279.04 \text{ KVA}$$

and $\phi = \tan^{-1}\dfrac{Q}{P} = \tan^{-1}\dfrac{126.49}{248.72} = 26.96°$ (lag).

(d) $\because \quad |S| = \sqrt{3}\,|V_L||I_L|,$

$$\therefore \quad |I_L| = \frac{|S|}{\sqrt{3}|V_L|} = \frac{279.04 \times 10^3}{\sqrt{3} \times 440} = 366.15 \text{ A.}$$

4.39 Two wattmeters measure the three-phase power of a load and read 80 and 50 kW (for W_1 and W_2 respectively). Find the total complex power and the power factor. Also find the total power and reactive power.

Solution

$$P = W_1 + W_2 = 80 + 50 = 130 \text{ kW}$$

$$\tan \phi = \sqrt{3}\frac{W_2 - W_1}{W_2 + W_1} = \sqrt{3}\frac{50 - 80}{80 + 50} = -0.4$$

$\therefore$ $\phi = -21.78°$ and P.F. ($\cos \phi$) = 0.9286 (lag)

Since real power = (total power) $\times \cos \phi$,

We can write,

Complex power (S) = $\dfrac{P}{\cos \phi} = \dfrac{130}{0.9286}$ 140 KVA.

Reactive power (Q) is obtained as

$$Q = \sqrt{S^2 - P^2} = \sqrt{(140)^2 - (130)^2} \quad 52 \text{ KVAR.}$$

4.40 A three phase induction motor, operating from a 400 V, 50 Hz supply, takes 25 A. The power factor of the motor is poor and found to be 0.5 lagging. If the two wattmeter method is used to measure the three-phase power supplied to the motor, what would each wattmeter read?

Solution

The connection diagram is shown in Fig. 4.21 while the phasor diagram in Fig. 4.22. Here, $\phi = \cos^{-1}(0.5) = 60°$ (lagging)

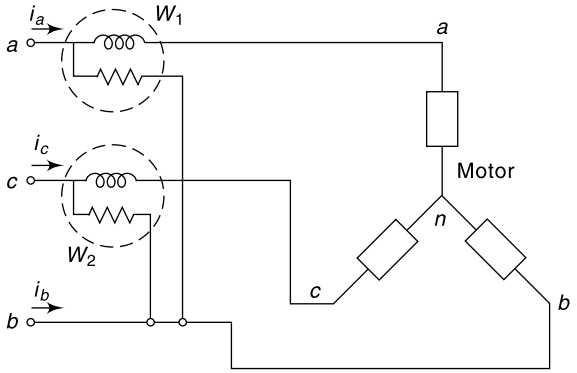


Fig. 4.21 ***Power measurement for the system in Ex. 4.40***

[Voltage across $W_1 = V_{a-c}$ (= $\bar{V}_a - \bar{V}_c$); V_{ac} is lagging I_a by (30° – ϕ). Then the reading of W_1 is $V_{ac}I_a \cos (30° - \phi)$. Similarly, $W_2 = V_L I_L \cos (30° - \phi)$.

$W_1 = V_L I_L \cos (\phi + 30°)$

[Actually $W_1 = V_L I_L \cos (30° - \phi)$

$= V_L I_L \cos (30 - (-\phi))$

$= V_L I_L \cos (30 + \phi)$]

$= 400 \times 25 \times \cos (60° + 30°) = 0.$

$W_2 = V_L I_L \cos (\theta - 30°)$

[$\because$ $W_2 = V_L I_L \cos (30° + \phi)$

$= V_L I_L \cos (30° - \phi)$]

$= 400 \times 25 \times \cos (60° - 30°)$

$= 8.66$ kW.

Thus, W_1 will read zero while W_2 will read 8.66 kW.

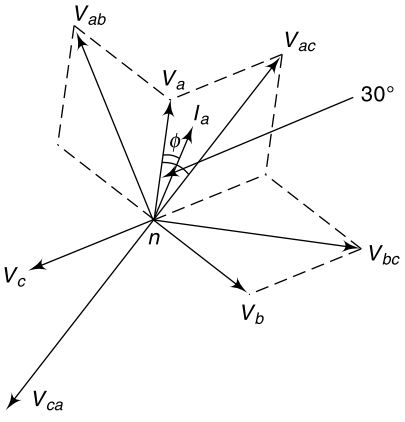


Fig. 4.22 ***Phasor diagram of Ex. 4.40***

4.41 In Fig. 4.23, ammeter A_1 reads 10 A, while A_2 also reads 10 A. Wattmeters W_1 and W_2 read 200 W and 800 W respectively. If $V_1 = V_2 = 400$ V, find the power factor. Also find the KVAR rating of a delta connected capacitor bank to enhance the power factor to 0.85 (lag).

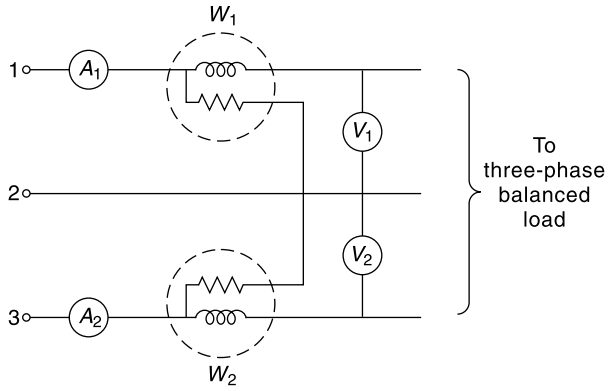


Fig. 4.23 *Circuit of Ex. 4.41*

Solution

$$S = \sqrt{3}\, V_L I_L = \sqrt{3} \times 400 \times 10 = 6928 \text{ VA}$$

$$P = W_1 + W_2 = 200 + 800 = 1000 \text{ W}$$

$$\therefore \quad PF = \frac{P}{S} = \frac{1000}{6928} = 0.144 \text{ (lag)}. \quad [\text{This gives } \phi = \cos^{-1}(0.144) = 81.72°]$$

The reactive load demand is thus

$$Q = P \tan \phi = 1000 \times \tan 81.72° = 6871.54 \text{ VAR}.$$

To improve the p.f. from 0.144 to 0.85 we require that the angle $\phi = 81.72$ becomes $\phi = \cos^{-1}(0.85) = 31.79°$ (lag). Thus the reactive power demand would be P tan 31.79° i.e., 1000 × tan 31.79° = 619.79 KVAR.

This clearly means that the delta connected capacitor bank is to supply (6871.54 – 619.79) KVAR i.e., 6251.77 KVAR.

Thus the rating of the delta connected KVAR bank needs to be 6251.77 KVAR (3 phase).

[We can find rating of the capacitor, per phase.

$$Q/\text{per phase} = \frac{6251.77}{3} = 2083.92 \text{ KVAR}$$

i.e., $V^2 \omega C = 2083.92 \times 10^3$

or, $(400)^2 \times 314 \times C = 2083.92 \times 10^3$

$\therefore$ $C = 0.04$ F per phase].

4.42 A balanced 25 kW load operates at 0.85 p.f. (lag) from a 440 V, 50 Hz, three-phase supply. Calculate the total power, line current and reactive power drawn by the load.

Solution

$$|S_{3\phi}| = \frac{P_{3\phi}}{\cos \phi} = \frac{25 \times 10^3}{0.85} = 29.4 \text{ KVA}$$

$$|I_L| = \frac{|S_{3\phi}|}{\sqrt{3}\,|V_L|} = \frac{29.4 \times 10^3}{\sqrt{3} \times 440} = 38.58 \text{ A}$$

and $$Q_{3\phi} = \sqrt{3}\,|V_L||I_L| \sin \phi$$
$$= \sqrt{3} \times 440 \times 38.58 \times \sin (\cos^{-1} 0.85) = 15.49 \text{ KVAR.}$$

4.43 At what p.f. will one of the wattmeter reading be zero in a three-phase system?

Solution

Let $W_2 = 0$

Then, $$\tan \theta = \sqrt{3}\,\frac{W_1 - 0}{W_1 + 0} = \sqrt{3}$$

$\therefore$ $\theta = \tan^{-1} \sqrt{3} = 60°$.

Also, $\cos 60° = 0.5$

Thus, at 0.5 p.f., one of the two wattmeters would show zero reading.

4.44 The total input power in a three-phase circuit, as measured by two wattmeters, is 60 W. At what p.f. will the wattmeter readings be equal?

Solution

If the wattmeter readings are equal, then each wattmeter would read 30 W. Also, tan θ being zero, $\theta = 0°$.

Hence $\cos \theta = \cos 0° = 1$

Thus, at u.p.f., the readings of the two wattmeters are equal.

4.45 The input three phase power of a balanced impedance load of $(4 + j3)\ \Omega$ per phase is measured by two wattmeter method. Determine the wattmeter reading if the source is a balanced 220 V three phase 50 Hz source and the loads are first connected in star and then in delta.

Solution

For star connection

$$V_{\text{Ph}} = \frac{220}{\sqrt{3}} = 127 \text{ V.}$$

Also, $$I_L\ (= I_{\text{Ph}}) = \frac{V_{\text{Ph}}}{Z_{\text{Ph}}} = \frac{127 \angle 0°}{4 + j3} = 25.4 \angle -36.87° \text{A.}$$

$\cos \phi = \cos (-36.87°) = 0.8$ (lag)

$\therefore$ $$P = \sqrt{3}\,V_L I_L \cos \phi = \sqrt{3} \times 220 \times 25.4 \times 0.8$$
$$= 7742.96\ (= W_1 + W_2) \text{ W.}$$

Also, $$\tan \phi\ (= 0.75) = \sqrt{3}\,\frac{W_1 - W_2}{W_1 + W_2}$$

This gives $W_1 - W_2 = 3352.80$ W

Thus, $W_1 = 5547.88$ W

$W_2 = 2195.08$ W.

For delta connection

$$|I_{\text{Ph}}| = \frac{|V_L|}{|Z_{\text{Ph}}|} = \frac{220}{\sqrt{4^2 + 3^2}} = 44 \text{ A.}$$

$\therefore \quad |I_L| = \sqrt{3}\,|I_{Ph}| = 76.21$ A

and $P = \sqrt{3}\,V_L I_L \cos\phi = \sqrt{3} \times 220 \times 76.21 \times 0.8$

$= 23231.93$ W $(= W_1 + W_2)$

But $\tan\phi = \tan(36.87) = 0.75 = \sqrt{3}\dfrac{W_1 - W_2}{W_1 + W_2}$

or $W_1 - W_2 = 10{,}059.72$ W.

Hence, $W_1 + W_2 = 23231.93$ W

$W_1 - W_2 = 10059.72$ W.

This gives $W_1 = 16645.83$ W

$W_2 = 6586.11$ W.

4.46 Three impedances, Z_{ab}, Z_{bc} and Z_{ca}, are connected across a balanced 400 V, 50 Hz, 3-phase supply. Find I_a (Fig. 4.24).

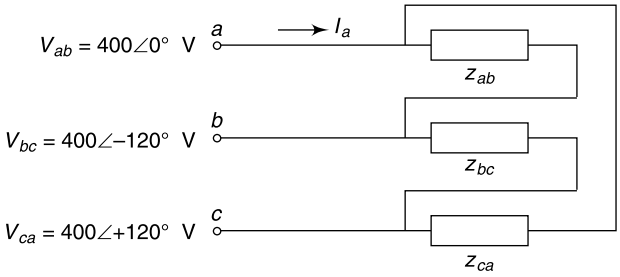


Fig. 4.24 *Circuit of Ex. 4.46*

Assume $Z_{ab} = 5\angle 30°\ \Omega$; $Z_{bc} = 10\angle 20°\ \Omega$; $Z_{ca} = 10\angle 0°\ \Omega$

Solution

It is evident from the figure that I_a is the phasor sum of currents passing through Z_{ab} and Z_{ca}. Hence we can write

$$I_a = \frac{V_{ab}}{Z_{ab}} + \frac{V_{ac}}{Z_{ca}}$$

$$= \frac{V_{ab}}{Z_{ab}} + \frac{-V_{ac}}{Z_{ca}}$$

$$= \frac{400\angle 0°}{5\angle 30°} + \frac{-400\angle +120°}{10\angle 0°}$$

$$= 80\angle -30° - 40\angle 120°$$

$$= 80(\cos 30° - j \sin 30°) - 40(\cos 120° + j \sin 120°)$$

$$= 69.28 - j40 + 20 - j34.64$$

$$= (89.28 - j74.64)\text{ A} = 116.37\angle -39.896°\text{ A}.$$

4.47 A balanced delta connected three-phase load of 30 kW is fed from a 400 V 50 Hz three-phase source. The load power factor is 0.7 (lag). It is desired to improve the power factor to 0.85 (lag) by using three delta connected capacitors. Obtain the value of the resultant current drawn from the supply and the capacitance of each capacitor.

Solution

$\because \quad P = \sqrt{3}\,|V_L|\,|I_L| \cos\theta,$

In this case $|I_L| = \dfrac{30 \times 10^3}{\sqrt{3} \times 400 \times 0.7} = 61.86$ A.

Since the load is Δ connected,

$\therefore \quad |I_L| = \sqrt{3}\,|I_{Ph}|$

In this problem, $|I_{Ph}| = (61.86)/\sqrt{3} = 35.72$ A.

Figure 4.25(a) represents the schematic diagram of the system after the capacitors are connected in Δ across the load in order to improve the p.f. from 0.7 to 0.85 (lag). Figure 4.25(b) rerpresents the circuit diagram per phase basis while Fig. 4.25(c) represents the phasor diagram on per phase basis.

It is evident that with connection of capacitors the power factor is improved from 0.7 (lag) to 0.85 (lag).

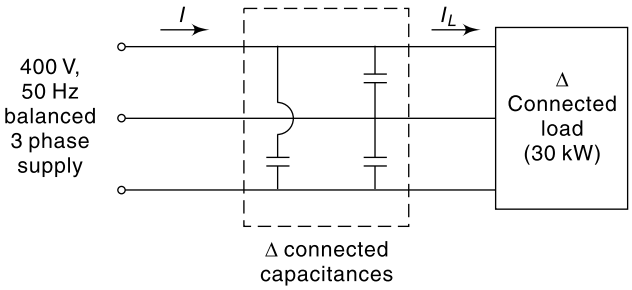


Fig. 4.25(a) ***System of Ex. 4.47***

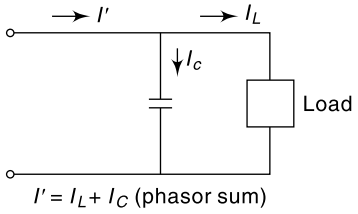


Fig. 4.25(b) ***Circuit diagram (per phase) for Fig. 4.25(a)***

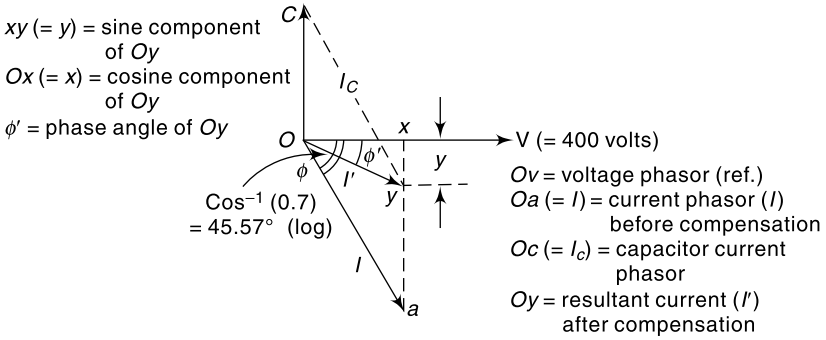


Fig. 4.25(c) ***Phasor diagram for Ex. 4.47***

From 4.31(c), we can write

$$I' \ (= Oy) = \frac{Ox}{\cos\phi'} = \frac{Oa\cos\phi}{\cos\phi'} = \frac{35.72 \times 0.7}{0.85}$$

$= 29.42$ A [$\because$ p.f. before adding capacitor is 0.7 and after adding capacitor is 0.85]

$\therefore$ The current drawn from the supply is 29.42 A after installation of capacitors at load terminals.

Again, $xy = I' \sin\phi' = 29.42 \times \sin(\cos^{-1} 0.85) = 15.5$ A

$\therefore$ $I_C = ay = xa - xy = I \sin\phi - xy = 35.72 \times \sin(\cos^{-1} 0.7) - 15.5 = 10$ A.

But $|I_C| = \dfrac{|V|}{|X_C|}$

$\therefore$ $X_C = \dfrac{|V|}{|I_C|} = \dfrac{400}{10} = 40\ \Omega$ [$\because$ capacitors are connected in Δ fachion, hence $|V_L| = |V_{ph}| = 400$ V]

or $\dfrac{1}{\omega C} = 40$

$\therefore$ $C = \dfrac{1}{2 \times \pi \times 50 \times 40} = 79.61\ \mu$F (for each capacitor.)

4.48 A balanced three-phase load consists of impedances $(4 + j3)\ \Omega$ per phase and is connected to a 400 V source. Assuming V_{1-n} to be the reference phasor calculate the current per phase, power per phase and the total three phase power for a Y-connected load. Repeat the calculation for a Δ-connected load.

Solution

For star (Y) load:

Phase voltages are as follows

$$V_{1-n}\angle 0°,\ V_{2-n}\angle -120°,\ V_{3-n}\angle 120°$$

while line voltages would be

$$V_{1-2}\angle 30°,\ V_{2-3}\angle -90°,\ V_{3-1}\angle 150°.$$

$\therefore$ $I_{\text{Ph}_1} = \dfrac{V_{\text{Ph}_1}}{Z_{\text{Ph}_1}} = \dfrac{\frac{400}{\sqrt{3}}\angle 0°}{(4 + j3)} = 46.2\angle -37°$ A

Similarly, for phases 2 and 3, the phase currents would be

$$I_{\text{Ph}_2} = 46.2\angle -37° - 120° = 46.2\angle -157°\ \text{A}$$

$$I_{\text{Ph}_3} = 46.2\angle -37° + 120° = 46.2\angle 83°\ \text{A}.$$

The phasor diagram is shown is shown in Fig. 4.26. Since the voltages are balanced, the load and the phase currents are balanced. The line currents for the star connected load will be same to those of phase currents.

The power per phase is obtained as

$$P_{\text{Ph}} = |V_{\text{Ph}}||I_{\text{Ph}}| \cos\phi = 231 \times 46.2 \times \cos(-37°) = 8.523\ \text{kW}.$$

The three-phase power would be

$$P_{3\phi} = 3 \times P_{\text{Ph}} = 3 \times 8.523 = 25.569\ \text{kW}$$

[Check: $P_{3\phi} = \sqrt{3}\,|V_L||I_L| \cos\phi = \sqrt{3} \times 400 \times 46.2 \times \cos(-37°) = 25.563$ kW.]

For Delta (Δ) load

Here the line voltage is equal to the phase voltges. The voltages are as follows:

$$V_{1-2}\angle 30°,\ V_{2-3}\angle -90°,\ V_{3-1}\angle 150°.$$

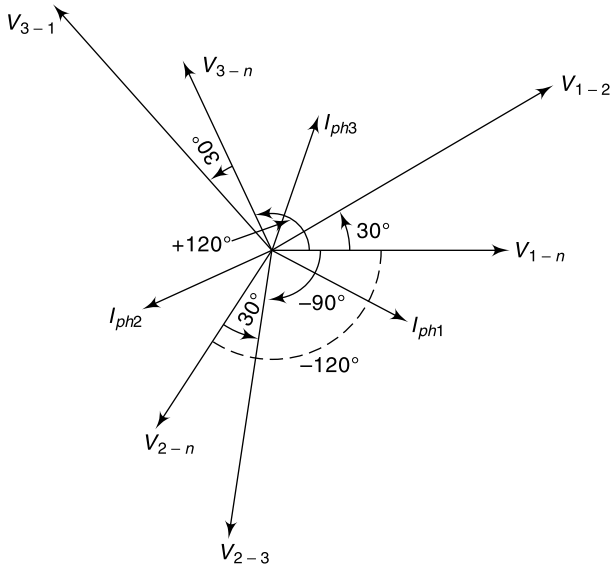


Fig. 4.26 ***Phasor diagram for the star connected system of Ex. 4.48***

Phase currents are obtained as

$$I_{\text{Ph}_1} = \frac{V_{1-2}\angle 30^\circ}{(4 + j3)} = \frac{400\angle 30^\circ}{5\angle 37^\circ} = 80\angle -7^\circ \text{ A}$$

Similarly, $I_{\text{Ph}_2} = 80\angle -127^\circ$ A

$I_{\text{Ph}_3} = 80\angle +113^\circ$ A.

The phasor diagram is shown in Fig. 4.27.

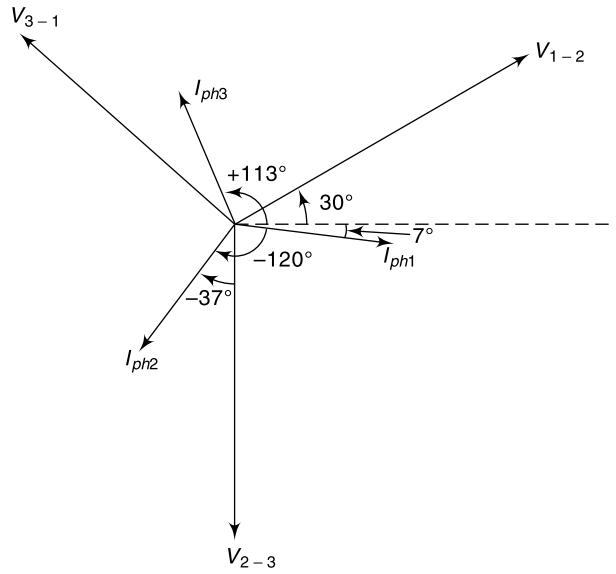


Fig. 4.27 ***Phasor diagram of the delta connected system of Ex. 4.48***

ϕ, the angle between the voltage and current is found to be [–30° – (7°)] i.e., (–37°).

$\therefore$ $P_{ph} = |V_{Ph}||I_{Ph}| \cos \phi = 400 \times 80 \times \cos(-37°) = 25.556$ kW.

and three-phase power is

$P_{3\phi} = 3 \times 25.556 = 76.668$ kW.

[Check: $P_{3\phi} = \sqrt{3}\ |V_L||I_L| \cos \phi$

$= \sqrt{3} \times 400 \times (80 \times \sqrt{3}) \times \cos(-37°) = 76.668$ kW.]

It may be noted here that we can calculate the reactive powers also drawn by the load for both star and delta connection using the formulae

$Q_{3\phi} = \sqrt{3}\ |V_L||I_L| \sin \phi$

In star connection $V_L = 400$ V, $I_L = 46.2$ A, $\phi = -37°$.

In delta connection $V_L = 400$ V, $I_L = (\sqrt{3} \times 80)$ A, $\phi = -37°$.

The total power in each case is given by $|S| = \sqrt{3}\ |V_L||I_L|$.]

EXERCISES

Short- and Long-Answer-Type Questions

1. A three-phase four wire 208 V, system supplies a star connected load in which $Z_A = 10\angle 0°\ \Omega$, $Z_B = 15\angle 30°\ \Omega$ and $Z_C = 10\angle -30°\ \Omega$. Find the line currents, the neutral current and the load power. Assume V_{AN} to be the reference phasor folled by V_{BN} and V_{CN}.
   [*Ans:* $12\angle 0°$, $8\angle -150°$, $12\angle -210°$ A; $5.69\angle 159.4°$ A, 3519 W]
2. Calculate the active and reactive components for the current in each phase of a star connected 5000 V, three-phase alternator supplying 3000 kW at power factor 0.8. [*Ans:* 346.2 A, 260 A]
3. Three similar coils of resistance 9 Ω and reactance 12 Ω are connected in delta to a three-phase, 440 V, 50 Hz supply. Find the line current, power factor, total KVA and total kW. [*Ans:* 50.8 A, 0.6, 38.7 KVA, 23.23 kW]
4. For the unbalanced delta connected load shown in Fig. 4.28 find the phase currents, line currents and the total power consumed by the load.
   [*Ans:* $10\angle -53.13°$, $10\angle 156.86°$, $20\angle 156.86°$, $15.73\angle 165.3°$, $29.1\angle -33.2°$, $4.94\angle 128°$ 3000 W]

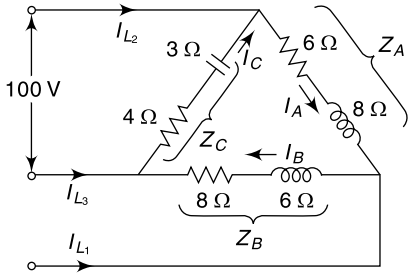


Fig. 4.28

5. A balanced three-phase load consists of three coils each of resistance 4 Ω and inductance 0.02 H. Determine the total power when the coils are
   (i) star connected and
   (ii) delta connected to a 440 V, 3 phase, 50 Hz supply

   [*Ans:* 13.99 kW; 41.97 kW]

   [*Hint:* $Z = 4 + j(2\pi \times 50 \times 0.02) = (4 + j6.28) = 7.44\angle 57.5°\ \Omega$

   $\cos \theta = \dfrac{R}{Z} = \dfrac{4}{7.44} = 0.5376.$

   (i) Star connection

   $$V_L = 440 \text{ V } \therefore\ V_{Ph} = \frac{440}{\sqrt{3}} \text{ V}$$

$$|I_{Ph}| = \frac{440\sqrt{3}}{7.44} = 34.14 \text{ A} = |I_L|$$

$$P = \sqrt{3}\,|V_L|I_L \cos\theta = \sqrt{3} \times 440 \times 34.14 \times 0.5376$$
$$= 13987.855 \text{ W} = 13.988 \text{ kW}.$$

(ii) Delta connection

$$|V_L| = |V_{Ph}| = 440 \text{ V}$$

$$|I_{Ph}| = \frac{440}{7.44} = 59.14 \text{ A}$$

$$\therefore \quad P = 3\,V_{Ph}\,I_{Ph} \cos\theta = 3 \times 440 \times 59.14 \times 0.5376$$
$$= 41967.48 \text{ W} = 41.97 \text{ kW}.$$

6. Three equal impedances of $(8 + j12)\ \Omega$ are connected in star across 415 V, 3 phase, 50 Hz supply. Calculate (i) line current (ii) Power factor) (iii) Active and reactive power drawn by the load.

[*Ans:* 16.616 A, 0.5556629 W; 9935.28 VAR]

[Hint: $Z = (8 + j12) = 14.42\underline{|56.32^\circ}\ \Omega$

$$|V_L| = 415 \text{ V}; |V_{Ph}| = \frac{415}{\sqrt{3}} \text{ V}$$

(i) Line current = phase current = $\dfrac{V_{Ph}}{Z} = \dfrac{\frac{415}{\sqrt{3}}}{14.42}$ A = 16.616 A.

(ii) Power factor $\cos\theta = \dfrac{R}{Z} = \dfrac{8}{14.42} = 0.555$.

(iii) Active power $\sqrt{3} \times 415 \times 16.616 \times 0.555 = 6628.7$ W.

Reative power = $\sqrt{3} \times 415 \times 16.616 \sin(\cos^{-1}0.555)$.

= 9935.28 VAR

7. In a balanced three-phase system load 1 draws 60 kW and 80 KVA leading while load 2 draws 160 kW and 120 KVAR lagging. If line voltage of the supply is 1000 V find the line current drawn by each load.

[*Ans:* 57.8 A, 115.5 A]

8. In the network shown in Fig. 4.29 three resistors are connected in star to a three-phase supply of 400 V. The wattmeter *W* is connected as shown. Calculate the currents in the three lines and the readings of the wattmeter.

[*Ans:* 230.094 A, 7.698 A, 11.547 A, 8 kW]

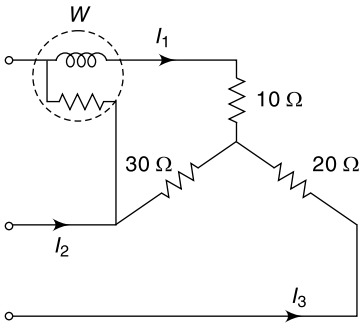


Fig. 4.29

9. A balanced three-phase star connected load draws 10 kW from a three-phase balanced systems of 400 V, 50 Hz while the line current is 75 A (leading). Find the circuit elements of the load.

[*Ans:* 0.6 Ω, 1054 μF]

10. An induction motor draws a three phase power. Two wattmeter method is applied to find the total power. If W_1 = 10 kW, W_2 = 5 kW, find the total three phase active power, reactive power and power factor.
[*Ans:* 15 kW, 8.66 KVAR, 0.866]
11. A delta connected load has following impedances: $Z_{RY} = j10\ \Omega$, $Z_{YB} = 10\angle 0°\ \Omega$, $Z_{BR} = -j10\ \Omega$. If the load is connected across a three phase 100 V supply find the line currents.
[*Ans:* $(-5 + j1.34)$ A, $(8.66 - j5)$ A, $(-3.66 + j3.66)$ A]
12. The power in a three-phase circuit is measured by two wattmeters. If the total power is 50 kW, power factor being 0.8 leading, what will be the reading of each wattmeter? For what p.f. will one of the wattmeter reading will be zero? [*Ans:* 35.825 W, –14.175 W, 0.5]
13. Derive the relation between phase and line voltages and currents for (i) star connected load (ii) delta connected load across a three-phase balanced system.
14. Show that sum of three emf's is zero in a three-phase balanced ac circuit.
15. Show that the power in a three-phase circuit can be measured using 2 wattmeters. Draw the circuit diagram and vector diagram.
16. What are the advantages of a polyphase system over the single-phase system?

MULTIPLE CHOICE QUESTIONS

1. In a balanced three-phase delta connected system the relation between the rms value of line and phase currents is given by

(a) $I_L = I_{hp}$ (b) $I_{ph} = \sqrt{3}\ I_{ph}$

(c) $I_L = \sqrt{2}\ I_{ph}$ (d) $I_L = \sqrt{3}\ I_{ph}$

Answer: (d) $I_L = \sqrt{3}\ I_{ph}$

2. In a balanced three-phase circuit, if the power is measured by two wattmeter method, one of the wattmeter readings is zero when the load power factor is

(a) 0.2 lag (b) 0.5 lag

(c) unity (d) zero

Answer: (b) 0.5 lag

3. A three-phase, 4 wire system suplies a balanced star load . The current in each phase is 5 A. The current in the nentral wire will be

(a) $5\sqrt{3}$ A (b) 0 A

(c) 15 A (d) 5 A

Answer: (b) 0 A

4. In a three-phase star connected system, the realation between the phase and the line voltage is

(a) $V_{ph} = V_L$ (b) $V_{ph} = \sqrt{3}\ V_L$

(c) $V_{ph} = \frac{1}{\sqrt{3}} \cdot V_L$ (d) $V_{ph} = \frac{1}{3} \cdot V_L$

Answer: (c) $V_{ph} = \frac{1}{\sqrt{3}} \cdot V_L$

5. In a three-phase system line voltage are
   (a) 30° apart (b) 60° apart
   (c) 90° apart (d) 120° apart
   Answer: (d) 120° apart
6. In a star connected three-phase supply, the phase currents and line currents are related as
   (a) $I_{ph} = I_L$ (b) $I_{ph} = \sqrt{3}\ I_L$
   (c) $I_{ph} = \frac{1}{\sqrt{3}}\ I_L$ (d) $I_{ph} = \frac{1}{\sqrt{2}}\ I_L$
   Answer: (a) $I_{ph} = I_L$
7. The expression of real power in a three-phase circuit is given by
   (a) $P = \sqrt{3}\ I_{ph} \cos \phi$ (b) $P = 3V_L I_L \cos \phi$
   (c) $P = \sqrt{3}\ V_{ph} I_{ph} \cos \phi$ (d) $P = \sqrt{3}\ V_L I_L \cos \phi$
   Answer: (d) $P = \sqrt{3}\ V_L I_L \cos \phi$
8. A three-phase system supplies a three-phase resistive load. The power is measured by two wattmeter method. During steady state condition for two wattmeter method,
   (a) $W_1 = W_2$ (b) $W_1 = 2W_2$
   (3) $W_1 = \frac{W_2}{2}$ (d) $W_2 = 0$
   Answer: (a) $W_1 = W_2$
9. A $100\angle 0°$ volt (line to line) ac supply opreting with 50 Hz supply frequency is supplyings a resistive load of 10 kW. What is the value of current in each phase if the load is delta connected.
   (a) 25 A (b) 30 A
   (c) 33.33 A (d) 100 A
   Answer: (c) 33.33 A
10. The phasor sum of all the voltages in a three-phase balanced system is
    (a) 0.5 (b) 0
    (c) $\sqrt{3}$ (d) negative
    Answer: (b) 0
11. The total input power in a three-phase circuit, as measured by two wattmeter, is 80 W. At what p.f. will the wattmeter readings be equal?
    (a) 0.5 lag (b) 0.2 lag
    (c) 0 (d) Unity power factor
    Answer: (d) Unity power factor

12. The phase curretns of both the delta and star loads being equal which of these two loads will dissipate more real power?
    (a) both will dissipate same power
    (b) star load will dissipate more power
    (c) delta load will dissipate more power
    Answer: (a) both will dissipate same power

UNIVERSITY QUESTIONS WITH ANSWERS

Long-Answer Type Questions

1. (a) Explain how the power factor of a balanced three phase load can be determined with the help of two wattmeters. (WBUT 2014)
    Answer: Article 4.7.

    (b) Three equal impedances of $(8 + j12)\ \Omega$ are connected in star across 415 V, 3 phase, 50 Hz. supply. Calculate (i) Line current (ii) Power factor (iii) Active and reactive power drawn by the total load. (WBUT 2005)

    Answer: Line voltage $(V_L) = 415$ V

    As the impedances are star connected phase voltage

$$(V_{ph}) = \frac{V_L}{\sqrt{3}} = \frac{415}{\sqrt{3}} \text{ V}$$

    Phase impedance (Z) $= 8 + j12 = 14.42 \angle 56.31° \ \Omega$

    (i) Phase current $(I_{ph}) = \dfrac{V_{ph}}{Z} = \dfrac{415}{\sqrt{3} \times 14.42} = 16.616$ A

    $\therefore$ Line current $(I_L) = I_{ph} = 16.616$ A

    (ii) Power factor $(\cos \theta) = \cos 56.31° = 0.554$ lag

    (iii) Active power drawn by total load $(P) = \sqrt{3} V_L I_L \cos \theta$

$$= \sqrt{3} \times 415 \times 16.616 \times 0.554$$
$$= 6616.75 \text{ W}$$

    Reactive power drawn by total load (Q) $= \sqrt{3} V_L I_L \sin \theta$

$$= \sqrt{3} \times 415 \times 16.616 \sin 56.31°$$
$$= 9937.39 \text{ VAR.}$$

2. (a) Explain the method of measurement of balanced three phase power by two wattmeter method. Draw the neat circuit diagram. (WBUT 2012, 2014)
    Answer: Article 4.6 and Fig. 4.13.

    (b) Three equal impedances $(6 + j8)\ \Omega$ are connected in *Y* across a 400 V, 3 phase, 50 Hz supply. Calculate (i) the line current and the phase current (ii) the power factor (iii) active and reactive powers drawn by the load per phase. (WBUT 2012)
    Answer: Impedance per phase $(Z) = 6 + j8 = 10 \angle 53.13°$
    Line voltage $(V_L) = 400$ V

As the load is connected in star the phase voltage $V_{ph} = \frac{V_L}{\sqrt{3}} = \frac{400}{\sqrt{3}}$ V

and line current (I_L) = phase current (I_{ph})

(i) Phase current (I_{ph}) = $\frac{V_{ph}}{Z} = \frac{400}{\sqrt{3} \times 10}$ = 23.1 A

$\therefore$ Line current (I_L) = 23.1 A

(ii) Power factor ($\cos \theta$) = $\frac{R}{Z} = \frac{6}{10}$ = 0.6

(iii) Active power drawn by the load per phase

$$(P) = V_{ph} I_{ph} \cos \theta = \frac{400}{\sqrt{3}} \times 23.1 \times 0.6 = 3200 \text{ W}$$

Reactive power drawn by the load per phase

$$(Q) = V_{ph} I_{ph} \sin \theta = \frac{400}{\sqrt{3}} \times 23.1 \times 0.8 = 4267.8 \text{ } VAR$$

3. For the balance three phase circuit shown below (Fig. 11), find
   (a) phase voltage
   (b) line current
   (c) power factor
   (d) total power consumed if the line voltage is 440 V.

   Draw the voltage and current phasor diagram. (WBUT 2007)

   Answer: The three phase given circuit is star connected.

   Line voltage (V_L) = 440 V

   (a) Phase voltage (V_{ph}) = $\frac{V_L}{\sqrt{3}} = \frac{440}{\sqrt{3}}$ = 254 V

   (b) Phase current = line current (I_L) = $\frac{V_{ph}}{R} = \frac{254}{20}$ = 12.7 A

   (c) Power factor ($\cos \theta$) = $\cos \theta^\circ$ = 1 ($\because$ circuit is purely resistive)

   (d) Total power consumed (P) = $\sqrt{3} V_L I_L \cos \theta$

   $= \sqrt{3} \times 440 \times 12.7 \times 1$

   = 9678.7 W = 9.678 kW

   Phasor diagram: Article 4.4.1 and Fig. 4.7.

4. (a) How will you measure the power consumed by a balanced star connected three phase circuit with two wattmeters? Draw the circuit and derive necessary relation.

   Answer: Refer Article 7.6 and Article 7.7.

   (b) A three-phase 230 V load has a power factor of 0.7. Two wattmeters are used to measure power which shows the input to be 10 kW. Find the reading of each wattmeter. (WBUT 2009)

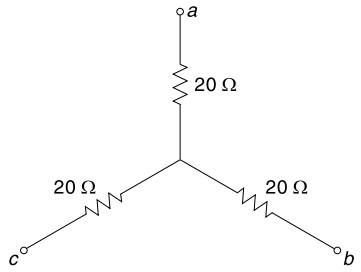


Fig. 4.30

Solution

$$V = 230 \text{ V}$$
$$\cos \phi = 0.7$$
$$W_1 + W_2 = 10{,}000 \text{ watts}$$
$$\therefore \quad \tan \theta = \tan (\cos^{-1} 0.7) = 1$$

$$\text{or,} \quad 1 = \sqrt{3}\, \frac{W_1 \sim W_2}{10{,}000}$$

$$\therefore \quad W_1 \sim W_2 = 5773.5$$
$$\therefore \quad W_1 = 7886.75 \text{ watt}$$
$$\text{and} \quad W_2 = 2113.25 \text{ watt}$$

5. What is a three phase balanced ac system? Show that in a three phase balanced ac circuit, the sum of current in the neutral is zero. (WBUT 2012, 2014)

   Answer: When three identical coils are placed with their axes 120° displaced from each other and rotated in a uniform magnetic field with same angular velocity, a sinusoidal voltage is generated across each coil. The emfs developed in the three coils are identical in all respects except that they are displaced from each other by 120°. When identical loads are connected in the three phases then the currents flowing in the three phases will have equal magnitude but they will be displaced from each other by 120°. This system is called the three phase balanced ac system.
   Refer to Section 4.4.1

Multiple Choice Questions

1. In a three phase balanced system, line voltage makes an angle with phase voltages (WBUT 2012)
   (a) 30° (b) 60°
   (c) 90° (d) 120°
   Answer: (a) 30°
2. Which of the following in a four-wire system? (WBUT 2012)
   (a) Delta with neutral
   (b) Star with neutral
   (c) Both delta and star
   (d) Any combination of four wires
   Answer: (b) star with neutral

3. In three-phase, 4-wire balanced system, the current in each phase is 10 A. The current through the neutral wire will be (WBUT 2013)
   (a) 30 A (b) 10 A
   (c) 0 (d) 15 A
   Answer: (c) 0
4. Three 50 Ω resistances are connected in star across a 400 V, 3-phase supply. If one of the resistances is disconnected, the line current will be (WBUT 2014)
   (a) 8 A (b) 4 A
   (c) $8\sqrt{3}$ A (d) $8/\sqrt{3}$ A
   Answer: (b) 4 A

5 THREE-PHASE INDUCTION MOTORS

5.1 INTRODUCTION

The whole concept of a polyphase ac, including the *induction motor*, was the idea of the great Yugoslavian engineer, Nikola Tesla.

The induction motor is, by a very considerable margin, the most widely used ac motor in industry. Induction motors normally require no electrical connection to the rotor windings. Instead, the rotor windings are short-circuited. Magnetic flux flowing across the air-gap links these closed rotor circuits. As the rotor moves relative to the air-gap flux, voltages are induced in the short-circuited rotor windings according to Faradays' law of electromegnetic induction causing currents to flow in them. The fact that the rotor current arises from induction, rather than conduction, is the basis for the name of this class of machines. They are also called "asynchronous" (i.e. not synchronous) machines because their operating speed is slightly less than synchronous speed in the motor mode and slightly greater than synchronous speed in the generator mode. Induction machines are usually operated in the motor mode, so they are usually called "induction motors."

Because of its simplicity and ruggedness, relatively less expensive and little maintenance, this motor is often the natural choice, as a drive in industry. The squirrel cage motor is often preferred over when a substantially constant speed of operation is desired, the wound rotor motor is a competitor of the dc motor when adjustable speed is required.

The chief disadvantages of induction motors are:

(a) The starting current may be five to eight times full-load current if direct on line start is allowed.
(b) The speed is not easily controlled.
(c) The power factor is low and also lagging when the machine is lightly loaded.

For most applications, their advantages far outweigh their disadvantages.

5.2 CONSTRUCTION OF INDUCTION MACHINES

Similar to other rotating electrical machines, a three-phase induction motor also consists of two main parts: the *stator* and the *rotor* (the stator is the stationary part and the rotor is the rotating part). Apart from these two main parts, a three-phase induction motor also requires bearings, bearing covers, end plates, etc. for its assembly.

The stator of a three-phase induction motor has three main parts namely, stator frame, stator core and stator windings. The stator frame can either be casted or can be fabricated from rolled steel plates. The stator core is built up of high silicon sheet steel laminations of thickness 0.4 to 0.5 mm. Each lamination is separated from the other by means of either varnish, paper or oxide coating. Each lamination is slotted on the inner periphery so as to house the winding. The laminations for small machines are in the form of complete rings, but for large machines these may be made in sections. The insulated stator conductors are connected to form a three-phase winding, the stator phase windings may be either *star* or *delta-connected*.

The rotor is also built up of their laminations of the same material as the stator. The laminated cylindrical core is mounted directly on the shaft or a spider carried by the shaft. These laminations are slotted on their outer periphery to house the rotor conductors. There are two types of induction motor rotors:

(a) Squirrel cage or simply cage rotor
(b) Phase wound or wound rotor or slip ring rotors.

In either case, the rotor windings are contained in slots in a laminated iron core which is mounted on the shaft. In small machines, the lamination stack is pressed directly on the shaft. In larger machines, the core is mechanically connected to the shaft through a set of *spokes* called a "spider".

The motor having the first type of rotor is known as a squirrel cage induction motor. This type of rotor is cheap and has a simple and rugged construction. It is cylindrical in shape and is made of sheet steel laminations. Here the slots provided to accommodate the rotor conductors, are not made parallel to the shaft but they are *skewed*. The purpose of skewing is (a) to reduce the magnetic hum and (b) to reduce the magnetic locking. The rotor conductors are short-circuited at the ends by brazing the copper rings, resembling the cage of a squirrel and hence the name squirrel cage rotor.

In present days, 'die-cast rotors' have become very popular. The assembled rotor laminations are placed in a mould. The molten aluminium is forced under pressure to form the bars. Figure 5.1 (a-c) shows a typical stator and rotor (both squirrel cage type and slip ring type) assembly. Figure 5.1(d) shows the schematic of a cage rotor separately.

The motor having the second type rotor, i.e. wound type rotor, is named as a slip-ring induction motor. In this motor, the rotor is wound for three-phase, similar to stator winding using open type slots in the rotor lamination. Rotor winding is always star connected and thus only three remaining ends of the windings are brought out and connected to the slip rings as shown in Fig. 5.2. With the help of these slip rings and brushes, additional resistances can also be connected in series

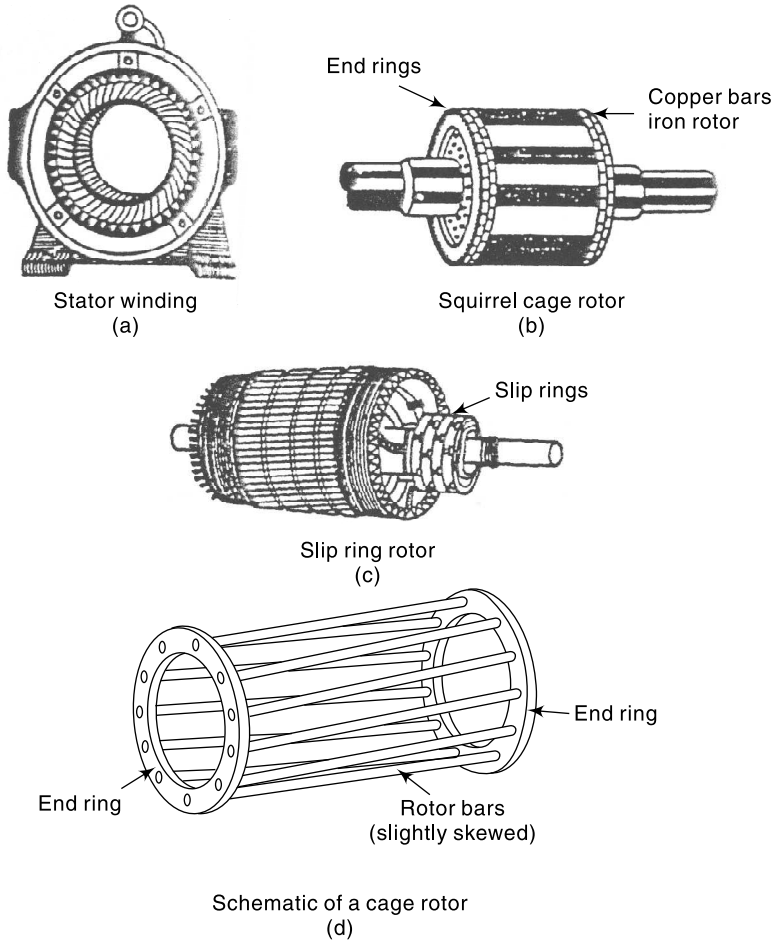


Fig. 5.1 ***Stator and rotor parts***

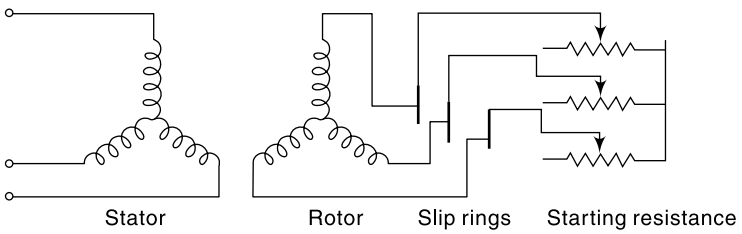


Fig. 5.2 ***Addition of external resistances to the rotor of wound rotor induction motor***

with each rotor phase (Fig. 5.2). This will increase the starting torque provided by the motor and will also help in reducing, the starting current. When running under normal condition, the external resistances are removed completely from the rotor by short circuiting these additional resistances from the rotor circuit and rotor behaves just like a squirrel cage rotor.

5.3 COMPARISON OF SQUIRREL CAGE AND WOUND ROTORS

The advantages of cage rotor induction motor are as follows:

(a) A rotor is of robust construction and cheaper.
(b) The absence of brushes reduces the risk of sparking.
(c) Squirrel cage rotors require lesser maintenance.
(d) Squirrel cage induction motors have higher efficiency and better power factor.

On the other hand, wound rotors have the following merits:

(a) High starting torque and low starting current.
(b) Additional resistance can be connected in the rotor circuit to control speed.

5.4 ADVANTAGES AND DISADVANTAGES OF A THREE-PHASE INDUCTION MOTOR

Advantages

(a) It is very simple, robust, rugged and capable of withstanding rough use.
(b) It is quite cheap in cost and reliable in operation.
(c) Its maintenance cost is low.
(d) The losses are reasonably small and hence it has sufficiently high efficiency.
(e) It is mostly a trouble-free motor.
(f) Its power factor is reasonably good at full load operation.
(g) It is simple to start (since it has a self starting torque).

An induction motor is equivalent to a static transformer whose secondary is capable of rotating with respect to the primary.

Usually the stator is treated as the primary, while the rotor is treated as the secondary. The induction motor operation is electrically equal even if the rotor is primary and the stator operation is treated as secondary.

Disadvantages

(a) Its speed cannot be varied without sacrificing efficiency.
(b) Its speed decreases with an increase in load.
(c) Its starting torque is inferior to that of a dc shunt motor.
(d) For direct on line starting, the starting current is usually 5 to 8 times of the full-load rated current.
(e) It runs at a low lagging power factor when it is lightly loaded.

5.5 PRINCIPLE OF OPERATION

A three-phase induction motor has a stator winding which is supplied by three-phase alternating balanced voltage and has balanced three-phase currents in the winding. The rotor is not excited from any source and has only magnetic coupling with the stator. Under normal running conditions, the rotor winding (cage or slip-ring) is always short circuited to allow induced currents to flow in the rotor

winding. The flow of three-phase currents in the stator winding produces a rotating magnetic field of constant amplitude and rotates at a synchronous speed. Let us assume that the rotor is at standstill initially; the rotating stator field induces an emf in the rotor conductor by transformer action. Since the rotor circuit is a closed set of conductors, a current flows in the rotor circuit. This rotor current then produces a rotor field. The interaction of stator and rotor field produces a torque which causes the rotation of the rotor in the direction of the stator rotating field.

As per Lenz's law, the rotor field will try to oppose the very cause of its production. Thus it speeds up in the direction of the stator field so that relative speed difference between these two fields is zero. In this way, the three-phase induction motor catches up the speed.

When the rotor is at standstill, the relative motion between the stator field and rotor is maximum. Therefore, the emf induced in the rotor and rotor current are reduced. However, the rotor cannot attain the speed of the stator field which is equal to the synchronous speed. This is evidently due to the reason that if the rotor is moving at synchronous speed, there is no relative motion between the stator field and the rotor. Hence the rotor induced emf and current become zero and the torque becomes zero. This would cause the rotor speed to decrease. As the rotor speed falls below the synchronous speed, the rotor emf and current continue to increase. Therefore, the electromagnetic torque continues to increase.

Finally, the rotor speed becomes constant at a value at speed slightly less than that of the stator field, the torque developed equals the sum of load torque and the mechanical losses.

5.6 CONCEPT OF PRODUCTION OF ROTATING FIELD

When a three-phase winding, *displaced in space* by 120°, are supplied by a three-phase currents *displaced in time* by 120°, a magnetic flux is produced which rotates in space. This causes the rotor to rotate. The method of analysis is as follows:

5.6.1 Analytical Method

Let us consider three identical coils placed 120° apart with respect to each other, as shown in Fig. 5.3(a).

The coils are supplied with currents having frequency of supply and varying sinusoidally in time. Each coil will produce an alternating flux along its own axis. Let the instantaneous flux be given by

$$\phi_1 = \phi_m \sin \omega t \qquad 5.1(a)$$

$$\phi_2 = \phi_m \sin (\omega t - 120°) \qquad 5.1(b)$$

$$\phi_3 = \phi_m \sin (\omega t - 240°) \qquad 5.1(c)$$

The resultant flux produced by this system may be determined by resolving the components with respect to the physical axis, as shown in Fig. 5.3(b).

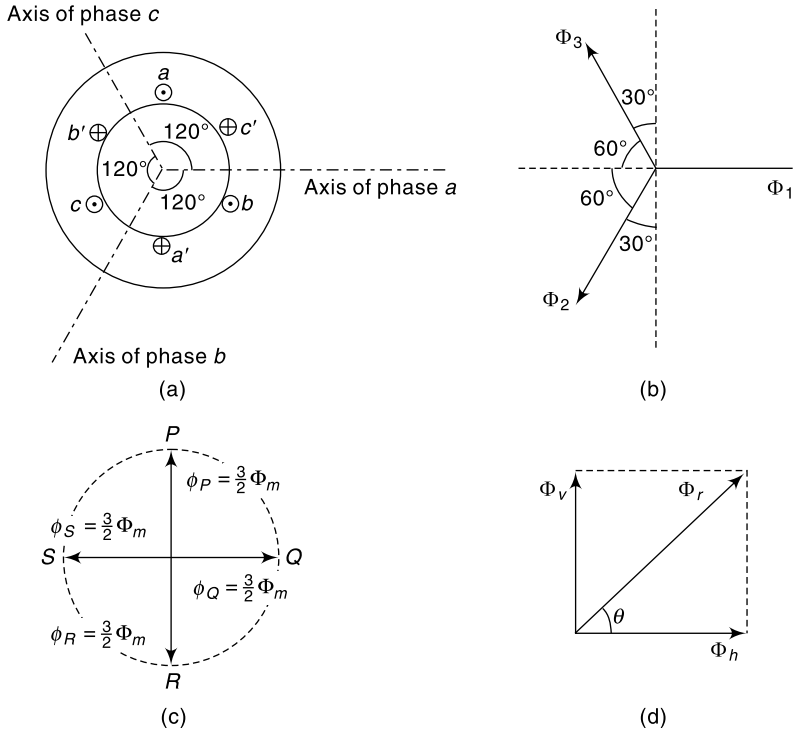


Fig. 5.3 ***Production of rotating field in a three-phase induction motor***

Therefore the resultant horizontal component of flux is given by

$$\begin{aligned}\phi_h &= \phi_1 - \phi_2 \cos 60° - \phi_3 \cos 60° \\ &= \phi_1 - (\phi_2 + \phi_3) \cos 60° \\ &= \phi_1 - (\phi_2 + \phi_3) \times \frac{1}{2} \\ &= \phi_m \sin \omega t - \frac{1}{2}[\phi_m \sin (\omega t - 120°) + \phi_m \sin (\omega t - 240°)] \\ &= \phi_m \sin \omega t - \frac{\phi_m}{2} \times (2 \sin \omega t)\left(-\frac{1}{2}\right) \\ &= \frac{3}{2}\phi_m \sin \omega t. \end{aligned} \tag{5.2}$$

Similarly, the vertical component of flux is given by

$$\begin{aligned}\phi_v &= 0 - \phi_2 \cos 30° + \phi_3 \cos 30° = \frac{\sqrt{3}}{2}[\phi_3 - \phi_2] \\ &= \frac{\sqrt{3}}{2}[\phi_m \sin (\omega t - 240°) - \phi_m \sin (\omega t - 120°)] \\ &= \frac{\sqrt{3}}{2} \times \phi_m \cdot 2 \cos \omega t \times \frac{\sqrt{3}}{2} \\ &= \frac{3}{2}\phi_m \cos \omega t \end{aligned} \tag{5.3}$$

∴ The resultant flux is (Fig. 5.3(d)),

$$\phi_r = \sqrt{(\phi_h)^2 + (\phi_v)^2} = \frac{3}{2}\phi_m \sqrt{\sin^2 \omega t + \cos^2 \omega t}$$

$$= \frac{3}{2}\phi_m \quad [\because \sin^2 \omega t + \cos^2 \omega t = 1] \tag{5.4}$$

and $$\tan \theta = \frac{\phi_v}{\phi_h} = \cot \omega t = \tan (90° - \omega t).$$

It implies $$\theta = (90° - \omega t). \tag{5.5}$$

The above equation shows that the resultant flux (ϕ_r) is free from time factor. It is a constant flux of magnitude equal to $\left(\frac{3}{2}\right)$ times the maximum flux per phase. However, θ is dependent on time and we can calculate θ at different values of (ωt); when (ωt) = 0, $\theta = \pi/2$ corresponding to position P in Fig. 5.3(c).

Similarly, for $\omega t = \pi/2$, $\theta = 0°$, corresponding to position Q,
when $\omega t = \pi$, $\theta = -\pi/2$, corresponding to position R,
when $\omega t = \frac{3\pi}{2}$, $\theta = -\pi$, corresponding to position S.

It is thus observed that the resultant flux ϕ_r rotates in space in the clockwise direction with angular velocity of ω radians per second.

Since $\omega = 2\pi f$ and $f = \frac{PN_s}{120}$, the resultant flux ϕ_r rotates with synchronous speed (N_s).

5.7 THE CONCEPT OF SLIP

The magnitude and frequency of the rotor voltages depend on the speed of the relative motion between the rotor and the flux crossing the air gap. The difference between the synchronous speed and the rotor speed expressed as a fraction (or percent) of synchronous speed is knows as *slip*, i.e.

Slip speed = $(n_s - n)$ rev/sec

and $$\text{slip (s)} = \frac{n_s - n}{n_s} \text{ p.u.} \tag{5.6(a)}$$

or $$n = n_s (1 - s) \text{ rps} \tag{5.6(b)}$$

where n_s = synchronous speed (rev/sec)
n = rotor speed (rev/sec)
s = slip.

When the speed is expressed in rpm, we can write

$$s = \frac{N_s - N}{N_s} \text{ p.u.} = \frac{N_s - N}{N_s} \times 100 \text{ (in \%)}$$

and $$N = N_s(1 - s) \text{ rpm.}$$

This slip s is a very useful quantity in studying induction motors.

The value of slip at full load is about 4 to 5% for small motors and about 2 to 2.5% for large motors. The slip at no load is about 1%. Thus the speed of an

induction motor is almost constant from no load to full load. If the machine has P number of poles, the frequency of induced emf in the rotor, i.e. f_2 is given by

$$f_2 = \frac{N_s - N}{N_s} \times f_1 \quad \left[\because\ f_1 = \frac{PN_s}{120};\ f_2 = \frac{P(N_s - N)}{120}\right.$$

$$\left. \text{and hence } (f_2/f_1) = \left(\frac{N_s - N}{N_s}\right)\right]$$

i.e. $f_2 = sf_1$

At standstill of the rotor, $s = 1$, i.e. the frequency of rotor currents is f_1 (the same as the supply frequency).

5.8 FREQUENCY OF ROTOR VOLTAGES AND CURRENTS

Let us consider a typical pair of rotor bars. As the rotor "slips" backward through the flux field, the flux linking these bars will vary cyclically. The voltage induced in the rotor circuit is composed of the voltages in these two bars and the end rings. It is at its peak at the instant when the rate of change of flux linkages is a maximum. Thus one cycle of rotor voltage is generated as a given conductor slips past two poles of the air-gap flux field. In other words, one cycle of rotor voltage corresponds to 360 electrical degrees of "slips". Then the frequency of the rotor voltages and currents is given by

f_2 = pole-pairs slipped per second

$$\frac{(n_s - n)}{n_s} \cdot n_s \cdot \frac{P}{2} = s \cdot f_1 \left[\because f_1 = \frac{PN_s}{120} = \frac{PN_s}{2 \times 60} = \frac{Pn_s}{2}\right]. \tag{5.7}$$

i.e., Rotor current frequency = Per unit slip × Supply frequency.

At standstill, rotor speed is zero.

$$\therefore \quad s = \frac{(n_s - n)}{n_s} = \frac{n_s - 0}{n_s} = 1$$

and $$f_2 = f_1. \tag{5.8}$$

5.1 A three-phase, 4-pole 50 Hz. induction motor runs at 1450 rpm. Find out the percentage slip of the induction motor.

Solution

$$N_s = \frac{120\,f}{P} = \frac{120 \times 50}{4} = 1500 \text{ rpm}$$

$$\therefore \quad \text{Slip} = \frac{N_s - N}{N_s} = \frac{1500 - 1450}{1500} = 0.033 = 3.33\%.$$

5.2 A three-phase, 50 Hz., 6-pole induction motor runs at 950 rpm. Calculate

(i) the synchronous speed
(ii) the slip and
(iii) frequency of the rotor emf.

Solution

(i) We know, $N_s = \dfrac{120\,f}{P} = \dfrac{120 \times 50}{6} = 1000$ rpm.

(ii) Slip $(s) = \dfrac{N_s - N}{N_s} = \dfrac{1000 - 950}{1000} = 0.05.$

$\therefore$ percentage of slip $= 0.05 \times 100 = 5.$

(iii) The frequency of rotor emf $= s.f_1 = 0.05 \times 50 = 2.5$ Hz.

5.3 The frequency of the emf in the stator of a 4-pole induction motor is 50 Hz., and that in the rotor is 2 Hz. What is the slip and at what speed is the motor running?

Solution

We know $f_2 = s \cdot f_1$

$\therefore$ $s = \dfrac{f_2}{f_1} = \dfrac{2}{50} = 0.04 = 4\%.$

Again $f_1 = \dfrac{P \cdot N_s}{120}$

$\therefore$ $N_s = \dfrac{120 \cdot f_1}{P} = \dfrac{120 \times 50}{4} = 1500$ rpm.

Speed of the motor

$N = (1 - s) \cdot N_s = (1 - 0.04) \times 1500 = 1440$ rpm.

5.4 A 10-pole induction motor is supplied by a 6-pole alternator, which is driven at 1400 rpm. If the motor runs with a slip of 2%, what is its speed?

Solution

For induction motor: Synchronous speed is given by

$$N_s = \frac{120\,f}{P} = \frac{120 \times 70}{10} = 840 \text{ rpm} \quad \left[\because f = \frac{PN_A}{120} = \frac{6 \times 1400}{120} = 70\,\text{Hz}.\right]$$

Now slip, $s = \dfrac{N_s - N}{N_s} = \dfrac{840 - N}{840}$

$\therefore$ $0.02 = \dfrac{840 - N}{840}$

$\therefore$ $N = 823.2$ rpm.

5.5 A three-phase 60 Hz induction motor has a no load speed of 890 rpm and a full load speed of 855 rpm. Calculate

(i) the number of poles
(ii) slip s at no load
(iii) slip at full load
(iv) frequency of rotor currents at no load
(v) frequency of rotor currents at full load.

Solution

(i) Since the no load slip of an induction motor is about one percent, the synchronous speed is slightly larger than the no load speed of 890 rpm. For 60 Hz frequency, the number of poles and their corresponding synchronous speeds are

P	2	4	6	8	10
N_s (rpm)	3600	1800	1200	900	720

It is obvious that the synchronous speed can be only 900 rpm and therefore the number of poles is 8.

(ii) No load slip (s) = $\frac{900-890}{900} \times 100 = 1.11\%$.

(iii) Full load slip = $\frac{900-855}{900} \times 100 = 5\%$.

(iv) At no load, f_2 (= sf_1) = $\frac{1.11}{100} \times 60 = 0.66$ Hz.

(v) At full load, $f_2 = \frac{5}{100} \times 60 = 3$ Hz.

5.6 A three-phase 6-pole induction motor runs at 760 rpm at full load. It is supplied from an alternator having four poles and running at 1200 rpm. Determine the full-load slip of the induction motor.

Solution

Given the number of poles of alternator $P_A = 4$ and the synchronous speed of the alternator is 1200 rpm, the frequency f is $\frac{N \cdot P_A}{120} = \frac{1200 \times 4}{120} = 40$ Hz.

∴ Frequency generated by the alternator is 40 Hz.

For the given induction motor, $P = 6$, Speed at full load $N = 760$ rpm, supply frequency from the alternator is $f = 40$ Hz.

∴ Synchronous speed of the motor, $N_s = \frac{120\,f}{P} = \frac{120 \times 40}{6} = 800$ rpm.

∴ The percentage slip, $s = \frac{N_s - N}{N_s} \cdot 100 = \frac{800-760}{800} \times 100 = 5\%$.

5.7 A three-phase, 400 V, 50 Hz induction motor has a speed of 900 rpm on full-load. The motor has six poles. (i) Find out the slip. (ii) How many complete alternations will the rotor voltage take per minute?

Solution

(i) Given $N = 900$ rpm, $f = 50$ Hz and $P = 60$.

∴ $N_s = \frac{120 \times f}{P} = \frac{120 \times 50}{6} = 1000$ rpm

∴ slip (s) = $\frac{N_s - N}{N_s} = \frac{1000-900}{1000} = 0.1$ or 10%.

(ii) Alternation of rotor voltage:

$f' = s \times f = 0.01 \times 50 = 0.5$/sec or 30/min.

5.8 A three-phase, 6-pole, 50 Hz induction motor has a slip of 0.8% at no load and 2% at full load. Calculate:

(i) the synchronous speed
(ii) the no-load speed
(iii) the full-load speed
(iv) the frequency of rotor current at standstill
(v) the frequency of rotor current at full load.

Solution

(i) $N_s = \dfrac{120\,f}{P} = \dfrac{120 \times 50}{6}$ = 1000 rpm.

(ii) Speed at no load = (1 – slip at no load) × N_s = (1 – 0.008) × 1000 = 992 rpm.

(iii) Speed at full load = (1 – slip at full load) × N_s = (1 – 0.02) × 1000 = 980 rpm.

(iv) Frequency of rotor current at standstill $f_2 = sf = 1 \times 50 = 50$ Hz.

(v) Frequency of rotor current at full load, f_2 = (slip at full load) × f
= 0.02 × 50 = 1.0 Hz.

5.9 The voltage applied to the stator of a three-phase, 4-pole induction motor has a frequency of 50 Hz. The frequency of the emf induced in the rotor is 1.5 Hz. Determine slip and speed at which motor is running.

Solution

(i) $N_s = \dfrac{120\,f}{p} = \dfrac{120 \times 50}{4}$ = 1500 rpm.

Rotor emf frequency, $f_2 = sf$

or $1.5 = s \times 50$

$\therefore$ slip $(s) = \dfrac{1.5}{50}$ = 0.03 or 3.0%.

(ii) Actual speed of motor is $N = (1 - s) \cdot N_s = 1500\ (1 - 0.03) = 1455$ rpm.

5.10 A three-phase, 50 Hz, 6-pole cage motor is running with a slip of 3%. Calculate:

(i) the speed of the rotating field relative to the stator winding

(ii) the motor speed

(iii) the frequency of emf induced in the rotor

(iv) the speed of rotation of rotor mmf relative to rotor winding

(v) the speed of rotation of rotor mmf relative to stator winding.

Solution

(i) $N_s = \dfrac{120\,f}{P} = \dfrac{120 \times 50}{6}$ = 1000 rpm.

(ii) $N = N_s(1 - s) = 1000\left(1 - \dfrac{3}{100}\right)$ = 970 rpm.

(iii) $f_2 = sf_1 = \dfrac{3}{100} \times 50 = 1.5$ Hz.

(iv) Speed of rotor mmf relative to rotor winding = $\dfrac{120 \times f_2}{P} = \dfrac{120 \times 1.5}{6}$ = 30 rpm.

(v) Since the rotor is rotating at 970 rpm and the rotor mmf is revolving at 30 rpm with respect to rotor, therefore speed of the rotor mmf relative to the stationary winding (stator) is (970 + 30) rpm = 1000 rpm.

5.9 TORQUE EXPRESSION OF AN INDUCTION MOTOR

Operating Torque

In the induction motor, the torque T is given by

$$T \propto \phi \cdot I_r \cdot \cos \phi_r \qquad (5.9)$$

where ϕ is the stator flux/pole and I_r is the rotor current/phase under running conditions, cos ϕ_r is the rotor power factor.

We have $$I_r = \frac{E_r}{Z_r} = \frac{E_2 \cdot s}{\sqrt{R_2^2 + (sX_2)^2}} \tag{5.10}$$

and $$\cos \phi_r = \frac{R_r}{Z_r} = \frac{R_2}{Z_r} = R_2 \Big/ \sqrt{R_2^2 + (sX_2)^2} \tag{5.11}$$

($\because$ Resistance is independent of relative speed)

where E_r is rotor emf/phase

Z_r is the rotor impedance = $\sqrt{R_2^2 + (sX_2)^2}$

R_r is the rotor resistance/phase.

E_r, Z_r, R_r are the respective parameters of the rotor in running conditions. If s be the slip of the motor, operating at rated speed, we can write

$$X_r = sX_2$$

$$E_r = sE_2$$

and $$R_r = R_2$$

where, X_r is the rotor reactance/phase under running condition.

In the standstill condition,

X_2 is the rotor reactance/phase

E_2 is the rotor emf/phase

and R_2 is the rotor resistance/phase.

From the fundamentals, we have

$$|Z_r| = \sqrt{R_r^2 + X_r^2} = \sqrt{R_2^2 + X_r^2}\ .$$

The equation of the torque can be rewritten as

$$T = K_1 \phi \frac{E_r}{Z_r} \cdot \frac{R_2}{Z_r}$$

[K_1 is the constant of proportionality in Eq. (5.9)]

$$= \frac{K_1 \phi\, sE_2\, R_2}{R_2^2 + X_r^2} = \frac{K_1 \phi\, sE_2\, R_2}{R_2^2 + (sX_2)^2}\ . \tag{5.12}$$

Again, the flux(ϕ) produced by the stator being proportional to the applied phase voltage (E_1), we can write

$$\phi \propto E_1$$

i.e., $$\phi = K_2 E_1$$

Also $$\frac{E_1}{E_2} = \frac{N_1}{N_2} = k.$$

$\therefore$ $$E_2 = \frac{1}{k} \cdot E_1$$

Substituting the expressions for ϕ and E_2 in Eq. (5.12) we get

$$T = \frac{K_1 \cdot K_2 E_1 \cdot s \cdot (E_1/k) \cdot R_2}{R_2^2 + (sX_2)^2} = \frac{KE_1^2 \cdot s \cdot R_2}{R_2^2 + (sX_2)^2} \tag{5.13}$$

where $$K = \frac{K_1 K_2}{k}$$

i.e., $$T \propto \frac{sE_1^2 R_2}{R_2^2 + (sX_2)^2} \tag{5.13a}$$

Here T is expressed in watts on per phase basis for $K = 1$. In order to get the value of three-phase torque, the expression obtained in (5.13) or (5.13a) is to be multiplied by a factor 3, provided K is known and all the quantities in the RHS of equation (5.13) are expressed in phase values. We will discuss later how K can be obtained. Actually $K = \frac{3}{\omega_s}$, where $\omega_s = 2\pi n_s$, n_s is expressed in rps i.e., equal to $\left(\frac{N_s}{60}\right)$. For three phase, the electromagnetic torque T is

$$T_{3\phi} = \frac{3}{\omega_s} \cdot \frac{sE_1^2 R_2}{R_2^2 + (sX_2)^2} \text{ Nm}$$

i.e. $$T_{3\phi} = 3 \cdot \frac{sE_1^2 R_2}{R_2^2 + (sX_2)^2} \text{ W} \left(= \frac{3}{\omega_s} \cdot \frac{sE_1^2 R_2}{R_2^2 + (sX_2)^2} \text{ Nm} \right). \tag{5.13b}$$

5.9.1 Starting Torque (T_s)

At starting the rotor is stationary, the slip $s = 1$ and the rotor reactance X_2 is much larger compared to the rotor resistance R_2. So neglecting R_2 in Eq. (5.13 a), we get for $s = 1$,

$$T_s \propto \frac{E_1^2 R_2}{X_2^2} \tag{5.14a}$$

or $T_s \propto R_2$ and $T_s \propto E_1^2$ [assuming (X_2) as constant]

The general expression of starting torque can be obtained from equation (5.13) with $s = 1$.

$$T_s = \frac{KE_1^2 R_2}{R_2^2 + X_2^2} \tag{5.14b}$$

Thus for obtaining large starting torque, the rotor resistance R_2 as well as applied voltage E_1 should be large.

To get the three-phase starting torque, T_s obtained in Eq. 5.14(a) or (b) is to be multiplied by a factor 3.

5.9.2 Effect of Change in Supply Voltage on Torque and Slip

Since $$T \propto \frac{sE_1^2 R_2}{R_2^2 + (sX_2)^2},$$

at rated speed, with low values of s we have

$$T \propto \frac{sE_1^2 R_2}{R_2^2} \quad (\because (sX_2) \text{ is very low})$$

i.e. $$T \propto \frac{sE_1^2}{R_2}$$

i.e., torque under normal operating condition is proportional to the square of supply voltage. With drop in supply voltage, running torque T decreases and to maintain same torque, slip must increase (i.e., speed drops.)

5.9.3 Effect of Change in Supply Voltage in Starting Torque

Since $$T_s \propto \frac{E_1^2 R_2}{X_2^2},$$

at constant (X_2) and (R_2), the *starting torque is also proportional to the square of the supply voltage*.

5.9.4 Condition for Maximum Torque

Under normal running conditions,

$$T = \frac{KE_1^2 \; R_2 \cdot s}{R_2^2 + X_2^2 \cdot s^2} \tag{5.15}$$

When the motor is operating on constant applied voltage E_1, then

$$T = \frac{K' R_2 s}{R_2^2 + X_2^2 s^2} = \frac{K' R_2}{\frac{R_2^2}{s} + X_2^2 s} \quad [K' = KE_1^2]$$

Since the numerator of the right hand side of the expression is constant, thus for getting the condition for maximum torque we differentiate the denominator with respect to slip s and equate the differential co-efficient to zero.

Thus we have, at maximum torque condition,

$$-(R_2^2/s^2) + X_2^2 = 0$$

or $$X_2^2 = R_2^2/s^2$$

or $$s = s_{\max} = \frac{R_2}{X_2} \tag{5.16}$$

(where $s_{\max}$ is *slip for maximum torque*)

From Eq. (5.15) (at constant applied voltage E_1), and (5.16), we have

$$T_{\max} = \frac{K \cdot R_2 \cdot \left(\frac{R_2}{X_2}\right) \cdot E_1^2}{R_2^2 + X_2^2 \cdot \frac{R_2^2}{X_2^2}} = \frac{K \cdot R_2^2 \cdot E_1^2}{2R_2^2 X_2} = \frac{K''}{X_2} \tag{5.17a}$$

Also, $$T_{\max} = \frac{KE_1^2 \; (sX_2) \cdot s}{(sX_2)^2 + (sX_2)^2}$$ [using $R_2 = sX_2$ in Eq. (5.15) to obtain $T_{\max}$]

$$= \frac{KE_1^2}{2X_2} \tag{5.17b}$$

[it may be noted here that $K'' = \frac{K}{2} \cdot E_1^2$]

Thus the *maximum torque of an induction motor, operating on constant applied phase voltage E_1 and constant supply frequency f is inversely proportional to the standstill rotor reactance X_2 but is independent of rotor circuit resistance R_2*. The slip for maximum torque is the ratio of rotor resistance and standstill rotor-reactance, i.e. $S_{\max} = \frac{R_2}{X_2}$.

Also,
$$\frac{T}{T_{\max}} = \frac{KE_1^2 \cdot R_2 \cdot s}{X_2^2\left(\frac{R_2^2}{X_2^2} + s^2\right)} \Bigg/ \frac{K''}{X_2}$$

$$= \frac{KE_1^2 \cdot R_2 \cdot s}{X_2^2\left(s_{\max}^2 + s^2\right)} \frac{X_2}{K''}$$

$$= K''' \cdot \frac{s_{\max} \cdot s}{s^2 + s_{\max}^2} \left[K''' = \frac{KE_1^2}{K''}\right] \tag{5.18(a)}$$

Also, we can write

$$\frac{T}{T_{\max}} = \frac{KE_1^2 R_2 s}{R_2^2 + (sX_2)^2} \Bigg/ \frac{KE_1^2}{2X_2} = \frac{2sR_2 X_2}{R_2^2 + (sX_2)^2} \tag{5.18b}$$

$$= \frac{2s \cdot s_{\max}}{s^2 + s_{\max}^2} \tag{5.18c}$$

Equations (5.18(a)) and (5.18(c)) are identical if we use the relation $K''' = \frac{KE_1^2}{K''}$ and $K'' = \frac{K}{2} \cdot E_1^2$ in Eq. 5.18(a).

At starting, $s = 1$

$$\therefore \quad \frac{T_s}{T_{\max}} = \frac{K''' \cdot s_{\max}}{(1 + s_{\max}^2)} = \frac{K''' \cdot a}{1 + a^2} \text{ (where } a = s_{\max}) \tag{5.19a}$$

[Also for Eq. 5.18(c), at $s = 1$, $\frac{T_s}{T_{\max}} = \frac{2s_{\max}}{1 + s_{\max}^2}$; (5.19b)

from the equation of torque we can write

$$\frac{T_s}{T} = \frac{KE_1^2 R_2}{R_2^2 + X_2^2} \times \frac{R_2^2 + s^2 X_2^2}{KE_1^2 R_2 \cdot s} = \frac{s^2 + \left(\frac{R_2}{X_2}\right)^2}{s\left[1 + \left(\frac{R_2}{X_2}\right)^2\right]} = \frac{s^2 + s_{\max}^2}{s(1 + s_{\max}^2)} \tag{5.19c}$$

Case I (Squirrel-cage induction motor) Since the rotor is permanently short-circuited, so no resistance can be inserted in its rotor circuit. Thus, slip for maximum torque is constant, and its value cannot be varied.

Case II (Slip ring induction motor) Since external resistance can be inserted in the rotor circuit, so its slip can be varied for maximum torque. For rotor circuit without external resistance

$$s_{max}\ (1) = \frac{R_2}{X_2}$$

and if a resistance r per phase is inserted in the rotor circuit, then

$$s_{max}(2) = (R_2 + r)/X_2. \tag{5.20}$$

5.9.5 Condition for Maximum Starting Torque

At starting, the starting torque (for a given applied voltage) is given by

$$T_s = \frac{KE_1^2 R_2}{R_2^2 + X_2^2} = \frac{K' R_2}{R_2^2 + X_2^2} \tag{5.21}$$

We obtain maximum starting torque by differentiating expression (5.21)

$$\frac{dT_s}{dR_2} = K\left[\frac{1\cdot(R_2^2 + X_2^2) - R_2(2R_2)}{(R_2^2 + X_2^2)^2}\right] = 0$$

$$R_2^2 + X_2^2 - 2R_2^2 = 0$$

$$R_2 = X_2$$

i.e. for a given applied voltage E_1, the starting torque is maximum when the resistance of rotor R_2 equals its reactance X_2.

5.11 A three-phase 4-pole 50 Hz induction motor has a rotor resistance of 0.020 Ω/phase and standstill reactance of 0.5 Ω/phase, calculate the speed at which the maximum torque is developed.

Solution

$$N_s = \frac{120\,f}{P} = \frac{120\times 50}{4} = 1500 \text{ rpm}$$

For maximum torque slip $s_{max} = \frac{R_2}{X_2} = \frac{0.020}{0.5} = 0.04$

$\therefore$ Speed at maximum torque = $N_s(1 - s_{max})$ = 1500 (1 – 0.04) = 1440 rpm.

5.12 A three-phase 8-pole 50 Hz. induction motor has a full-load slip of 1.5%, the rotor resistance is 0.001 Ω/phase and the standstill reactance is 0.005 Ω/phase. Calculate the ratio of the maximum to full load torque, and the speed at which maximum torque takes place.

Solution

Given f = 50 Hz., P = 8, s = 0.015, R_2 = 0.001 Ω;

X_2 = 0.005 Ω,

$$s_{max} = \frac{R_2}{X_2} = \frac{0.001}{0.005} = 0.2$$

Now $$\frac{T}{T_{max}} = \frac{2\cdot s\cdot s_{max}}{s^2 + s_{max}^2} = \frac{2\times 0.015\times 0.2}{(0.015)^2 + (0.2)^2} = \frac{6\times 10^{-3}}{4.02\times 10^{-2}}$$

$$\therefore \quad \frac{T_{max}}{T} = \frac{4.02 \times 10^{-2}}{6 \times 10^{-3}} = 6.7$$

Now, $$N_s = \frac{120\,f}{P} = \frac{120 \times 50}{8} = 750 \text{ rpm}$$

$\therefore$ Speed at maximum torque = $N_s\,(1 - s_{max}) = 750(1 - 0.2) = 600$ rpm.

5.13 A three-phase, 50 Hz. 6-pole induction motor runs on full load with a slip of 0.04. Determine the available maximum torque in terms of full load torque. Also determine the speed at which the maximum torque takes place. [Given that the rotor standstill impedance per phase is $(0.01 + j\,0.05)\ \Omega$.]

Solution

Given slip (s) = 0.04

$$s_{max} = \frac{R_2}{X_2} = \frac{0.01}{0.05} = 0.2$$

$\therefore$ Speed at maximum torque = $N_s(1 - s_{max}) = (1 - 0.2) \times 1000 = 800$ rpm

$$\therefore \quad \frac{T_{max}}{T} = \frac{s^2 + s_{max}^2}{2 \cdot s \cdot s_{max}} = \frac{(0.04)^2 + (0.2)^2}{2 \times 0.04 \times 0.2} = 2.6$$

or $$T_{max} = 2.6 \times T \quad [T \text{ is full load torque}].$$

5.14 A three-phase, 50 Hz 4-pole induction motor (slip ring) develops a maximum torque of 100 Nm at 1400 rpm. The resistance of the star connected rotor is 0.25 Ω/phase. Determine the value of resistance that must be inserted in series with each rotor phase to produce a starting torque equal to half the maximum torque.

Solution

The synchronous speed $N_s = \frac{120\,f}{P} = \frac{120 \times 50}{4} = 1500$ rpm.

Speed at maximum torque = 1400 rpm (given)

$$\therefore \text{ Slip } (s_{max}) \text{ at maximum torque } = \frac{N_s - \text{speed at maximum torque}}{N_s}$$

$$= \frac{1500 - 1400}{1500} = 0.067.$$

Also, $$s_{max} = \frac{R_2}{X_2}$$

$$\therefore \quad X_2 = \frac{R_2}{s_{max}} = \frac{0.25}{0.067} = 3.73$$

$$T_{max} = \frac{KE_1^2}{2X_2} = \frac{KE_1^2}{2 \times 3.73} = 0.134\,KE_1^2$$

Let r be the external resistance to be inserted per phase in the rotor circuit, then starting torque

$$T_{st} = \frac{K \cdot E_1^2\,(R_2 + r)}{(R_2 + r)^2 + X_2^2} = \frac{K(0.25 + r)\,E_1^2}{(0.25 + r)^2 + (3.73)^2}$$

Again, it is given that $T_{st} = \frac{1}{2} T_{max}$;

$$\therefore \quad \frac{K(0.25 + r) \cdot E_1^2}{(0.25 + r)^2 + (3.73)^2} = \frac{1}{2} \times 0.134\, K \cdot E_1^2.$$

Simplifying,

r = 13.67 ohm or 0.75 ohm;

but we ignore the value of r = 13.67 ohm as it corresponds to T_{max} lying in the region where $s > 1$.

$\therefore$ r = 0.75 ohm per phase.

5.15 A three-phase, 24-pole, 50 Hz, 3200 volt star connected induction motor has a slip ring rotor of resistance 0.016 Ω and standstill reactance of 0.270 Ω per phase. Full load torque is obtained at a speed of 247 rpm. Determine:

(a) the ratio of maximum to full-load torque.

(b) the speed at maximum torque, stator impedance being neglected.

Solution

(i) Synchronous speed $N_s = \frac{120\, f}{P} = \frac{120 \times 50}{24}$ = 250 rpm.

$\therefore$ Slip $(s) = \frac{N_s - N}{N_s} = \frac{250 - 247}{250}$ = 0.012.

Also, $s_{max} = \frac{R_2}{X_2} = \frac{0.016}{0.270}$ = 0.059.

We know, $\frac{T}{T_{max}} = \frac{2 \cdot s_{max} \cdot s}{s^2 + s_{max}^2}$.

Here, $\frac{T}{T_{max}} = \frac{2 \times 0.059 \times 0.012}{(0.012)^2 + (0.059)^2}$

or $\frac{T_{max}}{T} = \frac{(0.012)^2 + (0.059)^2}{2 \times 0.059 \times 0.012}$ = 2.56.

Let N' be the intended speed at maximum torque

Then, $s_{max} = \frac{N_s - N'}{N_s} = \frac{250 - N'}{250}$

s_{max} = 0.059 from calculation we have got earlier.

i.e., $0.059 = \frac{250 - N'}{250}$

or N' = 235.25 rpm.

5.16 A three-phase, 6-pole 50 Hz. induction motor develops a maximum torque of 30 Nm at 960 rpm. Calculate the torque produced by the motor at 6% slip. The rotor resistance per phase is 0.6 Ω.

Solution

Given, f = 50 Hz., P = 6

$\therefore$ $N_s = \frac{120\, f}{P} = \frac{120 \times 50}{6}$ = 1000 rpm.

Speed at maximum torque = 960 rpm

Slip at maximum torque $= \dfrac{N_s - \text{speed at maximum torque}}{N_s} = \dfrac{1000 - 960}{1000} = 0.04\ (= s_{max})$

Also, $s_{max} = \dfrac{R_2}{X_2}$

$\therefore \quad X_2 = \dfrac{R_2}{s_{max}} = \dfrac{0.6}{0.04} = 15\ \Omega.$

If T is the torque at slip s, $\dfrac{T}{T_{max}} = \dfrac{2s \cdot s_{max}}{s^2 + s_{max}^2}$

here, $s = 0.06,\ T_{max} = 30$ Nm

$\therefore \quad T = \dfrac{2 \times 0.06 \times 0.04}{(0.06)^2 + (0.04)^2} \times 30 = 27.692$ Nm.

5.17 A 746 kW, three-phase, 50 Hz., 16-pole induction motor has a rotor impedance of $(0.02 + j0.15)$ ohm at standstill. Full load torque is obtained at 350 rpm.

Determine (i) the speed at which maximum torque occurs, (ii) the ratio of maximum to full load torque, (iii) the external resistance per phase to be inserted in the rotor circuit to get maximum torque at starting.

Solution

$$N_s = \frac{120\,f}{P} = \frac{120 \times 50}{16} = 375 \text{ rpm}$$

Speed at full load = 350 rpm

$\therefore$ Slip at full load $= \dfrac{375 - 350}{375} = 0.06$

Slip at maximum torque

$$s_{max} = \frac{R_2}{X_2} = \frac{0.02}{0.15} = \frac{2}{15} = 0.133$$

(i) Speed at which maximum torque occurs $= (1 - s_{max})N_s = \left(1 - \dfrac{2}{15}\right) \times 375 = 325$ rpm.

(ii) $\dfrac{T_{max}}{T} = \dfrac{s_{max}^2 + s^2}{2s \cdot s_{max}} = \dfrac{(0.06)^2 + \left(\dfrac{2}{15}\right)^2}{2 \times 0.06 \times \dfrac{2}{15}} = 1.33.$

(iii) Let the external resistance per phase added to the rotor circuit be 'r' Ω, so that R rotor resistance per phase, $R_2 = (0.02 + r)$.
The starting torque will be maximum when $R_2 = X_2$
$\therefore \quad 0.02 + r = 0.15$
or $\quad r = 0.13\ \Omega$ per phase.

5.10 TORQUE SLIP CHARACTERISTICS OF A THREE-PHASE INDUCTION MOTOR

The torque T of an induction motor (three-phase) is given by (Eq. 5.13)

$$T = \frac{KE_1^2\ R_2 \cdot s}{R_2^2 + X_2^2 s^2}$$

For a constant supply voltage E_1, the value of E_2 is constant. Assuming R_2 as constant, we can write

$$T \propto \frac{s}{R_2^2 + X_2^2 s^2} \tag{5.22}$$

At synchronous speed, slip s is zero, hence torque T is zero; at starting $s = 1$, thus torque T is maximum.

Consequently, the torque slip curve starts from origin (i.e., $s = 0$), and ends at $s = 1$.

Case study I When s (slip) is very low (at rotor speeds close to synchronous speed), $sX_2 \ll R_2$ and $T \propto \frac{s}{R_2^2}$ (at low-slips).

i.e., *Torque-slip curve at low values of slip is a straight line passing through the origin, and torque is maximum when* $s = \frac{R_2}{X_2}$.

Case study II When the load on the motor increases, the speed of the motor decreases. When slip s is large, compared to R_2, sX_2 is much large and hence $sX_2 \gg R_2$.

$$\therefore \quad T \propto \frac{s}{(sX_2)^2} \propto \frac{1}{sX_2^2} \propto \frac{1}{s} \quad \text{(at high slips)}$$

i.e., the torque T slip s curve for larger values of slip is approximately a rectangular hyperbola. Consequently, any further increase in motor load, beyond the point of maximum torque, results in decrease of the torque developed by the motor. Eventually, the motor slows down. The maximum torque developed in an induction motor is called the *pull-out torque* or *break down torque*. This torque is a measure of the short time over loading capability of the motor. Figure 5.4 Shows the torque-slip characteristics of an induction motor operating with constant applied voltage, and constant frequency.

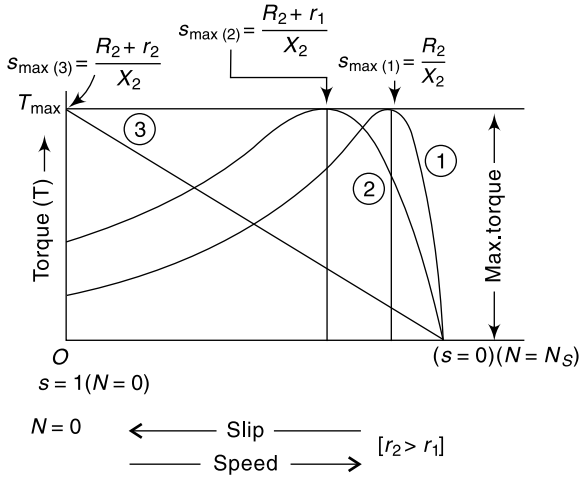


Fig. 5.4 ***Torque-slip characteristics of an induction motor***

Curve 1 represents (T-s) characteristic of an induction motor having low rotor resistance or when no resistance is inserted in the rotor circuit.

Maximum torque is developed at s_{max} (1) = $\frac{R_2}{X_2}$.

Curve 2 represents the (T-s) characteristic of an induction motor. When an external resistance of r_1 Ω/phase is inserted in the rotor circuit the magnitude of the maximum torque remains unchanged, but the slip for maximum torque in $s_{max}(2) = (R_2 + r_1)/X_2$.

Curve 3 represents the (T-s) characteristic of an induction motor, when an external resistance of r_2 Ω/phase is inserted in the rotor circuit such that $R_2 + r_2 = X_2$, a condition for maximum torque is there at starting.

It may be noted here that $(R_2 + r_2) > (R_2 + r_1) > R_2$

It is also seen that *as the rotor resistance is increased, the pull out speed of the motor decreases, but the maximum torque remains constant*. However, for squirrel cage rotors it is not possible to insert any rotor resistance under normal operating conditions and hence *it is not easily possible to enhance the value of the starting or maximum torque for a squirrel cage induction motor.*

5.11 EQUIVALENT CIRCUIT OF INDUCTION MOTOR

In the case of an ideal induction motor, the equivalent circuit can be represented like that of an ideal transformer. The only difference is that the rotor of induction motor is not static and mechanical power is developed.

Figure 5.5(a) shows the equivalent circuit of an induction motor with all quantities referred to the stator. During shifting of impedance or resistance from the secondary to primary, the secondary quantity is multiplied by (k^2), (where k = transformation ratio = number of stator turns/number of rotor turns). *It is to be remembered that the equivalent circuit is always drawn for the per phase values.*

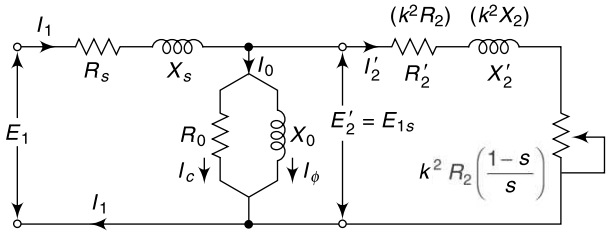


Fig. 5.5(a) ***Equivalent circuit of an induction motor***

Looking at the stator side, counter emfs are generated in all the three phases of stator due to rotating air-gap flux wave. The application of a voltage E_1 to the stator winding creates a mutual flux which sets up induced emf E_{1s} in the stator and rotor. Since $E_{1s} < E_1$, so this difference $(E_1 - E_{1s})$ represents the impedance drop $[I_1 (R_s + jX_s)]$. The effect of no-load current I_0 (= $I_C + I_\phi$, where I_C is the core loss component and I_ϕ is the magnetizing component lagging by an angle $\pi/2$ and is represented by a shunt consisting of R_0 and X_0 connected in parallel).

Thus, R_0 and X_0 account for *working component* and *magnetizing component* of no-load current respectively.

Now, if we block the rotor and make the total rotor resistance equal to R_2/s by inserting an additional resistance in the rotor circuit, then the rotor current, mmf, reactance of rotor on stator, stator current and input to machine would be same as they were when the rotor was running at slip s.

Also, $\frac{R_2}{s} = R_2 + R_2\left(\frac{1-s}{s}\right)$

= Actual resistance of rotor + Fictitious resistance $\left(R_2 \cdot \frac{1-s}{s}\right)$.

Let us calculate the rotor quantities with respect to the stator. If k is the effective transformation ratio then total rotor resistance R_2 and reactance X_2, when referred to the stator, appear as R_2' and X_2' where ($R_2' = R_2k^2$) and ($X_2' = X_2k^2$). Moreover, the rotor current I_2 when referred to the stator, appears as $I_2'\left(=\frac{I_2}{k}\right)$.

Also, $I_2' + I_0 = I_1$ (stator current). In the above expression $\left[R_2\left(\frac{1-s}{s}\right)\right]$ is the electrical analogue of the variable mechanical load and is the *fictitious resistance* equivalent to load on the motor.

The equivalent circuit can be simplified by transforming no-load current component to the supply side as shown in Fig. 5.5(b).

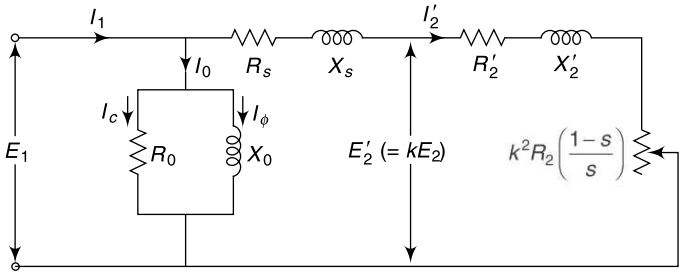


Fig. 5.5(b) ***Simplified equivalent circuit***

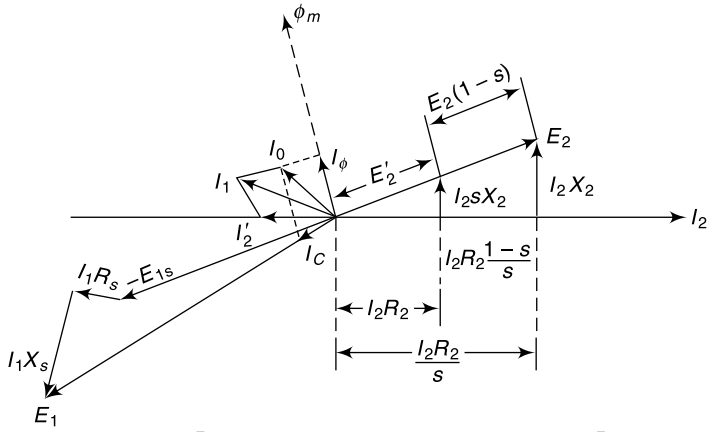
The phasor diagram of the induction motor is shown in Fig. 5.5(c).

5.12 LOSSES AND EFFICIENCY

At starting and during acceleration the rotor core losses are high; with the increase in speed these losses decrease to some extent. The friction and windage losses are zero at start and with increase in speed these losses increase. However, the sum of friction, windage and core losses is roughly constant for a motor even with variable speed. Therefore, these categories of losses are sometimes lumped together and called *constant losses* and are then defined as follows:

$$P_{(\text{constant loss})} = P_{\text{core loss}} + P_{\text{mechanical loss}}$$

$\therefore$ Output power P_0 = Total mechanical power developed – Mechanical losses



$$\left[-E_{1s} = E_2;\ I'_2 = I_2 / k;\ I_o = \sqrt{I_C^2 + I_\phi^2};\ I_1 = \sqrt{I_0^2 + I_2'^2};\ \frac{I_2R_2}{s} = I_2R_2 + I_2R_2\frac{1-S}{S}\right]$$

Fig. 5.5(c) ***Phasor diagram of a 3-phase induction motor on per phase basis***

Losses in a three-phase Induction motor are of two types mainly (a) Fixed losses and (b) Variable losses.

(a) Fixed losses
- Core loss
- Bearing friction loss
- Brush friction loss in wound rotors
- Windage loss

(b) Variable losses
- Stator ohmic loss (I^2R loss in stator)
- Rotor ohmic loss (I^2R loss in rotor)
- Brush contact loss for wound rotor motors only
- Stray load loss.

The rotor output gives rise to the development of *gross torque* or *electromagnetic torque* T_g, which is partly "wasted" (in the form of winding, and frictional losses in the rotor), and partly appears as the *useful shaft torque* T_{sh}. Let n be the actual speed of the rotor (in rps) and T_g be the gross torque (or electromagnetic torque) developed by the rotor, then,

$$T_g \times 2\pi n = \text{Rotor output } (P_0)$$

or
$$\text{Gross torque } T_g = \frac{\text{Rotor output } (P_0)}{2\pi n} \tag{5.23}$$

Since the copper losses in the rotor is negligible, so the input of the rotor equals the output of the rotor.

$$\therefore \quad T_g = \frac{\text{Rotor input } (P_{ag})}{2\pi n_s} \tag{5.24}$$

(n_s being the synchronous speed in rps)

From Eqs (5.23) and (5.24) we can write

$$\text{Rotor output } (P_o) = T_g \times 2\pi n$$

and
$$\text{Rotor input } (P_{ag}) = T_g \times 2\pi n_s$$

$\therefore$ Copper losses (ohmic loss) of rotor = Rotor input – Rotor output

$$= T_g \cdot 2\pi (n_s - n)$$

i.e. $P_{\text{rcu}} = T_g \cdot 2\pi \dfrac{(n_s - n)}{n_s}\ n_s = T_g \cdot 2\pi \cdot s \cdot n_s$ = Slip × Rotor input (P_{ag})

$$\therefore \quad P_{\text{rcu}} = s \times P_{ag} \tag{5.25}$$

when (P_{rcu}) is the *rotor copper loss*.

Hence gross mechanical power developed in rotor P_m is equal to (rotor input P_{ag} – rotor copper losses).

i.e., P_m = Rotor input – s × Rotor input = Rotor input $(1 - s)$

or, $$P_m = P_{ag}(1 - s) \tag{5.26}$$

Hence, rotor efficiency

$$\eta = \frac{\text{Output of rotor}}{\text{Rotor input}}$$

$$= (1 - s) = 1 - \left(\frac{n_s - n}{n_s}\right) = \frac{n}{n_s} = \frac{\text{Actual speed of rotor}}{\text{Synchronous speed of the motor}} \tag{5.27}$$

[The torque of a polyphase induction motor may be expressed in "Synchronous Watts". It is defined as the torque which develops a power of 1 W at the synchronous speed of the motor.
$\because$ Rotor input = $T_g \times 2\pi n_s$, hence we can write

$$T_g \text{ (synchronous W)} = \frac{\text{Rotor input in W}}{2\pi \times n_s},$$

where n_s is expressed in rps.]

Also, copper losses of rotor (P_{rcu}) = s × Rotor input (P_{ag})

$$\text{or} \quad P_{\text{rcu}} = s \times \frac{\text{Mechanical power in rotor } (P_m)}{(1 - s)}$$

$$= \left(\frac{s}{1 - s}\right) \times \text{Mechanical power developed in rotor } (P_m) \tag{5.28}$$

$\therefore$ Rotor input : rotor copper loss : mechanical power developed in rotor = 1 : s : $(1 - s)$.

It may be noted here that T or T_g (developed torque/gross torque/electromagnetic torque) can thus be obtained from the following formula:

T ($=T_g$) = $\dfrac{P_{ag}}{\omega_s}$ Nm, where $\omega_s = 2\pi n_s$ and (P_{ag}) is the *air gap power of the motor*, i.e. the power being transferred from the stator to rotor. We have termed it as rotor input earlier where *rotor input* (= air gap power) = (stator input – stator copper loss – stator core loss).

The *shaft output torque* T_{sh} is developed at the output of the motor (i.e., at the shaft) and is due to the output power which is the difference between the air gap power (or rotor input) and the rotor losses. Rotor losses include rotor copper loss and mechanical losses (we neglect the rotor iron loss). Thus the shaft torque is obtained as

$$T_{sh} = \frac{P_0}{\omega} \text{ Nm},$$

where P_o is the motor output and (ω) is $2\pi n$, n_s and n are both expressed in rps, i.e. $n_s = \frac{N_s}{60}$ rps ; $n = \frac{N}{60}$ rps, where N_s and N are expressed in rpm.

The gross mechanical power developed in the rotor being the difference of rotor input P_{ag} and the rotor copper loss P_{rcu}, we can find the gross mechanical torque developed using the relation, $T_m = (P_m/\omega)$ Nm, where T_m is the *gross mechanical torque* developed in the rotor.

Thus finally we have

- P_{rcu} (rotor copper loss in watts) = $s \times P_{ag}$, where P_{ag} = air gap power (or rotor input) in watts = P_{in} – stator losses.

  [P_{in} (= stator input) = ($\sqrt{3}\, E_L\, I_L \cos \phi$) W and stator losses include stator copper loss and stator core loss]
- P_{rcu} (rotor copper loss in watts) = $\frac{s}{1-s} \times P_m$
- P_m (gross mechanical power developed in the rotor) = $P_{ag}(1 - s)$; P_m and P_{ag} both being expressed in watts.
- η (motor efficiency)% = $\frac{P_o}{P_{in}} \times 100 = \frac{n}{n_s} \times 100$:

  where P_o = motor output in HP converted to watts, n is the rotor speed in rps and n_s is the synchronous speed of the motor in rps.
- T (in Nm) (= T_g) = $\frac{P_{ag}}{\omega_s}$; $\omega_s = 2\pi n_s$.

  Also, $T = K \frac{sE_1^2 R_2}{R_2^2 + (sX_2)^2}$; $K = \frac{3}{\omega_s}$ when we desire to get three-phase torque; $K = \frac{1}{\omega_s}$ for single-phase expression.
- T_m (mechanical torque developed in rotor) = $\frac{P_m}{\omega}$ Nm; $\omega = 2\pi n$.
- $T_{sh} = \frac{P_o}{\omega}$ Nm

  [if rotational losses are neglected, $P_m = P_o$ and hence $T_m = T_{sh}$]

  [$P_{ag} = P_{in} - (P_{scu} + P_{sc})$; $P_m = P_{ag} - P_{rcu}$; $P_o = P_m - P_{rm}$ where, P_{scu} and P_{sc} are the stator copper loss and stator core loss respectively and P_{rm} in the rotor mechanical loss in watts.]

Let us now extend the discussion to review the aspect of loss in an induction motor.

Fixed loss = (Power input at no load) – (Stator Cu-loss at no load).

This loss can be obtained by performing no load test of the induction motor. Total ohmic losses under variable loss can be obtained using blocked rotor test of induction motor. It should be noted that the brush contact loss for wound rotor induction motor (WRIM) = slip ring current times volt drop in brushes.

Stray load loss occurs in iron and conductors. It is very difficult to measure stray load loss. To account this, the efficiency η is taken as 0.5% less than the calculated value on full load and for other loads.

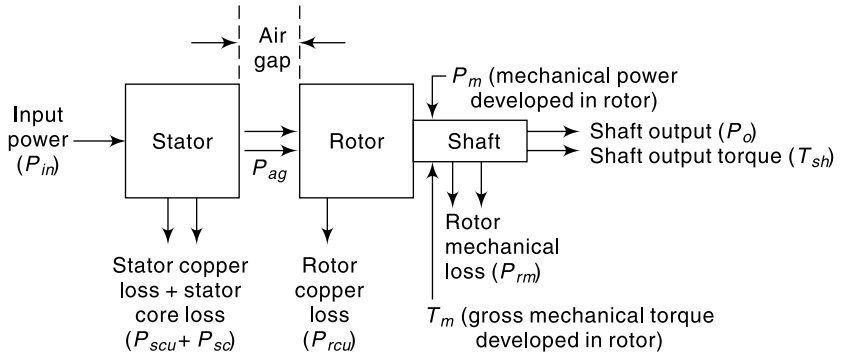


Fig. 5.6 ***Power stages in a three-phase induction motor***

The efficiency η of a three-phase induction motor is given by

$$\eta_{\%} = \frac{P_o}{P_o + P_{fl} + P_{cu}} \times 100 \tag{5.29}$$

where P_o is the output power, P_{fl} is fixed loss, and P_{cu} is stator and rotor ohomic losses plus brush contact loss.

[Also, Stator input = Stator output + Stator losses.

But the stator output is entirely transferred inductively to the rotor circuit, so Rotor input = Stator output; also Rotor output = Rotor input – Rotor copper losses].

Expression of Torque from Power Input

The rotor input also being termed as air gap power P_{ag} in an induction motor, we can write from Eq. (5.25),

$$\text{Rotor input } P_{\text{ag}} = \frac{\text{rotor copper loss}}{s} = \frac{I_2'^2 R_2'}{s} \tag{5.30a}$$

[when all the quantities are referred to the stator side]

i.e. $$P_{\text{ag}} = \frac{s^2 E_2'^2}{R_2'^2 + (sX_2')^2} \cdot \frac{R_2'}{s} \qquad \left[\because I_2' = \frac{sE_2'}{[R_2'^2 + (sX_2')^2]^{0.5}}\right]$$

$$= \frac{sE_2'^2 R_2 \times k^2}{(k^2 R_2)^2 + (s \cdot k^2 X_2)^2} \qquad [\because R_2' = k^2 R_2;\ X_2' = k^2 \cdot X_2]$$

But $$E_2' = kE_2$$

$\therefore$ $$P_{\text{ag}} = \frac{sE_2^2 R_2 \cdot k^4}{k^4 [R_2^2 + (sX_2)^2]} = \frac{sE_2^2 R_2}{R_2^2 + (sX_2)^2}$$

Now we refer to the approximate equivalent circuit of Fig. 5.5(b). We observe that if $R_s = 0$; $X_s = 0$ (i.e., we neglect stator resistance and reactance) then E_2' becomes equal to E_1, the applied voltage per phase. With this simplification we can write for the expression of P_{ag} (derived above) as follows:

$$P_{\text{ag}} = \frac{sE_1^2 R_2}{R_2^2 + (sX_2)^2}$$

$$\therefore \quad \text{Torque } T = \frac{P_{ag}}{\omega_s} = \frac{1}{\omega_s} \cdot \frac{sE_1^2 R_2}{R_2^2 + (sX_2)^2} \text{ (where } \omega_s = 2\pi n_s) \tag{5.30b}$$

If we compare Eq. (5.13) with Eq. (5.30b), we find K in Eq. (5.13) is $\left(\frac{1}{\omega_s}\right)$.

With $K = \frac{1}{\omega_s}$, T gives the expression of electromagnetic torque developed in the rotor on per phase basis and is expressed in Nm.

For three-phase, the expression of torque is $T = \frac{3}{\omega_s} \cdot \frac{sE_1^2 R_2}{R_2^2 + (sX_2)^2}$ Nm. (5.30c)

5.13 DETERMINATION OF MOTOR EFFICIENCY

The efficiency of small induction motors can be determined by directly loading them and by measuring their input and output powers. For larger motors, it may be difficult to arrange loads for them. Moreover, the power loss will be large with direct loading tests. Therefore, indirect methods are used to determine the efficienty of a three-phase induction motors. The following tests are performed on the motor:

(a) No-load test (or open circuit test).
(b) Blocked-rotor test.

The parameters of the equivalent circuit can be found from the no-load and blocked rotor test also.

Open Circuit or No-load Test

This test is similar to the open circuit test on a transformer. A three-phase auto-transformer is used to supply rated voltage at the rated frequency. The motor is run at no load. The power input is measured by two wattmeter method. The power factor under no load condition is generally less than 0.5. Therefore one of the wattmeters will show negative reading. It is, therefore, necessary to reverse the direction of current coil terminals to take the reading.

Let W_o, i.e. the wattmeter reading be equal to the sum of stator core losses and mechanical losses. Let V_o and I_o be the per phase values of voltage and current.

Then no load power factor is

$$\cos \theta_o = \frac{W_o}{3 V_o I_o}$$

However $I_C = I_o \cos \theta_o$

and $I_\phi = I_o \sin \theta_o$

$$\therefore \quad R_o = \frac{V_o}{I_c} = \frac{V_o}{I_o \cos \theta_o} \tag{5.31a}$$

$$X_o = \frac{V_o}{I_\phi} = \frac{V_o}{I_o \sin \theta_o} \tag{5.31b}$$

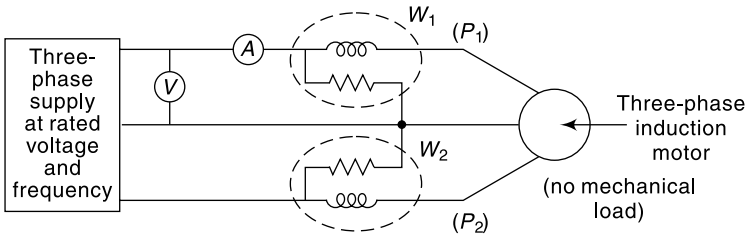


Fig. 5.7(a) *Circuit diagram for no-load test on a three-phase induction motor*

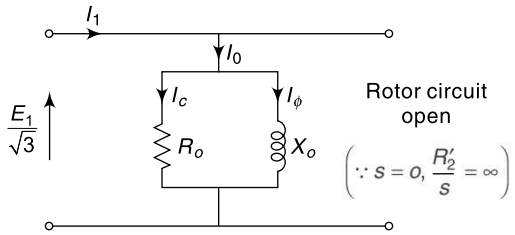


Fig. 5.7(b) *Equivalent circuit at no load*

Blocked Rotor Test The circuit is the same as shown in Fig. 5.8. The motion of the rotor is blocked by a brake (or a belt). This test is analogous to the short-circuit test of a transformer because the rotor winding is short-circuited through slip rings and in cage motors, the rotor bars are permanently short circuited. Only a reduced voltage needs to be applied to the stator at rated frequency. This voltage should be such that the ammeter reads rated current of the motor.

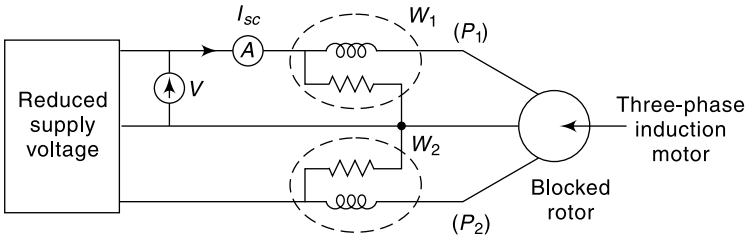


Fig. 5.8(a) *Circuit diagram for blocked rotor test*

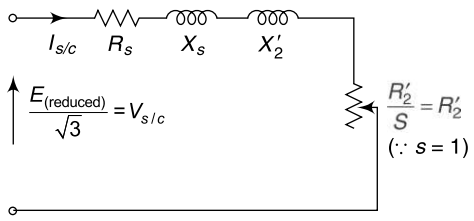


Fig. 5.8(b) *Equivalent circuit during blocked-rotor test*

The total power input on short circuit $W_{s/c}$ is equal to the algebraic sum of the two wattmeter readings, i.e. equals the copper losses of the stator and rotor. Let $V_{s/c}$ and $I_{s/c}$ be the voltage and current per phase; then the power factor under blocked rotor condition is

$$\cos\ \theta_{s/c} = \frac{W_{s/c}}{3(V_{s/c})(I_{s/c})}\ \text{[neglecting the core and mechanical losses].}$$

Since in a R-L circuit, $R = Z \cos\ \theta$ and $X = Z \sin\ \theta$, here we can write

$$(R_s + R_2') = \left(\frac{V_{s/c}}{I_{s/c}}\right)\cos\ \theta_{s/c} \tag{5.32a}$$

$$(X_s + X_2') = \left(\frac{V_{s/c}}{I_{s/c}}\right)\sin\ \theta_{s/c} \tag{5.32b}$$

The stator resistance R_s is measured separately by using a battery, ammeter and a voltmeter. Then R_2' can be found from equation 5.32(a). The reactances (X_s) and (X_2') are generally assumed equal.

5.18 A three-phase, 5 HP, 400 V, 50 Hz induction motor is working at full load with an efficiency of 90% at a power factor of 0.8 lagging.
Calculate: (i) the input power and (ii) the line current.

Solution

Rating of the motor = 5 HP = 5 × 735.5 = 3677.50 watt; V = 400 V (line value); f = 50 Hz; full-load efficiency = 90% (= 0.9) and p.f = 0.8 (lagging)

(i) $\because$ Efficiency $\eta = \dfrac{\text{Output}}{\text{Input}}$,

$\therefore$ Input power $= \dfrac{\text{Output}}{\eta} = \dfrac{5 \times 735.5}{0.9} = 4.086$ kW

(ii) For a three-phase induction motor

Input power $= \sqrt{3}\, V_L\, I_L \cos\ \phi$

or $4086 = \sqrt{3} \times 400 \times I_L \times 0.8$

Hence the line current $(I_L) = \dfrac{4086}{\sqrt{3} \times 400 \times 0.8} = 7.37$ A.

5.19 A three-phase, 4-pole induction motor runs at a speed of 1440 rpm on 500 V, 50 Hz mains. The mechanical power developed by the rotor is 20.3 HP. The mechanical losses are 2.23 HP. Determine (i) the slip, (ii) the rotor copper losses (iii) the efficiency.

Solution

(i) $N_s = \dfrac{120 \cdot f}{P} = \dfrac{120 \times 50}{4} = 1500$ rpm

$\therefore$ Slip $= \dfrac{N_s - N}{N_s} = \dfrac{1500 - 1440}{1500} = 0.04$ or 4%.

(ii) Mechanical power developed in rotor = Power output + rotor losses = 20.3 + 2.23 = 22.53 HP = 22.53 × 735.5 = 16.571 kW

$\therefore$ Power transferred from stator to rotor $(P_{ag}) = \dfrac{16571}{(1-s)} = \dfrac{16571}{(1-0.04)} = 17261.46$ W

$\therefore$ Rotor copper losses = 17261.46 – 16571.00 = 690.46 W.

(iii) Efficiency $(\eta) = \dfrac{\text{Output}}{\text{Input}} = \dfrac{20.3 \times 735.5}{17261.46} = 0.865 = 86.5\%$.

5.20 The full-load slip of a 500 HP, 50 Hz three-phase induction motor is 0.03. The rotor winding has a resistance of 0.30 Ω/phase. Determine the slip and the power output, if external resistance of 2 ohms is inserted in each rotor phase. Assume that the torque remains same.

Solution

(i) $R_2 = 0.3\ \Omega,\ R_2' = 2 + 0.3 = 2.3\ \Omega,\ s = 0.03$

$$\therefore \quad \text{Slip} \quad s' = \frac{R_2' \cdot s}{R_2} = \frac{2.3 \times 0.03}{0.3} = 0.23$$

(ii) Let N_s be the synchronous speed, then

$$N = N_s\ (1 - 0.03) = 0.97\ N_s$$

and $N' = N_s\ (1 - 0.23) = 0.77\ N_s$ [N' is the new speed when external resistance of 2 ohm is inserted in each rotor phase]

Since the torque remains same, output is directly proportional to speed.

$$\therefore \text{ New motor output} = 500 \times \frac{0.77\ N_s}{0.97\ N_s} = 397 \text{ HP}.$$

5.21 A three-phase, 50 Hz, 4-pole induction motor has a star connected wound rotor. The rotor emf is 50 V between the slip rings at standstill. The rotor resistance and standstill reactance are 0.4 Ω and 2.0 Ω respectively. Calculate

(i) the rotor current per phase at starting with slip rings short circuited,
(ii) the rotor current per phase at starting if 50 Ω per phase resistance is connected between slip rings,
(iii) the rotor emf when the motor is running at full load at 1440 rpm,
(iv) the rotor current at full load, and
(v) rotor power factor (p.f.) at full load.

Solution

$$N_s = \frac{120 \times 50}{4} = 1500 \text{ rpm}.$$

(i) $E_2 = \dfrac{50}{\sqrt{3}} = 28.867$ V.

At standstill with slip rings short circuited

$$I_2 = \frac{E_2}{(R_2^2 + X_2^2)^{0.5}} = \frac{28.867}{\{(0.4)^2 + 2^2\}^{0.5}} = 14.15 \text{ A}.$$

(ii) The total resistance in the rotor circuit is 5.4 ohm per phase.

$$\therefore \quad I_2 = \frac{28.867}{\{(5.4)^2 + 2^2\}^{0.5}} = 5.01 \text{ A}.$$

(iii) Full load slip $= \dfrac{1500 - 1440}{1500} = 0.04$

$\therefore$ Rotor emf $= 28.867 \times 0.04 = 1.55$ V/Ph.

(iv) $I_2 = \dfrac{sE_2}{[R_2^2 + (sX_2)^2]^{0.5}} = \dfrac{1.155}{[0.4^2 + (0.04 \times 2)^2]^{0.5}} = 2.82$ A.

(v) Rotor power factor (full load) $= \dfrac{R_2}{Z_2} = \dfrac{0.4}{[0.4^2 + (0.04\ X_2)^2]^{0.5}} = 0.98$ (lagging).

5.22 A three-phase, 4-pole, 50 Hz induction motor supplies a useful torque of 160 N-m at 4% slip. Determine: (i) rotor input, (ii) motor input, (iii) efficiency. Friction and windage losses are 500 W and stator loss is 1000 W.

Solution

(i) Motor speed, $N = N_s(1 - s) = \dfrac{120\,f\,(1-s)}{P} = \dfrac{120\times 50\,(1-0.04)}{4} = 1440$ rpm.

Gross power developed in rotor of motor

$$(P_m) = \frac{T_{\text{shaft}} \times 2\pi N}{60} + \text{friction} + \text{windage losses.}$$

or, $$(P_m) = \frac{160\times 2\pi \times 1440}{60} + 500 = 24615 \text{ W.}$$

$$\therefore \text{ Rotor input } (P_g) = \frac{P_m}{(1-s)} = \frac{24615}{(1-0.04)} = 25640 \text{ W.}$$

(ii) Motor input (P_{in}) = Rotor input (P_{ag}) + stator losses = 25640 + 1000 = 26640 W

(iii) Efficiency $(\eta) = \dfrac{\text{Net motor output } (P_o)}{\text{Motor input } (P_{\text{in}})} = \dfrac{24615 - 500}{26640} = 0.9052 = 90.52\%$

5.23 A three-phase, 50 Hz, 4-pole induction motor has a slip of 4%. Determine (i) speed of the motor, (ii) frequency of rotor emf. (iii) if rotor has a resistance of 1 Ω and standstill reactance of 4 Ω, calculate power factor (a) at stand still and (b) at speed of 1400 rpm.

Solution

(i) $N_s = \dfrac{120\,f}{P} = \dfrac{120\times 50}{4} = 1500$ rpm.

Now, slip $(s) = 0.04 = (N_s - N)/N_s = \dfrac{(1500 - N)}{1500}$

$\therefore$ Speed of motor, $N = 1440$ rpm.

(ii) Frequency of rotor emf, $f_2 (= sf_1) = 0.04 \times 50 = 2$ Hz = 120 rpm.

(iii) (a) at standstill, $N = 0$, so $s = 1$

$\therefore$ Rotor reactance $= 4 \times s = 4 \times 1 = 4\ \Omega$

$\therefore$ Rotor impedance $= (1 + j4)$ ohm $= 4.123 \angle 75.96°\ \Omega$ and p.f. $(\cos \phi)$ $= \cos 75.96° = 0.243$ (lag).

[Rotor resistance is independent of slip and hence $R_2 = 1\ \Omega$]

(b) Slip at 1400 rpm speed is given by

$s' = (1500 - 1400)/1500 = 0.067.$

$\therefore$ Rotor impedance $(Z') = 1 + j\,(4 \times 0.067) = (1 + j0.268)\ \Omega$

and $$\text{p.f } (\cos \phi) = \frac{1}{\{1^2 + (0.268)^2\}^{0.5}} = 0.966 \text{ lag.}$$

5.24 The power input to a 6-pole, three-phase, 50 Hz induction motor is 40 kW. Stator loss is 1 kW. Friction and windage loss = 0.2 kW. Speed is 960 RPM. Calculate (i) the slip, (ii) the BHP (iii) the rotor copper loss, and (iv) the efficiency η.

Solution

(i) $N_s = \dfrac{120\,f}{P} = \dfrac{120\times 50}{6} = 1000$ rpm

$\therefore$ Slip $(s) = \dfrac{N_s - N}{N_s} = \dfrac{1000 - 960}{1000} = 4\%$.

(ii) BHP (Brake Horse Power) $= \dfrac{40}{0.7355} = 54.38$ BHP. [$\because$ 1 HP = 735.5 W]

(iii) Motor input = 40 kW, stator loss = 1 kW
$\therefore$ Rotor input = 39 kW.
Rotor copper loss = slip × rotor input = 0.04 × 39 = 1.56 kW.

(iv) Rotor gross output is $(1 - s) \times$ rotor input $= 39(1 - 0.04) = 37.44$ kW
$\therefore$ Rotor output power = (37.44 – 0.2) kW = 37.24 kW.
$\therefore$ Motor efficiency $(\eta) = \dfrac{37.24}{40} \times 100$
i.e., $\eta = 93\%$ (app.).

5.25 A 18.65 kW, 4-pole, 50 Hz, three-phase induction motor has friction and windage losses of 2.6% of the output and full load slip is 4.2%. Find out (i) the rotor copper loss, (ii) the rotor input, (iii) the output torque and (iv) the gross mechanical torque developed in the rotor.

Solution

Motor output = 18650 W, friction and windage losses $= \dfrac{2.6}{100} \times 18650 = 484.9$ W.

$\therefore$ Rotor gross power developed = 18650 + 484.9 = 19134.9 W $(=P_m)$

(i) Rotor copper loss = Rotor gross power developed $\times \left(\dfrac{s}{1-s}\right)$
$= 19134.9 \times 0.042/(1 - 0.042) = 838.89.$

(ii) Rotor input $P_{ag} = \dfrac{\text{Rotor copper loss}}{\text{slip}} = \dfrac{838.89}{0.042} = 19973.5$ W.
[Alternatively: Rotor input = 19134.9 + 838.89 = 19973.79 W]

(iii) $N_s = \dfrac{120\,f}{P} = \dfrac{120 \times 50}{4} = 1500$ rpm
$N = N_s(1 - s) = 1500(1 - 0.042) = 1437$ rpm.
Shaft torque, $T_{sh} = \dfrac{\text{output in watts}}{(2\pi N/60)} = \dfrac{(18650 \times 60)}{2\pi \times 1437} = 123.9$ Nm

(iv) Gross mechanical torque T_m
$= \dfrac{\text{Gross mechanical power developed in rotor in watts}}{(2\pi N/60)} = \dfrac{(19134.9 \times 60)}{2\pi \times 1437} = 127.2$ Nm.

5.26 A three-phase, 50 Hz, 6-pole induction motor runs at 950 rpm and delivers 8 kW output. What starting torque will the motor develop when switched directly onto the supply if maximum torque is developed at 800 rpm, the friction and windage losses being total of 840 W.

Solution

$$\text{Slip } s = \frac{N_s - N}{N_s} = \frac{1000 - 950}{1000} = 0.05$$

$$s_{max} = \frac{N_s - N_{max}}{N_s} = \frac{1000 - 800}{1000} = 0.2$$

$\therefore$ Motor shaft power (P_{md}) = 8000 + 840 = 8840 W.

We know $P_{md} = 2\pi NT$

$\therefore$ Torque $(T) = \dfrac{8840 \times 60}{2\pi \times 950} = 88.90$ Nm

Also, $T_{st} = \dfrac{s^2 + s_{max}^2}{s(1 + s_{max}^2)} \cdot T$

Here, $T_{st} = \dfrac{(0.05)^2 + (0.2)^2}{0.05\{1 + (0.2)^2\}} \times 88.9 = 72.65$ Nm.

5.27 A three-phase, 440 V, 50 Hz. 6-pole induction motor running at 950 rpm takes 50 kW at a certain load. The friction and windage loss is 1.5 kW and stator losses = 1.2 kW. Determine (i) the slip (ii) the rotor copper loss (iii) the output from the rotor and (iv) efficiency.

Solution

(i) Slip $= \dfrac{N_s - N}{N_s} = \dfrac{1000 - 950}{1000} = 0.05.$

$\left(\text{as } N_s = \dfrac{50 \times 120}{6} = 1000 \text{ rpm}\right).$

(ii) Rotor copper loss = slip × rotor input = 0.05 × 48.8 kW = 2.44 kW.
[rotor input = input – stator loss = 50 – 1.2 = 48.8 kW]

(iii) Rotor output = Rotor input – Rotor copper loss – Friction and windage loss
= 48.8 – 2.44 – 1.5 = 44.86 kW.

(iv) Efficiency $(\eta) = \dfrac{\text{motor output}}{\text{motor input}} \times 100 = \dfrac{44.86}{50} \times 100 = 0.897 = 89.7\%.$

5.28 A three-phase, 415 V, 50 Hz star connected 4-pole induction motor has stator impedance $Z_1 = (0.2 + j0.5)\ \Omega$ and rotor impedance referred to stator side is $Z_2 = (0.1 + j0.5)\ \Omega$ per phase. The magnetizing reactance is 10 Ω and resistance representing core loss is 50 Ω on per phase basis.

Determine (i) the stator current (ii) the stator power factor (iii) the rotor current. Consider slip as 0.04.

Solution

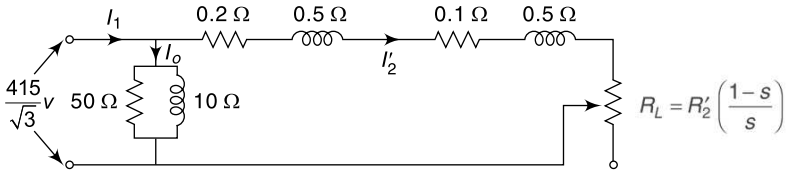


Fig. 5.9 ***Circuit diagram of Ex. 5.28***

Let Z be the total impedance of the circuit (Fig. 5.9).

Load resistance $R_L = R_2'\left(\dfrac{1-s}{s}\right) = 0.1\left(\dfrac{1 - 0.04}{0.04}\right) = 2.4\ \Omega.$

$\therefore$ Total resistance $R_{1e} = 2.4 + 0.2 + 0.1 = 2.7\ \Omega$

and total reactance $X_1 = 0.5 + 0.5 = 1\ \Omega$

Impedance $Z_1 = \sqrt{(2.7)^2 + 1} = \sqrt{8.29} = 2.88\ \Omega$.

Angle of Z_1 is $\tan^{-1}$ is (1/2.7) i.e., 20.323° (lag.)

Given, $V_L = 415$ V.

$$\therefore \quad V_{\text{phase}} = \frac{415}{\sqrt{3}} = 240 \text{ V}$$

$$\therefore \quad I_2' = \frac{V_{\text{ph}}}{Z_1} = \frac{240 \angle 0°}{2.88 \angle 20.323°} = 83.36 \angle -20.323° \text{ A}$$

i.e., rotor current (referred to stator) = 83.36 A (Ans. of (iii))

[Also, $I_2' = 83.36 \angle -20.323$

$\therefore$ $= (78.17 - j28.95)$ A]

$\because$ $I_0 = I_C + I_\phi$,

and $I_C = I_0 \cos \phi_0$, we have, $I_C = \frac{240}{50} = 4.8$ A

and $I_\phi = I_0 \sin \phi_0 = \frac{240}{10} = 24$ A

$\therefore$ $I_0 = (4.8 - j24)$ A

Thus, $I_1 = I_0 + I_2' = (4.8 - j24) + (78.17 - j28.95) = (82.97 - j52.95)$ A

$\therefore$ $|I_1| = \sqrt{(82.97)^2 + (52.95)^2} = 98.44$ A (Ans. of (i))

Again, $\tan \phi_1 = \frac{52.95}{82.97} = 0.63818$

or, $\phi_1 = 32.545°$.

i.e., $\cos \phi_1 = \cos (32.545°) = 0.843$ (lagging) (Ans. of (ii))

5.29 A 20 Hp three-phase, 400 V star connected induction motor gave the following test results:

DC test with the stator windings of two phases in series: 21 V, 30 A.

No load test: Applied voltage 400 V line, line current 8 A, wattmeter reading (2360) W and (–1160) W.

Short circuit test: Applied voltage 140 V, line current 33 A, wattmeter reading 2820 W and –370 W.

Determine the parameters of the equivalent circuit. Assume $X_1 = X_2'$.

Solution

Since two phases of stator windings are in series in the dc test, we have

$$2R_1 = \frac{21}{30} = 0.70\ \Omega$$

or $R_1 = 0.35\ \Omega$.

No load test:

$$V_o = \frac{400}{\sqrt{3}} = 230.95 \text{ V} ; I_o = 8 \text{ A}.$$

$$W_o = (W_{10} + W_{20}) = 2360 - 1160 = 1200 \text{ W}.$$

$$\therefore \quad \cos \theta_o = \frac{1200}{3 \times 230.95 \times 8} = 0.216$$

$$R_o = \frac{V_o}{I_o \cos \theta_o} = \frac{230.95}{8 \times 0.216} = 133.65\ \Omega.$$

$$X_o = \frac{V_o}{I_o \sin \theta_o} = \frac{230.95}{8 \times 0.976} = 29.57 \text{ W.}$$

Short circuit test:

$$V_{sc} = \frac{140}{\sqrt{3}} = 80.83 \text{ V}$$

$$I_{sc} = 33 \text{ Amps; } W_{sc} = 2450 \text{ W}$$

$$\therefore \quad \cos \theta_{sc} = \frac{2450}{3 \times 80.83 \times 33} = 0.306$$

$$\therefore \quad R_1 + R_2' = \frac{V_{sc}}{I_{sc}} \cdot \cos \theta_{sc} = \frac{80.83}{33} \times 0.306 = 0.745 \ \Omega$$

$$\text{and} \quad X_1 + X_2' = \frac{V_{sc}}{I_{sc}} \cdot \sin \theta_{sc} = \frac{80.83}{33} \times \sin \theta_{sc} = \frac{80.83}{33} \times 0.9518 = 2.33 \ \Omega$$

$$\therefore \quad X_1 = X_2' = 0.5 \times 2.33 \quad 1.666 \ \Omega.$$

$$\text{and} \quad R_2' = 0.745 - 0.35 = 0.395 \ \Omega.$$

Hence we can write

$$R_0 = 133.65 \ \Omega$$
$$X_0 = 29.57 \ \Omega$$
$$R_1 = 0.35 \ \Omega$$
$$R_2' = 0.395 \ \Omega$$
$$X_1 = X_2' = 1.166 \ \Omega.$$

5.30 A three-phase, 50 Hz, 500 V induction motor develops 20 BHP at a slip of 4%. The mechanical losses are 1 HP. Calculate the efficiency η, if the stator loss is 1000 W.

Solution

Here $V_L = 500$ V, $f = 50$ Hz, $s = 4\% = 0.04$

Given, BHP = 20, stator losses = 1000 W,

Mechanical loss = 1 HP = 735.5 W

Power output = 20 BHP = 20×735.5 W = 14710 W = Rotor net output.

$\therefore$ Rotor gross mechanical power developed = Rotor net output + Mechanical loss

= 14710 + 735.5 = 15445.5 W.

$$\text{Hence, Rotor input} = \frac{\text{Rotor gross mechanical power developed}}{(1 - s)} = \frac{15445.5}{1 - 0.04} = 16089.06 \text{ W}$$

$\therefore$ Stator input = rotor input + stator losses = 16089.06 + 1000 = 17089.06 W.

5.31 A three-phase, 6-pole induction motor develops 30 HP including 2 HP mechanical losses at a speed of 960 rpm from 550 V, 50 Hz mains. The power factor is 0.9 lagging. Determine (i) the slip (ii) the rotor copper loss (iii) the total input, if stator losses are 2 kW (iv) the efficiency and (v) the line current.

Solution

Here $P = 6$, $N = 960$ rpm, $f = 50$ Hz,

$V_L = 550$ V, p.f = $\cos \phi = 0.90$

(i) $N_s = \frac{120 f}{P} = \frac{120 \times 50}{6} = 1000$ rpm

Slip $s = \dfrac{N_s - N}{N_s} = \dfrac{1000 - 960}{1000} = 0.04 = 4\%$.

(ii) Power transferred from stator to rotor $(P_{ag}) = \dfrac{30 \times 735.5}{1 - s} = \dfrac{30 \times 735.5}{(1 - 0.04)} = 22984.4$ W

$\therefore$ Rotor copper loss = $(22984.4 - 28 \times 735.5) = 2390.4$ W.

(iii) Total input = $(30 \times 735.5 + 2000) = 24{,}065$ W.

(iv) Efficiency = $\dfrac{30 \times 735.5}{22984.4} = 0.96 = 96\%$.

(v) Line current $(I_L) = \dfrac{\text{Input}}{\sqrt{3}\, V_L \cos\phi} = \dfrac{24065}{\sqrt{3} \times 550 \times 0.9} = \dfrac{24065}{857.365} = 28.06$ A.

5.14 STARTING OF THREE-PHASE INDUCTION MOTORS

A three-phase induction motor has a definite positive starting torque. When switched on to supply it starts itself but draws a high starting current. This is evident from the equivalent circuit. At the time of starting, slip $s = 1$ and hence the resistance $\left[\dfrac{R_2\,(1 - s)}{s}\right]$ becomes zero (The motor behaves as a short circuited transformer). The current in the rotor and the stator windings may be about five times more than full load values.

These high rotor and stator currents cause many problems:

(a) High electromagnetic forces between the conductors on the same part.
(b) High heat generation causing high temperature may damage the insulation.
(c) High current (at low power factor) may cause an appreciable drop in supply voltage causing undesirable effects on other equipments.

Therefore suitable means must be provided with the motor at start, to limit the starting current upto safe value.

The device which is used to start the three-phase induction motor is termed as starter. The function of the starter is to limit the initial rush of current to a predetermined safe value.

The various methods of starting the three-phase induction motor are:

1. By *Direct On Line (DOL) starter*
2. By *Star-delta starter*
3. By *Auto-transformer starter*

Direct On Line Starting (DOL)

For small size squirrel cage (less than 2 HP) motor or for motors in power system where inrush of high-starting current is permissible, direct start may be used. For these small motors, the starting torque is about twice the full-load torque and the starting period lasts only a few seconds.

Figure 5.10 shows a starter for direct starting with in-built short circuit, overload and under voltage protection. When the motor is to be started, the main switch is put on and start button is pressed. This energises the relay coil S causing the normally open contacts S_1, S_2, S_3 to close. Power is supplied to the motor and

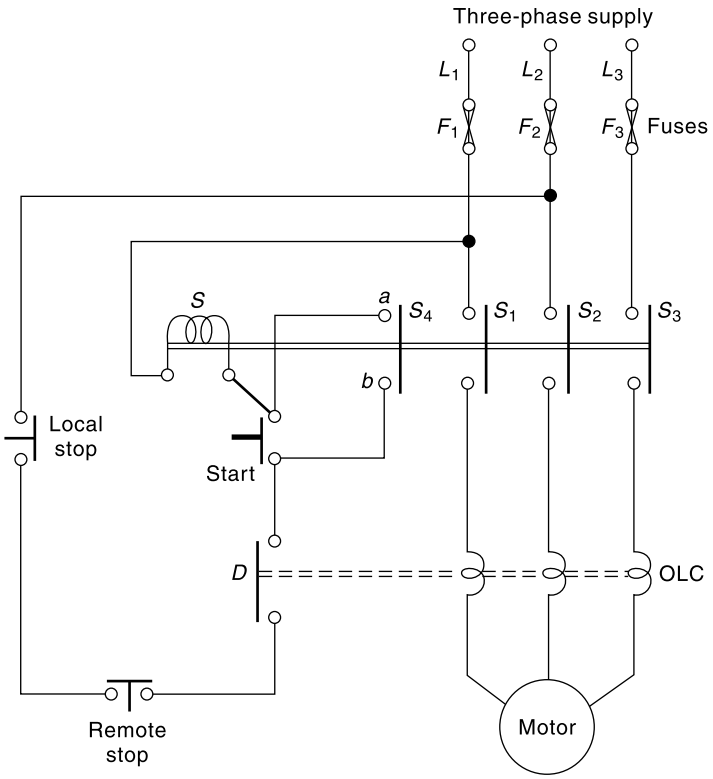


Fig. 5.10 ***Direct on-line starter***

it starts. The contact S_4 also shuts, thus shorting out the starting switch allowing the operator to release it without removing power from the S relay. When the stop button is pressed, the S relay is de-energised and the S contacts open, thus stopping the motor. Short circuit protection is provided by fuses F_1, F_2 and F_3. Thermal overload relay (OLC) protects the motor from sustained overloads opening the contact D.

Star-Delta Starter

Figure 5.11 shows the diagram of the star-delta starter. Star-delta starter can be used only for those three-phase induction motors whose stator winding has been designed for delta connection. All the six terminals (of the three phases) are brought out. For starting, the phases are connected in star thereby reducing the voltage of each phase to $\frac{1}{\sqrt{3}}$ of its normal value.

[From equation (5.30a), we have

$$P_{ag} = \frac{I_2'^{\,2} R_2'}{s}$$

$$\therefore \quad T = \frac{P_{ag}}{\omega_s} = \frac{1}{\omega_s} \cdot I_2'^{\,2} R_2' \times \frac{1}{s}$$

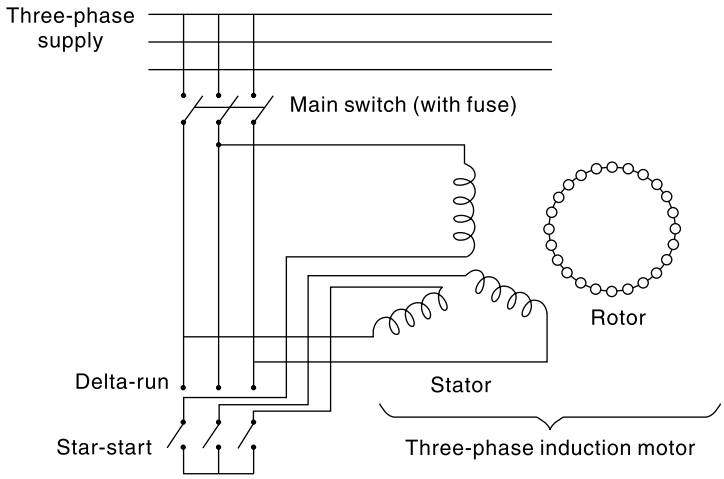


Fig. 5.11 ***Star-delta starter***

At $s = 1$ (i.e., at starting),

$$T_s = \frac{1}{\omega_s} I_2''^2 \times R_2' \quad [I_2'' \text{ is the rotor current reflected at primary at starting}]$$

$$\therefore \quad \frac{T_s}{T} = \frac{I_2''^2}{I_2'^2} \cdot s$$

If T represents full load torque, I_2' the full load rotor current reflected to primary, we have $I_{fl} = I_2'$, neglecting the magnetizing branch current. Similarly I_2'' represents the starting current (I_s) at stator, the magnetizing branch being neglected.

$$\therefore \quad \text{We have } \frac{T_s}{T} = \left(\frac{I_s}{I_{fl}}\right)^2 \times s_{fl} \tag{5.33}$$

The starting line current of the motor with star-delta starter is thus also reduced to $\frac{1}{\sqrt{3}}$ full voltage starting line current. The starting torque which is proportional to $\left(\frac{E_1}{\sqrt{3}}\right)^2$ is reduced to 1/3 of the full load torque. Thus, for star delta start though we are able to reduce the starting current, we sacrifice the torque and the starting torque reduces to 1/3 of the full load torque.

Let us analyse the star delta starting method to find the torque. We assume that the motor first operates with star connection [Fig. 5.12(a)] and when speeds up it operates with delta connection of the stator [Fig. 5.12(b)].

In Fig. 5.12(a),

Starting line (phase) current ($I_{s(\text{star})}$) is given by

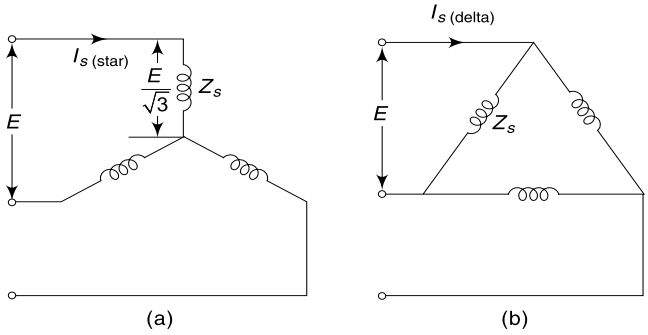


Fig. 5.12 ***Star-delta starting***

In Fig. 5.12(b),

Starting phase current $I_{P(\text{start})} = \dfrac{E}{Z_s}$

$\therefore$ Starting line current $I_{s(\text{delta})} = \sqrt{3}\, I_{P(\text{start})}$

$\therefore$ $$\frac{I_{s(\text{start})}}{I_{s(\text{delta})}} = \left(\frac{1}{\sqrt{3}} \cdot I_{P(\text{start})}\right) \div (\sqrt{3}\, I_{P(\text{start})}) = \frac{1}{3}.$$

Using relation (5.33) we can write $T_{s(\text{star})}/T_{\text{fl}} = \dfrac{1}{3}(I_{P(\text{start})}/I_{\text{fl}})^2 \times s_{\text{fl}}$. Thus starting torque is $\dfrac{1}{3}$ of that obtained in DOL starting.

This method is bit economical one but for motors rated beyond 3 KV, this method is not applicable. Like other three-phase motor starters, in this starter also overload coil and no-voltage coils are provided for the protection of the motor (not shown in the star-delta figure). An automatic star-delta starter can also be made by using push button, contactors, time delay relay (TDR), etc.

Auto-Transformer Starter (Fig. 5.13)

In this method reduced voltage is obtained by some fixed tappings on the three-phase auto transformer. Generally 60 to 65% tappings can be used to obtain a safe value of starting current. The full rated voltage is applied to the motor by taking the auto-transformer out of the motor circuit when motor has picked up the speed upto 85% of its normal speed. Figure 5.13 shows the circuit.

Let us assume that the input voltage E is reduced to xE using auto-transformer tappings.

$\therefore$ the motor starting currnet is, $I_s = xI$, where I is the motor starting current when full voltage E is applied. However, the current drawn from the supply $I_{s(\text{line})}$ is obtained from the relation

$$\frac{I_{s(\text{line})}}{I_{s(\text{motor})}} = x$$

$\therefore$ here we have $I_s(\text{line}) = x \cdot I_{s(\text{motor})} = x^2 I$.

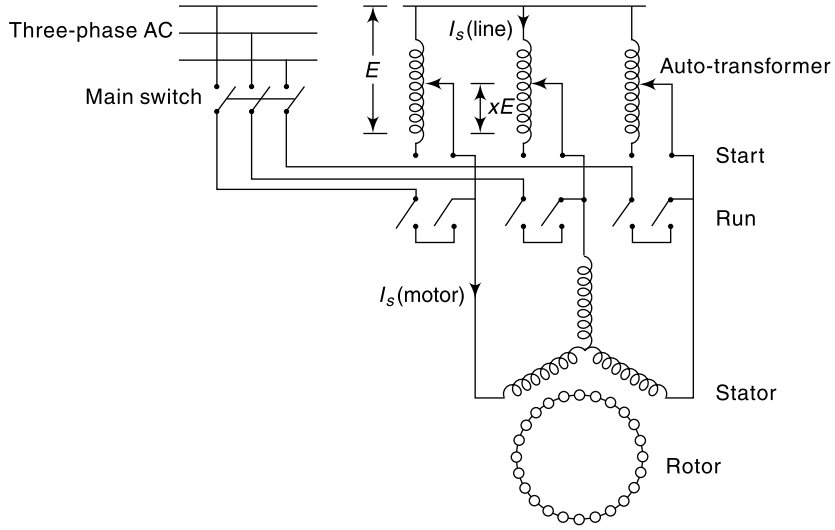


Fig. 5.13 ***Auto-transformer starter***

Hence from relation (5.33) we get

$$\frac{T_s}{T_{\text{fl}}} = x^2\left(\frac{I}{I_{\text{fl}}}\right)^2 \cdot s_{\text{fl}}$$

It is found that while the starting torque is reduced by x^2 of that of DOL start, starting line current is also reduced by same fraction.

5.15 COMPARISON AMONG DIRECT ON LINE STARTER, STAR DELTA STARTER AND AUTO-TRANSFORMER STARTER

DOL starter	*Star delta starter*	*Auto-transformer starter*
1. Full voltage is applied to the motor at the time of starting.	1. Each winding gets 58% of the rated line voltage at the time of starting.	1. The starting voltage can be adjusted according to the requirement.
2. The starting current is 5–6 times of the full load current.	2. The starting current is reduced to $\frac{1}{3}$ that of direct on line starting.	2. The starting current can be reduced as desired.
3. The three windings are connected generally in star.	3. The three windings are connected in star at the time of starting, and then in delta at the time of running.	3. The three windings are generally connected in delta.
4. Only three wires are to be brought out from the motor.	4. Six wires to be brought out from the motor.	4. Only three wires are to be brought out from the motor.

(*Contd*)

(*Contd*)

5. Easy to connect motor with direct on line.	5. Identification of three starting leads and three end leads is not so easy.	5. Input and output connections of the auto-transformers are to be made properly.
6. Very easy operation.	6. It is required that connections are first to be made in star, and then in delta either manually or automatically.	6. Skilled operator is needed for connection and starting.
7. Low cost.	7. More cost	7. High cost.
8. Less space required for installation.	8. More space required	8. More space required.
9. Used for motor up to 5 HP.	9. Up to 10 HP	9. Large motors.

5.16 SPEED CONTROL OF A THREE-PHASE INDUCTION MOTOR

The synchronous speed (N_s) of a three-phase induction motor is given by

$$N_s = \frac{N}{1-s} \text{ or } N = N_s\,(1-s) = \frac{120\,f}{P}\,(1-s)$$

The speed N of induction motor can be changed by the three basic methods.

(a) Frequency Control Changing the supply frequency f the speed can be varied directly proportional to the supply frequency of ac supply.

(b) Pole Changing Speed control can also be obtained by changing the number of poles P on the stator (as speed is inversely proportional to the number of poles). This change can be incorporated by changing the stator winding connections with a suitable switch. The change in the number of stator poles P changes the synchronous speed N_s of the rotating flux, thereby the speed of the motor also changes.

(c) By Changing the Slip This can be accomplished by introducing resistance in the rotor circuit, which causes an increase in slip, thereby bringing down the speed of the motor.

Change of Supply Frequency

If the frequency of the supply to the stator of an induction motor is changed its synchronous speed is changed depending on the frequency and hence provides a direct method of speed control. To keep the magnetization current within limits, the applied voltage must be reduced in direct proportion to the frequency. Otherwise the magnetic circuit will become saturated resulting in excessive magnetization current.

The starting torque at reduced frequency is not reduced in the same proportion, because rotor power factor improves with reduction in frequency. The torque

that can be produced by the maximum permissible rotor current is equal to that at rated conditions. Since power is the product of torque and speed, operation at reduced speed results in lesser permissible output.

This method of speed control is not a common method and hence this method would be used only as a special case.

In earlier days, the variable frequency was obtained from a motor generator set or mercury arc inverter. In recent days frequency control is used by SCR based inverters or by using IGBT inverters.

Pole Changing

If an induction motor is to run at different speeds, one way is to have different windings for the motor so that it will have different synchronous speeds and the running speeds. Another method is used with suitable connections for a change-over to double the number of poles. The principle of formation of consequent poles is used. The method of changing the number of poles is accomplished by producing two sections of coils for each phase which can be reversed with respect to the other section. It is important to note in this connection that slot angle (i.e. electrical degrees), phase spread, breadth factor and pitch factors will be different for the low and high speed connections. The three phases can be connected in star or delta, thus giving a number of connections. If 50% per pole pitch is used for a high speed connection, a full-pitch winding is obtained for low speed connection. The method of connecting coils of a four pole motor is shown in Fig. 5.14 for one phase and also change over connections to obtain eight poles for the same machine with the same winding.

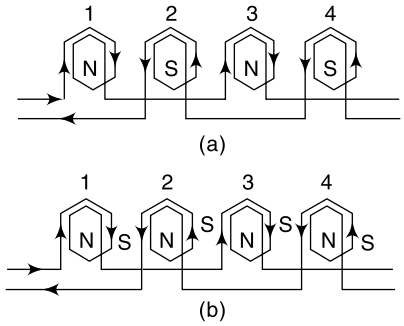


Fig. 5.14 ***Four-pole/eight-pole connections for one phase of induction motor***

The methods of speed control by pole changing are suitable for squirrel cage motors only because, a cage rotor has as many poles induced in it as there are in the stator and can thus adopt when the number of stator poles changes.

By Line Voltage Control

The torque developed by an induction motor is proportional to square of voltage. If the applied voltage to the motor is reduced, the torque is reduced and the slip is increased. Therefore, this method of speed control is applicable over a limited range only. This method is sometimes used on small motors driving fans, whose torque requirement is proportional to square of speed.

5.17 REVERSAL OF ROTATION

The direction of rotation of a three-phase induction motor can be reversed by reversing the direction of the rotation of the magnetic field. This can be done by interchanging the connections of any two of the three wires of the three-phase

power supply. This causes the currents in the phases to interchange their relative timings in going positive and negative with the result that the magnetic field produces reversal in direction of rotation.

5.32 A cage motor has a starting current of 40 A when switched on directly. Auto-transformer with 45% tapping is used.

Determine (i) starting current and (ii) ratio of starting torque with auto-transformer to the starting torque with direct switching.

Solution

The ratio of transformation (x) is 0.45

(a) $\therefore$ Starting current with auto-transformer = $(0.45)^2 \times 40 = 5.1$ A.

(b) $\dfrac{\text{Starting torque with auto-tranformer}}{\text{Starting torque with direct starting}} = (0.45)^2 = 0.2025.$

5.33 A three-phase, 10 kW, 6-pole, 50 Hz, 400 V of delta connected induction motor runs at 960 rpm on full load. If it draws 85 A on direct on line starting, calculate the ratio for the starting torque to full load torque with Y-Δ starter. Power factor and full load efficiency are 0.88 and 90% respectively.

Solution

Given: Output = 10 kW
No. of poles = 6
Frequency f = 50 Hz
N = 900 rpm
η = 90%
Full load p.f. = 0.88.

Full-load line current drawn by a three-plane Δ-connected induction motor is given as

$$(I_{\text{fl}}) = \frac{\text{Output in watt}}{\sqrt{3} \cdot V_L \times \text{P.f.} \times \text{efficiency}}$$

$$= \frac{10 \times 1000}{\sqrt{3} \times 400 \times 0.88 \times 0.9} = \frac{10000}{548.71} = 18.22 \text{ A}$$

Now, full-load current per phase (Δ-connection)

$$I_{\text{fl}} = \frac{18.22}{\sqrt{3}} = 10.52 \text{ A.}$$

On direct on line start the current I_{sc} drawn by the motor per phase is given as

$$I_{sc} = \frac{85}{\sqrt{3}} = 49.07 \text{ A}$$

Synchronous speed $(N_s) = \dfrac{120\,f}{P} = \dfrac{120 \times 50}{6} = 1000$ rpm

Full-load slip (s) $= \dfrac{N_s - N}{N_s} = \dfrac{1000 - 960}{1000} = 0.04$

$\because$ $$\frac{T_s}{T_{\text{fl}}} = \frac{1}{3}\left(\frac{I_{sc}}{I_{\text{fl}}}\right)^2 \times s_{\text{fl}}$$

$\therefore$ Here $$\frac{T_s}{T_{\text{fl}}} = \frac{1}{3}\left(\frac{49.07}{10.52}\right)^2 \times 0.04 = 0.290.$$

5.34 A three-phase delta connected cage type induction motor when connected directly to a 400 V, 50 Hz supply takes a starting current of 105 A in each stator phase. Find out

(i) the line current for DOL starting
(ii) line and phase starting currents for *Y*-Δ starting, and
(iii) line and phase starting currents for a 70% tapping on auto-transformer starting.

Solution

(i) Direct on line (DOL) starting current = $\sqrt{3} \times 105 = 181.86$ A

(ii) In *Y*-Δ starting, phase voltage on starting = $\frac{V_L}{\sqrt{3}} = \frac{400}{\sqrt{3}} = 230.9$ V

Since 400 V produce 150 A in phase winding, $\frac{400}{\sqrt{3}}$ will produce $\frac{105}{\sqrt{3}} = 60.62$ A

$\therefore$ Starting phase current = 60.62 A.

In *Y*-connection, line current = phase current

$\therefore$ Starting line current = 60.62 A.

(iii) In auto transformer start, with 70% tapping on auto-transformer, the line voltage across the Δ-connected motor = 0.7 × 400 V. For Δ-connection,

In Δ-connection, phase voltage = line voltage = 0.7 × 400 = 280 V. Since 400 V produces 105 A in phase winding. (0.7 × 400) V = 280 V produces 0.7 × 105 = 73.5 A.

Hence motor phase current is 73.5 A.

$\therefore$ Motor line current = $\sqrt{3} \times 73.5 = 127.30$ A.

But $\frac{\text{supply line current}}{\text{motor line current}} = \frac{\text{motor applied voltage}}{\text{supply voltage}} = 0.7$

$\therefore$ Supply line current = 0.7 × 127.30 = 89.11 A.

5.35 Calculate the suitable tapping on an auto-transformer starter for a three-phase induction motor required to start the motor with 50% of full-load torque. The short circuit current of the motor is 6 times the full load current and full-load slip is 0.035. Also calculate the current drawn from the main supply as a fraction of full-load current.

Solution

Starting torque = $x^2 \cdot \left(\frac{I_{sc}}{I_{fl}}\right)^2 \times$ slip at full load × torque at full load

or $0.5 \times$ Torque at full load = $x^2 \times 6^2 \times 0.035 \times$ torque at full load

$\therefore \quad x^2 = \frac{0.5}{6^2 \times 0.035} = 0.396$

i.e., $x = 0.629$

$\therefore$ Current drawn from the supply mains = $x^2 I_{sc} = 0.396 \times 6 \times I_{\text{full-load}} = 2.736\ I_{\text{fl}}$.

ADDITIONAL EXAMPLES

5.36 A 10-pole, 50 Hz, three-phase star connected slip ring induction motor has a rotor resistance of 0.05 Ω and a standstill rotor reactance of 0.3 Ω per phase. At full load the motor is running at a speed of 585 rpm. Determine the slip at maximum torque and find the ratio of maximum to full load torque.

Solution

$$s_{max} = \frac{R_2}{X_2} = \frac{0.05}{0.3} = 0.167$$

i.e. at 16.7% slip, torque will be maximum.
The full load slip is obtained as

$$s_{fl} = \frac{N_s - N}{N_s} = \frac{600 - 585}{600} = 0.025 \text{ i.e., } 2.5\%$$

$$[\because N_s = \frac{120\, f}{P} = \frac{120 \times 50}{10} = 600 \text{ rpm; } N = 585 \text{ rpm.}]$$

In Eq. 5.18(c) the ratio of full load torque and maximum torque has been obtained.

$$\frac{T}{T_{max}} = \frac{2 \cdot s \cdot s_{max}}{s^2 + s_{max}^2}.$$

For the given problem, we find

$$\frac{T_{max}}{T} = \frac{(0.025)^2 + (0.167)^2}{2 \times 0.025 \times 0.167} = 3.414.$$

5.37 A 6-pole three-phase induction motor is running at a speed of 950 rpm when the input is 50 kW. At this condition the stator copper loss is 1.5 kW and the rotational loss is 1 kW. Determine the rotor copper loss, electromagnetic power developed by the rotor and the mechanical power output.

Solution

Synchronous speed = $\frac{120 \times 50}{6} = 1000$ rpm

Rotor speed 950 rpm.

Hence slip $s = 1 - \frac{950}{1000} = 0.05$

Input = 50 kW

Stator copper loss = 1.5 kW

Hence, air gap power (P_{ag}) = (50 – 1.5) = 48.5 kW

$\therefore$ Rotor copper loss is (sP_{ag}) (= 0.05 × 48.5) or 2.425 kW

$\therefore$ Gross mechanical power developed by the rotor is

[$(1 - s)\, P_{ag}$] or, (1 – 0.05) × 48.5 = 46.075 kW.

$\therefore$ Shaft power output = gross mech. power – rotational loss

= 46.075 – 1 = 45.075 kW.

5.38 A three-phase, 415 V, 4 kW delta connected induction motor has a short-circuit line current of 20 A at 200 V. The motor is started by a star-delta starter. If the full load efficiency and p.f. are 0.85 and 0.8 respectively determine the starting current drawn by the motor and ratio of starting to full load current.

Solution

Short-circuit line current of the motor at 200 V is 20 A. Hence phase current of the motor is $\frac{20}{\sqrt{3}}$ A, i.e., 11.55 A.

The phase voltage of the motor is $\frac{415}{\sqrt{3}} = 239.6$ V (when started by star delta starter).

Hence the starting current drawn by the motor is $\left[11.55 \times \frac{239.6}{200} \text{A}\right]$, i.e., 13.83 A.

At full load condition the motor is delta connected.

Hence full load line current is $\frac{4000}{\sqrt{3} \times 415 \times 0.85 \times 0.8} = 8.184$ A.

$\therefore$ The ratio of starting to full load current $\frac{13.83}{8.184} = 1.689$.

5.39 A three-phase, 50 Hz, 100 kW induction motor has a full load efficiency of 85%. The stator copper loss and rotor copper loss are each equal to the stator core loss at full load. The mechanical loss is equal to one fourth of the rotor copper loss. Calculate (i) the rotor copper loss, (ii) the air gap power, and (iii) the slip.

Solution

Input power of the motor is $\frac{100}{0.85}$ kW $= 117.65$ kW

Total losses = Input – Output = (117.65 – 100) kW = 17.65 kW

Let stator copper loss = rotor copper loss = stator core loss = P

Mechanical loss = $\frac{1}{4}$ rotor copper loss = $\frac{P}{4}$

Now total loss = stator core loss + stator copper loss + rotor copper loss + mechanical loss

$$= P + P + P + \frac{P}{4} = \frac{13P}{4}$$

Hence $\frac{13P}{4} = 17.65$

or $P = 5.43$

$\therefore$ Rotor copper loss is 5.43 kW.

Air gap power = Input power – Stator core loss – Stator copper loss

= 117.65 – 5.43 – 5.43 = 106.788 kW.

But Rotor copper loss = Slip × Air gap power

Hence Slip = $\frac{5.43}{106.788} = 0.05$.

5.40 A 440 V, 50 Hz, 8-pole star connected three-phase induction motor has the following test results:

No load test: 440 V, 25 A, 2500 W

Blocked rotor test: 150 V, 115 A, 9000 W

Determine the equivalent circuit parameters of the motor when the per phase stator resistance is 0.2 Ω.

Solution

From no load test we have,

Per phase voltage $E_0 = \frac{440}{\sqrt{3}}$ V $= 254.03$ V

Per phase current $I_C = 25$ A

Per phase power $W_0 = \frac{2500}{3}$ W $= 833.33$ W

Power factor under no load condition (cos θ_0) = $\dfrac{W_o}{V_o I_o}$.

Hence $\cos\theta_0 = \dfrac{833.33}{254.03 \times 25} = 0.1312$ (lag)

[usually the no load p.f. is very low for induction motors]

Core loss component of the no load current

$$I_C = I_0 \cos\theta_0 = 25 \times 0.1312 = 3.2804 \text{ A},$$

magnetizing component of the no load current

$$I_\phi = I_0 \sin\theta_0 = 25 \sin(\cos^{-1} 0.1312) = 24.783 \text{ A}.$$

Voltage across the magnetizing branch is obtained as $[V_0 - I_0(R_s + jX_s)]$, where $(R_s + jX_s)$ is the per phase stator impedance in ohms.

Again from blocked rotor test data we have

Per phase voltage $E_{s/c} = \dfrac{150}{\sqrt{3}}$ V = 86.6 V

Per phase current $I_{s/c}$ = 115 A

Per phase power $W_{s/c} = \dfrac{9000}{3}$ W = 3000 W

$\therefore$ Per phase impedance $Z_{s/c} = \dfrac{E_{s/c}}{I_{s/c}} = \dfrac{86.6}{115}\ \Omega = 0.753\ \Omega$

Per phase resistance $R_{s/c} = \dfrac{W_{s/c}}{I_{s/c}^2} = \dfrac{3000}{(115)^2}\ \Omega = 0.2268\ \Omega$

Per phase reactance $X_{s/c} = \sqrt{(0.753)^2 - (0.2268)^2} = 0.718\ \Omega$

Per phase rotor resistance referred to the stator,

$$R_2' = R_{s/c} - R_s = 0.2268 - 0.2 = 0.0268\ \Omega.$$

We assume here that per phase stator reactance X_s = Per phase rotor reactance X_2'

$\therefore$ $X_1 = X_2' = \dfrac{X_{s/c}}{2} = \dfrac{0.718}{2} = 0.359\ \Omega.$

Voltage across the magnetizing branch is obtained from the formula $[E_0 - I_0(R_s + jX_s)]$. This gives the required voltage as $[254.03 - 25\ (0.2 + j0.359)]$ V.

i.e., $(249.03 - j8.975)$ V or $(249.192\angle -2.064°$ V)

$\therefore$ Core loss resistance $R_C = \dfrac{249.192}{I_C} = \dfrac{249.192}{3.2804}\ \Omega = 75.963\ \Omega.$

Magnetizing reactance $X_o = \dfrac{249.192}{I_\phi} = \dfrac{249.192}{24.783}\ \Omega = 10.054\ \Omega.$

Hence the equivalent circuit parameters are

$R_0 = 75.963\ \Omega$ $X_0 = 10.054\ \Omega$ $R_s = 0.2\ \Omega$

$R_2' = 0.0268\ \Omega$ $X_s = X_2' = 0.359\ \Omega.$

5.41 A 5 kW, 4-pole, three-phase star connected inductor motor has slipring rotor resistance of 0.05 Ω and standstill reactance of 0.5 Ω for phase. The full-load speed is 1450 rpm. Determine the ratio of maximum torque to the full-load torque, starting torque to the full-load torque and ratio of starting torque to the full-load torque.

Solution

$$N_s = \frac{120 f}{P} = \frac{120 \times 50}{4} = 1500 \text{ rpm}$$

N = 1450 rpm (given)

$\therefore$ s_{fl}(full load slip) = $1 - \dfrac{1450}{1500}$ = 0.033 (= s) (i.e., 3.3%)

s_{max} (slip at maximum torque) = $\dfrac{R_2}{X_2} = \dfrac{0.05}{0.5}$ = 0.1 (i.e., 10%)

$\because$ $\dfrac{T}{T_{max}} = \dfrac{\text{Full load torque}}{\text{Maximum torque}} = \dfrac{2 \cdot s \cdot s_{max}}{s^2 + s_{max}^2}$

Here, $\dfrac{T}{T_{max}} = \dfrac{2 \times 0.033 \times 0.1}{0.033^2 + 0.1^2} = \dfrac{0.0066}{0.011} = 0.595$

$\therefore$ $\dfrac{T_{max}}{T} = 1.68$

Also, $\dfrac{T_{starting}}{T_{max}} = \dfrac{2 \cdot s_{max}}{1 + s_{max}^2} = \dfrac{2 \times 0.1}{1 + 0.1^2} = 0.198.$

We have seen in the text that

$$T_s = \frac{KE_1^2 R_2}{R_2^2 + X_2^2}$$

and $$T = \frac{KE_1^2 \cdot sR_2}{R_2^2 + (sX_2)^2}$$

$\therefore$ $$\frac{T_s}{T} = \frac{KE_1^2 R_2}{R_2^2 + X_2^2} \times \frac{R_2^2 + (sX_2)^2}{KE_1^2 sR_2}$$

$$= \frac{R_2^2 + (sX_2)^2}{(R_2^2 + X_2^2)s} = \frac{(0.05)^2 + (0.033 \times 0.5)^2}{0.033(0.05^2 + 0.5^2)} = \frac{0.0028}{0.00833} = 0.336$$

i.e. $T_s/T = 0.336$.

5.42 An 8-pole, 50 Hz, three-phase induction motor has a full-load torque of 200 Nm when the frequency of the rotor emf is 2.5 Hz. If the mechanical loss is 15 Nm determine the rotor copper loss and the efficiency of the motor. The total stator loss is 1000 W.

Solution

If s be the slip at full load then

s.f = 2.5 (from the given data)

$\therefore$ $s = \dfrac{2.5}{50} = 0.05.$

The speed of the motor at full load

$N = (1 - s)\, N_s$

But synchronous speed $N_s = \dfrac{120\, f}{P} = \dfrac{120 \times 50}{8} = 750$ rpm

Hence $N = (1 - 0.05)\ 750 = 713$ rpm.

or $\omega = \dfrac{713 \times 2\pi}{60}$ rpm = 74.665 rad/s.

Mechanical power developed by the rotor

P_m = (200 + 15) Nm = 215 Nm = 215 × 74.665

= 16052.975 W. [$\because$ $P = \omega_s \times T$]

If P_{ag} be the air gap power then,

$$(1 - s)\, P_{ag} = P_m$$

or $$P_{ag} = \frac{16.053}{1-0.05}\text{ kW} = 16.898\text{ kW}$$

Rotor copper loss is $(sP_g) = 0.05 \times 16.898 = 0.845$ kW
Motor input = 16.052 + 0.845 + 1 = 17.897 kW
Motor output = 200 × 74.665 W = 14.933 kW

Hence efficiency is $\frac{14.933}{17.897} = 0.8344$ or 83.44%.

5.43 A 6-pole, 50 Hz, three-phase induction motor has a maximum torque of 200 Nm when it is running at a speed of 900 rpm. The resistance of the rotor is 0.25 Ω. Neglecting stator impedance determine the torque at 5% slip.

Solution

Synchronous speed $N_s = \frac{120 \times 50}{6} = 1000$ rpm

At maximum torque slip $s_{max} = \left[1 - \left(\frac{900}{1000}\right)\right] = 0.1$

$R_2 = 0.25$ (given)

Hence, $$X_2 = \frac{R_2}{s_{max}} = \frac{0.25}{0.1} = 2.5\ \Omega$$

Torque at any slip s is given by

$$T = \frac{3}{\omega_s} \cdot \frac{E_1^2\, sR_2}{[R_2^2 + (sX_2)^2]}\text{ Nm}$$

$$= \frac{3}{\omega_s} \cdot E_1^2 \times \frac{0.05 \times 0.25}{(0.25)^2 + (0.05 \times 2.5)^2} = \frac{3E_1^2}{\omega_s}\ 0.16.$$

Maximum torque is given by

$$T_{max} = \frac{3}{\omega_s} \cdot \frac{E_1^2}{2X_2} = \frac{3E_1^2}{\omega_s} \cdot \frac{1}{2 \times 2.5} = \frac{1}{5} \cdot \frac{3E_1^2}{\omega_s}$$

Using this expression of (T_{max}) in the expression of (T) we get

$$T = 5T_{max}\, 0.16$$

As $T_{max} = 200$ Nm, we get

$$T = 5 \times 200 \times 0.16 = 160\text{ Nm}.$$

5.44 A 6-pole, three-phase induction motor develops 35 HP including 3 HP mechanical losses at a speed of 960 rpm when connected to 440 V, 3-phase mains. The power factor is 0.8. Find (i) the slip (ii) the rotor copper loss (iii) the total input if stator loss is 3 kW and (iv) the efficiency.

Solution

Synchronous speed $N_s = \frac{120 \times 50}{6} = 1000$ rpm

Speed of the motor $N = 960$ rpm

(i) Slip $= \left(1 - \frac{960}{1000}\right) = 0.04.$

(ii) Gross mechanical power developed is 35×735.5 W = 25742.5 W.
or P_m = 25742.5 W = 25.742 kW.

$$\therefore \text{ Air gap power } (P_{ag}) = \frac{P_m}{1-s} = \frac{25.742}{1-0.04} = 26.81 \text{ kW.}$$

Hence, rotor copper loss is sP_g, i.e., 0.04×26.81 or 1.072 kW.

(iii) Stator loss 3 kW (given).
Hence, total input = 26.81 + 3 = 29.81 kW.

(iv) $\because$ Input = 29.81 kW and
Output = (35 – 3) = 32 HP = 32×0.7355 kW = 23.536 kW,

Hence, efficiency is $\frac{23.536}{29.81} \times 100\% = 78.95\%$.

5.45 A 15 kW, 4-pole, 50 Hz, three-phase induction motor has a mechanical loss 2% of the output. For a full load slip of 3% determine the rotor copper loss and air gap power.

Solution

Output = 15 kW

$$\text{Mechanical loss} = \frac{2}{100} \times 15 = 0.3 \text{ kW}$$

Slip = 0.03

Power developed by the rotor is $P_m = 15 - 0.3 = 14.7$ kW

If P_{ag} be the air gap power then $(1 - s)P_g = P_m$

or $$P_g = \frac{14.7}{1-0.03} \text{ kW} = 15.15 \text{ kW}$$

Rotor copper loss $sP_g = 0.03 \times 15.15 = 0.4545$ kW.

5.46 The rotor resistance of an 8-pole, 50 Hz. wound rotor induction motor has a resistance of 0.5 Ω per phase. The speed of the rotor is 720 rpm at full load.

Determine the external resistance to be connected with the rotor circuit to reduce the speed to 680 rpm for full-load torque.

Solution

$$\text{Synchronous speed } N_s = \frac{120\,f}{P} = \frac{120 \times 50}{8} = 750 \text{ rpm.}$$

$$\text{Slip } (s) = \left[1 - \frac{720}{750}\right] = 0.04$$

If R_2 be the rotor resistance then the rotor copper loss is $I_2^2 R_2$, where I_2 is the rotor current. If P_{ag} be the air gap power or power input to the rotor then

$$sP_{ag} = I_2^2 R_2$$

or $$0.04 = \frac{I_2^2 R_2}{P_{ag}} = \frac{0.5 I_2^2}{P_{ag}} \quad \text{(i)}$$

The new speed N = 680 rpm.

$$\therefore \quad s = \left(1 - \frac{680}{750}\right) = 0.093$$

Let R be the total resistance of the rotor circuit.

In order that the full load torque remains same P_{ag} should have the same value as the previous one.

Hence, $$0.093 = \frac{I_2^2 R}{P_{ag}} \quad \text{(ii)}$$

From equations (i) and (ii)

$$0.093 = \frac{0.04}{0.5} \cdot R$$

or $$R = 1.1625\ \Omega$$

Hence the external resistance to be connected is $(R - R_2)$ or $(1.1625 - 0.5)$, i.e., $0.6225\ \Omega$ per phase.

EXERCISES

Short- and Long-Answer-Type Questions

1. What are the types of three-phase induction motors as per their rotor construction? Compare between them.
2. What are the advantages of using a three-phase induction motors in industry? What are the disadvantages?
3. Briefly explain the principle of operation of a three-phase induction motor.
4. Analytically justify how a rotating field is created in a three-phase induction motor when a balanced three-phase ac supply is applied at the stator terminals.
5. What is slip? Deduce a relationship between rotor current frequency and supply frequency in terms of slip.
6. Derive the torque equation of a three-phase induction motor in terms of rotor quantities. What is the expression for starting torque?
7. Derive the expression for maximum torque in a three-phase induction motor. Obtain the ratios of the full load torque to maximum torque and starting torque to maximum torque of such a motor.
8. Discuss the role of change of supply voltage on the torque and slip of induction motor.
9. Show that starting torque of a polyphase induction motor is governed by the rotor resistance. Hence discuss how we can improve the starting torque of a slip ring induction motor.
10. Show that for a given applied voltage, the starting torque is maximum when the rotor resistance is equal to the stand-still rotor reactance.
11. Derive the torque-slip characteristic of a three-phase inductor motor. What is the affect of variation of rotor resistance?
12. Derive the exact equivalent circuit of a polyphase induction motor on per phase basis. Draw the approximate equivalent circuit with necessary assumptions.
13. What are the different losses in a three-phase induction motor? How do you find efficiency of such a motor?
14. For a three-phase induction motor, prove the following.
    (i) Rotor copper loss = Slip × Rotor input
    (ii) Mechanical power developed in the rotor = (1 – slip) × Airgap power
    (iii) Rotor copper loss = $\left(\frac{\text{slip}}{1-\text{slip}}\right)$ × Mechanical power developed in rotor.

15. Why do we perform no load test and blocked rotor test on induction motors? Describe how we can find the equivalent circuit parameters from these two tests. State the necessary assumptions.
16. Why do we need a starter in starting a three-phase induction motor?
17. Write short notes on:
    (i) Direct on line starting
    (ii) Auto-transformer starting
    (iii) Star delta starter.
18. A 6-pole, 60 Hz induction motor rotates at 3% slip. Find the speed of the stator field, the rotor and the rotor field. What is the frequency of the rotor currents? [*Ans:* 1200 rpm, 1164 rpm, 1200 rpm, 1.8 Hz]

    [*Hint:* $N_s = \dfrac{120 \times 60}{6} = 1200$ rpm.]

    ∴ Stator field rotates at 1200 rpm. Rotor field rotates in the air gap in the same speed.

    N(rotor speed) $= N_s(1 - s) = 1200(1 - 0.03) = 1164$ rpm

    The rotor speed is then 1164 rpm.

    If frequency of rotor current is f_r,

    $$f_r = sf_s = 0.03 \times 60 = 1.8 \text{ Hz}.$$

    Since rotor rotates at 1164 rpm while the speed of the rotor field is 1200 rpm, hence the field speed with respect to the rotor is $(N_s - N)$ i.e., 36 rpm].
19. A three-phase 8-pole squirrel cage induction motor, connected to a 400 V $(L - L)$ 50 Hz supply, rotates at 3% slip at full load. The copper and iron losses at the stator are 2 kW and 0.5 kW respectively. If the motor takes 50 kW at full load, find the full load developed torque at the rotor. [*Ans:* 605 Nm]

    [*Hint:* $P_{ag} = P_{in} - P_{scu} - P_{sc}$
    $= 50 - 2 - 0.5 = 47.5$ kW

    $$\therefore \quad T = \frac{P_{ag}}{\omega_s} = \frac{47.5 \times 10^3}{2\pi \times \dfrac{120 \times 50}{8 \times 60}} = 605 \text{ Nm.}]$$

20. The power input to a three-phase induction motor is 50 kW. Stator loss is 1 kW. Find the gross mechanical power developed in the rotor and the rotor copper loss per phase when the motor has a full load slip of 4%. [*Ans:* 15.68 kW]

    [*Hint:* $P_{\text{in}} = 50$ kW; $s = 0.04$; $P_{scu} = 1$ kW.

    $$\therefore \quad P_{ag} = P_{in} - P_{scu} = 49 \text{ kW}$$

    $$P_{rcu} = s \times P_{ag} = 0.04 \times 49 = 1.96 \text{ kW} \left(= \frac{1.96}{3} \text{ kW per phase}\right)$$

    $$\therefore \quad P_m = P_{ag} - P_{rcu} = \left(\frac{49}{3}\right) - \frac{1.96}{3} = 15.68 \text{ kW}].$$

21. The loss at the stator of a three-phase squirrel cage 25 HP, 1500 rpm induction motor is 2 kW. What is rotor mechanical power if the rotor copper loss is 1 kW? What is the running slip? [*Ans:* 15.65 kW; 6%]

[*Hint:* $P_{in} = 25 \times 746 \times 10^{-3} = 18.65$ kW

$\therefore \quad P_{ag} = 18.65 - 2 = 16.65$ kW

$P_m = P_{ag} - P_{rcu} = 16.65 - 1 = 15.65$ kW.

$\because \quad P_{rcu} = s \times P_{ag}$; $s = \dfrac{P_{rcu}}{P_{ag}} = \dfrac{1000}{16650} = 0.06$ i.e., slip is 6%.]

22. The rotor of a 6-pole, 50 Hz, slip ring induction motor has a resistance of 0.3 Ω/phase and it runs at 960 rpm at full load. How much external resistance/phase must be added to the rotor circuit to reduce the speed to 800 rpm, the torque remaining constant? [*Ans:* 1.2 Ω]

[*Hint:* $N_s = \dfrac{120\,f}{P} = 1000$ rpm

s_{fl} (full load slip) $= \dfrac{1000 - 960}{1000} = 0.04.$

If r be the additional resistance per phase in rotor circuit, we can write $\dfrac{s_{\text{new}}}{s_{\text{fl}}} = \dfrac{R_2 + r}{R_2}$.

Since the power input to the rotor and rotor current remain constant for constant torque and hence from the relation, slip $= \dfrac{\text{Rotor Cu loss}}{\text{Rotor input}}$, we have

$$\frac{s_{\text{new}}}{s_{\text{fl}}} = \frac{3I_2^2(R_2 + r)}{3I_2^2 R_2} = \frac{R_2 + r}{R_2}.$$

Substitution of the values of $s_{\text{fl}} = 0.04$,

$s_{\text{new}} = \dfrac{1000 - 800}{1000} = 0.2$ and $R_2 = 0.3$, yields $r = 1.2$ Ω.]

23. A three-phase, 50 Hz induction motor has an output rating of 500 HP, 3.3 kV ($L - L$). Calculate the approximate full-load current at 0.85 p.f., locked rotor current and no-load current. What is the apparent power drawn under locked rotor condition? Assume the starting current to be 6 times full load current and no load current to be 30% of full load current.

[*Ans:* $I_{\text{fl}} = 76.78$ A; $I_{\text{no load}} = 23.093$ A; $I_{\text{lock rotor}} = 460.68$ A; $P_{\text{locked rotor}} = 2633$ KVA]

[*Hint:* $I_{\text{fl}} = \dfrac{500 \times 746}{\sqrt{3} \times 3300 \times 0.85} = 76.78$ A

$\therefore \quad I_{\text{no load}} = 0.3 \times 76.78 = 23.03$ A

$\because \quad I_{\text{lock rotor}} \equiv I_{\text{start}}$

Hence $I_{\text{start}} = 6 \times I_{\text{fl}} = 460.68$ A.

Apparent power drawn during locked rotor condition is

$P_A = \sqrt{3} \times V_L \times I_{\text{st}} = \sqrt{3} \times 3300 \times 460.68 = 2633$ KVA.]

24. A 4-pole, 60 Hz, 460 V, 5HP induction motor has the following equivalent circuit parameters:

$R_s = 1.21$ Ω; $X_s = 3.10$ Ω

$R_2' = 0.742\ \Omega$; $X_2' = 2.41\ \Omega$

$X_0 = 65.6\ \Omega$

Find the starting and no-load current of the machine.

[*Ans:* $46.15\angle -70.67°$A; $3.87\angle -89°$ A]

[*Hint:* With reference to the equivalent circuit of the induction motor, the input impedance looking from the input side is

$$Z_{in} = (R_s + jX_s) + \frac{jX_o\,(R_2' + jX_2')}{R_2' + jX_2' + jX_o}$$

$$= \left[(1.21 + j3.1) + \frac{j65.6(0.742 + j2.41)}{0.742 + j2.41 + j65.6}\right]\Omega = 5.75\angle 70.72°\ \Omega.$$

At start $s = 1.0$. This means the load resistor in equivalent circuit is, shorted, since $1 - s = 0$.

$$\therefore \quad I_{st} = \frac{V_{L-L}}{\sqrt{3}\,Z_{in}} = 46.15\angle -70.67°\text{ A}.$$

At no load, s 0, i.e., the load element in the equivalent circuit is open.

$\therefore$ Z_{in} (no load) $= (R_s + jX_s) + jX_0 = (1.21 + j68.7)\ \Omega = 68.71\angle 89°\ \Omega$

$$\therefore \quad I_{NL} = \frac{V_{L-L}}{\sqrt{3}\,Z_{in(NL)}} = \frac{460\angle 0°}{\sqrt{3}\,(68.71\angle 89°)} = 3.87\angle -89°\text{A.}]$$

25. A 30 HP, 3-phase 6 pole, 50 Hz slip ring induction motor runs at full load at a speed of 960 rpm. The rotor current is 30 A. If the mechanical loss in the rotor is 1 kW while 200 W loss is being incurred by the rotor short circuiting system, find the rotor resistance per phase. [*Ans:* $R_2 = 0.287\ \Omega$]

[*Hint:* $N_s = 100$ rpm; $s = \dfrac{N_s - N}{N_s} = 0.04$

$\because$ Rotor Cu loss $= \dfrac{s}{1-s} \times$ gross mech power developed in rotor Hence we can write for this problem,

$$3I_2^2 R_2 + 200 = \frac{0.04}{1 - 0.04}\ (30 \times 746 + 1000)$$

or, $3 \times 30^2 \times R_2 = 774.17$

or, $R_2 = 0.287\ \Omega$]

26. A 10 HP, 400 V($L - L$), 50 Hz, 3-phase induction motor has a full load p.f. of 0.8 and efficiency of 0.9. The motor draws 7 A when a voltage of 160 V is applied directly across the live terminals, the motor being standstill. Determine the ratio of starting to full load current when a star-delta starter is used to start the motor. [*Ans:* $(I_{st}/I_{fl}) = 0.39$]

[*Hint:* $I_{fl} = \dfrac{10 \times 746}{\sqrt{3} \times 400 \times 0.8 \times 0.9} = 15$ A.

$I_{s/c}$ at 160 V input = 7.0 A

$\therefore$ I_{s/c_f} at 400 V($L - L$) is $\dfrac{400}{160} \times 7.0 = 17.5$ A.

With star delta starter,

$$I_{\text{starting}} = \frac{1}{3} \times I_{s/c_f} = \frac{1}{3} \times 17.5 = 5.833 \text{ A.}$$

$$\therefore \quad \frac{I_{\text{starting}}}{I_{\text{fl}}} = \frac{5.833}{15} = 0.39.]$$

27. A 75 kW, three-phase induction motor has 1500 rpm synchronous speed. It is connected across a 440 V($L - L$) supply and rotates at 1440 rpm at full load. The two wattmeter method is applied to measure the power input which shows that the motor absorbs 70 kW while the line current is 80 A. If the stator iron loss is 2 kW and rotor mechanical loss is 1.5 kW, find
    (i) the power supplied to the rotor
    (ii) the rotor copper loss
    (iii) the mechanical power developed at shaft
    (iv) the torque developed at rotor
    (v) the efficiency of the motor.

    Assume stator resistance/phase = 0.2 Ω.

    [*Ans:* $P_{\text{ag}} = 64.16$ kW; $P_{\text{rcu}} = 2.57$ kW $P_m = 61.59$ kW; $T = 408.66$ Nm; $\eta = 85.84\%$]

    [*Hint:*

    (i) $P_{\text{in}} = 70$ kW; P_{scu} (stator Cu loss)

    $$= 3I_{fl}^2 \times R_s = 3 \times 80^2 \times 0.2 = 3.84 \text{ kW.}$$

    P_{sc}(core loss in stator) = 2 kW

    $\therefore P_{\text{ag}} = P_{\text{in}} - P_{\text{scu}} - P_{\text{sc}} = 64.16$ kW

    (ii) $P_{\text{rcu}} = s \times P_{\text{ag}} = 0.04 \times 64.16 = 2.57$ kW.

    (iii) $P_m = P_{\text{ag}} - P_{\text{rcu}} = 64.16 - 2.57 = 61.59$ kW.

    (iv) $$T = \frac{P_{\text{ag}}}{\omega_s} = \frac{64.16 \times 10^3}{2\pi \times \frac{1500}{60}} = 408.66 \text{ Nm.}$$

    (v) $$\eta = \frac{P_0}{P_{\text{in}}} = \frac{P_m - \text{mech loss in rotor}}{P_{\text{in}}}.$$

    $$= \frac{61.59 - 1.5}{70} = 0.8584 \text{ i.e., } 85.84\%.]$$

28. A 4-pole, three-phase 50 Hz induction motor develops a maximum torque of 20 Nm at 1440 rpm. Obtain the torque exerted by the motor at 5% slip. Assume rotor resistance to be 0.5 Ω. [*Ans:* 19.51 Nm]

    [*Hint:* $N_s = \frac{120\,f}{P} = 1500$ rpm

    $N = 1440$ rpm

    $$\therefore \quad s = \frac{N_s - N}{N_s} = 0.04 = s_{\max}$$

    But $$s_{\max} = \frac{R_2}{X_2}$$

$$\therefore \qquad X_2 = \frac{R_2}{s_{max}} = \frac{0.5}{0.04} = 12.5\ \Omega$$

If s be the required slip (5%) then from the relation

$$\frac{T}{T_{max}} = \frac{2 \cdot s \cdot s_{max}}{s^2 + s_{max}^2} = \frac{2 \times 0.05 \times 0.04}{(0.05)^2 + (0.04)^2} = 0.9756$$

$$\therefore \qquad T = 0.9756 \times 20 = 19.51 \text{ Nm.}]$$

29. You have a 50 HP, three-phase, 60 Hz, 4-pole, 1765 rpm induction motor operating at 400 V ($L - L$). Find the shaft torque. If the mechanical loss in the shaft (rotor) is 500 W, find the gross mechanical power developed in the shaft and the developed torque. If the rotor copper loss is 800 W, what is the value of air gap power? Also find the electromagnetic torque developed. If the total stator losses are 1 kW, find the motor input power.

[*Ans:* $T_{sh} = 201.91$ Nm, $P_m = 37.8$ kW; $T_m = 204.62$ Nm
$P_{ag} = 38.6$ kW; $T = 204.89$ Nm; $P_{in} = 39.6$ kW]

[*Hint:* $T_{sh} = \dfrac{P_0}{\omega} = \dfrac{50 \times 746}{2\pi \times \dfrac{1765}{60}} = 201.91$ Nm

$P_m = P_0$ + mech loss in rotor
$= 50 \times 746 \times 10^{-3} + 500 \times 10^{-3} = 37.8$ kW

$T_m = \dfrac{P_m}{\omega} = \dfrac{37.8 \times 10^3}{2\pi \times \dfrac{1765}{60}} = 204.62$ Nm

$P_{ag} = P_m$ + rotor copper loss
$= 37.8 \times 10^3 + 800 = 38600$ W $= 38.6$ kW

$T = \dfrac{P_{ag}}{\omega_s} = \dfrac{38.6 \times 10^3}{2\pi \times \dfrac{1800}{60}} = 204.89$ Nm

$\left(\because N_s = \dfrac{120 \times 60}{4} = 1800 \text{ rpm} \right)$

$\because$ Stator copper loss is 1 kW,

$\therefore \qquad P_{in} = 1 + P_{ag} = 1 + 38.6 = 39.6$ kW.]

30. A 400 V, 4-pole, 50 Hz, 3 phase squirrel cage induction motor develops 25 HP at 4% slip on full load. If the ratio of motor resistance to standstill reactance is 1:4, find the ratio starting torque to full load torque.

[*Ans:* $(T_s/T) = 1.51$]

[*Hint:* $N_s = 1500$ rpm; $N = N_s(1 - s) = 1440$ rpm ($\because s = 0.04$)

$$T(\text{full load}) = \frac{25 \times 735.5}{\omega} = \frac{25 \times 735.5}{2\pi \times \dfrac{1440}{60} \times 10^3} = 0.122 \text{ Nm.}$$

At standstill the torque is T_s while at 4% slip it is T.

$$\therefore \quad \frac{Ts}{T} = \frac{\dfrac{s_0 R_2 E_1^2}{R_2^2 + (s_0 X_2)^2}}{\dfrac{sR_2 E_1^2}{R_2^2 + (sX_2)^2}}$$, (s_o) being the slip at starting.

With $s_0 = 1$,

$$\frac{T_s}{T} = \frac{R_2^2 + (sX_2)^2}{s\left[R_2^2 + X_2^2\right]} = \frac{\left(\frac{R_2}{X_2}\right)^2 + s^2}{s\left[\left(\frac{R_2}{X_2}\right)^2 + 1\right]} = \frac{\left(\frac{1}{4}\right)^2 + (0.04)^2}{0.04\left[\left(\frac{1}{4}\right)^2 + 1\right]} \qquad 1.51]$$

31. A 415 V, three-phase, 6 pole, 50 Hz induction motor runs at a slip of 4% on full load. The rotor resistance and reactance are 0.01 Ω and 0.05 Ω when the motor is at standstill. Find the ratio of full load torque to maximum torque. Also obtain the speed at which the maximum torque occurs.
[*Ans:* $N_{\max}$ = 800 rpm; $(T/T_{\max}) = 0.385$]

[*Hint:* $s_{\max} = \frac{R_2}{X_2} = \frac{0.01}{0.05} = 0.2$.

The speed at a slip of 0.2 would then be 800 rpm as N_s = 1000 rpm.

$$\because \quad \frac{T}{T_{\max}} = \frac{2 \cdot s \cdot s_{\max}}{s^2 + s_{\max}^2}$$

for this problem $\frac{T}{T_{\max}} = \frac{2 \times 0.04 \times 0.2}{(0.04)^2 + (0.2)^2} = 0.385$.]

32. An induction motor has a short circuit current of 6 times the full load current at normal supply voltage. It has a full-load slip of 5%.
Calculate the starting torque in terms of the full load torque if started by
(i) star-delta starter
(ii) auto-transformer starter with 60% tapping.
Neglect magnetizing branch currents. [*Ans:* 0.2; 0.648]

[*Hint:* We have $\frac{T_s}{T_{\text{fl}}} = \left(\frac{I_s}{I_{\text{fl}}}\right)^2 \cdot s_{fl}$

(i) For *Y*-Δ starting: At start, winding is placed in star and only $\left(\frac{1}{\sqrt{3}}\right)$ of normal voltage is applied. Again, short circuit current being 6 times the full load current (winding in delta connection), we can write short circuit phase current as

$$I_{\text{s/c(ph)}} = \frac{6 \times \text{f.l. current}}{\sqrt{3}}$$

$$\therefore \quad I_{\text{starting/phase}} = \frac{1}{\sqrt{3}} \times I_{\text{s/c(ph)}}$$

as $\frac{1}{\sqrt{3}}$ of normal voltage is applied per phase.

i.e. $$I_{st/ph} = \frac{1}{\sqrt{3}} \times \frac{6}{\sqrt{3}} \times I_{fl}.$$

$$\therefore \quad \frac{I_{st}}{I_{fl}} = \frac{1}{\sqrt{3}} \times \frac{6}{\sqrt{3}} = 2$$

Hence, $$\frac{T_s}{T_{fl}} = (2)^2 \times 0.05 = 0.2.$$

(ii) Auto-transformer starting with 60% tapping:
At start, stator winding remain in delta connection. However, only 60% voltage is made available at stator.

$$\therefore \quad I_s = \frac{60}{100} \times 6\ I_{fl} = 3.6\ I_{fl}$$

Hence $$\frac{T_s}{T_{fl}} = (3.6)^2 \times 0.05 = 0.648.]$$

MULTIPLE CHOICE QUESTIONS

1. At standstill, the slip of an induction motor is given by
   (a) $s = 1$ (b) $s = 0$
   (c) $s = 1/2$ (d) $s = -1$
   Answer: (a) $s = 1$
2. Under blocked rotor test of a three-phase inductor motor, the ship is
   (a) 0 (b) 0.02
   (c) 1 (d) ∞
   Answer: (c) 1
3. A 4 pole, 50 Hz induction motor runs at a speed of 1440 rpm. The frequency of rotor current is
   (a) 2 Hz (b) 1 Hz
   (c) 3 Hz (d) 50 Hz
   Answer: (a) 2 Hz
4. A 50-Hz three-phase induction motor has rated speed of 725 rpm. The number of poles is
   (a) 2 poles (b) 6 poles
   (3) 4 poles (d) 8 poles
   Answer: (d) 8 poles
5. Synchronous speed is function of
   (a) frequency only
   (b) number of poles only
   (c) both frequency and number of poles
   (d) voltage
   Answer: (c) both frequency and number of poles

6. The frequency of the induced emf in the rotor circuit is
   (a) maximum at synchronous speed
   (b) maximum at standstill
   (c) zero at standstill
   (d) none of these
   Answer: (b) maximum at standstill
7. The three-phase ship ring induction motor has
   (a) short circuit rotor (b) double case rotor
   (c) wound rotor (d) open circuit rotor
   Answer: (c) wound rotor
8. The ship of a 400 V, three-phase, 50 Hz, 4 pole induction motor when rotating at 1440 rpm is
   (a) 2% (b) 3%
   (c) 4% (d) 5%
   (e) none of these
   Answer: (e) none of these
9. In a three-phase induction motor, the starting torque is proportional to
   (a) directly voltage (b) square of voltage
   (c) inverse of voltage (d) none of these
   Answer: (b) square of voltage
10. A three-phase 6 pole induction motor runs at 950 rpm. What is the synchronous speed?
   (a) 900 rpm (b) 1500 rpm
   (c) 1000 rpm (d) 1900 rpm
   Answer: (c) 1000 rpm
11. For star delta starter, the starting torque is
   (a) $\frac{1}{3}$ rd of that obtained in DOL starting
   (b) equal so that obtained in DOL starting
   (c) $\frac{1}{\sqrt{3}}$ times of that obtained in DOL starting
   (d) $\frac{1}{9}$ times of that obtained in DOL starting
   Answer: (a) $\frac{1}{3}$ rd of that obtained in DOL starting
12. The relation between synchronous speed (N_s) and rotor speed (N) of a three-phase induction motor is given by
   (a) $N = \frac{f}{p} \cdot s$ (b) $N = \frac{120f}{p}$
   (c) $N = \frac{120}{f} \cdot p(1-s)$ (d) $\frac{120f}{p}(1-s)$
   Answer: (d) $\frac{120f}{p}(1-s)$

UNIVERSITY QUESTIONS WITH ANSWERS

Long-Answer-Type Questions

1. (a) "A three-phase induction motor is self-starting"—why? (WBUT 2012)
   Answer: Article 5.5
   (b) Obtain the relation between the slip and the frequency of the rotor induced emf. (WBUT 2012)
   Answer: Article 5.8
   (c) A 4 pole, 3 phase, 275 KW, 440 V, 50 Hz, induction motor is running with a slip of 4%. Find (i) synchronous speed (ii) rotor speed (iii) frequency of the rotor induced emf. (WBUT 2004)

   Answer: $\left.\begin{aligned} s &= 0.04 \\ f &= 50 \text{ Hz} \\ P &= 4 \end{aligned}\right\}$ given.

   (i) Synchronous speed $(N_s) = \dfrac{120f}{P} = \dfrac{120 \times 50}{4} = 1500$ rpm

   (ii) Rotor speed $(N_r) = (1 - s)\, N_s = (1 - 0.04) \times 1500 = 1440$ rpm

   (iii) Frequency of the rotor induced emf is (sf) i.e., $0.04 \times 50 = 2$ Hz

2. (a) Explain how rotating magnetic field is produced in a three phase induction motor. (WBUT 2007, 2013)
   Answer: Article 5.6.
   (b) A 3 phase, 6 pole, 50 Hz. induction motor has a slip of 1 % at no load and 3 % at full load. Calculate (i) synchronous speed, (ii) no load speed, (iii) full load speed, (iv) frequency f rotor current at full load, and (v) frequency f rotor current at standstill. (WBUT 2007)
   Solution: No load slip $s_{nl} = 0.01$.
   Full load slip $s_{fl} = 0.03$

   (i) Synchronous speed $N_s = \dfrac{120f}{P} = \dfrac{120 \times 50}{6} = 1000$ rpm

   (ii) No load speed $(N_{nl}) = (1 - s_{nl})\, N_s = (1 - 0.01)\, 1000 = 990$ rpm

   (iii) Full load speed $(N_{fl}) = (1 - s_{fl})\, N_s = (1 - 0.03)\, 1000 = 970$ rpm

   (iv) Frequency of rotor current at full load is $s_{fl}\, f = 0.03 \times 50 = 1.5$ Hz

   (v) Slip at standstill is 1.
   $\therefore$ frequency of rotor current at standstill is $1 \times 50 = 50$ Hz

   (c) Explain with suitable diagram a method of controlling speed of an induction motor.
   Answer Article 5.16.

3. (a) "A three-phase induction motor is self starting"—why?
   Solution: Refer Article 5.5.
   (b) Obtain the relation between the slip and the frequency of the rotor induced emf. (WBUT 2008)
   Solution: Refer Article 5.6.

(c) A 4-pole, 3-phase, 275 kW, 440 V, 50 Hz induction motor is running with a slip of 4 %. Find (WBUT 2012)

(i) Synchronous speed

(ii) Rotor speed

(iii) Frequency of the rotor induce emf.

Solution: $P = 4$

$s = 0.04$

$f = 50$ Hz

(i) Synchronous speed $N_s = \dfrac{120f}{P} = \dfrac{120 \times 50}{4} = 1500$ rpm

(ii) Rotor speed $N_r = (1 - s)\, N_s = (1 - 0.04) \times 1500 = 1440$ rpm

(iii) Frequency of the rotor induced emf is $sf = 0.04 \times 50 = 2$ Hz

(d) Derive an expression for torque-slip characteristics of a 3 phase induction motor.

Solution: Refer Article 5.10.

4. (a) Derive an expression for the torque slip characteristic of a three phase induction motor.

Answer: Article 5.10.

(b) A three phase 4 pole, 50 Hz induction motor has a slip of 1% at no load and 3% at full load calculate (i) synchronous speed, (ii) no load speed, (iii) full load speed, (iv) frequency of rotor current at standstill, and (v) frequency of rotor current at full load.

(WBUT 2005)

Answer: No. of poles (P) = 4

No. load slip (s_{nl}) = 0.01

Full load slip (s_{fl}) = 0.03

Frequency (f) = 50 Hz

(i) Synchronous speed $(N_s) = \dfrac{120f}{P} = \dfrac{120 \times 50}{4} = 1500$ rpm

(ii) No load speed $(N_{nl}) = (1 - s_{nl})\, N_s = (1 - 0.01) \times 1500 = 1485$ rpm

(iii) Full load speed $(N_{fl}) = (1 - s_{\text{fl}})\, N_s = (1 - 0.03) \times 1500 = 1455$ rpm.

(iv) Frequency of rotor current at standstill = $1 \times 50 = 50$ Hz

[$\because$ slip a standstill is 1]

(v) Frequency of rotor current at full load = $s_{fl} \times 50$

$= 0.03 \times 50 = 1.5$ Hz.

5. (a) Discuss briefly the principle of speed control of 3-phase induction motor by variation of input voltage and frequency. [WBUT 2013]

Solution: Refer Article 5.16.

(b) A three-phase 415 V, 50 Hz star-connected 4-pole induction motor has stator impedance $Z_1 = (0.2 + 10.5)\,\Omega$ and rotor impedance referred to the

stator side is $Z_2 = (0.1 + 10.5)\,\Omega$ and resistance representing core loss is $40\,\Omega$ on per-phase basis. Determine the rotor current at a slip of 0.04.

[WBUT 2013]

Solution: Refer Example 5.28.

6. (a) Obtain the condition for maximum torque for a 3 ϕ induction motor.

[WBUT 2014]

Solution: Refer Article 5.9.4.

(b) The power input to a 400 V, 60-pole, 50 Hz, 3 ϕ induction motor running at 975 rpm is 40 kW. The stator losses are 1 kW and friction and windage losses are 2 kW. Find the efficiency of the motor.

[WBUT 2014]

Solution: Refer Example 5.27.

Multiple Choice Question

1. The speed in which stator magnetic field rotates is called (WBUT 2012)
   (a) actual speed
   (b) synchronous speed
   (c) slip speed
   (d) super-synchronous speed

   Answer: (b) synchronous speed

2. The resistance R0 of the exciting branch of the equivalent circuit of a three-phase inductor motor represents (WBUT 2013)
   (a) stator core loss
   (b) stator copper loss
   (c) friction and windage losses
   (d) rotor copper loss

   Answer: (a) stator core loss

6 STRUCTURE OF A POWER SYSTEM

6.1 STRUCTURE OF A POWER SYSTEM

Electricity is the only for m of energy used in industrial, domestic, commercial and transportation sector. It is a coveted form of energy, since it can be generated in bulk and transmitted economically over long distances. Electric power system deals with generation, transmission and distribution of electric energy associated with the unique feature of control of the flow or demand of energy at desired nodes throughout the power network. Figure 6.1 represents the most basic structure of a power network, where generators produce electric energy, transformers transform this energy from one voltage level to another and transmission lines wheel the power from the generating stations to the load centers for final distribution of electrical energy to different loads. Tie lines interconnect one system with the neighbouring electric system belonging to the same grid. The circuit breakers isolate a faulty part of the network (the fault being sensed by the relays) while static/rotary compensators may be used for voltage control at load or remote buses. Conventionally, loads are represented in lumped or composite form.

The best location of a generating station being at a place very close to electrical load center (i.e., the region where the major energy demand exists), the practical location of the primary conventional energy sources do not necessarily coincide with the urban centers. The location of the power plant is frequently governed by its closeness to the energy resource and transportation facility of the fuel as well as availability of nearest load center. Environmental aspects are also key factors in determining the site of the plant. Mostly, a generating plant consists of generating units complete with necessary accessories. Control elements like different valves, exciters, regulators etc also form up transformers and instrument transformers along with breakers are intended in the station switchyard for transmission of power and protection of the system. Sources of input to the generating system are conventionally *fossil fuels* (e.g., coal, oil and gas), hydrosource and nuclear fuel; however, non-conventional sources like wind power, solar energy, tidal power, geothermal power etc. are also being used for *stand-alone systems*.

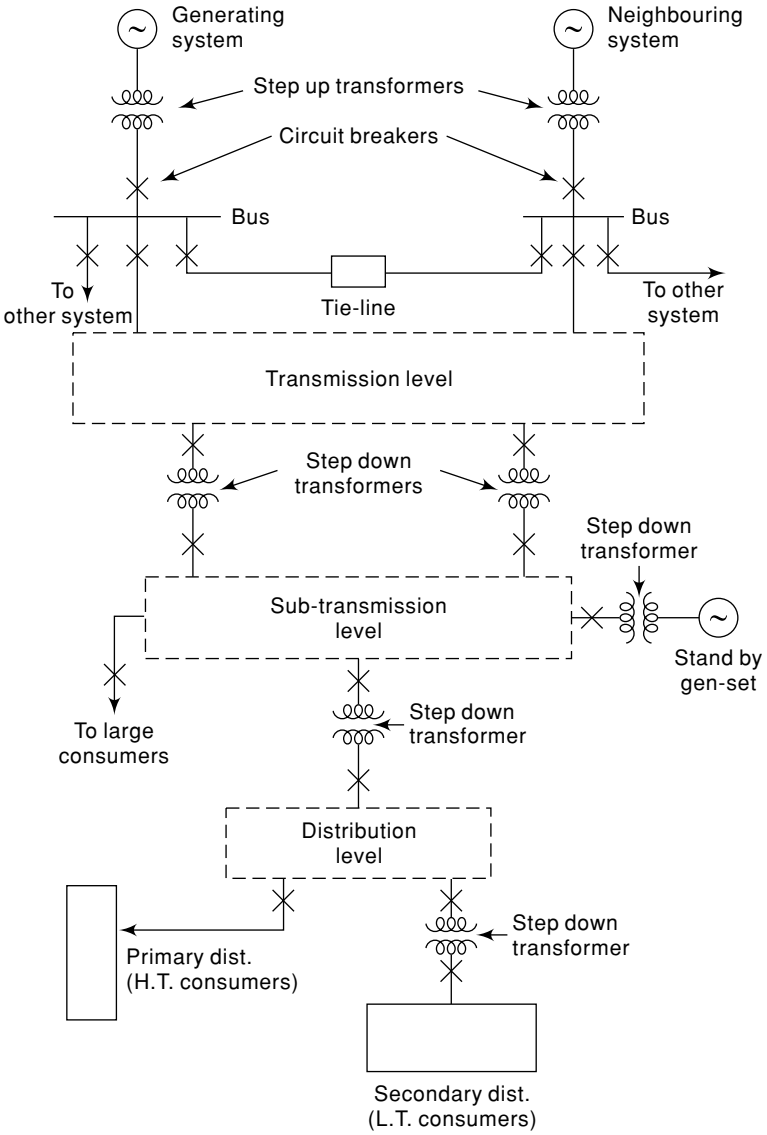


Fig. 6.1 ***Basic structure of a power system***

An electric power system, even a small one, usually constitutes an electric network of vast complexity. The diversity of the system magnitude being great, there is no general rule regarding the structure of the system that apply to any power system. However, mostly any power system could be categorized by a combination of generation, transmission and distribution networks. Next to generation, transmission plays a vital role in transporting power from the generating station to load centers. Transmission of power is usually done at HV/EHV/UHV range due to the known fact that it reduces the power loss in the line as well as

improves the stability. The common transmission voltage are 33 KV/66 KV/114 KV/132 KV/138 KV/161 KV/220 KV/230 KV/345 KV/400 KV/500 KV in the HV and EHV ranges and 765KV/800KV/1100KV/1500KV in the UHV ranges in most parts of the world while the generation voltages have commonly been 6 KV/ 11 KV/12.47 KV/13.2 KV/13.8 KV/15 KV/16 KV/22 KV (all line to line voltage).

In sub-transmission level, the circuits distribute electric power to a number of distribution centers in a certain geographical region at a voltage level that typically varies between 23 KV to 138 KV, the most common grades being 33 KV/ 66 KV/110 KV/120 KV/132 KV. The sub-transmission circuits may also receive electric power directly from any generator bus. Larger customers are mostly served by sub-transmission level circuits. In small power systems, the sub-transmission level may coincide with distribution level.

The distribution level consists of the distribution circuits in the overall region of distribution. Larger consumers i.e., high tension (H.T) consumers have been termed as *primary distributors* while low tension (L.T) consumers are *secondary distributors*. The consumers consuming energy between 3 KV and 23 KV are H.T consumers while the consumers in the category of 110V-400/440 V lie in the class of secondary or L.T consumers.

6.2 POWER DISTRIBUTION SYSTEMS

A distribution system can be subdivided into feeders, distributors and service mains. Feeders are conductors of large current carrying capacity and may be a cable in metropolitan city or a overhead line in sub-urban and village areas. Feeders carry the current in bulk from the substation (where transmission voltage is stepped down for distribution purpose) to the feeding points. The distributors are conductors from which power is tapped off for supply to the consumer. A feeder may feed a number of parallel distributors through a suitable bus arrangement in an enclosure (popularly known as—Feeder Pillar Box). The distributor may also be a cable or an overhead line. It may be noted that the size of the feeder is determined primarily by the current it is required to carry. This is due to the fact that the voltage drop across the feeder can be allowed for by stipulated regulation. On the other hand the permissible voltage drop along a distributor is the main basis of selection of distributors. For a given power delivered if the voltage is increased n times, the current in the feeder is reduced to $1/n$ times original value. This means the conductor of the feeder needs only $1/n$ times the original cross section.

If the distributor is connected to the supply system on one end only, the system is said to be a radial system of distribution. In such a case the end of the distributor nearest to the substation could be heavily loaded and the consumers at the distant end of the distributor would be subjected to voltage depression as the load on the distributor increases. In addition to this, the consumer is dependent upon a single feeder so that a fault on any feeder or distributor disrupts the supply to the consumers who are on the side of the fault away from the station. To eliminate this problem mesh type or ring main type distributors are used in planned metropolitan cities. This system employs a feeder which encircles the

whole area of supply finally returning to the substation (i.e. the feeder is closed on itself). The distributors are connected at different points on the ring main feeder and the arrangement is similar to two feeders in parallel but different routes. The reliability of supply is greatly increased and in the event of a fault in any section of the feeder the supply to all consumers can continue by isolating the faulty section.

The service mains are the small cables between the distributors and the consumers premises. The service mains may be single phase or three phase type.

6.3 POWER SYSTEM REPRESENTATION

Since a complete diagram of a practical power system presenting all the three phases (generation, transmission and distribution) is too complicated, it is a normal practice to represent a power system by means of simple systems for each component resulting in single-line diagram, as shown in Fig. 6.2.

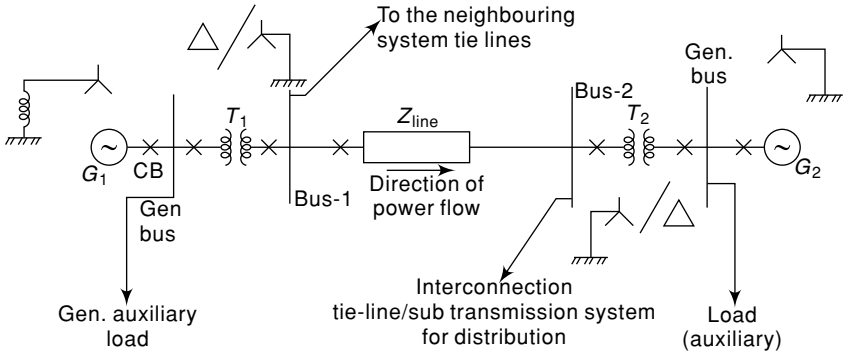


Fig. 6.2 ***Single line representation of a simple two bus system***

Any particular component may or may not be shown in the diagram depending on the information required in a system study e.g., circuit breakers need not be shown in a load flow analysis diagram but are to be shown for a protection study. Different generator and transformer connections are indicated by proper symbols. Equivalent circuits of power circuit components can be represented in the diagrams.

EXERCISES

Short- and Long-Answer-Type Questions

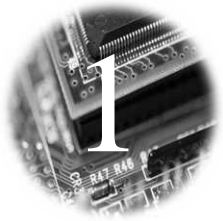
1. What are the primary functions of transformers in power transmission-distribution system?
2. What location is best suited for a generating station?
3. What are the different sources of input to the generating stations to produce electrical power?
4. What do you mean by a stand alone system?
5. Why the transmission of power is done at HV/EHV/UHV level?
6. What are the common transmission voltages in India?

7. What are the standard voltage levels for subtransmission and distribution circuits?
8. Write a brief note on power distribution system.
9. What are the advantages of a ring main distribution system over radial system?
10. Draw the single line diagram of a radial power system and label different parts.

UNIVERSITY QUESTION WITH ANSWER

1. Draw a general single-line diagram from power generation to distribution. (WBUT 2014)

   Solution: Refer Fig. 6.1.



1 FIELD EFFECT TRANSISTORS

1.1 INTRODUCTION

Bipolar Junction Transistor (BJT) is most commonly used as switching devices and amplifiers in analog electronics circuits. It has three terminals such as Base (B), Emitter (E) and Collector (C). It is a minority carrier device and it is also a current controlled device as depicted in Fig. 1.1(a). When a base current (I_B) flows, the transistor will be ON. If the base current (I_B) is equal to zero, the BJT is in OFF state.

Another popular transistor is Field Effect Transistor (FET). The FET is also a semiconductor device and its operation depends on the control of current by an applied electric field. Therefore, FET is a voltage controlled device. Unlike the BJT, FET is a majority carrier device and this device has three terminals such as gate (G), drain (D) and source (S) as depicted in Fig. 1.1(b).

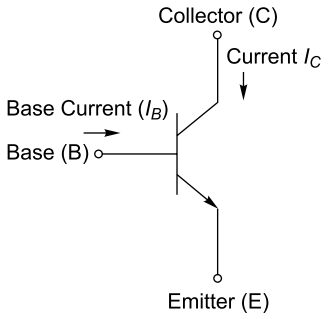


Fig. 1.1(a) *BJT*

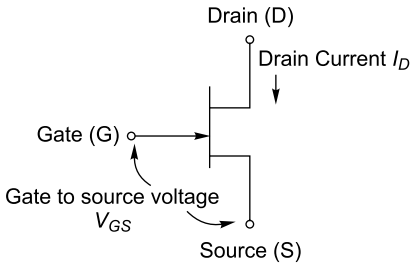


Fig. 1.1(b) *FET*

There are two types of field effect transistors namely, *Junction Field Effect Transistor* (JFET) and *Insulated Gate Field Effect Transistor* (IGFET). The IGFET is commonly known as metal-oxide-semiconductor (MOS) transistor or MOSFET. In 1960, the MOSFET was first developed by Kahng and Atalla.

FETs are used as switching devices in analog electronics circuits, amplifiers with high input impedance and integrated circuits (ICs). The features of field effect transistors (FET) are as follows:

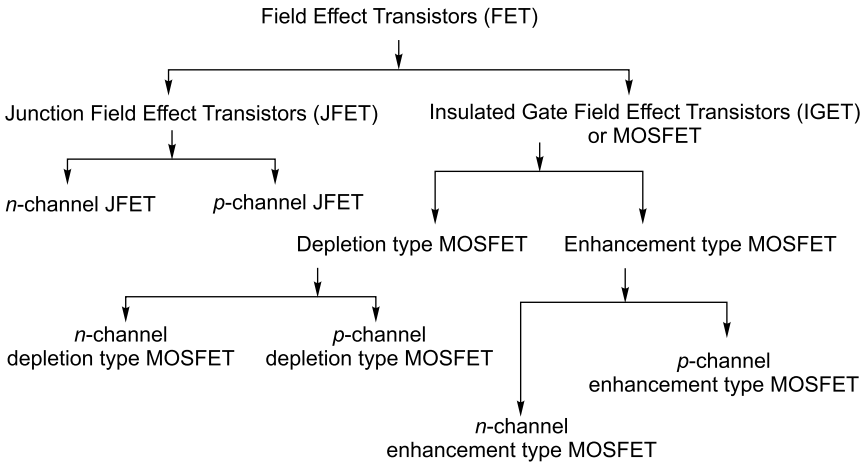
1. It provides high input impedance about 1 mega-ohm.
2. The operation of FET depends on the flow of majority carriers only. Therefore, it is called a unipolar device.
3. It is easy to fabricate and less space is required to develop ICs using FET.
4. FET has negative temperature coefficient at high current. If current decreases, temperature increases. Uniform temperature distribution with in device prevents to generate a thermal runway. Hence, second breakdown can be prevented. Consequently, this device is thermally stable.
5. It has relatively small noise with respect to BJT
6. It has zero offset voltage at zero drain current.

The only disadvantage of FET is that it has comparatively small gain bandwidth product compared to BJT.

In this chapter, the basic structure of FET with channel width modulation, JFET structure and characteristics, operating principle of JFET, structure of MOSFET, characteristics of MOSFET, common source (CS), common gate (CG), and common drain (CD) configurations of FET are discussed in detail. The basic principle of CMOS is also incorporated in this chapter.

1.2 CLASSIFICATION OF FIELD EFFECT TRANSISTOR

Field effect transistors are two types such as junction field effect transistor (JFET) and insulated gate field effect transistor (IGFET) or metal-oxide-semiconductor transistor (MOSFET). Depending on the types of channel, the junction field effect transistors can be divided as *n*-channel JFET and *p*-channel JFET. Depending upon the operating principle, MOSFET is classified as depletion type MOSFET and enhancement type MOSFET. Again MOSFET is further classified as *n*-channel and *p*-channel MOSFET. The following chart shows the classification of field effect transistors.



1.2.1 Gate Isolation Types

In a field effect transistor, a GATE electrode is placed above (electrically insulated from) the silicon surface, and is used to control the resistance between the SOURCE and DRAIN regions. The gate is isolated from the drain and source by using an oxide insulator (SiO_2) as depicted in Fig.1.2(a).

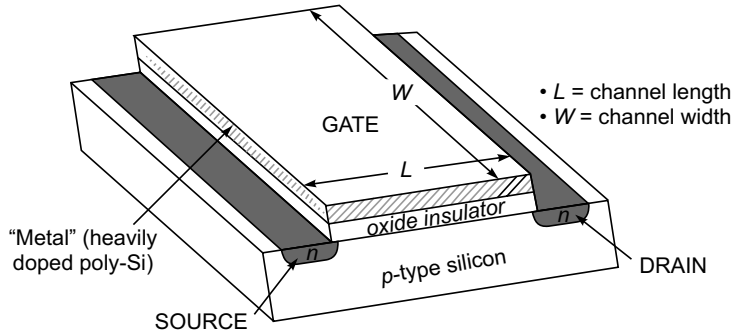


Fig. 1.2(a) ***Gate-isolation-type field effect transistor***

Gate-isolation-type field effect transistors are *n*-channel Metal Oxide Semiconductor (NMOS) and *p*-channel Metal Oxide Semiconductor (PMOS). In these transistors, without a gate-to-source voltage applied, no current can flow between the source and drain regions. When the gate-to-source voltage is greater than the *threshold voltage* V_T, a conducting layer of mobile electrons is formed at the Si surface beneath the oxide. These electrons can carry current between the source and drain. Figure 1.2(b) shows an *n*-channel metal oxide semiconductor (NMOS). The detailed operations of NMOS and PMOS are explained in Sections 1.11, 1.12, 1.13, 1.14, 1.15 and 1.16.

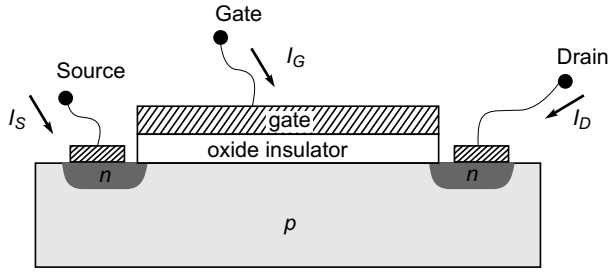


Fig.1.2(b) ***n-channel metal oxide semiconductor (NMOS)***

1.3 JUNCTION FIELD EFFECT TRANSISTOR

The junction field effect transistor (JFET) has a conducting channel with ohmic contacts on either end. The conducting channel will be either an *n*-type semicon-

ductor or a *p*-type semiconductor. Depending on the types of channel, JFET can be classified as *n*-channel JFET and *p*-channel JFET.

Figure 1.3 shows the structure of an *n*-channel JFET which has two p^+ regions on either sides of the *n*-channel. Actually, an *n*-type semiconductor bar has two *p*-type heavily doped regions (p^+ region) on the opposite sides of the *n*-channel. Hence, p^+ type region form two p^+n junctions. Two p^+ regions are connected internally and a single output terminal is available from the device and it is called gate (G) terminal.

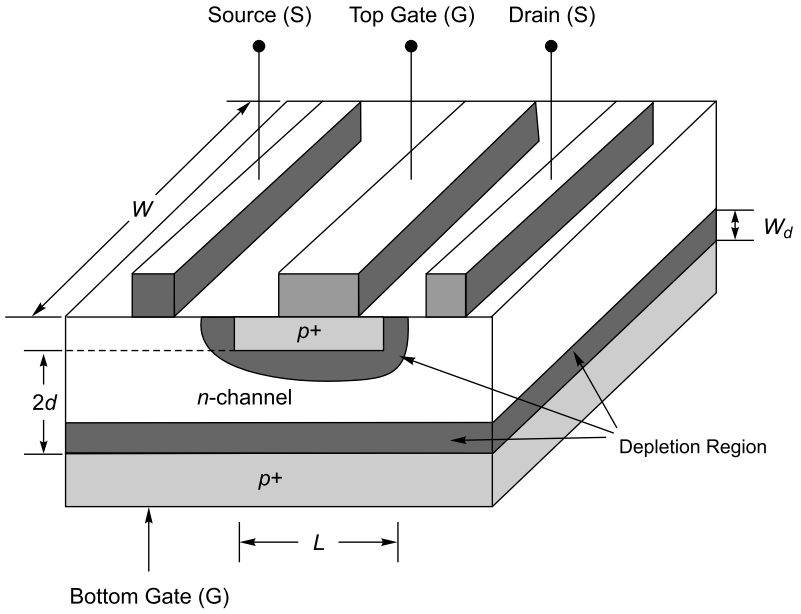


Fig. 1.3 ***Structure of an n-channel JFET***

One side of the ohmic contacts is called the source (S) and the other side is known as the drain (D). Source (S) is a terminal through which electrons can enter into the *n*-type semiconductor and the electrons leave the *n*-type semiconductor bar through drain (D) terminal. The most simplified representation of *n*-channel JFET is illustrated in Fig. 1.4.

Source (S): The source (S) is a terminal through which the majority carriers can enter into the semiconductor bar. The current enter the semiconductor through S terminal represented by I_S.

Drain (D): The drain (D) is a terminal through which the majority carriers can leave from the semiconductor bar. The current entering the semiconductor through drain (D) terminal is designated by I_D. The voltage between drain and source terminals is called V_{DS}. It is also represented by V_{DD}.

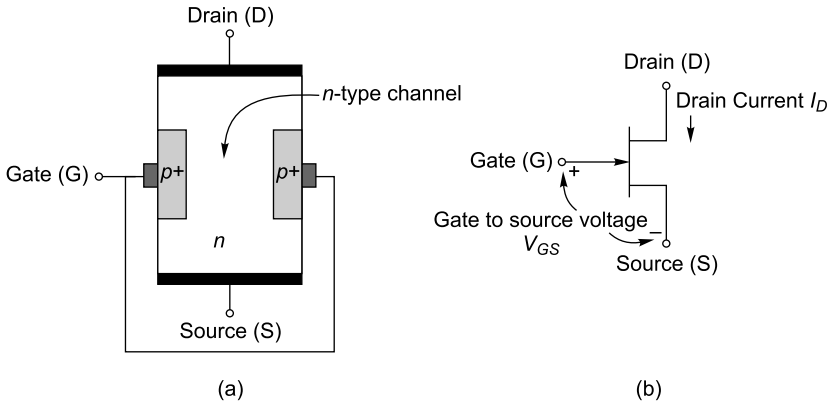


Fig. 1.4 ***(a) Simplified structure of an n-channel JFET (b) Symbol of JFET***

Gate (G): Two heavily doped p^+ regions on either side of n-channel are interconnected and called gate (G). The voltage between the gate and source is called V_{GS}. The V_{GS} is applied in the direction to the reverse bias the p-n junction. The current entering the semiconductor bar through G terminal is represented by I_G.

The basic structure of p-channel JFET is shown in Fig. 1.5(a) and the symbol of p-channel JFET is depicted in Fig. 1.5(b). The p-channel JFET consists of two n^+ type regions and a p-channel. The current carriers in a p-channel JFET are holes.

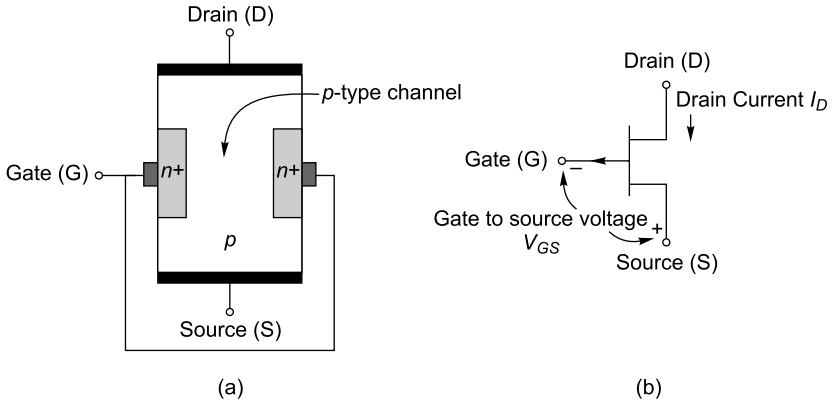


Fig. 1.5 ***(a) Simplified structure of an p-channel JFET (b) Symbol of JFET***

In n-channel JFET, if a p^+n junction is reverse biased, electrons and holes diffuse across the junction and leaves positive ions on the n-side and an negative ions on the p-side. These immovable positive and negative ions generate depletion regions. When the reverse bias voltage across p^+n junction increases, the thickness of the depletion region is also increased. While p-region and n-region of the junctions are equally doped, the depletion region can be extended equally in the p-regions and n-regions. Actually, in n-channel JFET p sides are heavily doped. Then depletion region can be extended into the lower doping region only. In a n-channel FET, the p-type region is heavily doped and n-type region is lightly doped. Consequently, depletion region is extended into the n-channel as shown in Fig. 1.6.

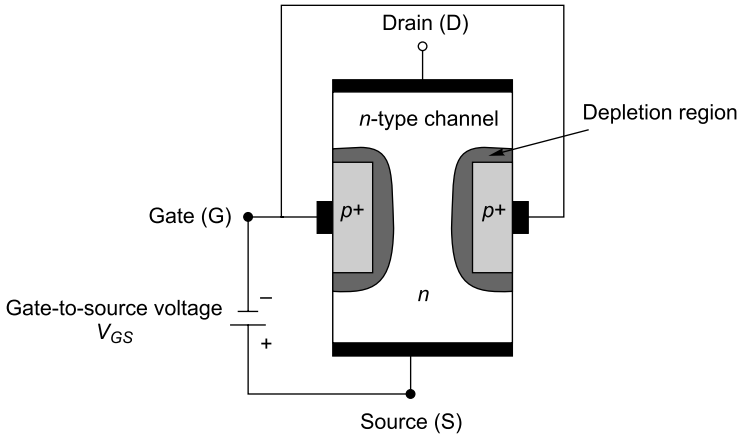


Fig. 1.6 *Depletion region in n-channel JFET*

While the voltage between gate and source becomes zero all of a sudden and the depletion region is present around the junction symmetrically, the conductivity of depletion region is zero since there is no mobile charge. Therefore, the width of *n*-channel can be reduced. With increasing the reverse–bias voltage between gate and source, the depletion region further increased in the *n*-type semiconductor. Hence, the channel width further reduces.

The gate to source p^+n junction of a JFET can be reverse biased when drain is connected to the positive terminal of the dc supply (V_{DD}) and the source is connected to the negative terminal of dc supply as depicted in Fig. 1.7 and gate is open. Assume that r_a and r_b are channel resistances which are variable. The value of r_a and r_b depends on the magnitude of gate to source voltage (V_{GS}) and drain to source voltage (V_{DS}).

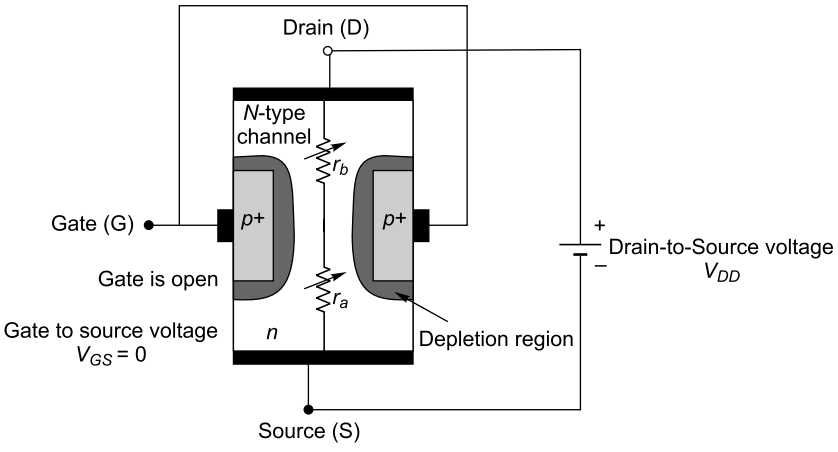


Fig. 1.7 ***Gate is open (V_{GS} = 0) and V_{DD} voltage is applied across drain and source while depletion region is symmetrical***

When the gate (G) terminal is opened and V_{DD} is applied across drain to source, electrons flow from source to drain through *n*-type channel. As a result the drain

current (I_D) flows from drain to source. Due to drain current, there will be a voltage drop across resistance r_b. This voltage across r_b provides the effect of reverse biasing of the gate to source p^+n junction. Hence, when the gate is open, gate to source p^+n junction is reverse biased by drain to source voltage. Then depletion region is developed with in the device as shown in Fig. 1.8.

The depletion region is asymmetrical and it is extended deeper in the *n*-channel near the drain terminal. The depletion layer thickness is less in the *n*-channel near source terminal. Actually, the voltage across r_a is larger than the voltage across r_b. Therefore, reverse bias voltage is comparatively high near drain with respect to source.

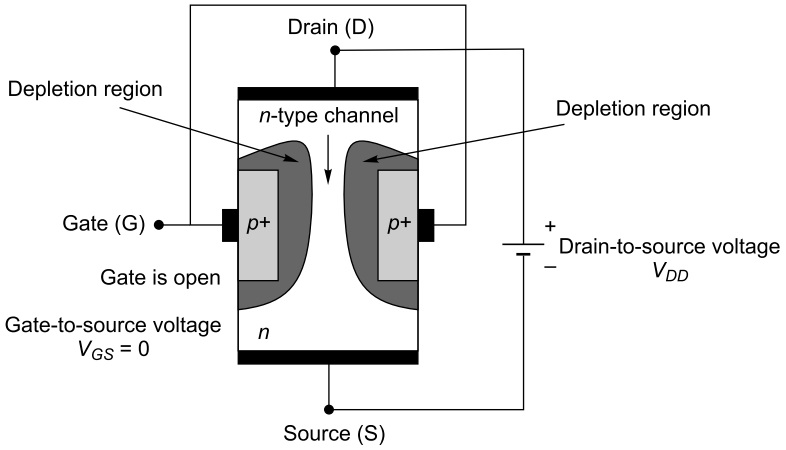


Fig. 1.8 ***Effect of drain to source voltage in depletion region***

1.4 OPERATION OF JFET

Figure 1.9 shows an *n*-channel JFET and the schematic block diagram of an *n*-channel JFET with channel length *L*, channel depth 2*d* and depletion region width W_d is depicted in Fig. 1.10. The channel resistance is $R = \rho \frac{L}{A}$ where ρ is the resistivity of the channel. The expression of conductivity σ is $\sigma = e\mu_n N_D$.

Then, $$R = \rho \frac{L}{A} = \frac{L}{\sigma A} \quad \text{where} \quad \sigma = \frac{1}{\rho}$$

or, $$R = \frac{L}{e\mu_n N_D A} \quad \text{as} \quad \sigma = e\mu_n N_D \tag{1.1}$$

where N_D is the donor concentration in *n*-type channel

As the depletion region width is W_d, the area of the channel is

$$A = 2W(d - W_d) \text{ where } W \text{ is the channel width.}$$

After substituting the value of A in Eq. (1.1), we get

$$R = \frac{L}{2e\mu_n N_D W(d - W_d)}$$

When the gate to source voltage $V_{GS} = 0$ and the drain-to-source voltage V_{DS} is very small value and V_{DS} is about zero, the reverse bias across the p^+n junction is constant and the thickness of the depletion region across the p^+n junction is uniform as depicted in Fig. 1.10.

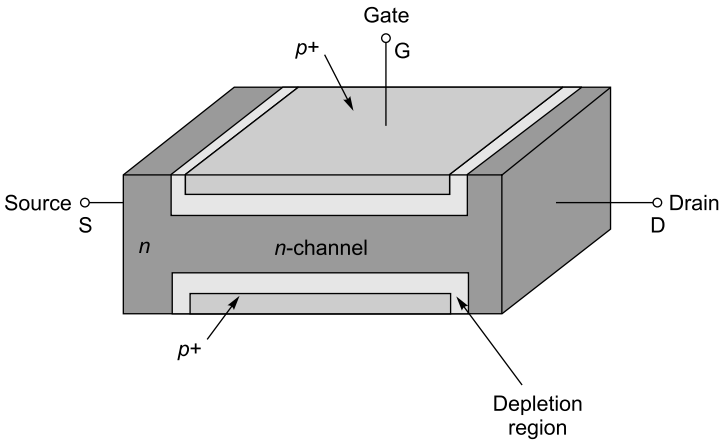


Fig. 1.9 ***Basic Structure of an n-channel JFET***

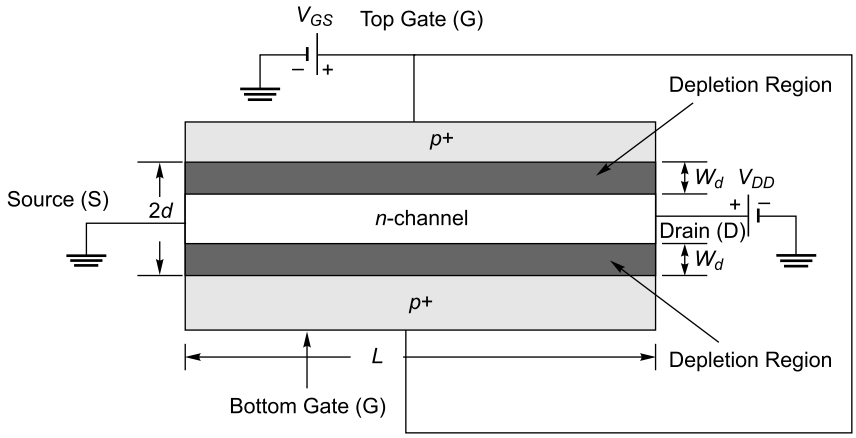


Fig. 1.10 ***Schematic diagram of an n-channel JFET***

If drain to source voltage $V_{DS} = 0$ and gate to source voltage V_{GS} decreases from zero, the reverse bias across the p^+n junction increases progressively from source to drain. Consequently, the depletion region width increases from source to drain and the effective channel width is reduced from source to drain. If again the V_{GS} decreases, the thickness of the depletion region in the channel increases until two depletion region may contact with each other. In this condition, the channel will be cut off completely. The gate-to-source voltage V_{GS} at which the channel will be cut off completely, is called the cut off voltage.

When $V_{GS} = 0$ and voltage V_{DS} increases gradually from zero, the drain is positive with respect to source. Then majority carriers (electrons) can flow through the *n*-type channel from source to drain and drain current I_D flows from drain to source. The magnitude of drain current depends on

(a) majority carriers available in the *n*-type channel
(b) resistance of channel which depend upon
  - Length of the channel (L)
  - Cross-sectional area of the channel i.e., $A = 2W(d - W_d)$
(c) the magnitude of the applied voltage V_{DS}

Due to the resistance of the channel and the voltage V_{DS}, the positive potential is gradually increased along the channel from source to drain. Therefore, the reverse voltage across the p^+n junction increases and the width of the depletion regions also increases as depicted in Fig. 1.10.

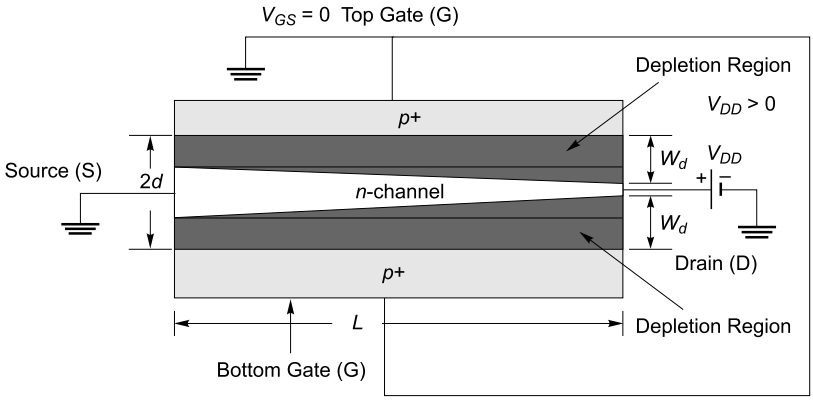


Fig. 1.10 ***n-channel JFET with $V_{GS} = 0$ and $V_{DD} > 0$***

With increases the voltage V_{DS}, the effective channel cross-sectional area decreases. As a result, channel resistance increases and the rate of change of the drain current decreases with increasing V_{DS}. Therefore, a certain portion of output characteristics is linear as shown in Fig. 1.11.

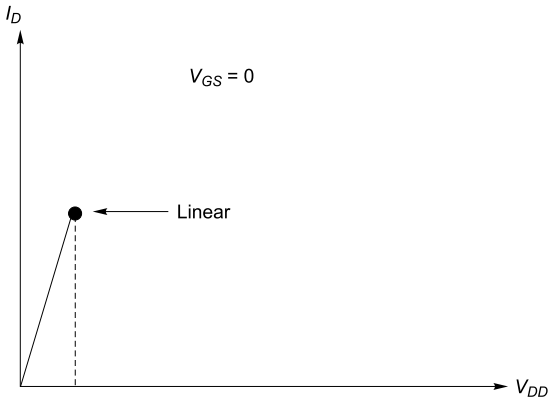


Fig. 1.11 ***Output characteristics of n-channel JFET with $V_{GS} = 0$ and $V_{DD} > 0$ in linear zone***

When the voltage V_{DS} is further increased progressively, the cross-sectional area of the channel will be reduced. At certain value of V_{DS}, the cross-sectional area of the channel becomes zero and the channel will be pinched off as shown in Fig. 1.12. The drain voltage at which pinched off occurs is called pinch-off voltage and it is represented by V_P.

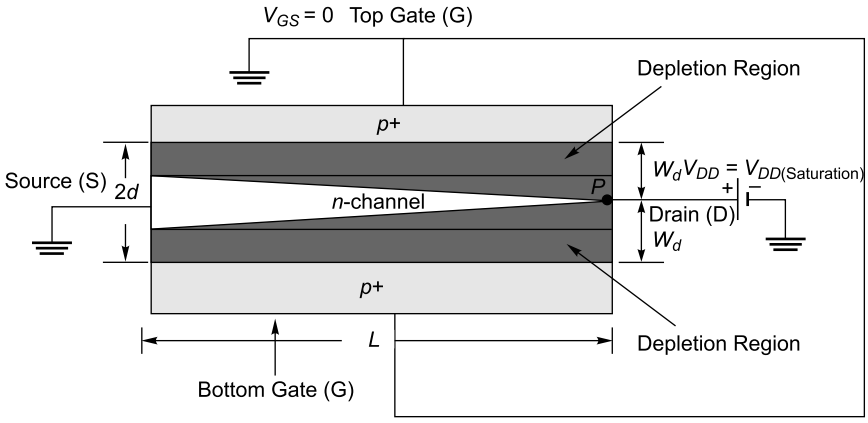


Fig. 1.12 ***n-channel JFET with V_{GS} = 0 and V_{DD} = $V_{DD(saturation)}$***

As the depletion region width increases with increasing V_{DS}, at certain value of V_{DS} the two depletion regions touch each other. At that time, the depletion region width (W_d) is equal to d at the drain and this is represented by the pinch-off point as depicted in Fig. 1.12. At pinch-off point the drain current is designated by $I_{D(\text{saturation})}$ and drain to source voltage is represented by $V_{DS(\text{saturation})}$. The output characteristics of JFET upto the pinch-off point is shown in Fig. 1.13.

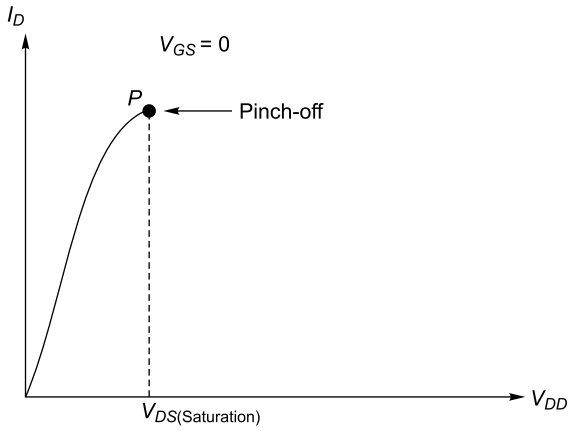


Fig. 1.13 ***Output characteristics of n-channel JFET with V_{GS} = 0 and V_{DD} > = $V_{DD(saturation)}$ at pinch-off***

When V_{DS} is further increased, the pinch-off point P shifts towards source terminal as shown in Fig. 1.14. The voltage drop in the channel between the source and the pinch-off point is constant. This constant potential drop ensures

that the flow of the number of electrons from source to the pinch-off point remains constant. Hence, the constant drain current (I_D) flows after the pinch-off point as depicted in Fig. 1.15 and the device operates in saturation region.

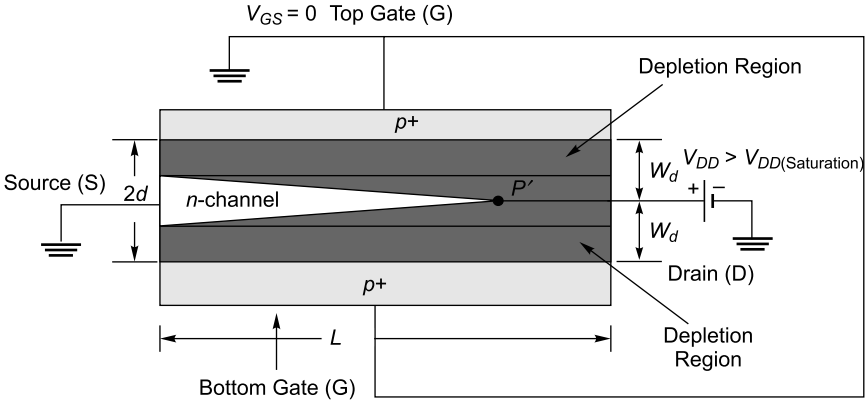


Fig. 1.14 ***n-channel JFET with V_{GS} = 0 and $V_{DD} > V_{DD\,(saturation)}$***

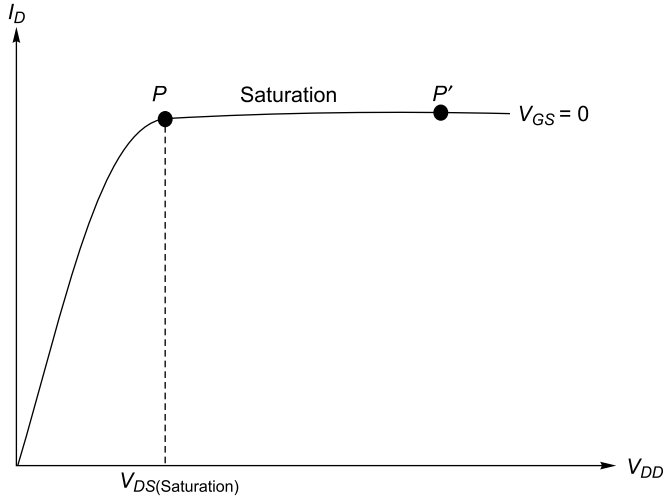


Fig. 1.15 ***Output characteristics of n-channel JFET with V_{GS} = 0 and V_{DD} > = $V_{DD(saturation)}$ at saturation***

When $V_{GS} < 0$, the depletion region width W_d is larger than the depletion region width with $V_{GS} = 0$. Then the cross-sectional area of the channel is reduced as shown in Fig. 1.16 and the resistance value will be increased. Therefore, the drain current (I_D) is also reduced for any value of V_{DS}. If the drain to source voltage V_{DS} is increased gradually with $V_{GS} < 0$, the different output characteristics curve will be obtained. The output characteristics of the JFET for different values of V_{GS} are depicted in Fig. 1.17.

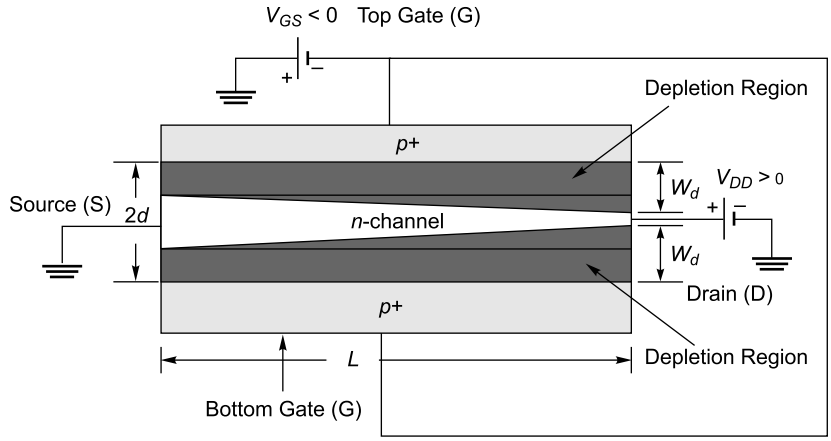


Fig. 1.16 *n-channel JFET with $V_{GS} < 0$ and $V_{DD} > 0$*

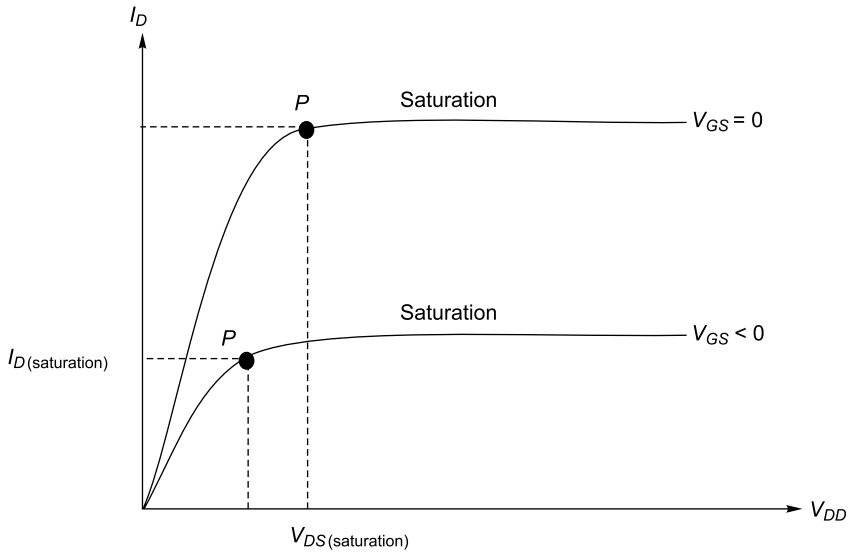


Fig. 1.17 *Output characteristics of n-channel JFET with $V_{GS} = 0$ and $V_{DD} > 0$ and $V_{GS} < 0$ and $V_{DD} > 0$*

1.5 CHARACTERISTICS OF JFET

Characteristic curves are a set of curves which represent the relationship between current and voltages. JFET has two important characteristics such as

(i) Drain characteristics It is a family of curves which relates between the drain current (I_D) and drain to source voltage (V_{DS}) for different values of gate to source voltage (V_{GS}).

(ii) Transfer Characteristics It is a family of curves which relates between the drain current (I_D) and gate to source voltage (V_{GS}) for different values of drain to source voltage (V_{DS}).

Figure 1.18 shows the circuit diagram of JFET to determine the drain and transfer characteristics of JFET. The potentiometer (P_1) is used to vary the gate to source voltage (V_{GS}) and the potentiometer (P_2) is used to vary the drain to source voltage (V_{DS}). The V_{GS} and V_{DS} voltages are measured by voltmeters. The drain current (I_D) can be measured by milli-ammeter.

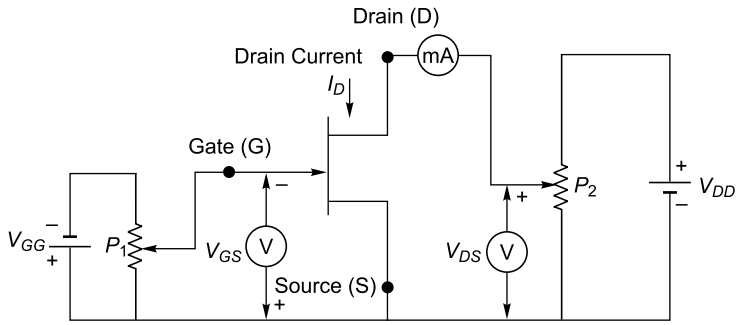


Fig. 1.18 ***Circuit diagram of an n-channel JFET to obtain characteristics***

1.5.1 Drain Characteristics

To get the drain characteristics, initially we maintain V_{GS} = 0 V and increase the drain-to-source voltage (V_{DS}) in small steps and measure the drain current in each step of V_{DS}. Then we plot the characteristics curve with drain-to-source voltage (V_{DS}) along the horizontal axis and drain current (I_D) along the vertical axis. This characteristics curve is subdivided into three regions such as

- Linear region
- Saturation (Pinch-off) region
- Breakdown region

Linear region In this region, the drain current (I_D) increases linearly when the drain to source voltage (V_{DS}) increases linearly and it flows Ohm's law. The region *OA* is linear region as depicted in Fig. 1.19. In this region, the *n*-type semiconductor channel acts as a resistance.

Saturation (Pinch-off) region The region *BC* is called saturation region as depicted in Fig. 1.19. Since the drain current (I_D) remains constant at its maximum value (I_{DSS}), this region is also known as constant current region. The drain current in saturation or pinch-off region depends on V_{GS}, V_P and I_{DSS} and it can be expressed by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where I_{DSS} drain saturation current, V_{GS} is gate-to-source voltage and V_P is the pinch of voltage.

The above equation is known as *Shockly's equation*. Usually, JFET is used as an amplifier when this device operates in pinch-off region.

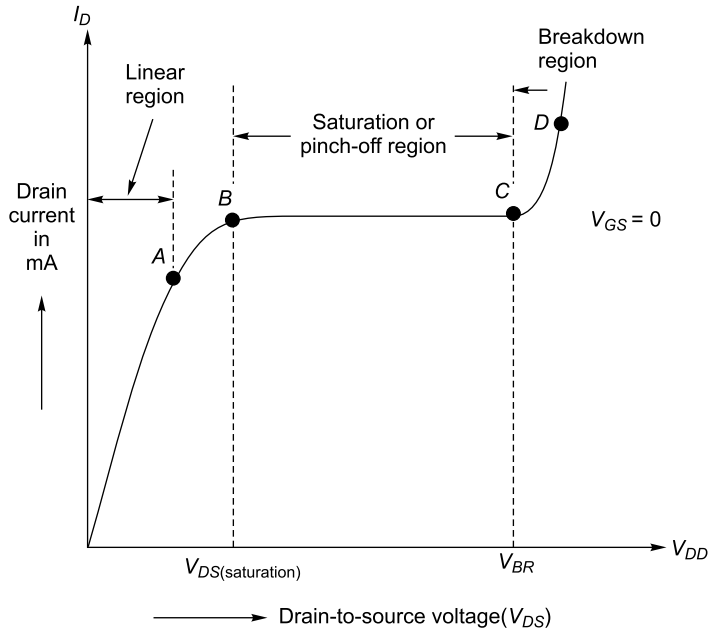


Fig. 1.19 ***Drain characteristics of a FET with $V_{GS} = 0$***

Figure 1.20 shows the schematic diagram of a FET when gate-to-source voltage is $-V_{GS}$ and drain-to-source voltage is V_{DD}. Assume that the p^+ region is doped with N_A acceptors per cubic meter and the n-region is doped with N_D donors per cubic meter and p^+n junction is abrupt. Since $N_A >> N_D$, $W_n >> W_p$. The space charge width is $W_n(x) = W_d(x)$ and the width of the channel at distance x from source terminal can be expressed by

$$W_d(x) = a - b(x) = \left[\frac{2\varepsilon}{qN_D}\{V_o - V(x)\}\right]^{\frac{1}{2}}$$

where ε is the dielectric constant of channel material
q is the magnitude of charge of electron
V_o is the junction contact potential at distance x
$V(x)$ is the applied potential across space charge region at a distance x

At pinch-off condition, $b(x)$ is zero and $W_d(x) = a$ and $V >> V_o$. Assume $V(x) = V_P$ and then pinch-off voltage is equal to $|V_P| = \frac{qN_D}{2\varepsilon} a^2$ as $a = \left[-\frac{2\varepsilon}{qN_D} V_P\right]^{\frac{1}{2}}$

When $V_o - V(x)$ is represented by V_{GS}, we can write

$$a - b(x) = \left[\frac{2\varepsilon}{qN_D} V_{GS}\right]^{\frac{1}{2}}$$

or,
$$V_{GS} = \frac{qN_D}{2\varepsilon}\{a - b(x)\}^2$$
$$= \frac{qN_D}{2\varepsilon}a^2\left\{1 - \frac{b(x)}{a}\right\}^2$$
$$= \left\{1 - \frac{b(x)}{a}\right\}^2 V_P \text{ as } |V_P| = \frac{qN_D}{2\varepsilon}a^2$$

Therefore,
$$\frac{V_{GS}}{V_P} = \left\{1 - \frac{b(x)}{a}\right\}^2$$

From the above equation, we get $b(x) = a\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]$

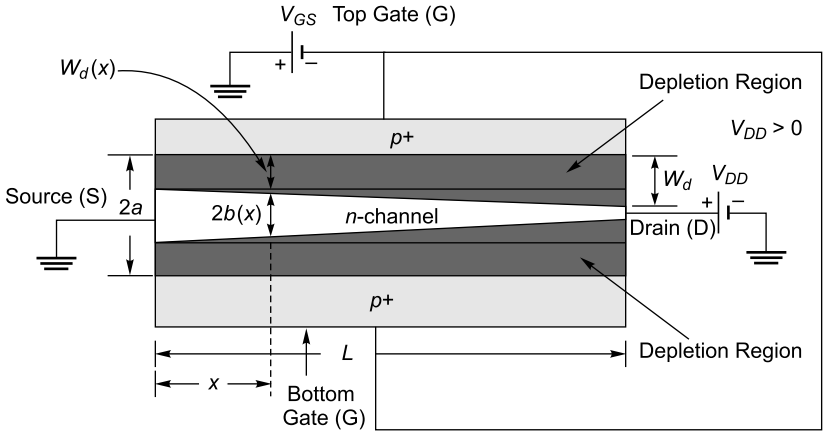


Fig. 1.20 ***The schematic diagram of a FET with $-V_{GS}$ and V_{DD}***

Breakdown region When drain to source voltage is increased above V_{BR}, the drain current increases very rapidly. Consequently, the breakdown of gate-to-source junction occurs due to avalanche effect. The drain to source voltage (V_{BR}) is called *breakdown voltage*. The breakdown region is represented by *CD* as depicted in Fig. 1.19.

When the gate-to-source voltage is reduced from zero, the value of pinch-off voltage (V_P) is smaller than the pinch-off voltage at $V_{GS} = 0$. The drain characteristics for different values of V_{GS} ($V_{GS} = -1$V, $V_{GS} = -2$V, $V_{GS} = -3$V and $V = -4V$) are shown in Fig. 1.21.

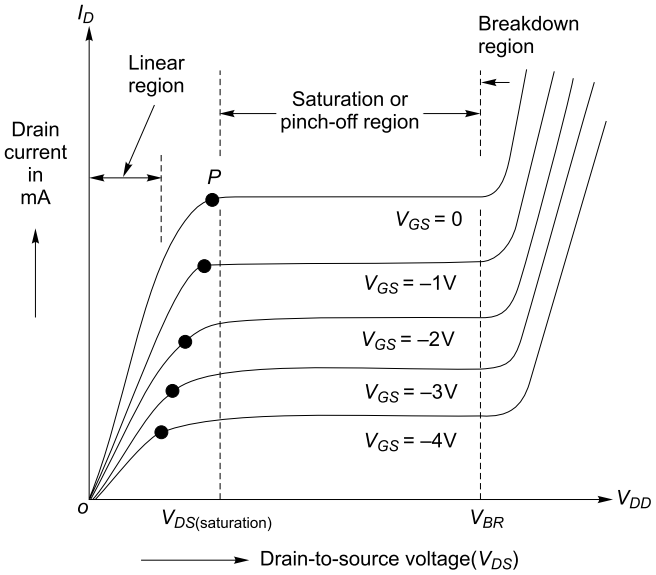


Fig. 1.21 ***Drain characteristics of an n-channel JFET with different values of V_{GS}***

Similarly, the circuit diagram of a *p*-channel JFET is shown in Fig. 1.22 which is used to determine the characteristics of *p*-channel JFET. The drain characteristics of *p*-channel JFET with different values of V_{GS} are illustrated in Fig. 1.23.

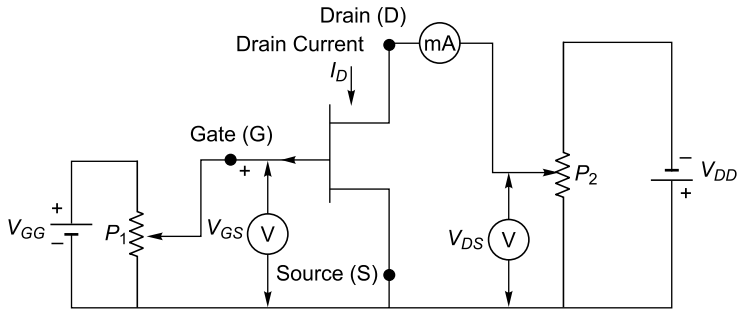


Fig. 1.22 ***Circuit diagram of p-channel JFET to obtain characteristics***

1.5.2 Transfer Characteristics

This is the relationship between drain current (I_D) and gate-to-source voltage (V_{GS}) for constant value of drain to source voltage (V_{DS}). In Fig. 1.18, initially maintain the drain-to-source voltage at specified value and then increase the gate-to-source voltage in small steps and measure the corresponding drain current at each step. After that, we can plot the curve between gate-to-source voltage (V_{GS}) and drain current (I_D). This curve is known as the transfer characteristics of FET as shown in Fig. 1.24 where I_{DSS} is the maximum drain current.

The nature of this curve is parabola and it can be expressed by

$$i_D = i_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = i_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{1.2}$$

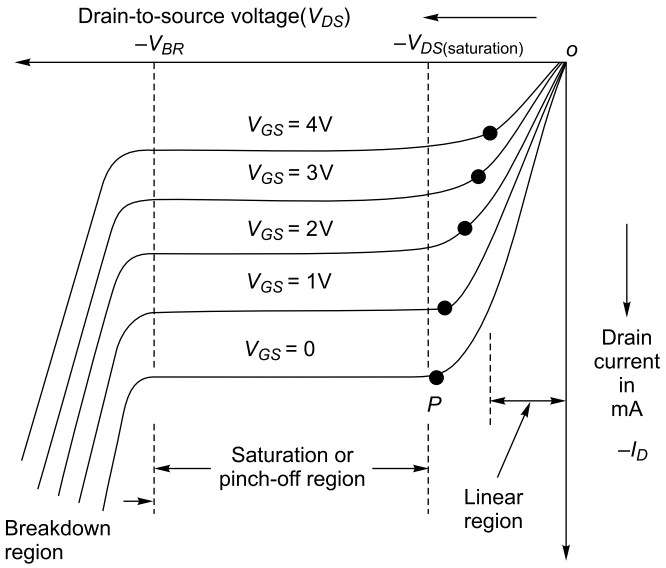


Fig. 1.23 ***Drain characteristics of an p-channel JFET with different values of V_{GS}***

Where, i_D is drain current, i_{DSS} is saturation drain current when $V_{GS} = 0$ and $V_{GS(off)} = V_P$ is the pinch-off voltage.

After differentiating Eq. (1.2) with respect to V_{GS}, we get

$$\frac{\partial i_D}{\partial V_{GS}} = i_{DSS} \times 2\left(1 - \frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right)$$

Since $g_m = \dfrac{\partial i_D}{\partial V_{GS}}$ when V_{DS} held constant, we find

$$g_m = -\frac{2i_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{1.3}$$

Form Eq. (1.2), we obtain $\left(1 - \dfrac{V_{GS}}{V_P}\right) = \left(\dfrac{i_D}{i_{DSS}}\right)^{\frac{1}{2}}$. After substituting the value of $\left(1 - \dfrac{V_{GS}}{V_P}\right)$ in Eq. (1.3), we obtain $g_m = \dfrac{2\sqrt{i_D i_{DSS}}}{V_P}$

If $$V_{GS} = 0, \quad g_m = g_{m0} = -\frac{2i_{DSS}}{V_P}$$

Then Eq. (1.3) can be written as

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

The slope of the transfer characteristics at drain current i_{DSS} is

$$g_m = \frac{2\sqrt{i_D i_{DSS}}}{V_P}$$

or, $$\frac{\partial i_D}{\partial V_{GS}} = -\frac{2\sqrt{i_D i_{DSS}}}{V_P}$$

If $$I_D = I_{DSS}, \quad \frac{\partial i_D}{\partial V_{GS}} = -\frac{2i_{DSS}}{V_P} = \frac{i_{DSS}}{-V_P/2}$$

When a tangent is drawn at $i_D = i_{DSS}$ and $V_{GS} = 0$, the characteristics curve can intercept at $-V_P/2$ on the x-axis i.e., V_{GS}. Then the value of V_P can be determined from Fig. 1.24. The gate to source cut-off voltage $V_{GS(off)}$ is also equal to pinch-off voltage V_P. Hence, $V_P = V_{GS(off)}$. Then, the Eq. (1.2) can be written as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

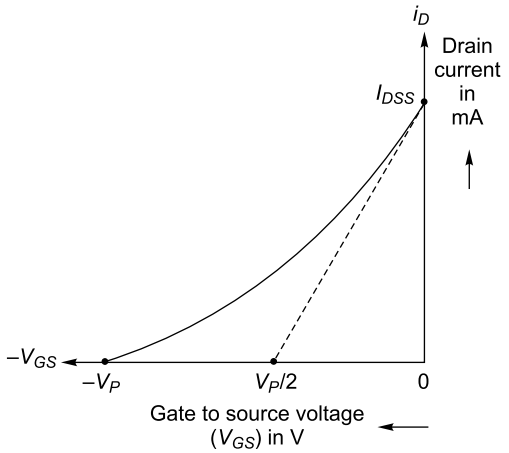


Fig. 1.24 *Transfer characteristics of n-channel JFET*

1.6 CHARACTERISTIC PARAMETER OF JFET

The drain current i_D of JFET is a function of the gate to source voltage V_{GS} and the drain to source voltage V_{DS} and it can be expressed by

$$i_D = f(V_{GS}, V_{DS}) \tag{1.4}$$

When any one of V_{GS} and V_{DS} is fixed, the relationship between other two variables can be used to determine the following three parameters:

- Transconductance (g_m)
- Drain resistance (r_d)
- Amplification factor (μ)

When gate-to-source voltage V_{GS} and drain to source voltage V_{DS} are varied, the change of drain current can be represented by the Eq. (1.5) which is the representation of Eq. (1.4) by Taylor's series expansion.

$$\Delta i_D = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} \Delta V_{GS} + \left.\frac{\partial i_D}{\partial V_{DS}}\right|_{V_{GS}} \Delta V_{DS} \tag{1.5}$$

Transconductance (g_m) This is the slope of the transfer characteristics curves and it is represented by g_m. It can be expressed by

$$g_m = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} = \frac{\Delta i_D}{\Delta V_{GS}} \quad \text{when } V_{DS} \text{ is constant.}$$

From the above equation, g_m is defined as it is the ratio of a small change in drain current Δi_D to the corresponding small change in the gate to source voltage ΔV_{GS} when drain voltage V_{DS} is constant. g_m is also known as *mutual conductance*. The unit of transconductance is mho.

Drain resistance (r_d) The reciprocal of the slope of the drain characteristics is called drain resistance and it is defined by

$$r_d = \left.\frac{\partial V_{DS}}{\partial i_D}\right|_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta i_D} \quad \text{where } V_{GS} \text{ is constant.}$$

Therefore, r_d is the ratio of a small change in the drain voltage ΔV_{DS} to the corresponding small change in the drain current Δi_D while gate voltage V_{GS} held constant. The unit of r_d is ohms.

Amplification factor (μ) The amplification of JFET is defined by

$$\mu = -\left.\frac{\partial V_{DS}}{\partial V_{GS}}\right|_{V_{GS}} = -\frac{\Delta V_{DS}}{\Delta V_{GS}} \quad \text{when } i_D \text{ is constant.}$$

Actually μ is the ratio of a small change in the drain voltage ΔV_{DS} to the small change in the gate voltage ΔV_{GS} when drain current held at constant. The negative sign represents that when V_{GS} is increased, V_{DS} will be decreased at constant drain current.

Dividing both sides of Eq. (1.5) by ΔV_{GS}, we get

$$\frac{\Delta i_D}{\Delta V_{GS}} = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} + \left.\frac{\partial i_D}{\partial V_{DS}}\right|_{V_{GS}} \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Since i_D is constant, $\dfrac{\Delta i_D}{\Delta V_{GS}} = 0$

Then $0 = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} + \left.\frac{\partial i_D}{\partial V_{DS}}\right|_{V_{GS}} \frac{\Delta V_{DS}}{\Delta V_{GS}}$

After substituting the value of the partial differential coefficients, we obtain

$$0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m \text{ where } g_m = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}}, r_d = \left.\frac{\partial V_{DS}}{\partial i_D}\right|_{V_{GS}}, \text{ and } \mu = -\frac{\Delta V_{DS}}{\Delta V_{GS}}$$

or, $\mu = r_d g_m$

Therefore, the amplification factor μ is the product of drain resistance (r_d) and transconductance (g_m).

1.7 SMALL SIGNAL MODEL OF FET

The small signal model of FET is used to represent the small changes in FET current and voltages about the quiescent operating point. This model is different at low frequency and high frequency. This model is equally valid for JFET and MOSFET. In this section, low frequency model and high frequency model of FET is explained.

1.7.1 Low Frequency Model of FET

The Eq. (1.5) can be represented by

$$i_d = g_m v_{gs} + r_d v_{ds} \quad \text{where } \Delta i_D = i_d, \Delta V_{GS} = v_{gs} \text{ and } \Delta V_{DS} = v_{ds}$$

The above equation is represented by Fig. 1.25 which is the small signal low frequency model of FET. In this model, the gate-to-source junction is represented by an open circuit. Since the input resistance between gate and source is very high; about 10^8 to $10^{10}\ \Omega$, no current is drawn from the input terminal of FET. This model has a voltage controlled current source. Amplitude of current is proportional to the gate-to-source voltage as it is represented by $g_m v_{gs}$. The proportionality factor is called transconductance g_m. Usually, transconductance g_m is measured in milli-amperes per volt (mA/V) or milli siemens (mS). The typical value of g_m is about 0.1 mA/V to 10 mA/V for JFET and 0.1 mA/V to 20 mA/V for MOSFET. The output resistance is equal to drain resistance and it is represented by r_d. The typical value of r_d is about 100 kΩ to 1 MΩ for JFET and 1 kΩ to 50 kΩ for MOSFET.

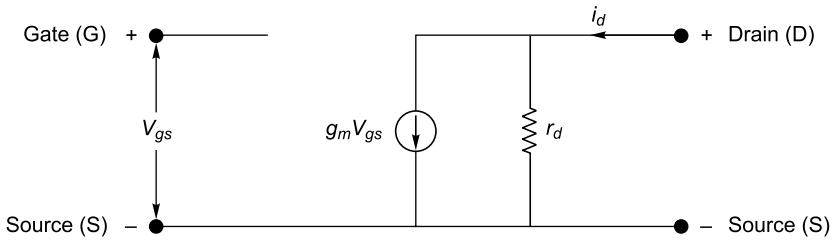


Fig. 1.25 *Small signal low frequency model of FET*

The Fig. 1.25 can be represented by the equivalent circuit as depicted in Fig. 1.26. The equivalent circuit consists of a voltage controlled voltage source in series with the drain resistance. The magnitude of voltage controlled voltage source is

$g_m r_d v_{gs} = \mu \cdot v_{gs}$ where $\mu = g_m r_d$ = amplification factor

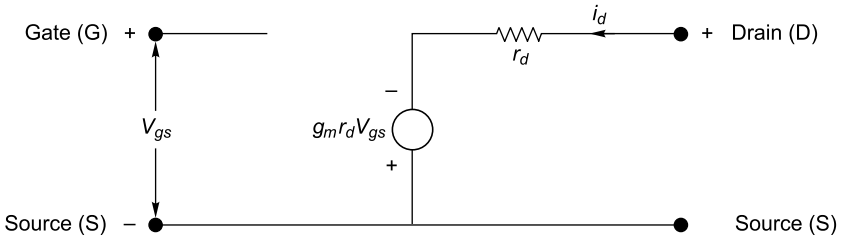


Fig. 1.26 ***Alternative small signal low frequency model of FET***

1.7.2 High Frequency Model of FET

Figure 1.27 shows the small signal high frequency model of FET. This model is identical with Fig. 1.25 except that the capacitances between each pair of terminals are incorporated. The capacitor C_{gs} represents the barrier capacitance between gate and source and its typical value is about 1 pF to 10 pF for both JFET and MOSFET. The capacitor C_{gd} represents the barrier capacitance between gate and drain and its typical value is also about 1 pF to 10 pF for both JFET and MOSFET. The C_{ds} represents the internal capacitance between drain and source and its typical value is about 0.1 pF to 1 pF for both JFET and MOSFET. The range of parameter values of a FET is given in Table 1.1.

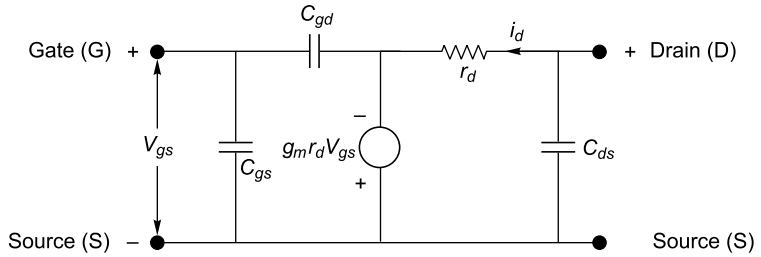


Fig. 1.27 ***Small signal high frequency model of FET***

Table 1.1 *Range of parameter values of a FET*

Parameter	*Jeet*	*Mosfet*
g_m	0.1 mA/V to 10 mA/V	0.1 mA/V to 20 mA/V
r_d	100 kΩ to 1 MΩ	1 kΩ to 50 kΩ
C_{gs}	1 pF to 10 pF	1 pF to 10 pF
C_{gd}	1 pF to 10 pF	1 pF to 10 pF
C_{ds}	0.1 pF to 1 pF	0.1 pF to 1 pF
r_{gs}	$>10^8$ Ω	$>10^{10}$ Ω
r_{gd}	$>10^8$ Ω	$>10^{14}$ Ω

1.8 COMPARISON BETWEEN FET AND BJT

The comparison between field effect transistor (FET) and bipolar junction transistor (BJT) is given in Table 1.2.

Table 1.2 *Comparison between FET and BJT*

Field Effect Transistor (FET)	*Bipolar Junction Transistor (BJT)*
FET is unipolar device as current flows through the device due to either electrons or holes.	BJT is bipolar device as current flows through the device due to both electrons and holes.
FET is a majority device.	BJT is a minority device.
FET is voltage controlled device.	BJT is current controlled device.
Input resistance of FET is very high and its value is about Mega-ohms.	Input resistance of BJT is very low compared to FET and its value is about few kilo-ohms.
This device has negative temperature coefficient. Therefore, the current decreases with increasing temperature. This characteristic prevents FET from thermal breakdown.	This device has positive temperature coefficient. Therefore, the current increases with increasing temperature. This characteristic leads BJT to thermal breakdown.
Since minority carrier storage effects do not exist in FET, this device operates at high switching speed and cut-off frequency.	Since minority carrier storage effects exist in BJT, this device operates at low switching speed and cut-off frequency.
As FET is less noisy compared to BJT, this device is also suitable for amplifier at low level signals.	BJT is more noisy compared to FET.
FET requires less space to fabricate integrated circuit (IC). It is comparative simpler to fabricate IC using FET.	BJT requires more space to fabricate integrated circuit(IC). It is comparative difficult to fabricate IC using FET.

1.9 COMPARISON BETWEEN *n*-CHANNEL FET AND *p*-CHANNEL FET

The comparison between *n*-channel JFET and *p*-channel JFET are given in Table 1.3.

Table 1.3 *Comparison between n-channel JFET and p-channel JFET*

n-channel JFET	*p-channel JFET*
In an *n*-channel JFET, the current carriers are electrons.	In a *p*-channel JFET, the current carriers are holes.
Mobility of electrons is large in *n*-channel JFET.	Mobility of holes is poor in *p*-channel JFET.
The input noise is less in an *n*-channel JFET.	The input noise is more in a *p*-channel JFET.
The transconductance is larger in *n*-channel JFET than that of *p*-channel JFET.	The transconductance is smaller in *p*-channel JFET than that of *n*-channel JFET.

1.10 APPLICATIONS OF JFET

The applications of field effect transistors (FET) are given below:

(i) As FET is a voltage controlled device, it can be used as a voltage variable resistance in operational amplifier circuits.
(ii) Since the coupling capacitor is small, FET can be used in low frequency amplifiers.
(iii) FET can be used a buffer in different measuring instruments as this device has high input impedance and low output impedance.
(iv) As the input capacitance is low, FET can be used in cascade amplifiers in different instruments.
(v) Frequency drift of FET is low and this device can be used in oscillator circuits.
(vi) FETs are used in mixer circuits in FM and TV receiver.
(vii) FETs can be used in different communication equipments for low noise level.
(viii) FET can used to manufacture integrated circuits (ICs), and memory circuits.

1.1 If a reverse gate voltage of 10 V is applied and the gate current is 10 nA, find the resistance between gate and source.

Solution

Given $V_{GS} = 10$ V, and $I_G = 10$ nA

The gate to source resistance is equal to $\frac{V_{GS}}{I_G} = \frac{10}{10 \times 10^{-9}} = 1000\ \text{M}\Omega$.

1.2 In an n-channel JFET, $a = 3.5 \times 10^{-4}$ cm and $N_D = 10^{21}$ electrons/cm^3, determine (a) the pinch-off voltage and (b) the channel width at $V_{GS} = \frac{V_P}{2}$ and $I_D = 0$. Assume $\varepsilon = 10\varepsilon_o$.

Solution

Given $a = 3.5 \times 10^{-4}$ cm, $N_D = 10^{21}$ electrons/cm^3

(a) The pinch-off voltage is $|V_P| = \frac{qN_D}{2\varepsilon}a^2 = \frac{1.6 \times 10^{-19} \times 10^{21} \times (3.5 \times 10^{-6})^2}{2 \times 10 \times (36 \times \pi \times 10^9)^{-1}}$ V

$= 11.08$ V

(b) We know that $b(x) = a\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right] = 3.5 \times 10^{-4}\left[1 - \left(\frac{1}{2}\right)^{\frac{1}{2}}\right]$ cm

$= 1.025 \times 10^{-4}$ cm.

1.3 Assume that the reverse gate voltage of JFET changes from 5.0 V to 4.9 V and the drain current changes from 1.2 mA to 1.5 mA. What is the value of transconductance?

Solution

Given $\Delta V_{GS} = 5 - 4.9 = 0.1$ V, and $\Delta I_D = 1.5 - 1.2 = 0.3$ mA

The value of transconductance is equal to $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{0.3 \times 10^{-3}}{0.1} = 3$ m.mho.

1.4 The drain current of a JFET is about 5 mA. When I_{DSS} is equal to 10 mA, $V_{GS(off)} = V_P = -5$ V, determine the value of V_{GS}.

Solution

Given $I_D = 5$ mA, $I_{DSS} = 10$ mA, and $V_{GS(off)} = V_P = -5$ V

We know that $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

or, $$5 \times 10^{-3} = 10 \times 10^{-3}\left(1 + \frac{V_{GS}}{5}\right)^2$$

or, $$\left(1 + \frac{V_{GS}}{5}\right)^2 = \frac{5}{10} = 0.5 \quad \text{or} \quad 1 + \frac{V_{GS}}{5} = 0.707$$

or, $$V_{GS} = -1.464\ V$$

The value of transconductance is equal to $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{0.3 \times 10^{-3}}{0.1} = 3$ m.mho.

1.5 In an *n*-channel JFET, I_{DS} is 6 mA and $V_P = -6$ V. Find the minimum value of V_{DS} for pinch-off operation. Determine the value of drain current at $V_{GS} = -3$ V.

Solution

Given $I_{DSS} = 6$ mA, and $V_P = -6$ V

The minimum value of V_{DS} for pinch-off operation is

$$V_{DS(\text{minimum})} = V_{GS} - V_P = -3 - (-6) = 3 \text{ V}$$

We know that $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 6 \times 10^{-3}\left(1 - \frac{(-3)}{(-6)}\right)^2 = 1.5 \text{ mA}.$$

1.6 In an *n*-channel FET has the following parameters,

$$I_{DSS} = 12 \text{ mA}, V_P = -8 \text{ V and } g_{mo} = 4000 \text{ μs}$$

Determine the drain current and transconductance at $V_{GS} = -5$ V

Solution

Given $I_{DSS} = 12$ mA, $V_P = -8$ V, $g_{mo} = 4000$ μs and $V_{GS} = -5$ V

The drain current is equal to $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 = 12 \times 10^{-3}\left(1 - \dfrac{(-5)}{(-8)}\right)^2 = 1.68$ mA

The transconductance is $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = 4000\left(1 - \frac{(-5)}{(-8)}\right)\mu s = 1500\ \mu s.$

1.11 METAL OXIDE SEMICONDUCTOR (MOS) FIELD EFFECT TRANSISTOR OR MOSFET

The Metal Oxide Semiconductor (MOS) Field Effect Transistor or MOSFET was introduced in 1970s. The MOSFET has many advantages such as

- It requires very small area on an integrated circuit (IC)
- Digital circuits can be designed using MOSFET only
- High-density VLSI circuits such as microprocessors, microcontrollers and memory ICs can be manufactured using MOSFET
- MOSFET can be used in analog circuits as switching device and amplifier

In MOSFET, field effect principle is used for proper operation of this device. In this device, the current is controlled by an applied electric field perpendicular to both the semiconductor surface and to the current direction. The operating principle of MOSFET can be explained by the basic MOS capacitor as depicted in Fig. 1.28.

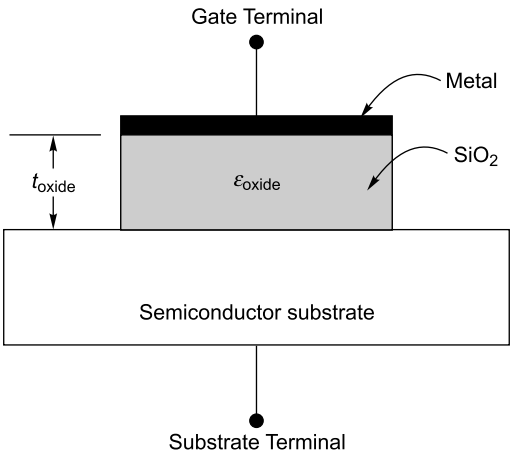


Fig. 1.28 ***Structure of basic MOS capacitor***

1.12 MOS CAPACITOR

The structure of basic MOS capacitor is shown in Fig. 1.28. Usually aluminum (Al) metal is used in MOSFET. Silicon dioxide SiO_2 is used in oxide layer and t_{oxide} is the thickness of the oxide and ε_{oxide} is the oxide permittivity. The operation of the MOS structure can be explained with the help of a simple parallel plate capacitor. Figure 1.29 shows a parallel plate capacitor where the top plate is connected with negative terminal of a voltage source with respect to bottom plate. Insulating materials are placed with in two plates to separate two plates. Then a negative

charge exists on the top plate and a positive charge exists on the bottom plate. Consequently, an electric field is developed between two plates as depicted in Fig. 1.29.

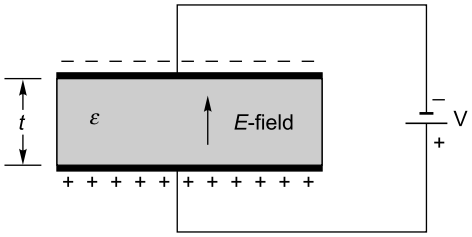


Fig. 1.29 *A parallel-plate capacitor showing the electric field and charges*

Figure 1.30 shows a MOS capacitor with a *p*-type substrate. The top metal is connected to the negative terminal of supply voltage with respect to substrate and it is called *gate*. Since a negative charge exists on the top metal plate, an electric field will be induced as shown in Fig. 1.30. When the induced electric field penetrates the semiconductor, the holes in the *p*-type semiconductor get a force towards the oxide semiconductor interface. Therefore, positively charged holes will be accumulated at the oxide-semiconductor interface corresponding to the positive charge on the bottom plate of MOS capacitor as shown in Fig. 1.31.

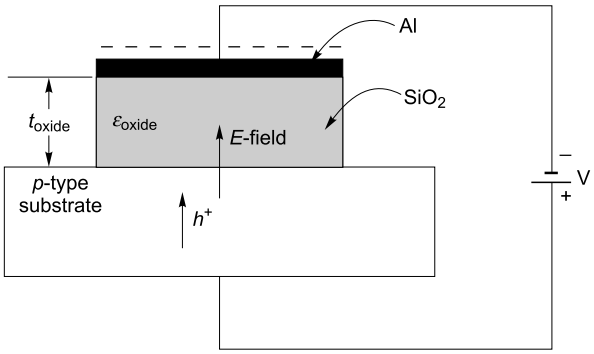


Fig. 1.30 *MOS capacitor with negative voltage at gate, showing the electric field and holes flow*

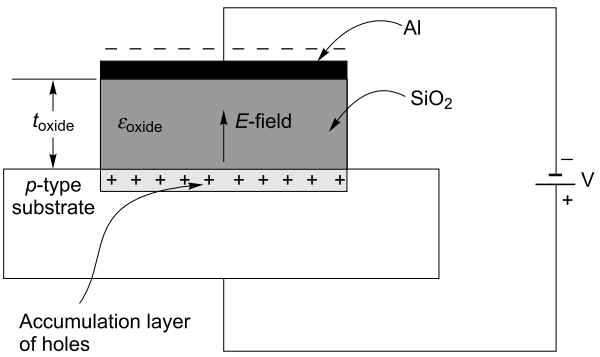


Fig. 1.31 *MOS capacitor with an accumulation layer of holes*

If the polarity of the applied voltage of a MOS capacitor is reversed, a positive charge exists on the top metal plate and induced electric field will be in opposite direction as depicted in Fig. 1.32(a). As the electric field penetrates the semiconductor, hole in the *p*-type material get a force away from the oxide-semiconductor interface. Since the holes are pushed away from the interface, a negative charge is induced in the *p*-type substrate as shown in Fig. 1.32(b). If a large positive voltage is applied to the gate, the induced electric field increases. As minority carrier electrons are attracted to the oxide-semiconductor interface, a region of minority carrier electrons accumulated near oxide-semiconductor interface and this region is called an *electron inversion layer* as depicted in Fig. 1.32(b).

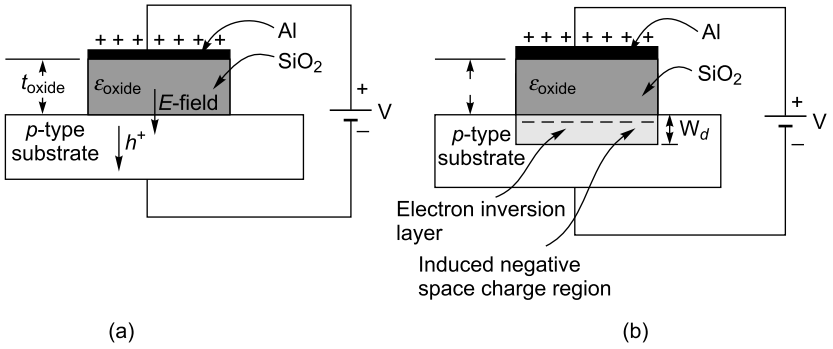


Fig. 1.32 ***(a) A MOS capacitor with p-type substrate showing electric field and holes flow for positive gate bias (b) MOS capacitor with an induced negative space charge region and electron inversion layer due to positive gate bias***

Figure 1.33 shows the charge distribution in a MOS capacitor with an *n*-type substrate. A positive voltage is applied to the top gate terminal, and then an accumulation layer of electrons is induced in the *n*-type substrate.

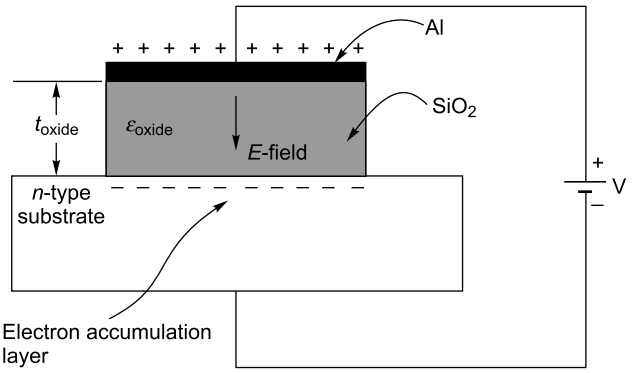


Fig. 1.33 ***A MOS capacitor with n-type substrate showing electric field and an electron accumulation layer for positive gate bias***

Figure 1.34(a) shows the MOS capacitor with an induced space-charge region due to a moderate negative gate bias. Since a negative voltage is applied to the

gate terminal, a positive space charge region is induced in the *n*-type substrate due to induced electric field. If a large negative voltage is applied, a region of positive charges (holes) accumulated near oxide-semiconductor interface and this region is called an *hole inversion layer* as depicted in Fig. 1.34(b). The magnitude of positive charges in the inversion layer is increased with increasing applied gate voltage.

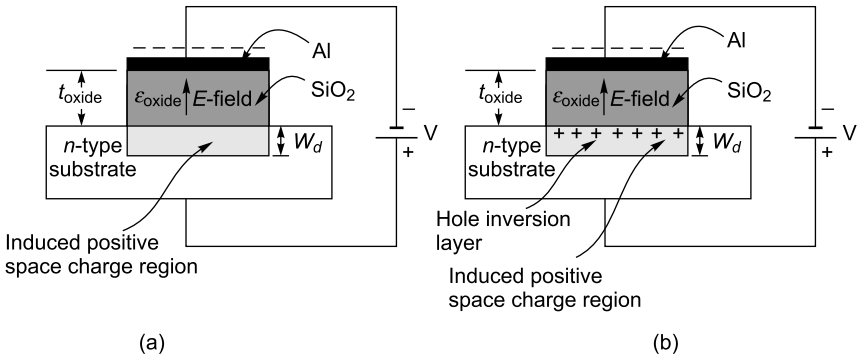


Fig. 1.34 ***(a) A MOS capacitor with an induced space charge region (b) A MOS capacitor with induced space charge region and hole inversion layer for large negative gate bias***

The term enhancement mode states that a voltage applied to MOS capacitor and correspondingly an inversion layer is induced. When the MOS capacitor has *p*-type substrate, a positive gate voltage is applied to create the electron inversion layer as shown in Fig. 1.32(a). If the MOS capacitor has *n*-type substrate, a negative gate voltage is applied to create the hole inversion layer as depicted in Fig. 1.34(b).

1.13 *n*-CHANNEL ENHANCEMENT MOSFET

There are two types of MOSFET such as depletion-type MOSFET and enhancement-type MOSFET. Again, each type of MOSFET is classified as *n*-channel and *p*-channel MOSFET. In this section, the structure and operation of depletion-type MOSFET and enhancement-type MOSFET are discussed in detail.

Figure 1.35 shows the simplified structure of an *n*-channel enhancement-type MOSFET which consists of a lightly doped *p*-type substrate and two n^+ regions. Actually, two highly doped n^+ regions are diffused within the *p*-type substrate. These n^+ type regions are separated by about 1 μm to 20 μm and act as source (S) and drain (D) terminal, respectively. A thin layer of silicon dioxide, SiO_2 is placed over the surface of the structure. Then holes are cut into the SiO_2 layer and metal contacts are inserted into holes to make the source and drain terminals as shown in Fig. 1.35. The metal contact over the channel region is used as gate terminal. The gate, oxide and *p*-type substrate behave as a MOS capacitor. In Fig. 1.35, L is the channel length and its typical value is about 1 μm to 20 μm. The thickness of oxide t_{oxide} is in the order of 400 angstroms. Figure 1.36 shows the detail cross section of an *n*-channel MOSFET showing field oxide and gate oxide.

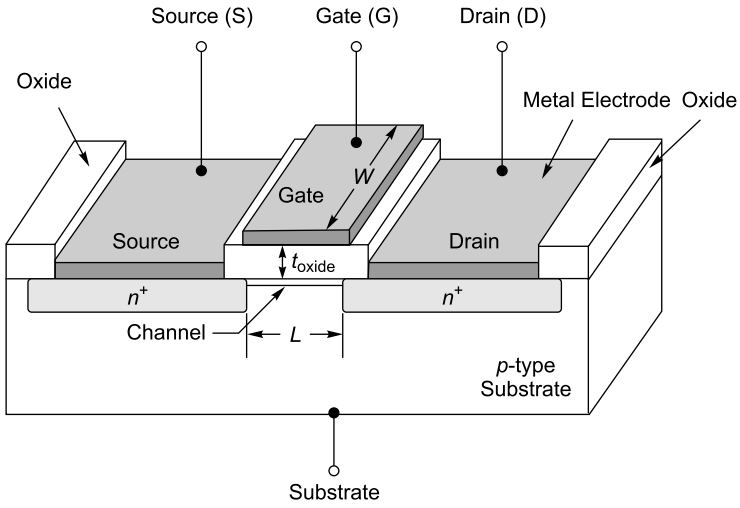


Fig. 1.35 *Schematic diagram of an n-channel enhancement type MOSFET*

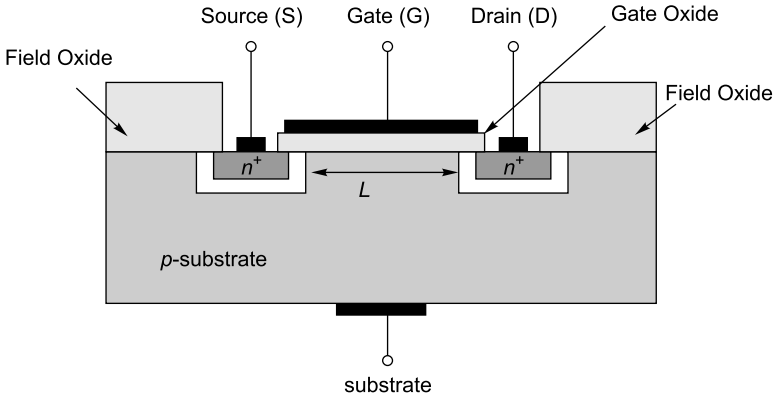


Fig. 1.36 *An n-channel MOSFET showing field oxide and gate oxide*

1.13.1 Operation of *N*-Channel Enhancement MOSFET

When zero biasing is applied to the gate, the source and drain terminals are separated by the *p*-type region as depicted in Fig. 1.37(a). Figure 1.37(a) is equivalent to two back to back pn^+ junction diodes as shown in Fig. 1.37(b). Therefore, the current flow through the device is zero. When the large positive gate voltage is applied between gate to source, an electron inversion layer will be developed at the oxide semiconductor interface and this electron inversion layer can be used interconnect the n^+ source and n^+ drain as shown in Fig. 1.38. As a result, current can flows between sources and drain terminals. With the increase of gate voltage, the width of electron inversion layer increases and more current flows between sources and drain. Consequently, this transistor is called enhancement-type MOSFET. Since the carriers in the inversion layer are electrons, this transistor is known as *n*-channel MOSFET or NMOS.

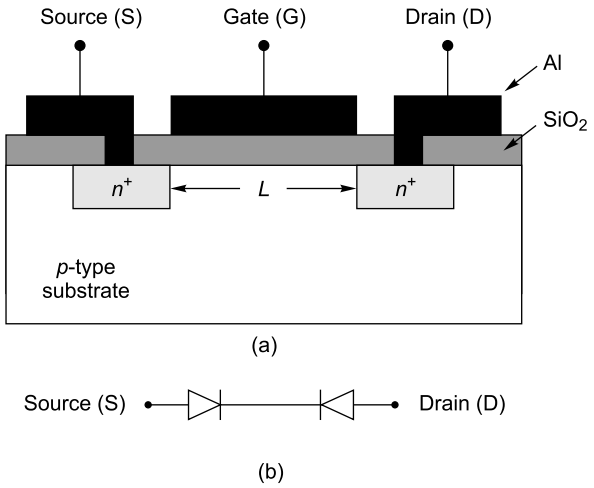


Fig. 1.37 (a) An n-channel MOSFET with zero voltage gate biased (VGS = 0) (b) equivalent circuit of Fig. 1.37(a)

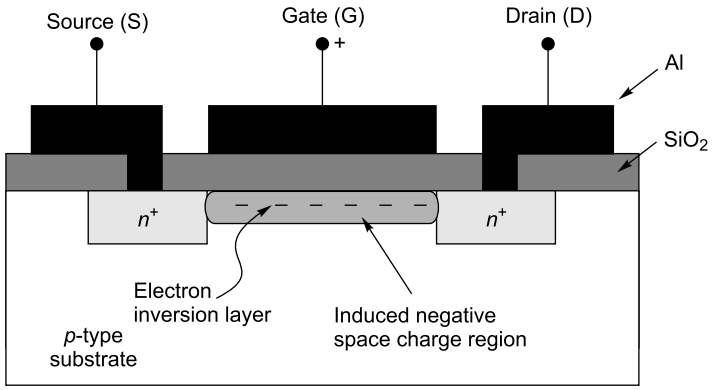


Fig. 1.38 An n-channel MOSFET with positive gate biased with electron inversion layer and induced negative space charge region

1.13.2 Drain Characteristics of *n*-Channel Enhancement MOSFET

The threshold voltage of an *n*-channel MOSFET is represented by V_{TN}. When the threshold voltage V_{TN} is applied to gate, an inversion layer of negative charges is created. The density of charge is equal to the concentration of majority carriers in the semiconductor substrate. Therefore, the threshold voltage is the gate voltage which is required to turn on the MOSFET.

In an *n*-channel enhancement type MOSFET, threshold voltage is positive as a positive gate voltage is required to generate the inversion layer. When the gate voltage is less than the threshold voltage, current in the device is about zero. If the gate voltage is greater than the threshold voltage, current flow from drain to source as the drain-to-source voltage is applied.

When the *p*-type substrate of the *n*-channel MOSFET is grounded, gate voltage is above V_{TN} and a small drain-to-source V_{DS} voltage is applied. Figure 1.39(a) shows the simplified representation of MOSFET. It is clear from Fig. 1.39(a) that the thickness of the inversion channel layer is constant along the entire channel length. Figure 1.39(b) shows the plot of drain current i_D with respect to V_{DS}.

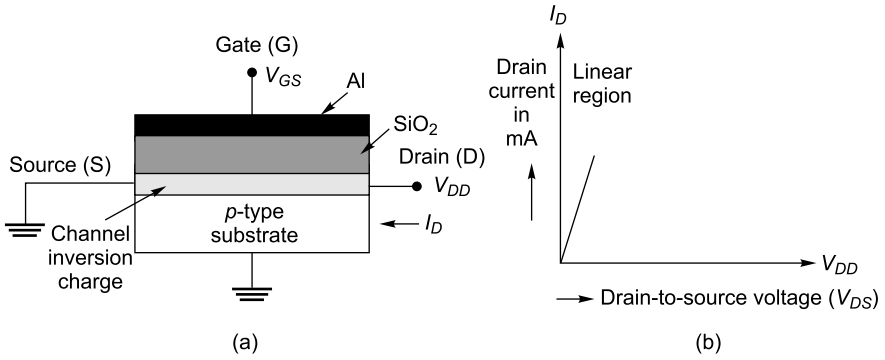


Fig. 1.39 ***(a) An n-channel MOSFET with channel inversion charge when $V_{GS} > V_{TN}$ and small V_{DS} (b) Drain current i_D vs V_{DS} for $V_{GS} > V_{TN}$***

When drain voltage increases, the voltage drop across the oxide near the drain terminals decreases. Consequently, the induced inversion charge density near the drain decreases. Then conductance of the channel at the drain decreases. Figure 1.40(a) shows the channel inversion charge when drain voltage increases and the i_D vs V_{DS} curve is depicted in Fig. 1.40(b).

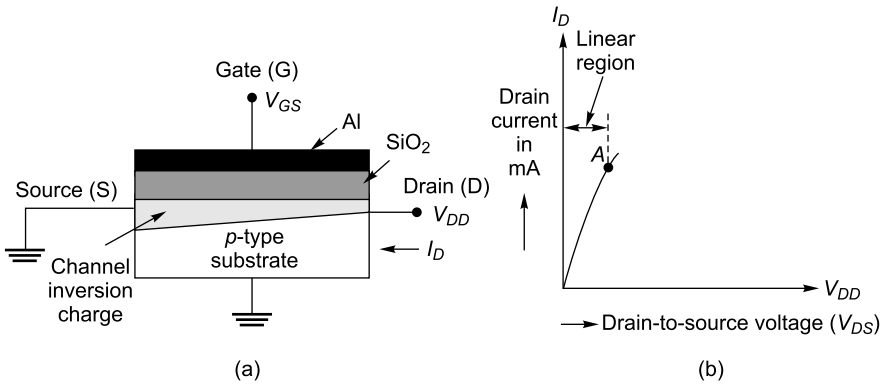


Fig. 1.40 ***(a) An n-channel MOSFET with channel inversion charge when $V_{GS} > V_{TN}$ and large value of V_{DS} (b) Drain current i_D vs V_{DS} for $V_{GS} > V_{TN}$ and large value of V_{DS}***

Due to increase of V_{DS}, the potential difference $V_{GS} - V_{DS}$ across the oxide is equal to V_{TN} at drain terminal. Then induced inversion charge density at the drain terminal is about zero as shown in Fig. 1.41(a). In this condition, the channel conductance at the drain terminal is zero and the slope of i_D vs V_{DS} curve becomes

zero. The drain current i_D vs V_{DS} is depicted in Fig. 1.41(b) when $V_{GS} > V_{TN}$ and $V_{DS} = V_{DS(\text{saturation})}$. The relationship between V_{GS}, $V_{DS(\text{saturation})}$ and V_{TN} is

$$V_{GS} - V_{DS(\text{saturation})} = V_{TN}$$

Therefore,

$$V_{DS(\text{saturation})} = V_{GS} - V_{TN}$$

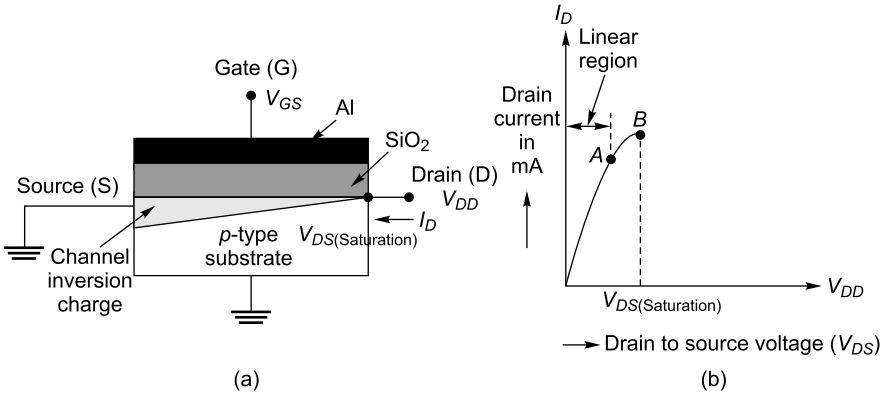


Fig. 1.41 ***(a) An n-channel MOSFET with channel inversion charge when $V_{GS} > V_{TN}$ and $V_{DS} = V_{DS(saturation)}$ (b) Drain current i_D vs V_{DS} for $V_{GS} > V_{TN}$ and $V_{DS} = V_{DS(saturation)}$***

If V_{DS} is greater than $V_{DS(\text{saturation})}$, the point at which the inversion charge is about zero moves towards the source terminal. In this condition, electrons enter from source, move through the channel toward the drain terminal as depicted in Fig. 1.42(a). Then at the point where the inversion charge becomes zero, electrons are injected into the space charge region and they are swept by the electric field to the drain. As a result the drain current is constant for $V_{DS} > V_{DS(\text{saturation})}$. The i_D vs V_{DS} characteristic is shown in Fig. 1.42(b).

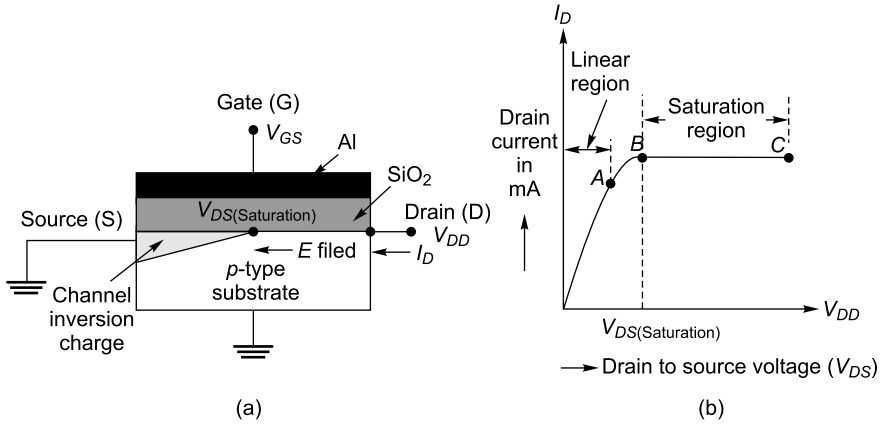


Fig. 1.42 ***(a) An n-channel MOSFET with channel inversion charge when $V_{GS} > V_{TN}$ and $V_{DS} > V_{DS(saturation)}$ (b) Drain current i_D vs V_{DS} for $V_{GS} > V_{TN}$ and $V_{DS} > V_{DS(saturation)}$***

The cross section of an *n*-channel enhancement type MOSFET when biasing with V_{GS} and V_{DS} is shown in Fig. 1.43. When the *p*-type substrate of the *n*-channel MOSFET is grounded and a positive voltage is applied across gate to source, an electric field will be generated perpendicularly through silicon dioxide. This field induced negative charges in the *p*-type substrate. These negative charges are minority carriers in the *p*-type substrate and develop an inversion layer. With the increase of gate to source voltage, the induced positive charges in the *n*-type substrate increases. Due to induced channel, the conductivity of semiconductor increases and current flows from source to drain through the induced channel.

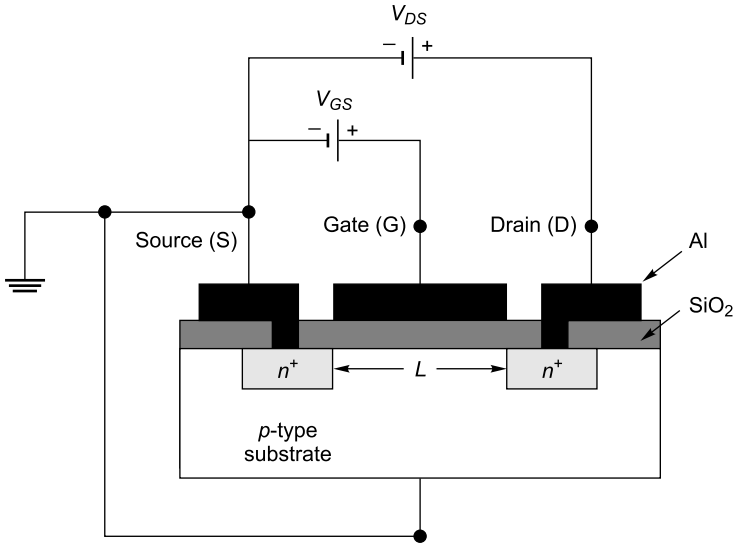


Fig. 1.43 ***Cross section of n-channel enhancement type MOSFET when biasing with V_{GS} and V_{DS}***

With increasing gate-to-source voltage V_{GS}, the drain current I_D increases gradually. If gate-to-source voltage is less than threshold voltage, there is no drain current. If V_{GS} is very small, the drain current I_D will be in few nano-amperes. With increasing gate voltage V_{GS}, the drain current I_D increases gradually. When the value of V_{GS} is grater than threshold voltage, drain current I_D increases rapidly. Figure 1.44 shows the plot of i_D vs V_{DS} for small value of V_{DS} at different V_{GS}. It is clear from Fig. 1.44 the slope of i_D vs V_{DS} increases with increasing V_{GS}. Since $V_{DS(\text{saturation})}$ is a function of V_{GS}, we can get a family of curves for an *n*-channel enhancement type MOSFET as shown in Fig. 1.45. The drain characteristics of an *n*-channel enhancement type MOSFET is divided into non-saturation and saturation regions as depicted in Fig. 1.45.

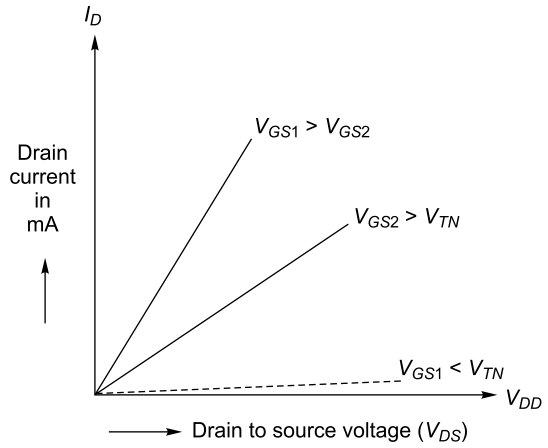


Fig. 1.44 *Plot of i_D vs V_{DS} increase with increasing V_{GS}*

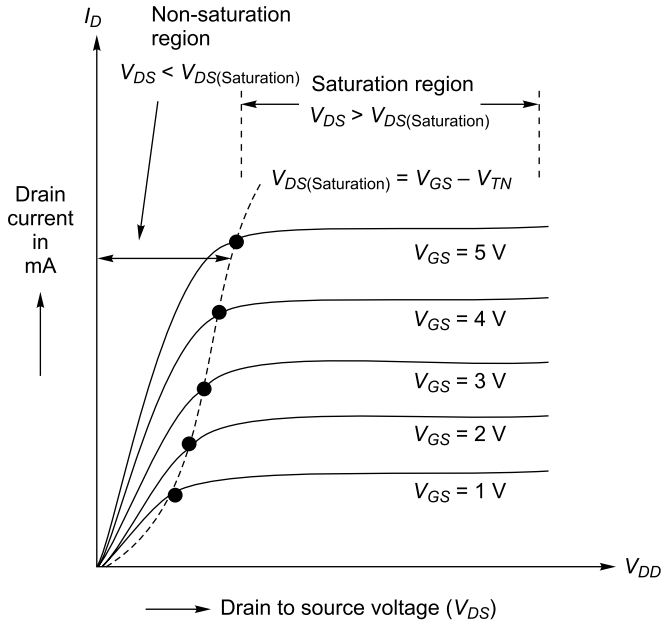


Fig. 1.45 *Drain characteristics of n-channel enhancement type MOSFET*

In Fig. 1.45, the region for which $V_{DS} < V_{DS(\text{saturation})}$ is called non-saturation region. The drain current –voltage characteristics in this region can be expressed as

$$i_D = K_N [2 V_{GS} - V_{TN}] V_{DS} - V_{DS}^2 \text{ where, } K_N \text{ is constant}$$

In the saturation region, the drain to source voltage is grater than $V_{DS\,(\text{saturation})}$ ($V_{DS} > V_{DS(\text{saturation})}$), the drain current –voltage characteristics can be expressed by

$$i_D = K_N\,[V_{GS} - V_{TN}]^2$$

1.13.3 Transfer Characteristics of *n*-Channel Enhancement MOSFET

Figure 1.46 shows the transfer characteristics of *n*-channel enhancement type MOSFET. It is depicted in Fig. 1.46 that there is no drain current if gate to source voltage $V_{GS} = 0$. When V_{GS} is increased about the threshold voltage $V_{GS\,(\text{th})}$, the drain current increases very rapidly. The transfer characteristics curve follows the equation:

$$i_D = K_N\,[V_{GS} - V_{GS\,(\text{th})}]^2 = K_N\,[V_{GS} - V_{TN}]^2 \text{ where, } K_N \text{ is constant}$$

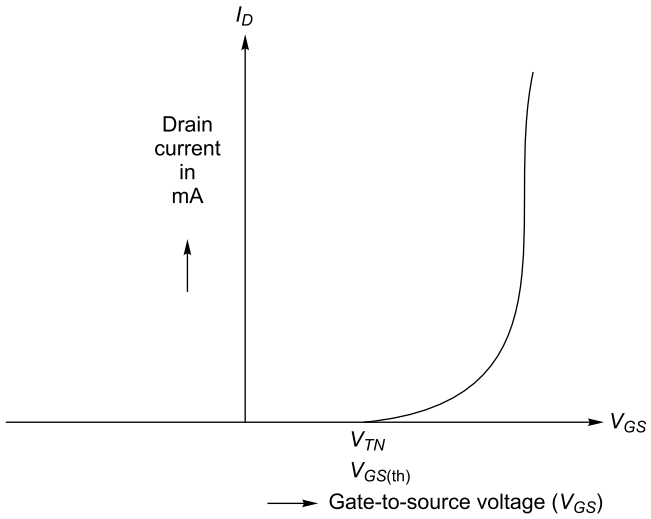


Fig. 1.46 ***Transfer characteristics of n-channel enhancement type MOSFET***

1.14 *p*-CHANNEL ENHANCEMENT MOSFET

Figure 1.47 shows the simplified structure of a *p*-channel enhancement-type MOSFET which consists of a lightly doped *n*-type substrate and two p^+ regions. In reality, two highly doped p^+ regions are diffused with in the *n*-type substrate. These p^+ type regions are separated by about 1 μm to 20 μm and work as source (S) and drain (D) terminals, respectively. The metal contact over the channel region is used as gate terminal. The gate, oxide and *n*-type substrate behave as a MOS capacitor. In Fig. 1.48, *L* is the channel length and its typical value is about 1 μm to 20 μm. The thickness of oxide t_{oxide} is in the order of 400 angstroms. Figure 1.48 shows the detail cross section of a *p*-channel MOSFET showing oxide and biasing arrangement.

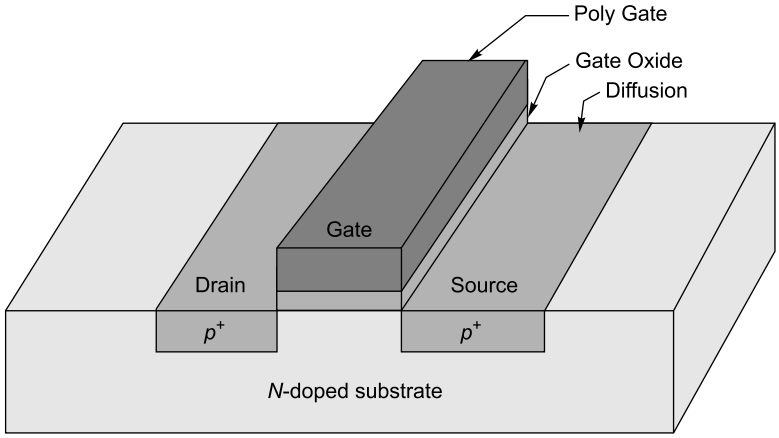


Fig. 1.47 *p-channel enhancement-type MOSFET*

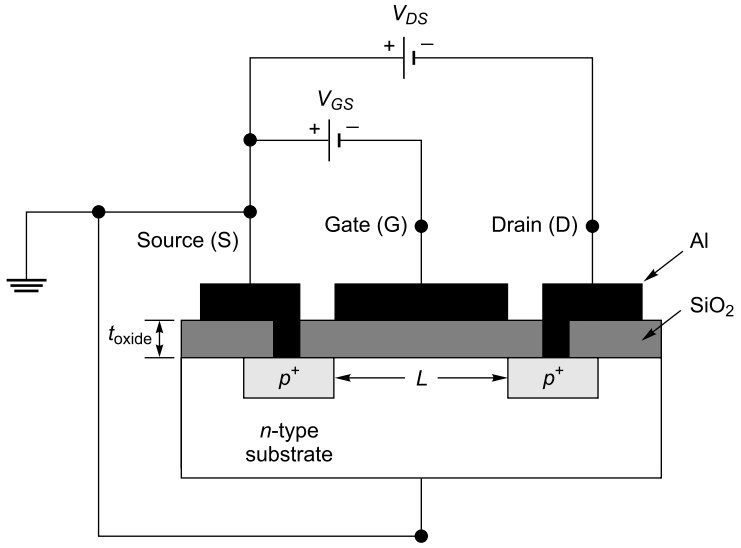


Fig. 1.48 *Cross section of p-channel enhancement type MOSFET*

1.14.1 Operation of *p*-Channel Enhancement MOSFET

The operation of the *p*-channel enhancement type MOSFET is same as *n*-channel enhancement type MOSFET, but hole is used as the charge carrier in place of electrons. A negative gate bias can able to induce an inversion layer of positive charges (holes) in the channel. The threshold voltage of *p*-channel enhancement type MOSFET is represented by V_{TP}. When the gate voltage is equal to the threshold voltage, an inversion layer is induced in the channel. Since the inversion layer is induced, the p^+ type source region is used as source of the charge carrier and holes flow from source to drain. If a negative drain voltage is applied, an electric field is developed in the channel which forcing the holes to move holes

from source to drain. The *p*-channel enhancement type MOSFET is known as PMOS transistor. The direction of drain current and voltage polarity of PMOS are reverse of NMOS.

The drain characteristics of *p*-channel enhancement type MOSFET are same as those shown in Fig. 1.45, but the drain current direction is out of drain and V_{DS} must be replaced by V_{SD}. At saturation point, $V_{SD(\text{saturation})} = V_{SG} + V_{TP}$. In the non-saturation region, the drain current can be expressed as

$$i_D = K\,[2V_{SG} + V_{TP}]\,V_{SD} - V_{SD}^2$$

In the saturation region, the drain current–voltage characteristics can be expressed by

$$i_D = K\,[V_{SG} + V_{TP}]^2$$

The drain characteristics and transfer characteristics of a *p*-channel enhancement MOSFET are given in Fig. 1.49(a) and (b), respectively.

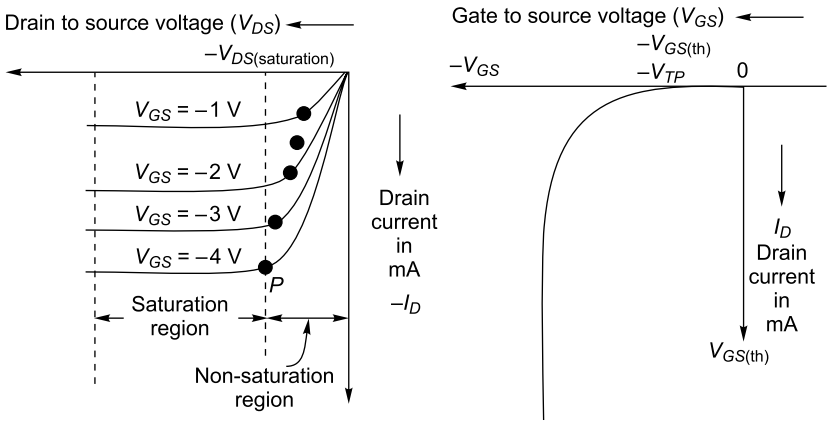


Fig. 1.49 ***(a) Drain characteristics and (b) Transfer characteristics of p-channel enhancement MOSFET***

1.15 *n*-CHANNEL DEPLETION TYPE MOSFET

Figure 1.50 shows an *n*-channel depletion type MOSFET. If zero voltage is applied to the gate ($V_{GS} = 0$), an *n*-channel region or an inversion layer present under the oxide as shown in Fig. 1.50. As the thin *n*-channel interconnects the n^+ type source and n^+ type drain, a drain-to-source current (I_D) flows even though the gate voltage is equal to zero. The term *depletion* means that the channel exists even at zero gate voltage. When a negative gate voltage is applied to the *n*-channel depletion type MOSFET, the device will be turned off.

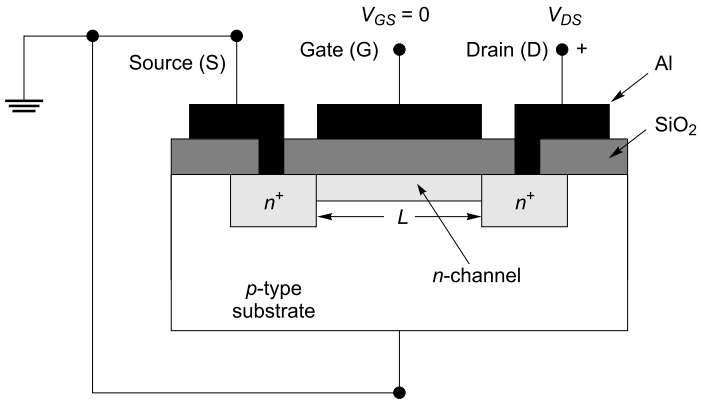


Fig. 1.50 *Cross section of an n-channel depletion MOSFET with* $V_{GS} = 0$

Figure 1.51 shows an *n*-channel depletion type MOSFET with negative gate voltage ($V_{GS} < 0$). Due to negative gate voltage, a space charge region is induced under the oxide. Hence, the thickness of *n*-channel region will be reduced. As the

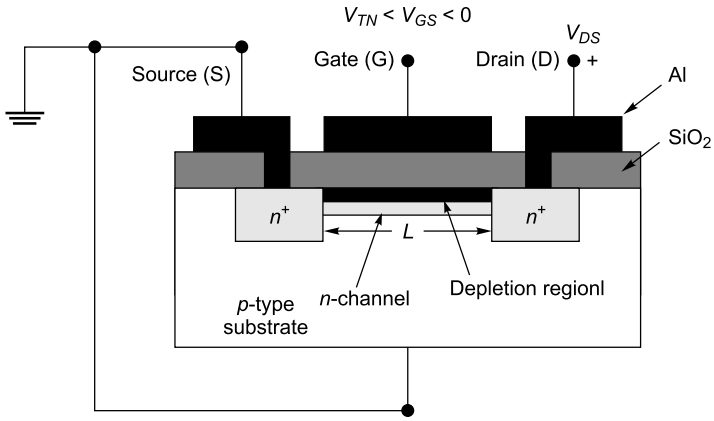


Fig. 1.51 *Cross section of an n-channel depletion MOSFET with* $V_{TN} < V_{GS} < 0$

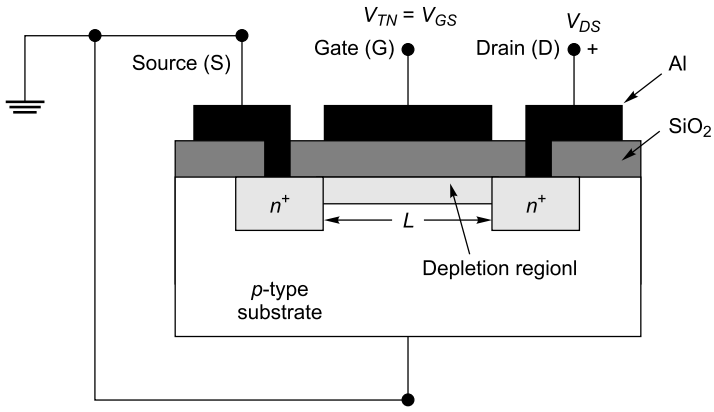


Fig. 1.52 *Cross section of an n-channel depletion MOSFET with* $V_{GS} = V_{TN}$

channel thickness is reduced, the channel conductance is also reduced and in turn drain current reduces. When the gate voltage is equal to the threshold voltage (V_{TN}), the induced space charge or depletion region extends completely through the *n*-channel region and drain current becomes zero as depicted in Fig. 1.52.

When a positive gate voltage is applied between gate to source ($V_{GS} > 0$), this positive gate voltage generates an electron accumulation layer as shown in Fig. 1.53. Due to accumulation of electrons in the *n*-type channel, drain current increases. The drain characteristics (i_D vs V_{DS} curves) of *n*-channel depletion MOSFET is depicted in Fig. 1.54. When the gate voltage is greater than zero ($V_{GS} > 0$), *n*-channel depletion MOSFET operates in enhancement mode. If the gate voltage is less than zero ($V_{GS} < 0$), *n*-channel depletion MOSFET operates in depletion mode.

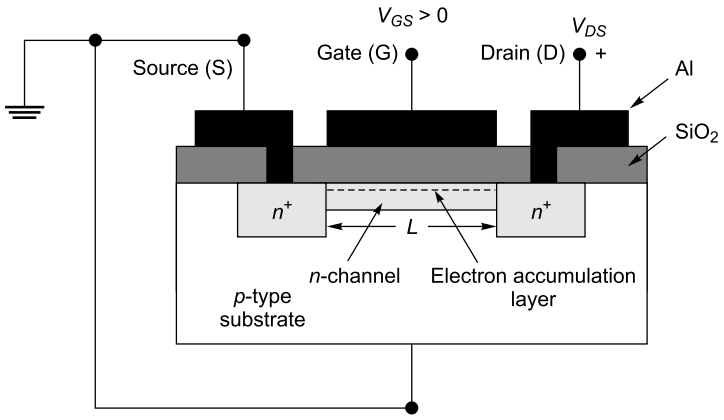


Fig. 1.53 ***Cross section of an n-channel depletion MOSFET with $V_{GS} > 0$***

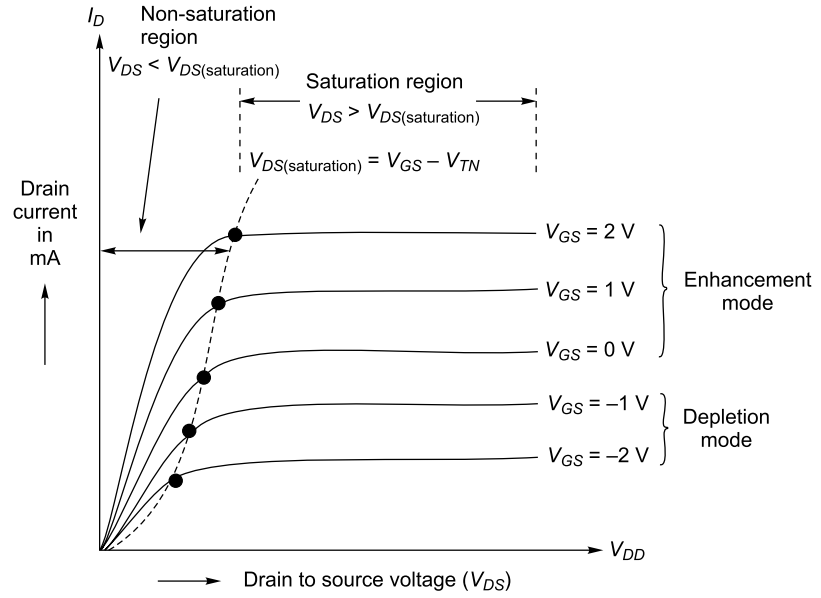


Fig. 1.54 ***Drain characteristics of n-channel depletion type MOSFET***

1.16 *p*-CHANNEL DEPLETION TYPE MOSFET

Figure 1.55 shows a *p*-channel depletion type MOSFET. When zero voltage is applied to the gate, a *p*-channel or an inversion layer of holes exist under the oxide. Since the *p*-channel interconnects the p^+ type source and p^+ type drain, a drain to source current flows even though the gate voltage is equal to zero. The depletion states that the channel exists even at zero gate voltage. If a positive gate voltage is applied between gate to source of the *p*-channel depletion type MOSFET, the device will be turned off.

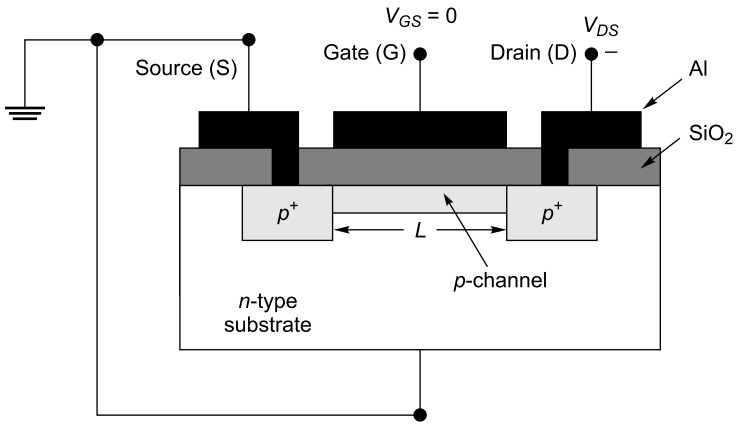


Fig. 1.55 ***Cross section of a p-channel depletion MOSFET with V_{GS} = 0***

A *p*-channel depletion type MOSFET with positive gate voltage is shown in Fig. 1.56. Due to positive gate voltage, a space charge region is induced under the oxide. Consequently, the thickness of *p*-channel region will be reduced. Since the channel thickness is reduced, the channel conductance is also reduced and in turn drain current reduces. If positive gate voltage is equal to the threshold voltage (V_{TP}), the induced space charge region extends completely through the *p*-channel region and drain current becomes zero.

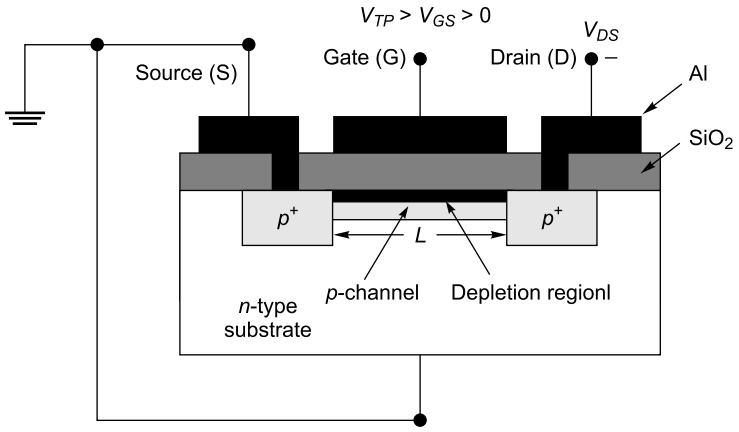


Fig. 1.56 ***Cross section of a p-channel depletion MOSFET with $V_{TP} > V_{GS} > 0$***

When a negative gate voltage is applied between gate to source, this negative gate voltage creates a hole accumulation layer as shown in Fig. 1.57. Due to accumulation of holes in the *p*-type channel, drain current increases. The drain characteristics (i_D vs V_{DS} curves) of *p*-channel depletion MOSFET is same as *n*-channel depletion MOSFET as depicted in Fig. 1.54, but the drain current direction is out of drain and V_{DS} must be replaced by V_{SD}. The cross section, drain or output characteristics and transfer characteristics of enhancement and depletion type MOSFETs are illustrated in Table 1.4.

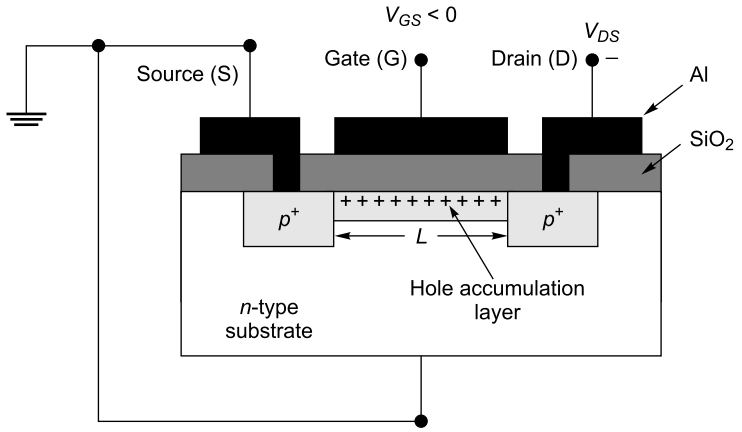
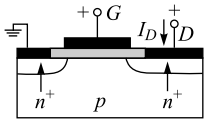
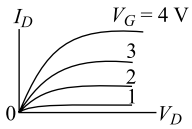
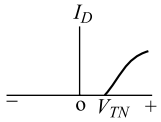
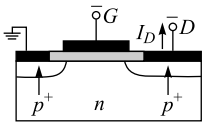
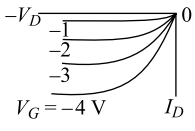
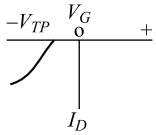
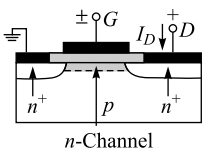
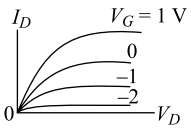
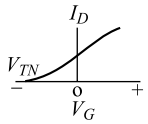
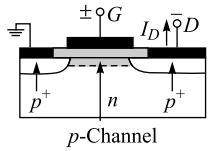
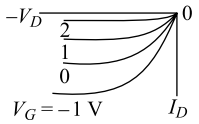
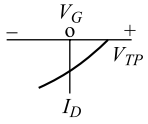


Fig. 1.57 ***Cross section of a p-channel depletion MOSFET with $V_{GS} < 0$***

Table 1.4 *Enhancement and depletion type MOSFETs*

Type	*Cross section*	*Drain or output characteristics*	*Transfer characteristics*
n-channel enhancement type MOSTFET (Normally OFF)			
p-channel enhancement type MOSTFET (Normally OFF)			
n-channel depletion type MOSTFET (Normally ON)			

Contd.

p-channel enhancement and depletion type MOSTFET (Normally ON)			

1.17 CURRENT VOLTAGE RELATIONSHIP BETWEEN *n*-CHANNEL MOSFET AND *p*-CHANNEL MOSFET

The current voltage relationship between *n*-channel MOSFET (NMOS) and *p*-channel MOSFET is given in Table 1.5.

Table 1.5 *Current-voltage relationship between NMOS and PMOS*

NMOS	*PMOS*
In non-saturation region, $V_{DS} < V_{DS\,(\text{saturation})}$ and $i_D = K_n[2V_{GS} - V_{TN}]\ V_{DS} - V_{DS}^2$.	In non-saturation region, $V_{SD} < V_{SD(\text{saturation})}$ and $i_D = K_p[2V_{SG} + V_{TP}]\ V_{SD} - V_{SD}^2$.
In saturation region, $V_{DS} > V_{DS(\text{saturation})}$ and $i_D = K_n[V_{GS} - V_{TN}]^2$.	In saturation region, $V_{SD} > V_{SD(\text{saturation})}$ and $i_D = K_p[V_{SG} + V_{TP}]^2$.
At transition point, $V_{DS(\text{saturation})} = V_{GS} - V_{TN}$.	At transition point, $V_{SD(\text{saturation})} = V_{SG} + V_{TP}$.
In enhancement mode of operation, $V_{TN} > 0$.	In enhancement mode of operation, $V_{TP} < 0$.
In depletion mode of operation, $V_{TN} < 0$.	In depletion mode of operation, $V_{TP} > 0$.

1.18 COMPARISON BETWEEN NMOS AND PMOS

The comparison between *n*-channel MOSFET (NMOS) and *p*-channel MOSFET (PMOS) is given in Table 1.6.

Table 1.6 *Comparison between NMOS and PMOS*

PMOS	*NMOS*
The *p*-channel enhancement type MOSFET is very popular as it is comparatively much easier and cheaper to manufacture the *n*-channel MOSFET.	The *n*-channel enhancement type MOSFET is less popular compared to *p*-channel enhancement type MOSFET.
The holes mobility is about 2.5 times lower than the electron mobility. Hence, *p*-channel MOSFET requires larger area than an *n*-channel MOSFET having same current rating.	The *n*-channel MOSFET requires less area than a *p*-channel MOSFET having same current rating.

Contd.

The *p*-channel MOSFET has the lower packing density and used in low and medium frequency switching applications.	The *n*-channel MOSFET has the higher packing density and used in high frequency switching applications due to smaller junction areas and lower inherent capacitance.
The *p*-channel MOSFET is bigger in size for the same complexity than *n*-channel device.	The *n*-channel MOSFET is smaller in size for the same complexity than *p*-channel device.
The drain resistance of a *p*-channel MOSFET is three times more than that of *n*-channel MOSFET having same current rating.	The drain resistance of an *n*-channel MOSFET is three times less than that of *p*-channel MOSFET having same current rating.

1.19 CIRCUIT SYMBOLS OF JFET AND MOSFET

The circuit symbols of an *n*-channel JFET and a *p*-channel JFET is shown in Fig. 1.58(a) and (b), respectively. Figure 1.59 shows the circuit symbols of *n*-channel MOSFET. Fig. 1.59(a) and (b) can be either depletion- or enhancement-types MOSFET. In Fig. 1.59(b), the substrate (G_2) is internally connected to the source. For enhancement-type MOSFET, G_2 is internally connected to *S* as shown in Fig. 1.59(c). The broken line indicates that there is no conducting channel between drain and source if $V_{GS} = 0$. Therefore, enhancement-type MOSFET is normally off MOSFET. For a *p*-channel MOSFET, the direction of arrow is reversed as depicted in Fig. 1.60.

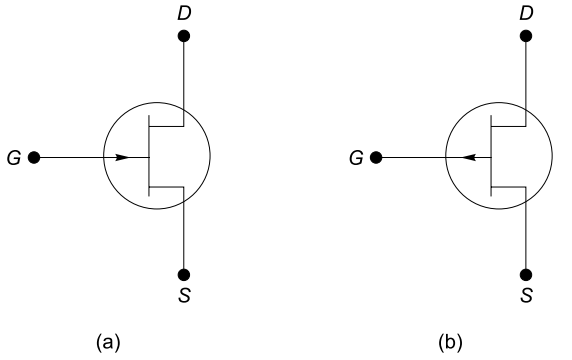


Fig. 1.58 *(a) n-channel JFET (b) p-channel JFET*

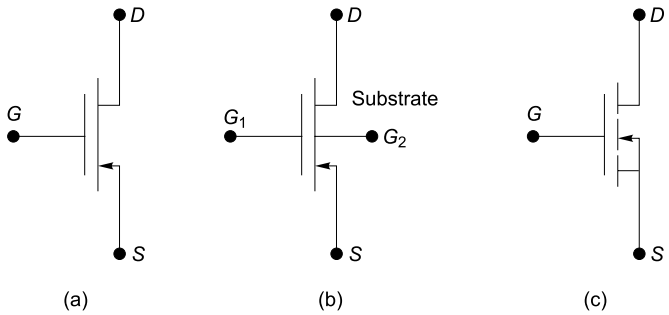


Fig. 1.59 *(a) and (b) n-channel depletion or enhancement types MOSFET (c) n-channel enhancement type MOSFET*

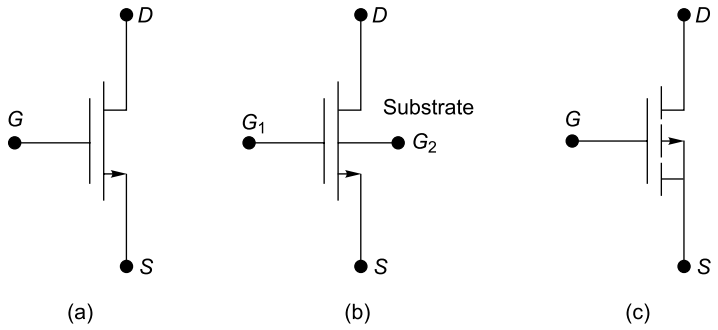


Fig. 1.60 *(a) and (b) p-channel depletion or enhancement types MOSFET (c) p-channel enhancement types MOSFET*

1.20 COMPLEMENTARY MOSFET (CMOS)

To reduce the power dissipation to very small about 50 nW, the complementary *p*-channel and *n*-channel enhancement MOSFET devices are manufactured with in a same chip. Figure 1.61 shows a complementary MOS (CMOS) inverter. Transistor T_1 is a *p*-channel MOSFET and transistor T_2 is an *n*-channel MOSFET. These two devices are connected in series, their drain terminals are connected together and gate terminals are also interconnected. The gate input voltage V_i varies from 0 V to $-V_{DD}V$. While $V_i = -V_{DD}$ (logic 1) transistor T_1 is turned on and T_2 is turned off, the output voltage V_o is equal to 0 V (logic 0). When $V_i = 0$ (logic 0), the transistor T_2 is turned on and transistor T_1 is turned off, then output voltage is $-V_{DD}$ (logic 1).

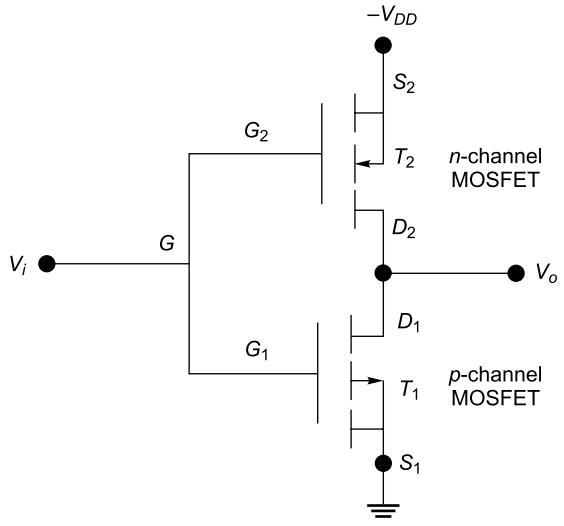


Fig. 1.61 *Complementary MOS inverter*

The cross-section view of complementary MOSFET (CMOS) is depicted in Fig. 1.62. In an *n*-type substrate, the *p*-type well is diffused. Then *n*-channel MOSFET T_2 is formed in this region and its three terminals are available.

Subsequently, a *p*-channel MOS T_1 is also formed into the *n*-type substrate and its three terminals are available as depicted in Fig. 1.62.

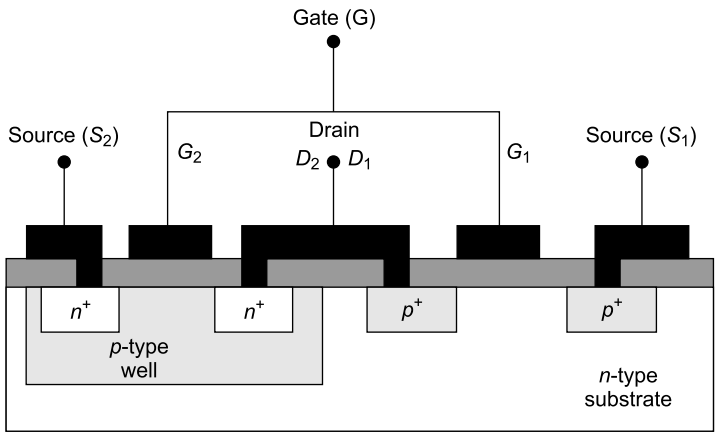


Fig. 1.62 ***Cross section of complementary MOS inverter***

1.21 BIASING THE FET

The biasing of FET is required to use FET as switching device and amplifiers in any applications. To turn on the FET and operate it in any region (linear or saturation), the biasing of FET is essential. When a FET is properly biased, a fixed level of drain current flows through the FET from drain to source and there will be a desired fixed voltage drop across the FET junctions. There are different types of biasing arrangement of FET such as

- Gate Bias
- Self-bias
- Voltage divider bias
- Source bias

In this section, gate bias, self-bias, and voltage divider bias of FET are discussed in detail.

1.21.1 Gate Bias

Figure 1.63(a) shows the gate bias of *n*-channel JFET. In this circuit, the gate voltage ($-V_{GG}$) is applied so that the gate source junction is properly reverse biased. As there is no gate current, there will be no voltage drop across resistance R_G. The gate biasing can not able to provide a stable *Q*-point. The resistance R_G is used for ac operation. Figure 1.63(b) shows the gate bias of *p*-channel JFET which is similar to Fig. 1.63(a) but the polarity of V_{GG} and V_{DD} are reversed.

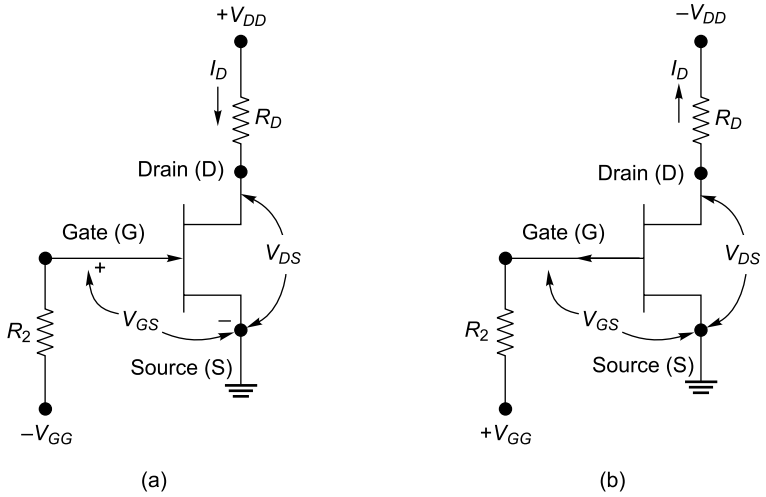


Fig. 1.63 *Gate bias: (a) n-channel JFET (b) p-channel JFET*

1.21.2 Self-bias

Figure 1.64(a) shows the self-bias of *n*-channel JFET. In this circuit, the drain voltage (V_{DD}) is applied and there is no gate voltage ($V_G = 0$). The source terminal is connected to the ground through resistance R_S.

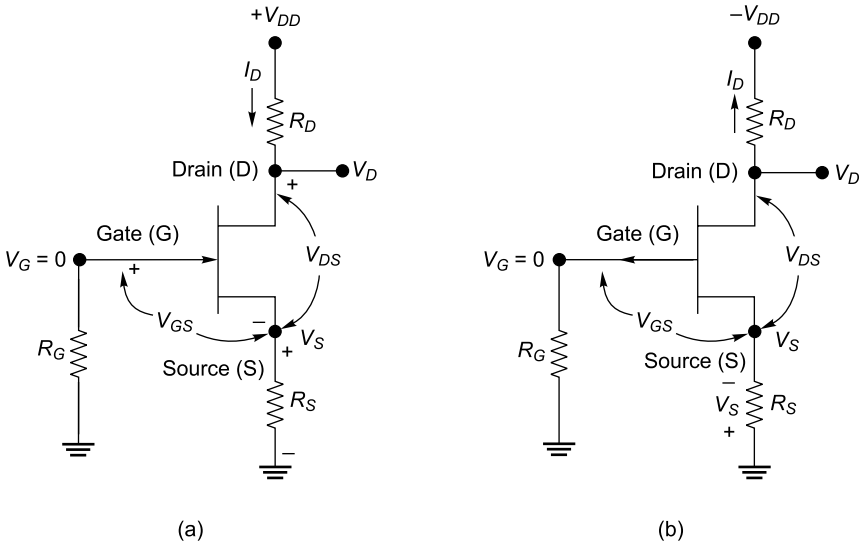


Fig. 1.64 *Self-bias: (a) n-channel JFET (b) p-channel JFET*

When the drain voltage (V_{DD}) is applied, a drain current (I_D) flows even though gate current is not present. Since the drain current (I_D) flows through R_S, the voltage drop across R_S is $V_S = I_D R_S$. This voltage drop reduces the gate to source reverse voltage required for FET operation. The resistance R_S is called a feed resistance and its function is to prevent any variation in FET drain current.

The source voltage is

$$V_S = I_D R_S$$

The drain voltage is equal to

$$V_D = V_{DD} - I_D R_D$$

The drain to source voltage (V_{DS}) is the difference between the drain voltage (V_D) and the source voltage (V_S) and it can be expressed as

$$V_{DS} = V_D - V_S = (V_{DD} - I_D R_D) - I_D R_S$$

or, $$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

The gate to source voltage (V_{GS}) is the difference between the gate voltage (V_G) and the source voltage (V_S) and it can be expressed as

$$V_{GS} = V_G - V_S = 0 - I_D R_S \text{ as } V_{GS} = 0$$

or, $$V_{GS} = -I_D R_S$$

Then drain current is $I_D = -\dfrac{V_{GS}}{R_S}$ and the plot of drain current (I_D) vs gate to source voltage (V_{GS}) is shown in Fig. 1.65.

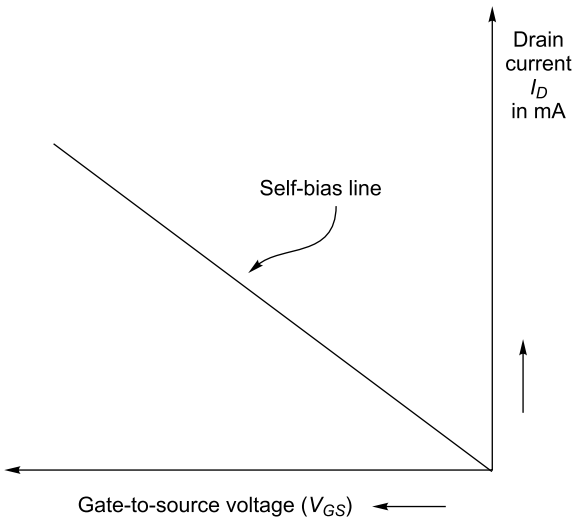


Fig. 1.65 ***Self-bias line***

Therefore, the gate-to-source voltage (V_{GS}) is equal to the negative of the voltage across the source resistance. Hence, if drain current increases, the voltage drop across R_S increases. This increased voltage drop increases the reverse gate to source voltage and the effective channel width will be decreases. Then drain current decreases. As a result, the reduced drain current decreases the gate-to-source voltage and the effective channel width of FET increases to increase the drain current.

The *Q*-point (quiescent operation point) of self-bias FET can be determined using graphical method as shown in Fig. 1.66. It is clear from Fig. 1.66 that a self-bias line intersects the transfer characteristic curve at mid-point. This point of

intersection is known as Q-point. Then the co-ordinates of Q point can be determined graphically.

The drain current $I_D = -\frac{V_{GS}}{R_S}$ is used for self-bias line and the transfer characteristic follows

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

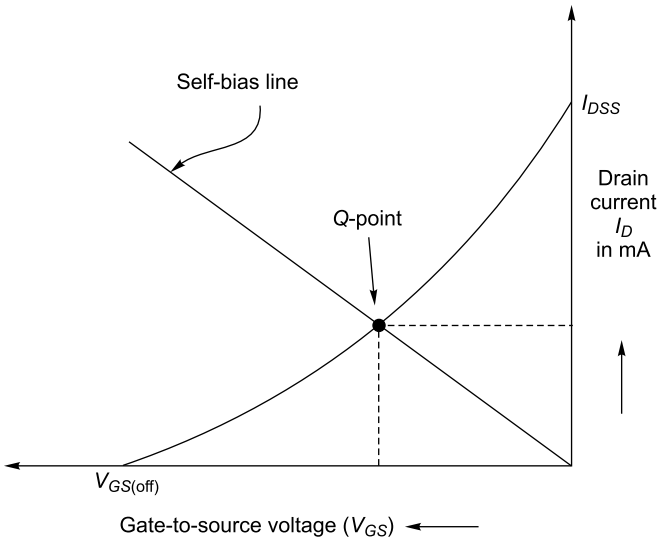


Fig. 1.66 ***Q-point***

The Q-point can also be determined using dc load line. Figure 1.67(a) shows the dc load line on the drain characteristics of a FET. The dc load line is a plot between drain current (I_D) and drain-to-source voltage (V_{DS}).

The drain-to-source voltage is $V_{DS} = V_{DD} - I_D(R_D + R_S)$. The dc load line intersects y-axis at point A and x-axis at point B. At point A, $V_{DS} = 0$ and the coordinate of point A is $\left(0, \frac{V_{DS}}{R_D + R_S}\right)$. Similarly at point B, $I_D = 0$ and the coordinate of point B is $(V_{DD}, 0)$. Since the Q point is the mid point of the dc load line as shown in Fig. 1.67(b).

The value of drain current at Q point is

$$I_{DQ} = \frac{V_{DD}}{2(R_D + R_S)} \text{ and the drain to source voltage is } V_{DQ} = \frac{V_{DD}}{2}.$$

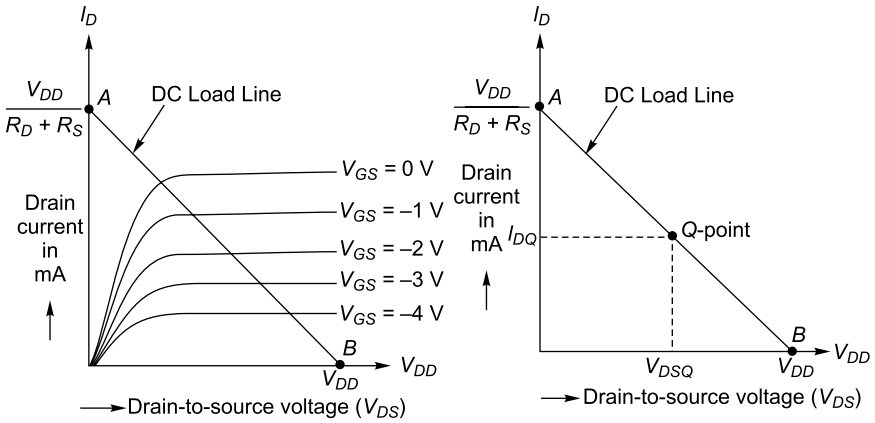


Fig. 1.67 *(a) Dc load line on drain characteristics (b) co-ordinate of Q-point*

1.21.3 Voltage Divider Bias

Figure 1.68(a) shows the voltage divider bias circuit of FET and its Thevenin's equivalent circuit shown in Fig. 1.68(b). In Fig. 1.68(a), resistance R_1 and R_2 form a voltage divider.

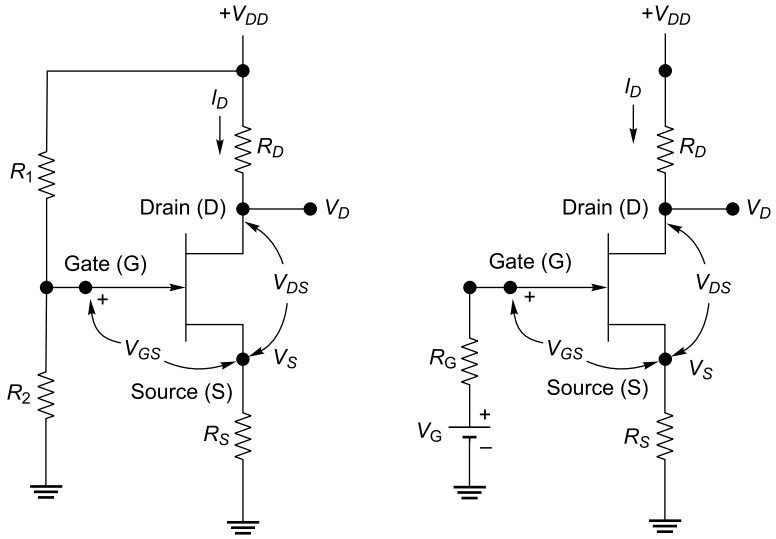


Fig. 1.68 *(a) Voltage divider bias of an n-channel JFET (b) Alternative representation of Fig. 1.68(a)*

The gate voltage is equal to

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} \text{ and the resistance } R_G = \frac{R_1 R_2}{R_1 + R_2}$$

The gate-to-source voltage $V_{GS} = V_G - I_D R_S$
The drain-to-ground voltage $V_D = V_{DD} - I_D R_D$

When the gate voltage is very large as compared to gate-to-source voltage, the drain current is approximately constant. In actual practice, the voltage divider bias is less effective with JFET than BJT. In BJT, the base to emitter voltage V_{BE} is about 0.7 with minor variation from one transistor to another. In case of JFET, the V_{GS} can vary several volts from one JFET to another.

1.7 Determine the value of R_S for a self-bias *n*-channel JFET, when I_{DSS} = 50 mA, V_P = –12 V, and V_{GS} = –5 V.

Solution

Given $I_{DSS} = 50$ mA, $V_P = -12$ V, and $V_{GS} = -5$ V.

We know that $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or, $$I_D = 50 \times 10^{-3}\left(1 - \frac{(-5)}{(-12)}\right)^2 = 17.013 \text{ mA}$$

The value of R_S is $R_S = \left|\frac{V_{GS}}{I_D}\right| = \left|\frac{-5}{17.013 \times 10^{-3}}\right| \Omega = 293.89\ \Omega$

1.8 Determine the value of drain-to-source voltage (V_{DS}) and gate-to-source voltage (V_{GS}) for an *n*-channel JFET as shown in Fig. 1.69. Assume I_D = 4 mA.

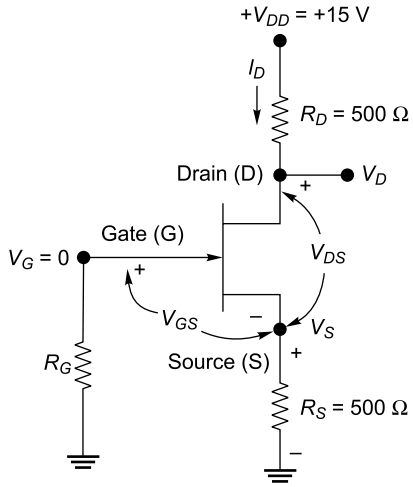


Fig. 1.69

Solution

Given $I_D = 4$ mA, $V_{DD} = 15$ V, $R_D = 1500\ \Omega$, and $R_S = 500\ \Omega$.
The source voltage across resistance R_S is

$$V_S = I_D R_S = 4 \times 10^{-3} \times 500 \text{ V} = 2 \text{ V}$$

The drain-to-ground voltage is

$$V_D = V_{DD} - I_D R_D = 15 - 4 \times 10^{-3} \times 1500 = 9 \text{ V}$$

The drain-to-source voltage is

$$V_{DS} = V_D - V_S = 9 - 2 = 7 \text{ V}$$

The gate-to-source voltage is

$$V_{GS} = -V_S = -2 \text{ V}$$

1.9 Determine the operating point of a self-biased JFET, when I_{DSS} = 10 mA, V_{GS} = –2 V, I_D = 4.5 mA, V_D = 6 V and V_{DD} = 12 V. Compute the value of R_D and R_S at this biasing condition.

Solution

Given I_{DSS} = 10 mA, V_{GS} = –2 V, I_D = 4.5 mA, and V_{DD} = 12 V.
At the Q point the drain current is

$$I_{DQ} = \frac{I_{DSS}}{2} = \frac{10}{2} \text{ mA} = 5 \text{ mA and}$$

the value of drain-to-source voltage is

$$V_{DSQ} = \frac{V_{DD}}{2} = \frac{12}{2} \text{ V} = 6 \text{ V}$$

Then operating point is V_{DSQ} = 6 V and I_{DQ} = 5 mA

The drain-to-ground voltage is

$$V_D = V_{DD} - I_D R_D$$

Then, the value of R_D resistance is

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12 - 6}{4.5 \times 10^{-3}} \ \Omega = 1333.33 \ \Omega$$

The source voltage across resistance R_S is $V_S = -V_{GS} = I_D R_S$
Therefore, the value of R_S resistance is

$$R_S = \frac{V_S}{I_D} = \frac{2}{4.5 \times 10^{-3}} \ \Omega = 444.44 \ \Omega$$

1.10 A voltage divider biasing circuit of JFET is shown in Fig. 1.70. Determine the value of drain current I_D, gate to source voltage V_{GS}, and drain to ground voltage V_D when I_{DSS} = 5 mA, V_P = –6 V, R_D = 1000 Ω, R_S = 1500 Ω, R_1 = 500 kΩ, R_2 = 1 MΩ and V_{DD} = 15 V.

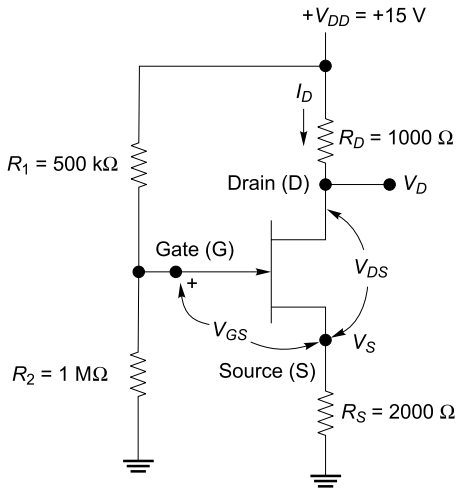


Fig. 1.70

Solution

Given I_{DSS} = 5 mA, V_P = –5 V, R_D = 1000 Ω, R_S = 2000 Ω = 2 kΩ, R_1 = 500 kΩ, R_2 = 1 MΩ = 1000 kΩ and V_{DD} = 15 V.

The gate voltage is equal to

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{1000\ \text{k}\Omega}{500\ \text{k}\Omega + 1000\ \text{k}\Omega} \times 15\ \text{V} = 10\ \text{V}$$

The gate-to-source voltage $V_{GS} = V_G - I_D R_S$

We know that $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

After substituting the value of V_{GS}, we get

$$I_D = I_{DSS}\left(1 - \frac{V_G - I_D R_S}{V_P}\right)^2$$

or, $$I_D = 5\left(1 - \frac{10 - I_D \times 2}{-5}\right)^2$$

or, $$I_D = 5\left(\frac{-5 - 10 + I_D \times 2}{-5}\right)^2$$

$$= 5\frac{(-15 + 2I_D)^2}{5^2}$$

$$= \frac{(-15 + 2I_D)^2}{5}$$

or, $$5I_D = 225 + 4I_D^2 - 60I_D$$

or, $$4I_D^2 - 65I_D + 225 + = 0$$

The I_D is 5 mA or 11.25 mA

As I_D = 11.25 mA > 5 mA = I_{DSS}, the appropriate value of I_D is 5 mA.

At the operating Q point, I_{DQ} is 5 mA

Then the gate-to-source voltage is

$$V_{GS} = V_G - I_D R_S = 10 - 5 \times 10^{-3} \times 1500 = 2.5\ \text{V}$$

The drain-to-ground voltage is

$$V_D = V_{DD} - I_D R_D = 15 - 5 \times 10^{-3} \times 1000 = 10\ \text{V}.$$

1.11 Figure 1.71 shows a voltage divider biasing circuit of JFET. I_{DSS} = 12 mA, V_P = –5 V, $R_1 + R_2$ = 500 kΩ, I_D = 6 mA, R_S = 500 Ω and V_{DS} = 5 V, compute the value of R_1, R_2 and R_D. Verify whether the JFET operates in saturation region. Assume V_{DD} = 10 V.

Solution

Given I_{DSS} = 12 mA, V_P = –5 V, $R_1 + R_2$ = 500 kΩ, I_D = 6 mA, V_{DS} = 5 V and V_{DD} = 10 V.

We know that $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or, $$6 \times 10^{-3} = 12 \times 10^{-3}\left(1 - \frac{V_{GS}}{-5}\right)^2$$

or, $$V_{GS} = -1.464 \text{ V}$$

The gate-to-source voltage is

$$V_{GS} = V_G - I_D R_S$$

Then $$V_G = V_{GS} + I_D R_S = -1.464 + 6 \times 10^{-3} \times 500 = 1.536 \text{ V}$$

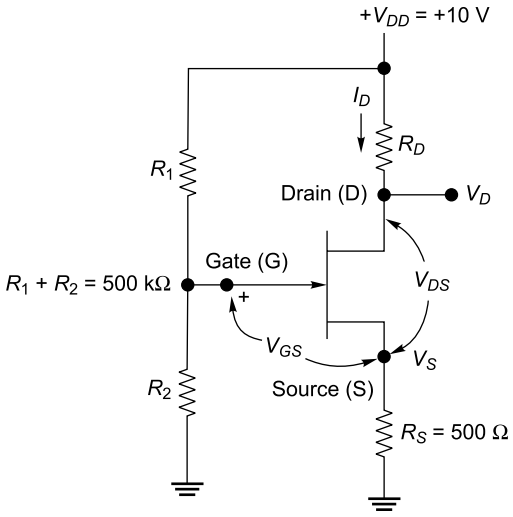


Fig. 1.71

The gate voltage is equal to

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

or, $$1.536 = \frac{R_2}{500} \times 10 \text{ as } R_1 + R_2 = 500 \text{ k}\Omega,\ V_G = 1.536 \text{ and } V_{DD} = 10 \text{ V}$$

The value of R_2 is 76.8 kΩ

The value of R_1 is 500 kΩ – R_2 = 500 kΩ – 76.8 KΩ = 423.2 kΩ

The drain-to-ground voltage $V_D = V_{DD} - I_D R_D = V_{DS} + I_D R_S$

Then, $$V_{DD} - V_{DS} - I_D R_S = I_D R_D$$

The drain resistance is $R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} = \frac{10 - 5 - 6 \times 10^{-3} \times 500}{6 \times 10^{-3}} = 333.33\ \Omega$

The voltage $V_{GS} - V_P = -1.464 - (-5) = 3.536$ V

Since $V_{DS} > V_{GS} - V_P$, the transistor operates in saturation region.

1.22 FET AMPLIFIER CONFIGURATIONS

Just like bipolar junction transistor (BJT), the field effect transistor (FET) is also used to amplify ac signals. Depending upon the configuration, the FET amplifiers can be classified into the following three amplifiers:

- Common source (CS) amplifier
- Common drain (CD) amplifier or Source flower
- Common gate (CG) amplifier

The small signal models of FET can be used for analyzing the above three FET amplifiers. In this section, common source (CS), common drain (CD) and common gate (CG) amplifiers are discussed in detail.

1.22.1 Common Source (CS) Amplifier

Figure 1.72 shows the common source amplifier circuit where resistance R_1 and R_2 are used as voltage divider bias of field effect transistor. The capacitor C_1 and C_2 are used to couple the ac input voltage and output voltage, respectively. Therefore, C_1 and C_2 are called coupling capacitors. The capacitor C_s is used as bypass capacitor.

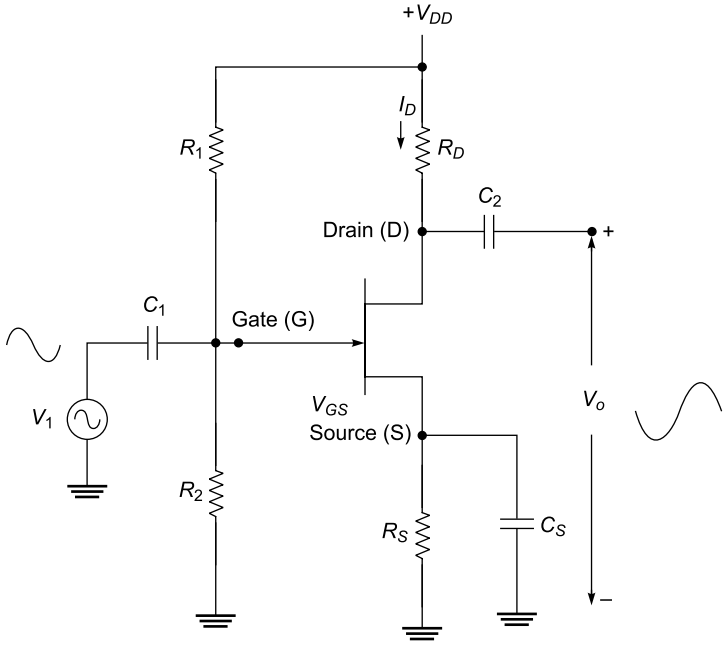


Fig. 1.72 *Common source amplifier circuit of FET*

When a small ac voltage signal is applied to the gate, it generates variations in the gate to source voltage. Consequently, the drain current varies. If the gate-to-source voltage increases, the drain current also increases. Accordingly, the voltage drop across the resistance R_D increases and the drain voltage decreases. As a result, the positive half cycle of input voltage generates the negative half cycle of output voltage. The output voltage is 180° out of phase with respect to input voltage. Due to 180° phase shift, the common source amplifier behaves as common emitter bipolar transistor amplifier.

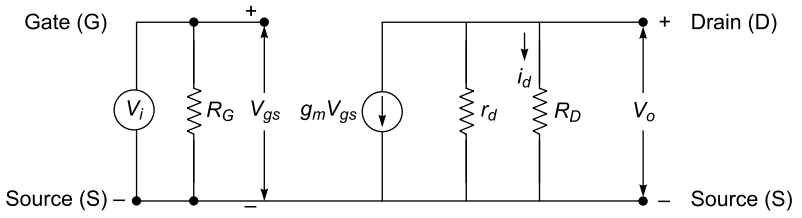


Fig. 1.73 ***Equivalent circuit of common source amplifier***

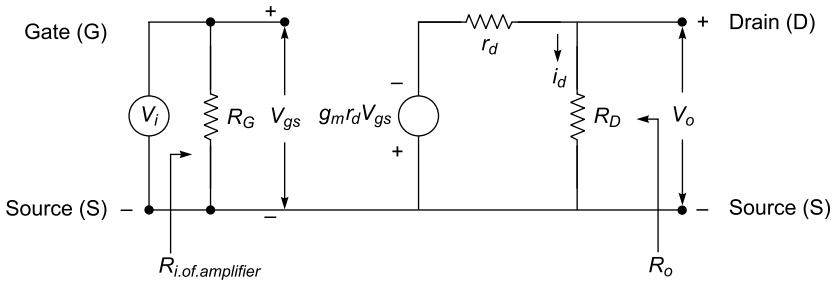


Fig. 1.74 ***Alternative representation of common source amplifier***

Figure 1.73 shows the ac equivalent circuit of common source amplifier which is obtained by short circuiting the capacitors and dc voltage supplies. Figure 1.73 can also be represented by the equivalent circuit as depicted in Fig. 1.74. The field effect transistor is replaced by small signal low frequency model of FET. Now we can determine the voltage gain, input resistance and output resistance.

Voltage gain: This the ratio of the output voltage (v_o) to the input voltage (v_i) and it can be expressed as $A_v = \dfrac{v_o}{v_i}$

The drain current i_d flows though R_D and it's value is equal to

$$i_d = \frac{g_m r_d v_{gs}}{r_d + R_D} = \frac{r_d}{r_d + R_D} g_m v_{gs}$$

The output voltage is equal to

$$v_o = -i_d R_D = -\frac{r_d}{r_d + R_D} g_m v_{gs} R_D$$

$$= -\frac{r_d R_D}{r_d + R_D} g_m v_{gs}$$

$$= -r_L g_m v_{gs} \text{ where } r_L = r_d \,\|\, R_D = \frac{r_d R_D}{r_d + R_D}$$

Since input voltage $v_i = v_{gs}$, output voltage $v_o = -r_L g_m v_i$

Then voltage gain v is

$$A_v = \frac{v_o}{v_i} = -r_L g_m$$

The negative sign indicates that the output voltage is 180° phase shift from input voltage.

As the drain resistance (r_d) is greater than R_D, the equivalent resistance of r_d and R_D in parallel is $r_L = R_D$. Then, voltage gain is $A_v = -g_m R_D$.

Input resistance It is the ratio of the input voltage to the input current and it can be expressed by

$$R_i = \frac{v_i}{v_i}.$$

Since input resistance (R_i) of a FET is very high, the gate to source is considered as open circuit. The input resistance of amplifier is the parallel combination of resistors R_1, R_2 and FER input resistance R_i. Then input resistance of amplifier can be expressed by

$$R_{i.of.amplifier} = R_1 \parallel R_2 \parallel R_i = R_1 \parallel R_2 = R_G$$

Output resistance The output resistance is the ratio of output voltage (v_o) to the output current (i_d) and it can be expressed as

$$R_o = \frac{v_o}{i_d}$$

Actually, the output resistance of FET is r_d. Then output resistance of amplifier is the parallel combination of r_d and R_D and it can be expressed as $R_o = r_d \parallel R_D$

As r_d is very large compared to R_D, the output resistance is equal to R_D and $R_o = R_D$

1.22.2 Common Drain (CD) Amplifier

Figure 1.75 shows the common source amplifier circuit. In this circuit self biasing is used. The capacitor C_1 and C_2 are used to couple the ac input voltage and output voltage, respectively. Hence, C_1 and C_2 are known as *coupling capacitors*. The capacitor C_s is used as bypass capacitor.

When a small ac voltage signal is applied to the gate, it produces variations in the gate-to-source voltage. Then the drain current varies. When the gate-to-source voltage increases, the drain current also increases. Consequently, the voltage drop across the resistance R_S increases and the output voltage also increases. Since the output voltage of common drain amplifier is approximately equal to input voltage and is in phase with input voltage, there is no phase shift between input voltage and output voltage. Therefore, this circuit is also known as *source follower*.

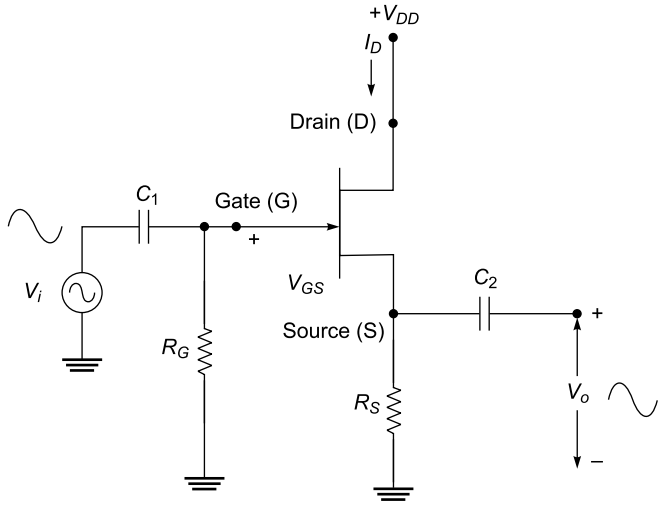


Fig. 1.75 *Common drain amplifier circuit of FET*

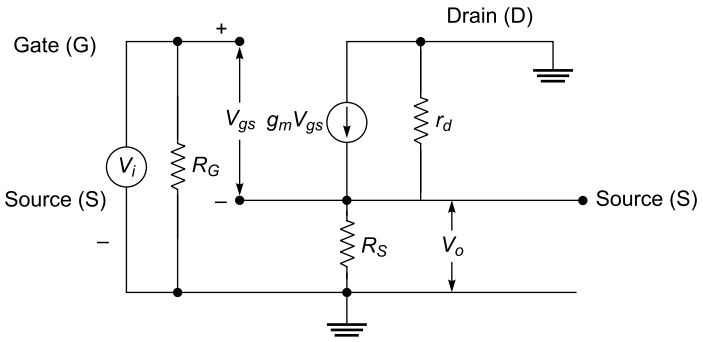


Fig. 1.76 *Equivalent circuit of common drain amplifier*

Figure 1.76 shows the ac equivalent circuit of common drain amplifier which is obtained by short circuiting the capacitors and dc voltage supplies. In this circuit, the field effect transistor is replaced by small signal low frequency model of FET. To determine the voltage gain, input resistance and output resistance, Fig. 1.76 can also be represented by the equivalent circuit as depicted in Fig. 1.77.

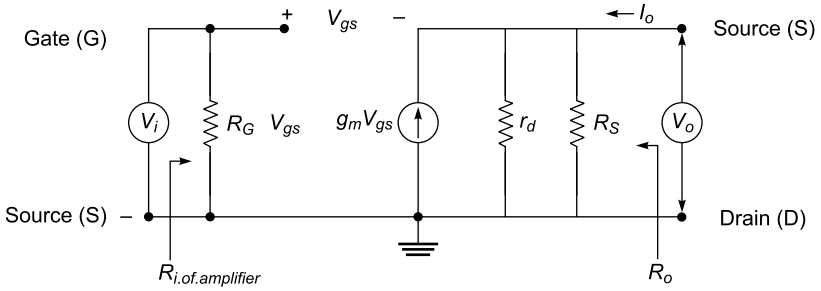


Fig. 1.77 *Alternative representation of common drain amplifier*

Voltage gain It the ratio of the output voltage (v_o) to the input voltage (v_i) and it can be expressed as $A_v = \frac{v_o}{v_i}$

The output voltage is equal to

$$v_o = g_m v_{gs} \times r_d \parallel R_S$$

$$= \frac{r_d R_S}{r_d + R_S} g_m v_{gs}$$

Writing the KVL equation from input to output, the input voltage is equal to

$$v_i = v_{gs} + v_o = v_{gs} + \frac{r_d R_S}{r_d + R_S} g_m v_{gs}$$

$$= \frac{r_d + R_S + r_d R_S g_m}{r_d + R_S} v_{gs}$$

Then voltage gain A_v is

$$A_v = \frac{v_o}{v_i} = \frac{r_d R_S}{r_d + R_s} g_m v_{gs} \Big/ \frac{r_d + R_S + r_d R_S g_m}{r_d + R_S} V_{gs}$$

$$= \frac{r_d R_S g_m}{r_d + R_S + r_d R_S g_m}$$

After dividing by $r_d g_m$, we get $A_v = \dfrac{R_S}{\dfrac{1}{g_m} + \dfrac{R_S}{r_d g_m} + R_S}$

Since R_S is much grater than $\frac{1}{g_m} + \frac{R_S}{r_d g_m}$, the voltage is approximately equal to unity.

Input resistance It is the ratio of the input voltage to the input current and it can be expressed by $R_i = \frac{v_i}{i_i}$.

As input resistance (R_i) of a FET is very high, the input resistance of amplifier is the parallel combination of resistors and FET input resistance R_i. Therefore, input resistance of amplifier is

$$R_{i.of.amplifier} = R_G \parallel R_i = R_G$$

Output resistance The output resistance is the ratio of output voltage (v_o) to the output current (i_o) and it can be expressed as

$$R_o = \frac{v_o}{i_o}$$

Applying the KCL, we write

$$i_o + g_m v_{gs} = \frac{v_o}{R_S} + \frac{v_o}{r_d}$$

Since there is no current in the input side of the circuit, we can assume $v_{gs} = -v_o$.

Then
$$i_o = g_m v_o + \frac{v_o}{R_S} + \frac{v_o}{r_d}$$

or,
$$\frac{i_o}{v_o} = g_m + \frac{1}{R_S} + \frac{1}{r_d}$$

Therefore, the output resistance R_o is equal to

$$R_o = \frac{1}{g_m} \| R_S \| r_d$$

1.22.3 Common Gate (CG) Amplifier

Figure 1.78 shows the common gate amplifier circuit. In this circuit, the input signal is applied at source through a coupling capacitor C_1 and the output voltage is obtained from the drain terminal through a coupling capacitor C_2. Due to the capacitor C_G, the gate is effectively ac ground.

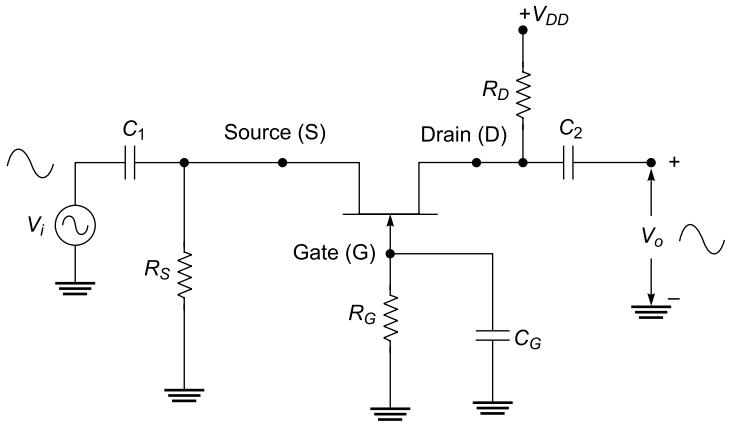


Fig. 1.78 ***Common gate amplifier circuit of FET***

When a small ac voltage signal is applied to the source, it generates variations in the gate to source voltage. Subsequently, the drain current varies. When the gate-to-source voltage increases, the drain current also increases. Therefore, the voltage drop across the resistance R_S increases and the output voltage also increases. Hence, the output voltage of common drain amplifier is in phase with input voltage.

Figure 1.79 shows the ac equivalent circuit of common drain amplifier which is obtained by short circuiting the capacitors and dc voltage supplies. In this circuit, the field effect transistor is replaced by small signal low frequency model of FET.

To determine the voltage gain, input resistance and output resistance, Fig. 1.79 will be represented by the equivalent circuit as depicted in Fig. 1.80.

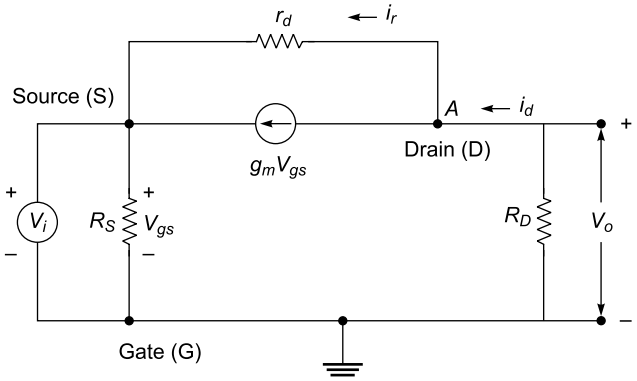


Fig. 1.79 *Equivalent circuit of common gate amplifier*

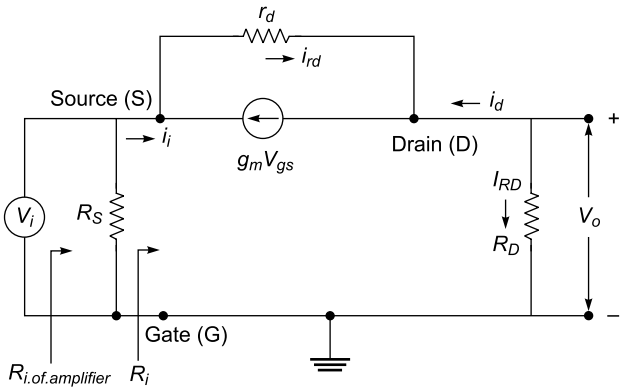


Fig. 1.80 *Alternative representation of common gate amplifier*

Voltage gain

Applying the KCL at point *A* in small signal equivalent circuit (Fig. 1.79), we get

$$i_r = i_d - g_m v_{gs}$$

Applying the KVL in the outer loop of Fig. 1.79, we obtain

$$v_o = (i_d - g_m v_{gs})\, r_d + v_{sg}$$

Since $v_{sg} = -v_{gs} = v_i$ and $i_d = -\dfrac{v_o}{R_D}$, we find that

$$v_o = \left(-\frac{v_o}{R_D} + g_m v_i\right) r_d + v_i$$

The voltage gain A_v is equal to

$$A_v = \frac{v_o}{v_i} = \frac{(1 + g_m r_d) R_D}{R_D + r_d}$$

Input resistance

As per Fig. 1.79 and Fig. 1.80 the current flow through resistance r_d is

$$i_{rd} = -i_r = i_i + g_m v_{gs} \text{ where } i_{rd} = \frac{v_i - v_o}{r_d} = \frac{v_i - I_{RD}R_D}{r_d} \quad \text{as } v_o = I_{RD}R_D$$

Therefore, $$i_i = \frac{v_i - I_{RD}R_D}{r_d} - g_m v_{gs}$$

As $$v_{sg} = -v_{gs} = v_i,\ i_i = \frac{v_i - I_{RD}R_D}{r_d} + g_m v_i$$

or, $$i_i + \frac{I_{RD}R_D}{r_d} = \frac{v_i}{r_d} + g_m v_i$$

As $i_i = I_{RD}$, we can write

$$i_i + \frac{i_i R_D}{r_d} = \frac{v_i}{r_d} + g_m v_i$$

Then input resistance is

$$R_i' = \frac{v_i}{i_i} = \frac{r_d + R_D}{1 + g_m r_d}$$

The input resistance of amplifier is $R_i = R_i' \parallel R_S$

Output resistance

The output resistance of common drain amplifier is $R_o = r_d \parallel R_D$.
Since $r_d >> R_D$, $R_o = R_D$.

1.12 A common source JFET amplifier has g_m of 5 mA/V. When the value of external drain resistance R_D is 2000 Ω, determine the value of voltage gain of amplifier.

Solution

Given $g_m = 5$ mA/V and $R_D = 2000\ \Omega$
The voltage gain is

$$A_v = -g_m R_D = -5 \times 10^{-3} \times 2000 = -10$$

1.13 A common source JFET amplifier has r_d of 500 kΩ and g_m of 4 mA/V. If the value of external load (drain) resistance R_D is 20 kΩ, find the value of voltage gain of the amplifier.

Solution

Given $r_d = 500$ kΩ, $g_m = 5$ mA/V and $R_D = 2000\ \Omega$
The equivalent resistance is

$$r_L = r_d \parallel R_D = \frac{r_d R_D}{r_d + R_D} = \frac{500 \times 20}{500 + 20}\ \text{k}\Omega = 19.23\ \text{k}\Omega$$

The voltage gain is

$$A_v = \frac{v_o}{v_i} = -r_L g_m = -19.23 \times 10^3 \times 4.5 \times 10^{-3} = -86.535$$

1.14 Figure 1.81 shows a common source JFET amplifier circuit. Determine the value of voltage gain of the amplifier, input resistance and output resistance. Assume r_d is 100 kΩ and g_m = 2 mA/V.

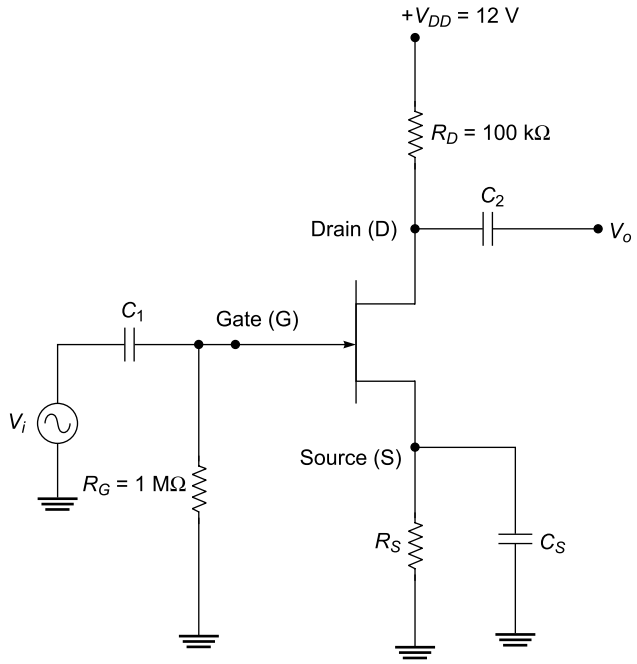


Fig. 1.81

Solution

Given r_d = 100 kΩ, g_m = 2 mA/V, R_G = 1 MΩ and R_D = 10 kΩ

The equivalent resistance is

$$r_L = r_d \parallel R_D = \frac{r_d R_D}{r_d + R_D} = \frac{100 \times 10}{100 + 10} \text{ kΩ} = 9.09 \text{ kΩ}$$

The voltage gain is

$$A_v = \frac{v_o}{v_i} = -r_L g_m = -9.09 \times 10^3 \times 2 \times 10^{-3} = -18.18$$

The input resistance of amplifier is

$$R_{i.of.amplifier} = R_G = 1 \text{ MΩ}$$

The output resistance of amplifier is $R_o = r_d \parallel R_D$ = 9.09 kΩ

1.15 A MOSFET amplifier operates at 30 KHz with the following parameters:

r_d = 200 kΩ, g_m = 4 mA/V, C_{GS} = 3.0 pF, C_{GS} = 1.5 pF, C_{GD} = 2.5 pF and R_D = 10 kΩ

Determine the voltage gain of the amplifier.

Solution

Given r_d = 200 kΩ, g_m = 4 mA/V, C_{GS} = 3.0 pF, C_{GS} = 1.5 pF, C_{GD} = 2.5 pF and R_D = 10 kΩ

The equivalent resistance is

$$r_L = r_d \parallel R_D = \frac{r_d R_D}{r_d + R_D} = \frac{200 \times 10}{200 + 10} \text{ k}\Omega = 9.52 \text{ k}\Omega$$

The voltage gain is

$$A_v = \frac{v_o}{v_i} = -r_L g_m = -9.52 \times 10^3 \times 4 \times 10^{-3} = -38.08$$

1.16 Figure 1.82 shows a common source JFET amplifier circuit. Determine the value of output voltage gain of the amplifier, if $g_m = 3000$ μS, and $I_D = 5$ mA. The effect of drain resistance is neglected.

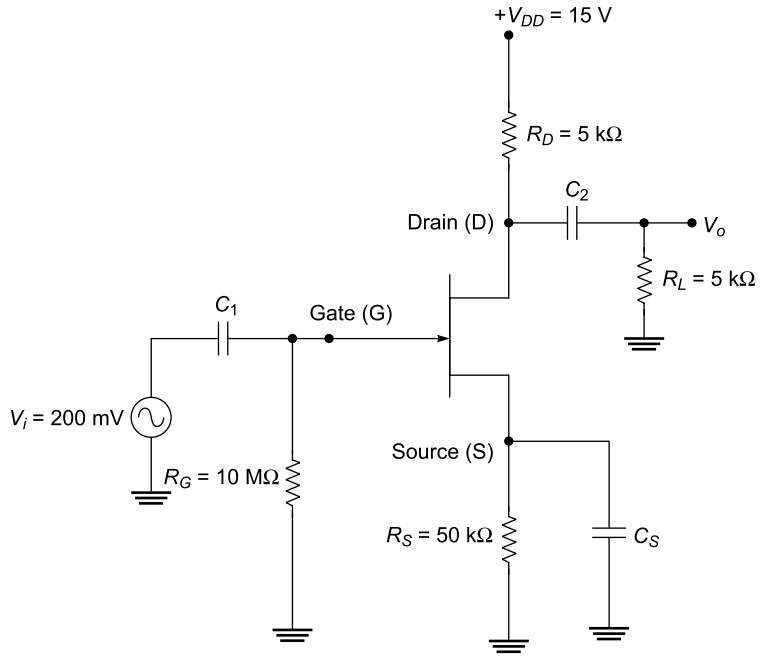


Fig. 1.82

Solution

Given $g_m = 3000$ μS, $R_G = 10$ MΩ, $R_D = 5$ kΩ, $R_D = 5$ kΩ, $V_i = 200$ mV and $I_D = 5$ mA
The equivalent resistance is

$$r_L = R_L \parallel R_D = \frac{R_L R_D}{R_L + R_D} = \frac{5 \times 5}{5 + 5} \text{ k}\Omega = 2.5 \text{ k}\Omega$$

The output voltage is

$$v_o = A_v v_i = -r_L g_m v_i = -2.5 \times 10^3 \times 3000 \times 10^{-6} \times 200 \text{ mV} = 1500 \text{ mV} = 1.5 \text{ V}$$

1.17 Find the value of voltage gain of a FET amplifier as shown in Fig. 1.83. The FET has the following parameters:

$I_{DSS} = 10$ mA, $V_P = -4$ V

At the Q point, $I_{DQ} = 5$ mA and $V_{GS} = -1.5$ V

Assume that the effect of drain resistance is neglected.

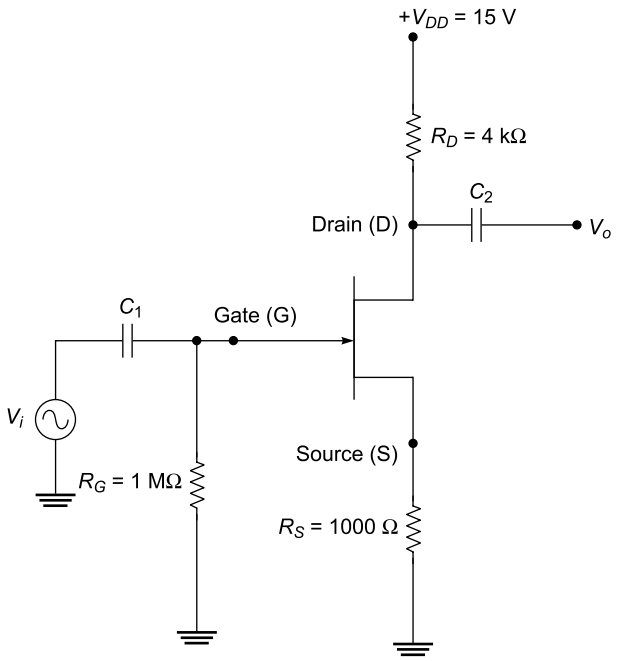


Fig. 1.83

Solution

Given $R_G = 1$ MΩ, $R_D = 4$ kΩ, $R_S = 1000$ Ω, $I_{DSS} = 10$ mA, $V_P = -4$ V, $I_{DQ} = 5$ mA and $V_{GS} = -1.5$ V

We know that $g_{m0} = -\dfrac{2I_{DSS}}{V_P} = -\dfrac{10\times10^{-3}}{-4} = 2.5$ mA/V

At the Q-point, $g_m = g_{m0}\left(1-\dfrac{V_{GS}}{V_P}\right) = 2.5\left(1-\dfrac{(-1.5)}{(-4)}\right)$ mA $= 1.5625$ mA/V

The equivalent resistance is

$$r_L = r_d \parallel R_D = \frac{r_d R_D}{r_d + R_D} = R_D = 4 \text{ kΩ}$$

The input voltage is

$$v_{\text{in}} = V_{GS} + i_D R_S$$

The output voltage is

$$v_o = -i_D r_L$$

The voltage gain is

$$A_v = \frac{v_o}{v_i} = \frac{i_D R r_L}{V_{GS} + i_D R_S} = \frac{g_m V_{GS} R_L}{V_{GS} + g_m V_{GS} R_S}$$

$$= \frac{g_m r_L}{1 + g_m R_S} = \frac{1.5625\times10^{-3}\times4\times10^{3}}{1+1.5625\times10^{-3}\times1000} = -2.439$$

1.18 Figure 1.84 shows a common drain JFET amplifier circuit. Determine the voltage gain of the amplifier, input resistance and output resistance if g_m = 5 mA/V. The effect of drain resistance is neglected ($r_d = \infty$).

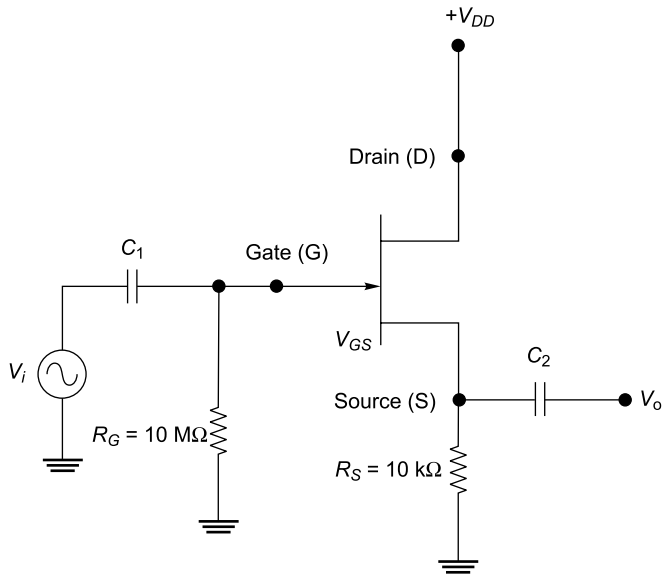


Fig. 1.84

Solution

Given g_m = 5 mA/V, R_G = 10 MΩ, and R_S = 10 kΩ
Then voltage gain A_v is

$$A_v = \frac{v_o}{v_i} = \frac{r_d R_S g_m}{r_d + R_S + r_d R_S g_m}$$

or,
$$A_v = \frac{R_S}{\frac{1}{g_m} + \frac{R_S}{r_d g_m} + R_S} = \frac{R_S}{\frac{1}{g_m} + R_S} \quad \text{as } r_d = \infty$$

Then
$$A_v = \frac{R_S}{\frac{1}{g_m} + R_S} = \frac{10 \times 1000}{\frac{1}{5 \times 10^{-3}} + 10 \times 1000} = 0.98$$

The input resistance of amplifier is

$$R_{i.of.amplifier} = R_G = 10 \text{ M}\Omega$$

The output resistance R_o is equal to

$$R_o = \frac{1}{g_m} \parallel R_S \parallel r_d = \frac{1}{g_m} \parallel R_S \quad \text{as } r_d = \infty$$

$$= \frac{\frac{1}{g_m} R_S}{\frac{1}{g_m} + R_S} = \frac{R_S}{1 + g_m R_S} = \frac{10 \times 1000}{1 + 5 \times 10^{-3} \times 10 \times 1000} = 196 \ \Omega$$

1.18 Figure 1.85 shows a common gate JFET amplifier circuit. Determine the voltage gain input resistance and output resistance of the amplifier Assume g_m = 4000 μS and r_d = 50 kΩ.

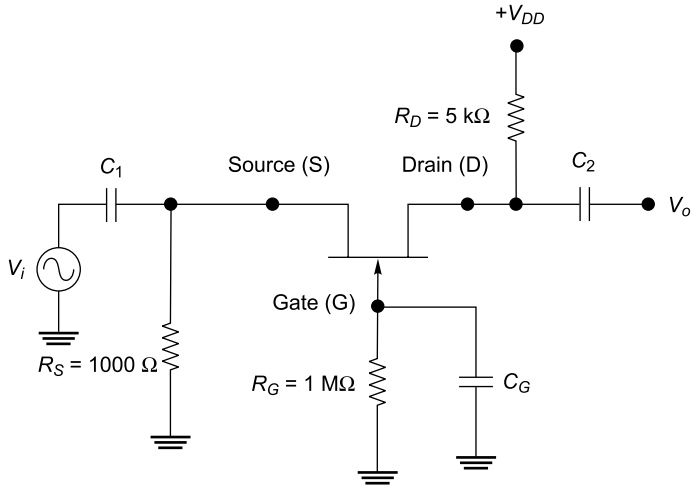


Fig. 1.85

Solution

Given $g_m = 4000\ \mu S$, $r_d = 50\ k\Omega$, $R_D = 5\ k\Omega$, $R_G = 1\ M\Omega$, and $R_S = 1000\ \Omega$

The voltage gain A_v is equal to

$$A_v = \frac{v_o}{v_i} = \frac{(1 + g_m r_d) R_D}{R_D + r_d} = \frac{(1 + 4000 \times 10^{-6} \times 50 \times 10^3) \times 5 \times 1000}{5000 + 50 \times 10^3} = 18.27$$

Then input resistance is

$$R_i' = \frac{v_i}{i_i} = \frac{r_d + R_D}{1 + g_m r_d} = \frac{(50 \times 10^3) + (5 \times 1000)}{1 + 4000 \times 10^{-6} \times 50 \times 10^3} = 273.63\ \Omega$$

The input resistance of amplifier is $R_i = R_i' \| R_S = 273.63 \| 1000 = \dfrac{273.63 \times 1000}{273.63 + 1000}$

$$= 214.84\ \Omega$$

The output resistance of amplifier is $R_o = r_d \| R_D = 50\ k\Omega \| 5\ k\Omega = \dfrac{50 \times 5}{50 + 5}\ k\Omega = 4.54\ k\Omega$

EXERCISES

Short- and Long-Answer-Type Questions

1. What is BJT? What is FET? Write the difference between BJT and FET.
2. Why FET is called Field Effect Transistor? Describe the classification of FET.
3. Explain the construction of *n*-channel JFET with diagram.
4. Discuss the construction of *p*-channel JFET with diagram.
5. Draw the drain characteristics and transfer characteristics of *n*-channel JFET and explain briefly.

6. Define the drain resistance r_d and amplification factor μ of a JFET.
7. Give a list of advantages and disadvantages of JFET and MOSFET.
8. Define the following terms of a FET:
   (i) I_{DSS}
   (ii) Transconductance
   (iii) Drain resistance
   (iv) Amplification factor
   (v) Pinch-off voltage
9. Define pinch-off voltage of a JFET. Draw the depletion region (i) before pinch-off, (ii) at pinch-off and (iii) after pinch off.
10. Derive the relationship between transconductance (g_m), drain resistance (r_d) and amplification factor (μ).
11. Derive the expression $b(x) = a\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]$ for a JFET.
12. What are characteristic curves of a JFET? Explain each characteristic curve in detail.
13. Prove that $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$ assuming $i_D = i_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$.
14. What is small signal model of FET? Draw the low frequency and high frequency small signal model of a FET.
15. Compare *n*-channel JFET and *p*-channel JFET.
16. Write the applications of field effect transistors (FET)
17. Explain why BJTs are called bipolar device while FETs are called unipolar devices.
18. What is MOSFET? What are the types of MOSFET?
19. Describe the construction and working principle of an *n*-channel enhancement type MOSFET with diagrams and draw the device characteristics.
20. Explain the construction and working principle of a *p*-channel enhancement type MOSFET with diagrams and draw the device characteristics.
21. Discuss the construction and working principle of an *n*-channel depletion type MOSFET with diagrams and draw the device characteristics.
22. Explain the construction and working principle of a *p*-channel depletion type MOSFET with diagrams and draw the device characteristics.
23. Write differences between enhancement mode FETs and depletion mode FETs with diagram.
24. Explain the effect of temperature in FET
25. Why *n*-channel MOSFET is preferred over *p*-channel MOSFET?
26. Draw the *i*-*v* characteristics of different types of MOSFET.
27. What is MOS? What the types of MOS? Explain the working principle of MOS in detail.
28. What are the biasing arrangement of a FET? Discuss any two biasing circuits of a FET.

29. Draw the circuit diagram of a common source (CS) JFET amplifier and explain its working principle. Derive the expressions for voltage gain, input resistance and output resistance.
30. Draw the circuit diagram of a common drain (CD) JFET amplifier and explain its working principle. Derive the expressions for voltage gain, input resistance and output resistance.
31. Draw the circuit diagram of a common gate (CG) JFET amplifier and explain its working principle. Derive the expressions for voltage gain, input resistance and output resistance.
32. Write a short note on CMOS.
33. When a reverse gate voltage of 12 V is applied and the gate current is 15 nA, find the resistance between gate and source.
34. In a *n*-channel JFET, $a = 3.75 \times 10^{-4}$ cm and $N_D = 10^{21}$ electrons/cm^3, determine (a) the pinch-off voltage and (b) the channel width at $V_{GS} = \frac{V_P}{2}$ and $I_D = 0$. Assume $\varepsilon = 15\varepsilon_o$.
35. Assume that the reverse gate voltage of JFET changes from 5.10 V to 4.9 V and the drain current changes from 1.2 mA to 1.75 mA. What is value of transconductance?
36. The drain current of a JFET is about 6 mA. When I_{DSS} is equal to 12 mA, $V_{GS(off)} = V_P = -6$ V, determine the value of V_{GS}.
37. In an *n*-channel JFET, I_{DS} is 5 mA and $V_P = -4$ V. Find the minimum value of V_{DS} for pinch-off operation. Determine the value of drain current at $V_{GS} = -2$ V.
38. In an *n*-channel FET has the following parameters,

$$I_{DSS} = 15 \text{ mA}, V_P = -7 \text{ V and } g_{mo} = 4500 \text{ µs}$$

Determine the drain current and transconductance at $V_{GS} = -6$ V.

39. Determine the value of R_S for a self-bias *n*-channel JFET, when I_{DSS} = 40 mA, V_P = –11 V, and $V_{GS} = -4.5$ V.
40. Find the value of drain-to-source voltage (V_{DS}) and gate-to-source voltage (V_{GS}) for an *n*-channel JFET as shown in Fig. 1.86. Assume $I_D = 5$ mA.
41. Determine the operating point of a self-biased JFET, when $I_{DSS} = 12$ mA, $V_{GS} = -3$ V, $I_D = 4.9$ mA, $V_D = 6$ V and $V_{DD} = 11$ V. Find the value of R_D and R_S at this biasing condition.

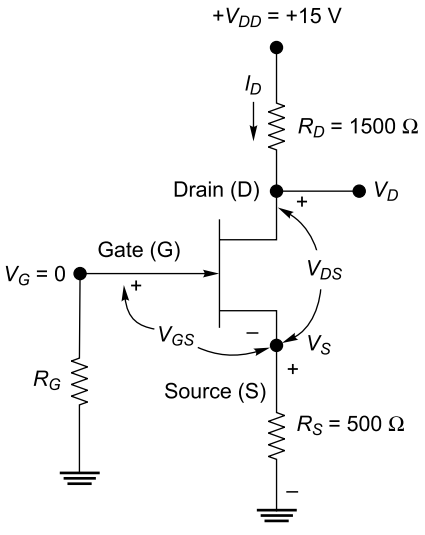


Fig. 1.86

42. A voltage divider biasing circuit of JFET is shown in Fig. 1.87. Determine the value of drain current I_D, gate-to-source voltage VGS, and drain-to-ground voltage V_D when $I_{DSS} = 6$ mA, $V_P = -5$ V, $R_D = 2000\ \Omega$, $R_S = 1500\ \Omega$, $R_1 = 700\ \text{k}\Omega$, $R_2 = 1\ \text{M}\Omega$ and $V_{DD} = 12$ V.

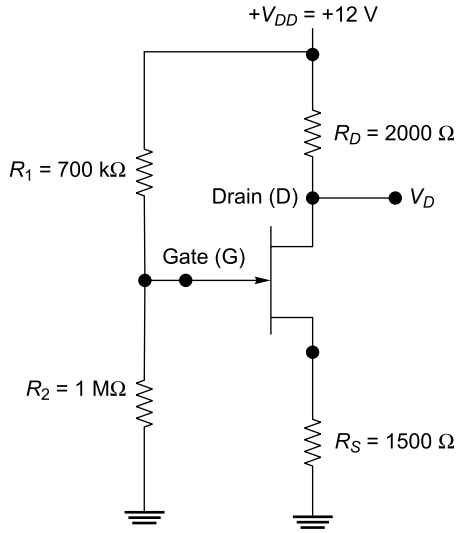


Fig. 1.87

43. Figure 1.88 shows a voltage divider biasing circuit of JFET. $I_{DSS} = 11$ mA, $V_P = -5$ V, $R_1 + R_2 = 700\ \text{k}\Omega$, $I_D = 6$ mA, $R_S = 500\ \Omega$ and $V_{DS} = 5$ V, compute the value of R_1, R_2 and R_D. Verify whether the JFET operates in saturation region. Assume $V_{DD} = 11$ V.

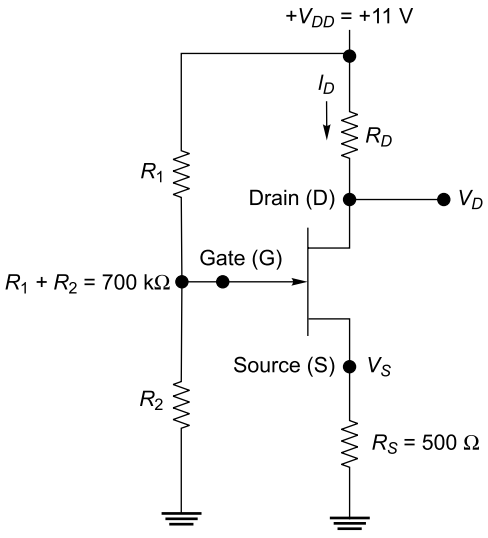


Fig. 1.88

44. A common source JFET amplifier has g_m of 6 mA/V. When the value of external drain resistance R_D is 2200 Ω, determine the value of voltage gain of amplifier.
45. A common source JFET amplifier has r_d of 550 kΩ and g_m of 5 mA/V. If the value of external load (drain) resistance R_D is 20 kΩ, find the value of voltage gain of the amplifier.
46. Figure 1.89 shows a common source JFET amplifier circuit. Determine the value of voltage gain of the amplifier, input resistance and output resistance. Assume r_d is 200 kΩ and g_m = 4 mA/V.

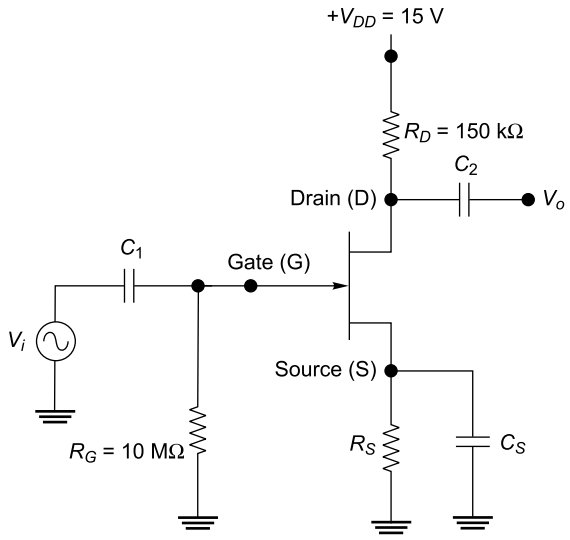


Fig. 1.89

47. A MOSFET amplifier operates at 250 KHz with the following parameters:

    r_d = 240 kΩ, g_m = 5 mA/V, C_{GS} = 3.3 pF, C_{GS} = 1.9 pF, C_{GD} = 2.8 pF and R_D = 15 kΩ

    Determine the voltage gain of the amplifier.
48. Figure 1.90 shows a common source JFET amplifier circuit. Determine the value of output voltage gain of the amplifier, if g_m = 4000 μS, and I_D = 6 mA. The effect of drain resistance is neglected.
49. Find the value of voltage gain of a FET amplifier as shown in Fig. 1.91. The FET has the following parameters:

    I_{DSS} = 15 mA, V_P = –5 V

    At the Q-point, I_{DQ} = 6 mA and V_{GS} = –2 V

    Assume that the effect of drain resistance is neglected.

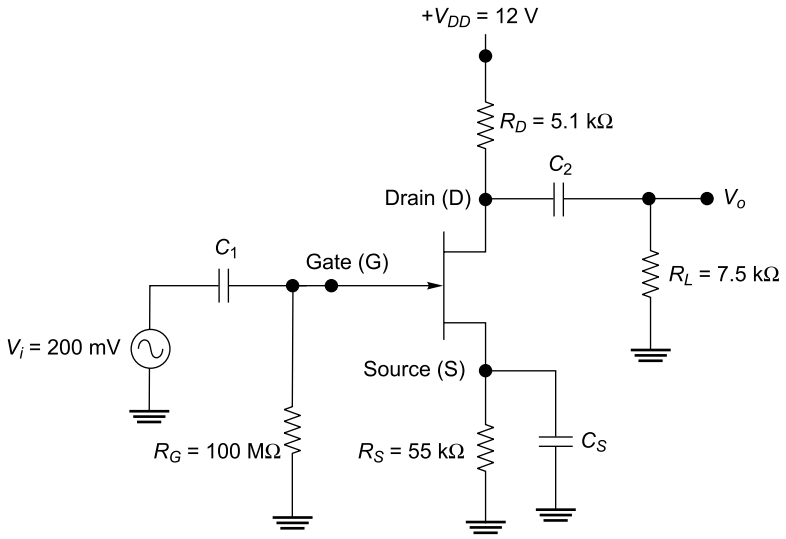


Fig. 1.90

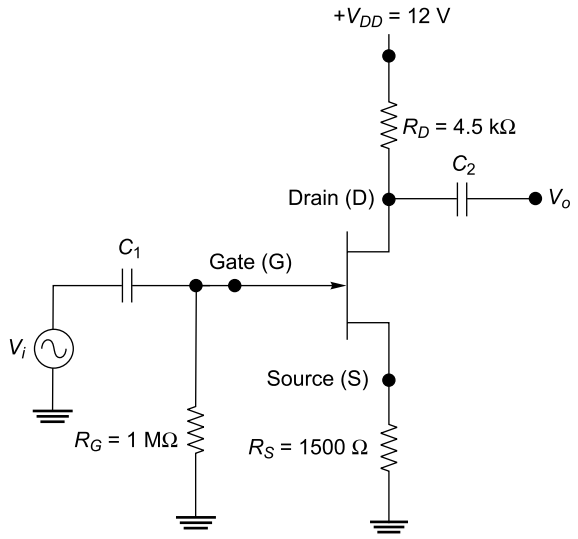


Fig. 1.91

50. Figure 1.92 shows a common drain JFET amplifier circuit. Determine the voltage gain of the amplifier, input resistance and output resistance if g_m = 10 mA/V. The effect of drain resistance is neglected.

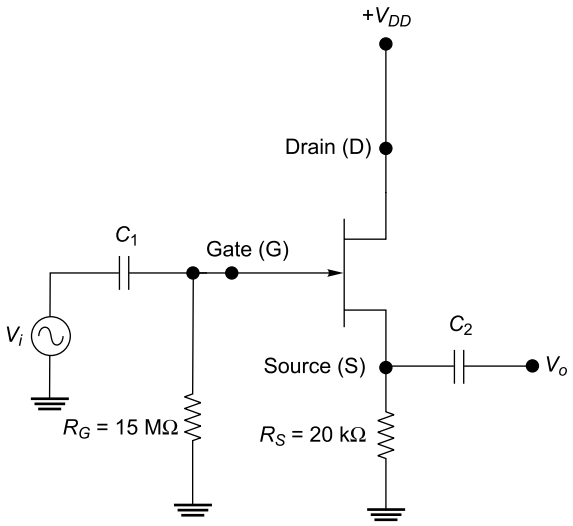


Fig. 1.92

51. Figure 1.93 shows a common gate JFET amplifier circuit. Determine the voltage gain input resistance and output resistance of the amplifier Assume that $g_m = 5000$ μS and $r_d = 55$ kΩ.

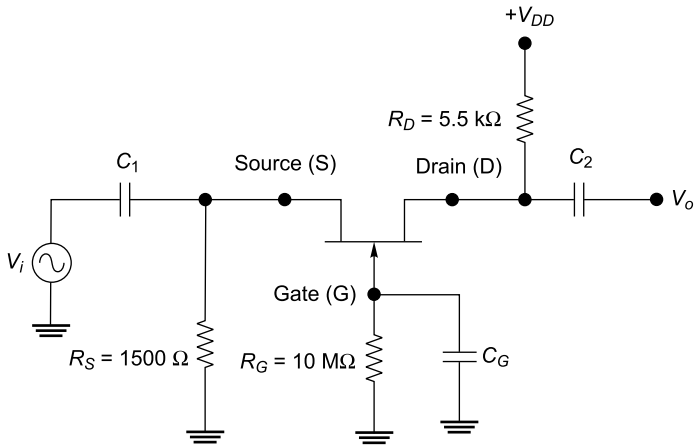


Fig. 1.93

MULTIPLE CHOICE QUESTIONS

1. A unipolar device uses
   (a) only free electrons
   (b) only holes
   (c) both electrons and holes
   (d) either electron or holes, but not both
   Answer: (d) either electron or holes, but not both

2. A bipolar transistor uses
   (a) only free electrons
   (b) only holes
   (c) both electrons and holes
   (d) either electron or holes, but not both
   Answer: (c) both electrons and holes
3. A field effect transistor operates on
   (a) minority carriers only
   (b) majority carriers only
   (c) positive and negative ions
   (d) positive charged ions
   Answer: (b) majority carriers only
4. The transconductance curve of JFET follows the equation

   (a) $I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_{GS(off)}}\right)^2$ (b) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$

   (c) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$ (d) $I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_{GS(off)}}\right)$

   Answer: (b) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$
5. When a JFET operates above pinch-off voltage,
   (a) drain current remain constant
   (b) drain current increase rapidly
   (c) drain current decrease gradually
   (d) depletion region becomes zero
   Answer: (a) drain current remain constant
6. CMOS stands for
   (a) *p*-channel MOS (b) *n*-channel MOS
   (c) complementary MOS (d) common MOS
   Answer: (c) Complementary MOS
7. The JFET is also called as square–law device as
   (a) resistance from drain to source varies inversely as square of the drain current
   (b) transconductance curve is parabolic
   (c) Reverse gate leakage current is directly proportional to the square of the reverse gate voltage
   (d) drain current varies as square of the drain voltage for a fixed gate-to-source voltage
   Answer: (b) transconductance curve is parabolic

8. During operation of *n*-channel depletion type MOSFET, the gate voltage has to be
   (a) negative (b) zero
   (c) low positive (d) high positive
   Answer: (a) negative
9. The *n*-channel MOSFETs are proffered more than *p*-channel MOSFETs as
   (a) *n*-channel MOSFETs have higher packing density compared to *p*-channel MOSFETs
   (b) *n*-channel MOSFETs are slower than *p*-channel MOSFETs *n*-channel
   (c) MOSFETs consumes less power than *p*-channel MOSFETs
   (d) *n*-channel MOSFETs have lower packing density than *p*-channel MOSFETs
   Answer: (a) *n*-channel MOSFETs have higher packing density compared to *p*-channel MOSFETs
10. As compared to *n*-channel MOS switch, the *p*-channel MOS switch has
   (a) high on state resistance
   (b) low on state resistance
   (c) same on state resistance
   Answer: (a) high on state resistance
11. Thermal runway cannot be developed in field effect transistor (FET) as the temperature of the FET increases
   (a) transconductance increases
   (b) drain current decrease
   (c) mobility decrease
   (d) mobility increases
   Answer: (a) transconductance increases
12. The transconductance g_m of a junction field effect transistor JFET can be expressed as

   (a) $g_m = \dfrac{2i_{DSS}}{V_P}\left(1 - \dfrac{V_{GS}}{V_P}\right)$ (b) $g_m = -\dfrac{2i_{DSS}}{V_P}\left(1 - \dfrac{V_{GS}}{V_P}\right)$

   (c) $g_m = -\dfrac{2i_{DSS}}{V_P}\left(1 + \dfrac{V_{GS}}{V_P}\right)$ (d) $g_m = -\dfrac{i_{DSS}}{V_P}\left(1 - \dfrac{V_{GS}}{V_P}\right)$

   Answer: (b) $g_m = -\dfrac{2i_{DSS}}{V_P}\left(1 - \dfrac{V_{GS}}{V_P}\right)$
13. An FET is better chopper than a BJT because it has
   (a) low offset voltage (b) high input current
   (c) high input resistance (d) high series ON resistance
   Answer: (c) high input resistance

14. In a biased JFET, the shape of the channel is shown in Fig. 1.94

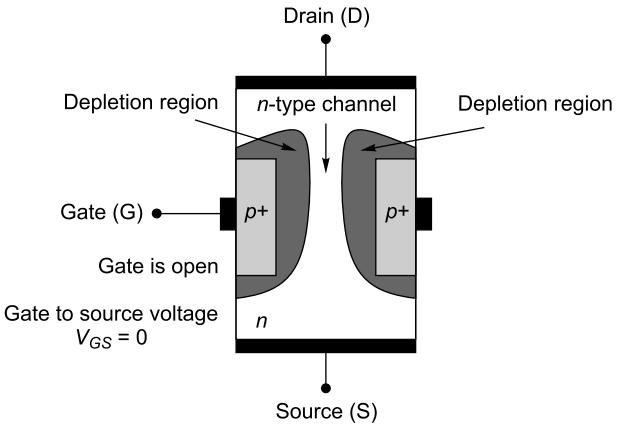


Fig. 1.94

(a) This is the property of the material used
(b) The drain end is more reverse biased than source end
(c) The drain end is more forward biased than source end

Answer: (b) The drain end is more reverse biased than source end

15. Which of the following statement relate to FET is true
(a) FET has low input impedance
(b) FET is less noisy than bipolar transistor
(c) FET has very large gain and bandwidth
(d) FET is a minority device

Answer: (b) FET is less noisy than bipolar transistor

16. A JFET is a
(a) Voltage controlled device with high input impedance
(b) Voltage controlled device with low input impedance
(c) Current controlled device with high input impedance
(d) Current controlled device with low input impedance

Answer: (a) Voltage controlled device with high input impedance

17. The input impedance of a JFET is in the range of
(a) Above 1 MΩ (b) 200 kΩ
(c) 2 kΩ (d) 200 Ω

Answer: (a) Above 1 MΩ

18. FET is a
(a) Voltage controlled device
(b) Current controlled device
(c) Impedance controlled device
(d) Resistance controlled device

Answer: (a) Voltage controlled device

19. The location of a *Q*-point on the dc load line of an FET amplifier is at
(a) mid-point (b) cut-off point

(c) saturation point (d) non-saturation point

Answer: (a) mid-point

20. Which biasing method provides a solid or most stable Q-point on a JFET amplifier
    (a) gate bias (b) self-bias
    (c) voltage divider bias (d) current source biasing

    Answer: (d) current source biasing

21. The voltage gain of a common source JFET amplifier is
    (a) $-r_L g_m$ (b) $r_L g_m$
    (c) $-\mu g_m$ (d) $-\mu r_L$

    Answer: (a) $-r_L g_m$

22. A common gate amplifier has
    (a) High input resistance and high output resistance
    (b) High input resistance and low output resistance
    (c) Low input resistance and low output resistance
    (d) Low input resistance and high output resistance

    Answer: (d) low input resistance and high output resistance

23. The voltage gain of a source follower or common drain JFET amplifier is

    (a) $A_v = \dfrac{R_S}{\dfrac{1}{g_m} + \dfrac{R_S}{r_d g_m} + R_S}$ (b) $A_v = \dfrac{R_G}{\dfrac{1}{g_m} + \dfrac{R_S}{r_d g_m} + R_S}$

    (c) $A_v = \dfrac{R_S}{\dfrac{1}{g_m} + \dfrac{R_G}{r_d g_m} + R_G}$ (d) $A_v = \dfrac{R_G}{\dfrac{1}{g_m} + \dfrac{R_G}{r_d g_m} + R_G}$

    Answer: (a) $A_v = \dfrac{R_S}{\dfrac{1}{g_m} + \dfrac{R_S}{r_d g_m} + R_S}$

24. When JFET is properly biased, JFET will act as
    (a) current controlled current source
    (b) voltage controlled current source
    (c) voltage controlled voltage source
    (d) current controlled voltage source

    Answer: (c) voltage controlled voltage source

25. The pinch-off voltage is equal to
    (a) Drain-to-source voltage
    (b) Gate-to-source voltage
    (c) Gate-to-source cut-off voltage
    (d) Gate voltage

    Answer: (c) Gate-to-source cut-off voltage

26. Compared to BJT, FET has higher
    (a) input impedance (b) output impedance

(c) current (d) voltage gain

Answer: (a) input impedance

27. The gate of FET controls
    (a) width of the channel (b) drain current
    (c) gate voltage (d) all of these

    Answer: (d) all of these

28. The gate-to-source diode of a JFET should be
    (a) reverse biased
    (b) forward biased
    (c) either forward biased or reverse biased
    (d) none of these

    Answer: (a) reverse biased

29. The voltage gain of a source follower or common drain JFET amplifier is
    (a) about unit (b) about 2
    (c) about 10 (d) about 100

    Answer: (a) about unit

30. When the gate voltage is more negative in an *n*-channel JFET, the channel width between the depletion layers
    (a) expands (b) shrinks
    (c) stops conducting (d) increase conducting

    Answer: (b) shrinks

31. Transconductance is measured in
    (a) Mhos or siemens (b) Ohms
    (c) Volts (d) Amperes

    Answer: (a) Mhos or siemens

32. If a JFET operates in cut off, the depletion layers are
    (a) touching each other
    (b) close together
    (c) far apart

    Answer: (a) touching each other

33. Transconductance represents how effectively the input voltage controls the
    (a) output current (b) voltage gain
    (c) input impedance (d) output impedance

    Answer: (a) output current

34. The input impedance of a JFET is
    (a) about zero (b) about infinity
    (c) about 100 Ω (d) about 10 kΩ

    Answer: (b) about infinity

35. The transconductance curve is
    (a) linear
    (b) non-linear or parabolic
    (c) drain characteristics

    Answer: (b) non-linear or parabolic

UNIVERSITY QUESTIONS WITH ANSWERS

Multiple-Choice-Type Questions

1. "*X*" has very high input impedance and low output impedance. *X* may be
   (a) FET and OP-AMP (b) FET and Transistor
   (c) Op-Amp and Transistor (d) None of these [WBUT-2007]
2. When the gate-to-source voltage V_{GS} of *n*-channel JFET is made more negative the drain current
   (a) increases (b) decreases
   (c) remains constant (d) many increase or decrease
   [WBUT-2007]
3. Compared to the BJT, FET
   (i) has a large gain bandwidth product
   (ii) is less noisy
   (iii) has less input resistance
   (iv) has only majority carrier flow the correct statements are
   (a) i and iii (b) i and ii (c) ii and iv (d) iii and iv [WBUT-2008]
4. Which of the following is not true about a JFET?
   (a) It is a current controlled device
   (b) It is a majority carrier device
   (c) Drain and source are interchangeable in a JFET
   (d) It can be used as a voltage variable resistor [WBUT-2008]
5. JFET is a
   (a) current control device
   (b) voltage control device
   (b) temperature control device
   (d) none of these [WBUT-2008]
6. A JFET
   (a) is a voltage controlled device
   (b) is a current controlled device
   (c) has a low input resistance
   (d) has a very large output resistance [WBUT-2009]
7. JFET is a
   (a) voltage controlled voltage source
   (b) voltage controlled current source
   (c) current controlled voltage source
   (d) current controlled current source [WBUT-2009]

Solutions

1. (a) FET and OP-AMP
2. (b) decreases
3. (c) ii and iv
4. (a) It is a current controlled device
5. (b) voltage control device
6. (a) is a voltage controlled device
7. (a) voltage controlled voltage source

Short- and Long-Answer-Type Questions

1. Why FET is called unipolar transistor? [WBUT-2002]

   Solution

   In a field effect transistor, current is conducted by only majority carriers, i.e., may be either electrons or holes. Due to this, FET is called unipolar transistor.

2. With a neat diagram explain the operation of JFET. What is meant by pinched-off voltage? [WBUT-2002]

   Solution Refer to Section 1.4

3. Explain pinch-off voltage for a JFET [WBUT-2003]

   Solution Refer to Section 1.4

4. What do you mean by inversion layer for an enhancement MOSFET? [WBUT-2003]

   Solution

   When the substrate of an enhancement-type MOSFET is grounded and a negative voltage is applied at the gate, the positive charges (minority carrier in the *n*-type substrate) are induced on the substrate side between source and drain region due to negative gate voltage. This induced minority carrier layer in the substrate is called the inversion layer. The width of inversion layer depends on the magnitude of the negative gate voltage.

5. What are the basic difference between BJT and FET? [WBUT-2003]

   Solution Refer to Section 1.8

6. With a neat diagram draw and explain the basic structure of *n*-channel JFET. [WBUT-2003]

   Solution Refer to Section 1.4

7. Draw and explain the drain characteristics of an *n*-channel enhancement MOSFET [WBUT-2003]

   Solution Refer to Section 1.13.2

8. The following readings were obtained experimentally from a FET

V_{GS}	0 V	0 V	0.2 V
V_{DS}	7 V	15 V	15 V
I_D	10 mA	10.25 mA	9.65 mA

   Define and determine (i) ac drain resistance (ii) transconductance (iii) amplification factor

   Solution [WBUT-2003]

   AC *drain resistance (r_d):* The reciprocal of the slope of the drain characteristics is called drain resistance and it is defined by

$$r_d = \left.\frac{\partial V_{DS}}{\partial i_D}\right|_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta i_D} \text{ where, } V_{GS} \text{ is constant.}$$

Hence, r_d is the ratio of a small change in the drain voltage ΔV_{DS} to the corresponding small change in the drain current Δi_D while gate voltage V_{GS} held constant. The unit of r_d is ohms.

$$\Delta V_{DS} = 15 - 7 = 8 \text{ V}$$
$$\Delta I_D = 10.25 - 10 = 0.25 \text{ mA}$$

$$r_d = \frac{\Delta V_{DS}}{\Delta i_D} = \frac{8}{0.25 \times 10^{-3}} = 32 \text{ k}\Omega$$

Transconductance (g_m): It is the slope of the transfer characteristics curves and it is represented by g_m. It can be expressed by

$$g_m = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} = \frac{\Delta i_D}{\Delta V_{GS}} \text{ when } V_{DS} \text{ is constant.}$$

From the above equation, g_m is defined as it is the ratio of a small change in drain current Δi_D to the corresponding small change in the gate-to-source voltage ΔV_{GS} when drain voltage V_{DS} is constant. g_m is also known as mutual conductance. The unit of transconductance is mho.

$$\Delta I_D = 9.65 - 10.25 = -0.6 \text{ mA}$$
$$\Delta V_{GS} = 0.2 - 0 = 0.2 \text{ V}$$

$$g_m = \frac{\Delta i_D}{\Delta V_{GS}} = \frac{-0.6 \times 10^{-3}}{0.2} = -3 \times 10^{-3} \text{ mho}$$

Amplification factor (μ): The amplification of JFET is defined by

$$\mu = -\left.\frac{\partial V_{DS}}{\partial V_{GS}}\right|_{I_D} = -\frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ when } i_D \text{ is constant.}$$

Actually, μ is the ratio of a small change in the drain voltage ΔV_{DS} to the small change in the gate voltage ΔV_{GS} when drain current held at constant. The negative sign represents that when V_{GS} is increased, V_{DS} will be decreased at constant drain current.

We know that $\mu = g_m r_d = -3 \times 10^{-3} \times 32 \times 10^3 = -96$

9. Draw the circuit diagram of common source amplifier. Derive an expression for voltage gain. [WBUT-2003]

Solution Refer to Section 1.22.1

10. A FET amplifier in the common source configuration uses a load resistance of 150 kΩ. The ac drain resistance of the device is 100 kΩ and the transconductance is 0.5 mA/V. What is the voltage gain of the amplifier? [WBUT-2004]

Solution

Given $r_d = 100 \text{ k}\Omega$, $R_L = 150 \text{ k}\Omega$ and $g_m = 0.5 \text{ mA/V}$

The amplification factor is $\mu = g_m r_d$

The voltage gain is $A_v = \dfrac{\mu R_L}{r_d + R_L} = \dfrac{g_m r_d R_L}{r_d + R_L}$

$$= \frac{0.5 \times 10^{-3} \times 100 \times 10^3 \times 150 \times 10^3}{(100 \times 10^3) + (150 \times 10^3)} = 30$$

11. What do you mean by the static characteristics of a JFET? Give necessary circuit diagram. [WBUT-2004]

Solution Refer to Sections 1.5.1 and 1.5.2

12. What is the function of gate in JFET? [WBUT-2004]

Solution

JFET is a voltage controlled device and the gate voltage controls the amount of drain current which is the output current. When the gate-to-source voltage (V_{GS}) is zero, maximum drain current flows through the JFET. If the gate voltage becomes more negative, the drain current will be smaller.

13. Compare the performance of JFET and BJT. [WBUT-2005]

Solution Refer to Section 1.8.

14. Describe the operation of an *n*-channel JFET. [WBUT-2005]

Solution Refer to Section 1.4

15. Draw the small signal equivalent of a common source JFET. [WBUT-2005]

Solution

The small signal equivalent of a common source JFET is shown below:

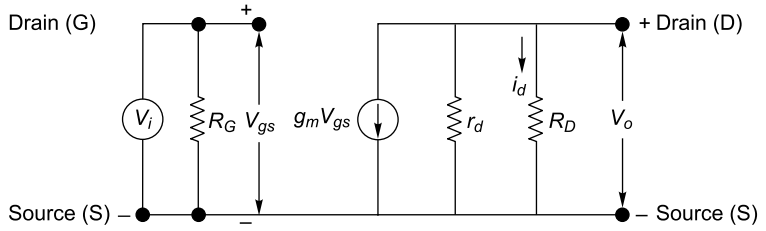


Fig. 1.95 ***Equivalent circuit of common source amplifier***

16. Handling precaution of MOSFET [WBUT-2005]

Solution

MOSFET gets damaged easily being very susceptible to overload voltage. Consequently, MOSFET requires special handling and precautions during installation. When someone picks up the transistor from its case and brushes the gate against some grounded object, there will be a huge electrostatic discharge. Therefore, MOSFET is protected by a shorting ring which is wrapped around all four terminals during shipping. This device must be remaining in place until after the device is soldered in to position. Before soldering, the technician should use a soldering strap to discharge static electricity during soldering and make sure that the tip of the soldering iron

must be grounded. When the power is ON, the MOSFET should never be inserted into or removed from a circuit. So that MOSFETs have a built in gate protection known as integral gate protection, a system built into the device to get around the problem of high voltage on the gate causing a puncturing of the oxide layer.

17. Why do field effect transistors not draw any dc current through gate under normal operation? [WBUT-2006]

Solution

Dc can not pass through the field effect transistor because of the capacitance effect of a gate.

18. Draw the circuit diagram of source following using JFET and explain its operation. What is the highest voltage gain available from such an amplifier circuit? Comment on the input and output impedance? [WBUT-2006]

Solution Refer to Section 1.22.2

19. What is understood by pinch-off voltage of an FET? For a depletion mode *n*-channel MOSFET, the pinch-off voltage is negative with respect to source– explain. For enhancement mode *p*-channel MOSFET. What is the polarity of pinch-off voltage? [WBUT-2006]

Solution

When the negative voltage at the gate is increased, depletion layers touched at center and drain current I_D is completely cut off. The gate to source voltage at which the drain current I_D is completely cut off (pinched off) is called the pinch-off voltage.

For depletion mode *n*-channel MOSFET, V_{GS} must be negative for reducing the channel width or channel narrowing which is responsible for pinch-off.

For enhancement mode *p*-channel MOSFET, the polarity of pinch-off voltage is positive.

20. Write a short note on

(i) Enhancement and Depletion MOSFET [WBUT-2007], [WBUT-2009]

Solution Refer to Section 1.13 and 1.14.

21. What are the basic differences between BJT and FET? [WBUT-2007]

Solution Refer to Section 1.8.

22. (a) Why a FET known as unipolar device? [WBUT-2008]

Solution Refer to Answer of Question 1.

(b) What is pinch-off phenomenon in a JFET?

Solution Refer to Section 1.4, Fig. 1.12 and Fig. 1.13.

(c) How do you compare this device with a BJT?

Solution Refer to Section 1.8.

23. What the disadvantages of FET over BJT?

Solution
The only disadvantage of FET is that it has comparatively small gain bandwidth product compared to BJT.

24. Why is FET called unipolar transistor? [WBUT-2008]
Solution Refer to Answer of Question 1.

25. What do you mean by pinch-off condition in JFET? [WBUT-2008]
Solution Refer to Section 1.4.

26. As V_{GS} is changed from –1 V to –1.5 V keeping V_{DS} constant, I_D of a FET drops from 7 to 5 mA. What is the transconductance of the FET? If the ac drain resistance is 200 kΩ, find also the amplification factor of the FET. [WBUT-2008]

Solution

$$\text{Thansconductance is } g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ when } V_{DS} \text{ is constant}$$

$$= \frac{(5-7)\times 10^3}{-1.5-(-1)} = 4\times 10^{-3} \text{ mho}$$

The ac drain resistance r_d is 200 kΩ
The amplification factor of the FET is

$$\mu = g_m r_d = 4\times 10^{-3}\times 200\times 10^3 = 800$$

27. Explain the operation of an *n*-channel JFET with suitable diagrams for
(i) $V_{GS} > 0$
(ii) $V_{GS} < 0$
(iii) $V_{GS} = 0$ [WBUT-2008]

Solution Refer to Section 1.4.

28. Define parameters μ, r_d, and g_m. Deduce the relationship $\mu = r_d g_m$. [WBUT-2008]

Solution Refer to Section 1.6.

29. What are the basic differences between BJT and FET? Define pinch off voltage. [WBUT-2009]

Solution Refer to Section 1.8 and Section 1.4.

30. Differentiate between depletion and enhancement type MOSFETs. [WBUT-2009]

31. Compare between an FET and a BJT. [WBUT-2010]

Solution Refer to Section 1.8.

32. Write the working principle of JFET with a diagram. [WBUT-2010]

Solution Refer to Section 1.4.

33. Define transconductance, ac drain resistance, amplification factor of JFET [WBUT-2010]

Solution Refer to Section 1.6.

34. Draw the common source JFET amplifier circuit and find out the expression for voltage gain, input impedance and output impedance. [WBUT-2010]

Solution Refer to Section 1.22.1.

35. Write three differences between JFET and MOSFET. [WBUT-2010]

Solution

JFET	*MOSFET*
In JFET, the transverse electric field is developed across the reverse biased *pn* junction which controls the conductivity of the channel.	In enhancement and depletion types MOSFET, the transverse electric field is induced across an insulating layer deposited on the semiconductor material which controls the conductivity of the channel.
The gate leakage current of a JFET is about 10^{-9} A and its input resistance is of the order of 10^8 ohms.	The gate leakage current in a MOSFET is about 10^{-12} A. Therefore, the input resistance of MOSFET is very high in the order of 10^{10} to 10^{15} ohms.
The output characteristics of JFET are flatter than those of the MOSFET. Therefore, the drain resistance of a JFET is about 1 MΩ which is much higher than that of MOSFET.	The drain resistance of a MOSFET is about 50 kΩ which is much lower than that of JFET.
JFET can be operating only in the depletion mode.	The depletion type MOSFET can be operate in both depletion and enhancement mode.
Compared to MOSFETs, JFET are complex to fabricate.	Compared to JFET, MOSFETs are easier to fabricate.
Compared to MOSFET, JFET is less susceptible to overload voltage.	MOSFET is very susceptible to overload voltage and needs special handling during installation. This device can be damaged easily if it is not properly handled.

2 FEEDBACK AMPLIFIER

2.1 INTRODUCTION

Usually, amplifier circuits are used in signal processing systems to provide good voltage gain. Therefore, amplifier circuits are called *voltage amplifiers*. The example of an amplifier circuit is an audio amplifier. The simplified block diagram of audio amplifier is shown in Fig. 2.1 which consists of a microphone, small signal amplifiers, large signal amplifiers and a speaker. The microphone generates a very small signal, in some millvolt range and fed to small signal voltage amplifiers. The first two stages (small-signal stages) of the amplifier are used to amplify the small voltage audio signal and it becomes larger in voltage level, but in low current. The output of the small signal stages of amplifier is fed to the last-stage amplifier which is known as a *power amplifier*. The power amplifiers are able to handle large voltage and current swings as they have larger power gain and high efficiency.

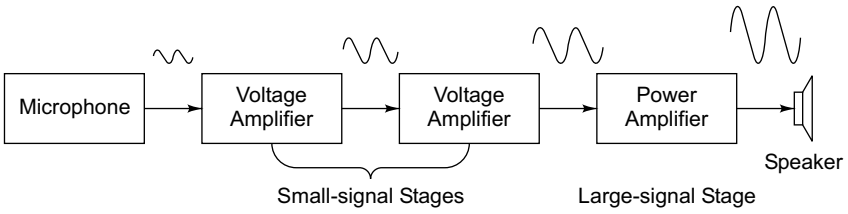


Fig. 2.1 *Block diagram of an audio amplifier*

Due to changes in ambient temperature, device (BJT or FET) parameters are varied. Therefore gain stability of practical amplifiers is not very high. In case of BJT amplifier circuits, this problem is very acute. The gain stability can be moderately improved by using feedback technique. The feedback in amplifiers gives better performance in different way such as

(i) Increased stability in the amplification, the gain is less dependent on device parameters

(ii) Higher input impedance
(iii) Lower output impedance
(iv) Feedback reduces distortion in the amplifier
(v) Bandwidth of the amplifier is increased leading to improved frequency response
(vi) Linear operation over a wide range

The above advantages are achieved at the expense of gain which is much less than the amplifier gain without feedback. The other disadvantages of feedback amplifiers are the following:

(i) The feedback amplifier may lead to instability if it is not designed properly.
(ii) Gain of the amplifier decreases.
(iii) Input and output impedances of feedback amplifier are sensitive with open-loop gain of amplifier, and parameter variations.

In this chapter, the basic concept of a feedback amplifier, positive and negative feedback, topologies of feedback amplifier, effect of feedback on gain, input impedance, output impedance, sensitivities, bandwidth stability and applications of feedback amplifiers are discussed elaborately.

2.2 FEEDBACK AMPLIFIER

A feedback amplifier is an electronic circuit in which the output signal is sampled and fed back to the input to generate an error signal which drives the amplifier. Generally feedback amplifiers are of two types as given below:

- Negative feedback amplifier
- Positive feedback amplifier

2.2.1 Negative Feedback Amplifier

Figure 2.2 shows the basic block diagram of a negative feedback amplifier (non-inverting type amplifier).

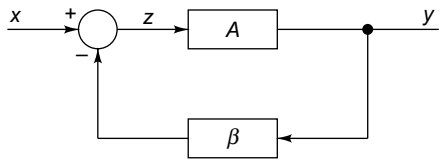


Fig. 2.2 *Negative feedback amplifier (non-inverting type)*

Here, x is the input signal
y is the output signal
z is the error signal
A is amplifier gain
β is the gain of feedback path

Depending on the types of feedback, the variables x, y and z are voltages or currents. The gain around the loop is negative and it is equal to $-\beta A$ where both A and β are positive real constants. Due to the loop gain being negative; the feedback is called negative feedback.

The output of feedback is $-\beta.y$.
The error signal can be computed as $z = x - \beta.y$
Then output signal is $y = A.z = A(x - \beta.y)$

The overall gain is equal to $A_f = \dfrac{y}{x} = \dfrac{A}{1+\beta.A}$

where, A is the gain without back or open-loop gain
A_f is the gain of amplifier with feedback or closed-loop gain

It is justified from the above expression that the effect of the feedback is to reduce the gain by the factor $(1 + \beta A)$. This factor is called *amount of feedback*. Commonly, it is specified in decibel (dB) by the relation 20 log $|1 + \beta A|$.

The amount of feedback is expressed by the following relationship as given below:

$$\text{Amount of feedback in dB} = 20\log_{10}\left|\frac{A_f}{A}\right| = 20\log_{10}\left|\frac{1}{1+\beta A}\right|$$

In negative feedback, the amount of feedback is negative as $|1+\beta A| > 1$, but during positive feedback, the amount of feedback is positive as $|1+\beta A| < 1$.

The basic block diagram of inverting feedback amplifier is depicted in Fig. 2.3. In this figure, x is the input signal, y is the output signal and z is the error signal. The gain around the loop is negative and it is equal to $-\beta A$ where both A and β are positive real constants. As the loop gain is negative, the feedback is said to be negative.

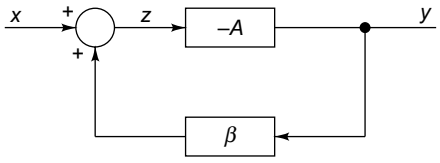


Fig. 2.3 ***Negative feedback amplifier (inverting type)***

This amplifier has an inverting gain, and the feedback signal must be added to the input signal to determine error signal.

The output of feedback is $\beta.y$.

In the inverting amplifier, the error signal is $z = x + \beta.y$. If x is positive and y is negative, so that the error signal represents a difference signal.

Then output signal will be $y = -A.z = -A(x+\beta.y)$

Then overall gain will be $A_f = \dfrac{y}{x} = \dfrac{-A}{1+\beta.A}$

Hence, the amount of feedback for inverting amplifier is the same as for the non-inverting amplifier.

When A is very large, $\beta A >> 1$, the gain of the negative feedback (non-inverting type) amplifier is about

$$A_f = \frac{y}{x} \cong \frac{A}{\beta.A} = \frac{1}{\beta}$$

The gain of the inverting type amplifier is approximated by

$$A_f = \frac{y}{x} \cong \frac{-A}{\beta.A} = -\frac{1}{\beta}$$

Therefore, the gain is set by the feedback network and not by the amplifier. The amplifier without feedback can be designed with the high gain. But when feedback is added, the gain can be reduced to any desired value by the feedback circuit.

2.2.2 Positive Feedback Amplifier

The basic block diagram of a positive feedback amplifier is depicted in Fig. 2.4(a). In this figure, x is the input signal, y is the output signal and z is the error signal. The gain around the loop is positive and it is equal to βA where both A and β are positive real constants. The amplifier has positive feedback which causes it to be unstable. This amplifier has a gain A, and the feedback signal must be added to the input signal to determine error signal.

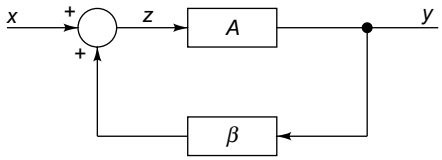


Fig. 2.4(a) *Positive feedback amplifier*

The output of feedback is $\beta.y$.

The error signal can be computed as $z = x + \beta.y$

Then output signal is $y = A.z = A(x + \beta.y)$

The overall gain is equal to $A_f = \frac{y}{x} = \frac{A}{1-\beta.A}$

In the positive feedback amplifier, the error signal is $z = x + \beta.y$. If x is positive and y is negative, the error signal represents a difference signal.

When A is the voltage gain (Output Voltage/Input Voltage) or A is the current gain (Output Current/Input Current), the product βA is dimension less and β is also dimensionless. If A is the transconductance gain (Output Voltage/Input Current), β has the units of ohms (Ω). When A is the transresistance gain (Output Current/input Voltage), the units of β will be siemens (S). Actually, the gains are phasor functions of frequency. This creates a stability problem in feedback amplifier. If frequency is increased, absolute value of $|A|$ must be decreased as each amplifier has a finite bandwidth. Therefore, the decrease in $|A|$ go along with a phase shift so that βA can be a negative real number at some frequency. If $\beta A = -1$ at some frequency, we can say from the expression $A_f = \frac{y}{x} = \frac{A}{1+\beta.A}$ that the overall gain becomes infinite at that frequency. Therefore, an amplifier with an infinite gain at any frequency can generate an output signal at that frequency without any input signal. Then the amplifier is called *oscillator*. A negative feedback amplifier will oscillate if $|\beta A| \geq 1$ at any frequency when βA is a negative real number and the phase of βA will be 180°.

2.2.3 Feedback Factor

Figure 2.4(b) shows a negative feedback system with positive gain, A and feedback, β. The summing junction at its input subtracts the feedback signal from the input signal to form the error signal $V_{in} - \beta A$, which drives the system. By using the basic closed-loop circuit as depicted in Fig. 2.4(b), we can derive the following general feedback equations:

The open-loop voltage gain is $A = \dfrac{V_{out}}{V_{in}}$

or, $V_{out} = AV_{in} = A(V_{in} - \beta V_{out})$ where, β is the feedback fraction

$= AV_{in} - A\beta V_{out}$ where $A\beta$ is the loop gain

Therefore, $AV_{in} = (1 + A\beta)\, V_{out}$

$\therefore \quad \dfrac{V_{out}}{V_{in}} = \dfrac{A}{1 + A\beta}$ where $1 + A\beta$ is the feedback factor

It is clear from the above equation that the effect of the negative feedback is to reduce the gain by the factor of $1 + \beta A$. This factor is called the "feedback factor" or "amount of feedback" and is often specified in decibels (dB) by the relationship of 20 log $(1+ \beta G)$.

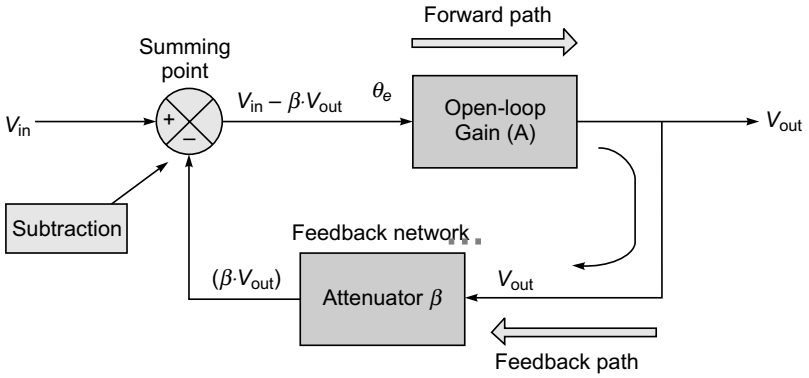


Fig. 2.4(b) ***Negative feedback system***

2.1 A power amplifier with a gain of 100 has an output voltage of 12 V. A negative feedback is provided to reduce the gain to 25%. What should be the gain of the feedback path?.

Solution

Gain of amplifier $A = 100$

Due to negative feedback, the overall gain is reduced to 25% of actual gain.

$A_f = 0.25$ A

The overall gain $A_f = \dfrac{A}{1 + \beta A}$

or, $$\frac{100}{1+\beta\times100}=0.25\times100$$

Then gain of the feedback path is $\beta = 0.03$

2.2 A feedback amplifier consists of two amplifying blocks and each amplifying block has a gain of 100.

(a) What should be the gain of the feedback block in order to maintain an overall gain of 90?

(b) When the gain of each amplifier block has been reduced to 50% of the actual value due to parameter variation, what is the % change in the overall gain of the feedback amplifier?

Solution

(a) Two amplifying blocks are connected in cascade and gain of each amplifying block is $A_1 = 100$

The gain of amplifier $A = A_1 \times A_1 = 100 \times 100 = 10^4$

The overall gain of feedback amplifier $A_f = \dfrac{A}{1+\beta A} = \dfrac{10^4}{1+\beta\times10^4}$

When $A_f = 90, \quad 90 = \dfrac{10^4}{1+\beta\times10^4}$

The gain of the feedback block is $\beta = (10^4 - 90)/(90\times10^4) = 0.011011$

(b) When the gain of each amplifier block has been reduced to 50% of the actual value, the gain of each amplifier block is $A'_1 = 50\% \times A_1 = \dfrac{50}{100}\times100 = 50$

New gain of amplifier $A' = A'_1 \times A'_1 = 50 \times 50 = 2500$

The new overall gain of feedback amplifier

$$A_f' = \frac{A'}{1+\beta A'} = \frac{50^2}{1+0.011011\times50^2} = \frac{2500}{28.5275} = 87.634$$

Reduction in over all gain = $A_f - A_f' = 90 - 87.634 = 2.366$

The % change in the overall gain of feedback amplifier

$$= \frac{A_f - A_f'}{A_f}\times100 = \frac{2.366}{90}\times100 = 2.62\%$$

2.3 An amplifier provides a gain of $A = 200$.

(a) Determine the feedback path gain to provide overall gain of $A_f = 100$

(b) If A is increased by 1%, calculate the new A_f. What is the percentage change in A_f?

Solution

(a) Given $A = 200$ and $A_f = 100$

The feedback path gain = β

Overall gain of the system $A_f = \dfrac{A}{1+\beta A}$

After substituting the value of A and A_f, we get

$$\frac{200}{1+\beta\times 200} = 100$$

Then the feedback path gain is $\beta = 100/(200 \times 100) = 0.005$

(b) As A is increased by 1%, the new value of A is $A' = 1.01 \times 200 = 202$

The new value of A_f is $A_f' = \dfrac{A'}{1+\beta A'} = \dfrac{202}{1+0.005\times 202} = 100.4975$

The percentage change in A_f is

$$\frac{A_f - A_f'}{A_f}\times 100$$

$$= \frac{100-100.4975}{100}\times 100 = \frac{-0.4975}{100}\times 100 = -0.4975\%$$

2.4 An amplifier has gain of –1000 and feedback of $\beta = -0.1$. If it had a gain change 10% due to temperature, what will be the change in gain of the feedback amplifier?

Solution

Assume amplifier gain $A = -1000$, feedback path gain $\beta = -0.1$ and

change in amplifier gain is $\dfrac{\partial A}{A} = 10\% = 0.1$

The overall gain of the system is $A_f = \dfrac{A}{1+\beta A}$

The rate of change in gain is $\dfrac{\partial A_f}{\partial A} = \dfrac{1+\beta A-\beta A}{(1+\beta A)^2}$

or, $$\partial A_f = \partial A \times \frac{1}{(1+\beta A)^2}$$

or, $$\frac{\partial A_f}{A_f} = \frac{\dfrac{\partial A}{A}}{(1+\beta A)}$$

or, $$\frac{\partial A_f}{A_f}\times 100 = \frac{\dfrac{\partial A}{A}}{(1+\beta A)}\times 100$$

$$= \frac{0.1}{1+(-1000)(-0.1)}\times 100 = 0.099\%$$

2.3 CLASSIFICATION OF AMPLIFIERS

To understand the basic concept of feedback, amplifiers are classified into four different categories such as

(i) Voltage amplifiers
(ii) Current amplifiers
(iii) Transconductance amplifiers
(iv) Transresistive amplifiers

Usually, the type of amplifiers can be determined based on the magnitudes of the input and output impedances of an amplifier with respect to source and load impedances. In this section, voltage amplifiers, current amplifiers, transconductance amplifiers and transresistive amplifiers are explained in detail.

2.3.1 Voltage Amplifiers

Figure 2.5 shows the Thevenin's equivalent circuit of a voltage amplifier. In this circuit,

V_s = Supply voltage, V_i = Input voltage, V_o = Output voltage
R_s = Source resistance, R_L = Load resistance, R_i = Input resistance
R_o = Output resistance, I_i = Input current and I_o = Output current

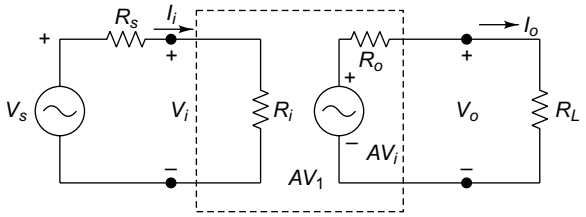


Fig. 2.5 *Equivalent circuit of a voltage amplifier*

The source voltage can be expressed as $V_s = I_i R_s + V_i$ and input voltage $V_i = I_i R_i$
Therefore, $V_s = I_i R_s + I_i R_i$

When $R_i >> R_s$, $V_s \approx I_i R_i = V_i$

If input resistance R_i of voltage amplifier is very large compared to source resistance R_s, supply voltage is equal to input voltage $V_s = V_i$

The output voltage is $V_o = A_v V_i + I_o R_o = I_o R_L$

If $R_L >> R_o$, $A_v V_i = I_o R_L = V_o$

In this amplifier, load resistance R_L is very large compared to output resistance and output voltage $V_o = A_v V_i = A_v V_s$ as $V_s = V_i$.

Voltage amplifier gain $A_v = \dfrac{V_o}{V_s}$

Therefore, we can say that output voltage is proportional to input voltage and proportionality factor A_v is independent of the magnitude of the source and load resistance. This circuit is called *voltage amplifier*. An ideal voltage amplifier should have infinite input resistance $R_i = \infty$ and zero output resistance $R_o = 0$.

2.3.2 Current Amplifiers

Figure 2.6 shows the Norton's equivalent circuit of a current amplifier. In this circuit,

I_s = Source current, R_s = Source resistance, I_i = Input current,
R_i = Input resistance, I_o = Output current, V_o = Output voltage,
R_o = Output resistance and R_L = Load resistance.

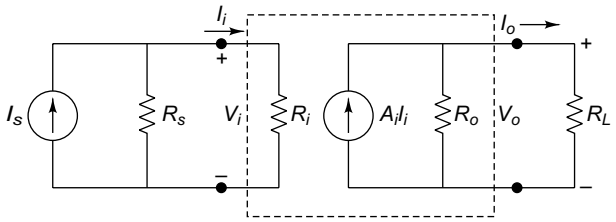


Fig. 2.6 *Equivalent circuit of a current amplifier*

The input current can be expressed as $I_i = I_s \dfrac{R_s}{R_s + R_i}$

If $R_s >> R_i$, $\quad I_i \approx I_s$

In a current amplifier circuit, source resistance R_s is very large compared to R_i and source current is equal to input current.

The output current can be expressed as

$$I_o = A_i I_i . \frac{R_o}{R_o + R_L}$$

If $R_o >> R_L$, $I_o = A_i I_i . = A_i I_s$ as $I_i = I_s$

Hence output current is proportional to the input current I_s and current amplifier gain A_i

Then current amplifier gain is $A_i = \dfrac{I_o}{I_s}$

Therefore, in a current amplifier, output current is proportional to the input current signal and the proportionality factor (A_i) and it is independent of R_s and R_o. An ideal current amplifier should have zero input resistance (R_i = 0) and infinite output resistance ($R_o = \infty$).

2.3.3 Transconductance Amplifiers

Figure 2.7 shows a transconductance amplifier which is represented by a Thevenin's equivalent in input circuit and a Norton's equivalent in output circuit.

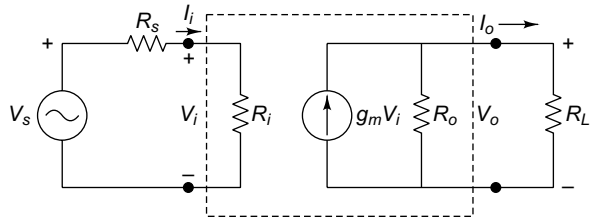


Fig. 2.7 *Equivalent circuit of a transconductance amplifier*

The source voltage can be expressed as

$$V_s = I_i R_s + V_i$$

or, $V_s = I_i R_s + I_i R_i$ as input voltage $V_i = I_i R_i$

If $R_i >> R_s$, $V_s \approx I_i R_i = V_i$

Therefore, source voltage is equal to input voltage as $R_i >> R_s$.

The output current can be expressed as

$$I_o = g_m V_i . \frac{R_o}{R_o + R_L}$$

If $R_o >> R_L$, $I_o = g_m V_i . = g_m V_s$ as $V_i = V_s$

The transconductance amplifier gain is $g_m = \frac{I_o}{V_s}$

In an ideal transconductance amplifier, output current is proportional to the supply voltage and the proportionality factor (g_m) and it is independent of R_i and R_o. This amplifier should have infinite input resistance $R_i = \infty$ and infinite output resistance ($R_o = \infty$).

2.3.4 Transresistive Amplifiers

The equivalent circuit of a transresistive amplifier is depicted in Fig. 2.8. It is represented by Norton's equivalent in input circuit and a Thevenin's equivalent in its output circuit.

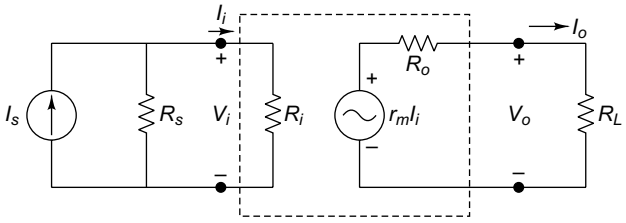


Fig. 2.8 ***Equivalent circuit of a transresistive amplifier***

The input current can be expressed as

$$I_i = I_s \frac{R_s}{R_s + R_i}$$

If $R_s >> R_i$, $I_i \approx I_s$

Hence source current is equal to input current as $R_s >> R_i$

The output voltage is

$$V_o = r_m I_i + I_o R_o = I_o R_L$$

If $R_L >> R_o$, $V_o = r_m I_i = I_o R_L$

or, $r_m I_s = I_o R_L$ as $I_i = I_s$

The transresistive amplifier gain is $r_m = \frac{V_o}{I_s}$

Therefore, output voltage V_o is directly proportional to the source current I_s and proportionality factor r_m and it is independent of R_s and R_L. This amplification is known as transresistive amplifier. This amplifier should have zero input resistance, $R_i = 0$ and zero output resistance, $R_o = 0$. Table 2.1 shows the ideal characteristics of amplifiers.

Table 2.1 *Amplifier characteristics*

Parameters	*Amplifier type*			
	Voltage Amplifier	*Current Amplifier*	*Transconductance Amplifier*	*Transresistive Amplifier*
Input resistance R_i	∞	0	∞	0
Output resistance R_o	0	∞	∞	0
Input quantity	V_s	I_s	V_s	I_s
Output quantity	V_o	I_o	I_o	V_o
Transfer characteristics	$A_v = \frac{V_o}{V_s}$	$A_I = \frac{I_o}{I_s}$	$g_m = \frac{I_o}{V_s}$	$r_m = \frac{V_o}{I_s}$

2.4 GENERALISED CONCEPT OF FEEDBACK AMPLIFIER

The schematic block diagram of a feedback amplifier is shown in Fig. 2.9. This block diagram consists of sampling network, mixer network, feedback network, main amplifier, source signal and load. The output signal (voltage or current) is sampled by a sampling network and fed to the feedback network. The output of feedback network is combined with the input signal in the mixer network to obtain the difference signal V_i. Then output of the mixer network is fed to the main amplifier (basic practical amplifier). In this section, operation of sampling network, mixer network, feedback network, and main amplifier are explained briefly.

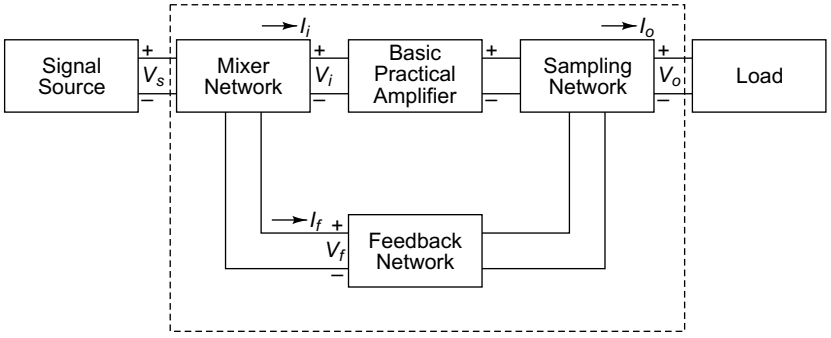


Fig. 2.9 ***Schematic diagram of a feedback amplifier***

Sampling Network Generally, two types of sampling networks such as voltage sampling and current sampling are used in a feedback system. In Fig. 2.10(a), the output voltage is sampled and in Fig. 2.10(b), the output current is sampled.

The voltage sampling is called *node sampling*, and the current sampling is known as *loop sampling*. Usually, the output voltage is sampled by connecting the feedback network in shunt across the output and the output current is sampled where feedback network is connected in series with the output as depicted in Fig. 2.10.

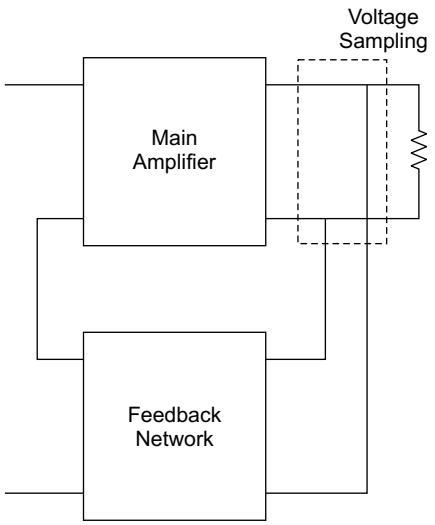


Fig. 2.10(a) *Voltage sampling*

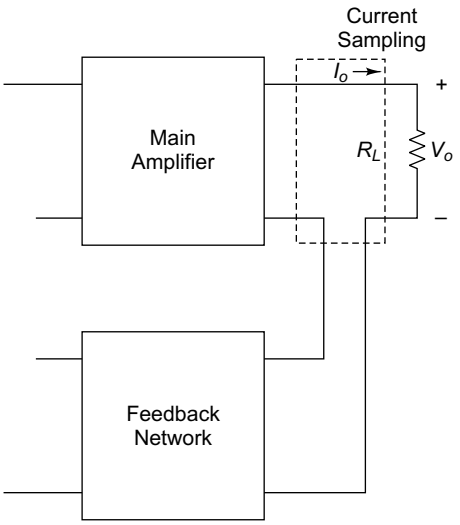


Fig. 2.10(b) *Current sampling*

Mixer network This circuit is also known as *comparator network*. There are two mixer networks such as series mixing and shunt mixing. Figure 2.11(a) shows the series mixing, and shunt mixing is depicted in Fig. 2.11(b). Sometimes, a differential amplifier is also used in mixer networks. The differential amplifier has two inputs and provides an output proportional to the difference between the two input signals.

Main amplifier The main amplifier is also known as *basic amplifier*. Usually, four types of amplifiers such as voltage amplifier, current amplifier, transconductance amplifier and transresistance amplifiers are used in the amplifier circuit.

Feedback network This network is a passive two-port network which consists of resistances, capacitances and inductances, and its input side is connected to the sampling network and output side is connected with the mixer network.

Signal source The input signal will be either a voltage source or a current source. The voltage source (a voltage signal V_s in series with a resistor R_s) is known as *Thevenin source*, and the current source (a current signal I_s in parallel with a resistor R_s) is called *Norton source*.

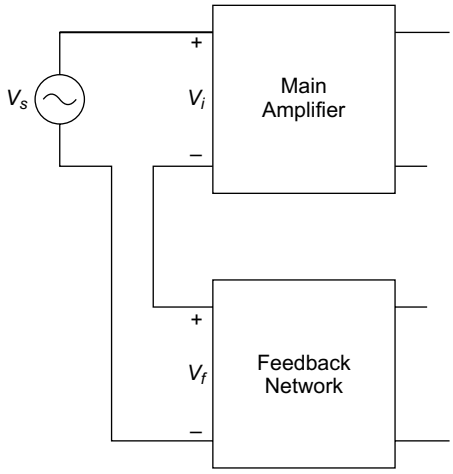


Fig. 2.11(a) *Series mixing*

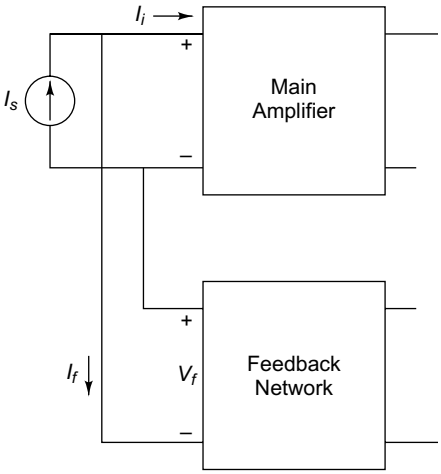


Fig. 2.11(b) *Shunt mixing*

2.5 TOPOLOGIES OF A FEEDBACK AMPLIFIER

In a feedback amplifier, the input and output variables can be modeled as either voltage or current. There are four combinations of inputs and outputs that represent the possible types of feedback amplifier. The four different types of feed back amplifiers are as follows:

(i) Series–Series feedback or Current–Series feedback

(ii) Series–Parallel feedback or Voltage–Series feedback

(iii) Parallel–Series feedback or Current–Shunt feedback

(iv) Parallel–Parallel feedback or Voltage–Shunt feedback

Table 2.2 shows the different types of feedback amplifiers with input variables, output variables, error signal, gain and feedback factor. The names of feedback amplifier come from the way that the feedback network is connected between input and output. The four different types of feedback amplifier circuits are shown in Fig. 2.12(a) to Fig. 2.12(d). In this section, all types of feedback amplifiers are explained in detail.

Table 2.2 *Types of feedback amplifiers*

Feedback amplifier	*Input variable*	*Output variable*	*Error signal*	*Forward gain*	*Feedback factor*
Series-Series	Voltage	Current	Voltage	Transconductance	Ohms
Series-Parallel	Voltage	Voltage	Voltage	Voltage gain	Dimensionless
Parallel-Series	Current	Current	Current	Current gain	Dimensionless
Parallel-Parallel	Current	Voltage	Current	Transresistance	Siemens

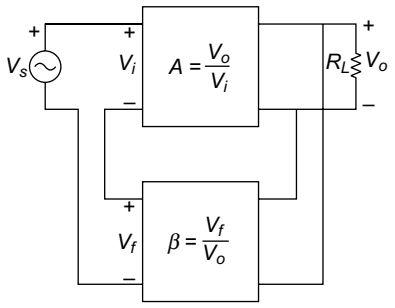


Fig. 2.12(a) *Voltage–Series feedback*

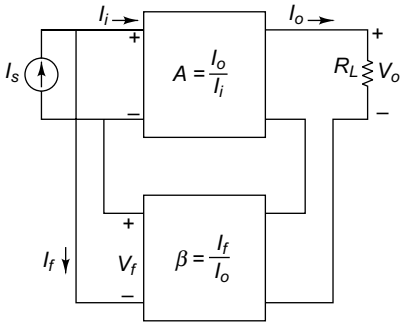


Fig. 2.12(b) *Current–Shunt feedback*

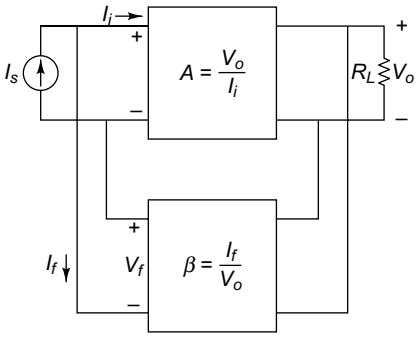


Fig. 2.12(c) *Voltage–Shunt feedback*

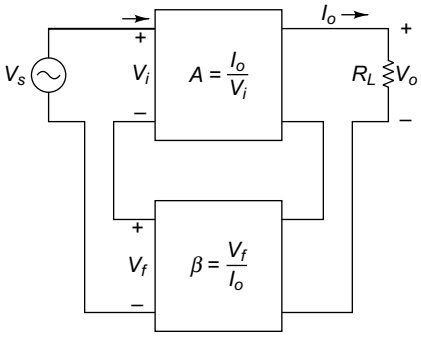


Fig. 2.12(d) *Current–Series feedback*

2.5.1 Voltage–Series Feedback Amplifier

Figure 2.13 shows the voltage series feedback amplifier. In this circuit, A is the gain of the main amplifier, β is the gain of the feedback amplifier, V_s is the supply voltage, and V_f is the feedback voltage, V_o is the output voltage.

The output voltage of the feedback amplifier is

$$V_f = \beta V_o \quad \text{as} \quad \beta = \frac{V_f}{V_o}.$$

The feedback amplifier output voltage V_f is connected in series but in opposition to the input voltage.

Therefore, input voltage of the main amplifier is

$$V_i = V_s - V_f = V_s - \beta V_o$$

The main amplifier gain is

$$A = \frac{V_o}{V_i}$$

Then output voltage is equal to

$$V_o = AV_i = A(V_s - \beta V_o)$$

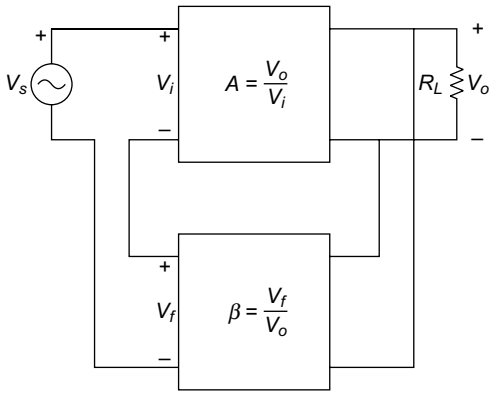


Fig. 2.13 *The voltage–series feedback amplifier*

The overall amplifier gain with feedback is

$$A_f = \frac{V_o}{V_s}$$

Then $V_o = A(V_s - \beta V_o)$
or, $V_o = AV_s - A\beta V_o$
or, $V_o + \beta V_o = AV_s$
or, $(1 + \beta A)V_o = AV_s$

The overall amplifier gain is expressed as $A_f = \frac{V_o}{V_s} = \frac{A}{1+\beta A}$

Hence, the negative feedback reduces the amplifier gain by a factor $(1 + \beta A)$.

2.5.2 Voltage–Shunt Feedback Amplifier

The block diagram of voltage–shunt feedback amplifier is shown in Fig. 2.14 where I_i is input current

I_f is feedback current

I_s is supply or source current

V_o is output voltage

In this circuit, the feedback signal is proportional to output voltage V_o and is fed in parallel to the input signal. The main amplifier is a transresistive amplifier, as output signal is voltage V_o and input signal is current I_i.

The gain of the main amplifier is

$A = \frac{V_o}{I_i}$ and units of A is ohms

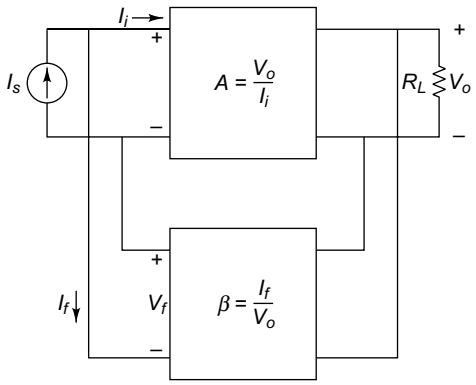


Fig. 2.14 ***The voltage–shunt feedback amplifier***

Output voltage is

$$V_o = AI_i$$

The gain of the feedback amplifier is

$$\beta = \frac{I_f}{V_o}$$

The feedback current is equal to

$$I_f = \beta V_o$$

The supply current is the sum of input current and feedback current.

Therefore, $I_s = I_i + I_f = I_i + \beta V_o$

The overall gain with feedback

$$A_f = \frac{V_o}{I_s} = \frac{V_o}{I_i + \beta V_o}$$

$$= \frac{AI_i}{I_i + \beta AI_o} = \frac{A}{1+\beta A}$$

Again we can say that the amplifier gain without feedback is reduced by a factor $(1 + \beta A)$ due to feedback.

2.5.3 Current–Shunt Feedback Amplifier

The block diagram of current shunt feedback is shown in Fig. 2.15. The feedback signal is proportional to the output current I_o and is fed in parallel with input. The main amplifier is a current amplifier.

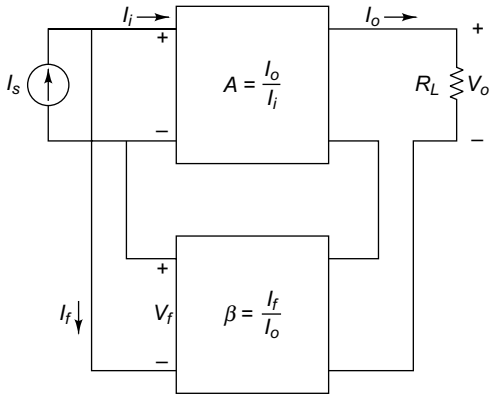


Fig. 2.15 *The current–shunt feedback amplifier*

The gain of the main amplifier is

$A = \frac{I_o}{I_i}$ and A is dimensionless

The output current is

$$I_o = AI_i$$

The gain of a feedback amplifier is

$$\beta = \frac{I_f}{I_o},$$

The feedback current is equal to $I_f = \beta I_o$

The source current is the sum of input current and feedback current.

Therefore, $I_s = I_i + I_f = I_i + \beta I_o$

The overall gain with feedback is

$$A_f = \frac{I_o}{I_s} = \frac{I_o}{I_i + I_f} = \frac{I_o}{I_i + \beta I_o}$$

$$= \frac{AI_i}{I_i + \beta AI_i} = \frac{A}{1+\beta A}$$

It is clear from the above expression that the amplifier gain is to reduced by a factor $(1 + \beta A)$ when negative current feedback is provided.

2.5.4 Current–Series Feedback Amplifier

Figure 2.16 shows the block diagram of a current–series feedback. In this case, the feedback signal is proportional to output current I_o which is fed back negatively to the input in series with the voltage source. The main amplifier is a transconductance amplifier as its output signal is current I_o and input signal is voltage V_i.

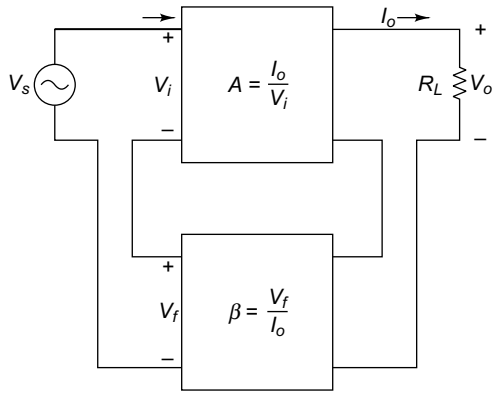


Fig. 2.16 ***The current–series feedback amplifier***

The gain of the main amplifier is

$$A = \frac{I_o}{V_i} \text{ and the units of } A \text{ is siemens}$$

The output current is

$$I_o = AV_i$$

The gain of the feedback amplifier is

$$\beta = \frac{V_f}{I_o}$$

The feedback voltage is equal to $V_f = \beta I_o$

The supply voltage is sum of input voltage and feedback voltage.

Therefore, $V_s = V_i + V_f$

$= V_i + \beta I_o$

$= V_i + \beta A V_i$

$= (1 + \beta A) V_i$

The overall gain with feedback is

$$A_f = \frac{I_o}{V_s} = \frac{I_o}{V_i + V_f}$$

$$= \frac{AV_i}{V_i + \beta AV_i} = \frac{A}{1 + \beta A}$$

Therefore, the amplifier gain is to reduce by a factor $(1 + \beta A)$ when feedback is provided.

2.6 EFFECT OF FEEDBACK ON IMPEDANCES

In this section, the effects of feedback on input and output impedances are explained for all four types of feedback amplifiers such as voltage–series, current–series, voltage–shunt and current–shunt feedback amplifiers.

2.6.1 Input Impedance

Effect of voltage–series feedback amplifier in input impedance In a voltage–series feedback amplifier, the main amplifier is modeled as a voltage–dependent voltage source as depicted in Fig. 2.17.

Input impedance of main amplifier is

$$Z_i = R_i$$

The input voltage is equal to

$$V_i = Z_i I_i = V_s - V_f$$

Assume R_o is negligible. Then output voltage is equal to $V_o = AV_i$

The feedback voltage is

$$V_f = \beta V_o$$

The source voltage is equal to

$$\begin{aligned} V_s &= V_i + V_f = Z_i I_i + \beta V_o \\ &= Z_i I_i + \beta A V_i \\ &= Z_i I_i + \beta A Z_i I_i \\ &= (1 + \beta A) Z_i I_i \end{aligned}$$

The input impedance of feedback amplifier is

$$Z_{if} = \frac{V_s}{I_i} = \frac{(1+\beta A) Z_i I_i}{I_i} = (1+\beta A) Z_i$$

Hence, the value of input impedance without feedback is multiplied by a factor $(1 + \beta A)$.

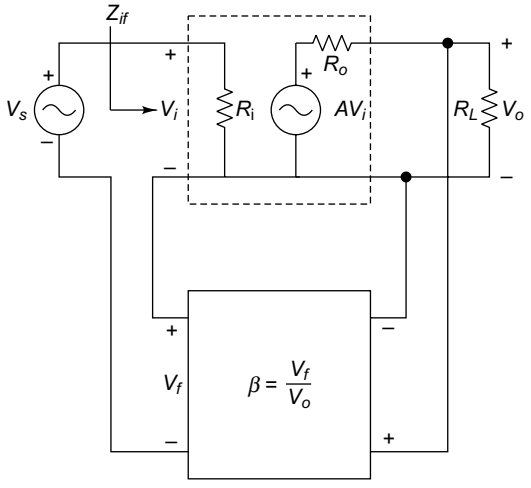


Fig. 2.17(a) ***Ideal structure of voltage–series feedback amplifier***

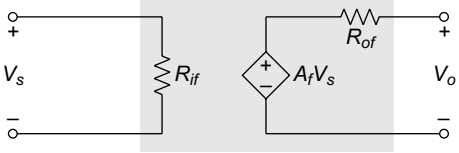


Fig. 2.17(b) ***Equivalent structure of voltage series feedback amplifier***

Effect of current–series feedback amplifier in input impedance Figure 2.18 shows the current–series feedback amplifier. In this circuit, the main amplifier is modeled as a voltage-dependent current source.

Input impedance of main amplifier is $Z_i = R_i$
The input voltage is equal to

$$V_i = Z_i I_i = V_s - V_f$$

Assume R_o is very high. Then output current is equal to $I_o = AV_i$
The feedback voltage is

$$V_f = \beta I_o$$

The source voltage is equal to

$$\begin{aligned} V_s &= V_i + V_f = Z_i I_i + \beta I_o \\ &= Z_i I_i + \beta A V_i \\ &= Z_i I_i + \beta A Z_i I_i \\ &= (1 + \beta A) Z_i I_i \end{aligned}$$

The input impedance of feedback amplifier is

$$Z_{if} = \frac{V_s}{I_i} = \frac{(1+\beta A) Z_i I_i}{I_i} = (1+\beta A) Z_i$$

Therefore, the value of input impedance without feedback is multiplied by a factor $(1 + \beta A)$.

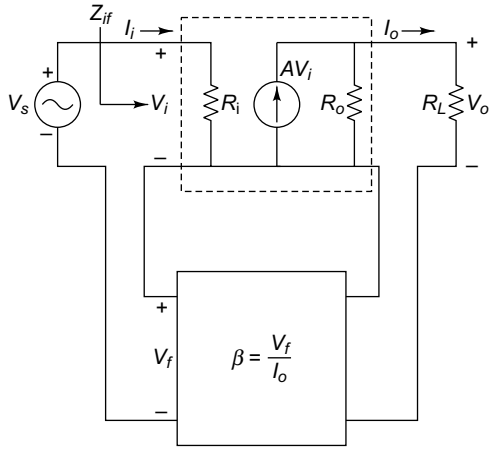


Fig. 2.18 ***Ideal structure of voltage–series feedback amplifier***

Effect of voltage–shunt feedback amplifier in input impedance Figure 2.19 shows a voltage shunt feedback connection where the main amplifier is modeled as current dependence voltage source.

The input impedance of main amplifier is $Z_i = R_i$
Input voltage is

$$V_i = Z_i I_i$$

Assume R_o is negligible. The output voltage is equal to $V_o = AI_i$

Feedback gain is

$$\beta = \frac{I_f}{V_o}$$

The feedback current is equal to $I_f = \beta V_o$
The source current is

$$I_s = I_i + I_f$$

The input impedance $Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f}$

$$= \frac{V_i}{I_i + \beta V_o} = \frac{V_i / I_i}{1 + \beta \frac{V_o}{I_i}}$$

$$= \frac{Z_i}{1 + \beta A}$$

Hence, input impedance is reduced by a factor $(1 + \beta A)$.

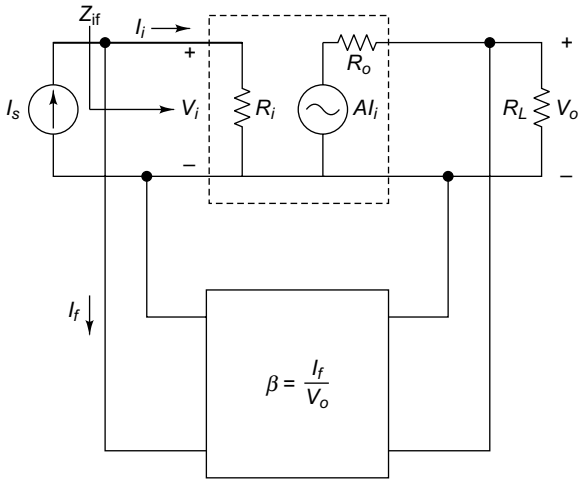


Fig. 2.19 *Ideal structure of voltage–shunt feedback amplifier*

Effect of current–shunt feedback amplifier in input impedance

Figure 2.20 shows a current shunt feedback connection where the main amplifier is modeled as current–dependence current source.

The input impedance of main amplifier $Z_i = R_i$
Input voltage is

$$V_i = Z_i I_i$$

Assume R_o is very high. The output current is equal to $I_o = AI_i$
Feedback gain is

$$\beta = \frac{I_f}{I_o}$$

The feedback current is equal to $I_f = \beta I_o$

The source current is $I_s = I_i + I_f$

The input impedance $Z_{if} = \dfrac{V_i}{I_s} = \dfrac{V_i}{I_i + I_f}$

$$= \frac{V_i}{I_i + \beta I_o} = \frac{V_i}{I_i + \beta A I_i}$$

$$= \frac{Z_i I_i}{I_i + \beta A I_i} = \frac{Z_i I_i}{(1+\beta A) I_i}$$

$$= \frac{Z_i}{1+\beta A}$$

Hence, input impedance is reduced by a factor $(1 + \beta A)$.

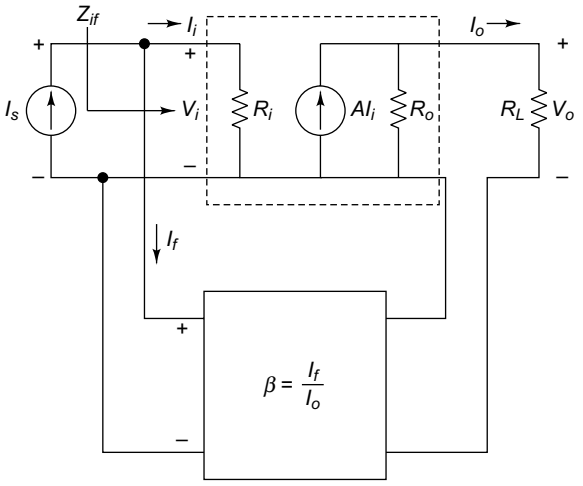


Fig. 2.20 *Ideal structure of current–shunt feedback amplifier*

2.6.2 Output Impedance

Effect of voltage series feedback amplifier in output Impedance The output impedance can be obtained when a voltage V is applied at output terminals and V_s is shorted. Refer the ideal structure of voltage series feedback amplifier as shown in Fig. 2.17 and V_s is shorted and a voltage V is applied at output terminals. Figure 2.21 shows the equivalent circuit to determine the

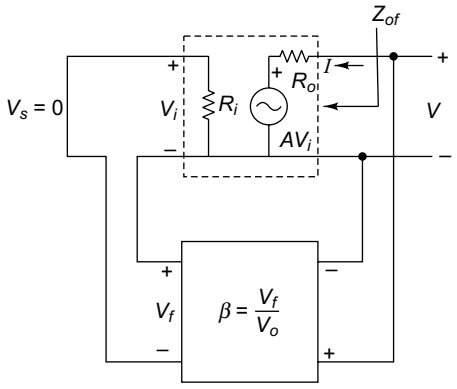


Fig. 2.21 ***Voltage series feedback amplifier when $V_s = 0$ and R_L is disconnected***

output impedance of a voltage–series feedback amplifier where $V_s = 0$ and load resistance is disconnected.

Assume I current flows through the circuit.
The voltage is

$$V = IZ_o + AV_i \text{ where } Z_o = R_o$$

The input voltage is equal to feedback voltage but polarity is reversed.
Therefore, $V_i = -V_f$

Then voltage $V = IZ_o - AV_f = IZ_o - A\beta V$ As $V_f = \beta V_o$
Hence, $IZ_o = V + \beta AV$

$$= (1 + \beta A)V$$

The output impedance is equal to

$$Z_{of} = \frac{V}{I} = \frac{Z_o}{1 + \beta A}$$

Hence, in voltage series feedback, the output impedance is reduced from the without feedback by the factor $(1 + \beta A)$.

In the same way, the output impedance of voltage shunt feedback amplifier can also be computed and output impedance can be expressed as $Z_{of} = \frac{Z_o}{1 + \beta A}$.

Effect of current–series feedback amplifier in output impedance

Figure. 2.18 shows the current–series feedback amplifier circuit. In this case, the main amplifier is represented by current model. To calculate the output impedance, voltage V is applied at output terminals with V_s is shorted. Figure 2.22 shows the equivalent circuit to determine the output impedance of a current–series feedback amplifier where $V_s = 0$ and load resistance is disconnected.

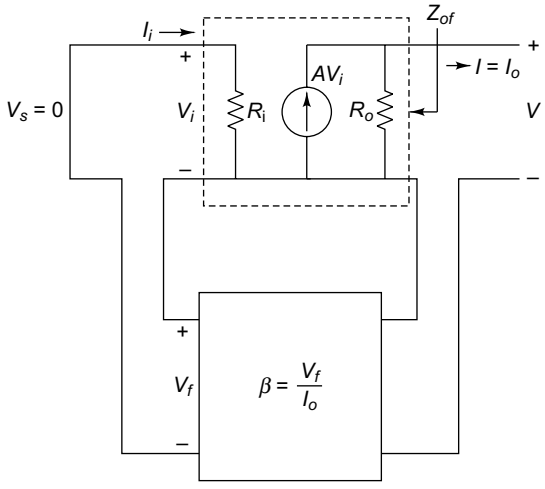


Fig. 2.22 ***Current–series feedback amplifier when $V_s = 0$ and R_L is disconnected***

Assume current I flows through the circuit.
As $V_s = 0$, $V_i = -V_f$

The output current is

$$I = \frac{V}{Z_o} + AV_i$$

$$= \frac{V}{Z_o} - AV_f \qquad \text{as} \quad V_i = -V_f$$

$$= \frac{V}{Z_o} - A\beta I \qquad \text{as} \quad V_f = \beta I$$

Then we can write $(1 + A\beta) I = \frac{V}{Z_o}$

or, $(1 + A\beta) IZ_o = V$

The output impedance is equal to

$$Z_{of} = \frac{V}{I} = Z_o (1 + \beta A)$$

In the same way, the output impedance of current–shunt feedback amplifier can be computed and output impedance can be expressed as $Z_{of} = Z_o (1 + \beta A)$.

Table 2.3 shows the summary of input and output impedances of voltage–series, current–series, voltage–shunt and current–shunt feedback amplifiers.

Table 2.3 *Input and output impedances of feedback amplifiers*

Impedance	*Types of feedback amplifier*			
	Voltage series	*Current series*	*Voltage shunt*	*Current shunt*
Input Impedance Z_{if}	Increased $Z_i (1 + \beta A)$	Increased $Z_i (1 + \beta A)$	Decreased $\frac{Z_i}{1 + \beta A}$	Dcreased $\frac{Z_i}{1 + \beta A}$
Output Impedance Z_{of}	Decreased $\frac{Z_o}{1 + \beta A}$	Increased $Z_o (1 + \beta A)$	Decreased $\frac{Z_o}{1 + \beta A}$	Increased $Z_o (1 + \beta A)$

2.5 In a voltage–series feedback amplifier A = 400, R_i = 2 kΩ, R_o = 100 kΩ and β = 0.1. Determine overall gain, input impedance, and output impedance of the feedback amplifier.

Solution

Assume $A = 400$, $R_i = 2$ kΩ, $R_o = 100$ kΩ and $\beta = 0.1$

In voltage–series feedback amplifier,

Overall gain is $A_f = \frac{A}{1 + \beta A}$

$$= \frac{400}{1 + 0.1 \times 400} = 9.756$$

Input impedance is $Z_{if} = Z_i (1 + \beta A)$

$$= R_i (1 + \beta A) = 2 \times 10^3 (1 + 0.1 \times 400) = 82 \text{ k}\Omega$$

Output impedance is $Z_{of} = \dfrac{Z_o}{1+\beta A}$

$$= \frac{R_o}{1+\beta A} = \frac{100\times10^3}{(1+0.1\times400)} = 2.439\ \text{k}\Omega$$

2.6 Calculate the overall loop gain, input and output impedances for an amplifier in a current series feedback amplifier with $A = 100$, $R_i = 1$ kΩ, $R_o = 50$ kΩ and $\beta = 0.025$.

Solution

Given $A = 100$, $R_i = 1$ kΩ, $R_o = 50$ kΩ and $\beta = 0.025$

In current series feedback amplifier,

Over all gain is $A_f = \dfrac{A}{1+\beta A} = \dfrac{100}{1+0.025\times100} = 28.571$

Input impedance is $Z_{if} = Z_i(1 + \beta A)$, assume $Z_i = R_i$

$= R_i(1+\beta A) = 1\times10^3(1+0.025\times100) = 3.5\ \text{k}\Omega$

Output impedance is $Z_{of} = Z_o(1+\beta A)$ assume $Z_o = R_o$

$= R_o(1+\beta A) = 50\times10^3(1+0.025\times100) = 175\ \text{k}\Omega$

2.7 A voltage–series feedback amplifier has $A = -100$, $R_i = 25$ kΩ, $R_o = 100$ kΩ and feedback factor $\beta = -0.1$.

(a) Determine overall gain, input impedance, and output impedance of the feedback amplifier.

(b) If the gain has been reduced to –2.5, what will be the feedback factor?

Solution

Given $A = -100$, $R_i = 25$ kΩ, $R_o = 10$ kΩ and $\beta = -0.1$

(a) In a voltage–series feedback amplifier,

Overall gain is

$$A_f = \frac{A}{1+\beta A} = \frac{-100}{1+(-0.1)\times(-100)} = 9.0909$$

Input impedance is

$Z_{if} = Z_i(1 + \beta A)$ as $Z_i = R_i$

$= R_i(1+\beta A) = 25\times10^3(1+(-0.1)\times(-100)) = 275\ \text{k}\Omega$

Output impedance is

$$Z_{of} = \frac{Z_o}{1+\beta A} \quad \text{as} \quad Z_o = R_i$$

$$= \frac{R_o}{1+\beta A} = \frac{-10\ \text{k}\Omega}{(1+(-0.1)\times(-100))} = 909.09\ \text{k}\Omega$$

(b) When the gain has been reduced to –2.5, the feedback factor will be computed from

$$A_f' = \frac{A}{1+\beta A} \quad \text{as} \quad A_f' = -2.5$$

$$= \frac{-100}{1+\beta\times(-100)} = -2.5$$

Then the feedback factor is $\beta = -0.39$

2.8 A feedback amplifier circuit is shown in Fig. 2.23 with the gain of amplifier A = $100 \angle 180°$, $R_1 = 10$ kΩ and $R_2 = 150$ kΩ.

Calculate output voltage and source voltage when input voltage of amplifier is $1\angle 0°$.

Solution

The above circuit configuration is voltage–series feedback.

The feedback voltage is

$$V_f = \frac{R_2}{R_1 + R_2} V_o = \frac{150}{150 + 10} V_o$$

$$= \frac{150}{160} V_o = \beta V_o$$

So, feedback path gain is $\beta = \frac{150}{160}$

The overall gain is $A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}$

$$= \frac{100\angle 180°}{1 + \frac{150}{160} \times 100\angle 180°}$$

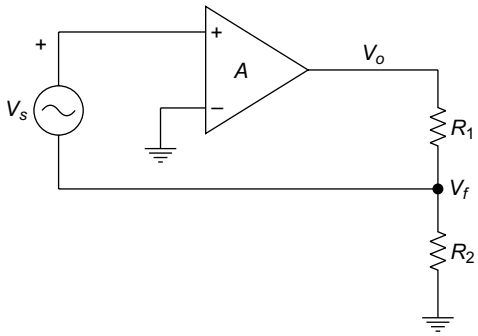


Fig. 2.23 *Circuit of Ex. 2.8*

$$= \frac{-100}{1 + \frac{150}{160} \times (-100)} = 1.078$$

Hence, $V_o = 1.078\ V_s$

The input voltage of main amplifier is

$$V_i = V_s - V_f = V_s - \beta V_o$$

$$= V_s - \frac{150}{160} \times 1.078 V_s = 0.010625\ V_s$$

As $V_i = 1\angle 0°$, the source voltage is equal to

$$V_s = -\frac{1\angle 0°}{0.010625} = -94.11\angle 0°$$

The output voltage is equal to $V_o = 1.078\ V_s$

Then output voltage $V_o = 1.078\ V_s = 1.078 \times (-94.11\angle 0°) = -101.45\ \angle 0°$

2.9 An amplifier has an open-loop gain of 200, an input impedance of 1 kΩ and an output impedance of 100 Ω. A feedback network with a feedback factor of 0.5 is connected in a voltage–series feedback mode. Determine the new input and output impedances.

Solution

Assume, input impedance $Z_i = 1$ kΩ, output impedance $Z_o = 100$ Ω, open–loop gain $A = 200$ and feedback factor $\beta = 0.5$.

After feedback, new input impedance is $Z_{if} = Z_i (1 + \beta A)$

$= 1$ kΩ $(1 + 0.5 \times 200) = 101$ kΩ

and new output impedance is $Z_{of} = \frac{Z_o}{1 + \beta A}$

$$= \frac{100}{1 + 0.5 \times 200} = 0.99\ \Omega$$

2.10 Determine overall gain, input impedance, and output impedance of a voltage shunt feedback amplifier. Assume the following parameters of feedback amplifier.

Open–loop gain $A = -1000$, input resistance $R_i = 10\ \text{k}\Omega$, output resistance $R_o = 20\ \text{k}\Omega$ and $\beta = -0.1$,

Solution

Given $A = -1000$, $R_i = 10\ \text{k}\Omega$, $R_o = 20\ \text{k}\Omega$ and $\beta = -0.1$

In voltage shunt feedback amplifier,

Over all gain is $A_f = \dfrac{A}{1 + \beta A}$

$$= \frac{-1000}{1 + (-0.1) \times -1000} = -9.90$$

Input impedance is

$$Z_{if} = \frac{Z_i}{1 + \beta A}$$

$$= \frac{R_i}{1 + \beta A} = \frac{10\,k\Omega}{1 + (-0.1)(-1000)} = 99\ \Omega$$

Output impedance is $Z_{of} = \dfrac{Z_o}{1 + \beta A}$

$$= \frac{R_o}{1 + \beta A} = \frac{20 \times 10^3}{\left(1 + (-0.1) \times (-1000)\right)} = 198\ \Omega$$

2.11 Compute input and output impedances for an amplifier in a current shunt feedback configuration with $A = 500$, $R_i = 1000\ \Omega$, $R_o = 5000\ \Omega$ and $\beta = 0.075$.

Solution

Given $A = 500$, $R_i = 1000\ \Omega$, $R_o = 5000\ \Omega$ and $\beta = 0.075$

In current–shunt feedback amplifier,

Input impedance is

$$Z_{if} = \frac{Z_i}{1 + \beta A}, \text{ assume } Z_i = R_i$$

$$= \frac{R_i}{1 + \beta A} = \frac{1000\ \Omega}{1 + (0.075 \times 500)} = 25.97\ \Omega$$

Output impedance is $Z_{of} = Z_o\ (1 + \beta A)$, assume $Z_o = R_o$

$$= R_o\left(1 + \beta A\right) = 5000\left(1 + 0.075 \times 500\right) = 192.5\ \text{k}\Omega$$

2.7 PROPERTIES OF FEEDBACK AMPLIFIERS

The properties of feedback amplifiers are

- Reduction in frequency distortion
- Reduction in noise and nonlinear distortion
- Effect of negative feedback on gain and bandwidth
- Gain stability with feedback
- Reduction in phase distortion

2.7.1 Reduction in Frequency Distortion

In a negative feedback amplifier with feedback gain β, the overall loop gain of the amplifier is reduced by a factor $(1 + \beta A)$. If we assume $\beta A >> 1$, the gain with feedback is $A_f \cong \frac{1}{\beta}$. It follows that the feedback network is purely resistive and the gain with feedback does not dependent on frequency even though the main amplifier gain is frequency dependent. Therefore, the frequency distortion arising because of varying amplifier gain with frequency is considerably reduced in a negative voltage feedback amplifier circuit.

2.7.2 Reduction in Noise and Nonlinear Distortion

Feedback signal tends to hold down the amount of noise signal and nonlinear distortion at the output stage. Figure 2.24 shows the block diagram representation of negative feedback amplifier with noise signal V_N.

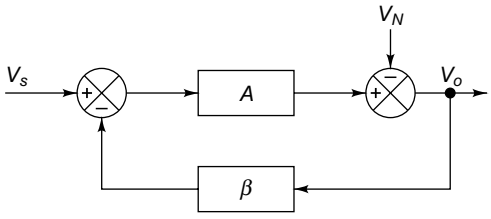


Fig. 2.24 ***Feedback amplifier with noise signal***

When the noise signal V_N is present, the output voltage will be function of input signal V_S, open loop gain A, gain of feedback path β and noise signal V_N. The output voltage can be expressed as

$$V_o = \frac{A}{1+\beta A} V_s + \frac{1}{1+\beta A} V_N$$

It is clear from the above expression that there is a reduction in overall gain, but noise is reduced by the factor $(1 + \beta A)$. Hence nonlinear distortion is considerably improved.

An additional preamplifier of gain $(1 + \beta A)$ is used to bring the overall gain up to the level without feedback as depicted in Fig. 2.25.

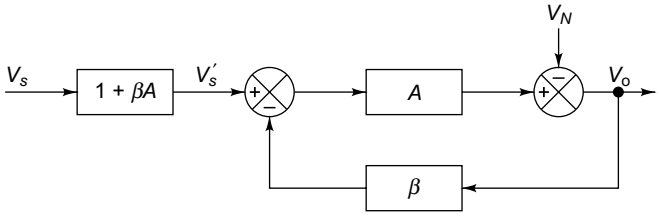


Fig. 2.25 ***Feedback amplifier with noise signal and a preamplifier***

The output voltage can be expressed as

$$V_o = \frac{A}{1+\beta A} V_s' + \frac{1}{1+\beta A} V_N$$

As $V_s = (1+\beta A) V_s'$, output voltage is $V_o = AV_s + \frac{1}{1+\beta A} V_N$

The above equation states that the input signal V_s is amplified by A and the noise signal in the output is reduced by $(1 + \beta A)$.

Sometimes the extra stages might introduce as much noise back into the system as that reduced by the feedback amplifier. This problem can be solved in some extent by readjusting the gain of the feedback amplifier circuit to obtain higher gain while also providing reduced noise signal.

2.7.3 Effect of Negative Feedback on Gain and Bandwidth

In a negative feedback amplifier, the overall loop gain can be expressed as

$$A_f = \frac{A}{1+\beta.A} \cong \frac{A}{\beta A} = \frac{1}{\beta} \qquad \text{as} \quad \beta A >> 1$$

As long as $\beta A >> 1$, the overall loop gain is $A_f = \frac{1}{\beta}$

Figure 2.26 shows the effect of negative feedback on gain and bandwidth.
The low-frequency gain of amplifier is A_l and it can be expressed as

$$A_l = \frac{A_o}{1 - j\left(\frac{f_1}{f}\right)}$$

where, A_o is the mid frequency gain and f_1 is the lower half power frequency.
The high-frequency gain of amplifier is A_l and it can be expressed as

$$A_h = \frac{A_o}{1 + j\left(\frac{f}{f_2}\right)}$$

where, f_2 is the upper half power frequency

With feedback, the overall gain at low frequency is $A_{lf} = \frac{A_l}{1+\beta A_l}$ and

With feedback, the overall gain at high frequency is $A_{hf} = \frac{A_h}{1+\beta A_h}$

After substituting the value of $A_l = \frac{A_o}{1 - j\left(\frac{f_1}{f}\right)}$ in equation $A_{lf} = \frac{A_l}{1+\beta A_l}$, we get

$$A_{lf} = \frac{A_o}{1 + \beta A_o - j\left(\frac{f_1}{f}\right)} = \frac{A_{fo}}{1 - j\left(\frac{f_{1f}}{f}\right)}$$

where, A_{fo} is the mid-frequency gain with negative feedback and $A_{fo} = \frac{A_o}{1 + \beta A_o}$

f_{1f} is known as lower half power frequency with negative feedback and

$f_{1f} = \frac{f_1}{1 + \beta A_o}$

After substituting the value of $A_h = \frac{A_o}{1 + j\left(\frac{f}{f_2}\right)}$ in equation $A_{hf} = \frac{A_h}{1 + \beta A_h}$, we obtain

$$A_{hf} = \frac{A_{fo}}{1 + j\left(\frac{f}{f_{2f}}\right)}$$

where, f_{2f} is known as upper-half power frequency with negative feedback and $f_{2f} = f_2(1 + \beta A_o)$.

In an amplifier without feedback, bandwidth is equal to the difference between f_2 and f_1

$$BW = f_2 - f_1$$

When feedback is used, there is some reduction in gain in low-frequency and high-frequency region. The feedback amplifier has a higher upper 3-dB frequency and smaller 3-dB frequency.

The bandwidth with feedback is $BW_f = f_{2f} - f_{1f}$
where upper cut-off frequency $f_{2f} = f_2(1 + \beta A_o)$

lower cut-off frequency $f_{1f} = \frac{f_1}{1 + \beta A_o}$

Therefore, an amplifier with negative feedback has larger bandwidth with respect to a bandwidth without feedback.

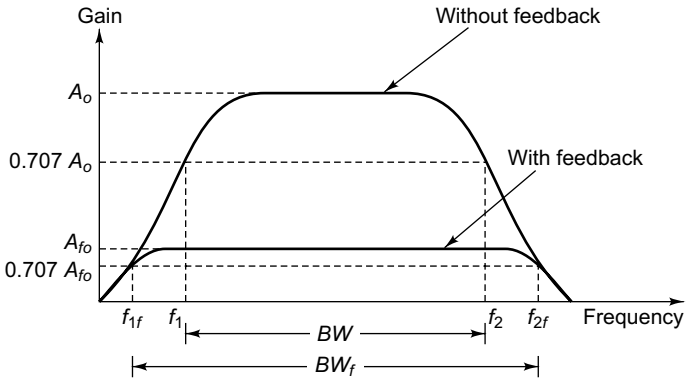


Fig. 2.26 *Effect of negative feedback on gain and bandwidth*

2.7.4 Gain Stability and Sensitivity with Feedback

The overall loop gain of a feedback amplifier is $A_f = \dfrac{A}{1+\beta.A}$

Differentiation of the above equation is

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1+\beta A|}\left|\frac{dA}{A}\right|$$

or, $$\left|\frac{dA_f}{A_f}\right| = \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \quad \text{for} \quad \beta A >> 1$$

This shows that the magnitude of relative change in overall gain $\left|\dfrac{dA_f}{A_f}\right|$ is reduced by the factor $|\beta A|$ compared to relative change $\left|\dfrac{dA}{A}\right|$ in basic amplifier gain.

The fractional change in amplification with feedback divided by the fractional change without feedback is called sensitivity of the transfer gain. The sensitivity S can be expressed as

Sensitivity $S = \dfrac{dA_f / A_f}{dA / A} = \dfrac{1}{1+\beta A} = \dfrac{1}{\beta A}$ for $\beta A >> 1$.

The desensitivity D is equal to $\dfrac{1}{\text{Sensitivity}} = \dfrac{1}{S}$.

Therefore $D = \dfrac{1}{S} = 1+\beta A$ and $\left|\dfrac{dA_f}{A_f}\right| = \dfrac{1}{|1+\beta A|}\left|\dfrac{dA}{A}\right| = \dfrac{1}{|D|}\left|\dfrac{dA}{A}\right|$

Since $|D|$ is greater than 1 for negative feedback amplifier, the percentage change in amplification with feedback is less than the percentage change in A. Therefore,

$$\left|\frac{dA_f}{A_f}\right| < \left|\frac{dA}{A}\right|$$

2.7.5 Phase Distortion with Feedback

The gain of amplifier is complex quantity and it has a magnitude and a phase angle. As a result, the gain A of the amplifier without feedback can be expressed as

$$A = |A| \angle\theta$$

With feedback the gain of amplifier is $A_f = \dfrac{A}{1+\beta.A}$.

The gain of feedback path β is either a real or a complex quantity. To simplify the mathematical analysis, we assume β is a real number.

After substituting the value of $A = |A| \angle\theta$ in overall gain, we get

$$A_f = \frac{A}{1+\beta.A} = \frac{|A|\angle\theta}{1+\beta|A|\angle\theta}$$

$$= \frac{|A|\angle\theta}{1+\beta|A|(\cos\theta + j\sin\theta)}$$

$$= \frac{|A|\angle\theta}{(1+\beta|A|\cos\theta) + j\beta|A|\sin\theta}$$

$$= \frac{A\angle\theta}{B\angle\phi}$$

where $|B| = \sqrt{(1+\beta|A|\cos\theta)^2 + (\beta|A|\sin\theta)^2}$ and

$$\phi = \tan^{-1}\left(\frac{\beta|A|\sin\theta}{1+\beta|A|\cos\theta}\right)$$

$$A_f = \frac{|A|}{|B|}\angle\theta - \phi = |A_f|\angle\psi$$

where $|A_f| = \frac{|A|}{|B|}$ and $\angle\psi = \angle\theta - \phi$

It is clear from $A_f = \frac{|A|}{|B|}\angle\theta - \phi = |A_f|\angle\psi$, the phase angle of the overall gain decreases by ϕ in negative feedback amplifier. Therefore, the phase distortion is reduced.

2.12 An operational amplifier has an open-loop gain of 10^6 and open-loop upper cut-off frequency of 10 Hz. If this operational amplifier is connected as an amplifier with a closed-loop gain of 100, what will be the new upper cut-off frequency?

Solution

The closed-loop gain is $A_f = \frac{A}{1+\beta.A}$

Here, $A = 10^6$ and $A_f = 100$ and open-loop upper cut-off frequency $f_2 = 10$ Hz

$$(1 + \beta A) = \frac{A}{A_f} = \frac{10^6}{100} = 10^4$$

The upper cut-off frequency $f_{2f} = f_2(1 + \beta A_o) = 10 \times 10^4 = 100$ kHz

2.13 An amplifier circuit has a gain of –100 and feedback path gain is $\beta = -0.01$. When the amplifier gain is changed by 25% due to temperature, determine the change in gain of feedback amplifier.

Solution

Given $A = -100$, $\beta = -0.01$ and $\left|\frac{dA}{A}\right| = 25\% = 0.25$

The change in gain of feedback amplifier

$$\left|\frac{dA_f}{A_f}\right| = \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| = \frac{1}{(-0.01)\times(-100)} \times 0.25 = 0.25 = 25\%$$

2.14 A amplifier circuit has a gain of –100 and feedback ratio is $\beta = -0.05$.
Determine (a) the amplifier gain with feedback
(b) the amount of feedback in dB
(c) the feedback factor
(d) feedback voltage
Assume input voltage $V_s = 50$ mV

Solution

Given $A = -100$, $\beta = -0.05$

(a) The amplifier gain with feedback is $A_f = \frac{A}{1+\beta.A} = \frac{-100}{1+(-0.05)(-100)} = -16.67$

(b) The amount of feedback in dB $= 20\log_{10}\left|\frac{A_f}{A}\right| = 20\log_{10}\left|\frac{-16.67}{-100}\right| = -15.56$ dB

(c) The feedback factor is $\beta = -0.05$

(d) The feedback voltage is

$$V_f = \beta V_o \quad \text{as } V_o = A_f V_s$$
$$= \beta A_f V_s = (-0.05) \times (-16.67) \times 50 \text{ mV} = 41.675 \text{ mV}$$

2.8 METHOD OF ANALYSIS OF A FEEDBACK AMPLIFIER

The complete analysis of a feedback amplifier is done by the following steps given below:

Step 1: Identify the topology of a feedback amplifier

(i) Find the sampled signal—it is either voltage or current. This can be understood by whether the sampled signal is taken from the output voltage node or from the output current loop.
(ii) Find the feedback signal—it is either voltage or current. If the feedback signal is voltage, it is mixed with external input signal in shunt connection. When the feedback signal is current, it is mixed with external input signal in series connection.

Depending upon the sampled signal as well as feedback signal, there are four different topologies of feedback amplifiers as given in Table 2.4.

Table 2.4 *Feedback amplifier*

Topology	*Sampled signal*	*Feedback signal*
Voltage series	Voltage	series
Voltage shunt	Voltage	shunt
Current series	Current	series
Current shunt	Current	shunt

Step 2: Draw the basic amplifier circuit without feedback by using the following method

(i) *For the input circuit, modify the output side as follows:*
- In case of voltage–series or voltage–shunt topology, short the output node to ground.
- In case of current–series or current–shunt topology, open the output loop.

(ii) *For the output circuit, modify the input side as follows:*
- In case of voltage–shunt or current–shunt topology, short the input node.
- In case of voltage–series or current–series topology, open the input loop.

Step 3: Input signal source must be converted into following ways

(i) Use Thevenin's source for voltage–series or current–series topology.
(ii) Use Norton source voltage–shunt or current–shunt topology.

Step 4: Mention the output signal (V_o or I_o) on the circuit.
Mention the feedback signal (V_f or I_f) on the circuit.

Step 5: Determine the gain of feedback path $\beta = \dfrac{\text{feedback signal}}{\text{output signal}}$

Step 6: Draw the equivalent circuit of the main amplifier by replacing each active device by its proper *h*-parameter model. From the equivalent circuit, determine A_V for voltage amplifier, A_I for current amplifier, g_m for transconductance amplifier or r_m for transresistance amplifier.

Step 7: Determine overall loop gain, $A_f = \dfrac{A}{1+\beta A}$

Step 8: In the same way, determine input impedance, R_{if} and output impedance, R_{of}.

2.9 PRACTICAL FEEDBACK CIRCUITS

This section provides some examples of practical feedback circuits to demonstrate the effect of feedback.

2.9.1 FET Amplifier with Voltage Series Feedback

Figure 2.27 shows an FET amplifier circuit with voltage–series feedback. A part of

output voltage can be feedback using a voltage divider circuit which consists of resistors R_1 and R_2. The feedback voltage is connected in series with source signal V_S. The mid-frequency small signal model of Fig. 2.27 is depicted in Fig. 2.28.

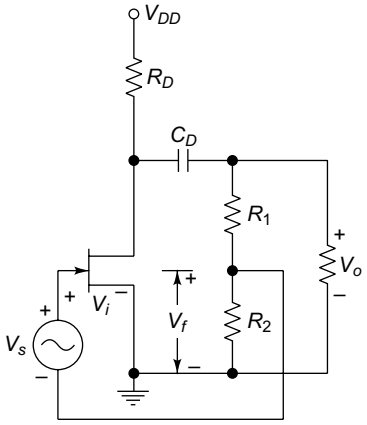


Fig. 2.27 *FET amplifier*

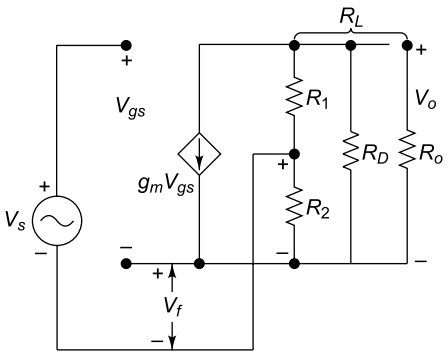


Fig. 2.28 *Equivalent circuit of FET amplifier*

Amplifier gain is $A = \dfrac{V_o}{V_i} = -g_m R_L$ where, R_L is parallel combination of resistances, R_o, R_D and R_1 and R_2.

R_L can be expressed as $R_L = R_D \parallel (R_1 + R_2) \parallel R_o$

Feedback factor $\beta = \dfrac{V_f}{V_o} = -\dfrac{R_2}{R_1 + R_2}$

Figure 2.29 shows the block-diagram representation of feedback amplifier. The gain of negative feedback amplifier is

$$A_f = \frac{A}{1 + \beta . A} = \frac{-g_m R_L}{1 + \left(-\dfrac{R_2}{R_1 + R_2}\right)(-g_m R_L)}$$

$$= \frac{-g_m R_L}{1 + g_m \left(\dfrac{R_2 R_L}{R_1 + R_2}\right)}$$

For $\beta A >> 1$, $A_f = \dfrac{1}{\beta} = \dfrac{-g_m R_L}{g_m \left(\dfrac{R_2 R_L}{R_1 + R_2}\right)} = -\dfrac{R_1 + R_2}{R_2}$

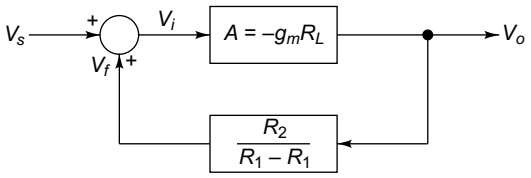


Fig. 2.29 *Block-diagram representation of feedback amplifier*

2.15 Determine the overall loop gain of FET amplifier circuit as depicted in Fig. 2.27 with the following parameters $g_m = 1000$ µs, $R_1 = 20$ kΩ, $R_2 = 10$ kΩ, $R_o = 15$ kΩ and $R_D = 10$ kΩ.

Solution

Given $g_m = 1000$ µs, $R_1 = 20$ kΩ, $R_2 = 10$ kΩ, $R_o = 15$ kΩ and $R_D = 10$ kΩ.

$$R_L = R_D \parallel (R_1 + R_2) \parallel R_o$$

or, $$\frac{1}{R_L} = \frac{1}{R_D} + \frac{1}{R_1 + R_2} + \frac{1}{R_o} = \frac{1}{10} + \frac{1}{30} + \frac{1}{15}$$

or, $$R_L = 5 \text{ k}\Omega$$

Amplifier gain is $A = \frac{V_o}{V_i} = -g_m R_L = -1000 \times 10^{-6} \times 5 \times 10^3 = -5$

Feedback factor is $\beta = \frac{V_f}{V_o} = -\frac{R_2}{R_1 + R_2} = -\frac{10}{20 + 10} = -\frac{1}{3}$

Overall loop gain is $A_f = \frac{A}{1 + \beta . A} = \frac{-5}{1 + \left(-\frac{1}{3}\right) \times (-5)} = -1.87$

2.9.2 BJT Emitter Follower Circuit

Figure 2.30 shows the emitter follower circuit with voltage–series feedback. In this circuit V_s is supply voltage, V_i is input voltage, V_o is output voltage and V_f is feedback voltage.

The output voltage is $V_o = V_f$

In this circuit, feedback voltage is in series with the input voltage.

The mid-frequency small signal model of Fig. 2.30 is depicted in Fig. 2.31.

Amplifier gain is $A = \frac{V_o}{V_s} = \frac{(1 + \beta)}{r_\pi} R_E = \frac{\beta}{r_\pi} R_E$ as $\beta >> 1$

Feedback factor is $B = \frac{V_f}{V_o} = 1$

The block diagram representation of Fig. 2.30 is depicted in Fig. 2.32.

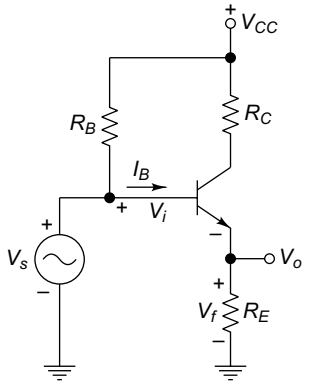


Fig. 2.30 *BJT amplifier with voltage–series feedback*

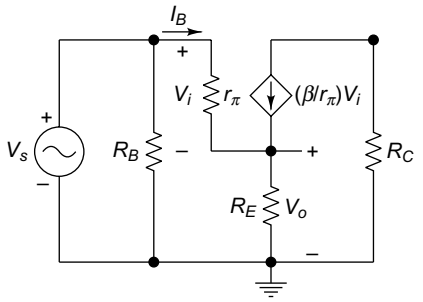


Fig. 2.31 *Equivalent circuit of BJT amplifier*

The overall loop gain is

$$A_f = \frac{A}{1 + B.A}$$

$$= \frac{\beta R_E}{r_\pi + \beta R_E} \approx 1 \qquad \text{as } \beta R_E >> r_\pi$$

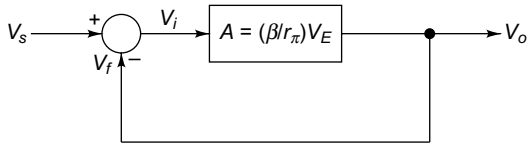


Fig. 2.32 *Block-diagram representation of feedback amplifier*

2.9.3 Emitter Current Feedback Amplifier

The emitter current feedback amplifier is shown in Fig. 2.33 and its small-signal model is depicted in Fig. 2.34. It is clear from Fig. 2.33 that the feedback voltage is proportional to the emitter current which is being fed negatively. The R_B resistance across base and V_{CC} does not affect voltage gain of the amplifier. The block-diagram representation of BJT amplifier with current series feedback is illustrated in Fig. 2.35.

The gain $A = -\dfrac{\beta}{r_\pi}$ and the feedback voltage $V_f = -I_o R_E$
As $V_f = BI_o$, $B = -R_E$
Amplifier gain is

$$A_f = \frac{I_o}{V_s} = \frac{A}{(1 + BA)} = \frac{-\dfrac{\beta}{r_\pi}}{1 + (-R_E)\left(-\dfrac{\beta}{r_\pi}\right)}$$

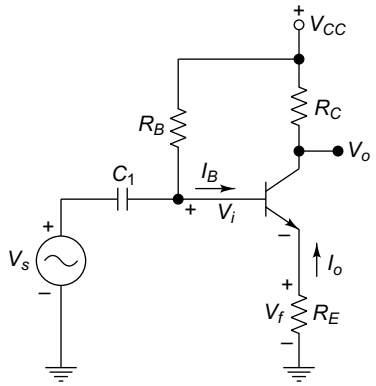


Fig. 2.33 *BJT amplifier with current–series feedback*

$$= -\frac{\beta}{r_\pi + \beta R_E}$$

Voltage gain with feedback is

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_C}{V_s} = \frac{I_o}{V_s} R_C = \left(-\frac{\beta}{r_\pi + \beta R_E} \right) R_C = -\frac{\beta R_C}{r_\pi + \beta R_E}$$

Input and output Impedances without feedback k

$Z_i = R_B \parallel r_\pi$, assuming $R_E = 0$

$Z_o = R_C$

Input and output impedances with feedback

$$Z_{if} = Z_i (1 + BA) = r_\pi + \beta R_E$$

$$Z_{of} = Z_o (1 + BA) = R_C \left(1 + \frac{\beta R_E}{r_\pi} \right)$$

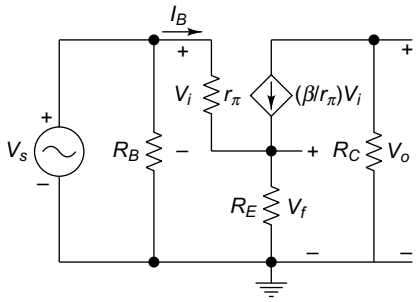


Fig. 2.34 *Equivalent circuit of BJT amplifier*

It is clear from the above expressions that input and output impedances are increased in current–series feedback amplifier.

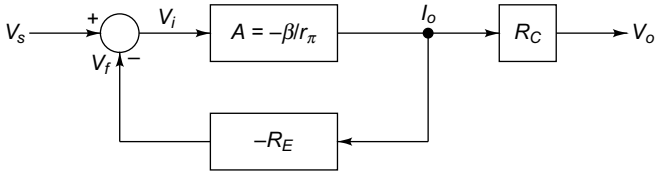


Fig. 2.35 *Block-diagram representation of BJT amplifier with current–series feedback*

2.16 Determine the voltage gain of BJT amplifier with current–series feedback as depicted in Fig. 2.33 with the following parameters β = 100, r_π = 800 Ω, R_C = 2.47 kΩ, R_E = 470 Ω, and R_B = 470 Ω.

Solution

Amplifier gain is

$$A = \frac{I_o}{V_s} = -\frac{\beta}{r_\pi + \beta R_E} = -\frac{100}{800 + 100 \times 470} = -0.00209$$

Voltage gain with feedback is

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_C}{V_s} = \frac{I_o}{V_s} R_C = \left(-\frac{\beta}{r_\pi + \beta R_E} \right) R_C = -\frac{\beta R_C}{r_\pi + \beta R_E}$$

$$= -\frac{100 \times 2.47 \times 10^3}{800 + 100 \times 470} = -5.167$$

2.9.4 Voltage Shunt Feedback

Figure 2.36 shows the voltage shunt feedback. Its equivalent circuit is illustrated in Fig. 2.37. The gain of the amplifier

$$A = \frac{V_o}{I_i}, A \to \infty \qquad \text{as} \quad I_i = 0$$

The feedback gain is $\beta = \dfrac{I_f}{V_o} = -\dfrac{1}{R_f}$

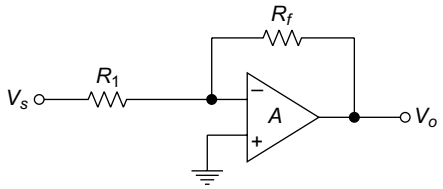


Fig. 2.36 *Voltage–shunt negative feedback amplifier*

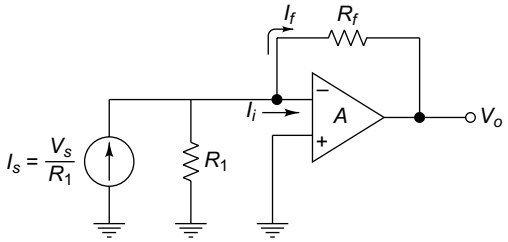


Fig. 2.37 *Equivalent circuit of voltage–shunt negative feedback amplifier*

The block–diagram representation of Fig. 2.36 is depicted in Fig. 2.38.
The overall loop gain is

$$A_f = \frac{V_o}{I_s} = \frac{A}{1+\beta A} = \frac{A}{1-\dfrac{A}{R_f}} = -R_f \qquad \text{as} \quad A \to \infty \text{ and } I_i = 0$$

The voltage gain is

$$A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s}\frac{I_s}{V_s} = -\frac{R_f}{R_1} \quad \text{as} \quad \frac{V_o}{I_s} = -R_f \text{ and } \frac{I_s}{V_s} = -\frac{1}{R_1}$$

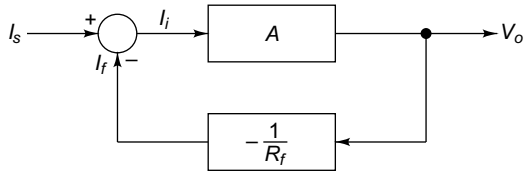


Fig. 2.38 *Block-diagram representation of voltage-shunt negative feedback amplifier*

2.17 Figure 2.39 shows the transistor feedback amplifier circuit and it has the following parameters

$$h_{ie} = 1\text{k}\Omega, \text{ and } h_{fe} = 50,\ R_C = 10\text{k}\Omega,\ R_B = 1\text{k}\Omega,\ R_F = 100\text{k}\Omega$$

Determine the topology of the feedback and compute $\frac{V_o}{V_S}$, R_{if} and R_{of}.

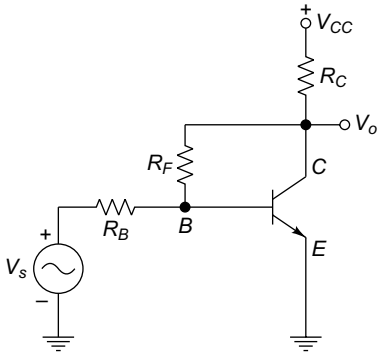


Fig. 2.39

Solution

The feedback signal is proportional to output voltage and is connected in shunt with input signal. Therefore, this circuit is a voltage–shunt topology.

The resistance R_F is connected between the collector terminal of transistor (output) and the base terminal of transistor (input). Applying Miller's theorem, the R_F can be replaced by the two resistances R_1 and R_2 as shown in Fig. 2.40. The values of R_1 and R_2 are given below:

$$R_1 = \frac{R_F}{1-K} \text{ and } R_2 = R_F \frac{K}{K-1}$$

where, $$K = \frac{\text{Collector voltage}}{\text{Base voltage}} = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \text{Voltage gain of amplifier} = A_V$$

The effective load resistance $R_L = R_C \parallel R_2$

where $$R_2 = \frac{100\text{k} \times A_V}{A_V - 1} \text{ and } R_C = 10\text{k}\ \Omega$$

$$R_L = \frac{10\text{k} \times \frac{100\text{k} \times A_V}{A_V - 1}}{10K + \frac{100\text{k} \times A_V}{A_V - 1}} = \frac{1000 \times A_V}{110A_V - 10}\text{k}\ \Omega$$

The voltage gain of transistor

$$A_V = -\frac{h_{fe}}{h_{ie}} R_L = -\frac{50}{1000} R_L = -\frac{50}{1000} \times \frac{1000 \times A_V}{110A_V - 10}\text{k}\,\Omega$$

$$= -\frac{50A_V}{110A_V - 10} \times 1000$$

or, $110\ A_V - 10 = -50 \times 1000$

or $$A_V = \frac{-50 \times 1000 + 10}{110} = -454.45$$

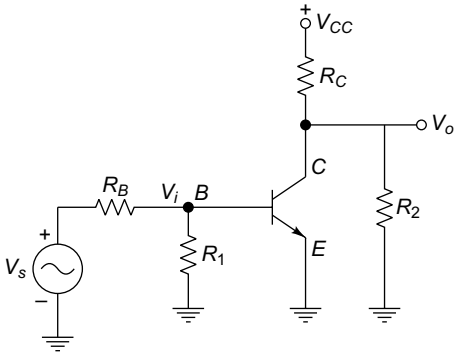


Fig. 2.40

The value of $R_1 = \frac{R_F}{1-K} = \frac{R_F}{1-A_V} = \frac{100K}{1-(-454.45)} = 219.56\ \Omega$

The value of $R_2 = R_F \frac{K}{K-1} = R_F \frac{A_V}{A_V - 1} = 100K \frac{(-454.45)}{-454.45-1} \approx 100\text{k}\Omega$

$$R_i = h_{ie} = 1K\Omega$$

$$R_{ieff} = R_1 \parallel R_i = 219.56 \parallel 1K = 180\ \Omega$$

The voltage gain $\frac{V_o}{V_S} = \frac{V_o}{V_i} \times \frac{V_i}{V_S} = A_V \times \frac{V_i}{V_S}$

The $\frac{V_i}{V_S} = \frac{R_{ieff}}{R_{ieff} + R_s} = \frac{180}{180+1000} = 0.1525$

The voltage gain is $\frac{V_o}{V_S} = A_V \times 0.1525 = (-454.45) \times 0.1525 = -69.30$

The output impedance $R_{of} = R_C \parallel R_2 = 10K \parallel 100K = 9.09$ K

2.18. Figure 2.41 shows the transistor feedback amplifier circuit and it has the following parameters: $h_{ie} = 2$ kΩ, and $h_{fe} = 100$, $R_C = 10$ kΩ, $R_E = 1$ kΩ, $R_B = 1$ kΩ, $R_F = 100$ kΩ

Determine the topology of the feedback and compute $\frac{V_o}{V_S}$, R_{if} and R_{of}.

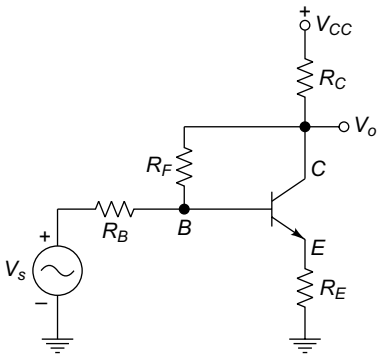


Fig. 2.41 *Circuit of Ex. 2.18*

Solution

The feedback signal is proportional to output voltage and is connected in shunt with input signal. Therefore, this circuit is a voltage–shunt topology.

The resistance R_F is connected between the collector terminal of transistor (output) and the base terminal of transistor (input). Applying Miller's theorem, the R_F can be replaced by the two resistances R_1 and R_2 as depicted in Fig. 2.42. The resistances R_1 and R_2 can be expressed as

$$R_1 = \frac{R_F}{1-K} \text{ and } R_2 = R_F \frac{K}{K-1} \qquad \text{where} \quad K = A_V$$

The effective load resistance $R_L = R_C \parallel R_2$

where $$R_2 = \frac{100K \times A_V}{A_V - 1} \qquad \text{and} \quad R_C = 10\text{k}\Omega$$

$$R_L = \frac{10K \times \frac{100K \times A_V}{A_V - 1}}{10K + \frac{100K \times A_V}{A_V - 1}} = \frac{1000 \times A_V}{110A_V - 10}\text{k}\Omega$$

The input resistance is

$$R_i = h_{ie} + (1 + h_{fe})R_E = 2K + (1 + 100)\ 1K = 103\ \text{k}\Omega$$

The voltage gain of transistor is

$$A_V = -\frac{h_{fe}}{h_{ie}} R_L = \frac{100}{2000} R_L = \frac{100}{2000} \times \frac{1000 \times A_V}{110A_V - 10}\text{k}\Omega$$

$$= -\frac{50A_V}{110A_V - 10} \times 1000$$

or, $110\ A_V - 10 = -50 \times 1000$

or, $$A_V = \frac{-50 \times 1000 + 10}{110} = -454.45$$

The value of $$R_1 = \frac{R_F}{1-K} = \frac{R_F}{1-A_V} = \frac{100K}{1-(-454.45)} = 219.56\ \Omega$$

The value of $R_2 = R_F \frac{K}{K-1} = R_F \frac{A_V}{A_V - 1} = 100K \frac{(-454.45)}{-454.45 - 1} \approx 100\ \text{k}\Omega$

$$R_{leff} = R_1 \parallel R_i = 219.56 \parallel 103\ \text{k}\Omega = 219.09\ \Omega$$

The voltage gain $\frac{V_o}{V_S} = \frac{V_o}{V_i} \times \frac{V_i}{V_S} = A_V \times \frac{V_i}{V_S}$

The $$\frac{V_i}{V_S} = \frac{R_{ieff}}{R_{ieff} + R_s} = \frac{219.09}{219.09 + 1000} = 0.179$$

The voltage gain $\frac{V_o}{V_S} = A_V \times 0.179 = (-454.45) \times 0.179 = -81.34$

The output impedance $R_{of} = R_C \,||\, R_2 = 10K \parallel 100\ K = 9.09K$

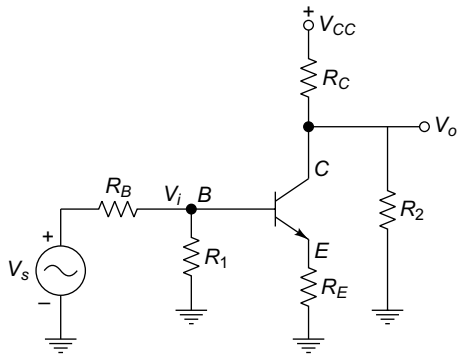


Fig. 2.42 *Solution of Ex. 2.18*

2.19 Figure 2.43 shows the transistor feedback amplifier circuit and it has the following parameters:

h_{ie} = 2kΩ , and h_{fe} = 100, R_{C1} = 10kΩ, R_{C2} = 1kΩ, R_E = 0.1kΩ, R_S = 2kΩ, R_f = 1kΩ

Determine the topology of the feedback, gain A_V and R_{if}.

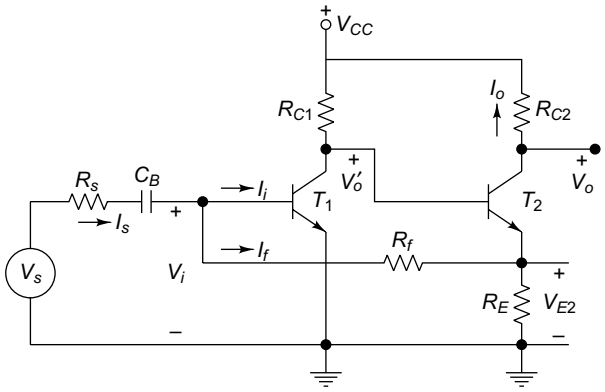


Fig. 2.43 *Emitter to base feedback amplifier circuit*

Solution

In Fig. 2.43, transistors T_1 and T_2 are connected in cascade. The feedback resistance R_f is connected between the emitter of T_2 and base of T_1 to provide a feedback path. The output voltage of transistor T_1 is the output voltage of first stage amplifier V_o and it is 180° out of phase from the input voltage V_i. The voltage across R_E is V_{E2}. The output voltage V_o is connected in series with the voltage V_{E2}. The topology of the feedback is current shunt or series shunt feedback.

The source current is the sum of input current and feedback current, i.e. $I_S = I_i + I_f$. The feedback current is equal to

$$I_f = \frac{V_i - V_{E2}}{R_f}$$

Since $V_{E2} >> V_i$, $I_f = -\frac{V_{E2}}{R_f}$

After neglecting the base current of transistor T_2, we obtain the emitter voltage

$$V_{E2} = (I_f - I_o)\, R_{E2}$$

Then $$I_f = -\frac{V_{E2}}{R_f} = -\frac{(I_f - I_o)R_{E2}}{R_f}$$

or $$I_f = \frac{R_{E2}}{R_f + R_{E2}} I_o$$

As feedback current is directly proportional to the output current I_o, the feedback configuration is current shunt or series shunt feedback.

This feedback amplifier circuit can be analyzed by using Miller's theorem. It is possible to replace the feedback resistance R_f with two equivalent resistances R_1 and R_2 as shown in Fig. 2.44.

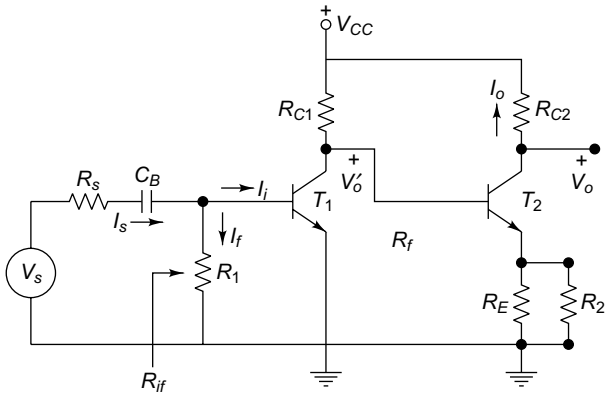


Fig. 2.44 ***Miller theorem applied to emitter to base feedback amplifier circuit of Fig. 2.43***

The values of R_1 and R_2 are

$$R_1 = \frac{R_f}{1 - A_V'} \text{ and } R_2 = \frac{R_f}{1 - 1/A_V'}$$

where, $A_V' = \frac{V_{E2}}{V_i}$ = voltage gain from base of transistor T_1 to the emitter of transistor T_2.

As $A_V' >> 1$, the effective emitter resistance is

$$R_E' = R_E \parallel R_f = 100 \parallel 1000\ \Omega = 90.909\ \Omega$$

The input resistance of T_2 is

$$R_{i2} = h_{ie} + (1 + h_{fe})R_E' = 2000 + (1+100)90.909\ \Omega = 11181.809\ \Omega$$

The voltage gain from base to collector of transistor T_2 is

$$A_{V_2} = 1 - \frac{h_{ie}}{R_{i2}} = 1 - \frac{200}{11181.809} = 0.821$$

The effective load resistance of T_1 is

$$R_L' = R_{C1} \parallel R_{i2} = 10{,}000 \parallel 11181.809\ \Omega = 5278.96\ \Omega$$

The voltage gain of transistor T_1 from base to collector is

$$A_{V1} = -\frac{h_{fe}}{h_{ie}} R_L' = -\frac{100}{2000} \times 5278.96 = -263.94$$

The voltage gain $A_V' = A_{V1} \times A_{V2} = (-263.94) \times 0.821 = -216.70$

The value of R_1 is

$$R_1 = \frac{R_f}{1 - A'_V} = \frac{1000}{1 + 216.70} = 4.59\,\Omega$$

The input impedance $R_{if} = R_1 \parallel R_{i1} = R_1 \parallel h_{ie} = 4.59 \parallel 2000 = 4.579\ \Omega$

The resistance of signal source is

$$R_S + R_{if} = (2000 + 4.579)\ \Omega = 2004.579\ \Omega$$

2.10 STABILITY OF A FEEDBACK AMPLIFIER

In this chapter, negative feedback amplifier is discussed so far. The gain A and phase shift of a feedback amplifier are functions of frequency. For negative feedback operation, $|1 + \beta A| > 1$. If $|1 + \beta A| < 1$, the feedback becomes positive or regenerative. During positive feedback, the overall gain A_f is greater than A. Therefore, regeneration means increasing the amplification of the amplifier.

If an amplifier is designed to operate at negative feedback at a specified frequency and it oscillates at some other frequency then the amplifier is not very useful for that specified application. As a result, feedback amplifiers must be designed in such a way that the circuit must be stable over a wide range of frequency or all frequencies. Otherwise, transient response makes the amplifier unstable. Any feedback amplifier will be stable when transient disturbance produces a response, but the amplitude of response must decay with time. The feedback system will be unstable if any transient disturbance persists indefinitely and output response increases with time, but amplitude of output response is limited by nonlinearity of the circuit parameters. For any stable system, all poles of the transfer function or the zeros of $(1 + \beta A)$ must be in the left half of the complex frequency plane. The stability of an amplifier can be investigated using the Nyquist criterion.

2.10.1 Nyquist Criterion

The gain A and phase shift of a feedback amplifier are functions of frequency. As βA is also a complex quantity and function of frequency, different points on the complex plane can be obtained corresponding to different values of frequency. When frequency is varied from $+\infty$ to $-\infty$, βA is plotted on a complex plane with the real component along the X-axis and the imaginary component along the Y-axis and a closed curve is formed by the locus of $(1 + \beta A)$. The locus of $|1 + \beta A|$ is a circle of unit radius with the center at point $(-1 + j0)$. This plot is known as Nyquist plot as shown in Fig. 2.45.

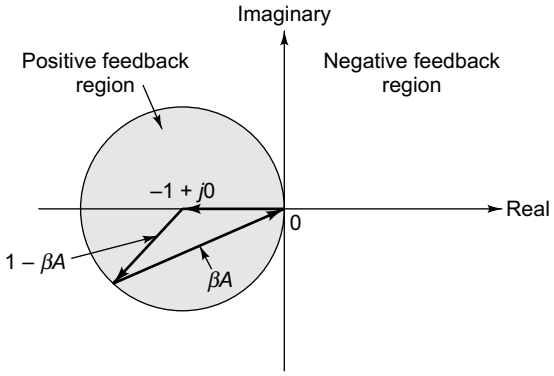


Fig. 2.45 *Locus of* $|1 + \beta A|$

The Nyquist criterion states that the amplifier is unstable if the Nyquist plot encloses the point $(-1 + j0)$ and the amplifier is stable if the curve does not enclose the point $(-1 + j0)$. The Nyquist criterion for positive and negative feedback is represented in the complex plane as depicted in Fig. 2.45. Figure 2.46 shows the frequency response of a feedback amplifier in the complex plane. When frequency is varied from 0 to f_1, the feedback is negative. During the frequency range from f_1 to ∞, the feedback is positive as shown in Fig. 2.46.

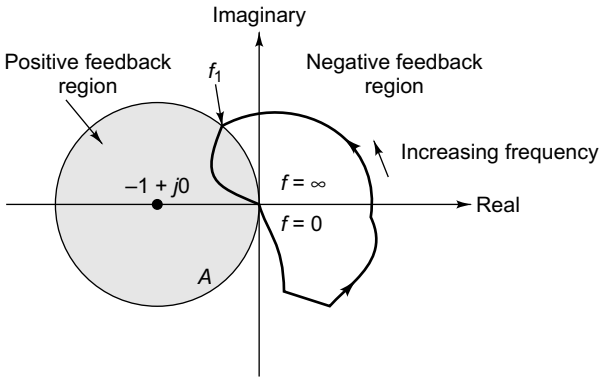


Fig. 2.46 ***Locus of βA in the complex plane for a feedback circuit which acts as negative feedback form $f = 0$ to $f = f_1$ and acts as positive feedback form $f = f_1$ to $f = \infty$***

At any frequency range, if the locus of βA does not enclose the point $(-1 + j0)$, the feedback is negative and the amplifier is stable. When the locus of βA enclose the point $(-1 + j0)$, the feedback is positive and amplifier is unstable as illustrated in Fig. 2.47. In this case, positive feedback amplifier acts as an oscillator whenever Nyquist criterion is satisfied.

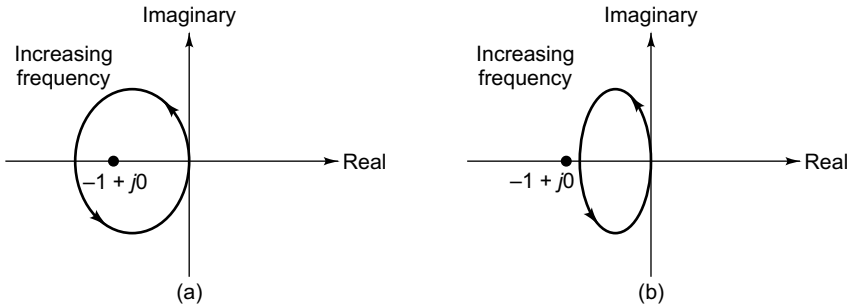


Fig. 2.47 ***Nyquist plot of feedback amplifier: (a) unstable (b) stable***

EXERCISES

Short- and Long-Answer-Type Questions

1. Define feedback amplifier. What are the types of feedback amplifiers? Write advantages of a feedback amplifier.
2. What do you mean by negative feedback and positive feedback? Derive the overall gain of negative feedback and positive feedback amplifiers. What is the amount of feedback of a negative feedback amplifier?

3. Explain the following amplifiers:
   a. Voltage amplifier
   b. Current amplifier
   c. Transconductance amplifie
   d. Transresistive amplifier
4. Draw a schematic block diagram of feedback amplifier and the working principle of a feedback amplifier in detail.
5. Justify the statement " Negative feedback can reduce the gain of an amplifier".
6. What are the different topologies of feedback amplifier? Explain any one feedback topology with an example.
7. Draw a voltage series feedback amplifier circuit and derive the following parameters:
   (a) Overall amplifier gain
   (b) Input impedance
   (c) Output impedance
8. Draw the circuit diagram of an emitter follower circuit. What type of feedback topology is used in this circuit? Derive the overall loop gain of the amplifier.
9. Give a list of properties of a feedback amplifier.
10. Explain the following terms:
    (a) Gain stability of negative feedback amplifier
    (b) Effect of negative feedback on bandwidth
    (c) Effect on input impedance of series–series feedback amplifier
    (d) Effect on output impedance of voltage–series feedback amplifier
11. Define the following terminology:
    (a) Feedback ratio
    (b) Feedback factor
    (c) Amount of feedback in dB
    (e) Phase distortion of negative feedback amplifier
12. Calculate the gain of a negative feedback amplifier if $A = -1000$ and $\beta = -1/10$.
13. When the gain of an amplifier changes from a value of –1000 by 10%, determine the gain change if the amplifier is used in a negative feedback circuit and $\beta = -1/50$.
14. Determine the gain, input and output impedances of a voltage–series feedback amplifier having $A = -200$, $R_i = 1.5$ kΩ, $R_o = 100$ kΩ and $\beta = -1/50$.
15. Compute the gain with and without feedback for an FET amplifier as shown in Fig. 2.48 for $R_1 = 500$ kΩ, $R_2 = 250$ kΩ, $R_o = 40$ kΩ $R_D = 8$ kΩ and $g_m = 1000$ μs
16. Figure 2.49 shows a BJT amplifier circuit. What type of feedback topology is used in this circuit? Calculate the gain,

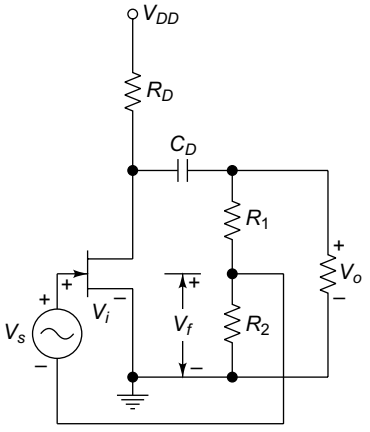


Fig. 2.48

input and output impedance with feedback R_B = 100 kΩ, R_E = 1.2 kΩ, R_C = 4.7 kΩ, h_{fe} = 100 and h_{ie} = 1000.

17. An amplifier with a gain of 2500 has an output voltage of 10 V. A negative feedback is provided to reduce the gain to 10%. What should be the gain of the feedback path?
18. A feedback amplifier consists of four amplifying blocks and each amplifying block has a gain of 10.
    (a) What should be the gain of the feedback path in order to maintain overall gain to 75?
    (b) If the gain of each amplifier block has been reduced to 80% of actual value due to parameter variation, what is the % change in the overall gain of feedback amplifier?

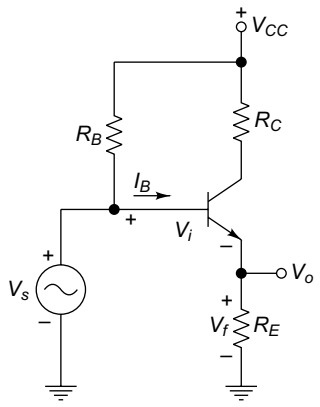


Fig. 2.49

19. An amplifier has an open-loop gain of A = 250. (a) Calculate the feedback path gain to provide overall gain of A_f = 100. (b) When A is increased by 10%, calculate the new A_f. What is the percentage change in A_f?
20. An amplifier has gain of –20000 and feedback of β = –0.1. Due to temperature rise, gain change is about 10%. What will be the change in gain of the feedback amplifier?
21. In a voltage–series feedback amplifier A = 5000, R_i = 100 Ω, R_o = 100 kΩ and β = 0.1 Compute input impedance, and output impedance of feedback amplifier.
22. Determine the overall loop gain, input and output impedances for an amplifier in a current series feedback amplifier with A = 1000, R_i = 2 kΩ, R_o = 50 kΩ and β = 0.01.
23. A voltage series feedback amplifier has A = –1000, R_i = 20 kΩ, R_o = 100 kΩ and feedback factor β = –0.2. (a) Find overall gain, input impedance, and output impedance of feedback amplifier. (b) If the gain has been reduced to –200, what will be the feedback factor?
24. The transistor feedback amplifier circuit is depicted in Fig. 2.50 and it has the following parameters:

    h_{ie} = 2kΩ, and h_{fe} = 120, R_C = 5kΩ, R_E = 1kΩ, R_B = 1kΩ, R_F = 100kΩ

    Determine the topology of the feedback and compute $\frac{V_o}{V_S}$, R_{if} and R_{of}.

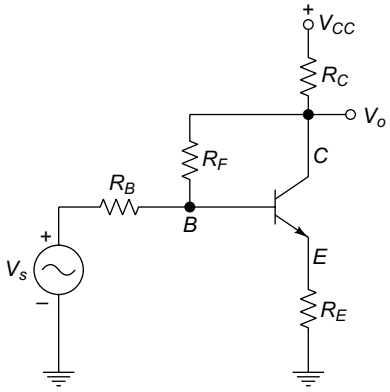


Fig. 2.50

25. Figure 2.51 shows the transistor feedback amplifier circuit and it has the following parameters

h_{ie} = 1kΩ, and h_{fe} = 50, R_{C1} = 5kΩ, R_{C2} = 1kΩ, R_E = 50, R_S = 1kΩ, R_f = 1kΩ.

Explain the topology of this feedback amplifier and determine A_{V1}, A_{V2}, A_V, and R_{if}. Assume any missing parameters.

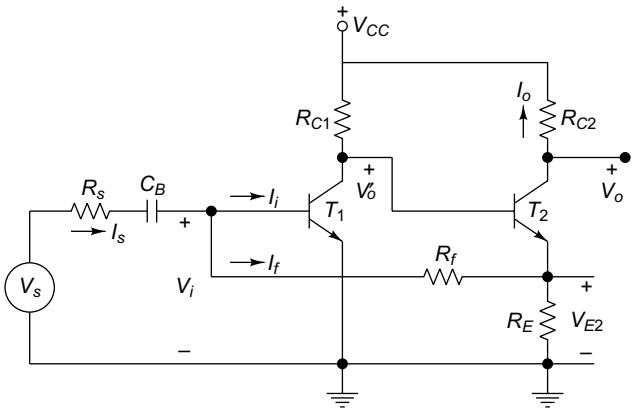


Fig. 2.51

26. Define desensitivity D. What is relation between D and A_f?
27. State the Nyquist criterion of stability of a feedback amplifier.
28. Explain sensitivity of a feedback amplifier.

MULTIPLE CHOICE QUESTIONS

1. A negative feedback amplifier has a gain A and feedback path gain is β. What will be the overall gain of amplifier?

(a) $\frac{A}{1+\beta A}$ (b) $\frac{1+A}{1+\beta A}$ (c) $\frac{A}{1-\beta A}$ (d) $\frac{1-\beta A}{A}$

Answer: (a) $\frac{A}{1+\beta A}$

2. A positive feedback amplifier has a gain A and feedback path gain is β. What will be the overall gain of amplifier?

(a) $\frac{A}{1-\beta A}$ (b) $\frac{1+A}{1+\beta A}$ (c) $\frac{A}{1+\beta A}$ (d) $\frac{1-\beta A}{A}$

Answer: (a) $\frac{A}{1-\beta A}$

3. The transfer characteristics of voltage amplifier is

   (a) $A_v = \frac{V_o}{V_s}$ (b) $A_I = \frac{I_o}{I_s}$ (c) $g_m = \frac{I_o}{V_s}$ (d) $r_m = \frac{V_o}{I_s}$

   Answer: (a) $A_v = \frac{V_o}{V_s}$

4. An amplifier has gain of –1000 and feedback of β = –0.1. If it had a gain change of 20% due to temperature, what will be the change in gain of the feedback amplifier?

   (a) 1% (b) 2% (c) 0.5% (d) 0.2%

   Answer: (d) 0.2%

5. An amplifier has an open-loop gain of 100, an input impedance of 1 kΩ and an output impedance of 100 Ω. A feedback network with a feedback factor of 0.5 is connected in a voltage–series feedback mode. The new input and output impedance are

   (a) 51 kΩ and 2 Ω (b) 510 kΩ and 20 Ω

   (c) 5.1 kΩ and 200 Ω (d) 5 kΩ and 100 Ω

   Answer: (a) 51 kΩ and 2 Ω

6. An operational amplifier has an open-loop gain of 10^4 and open loop upper cutoff frequency of 10 Hz. If this operational amplifier is connected as an amplifier with a closed-loop gain of 100, what will be the new upper cut-off frequency?

   (a) 1000 Hz (b) 100 Hz (c) 10 Hz (d) 1 Hz

   Answer: (a) 1000 Hz

7. Figure 2.52 shows the feedback amplifier circuit. What is the type of feedback used in this circuit?

   (a) Voltage–series feedback

   (b) Voltage–shunt feedback

   (b) Current–series feedback

   (d) Current–shunt feedback

   Answer: (a)Voltage–series feedback

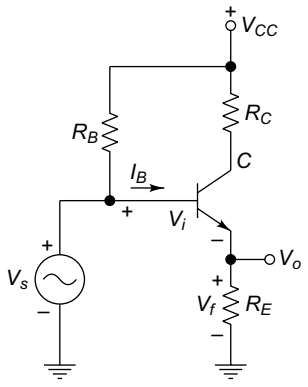


Fig. 2.52

8. Which topology of feedback amplifier has very high input and output impedances?

   (a) Voltage–series feedback

   (b) Voltage–shunt feedback

   (c) Current–series feedback

   (d) Current–shunt feedback

   Answer: (c) Current–series feedback

9. An amplifier with mid-band gain A = 500 has a negative feedback $\beta = \frac{1}{100}$.

   If the upper cut-off without feedback is 600 Hz, then with feedback it would become.

(a) 3000 Hz (b) 300 kHz (c) 30 Hz (d) 3 Hz

Answer: (a) 3000 Hz

10. The feedback factor of the circuit is shown in Fig. 2.53 is

(a) $\frac{10}{15}$ (b) $\frac{5}{15}$ (c) $\frac{1}{10}$ (d) $\frac{1}{5}$

Answer: (a) $\frac{10}{15}$

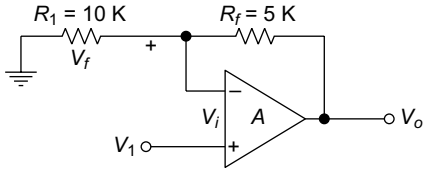


Fig. 2.53

11. Figure 2.54 shows an op-amp feedback amplifier circuit. What the type of feedback is it?

(a) Voltage–shunt feedback (b) Current–series feedback
(c) Voltage–series feedback (d) Current–shunt feedback

Answer: (a) Voltage–shunt feedback

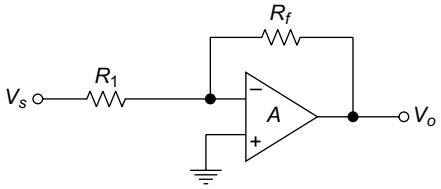


Fig. 2.54

12. In a common emitter amplifier, the unbypassed emitter resistance provides

(a) voltage–series feedback (b) voltage–shunt feedback
(c) current–series feedback (d) current–shunt feedback

Answer: (c) current–series feedback

13. The amount of feedback in negative feedback amplifier is expressed as

(a) $20\log_{10}\left|\frac{1}{1+\beta A}\right|$ (b) $20\log_{10}\left|\frac{1}{1-\beta A}\right|$

(c) $40\log_{10}\left|\frac{1}{1+\beta A}\right|$ (d) $40\log_{10}\left|\frac{1}{1-\beta A}\right|$

Answer: (a) $20\log_{10}\left|\frac{1}{1+\beta A}\right|$

14. The input and output impedances of a current shunt feedback amplifier is

(a) $\frac{Z_i}{1+\beta A}$ and $Z_0(1 + \beta A)$ (b) $Z_i (1 + \beta A)$ and $\frac{Z_o}{1+\beta A}$

(c) $\frac{Z_o}{1+\beta A}$ and $\frac{Z_o}{1+\beta A}$ (d) $Z_i (1 + \beta A)$ and $Z_o (1 + \beta A)$

Answer: (a) $\frac{Z_i}{1+\beta A}$ and $Z_0(1 + \beta A)$

15. The advantages of negative feedback amplifier are
(a) high input impedance (b) increase gain stability
(c) low output impedance (d) all

Answer: (d) all

16. A transconductance amplifier has
(a) high input impedance and high output impedance
(b) high input impedance and low output impedance
(c) low input impedance and low output impedance
(d) low input impedance and high output impedance

Answer: (a) high input impedance and high output impedance

17. Voltage–shunt feedback amplifier is a
(a) transconductance amplifier (b) transresistive amplifier
(c) voltage amplifier (d) current amplifier

Answer: (b) transresistive amplifier

18. A transreistive amplifier has
(a) low input impedance and high output impedance
(b) high input impedance and low output impedance
(c) low input impedance and low output impedance
(d) high input impedance and high output impedance

Answer: (a) low input impedance and high output impedance

19. Negative feedback increases the performance parameters except
(a) gain (b) input impedance
(c) noise distortion (d) 3 dB frequency

Answer: (a) gain

20. The transfer characteristic of transconductance amplifier is

(a) $g_m = \frac{I_o}{V_s}$ (b) $A_i = \frac{I_o}{I_s}$ (c) $A_v = \frac{V_o}{V_s}$ (d) $r_m = \frac{V_o}{I_s}$

Answer: (a) $g_m = \frac{I_o}{V_s}$

UNIVERSITY QUESTIONS WITH ANSWERS

Multiple-Choice-Type Questions

1. For an emitter follower, the voltage gain is
(a) unity (b) greater than unity
(c) less than unity [WBUT-2007] [WBUT-2008]

2. In case of voltage series feedback in an amplifier, the input resistance due to feedback
   (a) increases (b) decreases
   (c) zero (d) remains unchanged [WBUT-2008]
3. In a current amplifier
   (a) input is voltage, output is current
   (b) input is voltage, output is power
   (c) input is current, output is voltage
   (d) input is current, output is current [WBUT-2008]
4. In a transconductance amplifier
   (a) input is voltage, output is current
   (b) input is voltage, output is voltage
   (c) input is current, output is voltage
   (d) input is power, output is voltage [WBUT-2008]
5. Input and output impedances of a voltage shunt feedback are
   (a) $Z_i/(1 + A\beta)$ and $Z_o/(1 + A\beta)$
   (b) $Z_i(1 + A\beta)$ and $Z_o/(1 + A\beta)$
   (c) $Z_i/(1 + A\beta)$ and $Z_o(1 + A\beta)$
   (d) $Z_i(1 + A\beta)$ and $Z_o(1 + A\beta)$ [WBUT-2009]
6. In an amplifier
   (a) we apply a degenerative feedback
   (b) we apply a regenerative feedback
   (c) bandwidth decreases due to feedback [WBUT-2009]
7. Feedback amplifier in an amplifier always helps to
   (a) control its output
   (b) increase its gain
   (b) decrease its input impedance
   (d) stabilize its gain [WBUT-2009]
8. Voltage series negative feedback
   (a) increases input and output impedances
   (b) increases input impedance and decreases output impedance
   (c) decreases input and output impedances
   (d) increases output impedance and decreases input impedance
   [WBUT-2010]

Solutions

1 (a) unity
2 (a) increases;
3 (d) input is current, output is current
4 (a) input is voltage, output is current
5 (a) $Z_i/(1 + A\beta)$ and $Z_o/(1 + A\beta)$
6 (a) we apply a degenerative feedback
7 (d) stabilize its gain
8 (b) increases input impedance and decreases output impedance

Short- and Long-Answer-Type Questions

1. How does the negative feedback increase the bandwidth of the amplifier?

[WBUT-2002]

Solution

The difference between the upper cut-off frequency f_2 and lower cutoff frequency f_1 is called as bandwidth of an amplifier and it can be expressed as

$$BW = f_2 - f_1$$

When the negative feedback is applied in an amplifier, the cut-off frequencies are also effected. The lower cut-off frequency is reduced by a factor of $(1 + \beta A_o)$ but the upper cut-off frequency is increased by a factor $(1 + \beta A_o)$. When feedback is used, there is some reduction in gain in low frequency and high frequency region. The feedback amplifier has a higher upper 3-dB frequency and smaller 3-dB frequency.

The bandwidth with feedback is $BW_f = f_{2f} - f_{1f}$

where upper cut-off frequency $f_{2f} = f_2 (1 + \beta A_o)$

lower cut-off frequency $f_{1f} = \dfrac{f_1}{1 + \beta A_o}$

Since amplifier with negative feedback has larger bandwidth with respect to bandwidth without feedback.

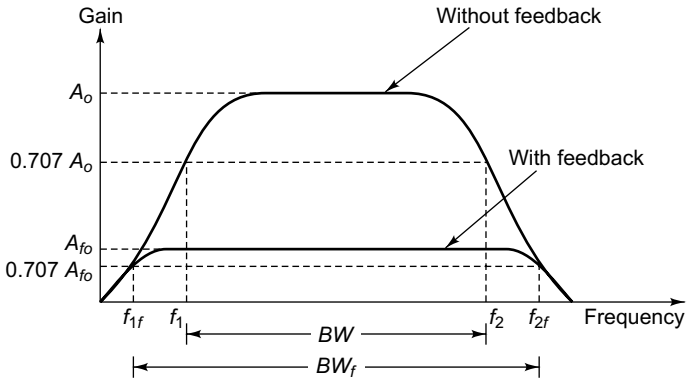


Fig. 2.55 ***Effect of negative feedback on bandwidth***

2. Establish the expressions for current gain, voltage gain, input resistance and output resistance of a CE transistor amplifier in terms of *h* parameters.

[WBUT-2002] [WBUT-2007] [WBUT-2008]

Solution

Figure 2.56 shows the *h*-parameter equivalent circuit of CE amplifier. The derivation of input resistance, output resistance, voltage gain and current gain are given below:

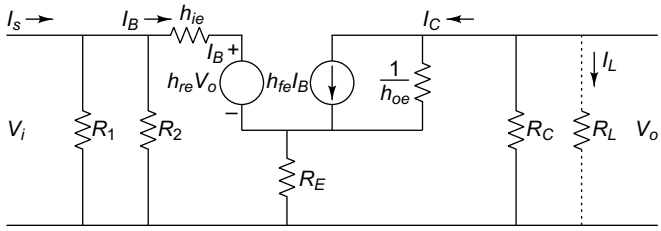


Fig. 2.56 ***Equivalent circuit of CE transistor amplifier***

Input Resistance

Looking from base emitter terminals, we find that h_{ie} is in series with $h_{re}V_o$. If we assume h_{re} is very small, the $h_{re}V_o$ is negligible with respect to voltage drop across h_{ie}. The input resistance is equal to

$$R_i = R_1 \parallel R_2 \parallel Z_B$$

where $$Z_B = \frac{V_i}{I_B} = \frac{h_{ie}I_B + R_E(I_B + I_C)}{I_B} = \frac{h_{ie}I_B + R_E I_B + R_E h_{fe} I_B}{I_B}$$

$$= h_{ie} + R_E(1 + h_{fe})$$

Output Resistance

Looking from collector emitter terminals output resistance is $R_o = \frac{1}{h_{oe}}$,

but actual output resistance is $R_o = \frac{1}{h_{oe}} \parallel R_C$

Voltage gain

The voltage gain is $A_V = \frac{V_O}{V_i} = -\frac{I_C(R_C \parallel R_L)}{I_B(h_{ie} + R_E(1+h_{fe}))}$

as $V_i = I_B\,(h_{ie} + R_E(1 + h_{fe}))$

$$= -\frac{h_{fe}I_B(R_C \parallel R_L)}{I_B(h_{ie} + R_E(1+h_{fe}))} = -\frac{h_{fe}(R_C \parallel R_L)}{(h_{ie} + R_E(1+h_{fe}))}$$

Current gain

$$I_L = I_C \frac{R_C}{R_C + R_L} = \frac{h_{fe}R_C}{R_C + R_L} I_B \text{ as } I_C = h_{fe}I_B$$

$$I_B = I_S \frac{R_B}{R_B + Z_B} \text{ where, } R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

The current gain is $A_i = \frac{I_L}{I_S} = \frac{-h_{fe}R_B R_C}{(R_C + R_L)(R_B + Z_B)}$

3. With the help of block diagram explain negative feedback amplifier. Point out function of each block and derive an expression for gain with negative feedback. [WBUT-2002]

Solution Refer Section 2.4.

4. Find the gain and feedback factor for (i) shunt–series (ii) shunt–shunt (iii) series–shunt (iv) series-series feedback circuits. Draw the block diagrams for each case. [WBUT-2002]

   Solution Refer Section 2.5.

5. Discuss the effect of –ve feedback on stability and gain. [WBUT-2002]

   Solution Refer Section 2.7.4.

6. (a) The open loop gain of an amplifier changes by 20% due to changes in the parameters of the active amplifying device. If a change of gain by 2% is allowable, what type of feedback has to be applied?

   (b) If the amplifier gain with feedback is 10, find the value of feedback ratio for an open loop gain of 100? [WBUT-2003]

   Solution

   (a) In a feedback amplifier

   $$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1+\beta A|}\left|\frac{dA}{A}\right|$$

   where A_f = closed loop gain, A = open loop gain and β = feed back ratio

   Here $\frac{dA_f}{A_f} = 2\% = \frac{2}{100}$ and $\frac{dA}{A} = 20\% = \frac{20}{100}$

   Therefore, $\frac{2}{100} = \frac{20}{100}\frac{1}{1+\beta A}$

   Then $\beta A = 9$

   As $\beta A > 1$, negative feedback to be applied.

   (b) The overall loop gain of a feedback amplifier is

   $$A_f = \frac{A}{1+\beta.A}$$

   if $A_f = 10$, $A = 100$, we can write $10 = \frac{100}{1+100\beta}$

   Then $\beta = \frac{9}{100} = 0.09$

7. Show the different feedback topologies with appropriate block diagrams. [WBUT-2003]

   Solution Refer Section 2.5.

8. FET amplifier in the common source configuration uses a load resistance of 150 kΩ. The ac drain resistance of the device is 100 kΩ and the transconductance is 0.5 mA/V. What is the voltage gain of the amplifier? [WBUT-2004]

   Solution

   Amplification factor $\mu = r_d \times g_m$ where r_d = drain resistance and g_m = transconductance

   Given $g_m = 0.5$ mA/V, $r_d = 100$ kΩ and $R_L = 150$ kΩ

The voltage gain

$$A_V = \frac{V_O}{V_i} = \frac{g_m r_d . R_L}{R_L + r_d}$$

$$= \frac{0.5 \times 10^{-3} \times 100 \times 10^3 \times 150 \times 10^3}{(150 + 100) \times 10^3} = 30$$

9. (a) What do you understand by negative feedback?
   (b) What is feedback factor? [WBUT-2004]

   Solution

   (a) Refer Section 2.2

   (b) Feedback factor: The ratio of feedback voltage V_f and output voltage V_o is called the feedback factor β. It can be expressed as $\beta = \frac{V_f}{V_O}$

10. An amplifier has a voltage gain of 200. The gain is reduced to 50 when negative feedback is applied. Determine feedback factor and express the amount of feedback in dB. [WBUT-2004] [WBUT 2010]

    Solution

    Given: $A = 200$, $A_f = 50$

    The closed-loop gain of a feedback amplifier is

$$A_f = \frac{A}{1 + \beta . A}$$

    or,
$$50 = \frac{200}{1 + 200\beta}$$

    Therefore,
$$\beta = \frac{3}{200} = 0.15$$

    The amount of feedback $= \frac{A_f}{A} = \frac{50}{200} = \frac{1}{4}$

    The amount of feedback in dB $= 20 \log_{10} \left(\frac{A_f}{A} \right) = 20 \log_{10} \left(\frac{1}{4} \right)$

    $= -20 \log_{10} 4$ dB $= -12.0411$ dB

11. Explain how stability of gain improves by negative feedback. [WBUT-2004]

    Solution Refer Section 2.7.4.

12. (a) Draw the circuit diagram of an emitter follower and explain the nature of feedback in this circuit.
    (b) What is its feedback topology? [WBUT-2004]

    Solution (a) Refer Section 2.9.2

    (b) Voltage series feedback or series parallel or series shunt topology

13. What is the effect of negative feedback on input and output impedance of an amplifier? [WBUT-2004]

Solution

Due to negative feedback, the input and output impedance of an amplifier is changed by a factor $(1 + \beta A)$. The input impedance is increased by a factor $(1 + \beta A)$ and the output impedance is reduced by a factor $(1 + \beta A)$. The input impedance is $Z_{if} = (1 + \beta A)Z_i$

The output impedance is $Z_{of} = \dfrac{Z_o}{1+\beta A}$ where A is amplifier gain and β is feedback factor.

14. Identify the circuit shown. In the circuit the value of $R_1 = 2\text{k}\Omega$, $R_f = 4\text{k}\Omega$, determine the output voltage, input resistance and input current for an input voltage of 2V. [WBUT-2004]

Figure 2.57 shows the voltage shunt feedback amplifier.

The gain of amplifier is $A_f = \dfrac{V_o}{V_{in}} = -\dfrac{R_f}{R_1}$

$$= -\frac{4}{2} = -2$$

The output voltage $V_o = -\dfrac{R_f}{R_1} V_{in} = -2 \times 2 = -4\text{V}$

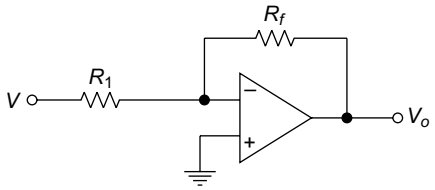


Fig. 2.57 ***Voltage shunt feedback amplifier***

The input resistance $R_i = R_1 = 2\text{k}\Omega$

Assume input current is I_{in}

The output voltage $V_o = -I_{in}R_f$

Then input current is $I_{in} = -\dfrac{V_o}{R_f} = -\dfrac{-4}{4 \times 10^3} = 1$ mA

15. (a) What do you mean by –ve feedback? (b)Why is it used in designing an amplifier? [WBUT-2005]

Solution (a) Refer Section 2.2.

(b) The negative feedback is used in designing an amplifier as it helps to

- Increase bandwidth
- Decrease distortion
- Stabilize the gain
- Decrease noise

- Reduction in frequency distortion
- Reduce phase distortion

16. The variation of open loop gain of an amplifier having internal gain 1000 is 10% but for a specific use only 1% gain variation is allowed. Design a feedback amplifier for this purpose and find the corresponding feedback fraction and overall gain. [WBUT-2005]

Solution

In a feedback amplifier

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1+\beta A|}\left|\frac{dA}{A}\right|$$

where A_f = closed loop gain, A = open loop gain and β = feed back ratio

Given: $\frac{dA_f}{A_f} = 1\% = \frac{1}{100}$ and $\frac{dA}{A} = 10\% = \frac{10}{100}$

Therefore, $\frac{1}{100} = \frac{10}{100}\frac{1}{1+\beta A}$

or, $\beta A = 9$

As $\beta A > 1$ negative feedback to be applied.

The feedback fraction is $\beta = \frac{9}{A} = \frac{9}{1000} = 0.009$ as $A = 1000$

The overall gain is

$$A_f = \frac{A}{1+\beta.A} = \frac{1000}{1+(0.009\times 1000)} = 100$$

17. Compare between voltage and current feedback mechanism. [WBUT-2005] [WBUT-2007]

Solution (a) Refer Table 2.1.

18. (a) Mention the advantage and disadvantage of a negative (–ve) feedback amplifier. [WBUT-2007]
    (b) Determine the gain bandwidth product negative (–ve) feedback amplifier.
    (c) An amplifier with negative (–ve) feedback provides an output voltage of 5 V with an input voltage of 0.2. On removal of feedback it needs only 0.1 V input voltage to give the same output. Find out the
        (i) Gain without feedback
        (ii) Gain with feedback
        (ii) Feedback ratio.

Solution

(a) The *advantages* of negative feedback amplifiers are given below:
- Increased stability in the amplification. The gain is less dependent on device parameters
- Higher input impedance
- Lower output impedance

- Feedback reduces distortion in the amplifier
- Bandwidth of the amplifier is increased. Improved frequency response
- Linear operation over a wide range

The *disadvantages* of feedback amplifiers are

- The feedback amplifier may lead to instability if it is not designed properly
- Gain of the amplifier decreases
- Input and output impedances of feedback amplifier are sensitive with open loop gain of amplifier, and parameter variations.

(b) Assume A_f = closed-loop gain, A = open loop gain and β = feed back ratio

The overall gain is $A_f = \dfrac{A}{1+\beta.A}$

The bandwidth without feedback = BW

The bandwidth with feedback = BW_f

The relation between BW and BW_f can be expressed as

$$BW_f = (1 + \beta A)BW$$

The gain bandwidth product can be expressed as

$$A_f \times BW_f = \frac{A}{1+\beta A} \times (1+\beta A)BW = A \times BW$$

(c) Output voltage V_o = 5 V and input voltage V_i = 0.2 V with feedback. Without feedback input voltage V_i = 0.1 V

(i) The gain without feedback is $A_f = \dfrac{V_o}{V_i} = \dfrac{5}{0.1} = 50$

(ii) The gain with feedback is $A_f = \dfrac{V_o}{V_i} = \dfrac{5}{0.2} = 25$

(iii) The overall gain is $A_f = \dfrac{A}{1+\beta.A}$

where A_f = closed loop gain, A = open loop gain and β = feed back ratio

Therefore, $25 = \dfrac{50}{1+\beta \times 50}$ and $\beta = \dfrac{1}{50}$

19. In a CC amplifier circuit R_1 = 10 kΩ, R_2 = 10 kΩ. R_e = 5 kΩ, R_s = 1 kΩ. Determine the circuit Input and output impedance, voltage and current and power gain if the transistor parameters are h_{ie} = 2kΩ, h_{fe} = 100.

[WBUT-2007]

Solution

The current gain of common collector amplifier is

$$A_I = 1 + h_{fe} = 1 + 100 = 101$$

The input impedance is

$$R_i = h_{ie} + (1 + h_{fe})R_e$$
$$= 200 + (1 + 100)\ 500 = 507\ \text{k}\Omega$$

The output impedance is

$$R_o = \frac{h_{ie} + R_s}{1 + h_{fe}} = \frac{2000 + 1000}{1 + 100} = 29.70\ \Omega$$

The voltage gain is

$$A_V = 1 - \frac{h_{ie}}{R_i} = 1 - \frac{2000}{507 \times 10^3} = 0.996$$

Power gain = current gain × voltage gain

$$A_P = A_I \times A_V = 101 \times 0.996 = 100.596$$

20. How does the negative feedback increase the bandwidth of the amplifier? [WBUT-2007]

Solution (a) Refer Section 2.7.3.

21. The open loop gain of an amplifier is 100. What will be the overall gain when a negative feedback of 0.6 is applied to the amplifier? [WBUT-2008]

Solution

Assume A_f = closed loop gain, A = open loop gain and β = feed back ratio

The overall gain is $A_f = \frac{A}{1 + \beta.A}$

Given $A = 100, \quad \beta = 0.6$

Then $A_f = \frac{A}{1 + \beta.A} = \frac{100}{1 + (0.6 \times 100)} = \frac{100}{61} = 1.6393$

22. (a) Draw the *h*-parameter equivalent circuit of a CE transistor amplifier and hence obtain the expressions for the (i) current gain (b) voltage gain (iii) input impedance.

(b) For a CE amplifier $h_{ie} = 2\ \text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 20 \times 10^{-6}$ mho. If the load resistance is 4 kΩ and source resistance is 200 Ω, determine the input impedance, voltage and current gains. [WBUT-2008]

Solution

(a) Solution of Question No. 2

(b) Given: $h_{ie} = 2\text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 20 \times 10^{-6}$ mho, $R_L = 4\ \text{k}\Omega$ and $R_s = 200\ \Omega$

The current gain of CE amplifier is

$$A_I = \frac{h_{fe}}{1 + h_{oe}R_L} = \frac{50}{1 + (20 \times 10^{-6} \times 4 \times 10^3)} = 46.296$$

Input resistance is

$R_i = h_{ie} + h_{re} A_I R_L = 2000 + (2 \times 10^{-4} - 46.296 \times 4000) = 2037.0368$

The voltage gain is

$$A_V = A_I \frac{R_L}{R_i} = 46.296 \times \frac{4000}{200} = 925.92$$

23. (a) Formulate the expression for voltage gain, current gain and output resistance of a transistor amplifier employing *h*-parameters.
    (b) A transistor amplifier in CE configuration couples a source of internal resistance 1 kΩ to a load 20 kΩ. Find the input and the output resistance if h_{ie}=1 kΩ, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 150$ and $1/h_{oe} = 40$ kΩ [WBUT-2009]

Solution

(a) Refer Solution of Question No. 2

(b) Given: $h_{ie} = 1$ kΩ, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 150$ and $1/h_{oe} = 40$ kΩ, $R_L = 20$ kΩ and $R_s = 1$ kΩ

The current gain of CE amplifier is

$$A_I = \frac{h_{fe}}{1 + h_{oe} R_L} = \frac{150}{1 + (1/40 \times 10^3) \times 20 \times 10^3)} = 100$$

Input resistance is

$$R_i = h_{ie} + h_{re} A_I R_L = 1000 + (2.5 \times 10^{-4} \times 100 \times 20{,}000) = 1500\ \Omega$$

The voltage gain is

$$A_V = A_I \frac{R_L}{R_i} = 100 \times \frac{20,000}{1500} = 1333.33$$

Looking from collector emitter terminals output resistance is $R_o = \frac{1}{h_{oe}} \| R_L$

$= 40\ \text{k}\Omega \| 20\ \text{k}\Omega = 13.33\ \text{k}\Omega$

24. (a) What is a feedback amplifier.
    (b) Derive an expression for closed-loop gain of the amplifier with feedback.
    (c) State the assumptions made in your derivation.
    (d) Write the effect of negative feedback in an amplifier in terms of gain, bandwidth, input resistance and output resistance with respect to voltage series configuration. [WBUT-2009]

Solution

(a) Refer Section 2.2. (b) Refer Section 2.5.1.

(d) The effect of negative feedback in an amplifier in terms of gain, bandwidth, input resistance and output resistance with respect to voltage series configuration are given below:

Gain The overall amplifier gain is expressed as $A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}$

Therefore, the negative feedback reduces the amplifier gain by a factor $(1 + \beta A)$.

Bandwidth The bandwidth with feedback is $BW_f = f_{2f} - f_{1f}$
where, upper cut-off frequency $f_{2f} = f_2(1 + \beta A_o)$

lower cut-off frequency $f_{1f} = \dfrac{f_1}{1 + \beta A_o}$

Therefore, amplifier with negative feedback has larger bandwidth with respect to bandwidth without feedback.

Input Resistance This is increased by a factor $(1 + \beta A)$ and $R_{if} = (1 + \beta A)$

Output Resistance The output resistance is decreased by a factor $(1 + \beta A)$ and $R_{of} = \dfrac{R_o}{1 + \beta A}$

25. (a) What are the advantages of negative feedback?
    (b) Explain with proper diagram the configuration of current series and current shunt feedback circuit. [WBUT-2009]

Solution

(a) Refer Section 2.1. (b) Refer Sectios 2.5.3 and 2.5.4.

3 OSCILLATORS

3.1 INTRODUCTION

An oscillator is an electronic circuit that generates a repetitive electronic signal or periodic wav eforms from a few hertz (Hz) to several gigahertzes (GHz). In the field of electronics, an oscillator is known as a wave generator. Wave generators use many different circuits and produce output signals such as sinusoidal, square, rectangular, sawtooth and trapezoidal wave shapes. These wave shapes serve different useful purposes in the electronic circuits.

Usually, oscillators use some form of active devices, crystal surrounded by passive devices such as resistors, capacitors and inductors to generate the output signals. For example, oscillators are extensively used in a television receiver to reproduce both sound and picture. The other example is that clock signals generated by oscillators regulate computers and quartz-clocks. A low-frequency oscillator generates an ac waveform at a frequency below 20 Hz. These low-frequency oscillators are typically used in audio synthesizers.

In this chapter, classification of oscillators, oscillator operation, Barkhausen criteria, sinusoidal oscillators, relaxation oscillators are discussed elaborately.

3.2 CLASSIFICATION OF OSCILLATORS

Oscillators can be classified depending upon the following parameters as given below:

(i) The wave shapes generated by the oscillators
(ii) The fundamental mechanisms used in oscillators
(iii) Range of frequency of output signal
(iv) Type of circuit (based on passive devices used in oscillators)

3.2.1 According to the Wave Shapes Generated by the Oscillators

Generally, oscillators are classified into two broad categories according to wave shapes such as

- Sinusoidal oscillators
- Non-sinusoidal or relaxation oscillators

(a) Sinusoidal Oscillators A sinusoidal oscillator generates a sine-wave output signal. Ideally, the output signal has constant amplitude with fixed frequency. But something less than this is usually obtained from oscillators. The accuracy of oscillators depends on the class of amplifier used, amplifier characteristics, frequency stability and amplitude stability.

A sine-wave generator produces sine-wave signals from audio frequency to ultra high radio frequency as well as microwave frequency. Low-frequency sine-wave oscillators use resistors (R) and capacitors (C) to form a frequency-determining network. These oscillators are known as RC oscillator and are widely used in the audio frequency range.

Some sine-wave oscillators use inductors (L) and capacitors (C) for their frequency determining network. These types of oscillators are called as LC oscillators. This oscillator is also known as tank circuit. LC oscillators are commonly used in high audio frequency range.

The third type of sine-wave generators is the crystal oscillators. This oscillator provides excellent frequency stability and used in mid-audio frequency range.

(b) Non-sinusoidal Oscillators The non-sinusoidal oscillator generates non-sinusoidal or complex waveforms such as square, rectangular, sawtooth and trapezoidal. As oscillator outputs are generally characterized by a sudden change or relaxation, these oscillators are called *relaxation oscillators*. Usually, the oscillators signal frequency is governed by the charge or discharge time of a capacitor in series with a resistor. Sometimes inductors are also used in oscillator's circuit. Hence, both RC and LC networks are used for determining the frequency of oscillation. The examples of non-sinusoidal oscillators are multivibrators, sawtooth generators and trapezoidal waveform generators.

3.2.2 According to the Fundamental Mechanisms Used in Oscillators

Oscillators can also be classified according to the fundamental mechanisms used in oscillators. Types of oscillators are

- Feedback oscillators
- Negative resistance oscillators

(a) Feedback Oscillators In these oscillators, positive feedback is used in feedback amplifier and Barkhausen criteria must be satisfied.

(b) Negative Resistance Oscillators In negative resistance oscillators, the amplifying device has negative resistance to neutralize the positive resistance of oscillators.

3.2.3 According to the Range of Frequency of Output Signal

Oscillators can be classified according to the frequency of output signal generated by oscillators. Usually, oscillators produce signals in the audio frequency (AF)

range and radio frequency range, and they are known as Audio Frequency Oscillators (AFO) and Radio Frequency Oscillators (RFO) respectively. Table 3.1 shows the different types of oscillators according to range of frequency.

Table 3.1 *Types of oscillators according to range of frequency*

Types of oscillators	*Frequency range*	*Example*
Audio Frequency Oscillators (AFO)	400 Hz to 20 kHz	*RC* oscillators such as phase-shift and Wien-bridge oscillators
Radio Frequency Oscillators (RFO)	20 kHz to 30 MHz	*LC* feedback oscillators such as tuned collector, Hartley and Colpitt oscillators
Very High Frequency (VHF) oscillators	30 MHz to 300 MHz	Crystal oscillators used in microprocessors, microcontrollers, ASICs, DSP processors and computer mother-boards
Ultra High Frequency (UHF) oscillators	300 MHz to 3 GHz	Bulk Acoustic Wave (BAW) AT cut quartz crystal oscillators
Microwave frequency oscillators	Above 3 GHz	YIG tuned oscillators, oven controlled crystal oscillators

3.2.4 According to the Type of Circuit (Based on Passive Devices Used in Oscillators)

The oscillators can also be classified according to the type of circuit as given below:

- *LC* tuned oscillators
- *RC* phase shift oscillators

3.3 THE BASIC OSCILLATOR

Figure 3.1 shows the basic oscillator block diagram. An oscillator can be regarded as an amplifier which provides its own input signal. It is clear from the block diagram that amplification of signal power occurs from input to output. In any oscillator circuit, a portion of the output is fed back to the input. Enough power

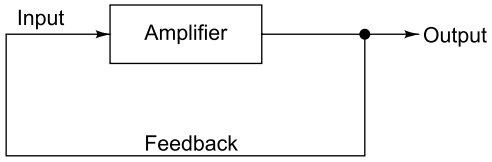


Fig. 3.1 *Block diagram of a basic oscillator*

must be fed back to the input for the oscillator to drive itself as a signal generator. Therefore, the oscillator must be self-driven and the feedback signal must be positive or regenerative.

As a practical oscillator generates signals at a predetermined frequency, a Frequency Determining Network (FDN) is required. The FDN acts as a filter which allows only the desired frequency to pass. The basic oscillator requirements, in addition to the application, determine the type of oscillator to be used. For any oscillator circuit, the following requirements must be fulfilled:

(i) Amplification is required to give necessary gain for the output signal.
(ii) There should be sufficient regenerative feedback to sustain oscillations.
(iii) A Frequency Determining Network (FDN) is required to maintain the desired output frequency.
(iv) Any oscillator has two types of stability such as amplitude stability and frequency stability. The amplitude stability refers to the ability of the oscillator to maintain constant amplitude of the output signal. Similarly, frequency stability refers to the ability of the oscillator to maintain constant frequency.
(v) Due to change in temperature and humidity, the value of capacitors, resistors and transistors can change. The changes in these components cause changes in amplitude and frequency. But change in amplitude and frequency must be minimum.
(vi) For proper use of oscillators, output power is also another consideration. Sometimes high power is obtained at some sacrifice to stability. Generally, stable oscillators will be followed by a higher-power buffer amplifier. The buffer is used to provide isolation between oscillator and load. So that changes in the load do not affect the oscillators.
(vii) Usually, oscillators use class C amplifier to increase efficiency. Some oscillators use class A amplifiers where high efficiency is not required but distortion must be minimum.

3.4 OSCILLATOR OPERATION

Figure 3.2 shows the negative feedback circuit. Assume the input voltage and output voltage are vector quantity and gains are also complex numbers. In this circuit,

$\overline{V_o}$ = output voltage

$\overline{V_s}$ = supply voltage

$\overline{A}$ = gain of main amplifier

$\overline{\beta}$ = feedback gain

The overall gain of the amplifier circuit is

$$\overline{A}_f = \frac{\overline{V}_o}{\overline{V}_s} = \frac{\overline{A}}{1+\overline{\beta}\,\overline{A}}$$

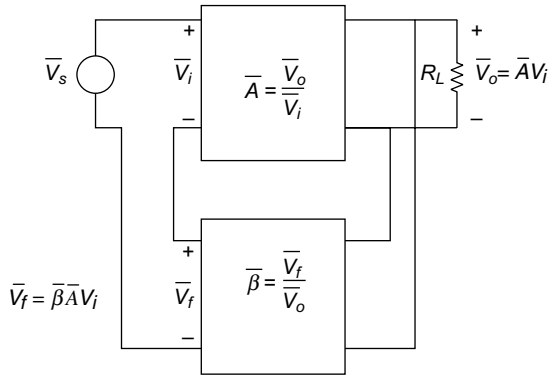


Fig. 3.2 ***Block diagram of a negative feedback amplifier***

At a particular frequency, the phase shift of $\bar{\beta}\bar{A}$ is 180° and polarity of the feedback voltage $\bar{V}_f$ is reversed. Therefore, the feedback is positive and overall gain becomes

$$\bar{A}_f = \frac{\bar{V}_o}{\bar{V}_s} = \frac{\bar{A}}{1 - \bar{\beta}\bar{A}}$$

When $\left|\bar{\beta}\bar{A}\right| < 2$, the gain of the amplifier must be larger than $\left|\bar{A}\right|$. If $\left|\bar{\beta}\bar{A}\right| = 1$ and $\angle\bar{\beta}\bar{A} = 180°$, the overall gain becomes infinite. It means that the input $\bar{V}_s$ is to be zero to produce any output voltage $\bar{V}_o$. Therefore, when the signal $\bar{V}_s$ is removed from Fig. 3.2, the circuit as shown in Fig. 3.3 can oscillates at a particular frequency determined by frequency determining network (FDN). Consequently, in a negative feedback circuit the condition for oscillation is $\left|\bar{\beta}\bar{A}\right| = 1$ and $\angle\bar{\beta}\bar{A} = 180°$ or $\bar{\beta}\bar{A} = -1$. This condition is called the Barkhausen criteria for oscillation.

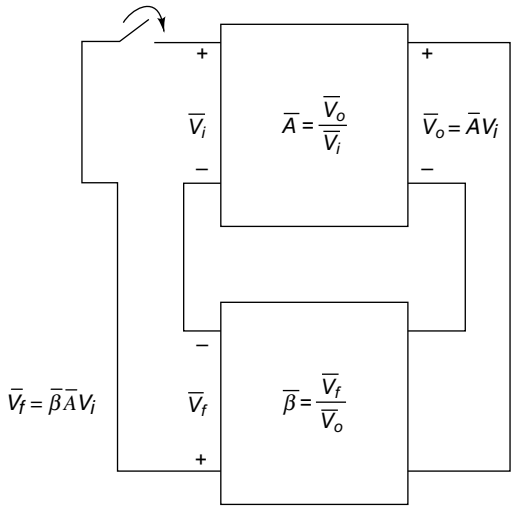


Fig. 3.3 ***Feedback circuit used as oscillator***

To satisfy the Barkhausen criteria, the magnitude of the loop gain is unity with a corresponding phase shift of 180° in a negative feedback circuit. An equivalent expression using complex algebra is $\overline{\beta}\overline{A} = 1 \angle -180°$ for a negative feedback system. In reality, there is no requirement of input signal to start oscillator. But the condition $\left|\overline{\beta}\overline{A}\right| = 1$ will be satisfied only for self-sustained oscillators. Practically, $\left|\overline{\beta}\overline{A}\right|$ is made greater than 1 and the feedback circuit is started oscillating by amplifying noise voltage which is always present in the system. The saturation factors of the feedback circuit provide an average $\left|\overline{\beta}\overline{A}\right|$ which is about 1. Hence, the output waveforms of oscillators are not exactly sinusoidal; and it will be non-sinusoidal in nature.

As the phase shift approaches 180° and $\left|\overline{\beta}\overline{A}\right| = 1$ in a negative feedback circuit, the output voltage of the system tends to infinity, but it is limited to finite value due to an energy-limited power supply. When the output voltage approaches power rail $+V_{CC}$ or $-V_{CC}$, the gains of active devices in the amplifiers are changed. The value of A changes and forces βA away from the singularity. Figure 3.4 shows the build up of oscillations starting from initial noise. Ideally, the trajectory of output voltage will be toward an infinite voltage, but practically the following things can occur:

(i) Nonlinearity in saturation causes the system to become stable.
(ii) The initial change causes the system to saturate and stay that way for a long time before it becomes linear. This produce highly distorted oscillations called as relaxation oscillators.
(ii) The feedback amplifier circuit stays linear and reverse direction heading for the opposite power rail. This condition provides a sine-wave oscillator.

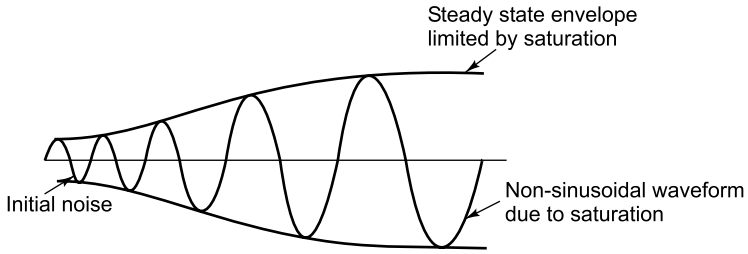


Fig. 3.4 ***The build-up of oscillations***

3.4.1 Barkhausen Criterion (See page II.3.44)

Generally, the amplifier gain A and feedback path gain β are complex quantity and function of frequency. Consequently, βA is also a complex quantity and function of frequency. When $|1 - \beta A| < 1$ in a positive feedback amplifier, the amplifier acts as an oscillator. Any feedback amplifier will be stable, when transient disturbance produces a response, but the amplitude of response must decay with time. The feedback system becomes unstable if any transient disturbance persists indefinitely and output response increases with time, but amplitude of output response is limited by nonlinearity of the circuit parameters. The stability of amplifier can be investigated using the Nyquist criterion.

The gain and phase shift of a feedback amplifier are plotted on a complex plane. As βA is also a complex quantity and function of frequency, different points on the complex plane can be obtained corresponding to different values of frequency. When frequency is varied from $+\infty$ to $-\infty$, a closed curve is formed by the locus of $(1 - \beta A)$. This plot is known as Nyquist plot.

The locus of $|1 - \beta A|$ is a circle of unit radius with the centre at point $(1 + j0)$. The locus of βA on the complex plane is $A_1 - A_2$, while frequency is varied. At a specified frequency f_o, the point on the locus $A_1 - A_2$ is P. If P is inside the circle of unit radius with the centre at point $(1 + j0)$, $|1 - \beta A| < 1$ and feedback is positive as shown in Fig. 3.6. If P is outside the circle, $|1 - \beta A| > 1$ and feedback is negative as depicted in Fig. 3.5. When P is located at the point $(1 + j0)$, the overall gain A_f is infinite and amplifier works as an oscillator. Consequently, Nyquist criterion states that the locus of βA passes through or enclose the circle of unit radius with the centre at point $(1 + j0)$, the amplifier is unstable and will oscillate. When the locus of βA does not pass through or does not enclose the circle of unit radius with the centre at point $(1 + j0)$, the amplifier is stable. Therefore, a positive feedback amplifier acts as an oscillator when Nyquist criterion is satisfied only.

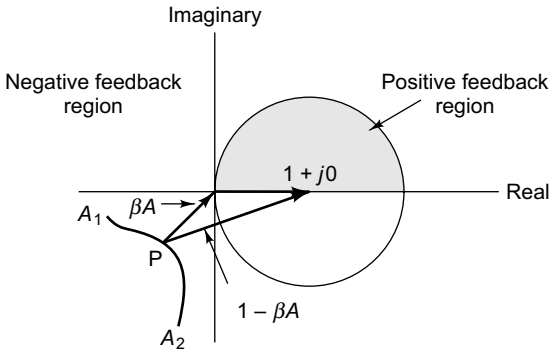


Fig. 3.5 *Negative feedback amplifier*

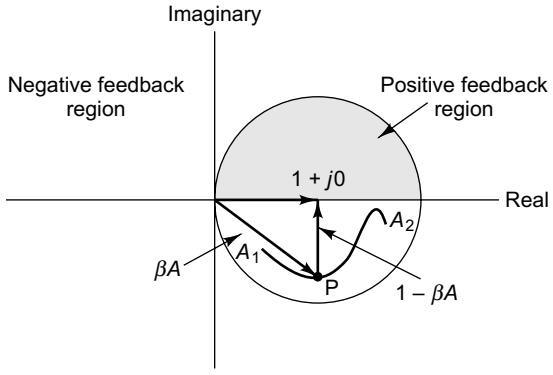


Fig. 3.6 *Positive feedback amplifier*

3.5 PHASE SHIFT IN OSCILLATION

The phase shift of $\beta A = 1\angle - 180°$ is introduced by active and passive components. In any well-designed feedback circuit, oscillators are made dependent on only the passive component phase shift as it is most accurate. The phase shift contributed by active components is minimized as it changes with temperature and is device dependent. So that amplifiers are selected in such a way that they contribute very little or no-phase shift at the oscillator.

A single-pole *RC* circuit contributes up to 90° phase shift per pole. To get 180° phase shift in any oscillators, at least two poles must be used in oscillator design. Figure 3.7 shows that two cascaded *RC* circuits provide 180° phase shift. The value of $\frac{d\phi}{d\omega}$ at the oscillator frequency is unacceptably small. Therefore, oscillators made with two cascaded *RC* circuits, have poor frequency stability. When three equal *RC* circuits are cascaded, the circuit has much higher $\frac{d\phi}{d\omega}$.

As a result, oscillator has improved frequency stability. The three section oscillators yield three sine waves 60° phase shift relative to each other. If another *RC* circuit is added or four equal cascaded *RC* circuits produces an oscillator with an excellent $\frac{d\phi}{d\omega}$. Hence this circuit is the most stable oscillator yields four sine waves 45° phase shift relative to each other.

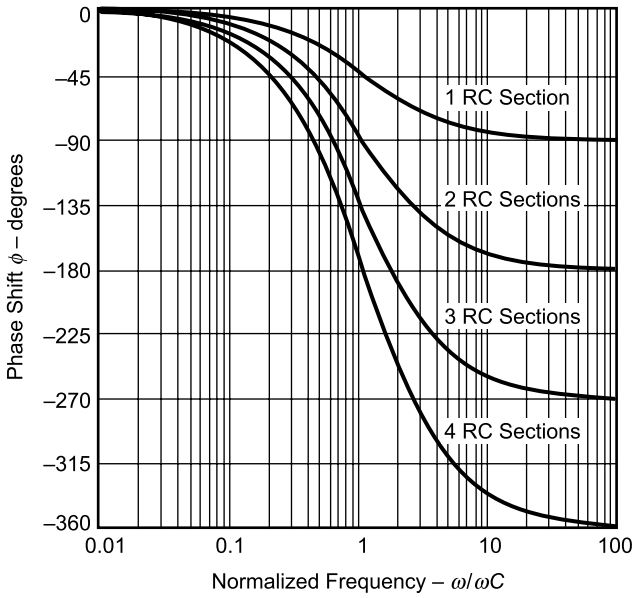


Fig. 3.7 ***Phase plot of RC sections***

An *LC* circuit has two poles and it can contribute up to 180° phase shift per pole pair. But *LC* oscillators are not very useful at low frequency operation as low frequency inductors are very expensive, heavy, and bulky. Usually, *LC*

oscillators are designed in high-frequency application, beyond the frequency range of voltage feedback OPAMPs. Multiple *RC* circuits are used in low-frequency oscillators.

3.6 PHASE SHIFT OSCILLATOR

Figure 3.8 shows a phase shift oscillator circuit. The phase shift in feedback path of an amplifier can be provided by an *RC* network. The *RC* sections are cascaded to get steep slope $\frac{d\phi}{d\omega}$ required for a stable oscillator frequency. The phase shifts of *RC* sections are independent of each other and βA will be equal to $\beta A = A\left(\frac{1}{1+sRC}\right)^3$.

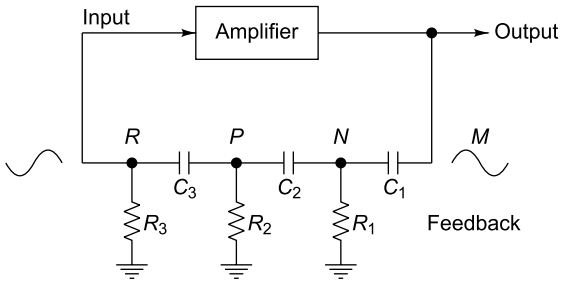


Fig. 3.8 ***Amplifier with an RC feedback network***

Figure 3.9 shows the vector diagram of *RC* feedback network. The signal at *M* is 180 degree out of phase with the signal input at *R*. To produce regenerative feedback, the *RC* network must provide a 180° phase shift of the signal. When power is applied to the circuit, a noise voltage will appear at *M*. This noise signal couples through C_1 and across R_1, a phase shift occurs. The voltage across R_1 is VR_1 has been shifted in phase about 60° and reduced in amplitude. The signal at the point *N* is coupled to the next *RC* section (R_2 and C_2). As resistance and capacitor size are same as before, there will be another 60° phase shift. The signal at point *P* is the voltage across R_2 represented by VR_2 which has been shifted about 120° and its magnitude is reduced further. The same type of operation takes place at last *RC* section (R_3 and C_3). There will be another 60° phase shift and has further amplitude reduction. Hence the signal at point *R*, VR_3 has been shifted 180°.

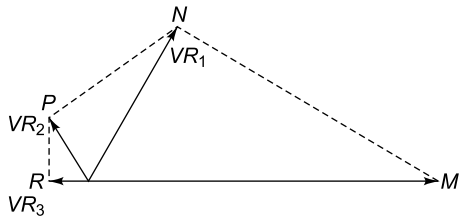


Fig. 3.9 ***Vector diagram of RC feedback network***

The loop phase shift is –180° when phase shift of each section is –60°. The 60° phase shift occurs when $\omega = 2\pi f = \dfrac{1.732}{RC}$ as $\tan 60° = 1.732$.

Assume the current I flows through C and R, the voltage across capacitor C is V_C which will be 90° lagging from the current I. The voltages across the resistance R is V_R which will be in phase with the current I. As a result, the voltage V has a phase shift of θ angle with respect to current.

Figure 3.10(b) shows the vector diagram of an RC section.

From Fig. 3.10(b), we can write

$$\tan\theta = \frac{V_C}{V_R} = \frac{IX_C}{IR} = \frac{1}{2\pi fRC}$$

The frequency is equal to

$$f = \frac{1}{2\pi RC\tan\theta}$$

As $\theta = 60°$, $\tan\theta = \tan 60° = \sqrt{3}$

Then $$f = \frac{1}{2\pi RC\sqrt{3}}$$

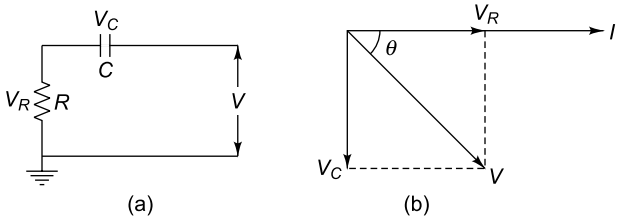


Fig. 3.10 ***RC section and its vector diagram***

The transfer function of the three RC networks is

$$\beta = \frac{V_f}{V_o} = \frac{1}{1 + \dfrac{6}{sRC} + \dfrac{5}{s^2R^2C^2} + \dfrac{1}{s^3R^3C^3}}$$

After substituting $s = j\omega = j2\pi f$ and $f_1 = \dfrac{1}{2\pi RC}$, we get

$$\beta = \frac{1}{1 - 5\left(\dfrac{f_1}{f}\right)^2 - j\left[6\left(\dfrac{f_1}{f}\right) - \left(\dfrac{f_1}{f}\right)^3\right]}$$

As $|\beta A| = 1$, β must be real. The imaginary term in the above equation must be zero.

$$6\left(\frac{f_1}{f}\right) - \left(\frac{f_1}{f}\right)^3 = 0$$

or, $$\frac{f_1}{f} = \sqrt{6}$$

The frequency of oscillator is

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

and the corresponding feedback gain is $\beta = \frac{1}{29}$

The above relation is only justified when each section of the *RC* the network does not affect other sections. But practically it is not possible due to device parameter variations.

As $|\beta A| = 1, |A| = \frac{1}{\beta} = 29$

So that the circuit will oscillate if $A = 29$.

3.1 In an *RC* phase shift oscillator, if the value of resistors are $R_1 = R_2 = R_3 = 100$ kΩ and the value of capacitors are $C_1 = C_2 = C_3 = 0.20$ nF. Determine the frequency of the oscillation.

Solution

Given $R_1 = R_2 = R_3 = 100$ kΩ and $C_1 = C_2 = C_3 = 0.20$ nF

The frequency of *RC* phase shift oscillator is

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$= \frac{1}{2\pi \times 100 \times 10^3 \times 0.20 \times 10^{-9}\sqrt{6}}$$

$$= 3.247 \text{ KHz}$$

3.7 BJT PHASE SHIFT OSCILLATOR

Figure 3.11 shows the BJT phase shift oscillator. The quiescent operating point of the transistor is determined by the resistances R_1, R_2, R_C, and R_E and supply voltage V_{CC}. The bypass capacitor C_E is connected in parallel with R_E and provides very small reactance at the low frequency signal. In this circuit, the transistor operates in common emitter configuration and it provides a 180° phase shift between input and output voltages. There are three *R-C* sections in the circuit and these three *R-C* sections provide another 180° phase shift. Hence the net phase shift around the loop is 0° or 360°. In this section the detail circuit analysis is explained.

3.7.1 Circuit Analysis of BJT Phase Shift Oscillator

Assume each *RC* section is identical. For this $C_1 = C_2 = C_3 = C$, $R_1 = R_2 = R$. As input impedance of transistor h_{ie} is connected in series with R', the effective resistance of last section is $R' = R - h_{ie}$. As R_1 and R_2 are very high, the effect on ac operation of the circuit is negligible. The parallel combination of R_E and C_E will be absent in the ac equivalent circuit of BJT oscillator. The equivalent

circuit of Fig. 3.11 is shown in Fig. 3.12. As h_{re} is very small, the value of $h_{re} V_2$ may be neglected. As $\frac{1}{h_{oe}} >> R_C$, we can also neglect $\frac{1}{h_{oe}}$. Then the equivalent circuit is modified as represented by Fig. 3.13. This circuit can be represented in most simplified form as shown in Fig. 3.14. There are three loops and loop currents are I_1, I_2 and I_3.

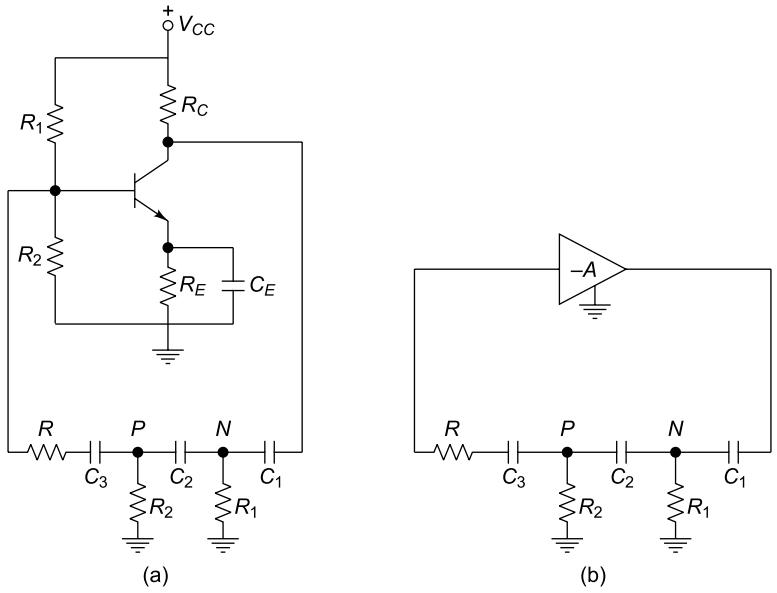


Fig. 3.11 *R-C phase shift oscillator using BJT*

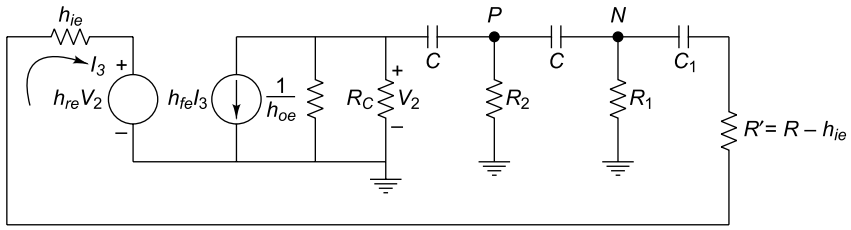


Fig. 3.12 *ac equivalent circuit of Fig. 3.11*

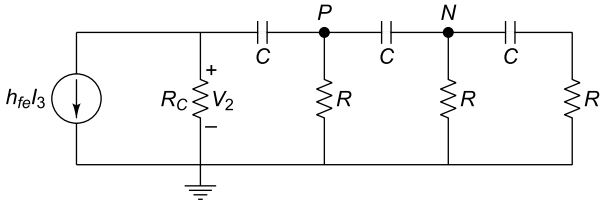


Fig. 3.13 *ac equivalent circuit of Fig. 3.11 when* h_{re} V_2 *and* $\frac{1}{h_{oe}}$ *are neglected*

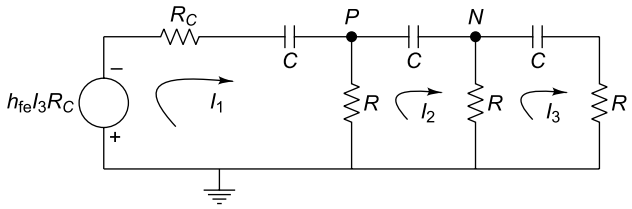


Fig. 3.14 ***Simplest ac equivalent circuit of Fig. 3.11***

KVL equation of loop-I is

$$\left(R_C + R - j\frac{1}{\omega C}\right)I_1 - RI_2 + h_{fe}R_C I_3 = 0$$

KVL equation of loop-II is

$$-RI_1 + \left(2R - j\frac{1}{\omega C}\right)I_2 - RI_3 = 0$$

KVL equation of loop-III is

$$-RI_2 + \left(2R - j\frac{1}{\omega C}\right)I_3 = 0$$

We can write the KVL equations in matrix form as given below:

$$\begin{bmatrix} R_C + R - j\frac{1}{\omega C} & -R & h_{fe}R_C \\ -R & 2R - j\frac{1}{\omega C} & -R \\ 0 & -R & 2R - j\frac{1}{\omega C} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = 0$$

As I_1, I_2, I_3 are non-zero quantities, the determinant of the coefficient of I_1, I_2 and I_3 must be zero.

Therefore, we can write the determinant of the matrix

$$\left(R_C + R - j\frac{1}{\omega C}\right)\left(3R^2 - j\frac{4R}{\omega C} - \frac{1}{\omega^2 C^2}\right) - R^2\left(2R - j\frac{1}{\omega C}\right) + h_{fe}R_C R^2 = 0 \quad (3.1)$$

The above equation has real and imaginary parts. For oscillation, the imaginary part must be zero as well as real part will also be zero.

The imaginary part is equal to

$$-4R\frac{R + R_C}{\omega C} - \frac{1}{\omega C}\left(3R_2 - \frac{1}{\omega^2 C^2}\right) + \frac{R^2}{\omega C} = 0$$

Then we can find that

$$\omega^2 = \frac{1}{C^2(6R^2 + 4RR_C)}$$

or,
$$\omega = \frac{1}{RC\sqrt{6 + \frac{R_C}{R}}}$$

Therefore, the circuit analysis of the small-signal model yields the frequency of oscillation as

$$f = \frac{\omega}{2\pi} = \frac{1}{2\pi RC\sqrt{6+4\frac{R_C}{R}}}$$

If we assume $\frac{R_C}{R} = K$, the frequency of oscillation is

$$f = \frac{1}{2\pi RC\sqrt{6+4K}}$$

The real part of Eq. (3.1) is equal to

$$(R+R_C)\left(3R^2 - \frac{1}{\omega^2C^2}\right) - 2R^3 - \frac{4R}{\omega^2C^2} + h_{fe}R_C R^2 = 0$$

After substituting the value of ω^2 in the above equation, we obtain

$$h_{fe} = 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

When the loop gain is greater than unity, the current gain of BJT must be equal to h_{fe} which follows the condition

$$h_{fe} \geq 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

The greater-than sign (>) in the above equation compensates for parameter changes in the amplifier. The optimum value of K is about 2.7. For this, the minimum value of h_{fe} is required for transistor to work as an RC oscillator. h_{fe} must be greater than 44.5 for oscillation.

RC phase shift oscillators are widely used as signal source in the audio-frequency and the ultrasonic range. If any one of the three capacitors or three resistors is changed in value, the phase shift provided by the section of the network becomes different and oscillator frequency will be changed. Due to change in a single capacitor or resistor, the amplitude of the output signal also changes to some extent. While a large range of frequency is required, all capacitors must be varied simultaneously. Generally, the range of capacitance is 50 pF to 500 pF and the frequency of oscillation can be changed in the ratio 10:1. For higher range of frequency variation, the resistance value of different resistors will be changed by a factor of 10.

3.8 FET PHASE SHIFT OSCILLATOR

Figure 3.15 shows the circuit diagram of an FET phase shift oscillator. The load resistance is $R_L = R_D \,||\, r_d$ and the amplifier gain is $A = -g_m R_L$.

As amplifier gain is negative, the feedback is to be negative.

The frequency of oscillator is $f = \frac{1}{2\pi RC\sqrt{6}}$ and magnitude of phase shift network gain $\beta = \frac{1}{29}$. The phase shift of 180° causes, this feedback behaves as

positive. At very high frequency, the input capacitance of FET contributes loading effect and FET should have high gain at low frequency for oscillation.

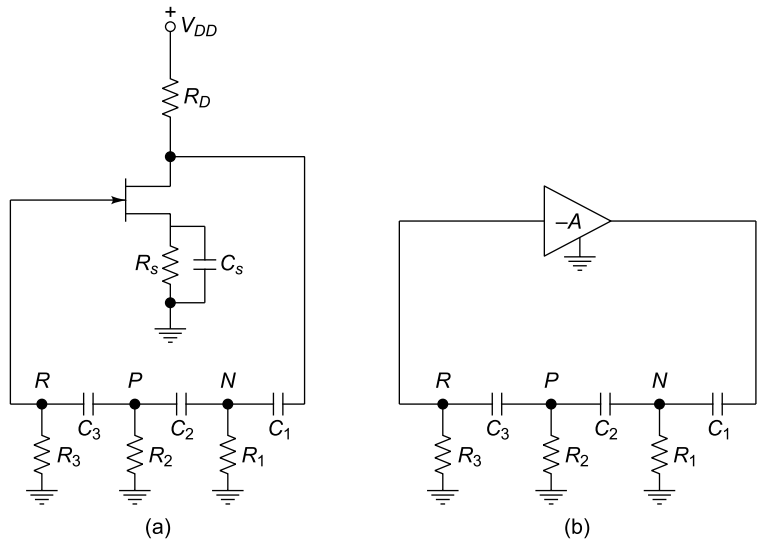


Fig. 3.15 ***RC phase shift oscillator using FET***

3.2 Find the frequency of oscillation in an *RC* phase shift oscillator as shown in Fig. 3.11. Assume R = 20 kΩ, C = 0.047 μF, R_C = 4.7 kΩ. Determine the minimum value of current gain for the oscillation.

Solution

Given R = 20 kΩ, C = 0.047 μF and R_C = 4.7 kΩ

The frequency of *RC* phase shift oscillator is

$$f = \frac{1}{2\pi RC\sqrt{6+4K}} \quad \text{where } \frac{R_C}{R} = K$$

$$K = \frac{R_C}{R} = \frac{4.7}{20} = 0.235$$

The frequency of the oscillation is

$$= \frac{1}{2\pi \times 20 \times 10^3 \times 0.047 \times 10^{-6}\sqrt{6+4\times 0.235}}$$

$$= 64.26 \text{ Hz}$$

The minimum value of current gain for the oscillation is

$$h_{fe} = 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

$$= 23 + 29 \times \frac{20}{4.7} + 4 \times \frac{4.7}{20} = 147.34$$

3.3 Determine the value of capacitors and current gain of the transistor when the frequency of oscillation in an *RC* phase shift oscillator is 20 kHz. Assume $R_1 = R_2 = R_3 = R$ = 100 kΩ, R_C = 5.6 kΩ.

Solution

Given f = 20 kHz, $R_1 = R_2 = R_3 = R$ = 100 kΩ, and R_C = 5.6 kΩ

The frequency of RC phase shift oscillator is

$$f = \frac{1}{2\pi RC\sqrt{6+4K}} \quad \text{where,} \quad \frac{R_C}{R} = K,$$

$$K = \frac{R_C}{R} = \frac{5.6}{100} = 0.056$$

The frequency of the oscillation is

$$20\times10^3 = \frac{1}{2\pi\times100\times10^3\times C\times\sqrt{6+4\times0.056}}$$

or,
$$C = \frac{1}{2\pi\times100\times10^3\times20\times10^3\times\sqrt{6+4\times0.056}}$$

$$= 0.03189 \text{ nF}$$

The minimum value of current gain for the oscillation is

$$h_{fe} = 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

$$= 23 + 29\frac{100}{5.6} + 4\frac{5.6}{100} = 541$$

3.9 WEIN BRIDGE OSCILLATOR

Figure 3.16 shows Wein bridge oscillator using OP-AMP and RC bridge circuit. The output voltage of the operational amplifier (OP-AMP), V_o is used as the input voltage of the bridge. The output voltage of the bridge V_i can be used as the input voltage of the amplifier. When bridge is in balanced condition, $V_i = 0$. But to sustain oscillation, V_i will not be zero ($V_i \neq 0$). Therefore, the bridge will be in slightly unbalanced condition by varying the ratio between the resistances R_3 and R_4. As the Wein bridge does not provide any phase shift between input and output voltages of bridge circuit, the operational amplifier must not introduce any phase shift between input and output voltages of amplifier and the overall phase shift around the loop is zero.

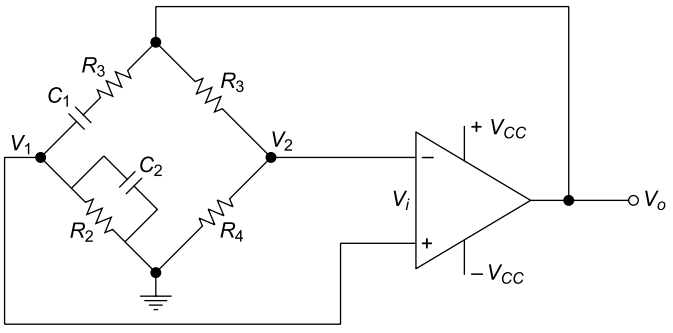


Fig. 3.16 *Wien-bridge oscillator*

3.9.1 Analysis of Wien-bridge Oscillator

The oscillator frequency is determined by R and C. Resistors R_1 and R_2 and capacitors C_1 and C_2 are used as frequency adjustment elements of Wein bridge oscillator. R_3 and R_4 are used as part of the feedback path of the amplifier circuit. The transfer function of the circuit has been derived using the following method as given below:

The impedances of four arms of the Wein bridge are Z_1, Z_2, Z_3 and Z_4.

Impedance Z_1 is the series connection of R_1 and C_1 and it is equal to

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{sR_1C_1 + 1}{sC_1} = \frac{1 + j\omega R_1C_1}{j\omega C_1} \quad \text{as } s = j\omega$$

Impedance Z_2 is the parallel combination of R_2 and C_2 and $Z_2 = R_2 \parallel \frac{1}{sC_2}$.

Therefore,

$$\frac{1}{Z_2} = \frac{1}{R_2} + sC_2$$

$$= \frac{1 + sR_2C_2}{R_2}$$

Then $Z_2 = \dfrac{R_2}{1 + sR_2 + C_2} = \dfrac{R_2}{1 + j\omega R_2C_2}$ as $s = j\omega$

The other two impedances are

$Z_3 = R_3$ and $Z_4 = R_4$

The frequency of oscillation can be determined from bridge balance condition. For the bridge balance condition, the phase angle of Z_1 and Z_2 will be same and oscillation frequency f_o can be obtained at this condition.

The bridge will be balanced, when $Z_1 R_4 = Z_2 R_3$ or $\dfrac{Z_1}{Z_2} = \dfrac{R_3}{R_4}$

Therefore, $$\frac{\dfrac{1 + j\omega R_1C_1}{j\omega C_1}}{\dfrac{R_2}{1 + j\omega R_2C_2}} = \frac{R_3}{R_4}$$

or, $$\frac{(1 + j\omega R_1C_1)(1 + j\omega R_2C_2)}{j\omega R_2C_1} = \frac{R_3}{R_4}$$

When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the above equation can be written as

or, $$\frac{(1 + j\omega RC)(1 + j\omega RC)}{j\omega RC} = \frac{R_3}{R_4}$$

or, $$2 - j\frac{(1 - \omega^2R^2C^2)}{\omega RC} = \frac{R_3}{R_4}$$

The condition for oscillation is that the real and imaginary parts on the both sides must be equal.

Therefore, $\frac{R_3}{R_4} = 2$ and $1 - \omega^2 R^2 C^2 = 0$

Hence we can also write the condition for oscillation as

$$\frac{Z_1}{Z_2} = \frac{R_3}{R_4} = 2$$

For oscillation, $Z_1 = 2Z_2$

or, $$\frac{1 + j\omega R_1 C_1}{j\omega C_1} = 2\frac{R_2}{1 + j\omega R_2 C_2}$$

or, $$(1 - \omega^2 R_1 C_1 R_2 C_2) = 0$$

Assume $R_1 = R_2 = R$ and $C_1 = C_2 = C$

Then $$(1 - \omega^2 R^2 C^2) = 0$$

or, $$\omega = \frac{1}{RC}$$

or $$2\pi f = \frac{1}{RC}$$

The frequency of oscillation is $f = \frac{1}{2\pi RC}$

At the balance condition of Wein bridge, the voltage across the two arms of the bridge must be equal.

Therefore, $$V_1 = V_2 = \frac{R_4}{R_3 + R_4} V_o$$

As $$\frac{R_3}{R_4} = 2, \ \frac{R_4}{R_3 + R_4} = \frac{1}{3} \text{ and } V_1 = V_2 = \frac{1}{3} V_o$$

At balanced condition, we get,

$$\frac{V_1}{V_o} = \frac{V_2}{V_o} = \frac{1}{3}$$

At oscillation, the input voltage of the amplifier is not equal to zero ($V_i \neq 0$) and the ratio $\frac{R_4}{R_3 + R_4}$ will be less than $\frac{1}{3}$. Then we can write

$$\frac{R_4}{R_3 + R_4} = \frac{1}{3} - \frac{1}{\delta}$$

where δ is the real number which is greater than 3. The bridge is slightly unbalanced and provides a feedback voltage, V_i.

The ratio $\frac{V_i}{V_o}$ remains at $\frac{1}{3}$ and the ratio $\frac{V_2}{V_o}$ is

$$\frac{V_2}{V_o} = \frac{1}{3} - \frac{1}{\delta}$$

Then input voltage of feedback amplifier is

$$V_i = V_1 - V_2 = \frac{1}{3}V_o - \left(\frac{1}{3} - \frac{1}{\delta}\right)V_o = \frac{V_o}{\delta}$$

The feedback factor is $\beta = \frac{V_i}{V_o} = \frac{1}{\delta}$

The condition of oscillation is $\beta A = 1$. Then, $\frac{A}{\delta} = 1$. For oscillation, $A = \delta > 3$.

Advantages of Wein Bridge Oscillator

The advantages of Wein bridge oscillator are as follows:

(i) As two stage amplifiers is used, the overall gain is very high.
(ii) The output waveforms will be pure sine waves.
(iii) The frequency stability is very good. Actually, oscillation frequency depends on R and C, since the values of R and C are fixed against temperature variations, frequency stability can be achieved.
(iv) The frequency of oscillation can be changed easily by varying R and C.
(v) When the resistance R_4 is replaced by a thermistor with negative temperature coefficient, the amplitude of oscillation will be stabilized with parameter variations of transistors, aging effect of transistor and other circuit parameters. Due to negative temperature coefficient, R_4 decreases with increasing temperature. Therefore, feedback factor β decreases. As a result, the Wein bridge adjust itself in such a way that $\beta A = 1$.

Disadvantages of Wein Bridge Oscillator

The disadvantages of Wein bridge oscillator are as follows:

(i) Large numbers of components are required for a two-stage amplifier.
(ii) Wein-bridge oscillators are able to generate only Audio Frequency (AF) range sine wave.

3.4 In a Wein-bridge oscillator when the value of resistor R = 200 kΩ and the frequency of the oscillation is 20 kHz, determine the value of capacitor C.

Solution

Given R = 200 kΩ and f = 20 kHz

The frequency of the oscillation is

$$f = \frac{1}{2\pi RC}$$

The value of capacitor C at the frequency of oscillation is

$$C = \frac{1}{2\pi Rf} = \frac{1}{2\pi \times 200 \times 10^3 \times 20 \times 10^3} = 0.0397 \text{ nF}$$

3.5 In a Wein-bridge oscillator, the value of capacitors can be changed from 10 pF to 100 pF to generate sine wave output signals from 20 Hz to 20 kHz.

(a) Determine the resistances required to generate the output signals from 20 Hz to 20 kHz.
(b) If the gain of the amplifier is 5, what will be the ratio of the resistances in the other arms of the bridge?

Solution

Given capacitor range is 10 pF to 100 pF and frequency range is 20 Hz to 20 kHz.

(a) The frequency of the oscillation is

$$f = \frac{1}{2\pi RC}$$

When f = 20 Hz, C = 100 pF

Then the value of required resistance is

$$R = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 20 \times 100 \times 10^{-9}} = 79.54 \text{ k}\Omega$$

The capacitance varies in the ratio 10 pF:100 pF = 1:10. Then the oscillator frequency range will be 20 Hz to 200 Hz with R = 79.54 kΩ.

Therefore, to generate output signal in the frequency range from 200 Hz to 2 kHz, the value of R will be $\frac{1}{10}$ th of 79.54 kΩ = 7.954 kΩ.

In the same way, for the frequency range from 200 Hz to 2 kHz, the value of R will be $\frac{1}{10}$ th of 7.954 kΩ = 0.7954 kΩ.

(b) Since the gain of amplifier A = 5, for oscillation $\delta = A = 5$

$$\frac{R_4}{R_3 + R_4} = \frac{1}{3} - \frac{1}{\delta} = \frac{1}{3} - \frac{1}{5} = \frac{2}{15}$$

or, $$1 + \frac{R_3}{R_4} = 7.5$$

Therefore, the ratio of the resistances in the other arms of the bridge is

$$\frac{R_3}{R_4} = 6.5$$

3.10 TUNED COLLECTOR OSCILLATOR

Figure 3.17 shows a tuned collector oscillator circuit. The quiescent operating point can be determined by the supply voltage V_{CC} and the resistances R_1, R_2, R_E and R_B. The resistance R_B is in parallel with R_2. As R_B is very large, the effect on the quiescent operating point is very small. In this circuit R_B is used to

- Control the amount of feedback to the value which is just required to sustain oscillations
- Reduce the loading effect of the collector by the transistor for low-input impedance
- Decrease distortion

The emitter bypass capacitor C_E is connected in parallel with resistance R_E and it will not appear in the ac equivalent circuit. Here transistor operates in common emitter configurations. The common emitter amplifier provides 180° phase shift between input and output voltages. The additional 180° phase shift is required to sustain oscillation. Actually phase shift of a tank circuit provides 180° phase shift.

The Frequency Determining Network (FDN) can be made up by the capacitor and transformer primary inductance L_P. As an *LC* tuned circuit is connected with the collector of transistor, this circuit is called as tuned collector oscillator. This *LC* tuned circuit is also known as *tank circuit* as this circuit is used as a frequency determining network.

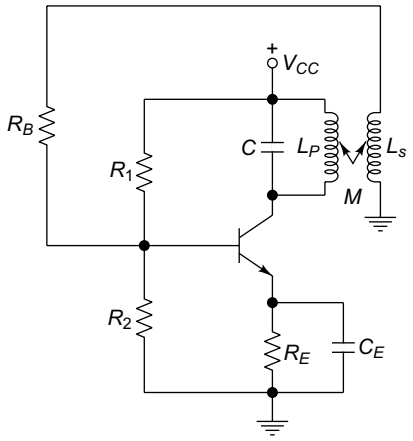


Fig. 3.17 *A tuned collector oscillator*

3.10.1 Analysis of Tuned Collector Oscillator

Figure 3.18 shows the *h*-parameter ac equivalent circuit of Fig. 3.17. *R* is the resistance of the transformer primary winding and its value is very small so that the tank circuit's quality factor *Q* is very high.

The effective resistance offered by this circuit is

$$R_{\text{eff}} = \frac{L_P}{CR}$$

The current flows through the secondary of transformer I_1 is very small so that it induces a negligible voltage in the transformer primary. Due to large value of R_B, the *LC* tuned circuit is not considerably loaded. The frequency of oscillation is

$$f = \frac{\omega}{2\pi} = \frac{1}{2\pi\sqrt{L_P C}} \quad \text{as} \quad \omega^2 = \frac{1}{L_P C}$$

Hence the frequency of oscillation can be varied by changing either L_P or C or both. Usually, tuned collector oscillators generate oscillation signals in the radio frequency (RF) range.

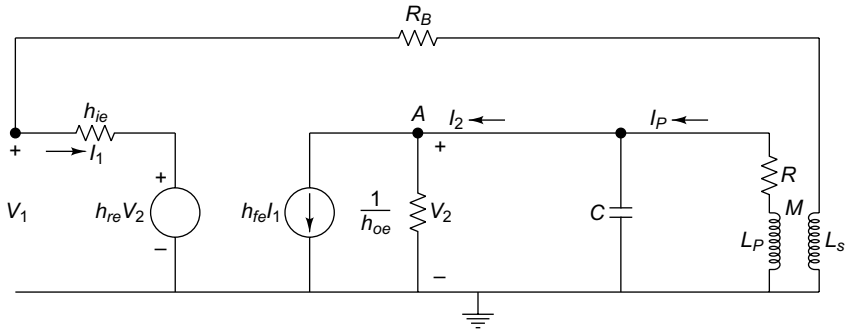


Fig. 3.18 *ac equivalent circuit of tuned collector oscillator*

The voltage V_2 is

$$V_2 = -I_2 R_{\text{eff}} = -I_2 \frac{L_P}{CR}$$

Applying KCL at the point A, we get

$$I_2 = h_{fe} I_1 + h_{oe} V_2$$

After substituting the value of V_2 in the above equation, we obtain

$$I_2 = h_{fe} I_1 + h_{oe}\left(-I_2 \frac{L_P}{CR}\right)$$

or
$$\left(1 + h_{oe} \frac{L_P}{CR}\right) I_2 = h_{fe} I_1 \tag{3.2}$$

The induced voltage across the transformer secondary winding is $j\omega M I_P$ where M is the mutual inductance between primary and secondary

I_P is the primary current

The transformer primary current is equal to

$$I_P = \frac{\frac{1}{j\omega C}}{R + j\omega L_P + \frac{1}{j\omega C}} I_2 = \frac{1}{j\omega CR - \omega^2 L_P C + 1} I_2$$

$$= \frac{1}{j\omega CR} I_2 \quad \text{as} \quad \omega^2 = \frac{1}{L_P C}$$

$$= -j\omega \frac{L_P}{R} I_2 \quad \text{as} \quad C = \frac{1}{\omega^2 L_P}$$

As $R_B >> |\omega L_S|$, the effective impedance in the secondary circuit is $R_B + h_{ie}$

Applying KVL in the secondary circuit, we get

$$I_1 h_{ie} + h_{re} V_2 = j\omega M I_P - I_1 R_B$$

or,
$$(R_B + h_{ie}) I_1 = j\omega M I_P - h_{re} V_2$$

or,
$$I_1 = \frac{j\omega M I_P - h_{re} V_2}{R_B + h_{ie}} \tag{3.3}$$

After substituting the values of I_P and V_2 in the above equation (3.3), we get

$$I_1 = \left(\frac{\omega^2 M L_P}{R} = h_{re} \frac{L_P}{CR} \right) I_2 / (R_B + h_{ie}) \tag{3.4}$$

After substituting the value of I_1 in Eq. (3.4), we obtain

$$\left(1 + h_{oe} \frac{L_P}{CR}\right) = \frac{h_{fe}}{R_B + h_{ie}} \left(\omega^2 M + h_{re} \frac{1}{C}\right) \frac{L_P}{R}$$

As $\omega^2 = \dfrac{1}{L_P C}$, we can find the mutual inductance is

$$M = \frac{R_B}{h_{fe}} \left(CR + h_{oe} L_P\right) + CR \frac{h_{ie}}{h_{fe}} + L_P \frac{\Delta_{he}}{h_{fe}}$$

where $\Delta_{he} = (h_{ie} h_{oe} - h_{fe} h_{re})$

3.6 A tuned collector oscillator is used in a radio receiver and it has inductance L_P = 0.5 mH and its tuning frequency range from 400 Hz to 1600 kHz. Determine the range of capacitors.

Solution

Given L_P = 0.5 mH and frequency range is 400 Hz to 1600 kHz.

The frequency of oscillation of a tuned collector oscillator is

$$f = \frac{1}{2\pi\sqrt{L_P C}}$$

Therefore, $$C = \frac{1}{4\pi^2 f^2 L_P}$$

When $f = 400$ Hz, $C = \dfrac{1}{4\pi^2 \times 400^2 \times 0.5 \times 10^{-3}} = 316.66$ μF

When $f = 1600$ kHz, $C = \dfrac{1}{4\pi^2 \times (1600 \times 1000)^2 \times 0.5 \times 10^{-3}} = 0.0198$ nF

3.7 A tank circuit has an inductance L_P = 0.25 mH. Calculate the range of capacitors when the tuning frequency range is 400 kHz to 1200 kHz.

Solution

Given L_P = 0.25 mH and the tuning frequency range is 400 kHz to 1200 kHz

At any resonance frequency, the value of capacitor is $C = \dfrac{1}{4\pi^2 f^2 L_P}$

If f = 400 kHz, $C = \dfrac{1}{4\pi^2 \times (400 \times 1000)^2 \times 0.5 \times 10^{-3}} = 0.31695$ nF

When f = 1200 kHz, $C = \dfrac{1}{4\pi^2 \times (1200 \times 1000)^2 \times 0.5 \times 10^{-3}} = 35.216$ pF

3.11 TUNED LC OSCILLATORS

The basic block diagram of tuned oscillator is shown in Fig. 3.19. Any one of the active devices such as transistor, FET and operational amplifiers can be used in amplifier. The open loop gain of the amplifier is A. Z_1, Z_2 and Z_3 are impedances which provide the feedback tank circuit and are used to determine the frequency of oscillation. In this circuit Z_1 and Z_2 act as a voltage divider circuit between the output voltage and feedback signal. The feedback voltage is the voltage across Z_1.

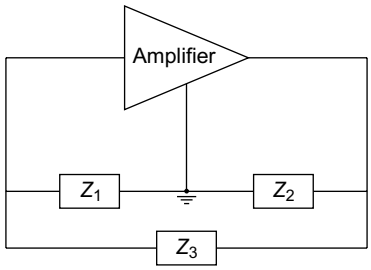


Fig. 3.19 ***Block diagram of tuned oscillator***

The gain with load but without feedback is

$$\overline{A_L} = \frac{\overline{Z_L} A}{\overline{Z_L} + R_o}$$

where, R_o is the output resistance of the amplifier

$\overline{Z_L}$ is the load impedance

The load impedance is

$$\overline{Z_L} = \overline{Z_2} \,||\, (\overline{Z_1} + \overline{Z_3}) = \frac{Z_2(Z_3 + Z_1)}{Z_1 + Z_2 + Z_3}$$

The feedback factor is

$$\overline{\beta} = \frac{\overline{Z_1}}{\overline{Z_1} + \overline{Z_3}}$$

The loop gain will be

$$-\overline{\beta}\,\overline{A_L} = -\frac{\overline{Z_1}}{\overline{Z_1} + \overline{Z_3}} \cdot \frac{\overline{Z_L} A}{\overline{Z_L} + R_o} = -\frac{A\overline{Z_1}\,\overline{Z_2}}{R_o\left(\overline{Z_1} + \overline{Z_2} + \overline{Z_3}\right) + \overline{Z_2}\left(\overline{Z_1} + \overline{Z_3}\right)}$$

The condition of oscillator is $\left|\overline{\beta}\,\overline{A}\right| = 1$

Assume $\overline{Z_1} = jX_1, \overline{Z_2} = jX_2$ and $\overline{Z_3} = jX_3$

Therefore, $-\overline{\beta}\,\overline{A_L} = \dfrac{AX_1X_2}{jR_o(X_1 + X_2 + X_3) - X_2(X_1 + X_3)}$

For oscillation, the loop gain must be real. As a result, $X_1 + X_2 + X_3 = 0$

Then, $$-\overline{\beta}\overline{A_L} = -\frac{AX_1X_2}{X_2(X_1+X_3)}$$

or, $$-\overline{\beta}\overline{A_L} = -\frac{AX_1}{(X_1+X_3)}$$

or, $$-\overline{\beta}\overline{A_L} = \frac{AX_1}{X_2} \text{ as } X_1+X_3 = -X_2$$

X_1 and X_2 must be both inductive or both capacitive. The choice of X_1, X_2 and X_3 gives the three different oscillators such as Colpitts, Hartley oscillators and tuned input tuned output. Table 3.2 shows reactive elements of different types of oscillators.

Table 3.2 *Reactive elements of oscillators*

Oscillator type	*Reactive elements*		
	X_1	X_2	X_3
Colpitts oscillator	*C*	*C*	*I*
Hartley oscillator	*L*	*L*	*C*
Tuned input, and Tuned output	*LC*	*LC*	

3.11.1 Transistor Colpitts Oscillators

Figure 3.20 shows the transistor Colpitts oscillator. The quiescent operating point of the transistor can be determined by the supply voltage V_{CC} and the resistances R_1, R_2, R_C and R_E. The capacitor C_B is used to block the dc current flow from the collector to the base of the transistor and the inductance L. The reactance of

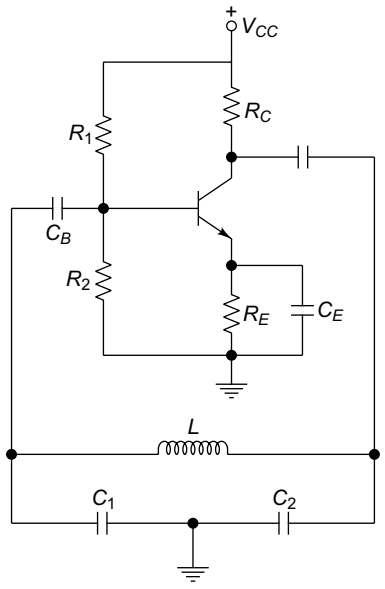


Fig. 3.20 ***Transistor Colpitts oscillators***

capacitor C_B is negligible at the frequency of oscillation. The emitter bypass capacitor C_E is connected in parallel with resistance R_E and it will not appear in the ac equivalent circuit. In this circuit, the transistor operates in common emitter configurations and introduces 180° phase shift between input and output voltages. The voltage across C_1 is a fraction of the output voltage. As the feedback voltage is equal to the voltage across C_1 and it is 180° out of phase with respect to output voltage, the net phase shift around the loop is 0° or 360°. The frequency determining network is formed by the inductance L and capacitors C_1 and C_2.

In this circuit, X_1, X_2 and X_3 are reactances of capacitors C_1, and C_2 and inductance L respectively. The reactance values are $X_1 = -\frac{1}{\omega C_1}$, $X_2 = -\frac{1}{\omega C_2}$, $X_3 = \omega L$

The condition for oscillation is

$$(X_1 + X_2 + X_3) = 0$$

Assuming ω_o at resonance frequency, we can write

$$\frac{1}{\omega_o C_1} + \frac{1}{\omega_o C_2} = \omega_o L$$

or, $$\frac{\omega_o (C_1 + C_2)}{\omega_0^2 C_1 C_2} = \omega_o L$$

or, $$\frac{1}{\omega_o C_{\text{eq}}} = \omega_o L \quad \text{where, } C_{\text{eq}} = \frac{C_1 C_2}{C_1 + C_2}$$

or, $$\omega_o^2 = \frac{1}{LC_{\text{eq}}}$$

or, $$\omega_o = \frac{1}{\sqrt{LC_{\text{eq}}}}$$

or, $$2\pi f_o = \frac{1}{\sqrt{LC_{\text{eq}}}}$$

The frequency of oscillation is

$$f_o = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}}$$

3.11.2 Analysis of Colpitts Oscillator

Figure 3.21 shows the ac equivalent circuit of transistor Colpitts oscillator. In this circuit, actually the current source $h_{fe}I_1$ is connected in parallel (shunt) with the resistance $\frac{1}{h_{oe}}$. After applying the Thevenin's theorem looking from *A*-*B* terminals, we obtain a most simplified *h*-parameter ac equivalent circuit as depicted in

Fig. 3.22. The Thevenin's *t* equivalent voltage is $\frac{h_{fe}}{h_{oe}} I_1$ and the internal resistance is $\frac{1}{h_{oe}}$.

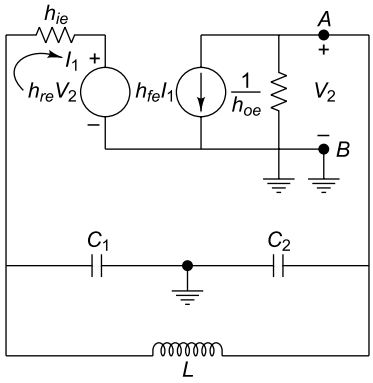


Fig. 3.21 *ac equivalent circuit of Colpitts oscilllator*

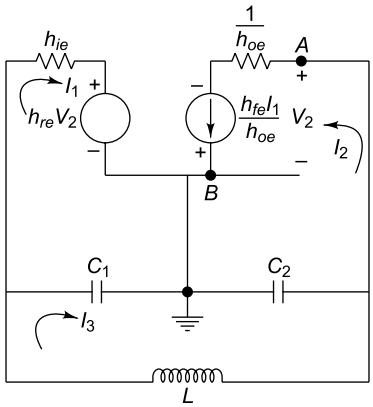


Fig. 3.22 *Simplified ac equivalent circuit of Colpitts oscilllator*

The voltage difference between *A* and *B* is V_2.

$$V_2 = \frac{1}{h_{oe}} I_2 - \frac{h_{fe}}{h_{oe}} I_1$$

KVL loop equations are as follows

Loop-I equation is

$$\left(h_{ie} - \frac{h_{fe} h_{re}}{h_{oe}} - j \frac{1}{\omega C_1} \right) I_1 + \frac{h_{re}}{h_{oe}} I_2 + j \frac{1}{\omega C_1} I_3 = 0$$

Loop-II equation is

$$-\frac{h_{fe}}{h_{oe}} I_1 + \left(\frac{1}{h_{oe}} - j \frac{1}{\omega C_2} \right) I_2 - j \frac{1}{\omega C_2} I_3 = 0$$

and Loop-III equation is

$$j\frac{1}{\omega C_1}I_1 - j\frac{1}{\omega C_2}I_2 + j\left(\omega L - \frac{1}{\omega C_1}\text{`} - \frac{1}{\omega C_2}\right)I_3 = 0$$

The loop equations can be represented in combined form as

$$\begin{bmatrix} h_{ie} - \frac{h_{fe}h_{re}}{h_{oe}} - j\frac{1}{\omega C_1} & \frac{h_{re}}{h_{oe}} & j\frac{1}{\omega C_1} \\ -\frac{h_{fe}}{h_{oe}} & \frac{1}{h_{oe}} - \frac{1}{\omega C_2} & -j\frac{1}{\omega C_2} \\ j\frac{1}{\omega C_1} & -j\frac{1}{\omega C_2} & j\omega L - j\frac{1}{\omega C_1} - j\frac{1}{\omega C_2} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = 0$$

As I_1, I_2 and I_3 are not equal to zero, the determinant of the coefficients of I_1, I_2 and I_3 must be zero.

The real part of the determinant of the coefficients of I_1, I_2 and I_3 must be zero and we can derive

$$\frac{C_1}{C_2} = \frac{h_{fe}}{\Delta_{he}} \quad \text{where, } \Delta_{he} = (h_{ie}h_{oe} - h_{fe}h_{re})$$

Therefore, the condition of oscillation is $\frac{C_1}{C_2} = \frac{h_{fe}}{\Delta_{he}}$. For example, if h_{fe} = 100 and Δ_{he} = 0.5, the condition for sustained oscillations is $\frac{C_1}{C_2} = \frac{h_{fe}}{\Delta_{he}} = \frac{100}{0.5} = 200.$

The imaginary part of the determinant of the coefficients of I_1, I_2 and I_3 must be zero and we can derive

$$\omega^2 = \frac{h_{oe}}{h_{ie}}\frac{1}{C_1C_2} + \frac{1}{LC_1} + \frac{1}{LC_2}$$

Then the frequency of oscillation is

$$\omega = 2\pi f = \left(\frac{h_{oe}}{h_{ie}}\frac{1}{C_1C_2} + \frac{1}{LC_1} + \frac{1}{LC_2}\right)^{\frac{1}{2}}$$

or,

$$f = \frac{1}{2\pi}\left(\frac{h_{oe}}{h_{ie}}\frac{1}{C_1C_2} + \frac{1}{LC_1} + \frac{1}{LC_2}\right)^{\frac{1}{2}}$$

Since $\frac{1}{LC_1} + \frac{1}{LC_2} >> \frac{h_{oe}}{h_{ie}}\frac{1}{C_1C_2}$, we get

$$f = \frac{1}{2\pi}\left(\frac{1}{LC_1} + \frac{1}{LC_2}\right)^{\frac{1}{2}} = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}}$$

where, $\frac{1}{C_{\text{eq}}} = \frac{1}{C_1} + \frac{1}{C_2}$ or $C_{\text{eq}} = \frac{C_1C_2}{C_1 + C_2}$ which is the equivalent capacitance of C_1 and C_2 connected in series.

3.8 In a Colpitts oscillator, the value of capacitors are $C_1 = 0.25$ pF and $C_2 = 0.020$ pF the inductance of coils are $L_1 = 0.5$ mH. Calculate the frequency of oscillations and the required gain for oscillation.

Solution

Given $C_1 = 0.25$ pF, $C_2 = 0.020$ pF and $L_1 = 0.5$ mH

The equivalent capacitance of C_1 and C_2 $C_{eq} = \dfrac{C_1 C_2}{C_1 + C_2}$

$$= \frac{0.25 \times 0.020}{0.25 + 0.020} \text{ pF} = 0.0185 \text{ pF}$$

The frequency of Colpitts oscillator is

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.5 \times 10^{-3} \times 0.0185 \times 10^{-12}}} = 0.523565 \text{ MHz}$$

3.9 In a Colpitts oscillator, the value of capacitors are $C_1 = 0.125$ μF and $C_2 = 0.020$ μF the inductance of coil is $L_1 = 0.5$ mH.

(a) Find the frequency of oscillation.

(b) If the frequency of the oscillation is 20 kHz, find the value of inductance of coil. And determine the voltage gain of oscillator.

Solution

Given $C_1 = 0.125$ μF , $C_2 = 0.020$ μF and $L_1 = 0.5$ mH

(a) The equivalent capacitance of C_1 and C_2

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.25 \times 0.020}{0.25 + 0.020} \text{ pF} = 0.01724 \text{ μF}$$

The frequency of Colpitts oscillator is

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.5 \times 10^{-3} \times 0.01724 \times 10^{-6}}} = 54.236 \text{ kHz}$$

(b) When frequency of the oscillation is 20 kHz, the value of inductance of the coil is

$$L = \frac{1}{4\pi^2 f^2 C_{eq}} = \frac{1}{4\pi^2 (20 \times 10^3)^2 \times 0.01724 \times 10^{-6}} = 3.677 \text{ mH}$$

The voltage gain is $\dfrac{C_1}{C_2} = \dfrac{0.125}{0.020} = 6.25$

3.10 In a Colpitts oscillator, the values of capacitors and coil inductance are $C_1 = 0.5$ μF and $C_2 = 2.5$ μF and $L_1 = 0.5$ mH.

(a) When the output voltage is 10 V, calculate the feedback voltage.

(b) What is the frequency of oscillation?

Solution

Given $C_1 = 0.5$ μF, $C_2 = 2.5$ μF and $L_1 = 0.5$ mH

(a) The feedback voltage is the voltage across C_2 and it is directly proportional to XC_2. Therefore $V_f \propto XC_2$

The output voltage is the voltage across C_1 and it is directly proportional to XC_1.

So that $V_o \propto XC_1$

$$\frac{V_f}{V_o} = \frac{XC_2}{XC_1} = \frac{\frac{1}{\omega C_2}}{\frac{1}{\omega C_1}} = \frac{C_1}{C_2}$$

$$V_f = \frac{C_1}{C_2} V_o = \frac{0.5}{2.5} \times 10 = 2 \text{ V}$$

(b) The equivalent capacitance of C_1 and C_2

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.5 \times 2.5}{0.5 + 2.5} \ \mu\text{F} = 0.417 \ \mu\text{F}$$

The frequency of Colpitts oscillator is

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.5 \times 10^{-3} \times 0.417 \times 10^{-6}}} = 11.02779 \text{ kHz}$$

3.11.3 Hartley Oscillator

Figure 3.23 shows the Hartley oscillator. The quiescent operating point of the transistor can be established by the supply voltage V_{CC} and the resistances R_1, R_2, R_C and R_E. The capacitor C_B is the blocking capacitor and is used to block the dc current flow. The reactance of capacitor C_B is negligible at the frequency of oscillation. C_E is the emitter bypass capacitor. C_E is connected in parallel with resistance R_E and it will not appear in the ac equivalent circuit. As the transistor operates in common emitter configuration, it introduces 180° phase shift between input and output voltages. In this circuit, the voltage across the tank circuit is connected to the collector. The feedback voltage is a fraction of the output voltage. As the feedback voltage is equal to the voltage across L_1 and it is 180° out of phase with respect to output voltage, the total phase shift around the loop is 0° or 360°. The frequency determining network is formed by the inductors L_1 and L_2 and capacitor C.

In this circuit, X_1, X_2 and X_3 are reactance of inductors L_1 and L_2 and capacitor C respectively. The reactance values are

$$X_1 = \omega(L_1 + M), \quad X_2 = \omega(L_2 + M), \text{ and } X_3 = -\frac{1}{\omega C}$$

where, M is the mutual inductance.

The condition for oscillation is

$$(X_1 + X_2 + X_3) = 0$$

So that $$\omega(L_1 + M) + \omega(L_2 + M) = \frac{1}{\omega C}$$

or, $$\omega(L_1 + L_2 + 2M) = \frac{1}{\omega C}$$

or, $$\omega^2 = \frac{1}{(L_1 + L_2 + 2M)C}$$

or, $$\omega^2 = \frac{1}{L_{eq}C}$$

as $L_{eq} = (L_1 + L_2 + 2M)$

or, $$\omega = \frac{1}{\sqrt{L_{eq}C}}$$

or, $$2\pi f = \frac{1}{\sqrt{L_{eq}C}}$$

The frequency of oscillation is

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}} \quad \text{and}$$

The condition for sustained oscillation is

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M}$$

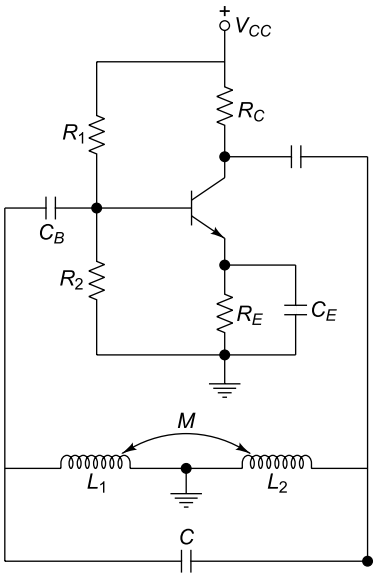


Fig. 3.23 *Transistor Hartley Oscillator*

3.11.4 Analysis of Hartley Oscillator

Figure 3.24 shows the *h*-parameter model ac equivalent circuit of Hartley oscillator. In this circuit, actually the current source $h_{fe}I_1$ is connected in parallel (shunt) with the resistance $\frac{1}{h_{oe}}$. After applying the Thevenin's theorem looking from *A-B* terminals, we obtain a most simplified circuit as shown in Fig. 3.25. The Thevenin's *t* equivalent voltage is $\frac{h_{fe}}{h_{oe}}I_1$ and the internal resistance is $\frac{1}{h_{oe}}$. For simplify the analysis of oscillator circuit, the mutual inductance between L_1 and L_2 is neglected.

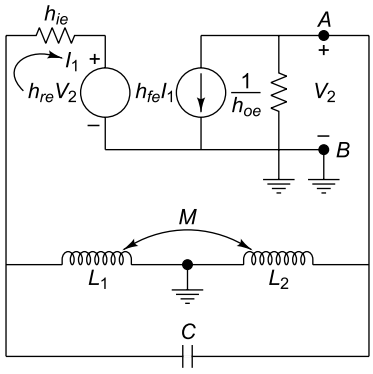


Fig. 3.24 *ac equivalent circuit of Hartley oscillator*

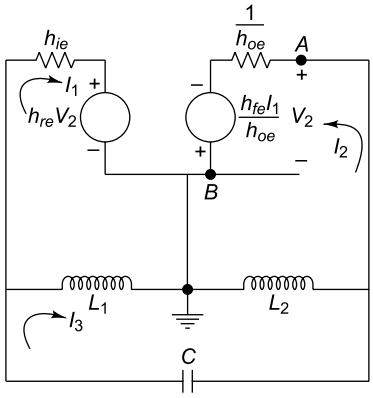


Fig. 3.25 *Simplified ac equivalent circuit of Hartley oscillator*

The voltage across A and B is V_2

$$V_2 = \frac{1}{h_{oe}} I_2 - \frac{h_{fe}}{h_{oe}} I_1$$

KVL equation for Loop-I is

$$\left(h_{ie} + j\omega L_1 - \frac{h_{fe} h_{re}}{h_{oe}} \right) I_1 + \frac{h_{re}}{h_{oe}} I_2 - j\omega L_1 I_3 = 0$$

KVL equation for Loop-II is

$$-\frac{h_{fe}}{h_{oe}} I_1 + \left(\frac{1}{h_{oe}} + j\omega L_2 \right) I_2 + j\omega L_2 I_3 = 0$$

KVL equation for Loop-III is

$$-j\omega L_1 I_1 + j\omega L_2 I_2 + \left(j\omega L_1 + j\omega L_2 - j\frac{1}{\omega C} \right) I_3 = 0$$

The loop equation can be represented in combined form as

$$\begin{bmatrix} h_{ie} + j\omega L_1 - \frac{h_{fe} h_{re}}{h_{oe}} & \frac{h_{re}}{h_{oe}} & -j\omega L_1 \\ -\frac{h_{fe}}{h_{oe}} & \frac{1}{h_{oe}} + j\omega L_2 & j\omega L_2 \\ -j\omega L_1 & j\omega L_2 & j\omega L_1 + j\omega L_2 - j\frac{1}{\omega C} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = 0 \quad (3.5)$$

As I_1, I_2 and I_3 are not equal to zero, the determinant of the coefficients of I_1, I_2 and I_3 must be zero.

The determinant of the coefficients of I_1, I_2 and I_3 is

$$\left(h_{ie} + j\omega L_1 - \frac{h_{fe} h_{re}}{h_{oe}} \right) L_2^2 + \frac{h_{re}}{h_{oe}} L_1 L_2 - \frac{h_{fe}}{h_{oe}} L_1 L_2 + \left(\frac{1}{h_{oe}} + j\omega L_2 \right) L_1^2 = 0 \quad (3.6)$$

as $$\omega L_1 + \omega L_2 - \frac{1}{\omega L} = 0 \text{ during oscillation}$$

The real part of the equation (3.6) is

$$\Delta_{he}L_2^2 - (h_{fe} - h_{re})L_1L_2 + L_1^2 = 0 \text{ where, } \Delta_{he} = (h_{ie}h_{oe} - h_{fe}h_{re})$$

or, $$\Delta_{he}L_2^2 - h_{fe}L_1L_2 + L_1^2 = 0 \text{ as } h_{re} << 1$$

The value of inductance L_2 is

$$L_2 = \frac{h_{fe}L_1 \pm \sqrt{h_{fe}L_1^2 - 4\Delta_{he}L_1^2}}{2\Delta_{he}}$$

or, $$L_2 = \frac{h_{fe}L_1}{2\Delta_{he}} \text{ as } h_{fe}^2 >> 4\Delta_{he}$$

The imaginary part of Eq. (3.5) is equal to zero, and we can write

$$\frac{\omega}{C}L_1L_2 + \frac{h_{ie}}{h_{oe}}\left(\omega L_1 + \omega L_2 - \frac{1}{\omega C}\right) = 0$$

or, $$\omega^2 = \frac{1}{\left(\frac{h_{oe}L_1L_2}{h_{ie}}\right) + C(L_1 + L_2)}$$

The frequency of oscillation is

$$f = \frac{1}{2\pi}\frac{1}{\sqrt{\frac{h_{oe}L_1L_2}{h_{ie}} + C(L_1 + L_2)}}$$

As $C(L_1 + L_2) >> \frac{h_{oe}L_1L_2}{h_{ie}}$, the $f = \frac{1}{2\pi}\frac{1}{\sqrt{C(L_1 + L_2)}}$

Then, oscillator frequency is $f = \frac{1}{2\pi}\frac{1}{\sqrt{L_{eq}C}}$ where $L_{eq} = L_1 + L_2$

In the above analysis, the mutual inductance M between L_1 and L_2 is neglected. When M is incorporated in the analysis, L_1 will be replaced by $L_1 + M$ and L_2 will be replaced by $L_2 + M$.

3.11 In a Hartley oscillator, $L_1 = 0.02$ mH and $C = 0.047$ μF. When the frequency of the oscillator is 100 kHz, determine the value of L_2. Assume mutual inductance is negligible.

Solution

Given $L_1 = 0.02$ mH, $C = 0.047$ μF and $f = 100$ kHz

The frequency of Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

The value of $L_2 = \frac{1}{4\pi^2 f^2 C} - L_1$

$$= \frac{1}{4\pi^2 \times (100 \times 10^3)^2 \times 0.047 \times 10^{-6}} - 0.02 \times 10^{-3}$$

$$= (0.05396 - 0.02) \text{ mL} = 0.03396 \text{ mL}$$

3.12 The frequency of a transistorized Hartley oscillator can be varied from 50 kHz to 150 kHz. The tuning capacitor can changed from 100 pF to 400 pF. Determine the values of inductances. Assume $h_{fe} = 100$ and $\Delta_{he} = 0.1$.

Solution

Given $h_{fe} = 100$ and $\Delta_{he} = 1$, range of frequency = 50 kHz to 150 kHz and capacitor range 100 pF to 300 pF.

The frequency of a transistorized Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

The effective inductance $L_1 + L_2 = \dfrac{1}{4\pi^2 f^2 C}$ mH

The ratio of inductances is $\dfrac{L_2}{L_1} = \dfrac{h_{fe}}{\Delta_{he}} = \dfrac{100}{0.1} = 1000$

So that $L_2 = 1000L_1$

The frequency variation ratio is 50 kHz : 100 kHz = 1 : 2. This frequency variation can be achieved by the capacitance ratio 100 pF : 400 pF = 1 : 4. Therefore, if frequency is 50 kHz, the capacitance value will be 400 pF.

When $f = 50$ kHz, $L_1 + L_2 = \dfrac{1}{4\pi^2 f^2 C}$

$$= \frac{1}{4\pi^2 (50\times10^3)^2 \times 400\times10^{-12}} \text{H}$$

$$= 25.35 \text{ mH}$$

$L_1 + L_2 = 1001L_1 = 25.35$ mH (as $L_2 = 1000L_1$)

Therefore, $L_1 = 0.02532$ mH and $L_2 = 25.32468$ mH

3.13 A Hartley oscillator uses a tank circuit with $L_1 = 0.4$ mH, $L_2 = 0.3$ mH and $C = 0.047$ μF. What is the frequency of oscillator? Assume mutual inductance is negligible.

Solution

Given $L_1 = 0.4$ mH, $L_2 = 0.3$ mH and $C = 0.047$ μF

The frequency of Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

$$= \frac{1}{2\pi\sqrt{(0.4\times10^{-3} + 0.3\times10^{-3})\times0.047\times10^{-6}}}$$

$$= \frac{1}{2\pi\times0.5735\times10^{-5}} = 27.765 \text{ KHz}$$

3.14 In a Hartley oscillator $L_2 = 0.2$ mH and $C = 0.47$ nF. When the frequency of the oscillator is 150 kHz, determine the value of L_1. Assume mutual inductance is negligible.

Solution

Given $L_2 = 0.2$ mH, $C = 0.47$ nF and frequency of the oscillator $f = 150$ kHz

The frequency of Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

The value of inductance L_1 is

$$L_1 = \frac{1}{4\pi^2 f^2 C} - L_2$$

$$= \frac{1}{4\pi^2 (150\times10^3)^2 \times 0.47\times10^{-9}} - 0.2\times10^{-3}$$

$$= 2.397 \text{ mH} - 0.2 \text{ mH} = 2.197 \text{ mH}$$

3.15 In a transistorized Hartley oscillator, $L_1 = 0.5$ mH, $L_2 = 0.5$ μH while the frequency has been changed from 100 kHz to 2000 kHz. Determine the range of the capacitor. Assume mutual inductance is negligible.

Solution

Given $L_1 = 0.5$ mH, $L_2 = 0.5$ μH and range of frequency = 100 kHz to 2000 kHz

The frequency of the Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

The value of the capacitor is

$$C = \frac{1}{4\pi^2 f^2 (L_1 + L_2)C}$$

When $f_1 = 100$ kHz, the capacitor value is

$$C = \frac{1}{4\pi^2 f_1^2 (L_1 + L_2)C} = \frac{1}{4\pi^2 (100\times10^3)^2 (0.5\times10^{-3} + 0.5\times10^{-6})}$$

$$= 5.066 \text{ nF}$$

When $f_2 = 2000$ kHz

$$C = \frac{1}{4\pi^2 f_2^2 (L_1 + L_2)C} = \frac{1}{4\pi^2 (2000\times10^3)^2 (0.5\times10^{-3} + 0.5\times10^{-6})}$$

$$= 12.665 \text{ pF}$$

Therefore, the range of capacitance is 5.066 nF to 12.665 pF.

3.16 In a Hartley oscillator, the value of the capacitor is 250 pF and the inductance of coils are $L_1 = 0.5$ mH, $L_2 = 0.025$ mH. Calculate the frequency of oscillations and the feedback factor. Assume mutual inductance is negligible.

Solution

Given $C = 250$ pF, $L_1 = 0.5$ mH, $L_2 = 0.025$ mH

The frequency of Hartley oscillator is

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}} = \frac{1}{2\pi\sqrt{(0.5 + 0.025)\times10^{-3} \times 250\times10^{-12}}}$$

$$= 439.53 \text{ kHz}$$

The feedback factor is $\beta = \frac{L_1}{L_2} = \frac{0.5}{0.025} = 20$

3.12 CRYSTAL OSCILLATORS

To get high frequency stability in an oscillators circuit, a crystal is used as the frequency determining element. This type of oscillator is known as crystal oscillator. Usually, cut-quartz crystals are used in crystal oscillators. There are two different methods of cutting quartz crystals. Actually, the methods of cutting find out the resonant frequency of oscillation and temperature coefficient of the crystal. The cross-section of a crystal is hexagonal. When the crystal is cut in such a way that its flat surfaces are perpendicular to *X*-axis (electrical axis), this cut is called *X*-cut crystal. If the crystal is cut in such a way that its flat surfaces are perpendicular to *Y*-axis (mechanical axis), this cut is called *Y*-cut crystal. Figure 3.26(a) shows the quartz crystal and *X*-cut and *Y*-cut of quartz crystal are shown in Fig. 3.26(b) and (c) respectively.

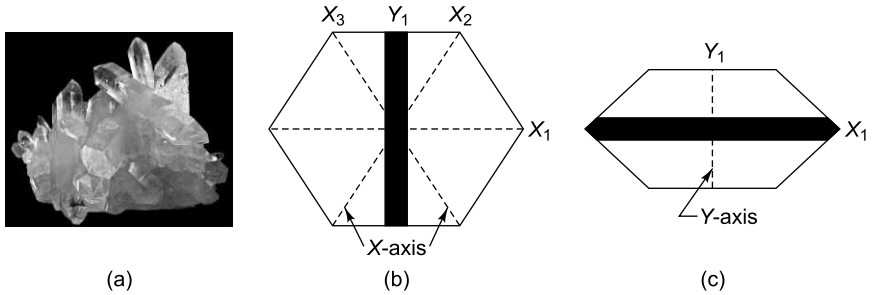


Fig. 3.26 ***(a) Quartz crystal (b) X-cut quartz crystal (c) Y-cut quartz crystal***

When the edges of *X*-cut crystal are subjected to mechanical stress, an electrical potential will be developed across its faces. The polarity of electrical potential will be reversed when stress changes from tension to compression. If electrodes are placed on opposite faces of a crystal or quartz (*X*-cut or *Y*-cut crystal) and a voltage is applied across electrodes, a mechanical stress is developed along the edges. Actually, the electric field set up exerts forces on bound charges within the crystal. Then the crystal electromechanically vibrates. This property of a crystal is known as piezoelectric effect.The crystal oscillators are available within a wide range of frequencies from a few kHz to 100 MHz and *Q* factors will be a few thousand to several hundred thousands. The crystal oscillator frequency is very stable with respect to temperature variation and aging. Figure 3.27(a) shows the crystal oscillator and its reactance variation with respect to frequency is depicted in Fig. 3.27(c).

Figure 3.27(b) shows an $L\ C_S\ R$ series resonant circuit which is used to represent a piezoelectric crystal. The inductance L, capacitance C_S and resistance R are electrical equivalents of the mass, compliance and friction of the vibrating crystal

respectively. The capacitance C_S is the electrostatic capacitance between the electrodes and crystal as the dielectric. The values of L, C_S, R and C_P depend on crystal cut and its size and the nature of vibration of the crystal oscillator.

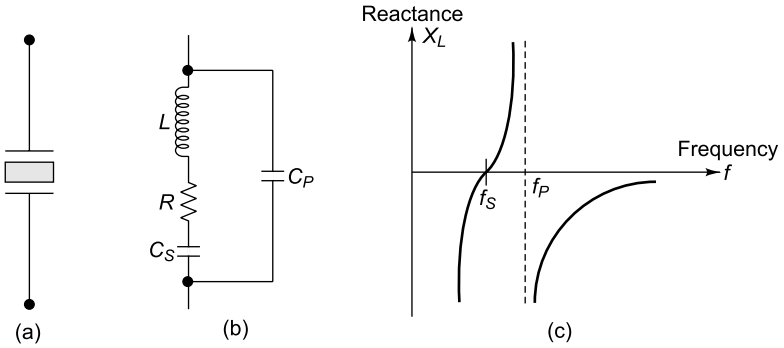


Fig. 3.27 ***(a) Symbol of crystal oscillator (b) Its circuit model (c) Reactance variation with respect to frequency***

This circuit has two resonant frequencies such as series resonant frequency and parallel resonant frequency. At series resonant frequency f_S, the reactance of the series arm is zero.

So that $\omega_S L - \dfrac{1}{\omega_S C_S} = 0$

Then series resonant frequency is $f_S = \dfrac{1}{2\pi\sqrt{LC_S}}$. At the frequency f_S, the impedance of the series arm is equal to R.

At parallel resonant frequency f_P, the reactance of the circuit will be zero. Then we can write $\omega_P L - \dfrac{1}{\omega_P C_s} - \dfrac{1}{\omega C_P} = 0$.

Subsequently, parallel resonant frequency is $f_P = \dfrac{1}{2\pi\sqrt{LC_{\text{eq}}}}$

where, $C_{\text{eq}} = \dfrac{C_S C_P}{C_S + C_P}$.

The variation of reactance with frequency is depicted in Fig. 3.27(c). For the frequency range $0 < f < f_S$, X is negative, i.e. capacitive. At series resonant frequency $f = f_S$, $X = 0$. In the frequency range $f_S < f < f_P$, X is positive, i.e., inductive. When $f > f_P$, X is capacitive and asymptotically approaches zero.

Figure 3.28 shows a crystal oscillator circuit. If we compare this circuit with Colpitts oscillator circuit, we find that both the circuits are identical except the inductor of the Colpitts oscillator is replaced by crystal. The frequency of oscillation of the crystal oscillator is the parallel resonant frequency $f_P = \dfrac{1}{2\pi\sqrt{LC_{\text{eq}}}}$ where,

$C_{eq} = \dfrac{C_S C_P}{C_S + C_P}$. Since R is very small, the quality factor Q of the circuit is very high. The typical value of Q will be several hundred thousand. The crystal oscillators are available with in a wide range of frequencies from some kHz to several MHz and Q factors will be a few thousand to several hundred thousands. The stability of crystal oscillator frequency is very stable with respect to temperature variation and aging.

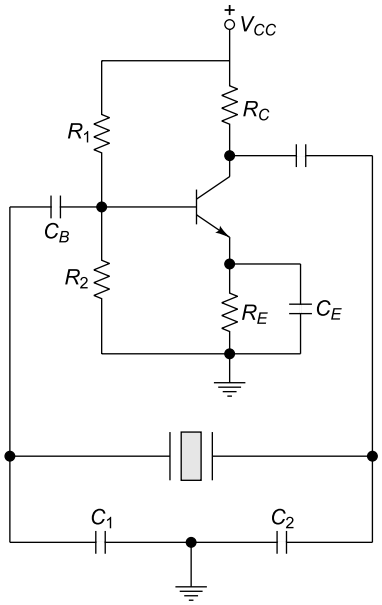


Fig. 3.28 *Circuit of a crystal oscillator*

3.17 In a crystal oscillator, the value of inductance L = 0.25 H, capacitor C_S = 0.047 pF capacitor C_P = 4.77 pF and R = 10 K. Determine the series resonant frequency, parallel resonant frequency and Q factor of the crystal.

Solution

Given L = 0.25 mH, C_S = 0.047 pF, C_P = 4.77 pF and R = 10 kΩ

The series resonant frequency is $f_S = \dfrac{1}{2\pi\sqrt{LC_S}}$

$$= \frac{1}{2\pi\sqrt{0.25\times10^{-3}\times0.047\times10^{-12}}} = 46.45 \text{ MHz}$$

The parallel resonant frequency is $f_P = \dfrac{1}{2\pi\sqrt{LC_{eq}}}$

where, $$C_{eq} = \frac{C_S C_P}{C_S + C_P} = \frac{0.047\times4.77}{0.047+4.77} = 0.0465 \text{ pF}$$

or, $$f_P = \frac{1}{2\pi\sqrt{0.25\times10^{-3}\times0.0465\times10^{-12}}} = 46.70 \text{ MHz}$$

Q factor of the crystal at series resonant frequency is

$$Q_S = \frac{\omega_S L}{R} = \frac{2\pi \times 46.45 \times 10^6 \times 0.25}{10 \times 10^3} = 7292.65$$

Q factor of the crystal at parallel resonant frequency is

$$Q_P = \frac{\omega_P L}{R} = \frac{2\pi \times 46.70 \times 10^6 \times 0.25}{10 \times 10^3} = 7331.9$$

EXERCISES

Short- and Long-Answer-Type Questions

1. Define oscillator. What are the types of oscillator? What are the basic requirements of an oscillator circuit?
2. Write the basic principle of oscillator. Explain the Barkhausen criteria for oscillation.
3. State the different conditions for oscillations in a feedback amplifier.
4. Explain Nyquist criterion to check the stability of amplifier.
5. Explain the following:
   (a) Phase shift in oscillation (b) Phase shift oscillator
   (c) BJT phase shift oscillator (d) FET phase shift oscillator
6. Draw a transistor phase shift oscillator circuit. Derive an expression for the frequency of oscillation and the condition for sustained oscillations.
7. Justify the statement "Positive feedback amplifier works as an oscillator".
8. Draw a Wein bridge oscillator using OP-AMP and *R-C* bridge circuit and derive an expression for the frequency of oscillation.
9. (a) State the amplitude stability of Wein bridge oscillator.
   (b) Justify the statement "The amplifier gain in a Wein bridge oscillator must be greater than 3 for sustained oscillations".
   (c) Write the advantages and disadvantages of Wein bridge oscillator.
   (d) Write difference between *RC* phase shift oscillator and Wein bridge oscillator.
10. Explain the operating principle of a tuned collector oscillator. Derive an expression for the frequency of oscillation. Write the condition for sustained oscillations.
11. Give the basic principle of operation of tuned *LC* oscillator.
12. Draw the circuit of transistor Colpitts oscillator and explain its operation. Analyse a transistor Colpitts oscillator and derive an expression for the frequency of oscillation and the condition for sustained oscillations.
13. (a) Explain the Hartley oscillator and explain its operation.
    (b) Analyse transistor Hartley oscillator and derive an expression for the frequency of oscillation and the condition for sustained oscillations.
    (c) What is the difference between a Colpitts oscillator and an Hartley oscillator?
14. (a) State the principle of operation of a crystal oscillator and derive the frequency of oscillation.
    (b) What are the advantages of crystal oscillators?

15. In an *RC* phase shift oscillator, if the value of resistors are $R_1 = R_2 = R_3 = 150$ kΩ and the value of capacitors are $C_1 = C_2 = C_3 = 0.25$ nF, determine the frequency of the oscillation.
16. Find the frequency of oscillation in an *RC* phase shift oscillator as shown in Fig. 3.11. Assume $R = 25$ kΩ, $C = 0.011$ μF, $R_C = 5.2$ kΩ. Determine the minimum value of current gain for the oscillation.
17. Determine the value of capacitors and current gain of the transistor when the frequency of oscillation in a *RC* phase shift oscillator is 20 KHz. Assume $R_1 = R_2 = R_3 = R = 150$ kΩ, $R_C = 4.7$ kΩ.
18. In a Wein bridge oscillator when the value of resistor $R = 250$ kΩ and the frequency of the oscillation is 30 kHz, determine the value of capacitor *C*.
19. In a Wein bridge oscillator, the value of capacitors can be changed from 10 pF to 100 pF to generate sine wave output signals from 50 Hz to 50 kHz.
    (a) Determine the resistances required to generate the output signals from 50 Hz to 50 kHz.
    (b) If the gain of the amplifier is 5, what will be the ratio of the resistances in the other arms of the bridge?
20. A tuned collector oscillator is used in a radio receiver and it has inductance $L_P = 0.5$ mH and its tuning frequency range from 200 Hz to 800 kHz. Determine the range of capacitors.
21. A tank circuit has an inductance $L_P = 0.25$ mH. Calculate the range of capacitors when the tuning frequency range is 400 kHz to 1200 kHz.
22. In a Colpitts oscillator, the value of capacitors are $C_1 = 0.20$ pF and $C_2 = 0.020$ pF, the inductance of coils are $L_1 = 0.5$ mH. Calculate the frequency of oscillations and the required gain for oscillation.
23. In a Colpitts oscillator, the value of capacitors are $C_1 = 0.125$ μF and $C_2 = 0.020$ μF the inductance of coil is $L_1 = 0.5$ mH.
    (a) Find the frequency of oscillation.
    (b) If the frequency of the oscillation is 15 kHz, find the value of inductance of coil and also determine the voltage gain of oscillator.
24. In a Colpitts oscillator, the values of capacitors and coil inductance are $C_1 = 0.5$ μF and $C_2 = 3.0$ μF and $L_1 = 0.5$ mH.
    (a) When the output voltage is 12 V, calculate the feedback voltage.
    (b) What is the frequency of oscillation.
25. In a Hartley oscillator, $L_1 = 0.025$ mH and $C = 0.047$ μF. When the frequency of the oscillator is 150 kHz, determine the value of L_2. Assume mutual inductance is negligible.
26. The frequency of a transistorized Hartley oscillator can be varied from 50 kHz to 100 kHz. The tuning capacitor can changed from 100 pF to 200 pF. Determine the values of inductances. Assume $h_{fe} = 50$ and $\Delta_{he} = 0.1$.
27. A Hartley oscillator uses a tank circuit with $L_1 = 0.5$ mH, $L_2 = 0.3$ mH and $C = 0.01$ μF. What is the frequency of oscillator? Assume mutual inductance is negligible.

28. In a Hartley oscillator $L_2 = 0.25$ mH and $C = 0.047$ μF. When the frequency of the oscillator is 125 kHz, determine the value of L_1. Assume mutual inductance is negligible.
29. In a transistorized Hartley oscillator $L_1 = 0.5$ mH, $L_2 = 0.5$ μH while the frequency has been changed from 50 kHz to 500 kHz. Determine the range of the capacitor. Assume mutual inductance is negligible.
30. In a Hartley oscillator, the value of a capacitor is 200 pF and the inductance of coils are $L_1 = 0.5$ mH, $L_2 = 0.025$ mH. Calculate the frequency of oscillations and the feedback factor. Assume mutual inductance is negligible.
31. In a crystal oscillator, the value of inductance $L = 0.20$ H, capacitor $C_S = 0.047$ pF capacitor $C_P = 4.77$ pF and $R = 5.7$ K. Determine the series resonant frequency, parallel resonant frequency and Q factor of the crystal.
32. Draw the circuit diagram of a crystal oscillator and explain its operating principle. Derive the frequency of oscillation of a crystal oscillator. What are the advantages of crystal oscillators?

MULTIPLE CHOICE QUESTIONS

1. A positive feedback amplifier with gain A and feedback path gain β works as an oscillator if

   (a) $|\overline{\beta}\overline{A}| = 1$ and $\angle\overline{\beta}\overline{A} = 180°$ (b) $|\overline{\beta}\overline{A}| = 2$ and $\angle\overline{\beta}\overline{A} = 180°$

   (c) $|\overline{\beta}\overline{A}| = 1$ and $\angle\overline{\beta}\overline{A} = 360°$ (d) $|\overline{\beta}\overline{A}| = 2$ and $\angle\overline{\beta}\overline{A} = 360°$

   Answer: (c) $|\overline{\beta}\overline{A}| = 1$ and $\angle\overline{\beta}\overline{A} = 360°$

2. The maximum phase shift of the RC network as shown in Fig. 3.29 is

   (a) 90° (b) 180°

   (c) 270° (c) 360°

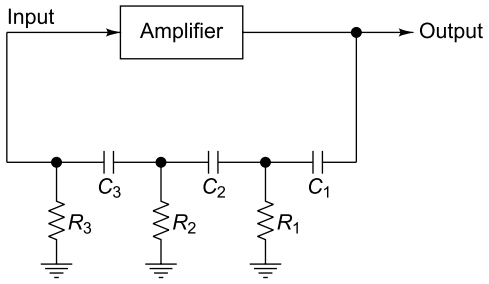


Fig. 3.29

   Answer: (b) 180°

3. Which of the following oscillators is used for generation of low frequencies?

   (a) RC phase shift oscillator (b) LC oscillator

   (b) Wein bridge oscillator (d) Blocking oscillator

   Answer: (a) RC phase shift oscillator

4. An oscillator is an amplifier that uses
   (a) positive feedback (b) negative feedback
   (b) degenerative feedback (d) differentiators and integrators
   Answer: (a) positive feedback
5. Wein bridge oscillator is a
   (a) sinusoidal oscillators (b) multivibrators
   (b) nonsinusoidal oscillators (d) relaxation oscillators
   Answer: (a) sinusoidal oscillators
6. The resonant frequency of a Wein bridge oscillator is about
   (a) 10 Hz (b) 10 kHz
   (c) 100 kHz (d) 10 MHz
   Answer: (b) 10 kHz
7. Which of the following statements is true of phase shift type and Wein-bridge type *RC* oscillators?
   (a) Both use positive feedback.
   (b) The phase shift type oscillator uses positive feedback only whereas a Wein-bridge oscillator uses both positive and negative feedback.
   (c) The phase shift type oscillator uses both positive and negative feedback whereas the Wein-bridge oscillator uses positive feedback only.
   (d) Both use negative feedback.
   Answer: (a) Both use positive feedback at oscillation.
8. The Barkhausen criterion for oscillations in a feedback amplifier at a particular frequency is
   (a) the magnitude of the loop gain must be equal to 1 and the phase shift must be 360°
   (b) the magnitude of the loop gain must be greater 1 when the phase shift is less than 360°
   (c) the magnitude of the loop gain must be greater than 1 when the phase shift is 180°
   (d) the magnitude of the loop gain must be less than 1 when the phase shift is 180°
   Answer: (a) the magnitude of the loop gain must be equal to 1 and the phase shift must be 360°
9. In a practical sinusoidal oscillator,
   (a) the magnitude of the loop gain is slightly greater than 1, and the amplitude of the oscillation is limited by circuit parameters
   (b) the phase shift of the loop gain is less than 360° and the oscillation frequency is variable with temperature
   (c) the magnitude of the loop gain is 1 and the phase shift is 180°
   (d) the magnitude of the loop gain is slightly greater than 1 and the phase shift is 180°
   Answer: (a) the magnitude of the loop gain is slightly greater than 1, and the amplitude of the oscillation is limited by circuit parameters

10. The frequency of oscillation of an *RC* phase shift oscillator is

(a) $f = \dfrac{1}{2\pi RC\sqrt{6}}$ (b) $f = \dfrac{1}{2\pi RC\sqrt{3}}$

(c) $f = \dfrac{1}{2\pi RC\sqrt{16}}$ (d) $f = \dfrac{1}{2\pi RC\sqrt{4}}$

Answer: (a) $f = \dfrac{1}{2\pi RC\sqrt{6}}$

11. In phase shift oscillator, the *RC* sections in the feedback path provide a phase shift of 180° and it is very difficult to design with bipolar transistors as
(a) the base current loads the phase shift *RC* network
(b) bipolar transistors have a current gain greater than 1
(c) the base-emitter voltage is about 0.7 V
(d) bipolar transistors provide a phase shift of 180° but not 360°

Answer: (a) the base current loads the phase shift *RC* network

12. The frequency of oscillation of a BJT *RC* phase shift oscillator is

(a) $f = \dfrac{1}{2\pi RC\sqrt{6}}$ (b) $f = \dfrac{1}{2\pi RC\sqrt{6+4K}}$

(c) $f = \dfrac{1}{2\pi RC\sqrt{6K+4}}$ (d) $f = \dfrac{1}{2\pi RC\sqrt{6-4K}}$

Answer: (b) $f = \dfrac{1}{2\pi RC\sqrt{6+4K}}$

13. Colpitts and Hartley oscillators are use the _____ feedback.
(a) voltage-series (b) current-series
(c) voltage-shunt (d) current-shunt

Answer: (a) voltage-series

14. In a Wein-bridge oscillator, the feedback factor β is

(a) $\beta = \dfrac{V_i}{V_o} = \dfrac{1}{\delta}$ (b) $\beta = \dfrac{V_i}{V_o} = \delta$

(c) $\beta = \dfrac{V_i}{V_o} = \dfrac{1}{\delta^2}$ (d) $\beta = \dfrac{V_i}{V_o} = \delta^2$

Answer: (a) $\beta = \dfrac{V_i}{V_o} = \dfrac{1}{\delta}$

15. A quartz crystal is widely used in the design of sinusoidal oscillators as
(a) the crystal is corresponding to a very high *Q*, LC-tuned circuit and its characteristics are stable with respect to temperature and time
(b) when pressure is applied to the crystal, it generates electrical oscillations
(b) the crystal provides accurate positive feedback
(c) piezoelectric properties of quartz crystal provide very low *Q*, *LC*-tuned circuit

Answer: (a) the crystal is corresponding to a very high *Q*, LC-tuned circuit and its characteristics are stable with respect to temperature and time

16. The frequency of oscillation of a Hartley oscillator is

(a) $f = \dfrac{1}{2\pi\sqrt{L_{eq}C}}$ (b) $f_o = \dfrac{1}{2\pi\sqrt{LC_{eq}}}$

(c) $f = \dfrac{1}{2\pi RC\sqrt{6}}$ (d) $f = \dfrac{1}{2\pi RC}$

Answer: (a) $f = \dfrac{1}{2\pi\sqrt{L_{eq}C}}$

UNIVERSITY QUESTIONS WITH ANSWERS

Multiple-Choice-Type Questions

1. How many PN junctions does a UJT have?
   (a) 0 (b) 1
   (c) 2 (d) 3 [WBUT-2008]
2. UJT is used as
   (a) rectifier (b) voltage follower
   (c) relaxation oscillator (d) none of these [WBUT-2008]
3. The phase difference between the input and output voltages in a common base arrangement is
   (a) 180° (b) 90°
   (c) 0° (d) 270° [WBUT-2009]

   Solution: 1. (b) 1; 2. (c) relaxation oscillator; 3. (a) 180°

Short- and Long-Answer-Type Questions

1. (a) Discuss the effect of positive feedback in an amplifier.
   (b) State and expain Barkhausen criterion. [WBUT-2003]

   Solution:

   (a) The effects of positive feedback in an amplifier are
   - Increase the gain of the amplifier
   - Reduce the bandwidth
   - Increase the distortion
   - Increase nose
   - Increase the instability

   (b) **Barkhausen Criterion** In a positive feedback amplifier, the overall voltage gain of positive feedback amplifier is given by

$$A_f = \frac{A}{1 - \beta A}$$

   where A is the gain of an amplifier without feedback or open-loop gain
   βA is the product of feedback amplifier and open loop gain.

   When βA is equal to one, the denominator becomes zero and the A_f will increase to infinity. But practically, the output of feedback amplifier

cannot be infinite. Consequently, $1 - \beta A = 0$ represents that the frequency of output voltage is completely different from input voltage. Therefore, the positive feedback amplifier circuit stop functioning as an amplifier but it starts to oscillate. So that the condition of oscillation is that $\beta A = 1$.

An amplifier circuit reverses the phase of input voltage at its output. Hence, there is 180° phase shift between input voltage and output voltage. In positive feedback circuit, the feedback networks provide a phase shift of 180° and generate a signal with 0° or multiple of 360° at the amplifier input.

When the positive feedback circuit has the following conditions:

(i) $\beta A = 1$ and
(ii) the total phase shift around the loop is 0° or multiple of 360°,

it behaves as an oscillator. The above conditions for oscillation are called *Barkhausen Criterion for oscillation.* As βA is a complex quantity, mathematically the Barkhausen Criterion is represented by

$$\beta A = 1 + j0$$

or, $\beta A = 1$ and $\angle \beta A = 0°$ or multiple of 360°

In an oscillator, the value of βA must be exactly unity but it is not practicable for implementation. Therefore, for all practical oscillator, the value of βA is slightly greater than unity.

2. What is the main application of positive feedback? [WBUT-2005]

Solution: The main application of positive feedback is OSCILLATOR

3. Write a short not on Barkhausen conditions of oscillation in electronic system. [WBUT-2005] [WBUT-2006] [WBUT-2007]

Solution: Refer Section 3.4.

4. (a) Discuss the basic structure of an UJT and explain its *V-I* characteristics.
   (b) Draw the circuit of relaxation oscillator using UJT. [2007] [2008]

Solution: A UJT is a *three-terminal* semiconductor device (Emitter *E*, Base B_1 and Base B_2) as shown in Fig. 3.30(a) and (b). It is formed from a lightly doped slab of *n*-type material which has high resistance. The two base contacts are made at each end of one side of the slab and aluminum rod is inserted on the other side to form a *single p-n junction*. Therefore, UJT is called as uni-junction. The aluminum rod is located near to the base terminal 2 (B_2). The B_2 is positive with respect to B_1 by voltage V_{BB}. The symbol of a UJT is shown in Fig. 3.31(a).

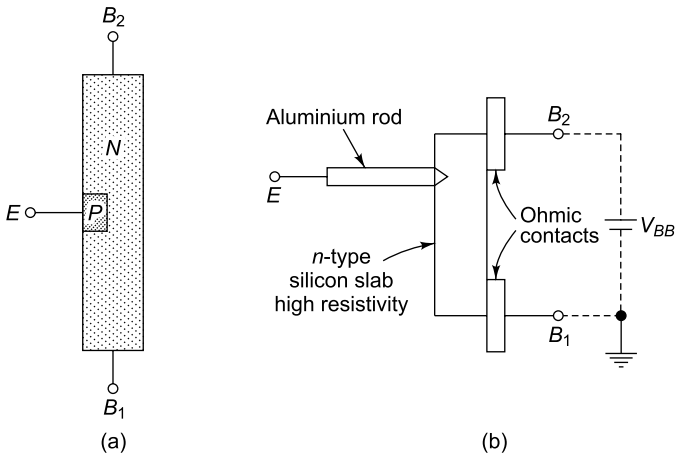


Fig. 3.30 *The basic structure of an UJT*

Figure 3.31(b) shows the equivalent circuit of the UJT. The diode represents the *p-n* junction, R_{B1} is a variable resistance, and R_{B2} is a fixed resistance. The value of R_{B1} decreases when emitter current increases. The R_{B1} varies from 50 kΩ to 50 Ω when emitter current I_E changes from 0 to 50 mA.

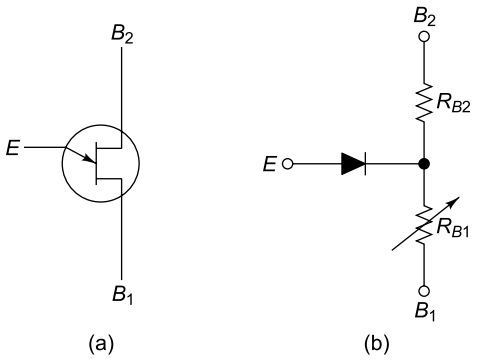


Fig. 3.31 *(a) Symbol of UJT (b) Equivalent circuit of the UJT*

The inter-base resistance between B_1 and B_2 is expressed as

$RB_B = R_{B1} + R_{B2}$ and it's range is approximately 4 kΩ to 10 kΩ.

When $I_E = 0$, the voltage across R_{B1} is

$$V_{R_{B1}} = \frac{R_{B1}}{R_{B1} + R_{B2}} V_{BB} = \eta V_{BB}$$

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} \text{ is intrinsic stand-off ratio.}$$

Actually the intrinsic stand-off ratio is controlled by the location of the aluminum rod.

The emitter threshold potential is

$$V_P = \eta V_{BB} + V_D$$

The *V-I* characteristics of a UJT is depicted in Fig. 3.32 when V_E crosses the threshold potential V_P, the emitter fires and holes are injected into the *n*-type slab through the *p*-type rod. Therefore, the hole content of the *n*-type slab increases. Consequently, the number of free electrons increases and hence conductivity increased. Thus V_E drops off while increasing I_E. The UJT operates in the negative resistance region as depicted in Fig. 3.32. The UJT passes through the valley point (I_V, V_V) and then becomes saturated.

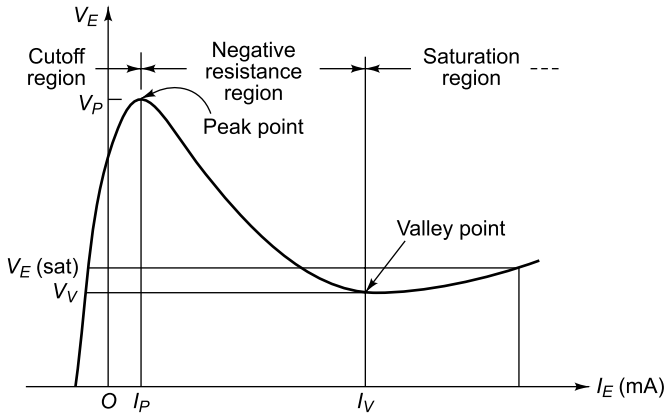


Fig. 3.32 ***V-I characteristics of a UJT***

(b) The *relaxation oscillator* is an oscillator using UJT which can generate sawtooth waveform. The UJT relaxation oscillators store energy in a capacitor and then dissipate that energy repeatedly to set-up the oscillations. For example, the capacitor can be charged toward a positive power supply until it reaches a threshold voltage sufficiently close to the supply. When the capacitor reaches each threshold, capacitor can be quickly discharged due to short. In all such capacitor-based relaxation oscillators, the period of the oscillations is set by the dissipation rate(s) of the capacitor. The UJT relaxation oscillators consist of a UJT, capacitor C which is charged through resistance R_E. Figure 3.33 shows the UJT relaxation oscillator.

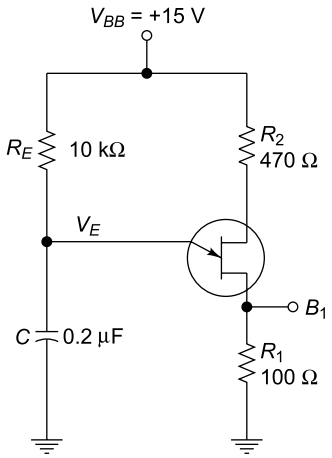


Fig. 3.33 ***Relaxation oscillator***

The voltage across the capacitor increases exponentially and when capacitor voltage reaches the peak point voltage V_P, the UJT starts

conducting and the capacitor voltage is discharged rapidly through R_{B1} and R_1. When the capacitor voltage is reached at the peak point voltage of UJT, UIT provides negative resistance to the discharge path of capacitor which is useful in the working of the relaxation oscillator. When the capacitor voltage is reached at V_V, the capacitor C starts to charge again. This cycle is repeated continuously generating a saw-tooth waveform across C.

The capacitor is charged and discharged cyclically as depicted in Fig. 3.34 V_C is the voltage across capacitor. The charging time constant of capacitor is RC. At time t_1, $V_C = V_P$, the UJT is turned ON and the capacitor discharges through R_1 for t_2 duration until reaches valley point voltage V_V. When UJT reaches the valley point, it becomes open circuit and capacitor starts to charge again.

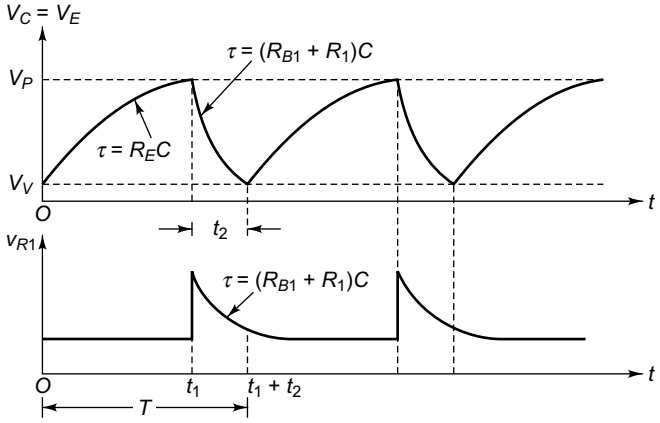


Fig. 3.34 ***Waveforms of V_C and V_{R1}***

The total cycle time $T = t_1 + t_2$.

Charging time of capacitor $t_1 = R_E C \ln\left(\frac{V - V_V}{V - V_P}\right)$

Discharging time of capacitor $t_2 = (R_{B1} + R_1)C \ln\left(\frac{V_P}{V_V}\right)$

Time period $T = t_1 + t_2$

The oscillation frequency is $f = \frac{1}{T} = \frac{1}{t_1 + t_2} = \frac{1}{R_E C \ln\left(\frac{1}{1-\eta}\right)}$ as $t_1 >> t_2$

5. Draw the volt-ampere characteristics of UJT and explain the reason for valley point in UJT characteristics. [WBUT-2007]
   Solution: Refer Solution of Question 4.
6. Write a short note on UJT and saw-tooth generator using UJT. [WBUT-2008] [WBUT-2010]
   Solution: Refer Solution of Question 4.

4 OPERATIONAL AMPLIFIER

4.1 INTRODUCTION

Commonly used semiconductor (solid state) devices are transistors (BJTs), diodes, and FETs. Any electronic circuit is formed when solid state devices or components are interconnected. This circuit is known as a *discrete circuit*. In this circuit, components are separable. An *integrated circuit* (IC) is a semiconductor wafer on which thousands or millions of tiny resistors, capacitors, diodes and transistors are fabricated. Sometimes, an IC is called a *chip* or microchip. The first integrated circuit was developed in the 1950s by Jack Kilby of Texas Instruments and Robert Noyce of Fairchild Semiconductor. An IC can function as an amplifier, oscillator, gate, flip-flop, timer, counter, computer memory, or microprocessor, etc. Depending on applications and type of signal process, ICs are categorized as

- *Linear* (analog) ICs
- *Digital* ICs

Based on application requirements, two distinctly different IC technologies such as monolithic technology and hybrid technology have been developed.

In *monolithic ICs*, all active and passive elements of any electronic circuit such as resistors, capacitors, diodes and transistors, and their interconnections are manufactured into a single chip of silicon. When identical circuits are required in very large quantities, monolithic ICs are manufactured at very low cost and high reliability.

In *hybrid ICs*, separate components are attached to a ceramic substrate and interconnected by wire or metallization pattern. Depending upon the active devices used in ICs, It can be classified as bipolar ICs using BJT and unipolar ICs using FET. Figure 4.1 shows the classification of ICs.

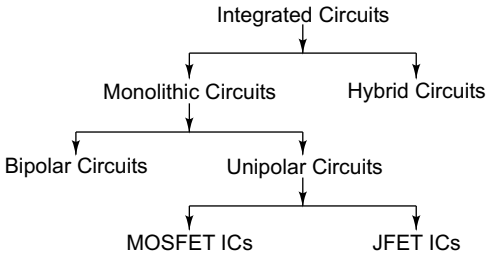


Fig. 4.1 *Classification of ICs*

The integrated circuits have a number of distinct advantages over discrete circuits. The advantages of ICs are as follows:

(i) Its size is small; due to miniaturization, the density of components is increased. It is possible to incorporate about 20,000 components per square inch
(ii) Improved performance as complex circuits are fabricated for better performance
(iii) Low cost due to batch processing
(iv) Reliability is high
(v) Less power consumption
(vi) Higher operating speed due to absence of parasitic capacitance effect
(vii) Matched devices
(viii) Less weight
(ix) Easy replacement

The limitations of ICs are as follows:

(i) Due to small size, ICs are unable to dissipate large amount of power. If the current flow in the IC is increased, more heat will be generated in the IC and the device may be damaged.
(ii) Inductance and transformers cannot be incorporated in ICs.

The integration of solid state technology has progressed day by day. Based on level of integration, integrated circuits are often classified by the number of transistors and other electronic components they contain. The ICs are classified as SSI (small-scale integration), MSI (medium-scale integration), LSI (large-scale integration), VLSI (very large-scale integration) and ULSI (ultra large-scale integration). SSI chips have up to 100 transistors per chip, MSI chips have 100 to 1000 transistors per chip, LSI chips have 1000 to 20,000 transistors per chip, VLSI chips have 20,000 to 1000,000 transistors per chip and ULSI chips have 10^6 to 10^7 transistors per chip. Table 4.1 shows the different types of ICs with their applications.

Table 4.1 *Types of integrated circuits*

Type of ICs	*SSI*	*MSI*	*LSI*	*VLSI*	*ULSI*
No. of transistors	Up to 100 transistors per chip	100 to 1000 transistors per chip	1000 to 20,000 transistors per chip	20,000 to 1000,000 transistors per chip	10^6 to 10^7 transistors per chip
No. of gates	Up to 30 gates per chip	30 to 300 gates per chip	300 to 3000 gates per chip	More than 3000 gates per chip	
Applications	Logic gates, flip-flops	Adders, Multiplexers, Counters	RAM, ROM, 8-bit microprocessor	16-bit and 32-bit microprocessor	Special processors sensors
Year of Development	1960-65	1965-70	1970-80	1980-90	1990-2000

ICs are also classified as linear ICs and digital ICs based on type of signals. Linear (analog) ICs operate on continuous or analog signals and the output signal is also continuous and depends on the input-signal level. Therefore, the output-signal level is a linear function of the input-signal level in linear ICs. Linear ICs are most commonly used as Audio-Frequency (AF) and Radio-Frequency (RF) amplifiers. The examples of linear ICs are OPAM, voltage regulators, comparators, and timers.

Digital ICs operate on discrete signals. The fundamental building blocks of digital ICs are logic gates, which work with binary data, either 0 V (logic 0) or + 5 V (logic 1). Digital or discrete ICs are logic gates, flip-flops, counters, memory, microprocessors, computers, computer networks, and modems.

The *operational amplifier* (OP-AMP) is a common device in audio-frequency (AF) and radio-frequency (RF) amplifiers applications. In this chapter, operation of OP-AMPs, symbol, equivalent circuit, voltage transfer curve, internal circuit diagram, and specification of OP-AMPs are explained in detail.

4.2 THE IDEAL OP-AMP

An ideal OP-AMP would exhibit the following characteristics.

(i) Infinite open loop voltage gain $A = \infty$

(ii) Infinite input resistance, $R_i = \infty$. Therefore, any input signal can drive it and there is no-loading on the preceding stage.

(iii) Zero output resistance $R_o = 0$. So that the output can drive an infinite number of the devices.

(iv) Infinite bandwidth, $BW = \infty$ so that any frequency signal from 0 to ∞ Hz can be amplified without attenuation.

(v) Infinite common mode rejection ratio, CMRR = ∞ so that output common mode noise voltage is zero.

(vi) Infinite slew rate, SR = ∞ so that output voltage changes occurs simultaneously with input voltage changes.

In practice, remove, the above characteristics of OP-AMPs can never be realized. An ideal OPAMP simplifies the mathematical representation of any OP-AMP circuit. The practical OP-AMP can be made close to ideal values as given in Table 4.2.

Table 4.2 *Characteristics of OP-AMPs*

Property	*Ideal*	*Practical*	*Typical Value*
Open loop gain	Infinite	Very high	2×10^5
Input resistance	Infinite	High	2 MΩ
Output resistance	Zero	Low	75 Ω
CMMR	Infinite	High	90 dB
Bandwidth	Infinite	Very high	Dominant pole 10 Hz

4.3 EQUIVALENT CIRCUIT OF AN OP-AMP

A equivalent circuit of an OP-AMP with finite input and out resistances is shown in Fig. 4.2. This circuit incorporates important values such as A, R_i, and R_o from the manufacturer's, data sheet.

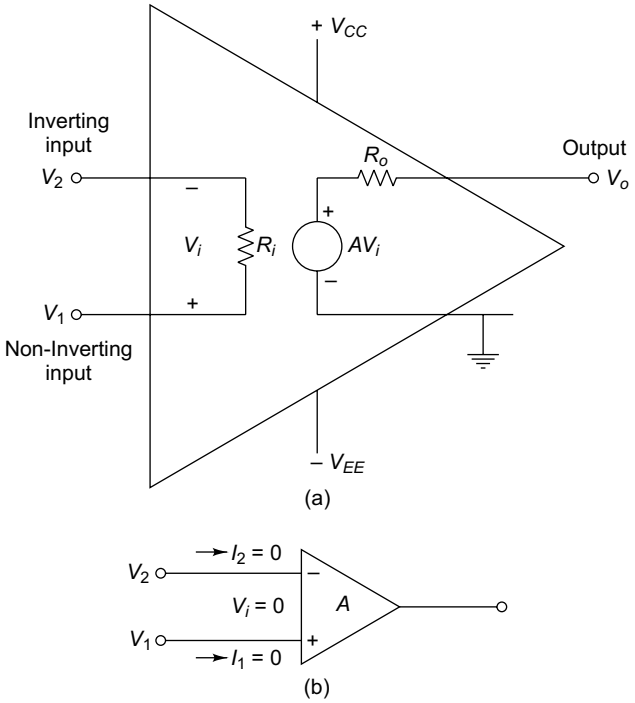


Fig. 4.2 ***Equivalent circuit of an OP-AMP***

In this figure,

AV_i is a Thevenin equivalent voltage source

R_o is the Thevenin equivalent resistance looking from the output terminal of an OP-AMP

V_i is difference input voltage

R_i is input resistance

V_O is output voltage

V_1 is voltage at non-inverting terminal with respect to ground

V_2 is voltage at inverting terminal with respect to ground

Assuming OP-AMP characteristics are close to the ideal characteristics, the following conditions prevail at the input side of the OP-AMP.

- As $R_i = \infty$, current input into inverting and non-inverting terminals is approximately zero as shown in Fig. 4.2(a).
- As $A = \infty$, for any finite output voltage V_o, $V_i = V_- - V_+ = 0$. Hence the inverting and non-inverting terminals should have the same potential.

The output voltage V_o can be expressed as

$$V_o = AV_i = A(V_1 - V_2)$$

Therefore, the output voltage V_o is directly proportional to the difference between two input voltages V_1 and V_2 or the operational amplifier amplifies the difference between two input voltages. The polarity of output voltage depends on the polarity of the difference voltage, $V_1 - V_2$.

4.4 IDEAL VOLTAGE TRANSFER CURVE

The basic OP-AMP equation $V_o = AV_i$ is justified when the output off-set voltage is assumed to be zero. This equation is very useful to study the OP-AMPs characteristics and to analyze different circuit configurations that employ feedback. Figure 4.3 shows the graphical representation of the equation, where x-axis represents input difference voltage V_i and y-axis represents output voltage V_o and gain A is constant.

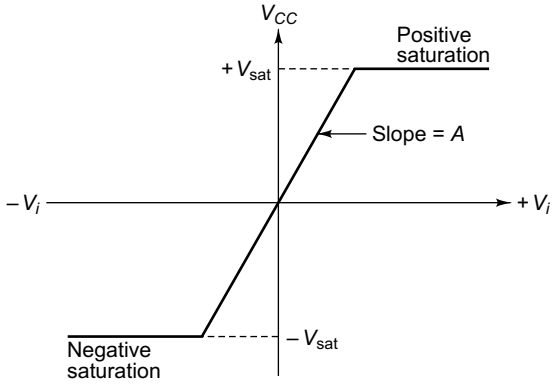


Fig. 4.3 ***Voltage transfer curve***

It is clear from Fig. 4.3 that the output voltage cannot exceed the positive saturation voltage $+V_{sat}$ and negative saturation voltage $-V_{sat}$. The $+V_{sat}$ and $-V_{sat}$ voltages are specified by an output voltage swing rating of the OP-AMP for given values of supply voltages. Therefore, the output voltage is directly proportional to V_i only until it reaches the saturation voltages and thereafter output voltage is constant either $+V_{sat}$ or $-V_{sat}$ depending upon the magnitude of V_i.

Figure 4.3 is called an ideal voltage transfer curve as output offset voltage V_{os} is assumed to be zero. In a negative feedback OP-AMP circuit, this voltage is approximately zero. This figure is not drawn according to scale. If it is drawn as per scale considering the very high value of A, the curve would be almost vertical.

4.5 OP-AMP SYMBOL AND TERMINALS

Figure 4.4 shows the symbol of an operational amplifier. The pin diagram of OP-AMP is depicted in Fig. 4.5(a). It is available in-duel-in line plastic package as shown in Fig. 4.5(b). Usually, it is indicated by a triangle with basic five terminals. The five basic terminals are as follows:

(i) Positive supply voltage terminal, $+V_{CC}$ (7)
(ii) Negative supply voltage terminal, $+V_{EE}$ (4)
(iii) Output terminal voltage, V_O (6)
(iv) Inverting input terminal (2)
(v) Non-inverting input terminal (3)

The other terminals are terminal (1) and terminal (5) which are used as null offsets. The terminal (8) is used as NC (no connection).

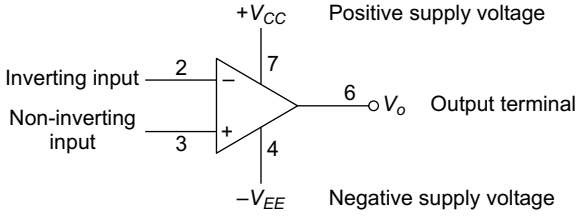


Fig. 4.4 *Symbol of OP-AMP*

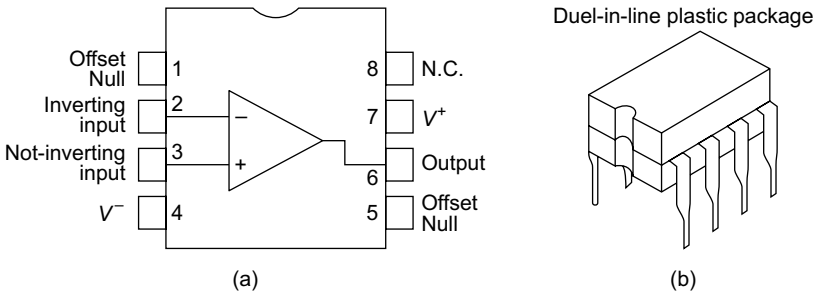


Fig. 4.5 *(a) Pin diagram of OP-AMP in mini DIP*
(b) Duel-in-line plastic package of OP-AMP

4.6 DIFFERENCE AMPLIFIER

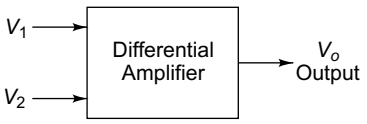


Fig. 4.6 *Difference amplifier*

Figure 4.6 shows a difference amplifier where V_1 and V_2 are voltage inputs and V_o is the output voltage. Assume it is formed by a linear active device and this linear active device is an ideal one for analysis of the difference amplifier. A difference amplifier can be defined as an ideal one if any signal, which is common to both inputs, has no effect on the output voltage.

The output voltage of difference amplifier is

$$V_o = A_d(V_1 - V_2)$$

where, A_d is the gain of difference amplifier.

If input voltage V_1 = input voltage V_2, output voltage $V_o = 0$. Actually, the signal common to both inputs gets cancelled and generates zero output voltage. This is only possible for an ideal operational amplifier. But the practical difference amplifier does not follow the above equation as the output voltage depends not only upon the difference signal V_d but also depends upon the average voltage of the input signals, V_C which is called the common mode signal. For example, the output voltage V_o with input voltages $V_1 = 200$ μV and $V_2 = 100$ μV will be different from the output voltage V_o with input voltages $V_1 = 1000$ μV and $V_2 = 900$ μV, even though the difference signal $(V_1 - V_2) = 100$ μV.

The common mode signal is $V_C = \frac{V_1 + V_2}{2}$

In any differential amplifier, the circuit is symmetric, but due to parameter mismatch, the gain at the output with respect to the positive terminal is different in magnitude to that of the negative terminal. Therefore, if the same voltage is applied to both terminals, the output is not zero.

Then output voltage can be expressed as

$$V_o = A_1 V_1 + A_2 V_2$$

where, V_i is amplified by A_1 and V_2 is amplified by A_2

At that moment, $2V_C = V_1 + V_2$ and

$$V_d = V_1 - V_2$$

Then $2V_C + V_d = 2V_1$

or, $$V_1 = V_C + \frac{1}{2} V_d$$

The input voltage is $V_2 = V_1 - V_d$

$$= V_C + \frac{1}{2} V_d - V_d = V_C - \frac{1}{2} V_d$$

The output voltage is $V_o = A_1 V_1 + A_2 V_2$

$$= A_1 \left(V_C + \frac{V_d}{2} \right) + A_2 \left(V_C - \frac{V_d}{2} \right)$$

$$= \left(A_1 + A_2 \right) V_C + \frac{A_1 - A_2}{2} V_d$$

$$= A_C V_C + A_d V_d$$

Here, common mode gain $A_C = A_1 + A_2$ and differential mode gain $A_d = \frac{A_1 - A_2}{2}$

4.6.1 Common Mode Rejection Ratio

The relative sensitivity of an operational amplifier to a difference signal as compared to a common mode signal is known as Common Mode Rejection Ratio (CMRR). CMRR can be defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_C. It can be expressed as

$$\text{CMRR} = \rho = \left| \frac{A_d}{A_C} \right|$$

Usually, CMRR is expressed in decibels (dB) as $\text{CMRR} = 20 \log \left| \frac{A_d}{A_C} \right|$ dB

The output voltage can be expressed in terms of CMRR is

$$V_o = A_d V_d + A_C V_C$$

$$= A_d V_d \left(1 + \frac{A_C V_C}{A_d V_d} \right)$$

$$= A_d V_d \left(1 + \frac{1}{\frac{A_d}{A_c}} \frac{V_C}{V_d} \right)$$

$$= A_d V_d \left(1 + \frac{1}{CMRR} \frac{V_C}{V_d} \right) \quad \text{as} \quad \text{CMRR} = \frac{A_d}{A_c} = \rho$$

$$= A_d V_d \left(1 + \frac{1}{\rho} \frac{V_C}{V_d} \right)$$

It is clear from the above equation that ρ must be large compared to the ratio of the common mode signal to the difference mode signal as there is always some noise signals on the signal lines. In addition, it is undesirable that the amplification of noise signal will be present in the output signal. The differential amplifier is able to virtually eliminate the noise signal.

4.1 Calculate the common mode gain of an operational amplifier for the following parameters:

The differential voltage gain $A_d = 10^4$ and common mode rejection ratio CMRR = 2000.

Solution

Given $A_d = 10^4$ and CMRR = 2000.

The Common Mode Rejection Ratio (CMRR) can be expressed as

$$\text{CMRR} = \rho = \left| \frac{A_d}{A_C} \right|$$

Then common mode gain $A_C = \dfrac{A_d}{\text{CMRR}} = \dfrac{10^4}{2000} = 5.$

4.2 Calculate the output voltage of a differential amplifier for the following parameters:

$V_1 = 1000$ μV, $V_2 = 500$ μV, $A_d = 1000$ and ρ = CMRR = 2000

Solution

Given $V_1 = 1000$ μV, $V_2 = 500$ μV, $A_d = 1000$ and ρ = CMRR = 2000

The common mode signal is

$$V_C = \frac{V_1 + V_2}{2} = \frac{1000 + 500}{2} \text{ μV} = 750 \text{ μV}$$

The difference signal V_d is

$$V_d = V_1 - V_2 = (1000 - 500) \text{ μV} = 500 \text{ μV}$$

The output voltage is

$$V_o = A_d V_d \left(1 + \frac{1}{\rho} \frac{V_C}{V_d} \right)$$

$$= 1000 \times 500 \times 10^{-6} \left(1 + \frac{1}{2000} \frac{750}{500} \right) = 500.375 \text{ mV}$$

4.3 The common mode rejection ratio CMRR of an operational amplifier is about 120 dB and difference mode voltage gain is 10,000. Determine common mode gain.

Solution

Given A_d = 10,000, CMRR = 120 dB

The common mode rejection ratio in dB can be expressed as

$$\text{CMRR} = 20\log\frac{A_d}{A_C} = 20(\log A_d - \log A_C)$$

$$= 20 \log 10000 - 20 \log A_C$$

$$= 80 - 20 \log A_C = 120$$

Therefore, $20 \log A_C = 120 - 80 = 40$ dB

The common mode gain is

$$A_C = \text{Anti log}\left(\frac{40}{20}\right) = 100.$$

4.4 The input signals of a differential amplifier are V_1 = 50 μV and V_2 = – 25 μV.

(a) When the common mode rejection ratio is 50, determine the output voltage of the differential amplifier.

(b) If ρ = 10,000, find the output voltage.

Assume difference mode gain A_d = 20,000

Solution

Given V_1 = 5 μV, V_2 = – 25 μV and common mode rejection ratio CMRR = 50

(a) The common mode signal is

$$V_C = \frac{V_1 + V_2}{2} = \frac{50 - 25}{2}\,\mu\text{V} = 12.5\ \mu\text{V}$$

The difference signal is

$$V_d = V_1 - V_2 = 50 - (-25)\ \mu\text{V} = 75\ \mu\text{V}$$

The output voltage is

$$V_o = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$$

$$= 20000 \times 75 \times 10^{-6}\left(1 + \frac{1}{50}\frac{12.5}{75}\right) = 1505\ \text{mV}$$

(b) if ρ = 10,000, the output voltage is

$$V_o = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$$

$$= 20000 \times 75 \times 10^{-6}\left(1 + \frac{1}{10000}\frac{12.5}{75}\right)$$

$$= 1500.025\ \text{mV}$$

4.5 In a differential amplifier, the input voltages are

$V_1 = 10 \sin(2\pi \times 25t) + 5 \sin(2\pi \times 1000t)$ mV and $V_2 = 10 \sin(2\pi \times 25t) - 5 \sin(2\pi \times 1000t)$

The common mode gain in ac is = 0.5 and difference mode gain A_d = 100. Determine (a) V_{O1} (b) V_{O2} (c) V_O. Assume a 25 Hz signal is a noise signal and 1000 Hz frequency signal will be processed.

Solution

(a) The common mode signal is

$$V_C = \frac{V_1 + V_2}{2} = 10 \sin(2\pi \times 25t) \text{ mV}$$

The difference signal is

$$V_d = V_1 - V_2 = 10 \sin(2\pi \times 1000t) \text{ mV}$$

The output voltage is

$$V_{O1} = A_d V_d + A_C V_C$$
$$= 100 \times 10 \sin(2\pi \times 1000t) + 0.5 \times 10 \sin(2\pi \times 25t) \text{ mV}$$

(b) The output voltage is

$$V_{O2} = -A_d V_d + A_C V_C$$
$$= -100 \times 10 \sin(2\pi \times 1000t) + 0.5 \times 10 \sin(2\pi \times 25t) \text{ mV}$$

(c) The output voltage is

$$V_O = V_{O1} - V_{O2}$$
$$= 2 \times 100 \times 10 \sin(2\pi \times 1000t) \text{ mV}$$
$$= 2 \sin(2\pi \times 1000t) \text{ V}$$

4.7 OPERATIONAL AMPLIFIER INTERNAL CIRCUIT

The block diagram of a typical operational amplifier is shown in Fig. 4.8. Usually, an operational amplifier consists of four cascaded blocks. The first two stages are cascaded differential amplifiers, which are used to provide high gain and high input resistance. The third stage works as a buffer as well as a level shifter. Actually, the buffer is an emitter follower. Its input impedance is very high hence it prevents loading of the high-gain stage. The level shifter adjusts the dc voltages and the output voltage is zero for zero inputs. As the gain stages are direct coupled, the adjustment of dc level is required.

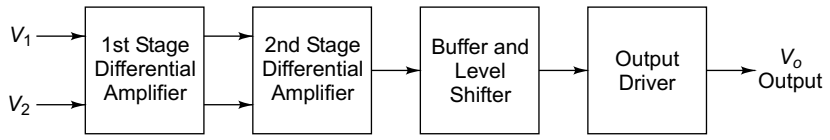


Fig. 4.7 ***Block diagram representation of OP-AMP internal circuit***

The output is used to provide low output impedance as demanded by the ideal characteristics of OP-AMP. The output voltage should swing symmetrically, in between $+V_{sat}$ and $-V_{sat}$. For this swing, the amplifier is provided with positive and negative supply voltages (±15 V).

In the first-stage differential amplifier, there are two inputs and balanced differential output. In this stage, maximum voltage gain is provided and also establishes the very high input impedance of operational amplifier. This stage should have the following characteristics:

- Very high input impedance about 10 MΩ
- High CMRR about 120 dB
- Very high open loop gain about 10^5
- Low input bias current about 0.5 μA
- Small input offset current about 0.2 mA
- Small input offset voltage about 10 mV

In the second-stage differential amplifier, there are two inputs and an unbalanced output differential amplifier. In this stage, the overall gain of the operational amplifier increases. Due to direct coupling between first-stage and second-stage differential amplifiers, the dc level at the output of the second-stage differential amplifier is much higher than the ground potential. Consequently, a level translator must be used in the next stage in order to bring the dc level back to the ground potential.

Generally, the third stage OP-AMP internal circuit is buffer and level shifter. This stage is used to shift the dc level to zero volts with respect to the ground. Usually, an emitter follower circuit is in this stage to provide low output resistance, and class B and class AB amplifiers are used to provide large output power. The last stage is the output driver circuit. In this stage, a complementary symmetry push-pull amplifier is used. The output stage should have the following characteristics:

- Low output impedance
- Large output voltage swing capability
- Large output current swing capability
- Short circuit protection

4.7.1 Differential Amplifier

The differential amplifier stages are used to provide high gain in the difference mode signal and cancel the common mode signal. The CMRR common mode rejection ratio is the relative sensitivity of an OP-AMP to a difference signal as compared to common mode signal, and CMRR is the advantages of the differential amplifier. If the CMRR value is very high, it is better for OP-AMP. An OP-AMP should have high input impedance.

A cascade dc amplifier can provide high gain down to zero frequency due to absence of a coupling capacitor. But this amplifier suffers from the drift of the operating point due to temperature dependency of I_{CBO}, V_{BE} and h_{fe} of transistors. This problem can be reduced by using differential amplifiers as depicted in Fig. 4.9. This is an emitter-coupled differential amplifier. This circuit has low drift due to symmetrical construction and can be designed in such a way that it provides high input resistance.

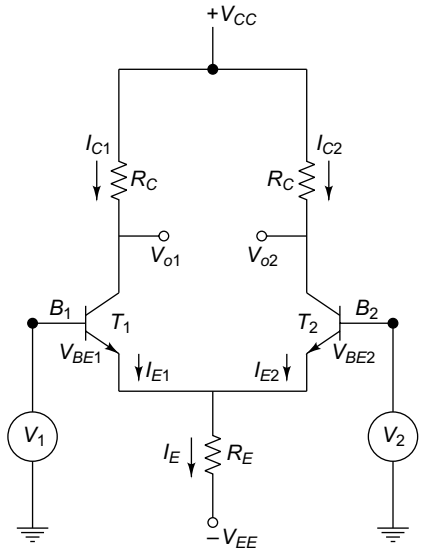


Fig. 4.8 ***Basic differential amplifier***

It has two input terminals B_1 and B_2. B_2 is the inverting terminal and B_1 is the non-inverting terminal. This amplifier can be used in four different configurations depending upon the input and output signals. These four different configurations are

(i) Differential input and differential output
(ii) Differential input and single ended output
(iii) Single input and differential output
(iv) Single input and single ended output

When a signal is applied to both the inputs, it is differential input and differences of signals applied to the two inputs are amplified.

Assume transistor bases B_1 and B_2 are joined together and connected to a voltage V_{CM} called the common mode voltage. It is clear from Fig. 4.9, $V_1 = V_2 = V_{CM}$. Transistors T_1 and T_2 are well matched and due to symmetry of the circuit, the current I_E divides equally through transistors T_1 and T_2. Therefore, the emitter current of T_1 is equal to emitter current of T_2.

Hence, $$I_{E1} = I_{E2} = \frac{I_E}{2}$$

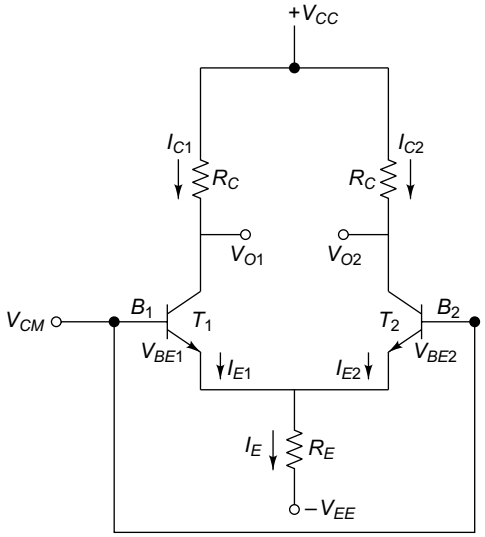


Fig. 4.9 ***Differential pair with a common-mode input signal V_{CM}***

The collector current I_{C1} and I_{C2} flow through the resistor R_C is $\alpha \frac{I_E}{2}$.

The voltage at each of the collectors will be

$$V_{CC} - \alpha \frac{I_E}{2} R_C$$

and the difference of the voltage between the two collectors, $V_{O1} - V_{O2}$ will be zero.

If the value of V_{CC} is changed, the output voltage across the two collectors will not be changed. Consequently, the differential pair will not respond to the common-mode input signals.

When the input voltage $V_2 = 0$ and input voltage $V_1 = 1$ V, Transistor T_1 will be ON and Transistor T_2 will be OFF as depicted in Fig. 4.10. Then the total current I_E will flow through T_1. As T_1 is ON, the voltage at emitter will be 0.3 V. As a result, the emitter-base junction of T_2 will be reversed biased and T_2 becomes

OFF. The collector voltage of T_1 is V_{O1} and will be $V_{o1} = V_{CC} - \alpha I_E R_C$ and collector voltage of T_2 is $V_{O2} = V_{CC}$. Therefore, it is clear from the above discussion that the differential pair only responds to difference mode signals and rejects common-mode signals.

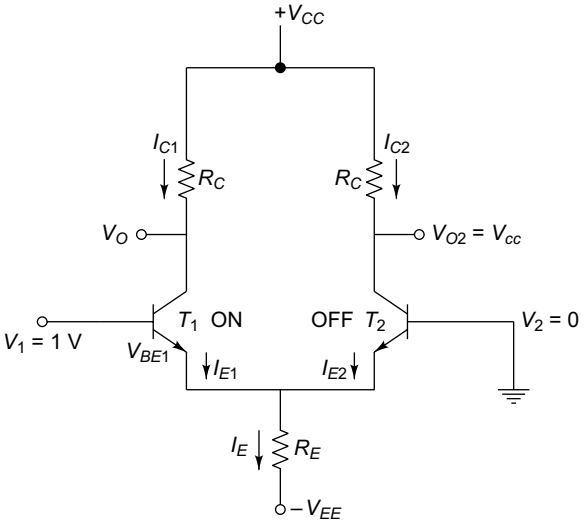


Fig. 4.10 ***Differential pair with large differential input signal***

Transfer Characteristics of Differential Amplifier

The collector currents for transistors T_1 and T_2 are I_{C1} and I_{C2} respectively. After neglecting the reverse saturation currents of the collector base junction, we obtain

The collector current for transistor T_1 is $I_{C1} = \alpha I_{ES} e^{\frac{V_{BE1}}{V_T}}$

The collector current for transistor T_2 is $I_{C2} = \alpha I_{ES} e^{\frac{V_{BE2}}{V_T}}$

where, I_{ES} is the reverse saturation current of emitter base junction.

The ratio of two collector currents is

$$\frac{I_{C1}}{I_{C2}} = \frac{\alpha I_{ES} e^{\frac{V_{BE1}}{V_T}}}{\alpha I_{ES} e^{\frac{V_{BE2}}{V_T}}} = e^{\frac{V_{BE1} - V_{BE2}}{V_T}}$$

KVL for loop equation for two emitter–base junctions is

$$V_1 - V_{BE1} + V_{BE2} - V_2 = 0$$

or, $$V_{BE1} - V_{BE2} = V_1 - V_2 = V_d$$

where, V_d is the difference of two input voltages.

The emitter current I_E is

$$I_E = I_{E1} + I_{E2}$$

$$= \frac{I_{C1}}{\alpha} + \frac{I_{C2}}{\alpha}$$

$$= \frac{I_{C1}}{\alpha}\left(1+\frac{I_{C2}}{I_{C1}}\right)$$

$$= \frac{I_{C1}}{\alpha}\left(1+e^{-\frac{V_d}{V_T}}\right)$$

Therefore, $I_{C1} = \dfrac{\alpha I_E}{1+e^{-\frac{V_d}{V_T}}}$ and $I_{C2} = \dfrac{\alpha I_E}{1+e^{-\frac{V_d}{V_T}}}$

The transfer characteristics for a difference amplifier (I_C vs V_d plot) is illustrated in Fig. 4.11. The following is clear from the transfer characteristics as depicted Fig. 4.10:

- If $V_d > 4V_T$ about 100 mV, $I_{C1} = \alpha I_E$ and $I_{C2} = 0$. Then output voltages are $V_{O1} = V_{CC} - \alpha I_E R_C$ and $V_{O2} = V_{CC}$
- If $V_d < -4V_T$ about –100 mV, $I_{C1} = 0$ and $I_{C2} = \alpha I_E$. The output voltage $V_{O1} = V_{CC}$ and V_{O2} is very small or negligible. Therefore, during $-4V_d < V_d < 4V_T$, the differential amplifier can acts as switch.
- When $V_d > \pm 4V_T$, the differential amplifier can acts as a very good limiter.
- $-2V_T < V_d < 2V_T$, difference amplifier can be function as linear amplifier.

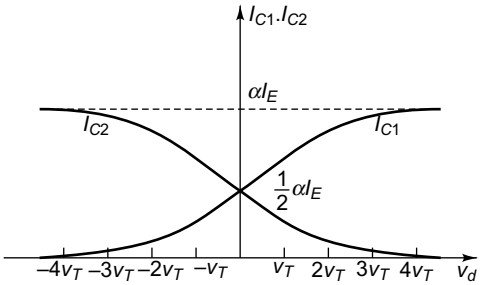


Fig. 4.11 *Transfer characteristics for difference amplifier*

4.6 The difference amplifier as shown in Fig. 4.12 has the following parameters:

$R_C = 10\ \text{k}\Omega$, $R_E = 100\ \text{k}\Omega$, $R_S = 10\ \text{k}\Omega$

The transistor parameters are as follows:

$h_{ie} = 10\ \text{k}\Omega$, $h_{fe} = 100$, $h_{re} = 0$, $h_{oe} = 0$

When the amplifier is operated with common mode signal of 50 mV and difference signal of 25 mV, determine output voltage and CMRR.

Solution

The difference gain is

$$A_d = -\frac{h_{fe}R_C}{2\left(R_S + h_{ie}\right)}$$

$$= -\frac{100 \times 100\ \text{k}\Omega}{2(10\ \text{k}\Omega + 10\ \text{k}\Omega)} = -250$$

The common mode gain is

$$A_C = -\frac{h_{fe}R_C}{R_S + h_{ie} + \left(1 + h_{fe}\right)2R_E}$$

$$= -\frac{100 \times 10\ \text{k}\Omega}{10\ \text{k}\Omega + 10\ \text{k}\Omega + \left(1 + 100\right)) \times 2 \times 100\ \text{k}\Omega} = -0.049$$

The output voltage is

$$V_O = A_d V_d + A_C V_C$$
$$= (-250) \times 25\ \text{mV} + (-0.49) \times 50\ \text{mV} = 6252.45\ \text{mV}$$

The common mode rejection ratio in dB is

$$\text{CMRR} = 20 \log \frac{A_d}{A_C} = 20 \log \frac{250}{0.049}\ \ 74.15\ \text{dB}$$

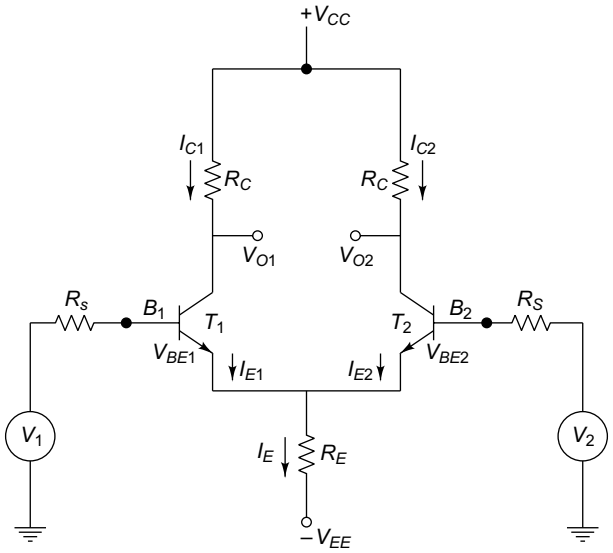


Fig. 4.12 ***Difference amplifier***

4.8 OPEN-LOOP CONFIGURATIONS OF OP-AMP

The open-loop configuration of operational amplifier means that there is no connection between the output and input terminals either direct or via another network. Therefore, the output signal is not feedback in any form as a part of the input signal, and the loop is open as there is no feedback.

During open-loop configuration, the operational amplifier simply works as a high gain amplifier. Usually, the open-loop configurations of OP-AMP are classified based on the number of inputs used and the terminal to which the input signal is applied. There are three different open-loop configurations of OP-AMP as given below:

(i) Differential Amplifier
(ii) Inverting Amplifier
(iii) Non-invert Amplifier

In this section, the above three configurations are explained elaborately.

4.8.1 Differential Amplifier

The circuit diagram of the open-loop differential amplifier is shown in Fig. 4.13. In this circuit diagram,

V_1 input signal is applied to non-inverting terminal

V_2 input signal is applied to inverting terminal

As the OP-AMP amplifies the difference between two input signals ($V_1 - V_2$), this circuit configuration is known as differential amplifier.

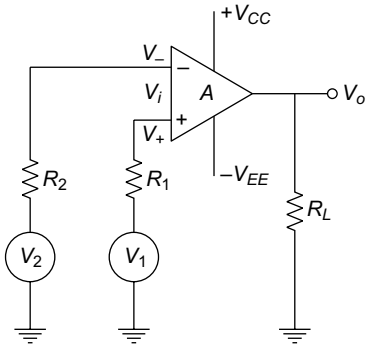


Fig. 4.13 *Open-loop difference amplifier*

As OP-AMP amplifies both ac and dc input signals, this device is called a *versatile device*. Therefore, input signal V_1 and V_2 will be either ac or dc voltages. R_1 and R_2 are the source resistances of supply voltage V_1 and V_2 respectively. The magnitude of R_1 and R_2 are very less value compared to the input resistance R_1. Consequently, the voltage drops across R_1 and R_2 can be assumed to be zero. Therefore, inverting terminal voltage $V_- = V_2$ and non-inverting terminal voltage $V_+ = V_1$.

The output voltage of OP-AMP is $V_o = A(V_+ - V_-)$
where, A is the open loop gain of OP-AMP.

After substituting the values of $V_+ = V_1$ and $V_- = V_2$, we get

$$V_o = A(V_1 - V_2)$$

From the expression $V_o = A(V_1 - V_2)$, we can state that the output voltage is equal to the voltage gain A times the difference between two input voltages ($V_1 - V_2$). It is also clear that the polarity of the output voltage is dependent on the polarity of the input difference voltage.

4.8.2 Inverting Amplifier

Figure 4.14 shows the open-loop configuration of the inverting amplifier. In this amplifier only one input signal is applied to the inverting input terminal. The non-inverting input terminal is grounded.

Therefore, $V_+ = 0$ and $V_- = V_2$.

Then output voltage is

$$V_o = A(V_+ - V_-) = A(0 - V_2) = -AV_2$$

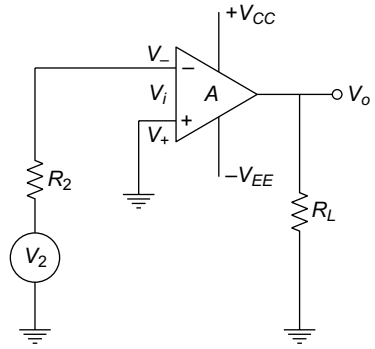


Fig. 4.14 *Inverting amplifier*

The negative sign indicates that output voltage is 180° out of phase with respect to input or output voltage has opposite polarity. In this way, the input signal is amplified by the open loop gain A and is also inverted at the output in the inverting amplifier.

4.8.3 Non-Inverting Amplifier

The open-loop configuration of non-inverting amplifier is depicted in Fig. 4.15. In this configuration, the input signal is applied to the non-inverting input terminal and inverting terminal is grounded.

Since $V_+ = V_1$ and $V_- = 0$, the output voltage is

$$V_o = A(V_+ - V_-) = A(V_1 - 0) = AV_1$$

Therefore, the input voltage V_1 is amplified by a gain A. The output voltage is greater than A and it is in phase with the input voltage.

In each open-loop configuration of operational amplifier, if any input signal is slightly greater than zero, the output voltage of operational amplifier will be at saturation level. These results are obtained from the very high gain A of operational amplifier. Hence, when OP-AMP operates in open loop configuration, the output of OP-AMP is either positive saturation voltage + V_{sat} or negative saturation $-V_{sat}$. Consequently, open-loop OP-AMPs are not used in linear applications.

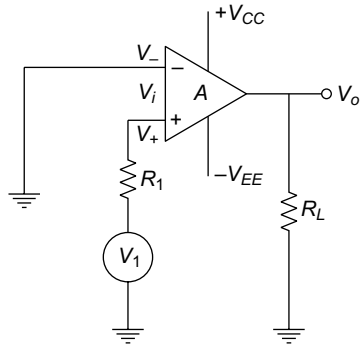


Fig. 4.15 *Non-inverting amplifier*

4.9 FEEDBACK IN IDEAL OP-AMP

The utility of OP-AMPs can be increased by using a negative feedback. In this case, the output voltage is not saturation voltage and the OP-AMPs behave as a linear device as the output voltage directly proportional to input voltages. There are two negative feedback circuits such as

(i) Inverting amplifier
(ii) Non-inverting amplifier

In this section, inverting as well as non-inverting amplifier are discussed assuming the following assumptions:

- The current drawn by either inverting or non-inverting terminals is negligible.
- The differential input voltage V_i between non-inverting and inverting terminals is approximately zero.

4.9.1 Inverting amplifier

Figure 4.16 shows inverting amplifier. The output voltage V_o is fed back to the inverting terminal through feedback resistance R_f and resistance R_1. The input voltage is applied to the inverting input terminal through resistance R_1. The non-inverting terminal is grounded.

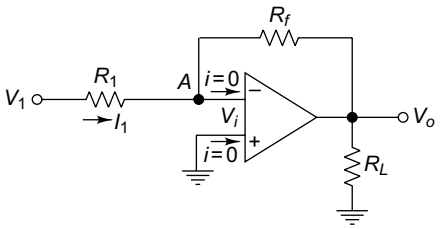


Fig. 4.16 *Inverting amplifier*

In an ideal amplifier, $V_i = 0$, $i = 0$ for simplifying the output voltage equation. But in practical OP-AMP, $V_i \neq 0$. The equivalent circuit of a practical inverting amplifier is shown in Fig. 4.17. This circuit can be simplified by thevenin's equivalent as depicted in Fig. 4.18 where, V_{eq} is Thevenin's equivalent voltage.

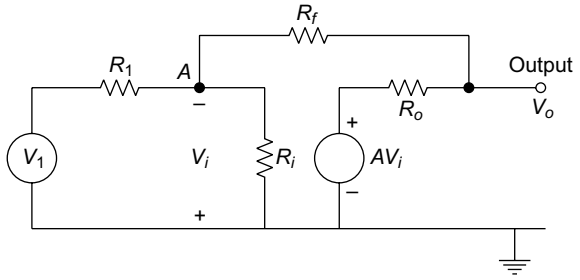


Fig. 4.17 *Equivalent circuit of inverting amplifier*

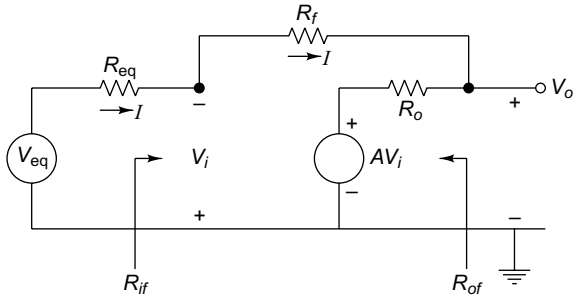


Fig. 4.18 *Thevenin's equivalent circuit of inverting amplifier*

The Thevenin's equivalent voltage is $V_{eq} = V_1 \dfrac{R_i}{R_1 + R_i}$

R_{eq} is Thevenin's equivalent resistance and $R_{eq} = R_i \parallel R_1 = \dfrac{R_1 R_i}{R_i + R_1}$

As $R_i >> R_1$, $R_{eq} = R_1$

$$V_{eq} = V_i \frac{R_i}{R_i + R_i} = V_i, \text{ as } R_i >> R_i$$

The loop equations are

$$V_o = IR_o + AV_i \tag{4.1}$$

and $V_i + IR_f + V_o = 0$

After substituting V_i in Eq. 4.1, we get

$$V_o = IR_o - A(IR_f + V_o)$$

or, $(1 + A)V_o = I(R_o - AR_f)$

The KVL equation is

$$V_{eq} = I(R_{eq} + R_f) + V_o = I(R_1 + R_f) + V_o \text{ as } R_{eq} = R_1$$

As $$I = \frac{(1 + A)V_o}{R_o - AR_f}$$

$$V_{eq} = V_1 = \frac{(1+A)V_o}{R_o - AR_f}(R_1 + R_f) + V_o$$
$$= \frac{(1+A)(R_1 + R_f) + R_o - AR_f}{R_o - AR_f} V_o$$
$$= \frac{(1+A)R_1 + R_f + R_o}{R_o - AR_f} V_o$$

Closed Loop Gain

The closed loop gain is $A_f = \frac{V_o}{V_1} = \frac{R_o - AR_f}{R_o + R_f + (1+A)R_1}$

As $A >> 1$ and $AR_1 >> R_o + R_f$, $AR_f >> R_o$

Therefore, $A_f = \frac{V_o}{V_1} = -\frac{R_f}{R_1}$

Then the output voltage is $V_o = -\frac{R_f}{R_1} V_1$

The negative sign indicates that there is 180° phase shift between V_1 and V_o.

When R_f is replaced by Z_f and R_1 is replaced by Z_1, we get $V_o = -\frac{Z_f}{Z_1} V_1$.

This expression can be used different OP-AMPs applications such as integrator and differentiator which are explained in Chapter 5.

Input Resistance

Input resistance of OP-AMP is $R_{if} = \frac{V_i}{I}$

The KVL loop equation is

$$V_i + I(R_f + R_o) + AV_i = 0$$

or, $$(1 + A)V_i + I(R_f + R_o) = 0$$

or, $$R_{if} = \frac{R_f + R_o}{1 + A}$$

Output Resistance

Output resistance is calculated from the open-circuit output voltage V_{OC} and short circuit output current I_{SC}

Output resistance is $R_{of} = \frac{V_{OC}}{I_{SC}}$

Figure 4.18 shows the equivalent circuit for calculating output resistance R_{of} when output is shorted.

Current $I_1 = \frac{V_{eq} - 0}{R_1 + R_f} = \frac{V_1}{R_1 + R_f}$ flows through R_{eq} and R_f

Current $I_2 = \dfrac{AV_i}{R_o}$, flows through R_o

$$V_i = -I_1 R_f,\ I_2 = -\frac{AR_f}{R_o} I_1 = -\frac{ARF}{R_o} I_1$$

The short circuit output current is

$I_{SC} = I_1 + I_2$ After substituting I_1 and I_2, we get

$$= \frac{V_1}{R_1 + R_f} - \frac{AR_f}{R_o} \frac{V_1}{R_1 + R_f}$$

$$= \frac{V_1}{R_o(R_1 + R_f)} (R_o - AR_f)$$

The open circuit output voltage is

$$V_{OC} = V_O = \frac{R_o - AR_f}{R_o + R_f + R_1 (1 + A)} V_1$$

The output impedance is

$$R_{of} = \frac{V_{OC}}{I_{SC}} = \frac{\dfrac{R_o - AR_f}{R_o + R_f + R_1 (1 + A)} V_1}{\dfrac{(R_o - AR_f) V_1}{R_o (R_1 + R_f)}}$$

$$= \frac{R_o - AR_f}{R_o + R_f + R_1 (1 + A)} \frac{R_o (R_1 + R_f)}{R_o - AR_f}$$

$$= \frac{R_o (R_1 + R_f)}{R_o + R_f + R_1 (1 + A)}$$

$$= \frac{R_o (R_1 + R_f)}{(R_o + R_1 + R_f) + AR_1}$$

$$= \frac{\dfrac{R_o (R_1 + R_f)}{(R_o + R_1 + R_f)}}{1 + A \dfrac{R_1}{(R_o + R_1 + R_f)}}$$

The numerator is $R_o \parallel (R_1 + R_f)$ and its value is less than R_o. Hence output resistance R_{of} is always less than R_o, if $A \to \infty$ and $R_{of} \to \infty$.

4.9.2 Non-inverting Amplifier

Figure 4.19 shows a non-inverting amplifier. The input voltage is applied to the non-inverting input terminal. The feedback resistance R_f and R_1 are connected between the output terminal, inverting input terminal and ground. This circuit amplifies input voltage without inverting. Therefore, there is no phase shift

between input and output signals. This circuit is a negative feed-back system as output is fed back to the inverting input terminal. The equivalent circuit of practical non-inverting amplifier is depicted in Fig. 4.20.

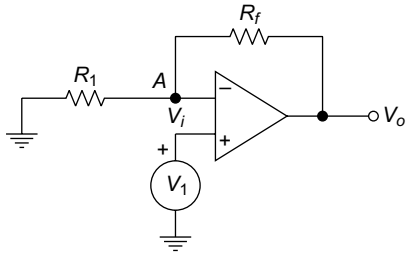


Fig. 4.19 ***Non-inverting amplifier***

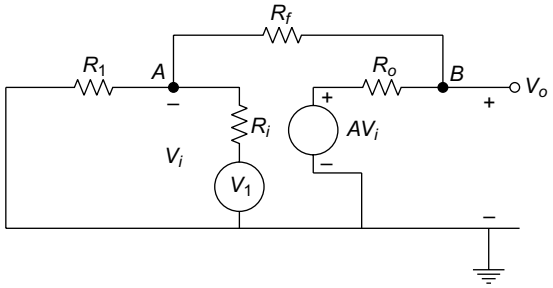


Fig. 4.20 ***Equivalent circuit of practical non-inverting amplifier***

The potential at node A is $V_A = V_1 - V_i$

KCL law at node A is

$$\frac{V_1 - V_i}{R_1} + \frac{V_i}{R_i} + \frac{V_1 - V_i - V_o}{R_f} = 0$$

Assume, $\frac{1}{R_1} = Y_1, \frac{1}{R_i} = Y_i$ and $\frac{1}{R_f} = Y_f$

Then we can write

$$(V_1 - V_i)\ Y_1 + V_i Y_i + (V_1 - V_i - V_o)\ Y_f = 0$$

or, $$-(Y_1 + Y_i + Y_f)\ V_i + (Y_1 + Y_f)\ V_1 = Y_f V_o \quad (4.2)$$

Applying KCL at node B, we get

$$\frac{(V_1 - V_i - V_o)}{R_f} + \frac{(AV_i - V_o)}{R_o} = 0$$

Assume $\frac{1}{R_o} = Y_o$

We can write $(V_1 - V_i - V_o)\ Y_f + (AV_i - V_o)\ R_o = 0$

or, $$-(Y_f - AY_o)\ V_i + Y_f V_1 = (Y_f + Y_o)\ V_o \quad (4.3)$$

After solving Eqs 4.2 and 4.3, we get

$$A_f = \frac{V_o}{V_i} = \frac{AY_o\left(Y_1 + Y_f\right) + Y_f Y_i}{\left(A+1\right)Y_o Y_f + \left(Y_1 + Y_i\right)\left(Y_f + Y_o\right)}$$

If $A \to \infty$

$$A_f = \frac{AY_o\left(Y_1 + Y_f\right)}{AY_o Y_f}$$

or, $$A_f = \frac{(Y_1 + Y_f)}{Y_f} = 1 + \frac{Y_1}{Y_f}$$

$$A_f = 1 + \frac{R_f}{R_1} \text{ As } \frac{1}{R_1} = Y_1, \text{ and } \frac{1}{R_f} = Y_f$$

The gain of amplifier can be adjusted by proper selection of resistances R_f and R_1.

4.10 OP-AMP CHARACTERISTICS

The manufacturers' data sheet of IC 741 series operational amplifiers provide information regarding pin diagram, electrical characteristics and equivalent circuit of devices, etc. IC 741 series OP-AMPs are available in different models such as IC741, IC741A, IC741C and IC741E. The schematic diagram and electrical parameters for all models are same, but the value of parameters will be differed from model to model. After study the data sheet we can state the following points:

- IC741 is internally frequency compensated OP-AMP.
- IC741 is a monolithic IC.
- Short circuit protection is provided in this IC.
- This IC has offset voltage null capacity.
- It has large common mode and differential voltage ranges.
- Its power consumption is low.
- Absence of latch-up makes the IC741 ideal for use as voltage follower.
- This IC is very useful for adder, subtractor, integrator, differentiation, voltage follower, multiplier and divider and other feedback applications.
- Absolute maximum ratings for the following parameters such as supply voltage, input voltage, differential input voltage, internal power dissipation, operating temp range and output short circuit duration, etc. are specified in the data sheet. Table 4.3 shows maximum rating of supply voltage; inter power dissipation and operating temperature, etc.
- The electrical specification of OP-AMP are input offset voltage, input offset current, input bias current, input capacitance, offset voltage adjustment range, etc. Table 4.4 shows the electrical characteristics of OP-AMPIC741C.

In this section, the electrical characteristics of typical operational amplifiers IC741C have been discussed.

Table 4.3 *Maximum rating of IC*

	Parameters	*Absolute maximum rating*
Supply Voltage	IC741, IC741A and IC741E	±22 V
	IC741C	±18 V
Internal power dissipation	Metal can	500 mW
	Molded and Hermetic DIP	670 mW
	Mini DIP	310 mW
	Flatpack	570 mW
Differential input voltage		±30 V
Input voltage		±15 V
Operating temperature	Military IC741 and IC741A	–55°C to 125°C
	Commercial IC741E and range IC741C	0°C to 70°C

Table 4.4 *Electrical characteristics of IC741 at V_S = ±15 V and operating temperature T_A = 25°C*

Electrical characteristics	*Conditions*	*Minimum value*	*Maximum value*
Input offset voltage	$R_s \leq$ kΩ		20 mV
Input offset current		20 nA	200 nA
Input bias current		80 nA	500 nA
Input resistance		2.0 MΩ	
Input capacitance		1.4 pF	
Offset voltage adjustment range		±15 mV	
Input voltage range	±12 V	±13 V	
Common mode rejection ratio	$R_s \leq$ 10 kΩ	70 dB	120 dB
Supply voltage rejection ratio		30 µV/V	150 µV/V
Large signal voltage gain	$R_L >$ 2 kΩ V_{out} = ±10 V	20,000	200,000
Output voltage swing	$R_L \geq$ 2 kΩ	±10 V	±14 V
Output resistance		75 Ω	
Output short circuit current		25 mA	
Supply current		1.7 mA	2.8 mA
Power consumption		50 mW	85 mW
Transient response	Rise time		0.3 µs
	overshoot		6%
Slew rate	$R_L \geq$ 2 kΩ		0.5 µs

4.10.1 Input Offset Voltage

The input offset voltage (V_{IOS}) is the voltage that must be applied between inverting and non-inverting terminals of an operational amplifier to null the output voltage. Figure 4.21 shows the input offset voltage of an OP-AMP. In this circuit, V_{DC1} and V_{DC2} are dc voltages and R_S represents source resistance.

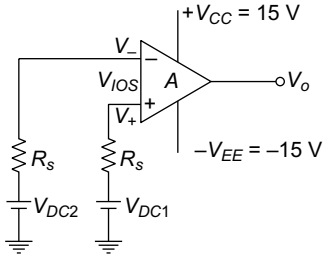


Fig. 4.21 *Input offset voltage*

The input offset voltage is $V_{IOS} = (V_{DC1} - V_{DC2})$

The magnitude of input offset voltage can be positive or negative, but its absolute value is given on the manufacturer data sheet; For example, the maximum value of V_{IOS} of IC 741C is about 20 mV. The smaller value of V_{IOS} is advantage for better input terminals matching.

4.10.2 Input Offset Current

The input offset current (I_{IOS}) is defined as the difference between the currents into the inverting and non-inverting terminals. Figure 4.22 shows the input offset current I_{IOS}.

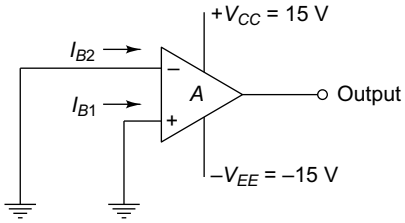


Fig. 4.22 *Input offset current*

The input offset current is

$$I_{IOS} = |I_{B1} - I_{B2}|$$

where, I_{B1} is the current input into the non-inverting terminal
I_{B2} is the current input into the inverting terminal.

The maximum value of input offset current for IC 741C is about 200 nA. The difference between I_{B1} and I_{B2} will be small when the matching between two input terminals is improved.

4.10.3 Input Bias Current

The input bias current I_B is the average of the two input currents I_{B1} and I_{B2}. In the form of the equation,

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

where, I_{B1} is the current input into the non-inverting terminal
I_{B2} is the current input into the inverting terminal.

For IC 741C, the maximum value of input bias current, I_B is 500 nA. Actually I_{B1} and I_{B2} are base currents of the first stage differential amplifier.

4.10.4 Offset Voltage Adjustment

One of the most important features of IC 741 is an offset voltage null capability. Pins 1 and 5 are used as offset null. Figure 4.23 shows the offset voltage adjustment of OP-AMP. A 10 kΩ potentiometer is connected between offset null pins 1 and 5. The wiper of the 10 kΩ potentiometer can be connected with the negative supply voltage $-V_{EE} = -15$ V.

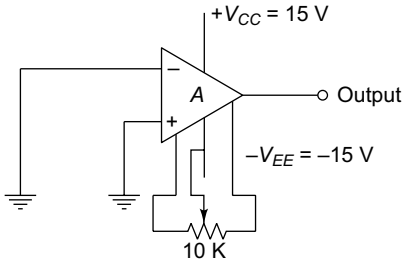


Fig. 4.23 *Offset voltage adjustment*

The output offset voltage can be reduced to zero, by changing the wiper position of the potentiometer. The offset voltage adjustment range is the range

through which the input offset voltage can be adjusted and it is about ±15 mV for IC741.

4.10.5 Thermal Drift

The operational amplifier parameters such as bias current, input offset current, input offset voltage change with temperature.

The average rate of change of input offset voltage permit change in temperature is called thermal voltage drift and it is represented by $\frac{\Delta V_{IOS}}{\Delta T}$ and it's unit value is μV/°C.

In the same way, we can define the thermal drift in the input offset current and input bias current.

Thermal drift of input offset current = $\frac{\Delta I_{IOS}}{\Delta T}$ nA/°C

Thermal drift of input bias current = $\frac{\Delta I_B}{\Delta T}$ nA/°C

4.7 Assume input offset current (I_{IOS}) = 20 nA and input offset voltage (V_{IOS}) = 0 and A = 10^5. (a) What is the differential input voltage? (b) What is the output offset voltage? Assume R_S = 1.5 kΩ

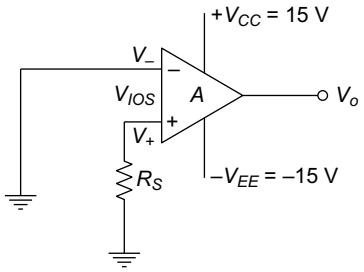


Fig. 4.24

Solution

(a) The differential input voltage = $I_{IOS} \times R_S$

$= 20 \times 10^{-9} \times 1.5 \times 10^3 = 30$ μV

(b) The output offset voltage is

$V_{out} = AV_d = 10^5 \times 30 \times 10^{-6}$ V = 3 V

4.8 The base current of a differential amplifiers are IB_1 = 15 μA and IB_2 = 20 μA.

(a) What is the input bias current?

(b) Calculate the input offset current.

Solution

Given IB_1 = 15 μA and IB_2 = 20 μA

Input bias current is

$$I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{15 + 20}{2} \text{ μA} = 17.5 \text{ μA}$$

The input offset current

$$I_{IOS} = |I_{B1} - I_{B2}| = |15 - 20|\ \mu A = 5\ \mu A$$

4.9 The input base current of a differential amplifiers are $IB_1 = 100$ nA and $IB_2 = 80$ nA.
(a) Determine the input bias current and the input offset current.
(b) When $A = 10^5$, calculate the output offset voltage.
Assume $R_S = 1\ k\Omega$

Solution

Given $IB_1 = 100$ nA and $IB_2 = 80$ nA

(a) Input bias current is

$$I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{100 + 80}{2}\,nA = 90\,nA$$

The input offset current

$$I_{IOS} = |I_{B1} - I_{B2}| = |100 - 80|\ nA = 20\ nA$$

(b) The differential input voltage = $I_{IOS} \times R_1$

$$= 20 \times 10^{-9} \times 1 \times 10^3 = 20\ \mu V$$

The output offset voltage is

$$V_{out} = AV_d = 10^5 \times 20 \times 10^{-6}\ V = 2\ V$$

4.10.6 Common Mode Rejection Ratio

Figure 4.25 shows the common mode circuit of OP-AMP. The common mode rejection ratio (CMRR) can be defined as the ratio of the differential voltage gain A_d to the common mode voltage gain A_{cm}. It is expressed as

$$\text{CMRR} = \frac{A_d}{A_{cm}}$$

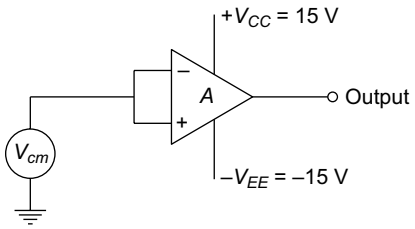


Fig. 4.25 ***Common mode circuit of OP-AMP***

The differential voltage gain A_d is same as the open loop voltage gain A.

The common mode voltage gain can be computed by using the equation

$$A_{cm} = \frac{V_{ocm}}{V_{cm}}$$

where, A_{cm} common mode voltage gain
V_{cm} input common mode voltage
V_{ocm} output common mode voltage

Normally, A_{cm} is very small and A_d is very large. Therefore, the CMRR is very large and it is very frequently expressed in decibels (dB). The CMRR value of IC741 is about 90 dB.

Figure 4.25 shows the common mode configuration of operational amplifier. For this circuit, R_S is assumed to be zero as source resistances of practical voltage sources are very small.

4.10.7 Supply Voltage Rejection Ratio

The change in an operational amplifiers input offset voltage due to variations in supply voltage is known as the Supply Voltage Rejection Ratio (SVRR). Some manufacturers represent the SVRR as power supply rejection (PSRR) or power supply sensitivity (PSS). Usually it is expressed in μV/V or in decibels (dB).

In the form of an equation

$$SVRR = \frac{\Delta V_{IOS}}{\Delta V}$$

where, ΔV is the change in supply voltage

ΔV_{IOS} change in the input offset voltage

For IC741, SVRR is about 6.3 μV/V.

4.10.8 Slew Rate

The Slew Rate (SR) is defined as the maximum rate of change of output voltage per unit time. It can be expressed as

$$SR = \frac{dV_o}{dt}\Big|_{\max} \text{ V/ μs.}$$

This is an important parameter for high frequency applications such as oscillators, comparators and filters. The typical values of slew rate for IC741 is about 0.5 V/μs.

The *SR* indicates how rapidly operational amplifier can varies in response to variation in the input frequency. These changes with change in voltage gain. Normally, the slew rate of an operational amplifier is fixed. If the slope requirements of the output signal are greater than the slew rate, output will be distorted. Therefore, slew rate is an important factor to select OP-AMPs in high frequency applications.

In a voltage follower circuit, the input voltage is large amplitude and high frequency sine wave.

Assume supply voltage is $V_S = V_m \sin \omega t$

Then output is $V_O = V_m \sin \omega t$

The rate of change of output is

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t$$

The maximum rate of change of output at $\cos \omega t = 1$

$$SR = \frac{dV_o}{dt}\Big|_{\max} = \omega V_m = 2\pi f V_m \text{ V/s} \quad \text{as } \omega = 2\pi f$$

$$= \frac{2\pi f V_m}{10^6} \text{ V/μs}$$

The slew rate can also be expressed as

$$SR = \frac{dV_o}{dt} = \frac{\Delta V_O}{\Delta t} = \frac{I_{\max}}{C} \text{ V/μs.}$$

where I_{max} is the maximum current which flows through the capacitor C
C is the value of capacitor

The slew rate can be improved by increasing the current and decreasing the capacitor value. For a high value of slew rate, operational amplifiers should have small value of capacitor with high current. The slew rate can also be improved with higher closed loop gain.

4.10 The output voltage of operational amplifier changes by 10 V with in 5 μs. Calculate the slew rate.

Solution

Given, change in output voltage $\Delta V_o = 10$ V and $\Delta t = 5$ μs
The slew rate is

$$SR = \frac{\Delta V_o}{\Delta t} \text{ V/μs} = \frac{10}{5} \text{ V/μs} = 2 \text{ V/μs}$$

4.11 The output voltage of an operational amplifier is shown in Fig. 4.26 When input voltage is triangular wave 8 V peak-to-peak amplitude with frequency 2 MHz. What is the slew rate of operational amplifier?

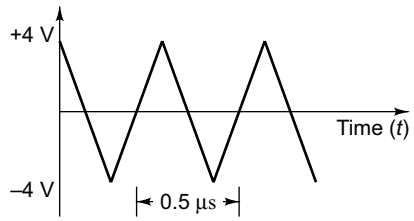


Fig. 4.26 ***Plot of Ex. 4.11***

Solution

The slew rate is defined as the maximum rate of change of the output voltage and it is expressed as

$$SR = \frac{\Delta V_o}{\Delta t} \text{ V/μs}$$

Here, $\Delta V_o = 8$ V and $\Delta t = \frac{0.5}{2} = 0.25$ μs

Then slew rate $SR = \frac{\Delta V_o}{\Delta t} \text{ V/μs} = \frac{8}{0.25} \text{ V/μs} = 32 \text{ V/μs}$

4.12 An IC 741C OPAMP is used as an inverting amplifier with a gain of 50. The input voltage is sinusoidal with maximum amplitude of 25 mV. What is the maximum frequency of the input voltage?

Solution

The typical slew rate of IC 741C OPAMP is 0.5 V/μs and $A = 50$
The maximum output voltage is

$$V_m = AV_{id} = 50 \times 25 \times 10^{-3} \text{ V} = 1.25 \text{ V} \qquad \text{As} \quad V_{id} = 25 \text{ mV}$$

The slew rate is $SR = \frac{2\pi f V_m}{10^6} = 0.5 \text{ V/μs}$

The maximum frequency is $f_{\max} = \dfrac{SR}{2\pi V_m} \times 10^6$

$$= \frac{0.5}{2\pi \times 1.25} \times 10^6 \text{ Hz}$$
$$= 63.694 \text{ kHz}$$

4.13 An IC 741C OPAMP is used as an inverting amplifier with a gain of 40. The voltage gain vs frequency response is flat up to 30 kHz. What is the maximum peak to peak input signal that can be applied without distorting the output voltage?

Solution

The typical slew rate of IC 741C OPAMP is 0.5 V/μs
Therefore $SR = 0.5$ V/μs
Frequency $f = 30$ kHz
The maximum output voltage is

$$V_m = \frac{SR}{2\pi f} \times 10^6 = \frac{0.5}{2\pi \times 30 \times 10^3} \times 10^6 \text{ V}$$
$$= 2.653 \text{ V (peak)} = 5.306 \text{ V (peak to peak)}$$

The maximum peak to peak input voltage without distorting the output is

$$= V_{id} = \frac{V_m}{A} = \frac{5.306}{40} \text{ V} = 132.65 \text{ mV (peak to peak)}$$

4.14 An operational amplifier has a slew rate of 0.5 V/μs. If the peak output voltage is 10 V, what is the maximum frequency at which the operational amplifier operates properly?

Solution

The slew rate of operational amplifier is 0.5 V/μs

The slew rate is $SR = \dfrac{2\pi f V_m}{10^6} = 0.5$ V/μs

The maximum frequency of operation is

$$f_{\max} = \frac{SR}{2\pi V_m} \times 10^6 = \frac{0.5}{2\pi \times 10} \times 10^6 \text{ Hz} = 7.96 \text{ kHz}$$

4.15 An operational amplifier has a slew rate of 0.45 V/μs. How much time it will take to change the output voltage from 0 V to 10 V?

Solution

The slew rate of operational amplifier is 0.45 V/μs
The change in output voltage, ΔV_o is 10 V
The slew rate is

$$SR = \frac{\Delta V_o}{\Delta t} \text{ V/μs}$$

or, $$\Delta t = \frac{\Delta V_o}{SR} = \frac{10}{0.45} \text{ μs} = 22.23 \text{ μs}$$

Therefore, the required time to change output voltage from 0 to 10 V is 22.23 μs

4.16 The charging current of a 150 pF capacitor is 100 μA. What is the slew rate of the operational amplifier?

Solution

Given capacitor $C = 150 \text{ pF} = 150 \times 10^{-12}$

Charging current $I_O = 100\ \mu\text{A} = 100 \times 10^{-6}$

The slew rate of operational amplifier is

$$SR = \frac{dV_o}{dt} = \frac{I_o}{C}$$

$$= \frac{100 \times 10^{-6}}{150 \times 10^{-12}} \text{ V/s} = \frac{100 \times 10^{-6}}{150 \times 10^{-12} \times 10^{6}} \text{ V/μs} = 0.667 \text{ V/μs}$$

4.17 An operational amplifier has slew rate about 0.45 V/μs and used as an inverting amplifier with a gain of 100. The voltage gain vs frequency curve of operational amplifier up to 20 kHz is flat. What is the maximum peak-to-peak input signal can be applied to the operational amplifier without distorting the output voltage?

Solution

Given $SR = 0.45$ V/μs, $A = 100$ and $f_{\max} = 20$ kHz

The slew rate is $SR = \dfrac{2\pi f V_m}{10^6} = 0.45$ V/μs

The maximum output voltage is

$$V_\mu = \frac{SR}{2\pi f} \times 10^6 = \frac{0.45}{2\pi \times 20 \times 10^3} \times 10^6 = 3.58 \text{ V}$$

The maximum output voltage is

$$V_m = AV_{id} \text{ V}$$

The maximum peak to peak input voltage to the OP-AMP without distorting the output voltage is

$$V_{id} = \frac{V_m}{A} = \frac{3.58}{100} \text{ V} = 35.8 \text{ mV}$$

4.18 Figure 4.27 shows an operational amplifier circuit. The operational amplifier has slew rate about 0.5 V/μs, gain is 10 and output saturation voltage levels are ±10 V, maximum frequency is 100 kHz.

(a) Determine the maximum peak amplitude of the output sinusoidal signal at 100 kHz for the undistorted output voltage?

(b) Calculate the value of R_1 and R_2.

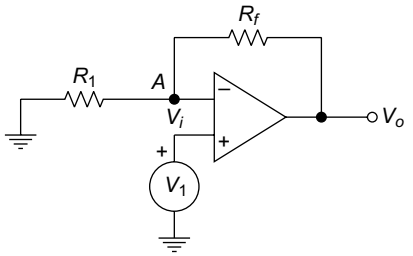


Fig. 4.27 *Circuit of Ex. 4.18*

Solution

Given $SR = 0.5$ V/μs, $A = 10$ and $f_{\max} = 100$ kHz

(a) The slew rate is $SR = \dfrac{2\pi f V_m}{10^6} = 0.5$ V/μs

The maximum peak amplitude of the output sinusoidal signal is

$$V_m = \frac{SR}{2\pi f} \times 10^6 = \frac{0.5}{2\pi \times 100 \times 10^3} \times 10^6 \text{ V}$$

$$= 0.796 \text{ V (peak)}$$

(b) The closed loop gain of operational amplifier is = 10

$$\text{As } gain = 1 + \frac{R_f}{R_1} = 10$$

$$\text{Therefore} \quad \frac{R_f}{R_1} = 9 \quad \text{or} \quad R_f = 9R_1$$

$$\text{If} \quad R_1 = 2.2 \text{ K} \quad \text{and} \quad R_f = 2.2 \times 9 \text{ k}\Omega = 19.8 \text{ k}\Omega$$

Input Resistance It is the differential input resistance seeing from any of the input terminals when the other terminal is grounded. The input resistance of 741C is about 2 MΩ.

Input Capacitance This is the equivalent capacitance which can be measured from any of the input terminals when other terminal is grounded. The input capacitance of 741C is about 1.4 pF.

Large Signal Voltage Gain Operational amplifier amplifies the difference voltage between two input terminals. The voltage gain is defined as

$$\text{Voltage gain} = \frac{\text{Output voltage}}{\text{Differential input voltage}}$$

As the amplitude of the output signal is larger than the input signal, the voltage gain is commonly known as large signal voltage gain. The typical value of voltage gain of IC 741 is 2,00,000 when $R_L \geq 2$ kΩ and $V_{\text{out}} = \pm 10$ V.

Output Resistance The output resistance R_O is the resistance measured between the output terminal and ground. The typical value of output resistance for IC 741C is about 75 Ω.

Output Short Circuit Current This current can flow when an operational amplifier gets shorted and it's value is very high. The operational amplifier must be provided with short circuit protection. The short circuit current of IC741 is about 25 mA.

Supply Current When the operational amplifier is working properly, the supply current I_S must be drawn by the device from the power supply. The typical value of supply current is 2.8 mA for IC741.

Power Consumption If the operational amplifier is working properly, a certain amount of power must be consumed by this device. The typical value of power consumption is about 85 mW for IC741.

Transient Response The rise time and overshoot are the two important characteristics of the transient response of an operational amplifier circuit. The typical values of rise time and overshoot are 0.3 μs and 6% respectively.

4.11 VIRTUAL GROUND

In an ideal operational amplifier, the input impedance is infinite ($Z_i = \infty$) and no current flows through inverting and non-inverting terminals ($I_i = 0$). As no current flow through the input terminals, the current I flows through resistance R_1 and the same current I is also passes through resistance R_f as shown in Fig. 4.28. Since gain of ideal operational $A = \infty$, $\frac{V_o}{V_i} = A$ and $V_i = 0$. This states that the input terminals of operational amplifier are effectively shorted and virtual ground exists in the circuit. The normal ground of a circuit means that it has zero potential (voltage) and it is able to sink infinite current.

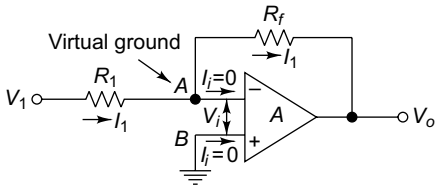


Fig. 4.28 *Ideal operational amplifier*

In case of virtual ground, at any point of the circuit, the terminal voltage is zero with respect to the ground and the said terminal draws zero current. Therefore, according to voltage is concerned, there is no difference between the normal ground and virtual ground, but as far as current is concerned, ordinary (normal) ground terminal can sink infinite current where as virtual ground terminal draws no current. For any operational amplifier circuit, the input part appears as a short as $V_i = 0$, but it appears as an open due to current $I_i = 0$.

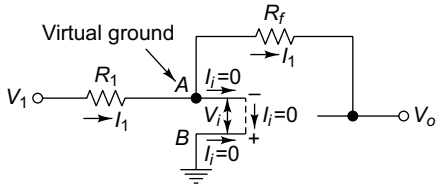


Fig. 4.29 *Equivalent circuit of Fig. 4.28*

Figure 4.29 shows the simplified equivalent circuit of Fig. 4.28. Assume B is connected with ground and it's potential is ground potential (zero volt). The non-inverting terminal has ground potential. The inverting terminal A is connected with non-inverting terminal B by dotted line. The current flow $I_i = 0$, and voltage across A and B is $V_i = 0$. Therefore, the inverting terminal is also at ground potential though there is no physical connection between inverting terminal and ground. For that reason, the inverting terminal A is called the virtual ground.

4.12 FREQUENCY RESPONSE OF OPERATIONAL AMPLIFIER

The open-loop voltage gain of operational amplifier is very high and it is about 10^5. When negative feedback is applied to an OP-AMP, the overall gain of feedback amplifier is reduced to any required value by the amount of feedback used in the circuit. At high frequency, negative feedback operational amplifier becomes unstable as the RC coupling network introduces a phase shift in the output voltage with respect to input voltage. When phase shift is equal to 180°, feedback will be positive and oscillations occur in the OP-AMP feedback circuit. To avoid this problem, IC741 has internal RC network which can reduce gain at high frequency.

The voltage gain of operational amplifier should be uniform at all frequencies in the bandwidth. For a practical OP-AMP circuit, ideal performance will not be available as the transistor circuit has frequency sensitive parameters such as inductance and capacitor in both lumped and distributed form. Capacitance effects come in the OP-AMP equivalent circuit due to transistors and FET devices as these are charge devices due to the substrate on which OP-AMPs are fabricated. Figure 4.30 shows the equivalent circuit incorporating capacitance. The frequency response of an amplifier has been divided into three regions such as low frequency, mid frequency and high frequency. Actually, an operational amplifier is a dc amplifier and frequency response in the low frequency and mid frequency regions will be flat. A single capacitor at the output represents a single pole and each pole is an energy storing element.

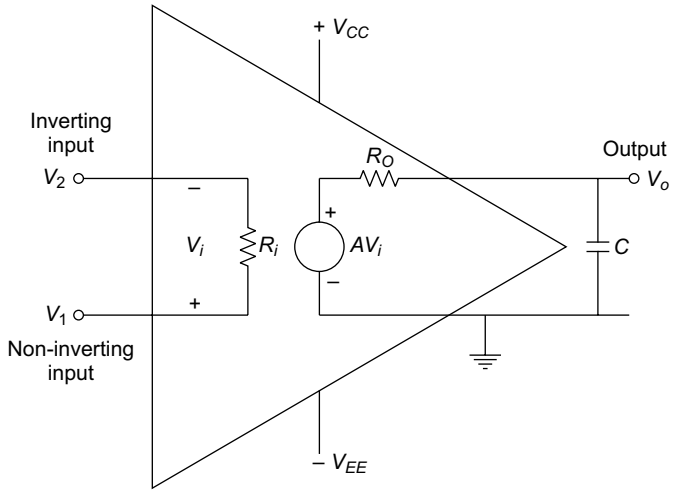


Fig. 4.30 ***Equivalent circuit of OP-AMP including capacitance***

The output voltage is

$$V_o = AV_i \frac{\dfrac{1}{sC}}{R_O + \dfrac{1}{sC}} = \frac{1}{1 + sCR_O} AV_i$$

The open-loop gain is

$$A_{OL} = \frac{V_o}{V_i} = \frac{A}{1 + sCR_o}$$

where A is the gain of the amplifier and CR_O is the time constant

After substituting $s = j\omega$ for a sinusoidal frequency response, the A_{OL} becomes

$$A_{OL} = \frac{A}{1 + j\omega CR_O} = \frac{A}{1 + j\dfrac{\omega}{\omega_C}} \qquad \text{as } \omega_C = \frac{1}{CR_O}$$

$$= \frac{A}{1 + j\frac{2\pi f}{2\pi f_C}} = \frac{A}{1 + j\frac{f}{f_C}}$$

The absolute magnitude is $|A_{OL}| = \frac{A}{\left[1 + \left(\frac{f}{f_C}\right)^2\right]^{1/2}}$ and phase angle $\phi = -\tan^{-1}\left(\frac{f}{f_C}\right)$

- At $f = 0$, $A_{OL} = A$ In dB, $A_{OL} = 20 \log A$
- At $f = 0.1f_c$, $|A_{OL}| = \frac{A}{\left[1 + \left(\frac{0.1f_C}{f_C}\right)^2\right]^{1/2}} = \frac{A}{1.005}$

  In dB, $A_{OL} = 20 \log A - 20 \log 1.005 = 20 \log A - 0.0433$ dB
- At $f = f_C$ $|A_{OL}| = \frac{A}{\sqrt{2}}$

  In dB, $A_{OL} = 20 \log A - 20 \log 1.414 = 20 \log A - 3.0089$ dB
- At $f = 10f_C$, $|A_{OL}| = \frac{A}{\sqrt{101}}$

In dB, $A_{OL} = 20 \log A - 20 \log 10.049 = 20 \log A - 20.043$ dB

Figure 4.31 shows the frequency response of an operational amplifier. When the open-loop gain of operational amplifier is 10^5, the gain at very low frequency is $20 \log(10^5) = 100$ dB. At frequency f_C, magnitude is reduced by $\frac{1}{\sqrt{2}}$ times or the gain drops by 3 dB. f_C is called the half power frequency. At frequency $f = 10 f_C$, the gain drops by 20 dB. The gain can be reduced to 0 dB (unity) at the frequency f_T. Then, f_T is called frequency of unity gain. After applying the negative feedback, if the overall gain A_f is 10, it will be 20 dB in dB as shown in Fig. 4.31 and the half-power frequency increases to f_H.

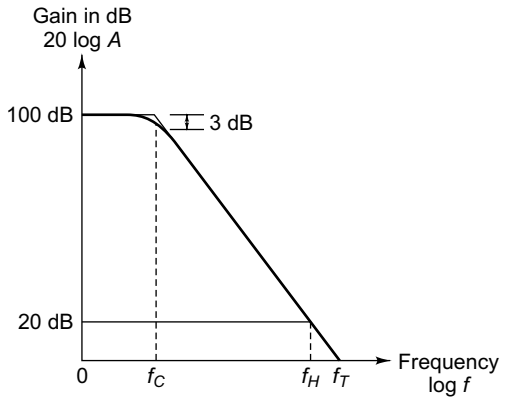


Fig. 4.31 *Gain vs frequency plot of OP-AMP including capacitance*

4.13 STABILITY OF OPERATIONAL AMPLIFIER

Assume the open-loop gain of operational amplifier is frequency dependent and it can be represented as $A(f)$. Figure 4.32 shows a non-inverting feedback amplifier circuit and its block diagram representation is depicted in Fig. 4.33.

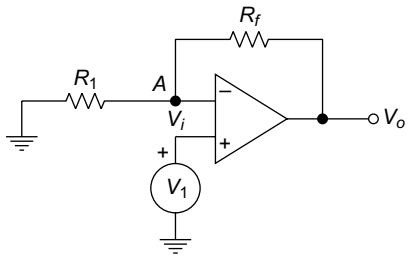


Fig. 4.32 *Non-inverting amplifier*

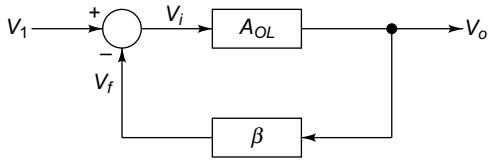


Fig. 4.33 *Block-diagram representation of non-inverting amplifier*

The error signal is

$$V_i = V_1 - \beta V_o$$

where feedback voltage is βV_o and input voltage is V_1

The output voltage is $V_o = A_{OL} V_i$ and $V_i = \dfrac{V_o}{A_{OL}}$

Therefore, $$V_i = \frac{V_o}{A_{OL}} = V_1 - \beta V_o$$

or, $$\frac{V_o}{A_{OL}} + \beta V_O = V_1$$

or, $$\frac{1 + \beta A_{OL}}{A_{OL}} V_o = V_1$$

Then, $\dfrac{V_o}{V_1} = \dfrac{A_{OL}}{1 + \beta A_{OL}}$. This is called the closed-loop gain of the amplifier and βA_{OL} is called the closed-loop gain which is used to determine the stability of operational amplifier. The condition for stability is $1 + \beta A_{OL} = 0$ or $\beta A_{OL} = -1$.

In the complex plane $\beta A_{OL} = -1$ can be expressed as $\beta A_{OL} = -1 + j0$

Therefore, absolute value of $|\beta A_{OL}| = 1$ and $\angle \beta A_{OL} = 0°$ or 360°.

When the conditions $|\beta A_{OL}| = 1$ and $\angle \beta A_{OL} = 0°$ or 360° are satisfied at a particular frequency, the system starts to oscillate and becomes unstable. The system will be stable if its output reaches a final value with infinite time. If output increases with time in the system or the system has output signal without

input, the system is said to be unstable. To check the stability of the system, the conditions $|\beta A_{OL}| = 1$ and $\angle \beta A_{OL} = 0°$ or 360° are verified. If these conditions are not satisfied, the system is stable and otherwise, it is unstable.

EXERCISES

1. Define integrated circuit. What are the types of ICs? Write some applications of ICs.
2. Give a list of advantages and disadvantages of ICs.
3. Explain the operation of difference amplifier with suitable diagram.
4. Define CMRR. Derive an expression for CMRR.
5. What are the characteristics of an ideal OP-AMP?
6. Draw the schematic block diagram of an OP-AMP and explain briefly.
7. Prove that $V_o = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$
8. Explain the following
   (a) Frequency response of OP-AMP
   (b) Stability of OP-AMP
   (c) Integrated circuits
   (d) Virtual ground
9. Define slew rate. How is it calculated for sinusoidal input voltage? What are the different methods to improve slew rate?
10. State specification of an IC 741.
11. What is virtual ground? Write the difference between ground and virtual ground.
12. Define (a) input offset voltage, (b) input bias current, (c) input offset current, (d) and thermal drift.
13. Draw the frequency response of an operational amplifier and explain its significance.
14. State the characteristics of an ideal operational amplifier. How the characteristics of practical operational amplifier is differed from ideal operational amplifier?
15. Calculate the common mode gain of a operational amplifier for the following parameters: the differential voltage gain $A_d = 10^5$ and common mode rejection ratio CMRR = 2000.
16. Calculate the output voltage of a differential amplifier for the following parameters:
    $V_1 = 500\ \mu V$, $V_2 = 100\ \mu V$, $A_d = 1000$ and ρ = CMRR = 20000
17. The common mode rejection ratio CMRR of an operational amplifier is about 100 dB and difference mode voltage gain is 10,000. Determine common mode gain.
18. The input signals of a differential amplifier are $V_1 = 150\ \mu V$ and $V_2 = -50\ \mu V$.
    (a) When the common mode rejection ratio is 50, determine the output voltage of differential amplifier.

(b) if $\rho = 20{,}000$ find the output voltage.
Assume difference mode gain $A_d = 20{,}000$

19. The difference amplifier as shown in Fig. 4.34 has the following parameters:
$R_C = 5\ \text{k}\Omega$, $R_E = 200\ \text{k}\Omega$, $R_S = 5\ \text{k}\Omega$
The transistor parameters are as follows:
$h_{ie} = 5\ \text{k}\Omega$, $h_{fe} = 100$, $h_{re} = 0$, $h_{oe} = 0$
When the amplifier is operated with common mode signal of 250 mV and difference signal of 250 mV, determine output voltage and CMRR.

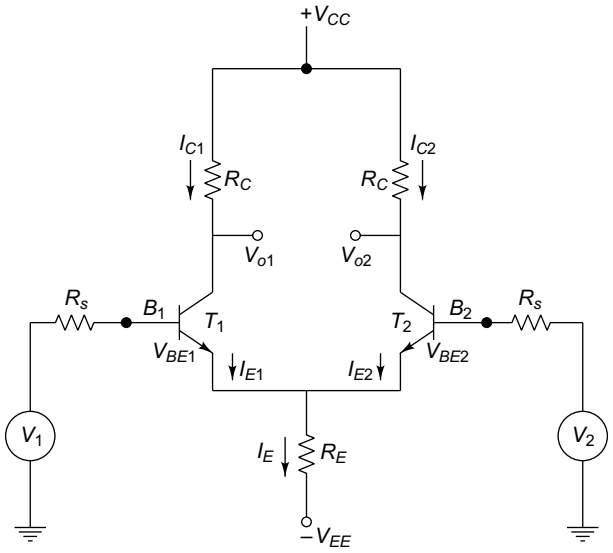


Fig. 4.34

20. Assume input offset current (I_{IOS}) = 100 nA and input offset voltage (V_{IOS}) = 0 and $A = 10^5$.
(a) What is the differential input voltage?
(b) What is the output offset voltage?.
Assume $R_S = 1\ \text{k}\Omega$

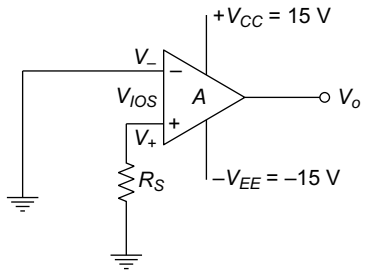


Fig. 4.35

21. The base current of a differential amplifiers are $IB_1 = 50\ \mu\text{A}$ and $IB_2 = 30\ \mu\text{A}$.
(a) What is the input bias current?
(b) Calculate the input offset current.

22. The input base current of a differential amplifiers are IB_1 = 200 nA and IB_2 = 10 nA.
    (a) Determine the input bias current and the input offset current.
    (b) When $A = 10^5$, calculate the output offset voltage.
    Assume R_S = 1.5 kΩ
23. The output voltage of operational amplifier changes by 12 V with in 4 μs. Calculate the slew rate.
24. The output voltage of an operational amplifier is shown in Fig. 4.36. When input voltage is a square wave of 6 V peak to peak amplitude with frequency 1 MHz. What is the slew rate of operational amplifier?

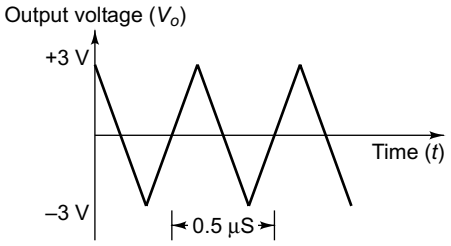


Fig. 4.36

25. An IC 741C OP-AMP is used as an inverting amplifier with a gain of 60. The input voltage is sinusoidal with maximum amplitude of 20 mV. What is the maximum frequency of the input voltage?
26. An IC 741C OP-AMP is used as an inverting amplifier with a gain of 50. The voltage gain vs frequency response is flat up to 20 kHz. What is the maximum peak to peak input signal that can be applied without distorting the output voltage?
27. An operational amplifier has a slew rate of 0.5 V/μs. If the peak output voltage is 12 V, What is the maximum frequency at which operational amplifier operates properly?
28. An operational amplifier has a slew rate of 0.55 V/μs. How much time will it take to change the output voltage from 0 V to 12 V?
29. The charging current of a 200 pF capacitor is 100 μA. What is the slew rate of operational amplifier?
30. An operational amplifier has slew rate about 0.5 V/μs and used as an inverting amplifier with a gain of 50. The voltage gain vs frequency curve of operational amplifier up to 30 kHz is flat. What is the maximum peak-to-peak input signal can be applied to the operational amplifier without distorting the output voltage?
31. Figure 4.37 shows an operational amplifier circuit. The operational amplifier has slew rate about 0. 5 V/μs, gain is 9 and output saturation voltage levels are ±10 V, maximum frequency is 50 kHz.
    (a) Determine the maximum peak amplitude of the output sinusoidal signal at 50 KHz for the undistorted output voltage?
    (b) Calculate the value of R_1 and R_f.

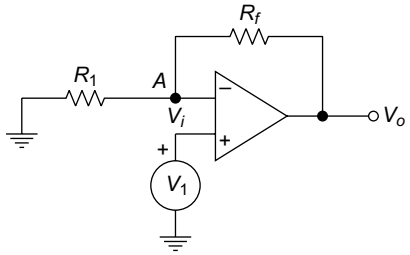


Fig. 4.37

MULTIPLE CHOICE QUESTIONS

1. The two input terminals of an operational amplifier are called as
   (a) differential and non-differential
   (b) inverting and non-inverting
   (c) positive and negative
   (d) high and low
   Answer: (b) inverting and non inverting
2. A differential amplifier has
   (a) four inputs (b) three inputs
   (c) two inputs (d) one input
   Answer: (c) two inputs
3. An OP-AMP circuit uses a feedback which is called
   (a) open loop (b) inverting feedback
   (c) inverting feedback (d) non-inverting feedback
   Answer: (b) inverting feedback
4. A differential amplifier has
   (a) common collector transistor (b) an emitter follower
   (c) common base transistor (d) an op-amp
   Answer: (b) an emitter follower
5. A differential amplifier is used in OPAMP circuits due to
   (a) high input impedance. (b) low input impedance
   (c) high output impedance (d) low output impedance
   Answer: (a) high input impedance.
6. Differential amplifiers are commonly used in
   (a) instrumentation amplifiers (b) buffers
   (c) summing amplifier (d) zero-crossing-detectors
   Answer: (a) instrumentation amplifiers
7. The common mode signal V_C is applied to
   (a) the inverting input terminal (b) the non-inverting input terminal
   (c) both the input terminals (d) all of the above
   Answer: (c) both the input terminals
8. When the two input terminals of a difference amplifier are grounded then
   (a) the dc output voltage is zero
   (b) the ac output voltage is zero

(c) the output offset voltage is exist
(d) none of these
Answer: (c) the output offset voltage is exist

9. The CMRR of a difference amplifier is

(a) $\text{CMRR} = 20\log\left|\frac{A_d}{A_C}\right|$ (b) $\text{CMRR} = 20\log\left|\frac{A_C}{A_d}\right|$ dB

(c) $\text{CMRR} = 40\log\left|\frac{A_C}{A_d}\right|$ dB (d) $\text{CMRR} = 40\log\left|\frac{A_C}{A_d}\right|$ dB

Answer: (a) $\text{CMRR} = 20\log\left|\frac{A_d}{A_C}\right|$

10. The input offset current of a difference amplifier is
(a) the difference of the two base currents
(b) average of the two collector currents,
(c) the average of the two base currents
(d) difference of the two collector currents
Answer: (c) the average of the two base currents

11. The input stage and second stage of an OP-AMP are
(a) differential amplifiers (b) CE amplifier
(c) common collector amplifier (d) power amplifier
Answer: (a) differential amplifiers

12. An operational-amplifier IC is a an
(a) analog IC (b) digital IC
(c) hybrid IC (d) digital as well as analog IC
Answer: (a) analog IC

13. The output voltage can be expressed in terms of CMRR is

(a) $A_d V_d\left(1+\frac{1}{\rho}\frac{V_C}{V_d}\right)$ (b) $A_d V_d\left(1-\frac{1}{\rho}\frac{V_C}{V_d}\right)$

(c) $A_d V_d\left(1+\frac{1}{\rho}\frac{V_d}{V_C}\right)$ (d) $A_d V_d\left(1-\frac{1}{\rho}\frac{V_d}{V_C}\right)$

Answer: (a) $A_d V_d\left(1+\frac{1}{\rho}\frac{V_C}{V_d}\right)$

14. In an ideal operational-amplifier IC, the transistors are
(a) matched (b) different characters
(c) unmatched (d) none of these
Answer: (a) matched

15. The last stage of an operational-amplifier is
(a) output driver (b) differential amplifier
(c) buffer (d) level shifter
Answer: (a) output driver

16. The rise time and overshoot of operational-amplifier are
    (a) 0.3 ns and 6% (b) 0.3 μs and 6%
    (c) 0.3 ps and 2% (d) 0.3 ps and 6%
    Answer: (b) 0.3 μs and 6%
17. An ideal op-amp has
    (a) infinite input impedance (b) zero output impedance
    (c) infinite voltage gain (d) all of the above
    Answer: (d) all of the above
18. The number of pins of the IC741 op-amp is
    (a) 8 (b) 10
    (c) 12 (d) 14
    Answer: (a) 8
19. The short-circuit output current of IC741 is
    (a) 25 A. (b) 25 mA
    (c) 25 pA (d) 25 nA
    Answer: (b) 25 mA
20. The maximum rate of change of output voltage per unit time is
    (a) slew rate (b) CMRR
    (c) offset voltage (d) supply voltage rejection ratio
    Answer: (a) slew rate

UNIVERSITY QUESTIONS WITH ANSWERS

Multiple Choice Type Questions

1. X has very high input impedance and low output impedance. X may be
   (a) FET and OP-AMP (b) FET and Transistor
   (c) OP-AMP and Transistor (d) none of these. [WBUT-2007]
2. A differential amplifier has a differential gain of 20000, and CMRR = 80 dB. The common mode gain is given by [WBUT-2007]
   (a) 2 (b) 1 (c) 0.5 (d) 0
3. The closed loop gain of an OP-AMP inverting amplifier is
   (a) always larger than unity (b) always equal to unity
   (c) always less than unity [WBUT-2007]
4. Gain of inverting amplifier is
   (a) $-R_f/R_1$ (b) $(1 + R_f/R_1)$ (c) $(R_f + R_1)/R_f$ (d) $-(R_f + R_1)/R_1$
   [WBUT-2009]
5. CMRR=
   (a) MOD (A_d/A_c) [A_d = voltage gain for difference signal; A_c = voltage gain for common mode signal]
   (b) V_2/V_1 [V_1 = non-inverting input terminal signal; V_2 = inverting input terminal signal]
   (c) $A_1 - A_2$ [A_1 = voltage gain when inverting terminal is grounded; A_2 = voltage gain when non-inverting terminal is grounded]
   (d) $V_d V_c$ [V_d = difference signal; V_c = common mode signal]
   [WBUT-2009]

6. An ideal OP-AMP has
   (a) infinite A_v (b) zero R_o (c) infinite R_i (d) all of these [WBUT-2009]
7. Output impedance of an ideal OP-AMP is
   (a) 0 (b) 75 ohm (c) 100 k ohm (d) none of these [WBUT-2010]
8. The value of CMRR for an ideal OP-AMP is
   (a) 0 (b) 1 (c) infinite (d) none of these [WBUT-2010]

Solutions:

1. (c) OP-AMP and Transistor; 2. (a) 2
3. (a) 4. (a) $-R_f/R_1$
5. (a) MOD (A_d/A_c) 6. (d) all of these
7. (a) 0 8. (c) infinite

Short- and Long-Answer-Type Questions

1. What is virtual ground in an inverting OP-AMP circuit? [WBUT-2002]
   Solution: Refer Section 4.11.
2. Write down the characteristics of an ideal OP-AMP. [WBUT-2002]
   Solution: Refer Section 4.2.
3. Define the following terms in connection with an operational amplifier:
   (i) common mode rejection ratio (CMRR)
   (ii) input offset current [WBUT-2003]
   Solution: Refer Section 4.10.
4. What is an integrated circuit? What are its advantages? [WBUT-2003]
   Solution:
   (a) An *integrated circuit* (IC), is a semiconductor wafer on which thousands or millions of tiny resistors, capacitors, diodes and transistors are fabricated. Sometimes, an IC is called a *chip* or microchip. The first integrated circuit was developed in the 1950s by Jack Kilby of Texas Instruments and Robert Noyce of Fairchild Semiconductor. An IC can function as an amplifier, oscillator, gate, flip-flop, timer, counter, computer memory, or microprocessor, etc.
   (b) The advantages of ICs are given below:
   - Its size is small. Due to miniaturization, the density of components is increased. It is possible to incorporate about 20,000 components per square inch.
   - Improved performance as complex circuits are fabricated for better performance
   - Low cost due to batch processing
   - Reliability is high
   - Less power consumption
   - Higher operating speed due to absence of parasitic capacitance effect
   - Matched devices
   - Less weight
   - Easy replacement

5. Explain the use of an OPAMP as an inverting amplifier. Derive the expression for its voltage gain assuming ideal OPAMP. [WBUT-2003]
Solution: Refer Section 4.9.1.

6. (a) What is an integrated circuit?
(b) Give an example of a linear IC chip with its various pin connections. [WBUT-2004]
Solution: (a) Refer Section 4.1.
(b) Refer Fig. 4.5.

7. An ideal OP-AMP has the output connected with the inverting input through resistance of 1 kΩ. An ac voltage of magnitude 5 V rms is applied through a series-resistance of 5 kΩ between non-inverting Input and ground. Draw the circuit diagram and state the assumptions for determination of the output voltage. [WBUT-2006]
Solution:
Figure 4.38 shows the amplifier circuit. Assume the resistance R_1 = 8 and R_f= 1 kΩ.

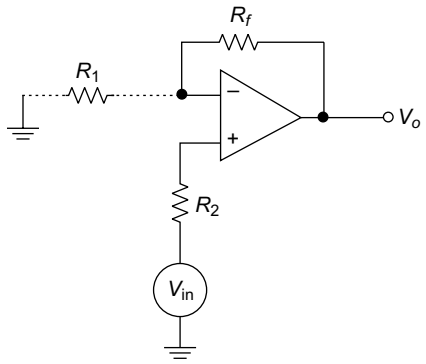


Fig. 4.38

The output voltage is

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$$

$$= \left(1 + \frac{5}{\infty}\right) V_{in} = (1 + 0)\ V_{in} = V_{in} = 5\ \text{V}$$

8. Define the following which are related to OP-AMP:
(a) Input bias current
(b) Input offset current
(c) Input offset voltage
(d) CMRR
(e) Slew rate [WBUT-2007]
Solution: (a) Refer Section 4.10.

9. (a) Define the characteristic of an ideal OP-AMP.
(b) Draw and explain the operation of an OP-AMP integrator circuit,

(c) Draw the block diagram of 741 OP-AMP. Show the terminals on diagram.

(d) An inverting amplifier has R_f = 500 kΩ, R_1 = 5kΩ. Determine the circuit voltage gain, input resistance, output resistance, output voltage, input current if the input voltage is 0.1 V.
(OP-AMP is ideal one.) [WBUT-2007]

Solution:

(a) Refer Section 4.2.

(b) Refer Section 4.11.

(c) Refer Section 4.7 and Section 4.5.

(d) Given: R_1 = 5 kΩ, R_f = 500 kΩ, input voltage V_{in} = 0.1 V

Figure 4.39 shows the inverting amplifier circuit

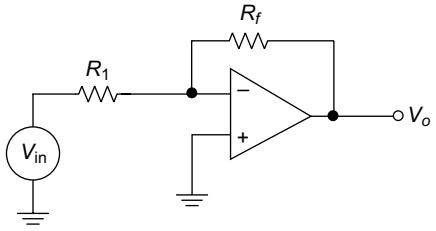


Fig. 4.39

The voltage gain is $A_f = -\frac{R_f}{R_1} = -\frac{500}{5} = -100$

The input resistance is $R_{in} = R_1 = 5$ KΩ

The output resistance is $R_o = 0$

The output voltage is $V_o = -\frac{R_f}{R_1} V_{in} = -\frac{500}{5} \times 0.1 = -10\text{ V}$

The input current $I = \frac{V_{in}}{R_1} = \frac{0.1}{5 \times 10^3} = 0.02\text{ mA}$

10. Define the following terms in connection with OP-AMP
(a) CMRR: (b) Output offset (c) Slew rate [WBUT-2007]
Solution: (a) Refer Section 4.10.

11. Calculate the common mode rejection ratio of an OP-AMP that has a differential gain of 2,00,000 and common mode gain of 6.33. [WBUT-2007]
Solution:

$$\text{CMRR} = \frac{\text{Differential gain}}{\text{Common mode gain}} = \frac{2,00,000}{6.33} = 31595.576$$

12. Draw the circuit diagram and derive the expression for voltage gain of a non-inverting amplifier using OP-AMP.
Solution: (a) Refer Section 4.9.2. [WBUT-2008]

13. Define the following terms in connection with an amplifier:
(i) Common mode rejection ratio
(ii) input bias current [WBUT-2008]
Solution: (a) Refer Section 4.10.

14. (a) Define CMRR of an OP-AMP
    (b) When a voltage of V_1 = 40 μV is applied to the non-inverting input terminal and a voltage V_2 = –40 μV is applied to the inverting input terminal of an OP-AMP, an output voltage V_o = 100 mV is obtained. But when $V_1 = V_2$ = 40 μV, one obtains V_o = 4 μV. Calculate the CMRR.

Solution:

(a) Refer Section 4.6.1.

(b) The common mode signal is $V_C = \frac{V_1 + V_2}{2}$ and the difference signal is $V_d = V_1 - V_2$

The output voltage is $V_o = A_C V_C + A_d V_d$

When V_1 = 40 μV, V_2 = –40 μV, the output voltage is V_o = 100 mV

Then $V_C = \frac{V_1 + V_2}{2} = \frac{40 - 40}{2} = 0$ V

$V_d = V_1 - V_2 = 40 - (-40) = 80$ μV

The output voltage is

$$V_O = A_C V_C + A_d V_d = A_C \times 0 + A_d \times 80 \times 10^{-6} = 100 \times 10^{-3}$$

or $A_d \times 80 \times 10^{-6} = 100 \times 10^{-3}$

$$A_d = \frac{100 \times 10^{-3}}{80 \times 10^{-6}} = 1250$$

When $V_1 = V_2$ = 40 μV, output voltage V_o = 4 μV

Then $V_C = \frac{V_1 + V_2}{2} = \frac{40 + 40}{2} = 40\,\mu\text{V}$

$V_d = V_1 - V_2 = 40 - 40 = 0$ V

The output voltage is

$$V_o = A_C V_C + A_d V_d = A_C \times 40 \times 10^{-6} + A_d \times 0 = 4 \times 10^{-6}$$

or $A_C \times 40 \times 10^{-6} = 4 \times 10^{-6}$

$$A_C = \frac{4 \times 10^{-6}}{40 \times 10^{-6}} = 0.1$$

$$\text{CMRR} = \frac{A_d}{A_C} = \frac{1250}{0.1} = 12500$$

15. (a) State the assumptions made for analyzing ideal OP-AMP
    (b) What do you mean by virtual ground in OP-AMP circuits?
    (c) Draw and explain the operation of an OP-AMP integrator circuit.

[WBUT-2009]

Solution:

(a) Refer Section 4.2.

(b) Refer Section 4.11.

(c) Refer Section 4.7.

16. (a) What are the properties of an OP-AMP?
    (b) How can a scale changer and a phase shifter be obtained with an OP-AMP?
    (c) Define the following: (i) Slew rate (ii) input bias current (iii) input offset current (iv) input offset voltage.
    (d) Calculate the output voltage using the circuit of Fig. 4.40 shown for reset components of values: R_f= 470 kΩ, R_1 = 4.3 kΩ, R_2 = 33 kΩ and R_3 = 33 kΩ for an input of 80 μV [WBUT-2009]

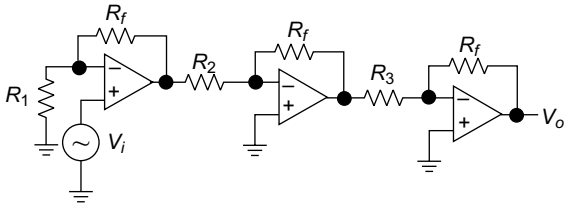


Fig. 4.40

Solution:

(a) Refer Section 4.2.

(b) Figure 4.41 shows the circuit diagram of inverting amplifier using operational amplifier. In this circuit, input voltage V_1 is applied to the inverting terminal through a series resistance R_1. The output voltage V_o is feedback to the inverting terminal through the feedback resistance R_f and the non-inverting terminal of operational amplifier is grounded.

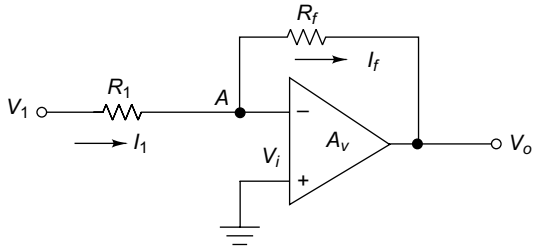


Fig. 4.41 ***Inverting amplifier***

The output voltage of an inverting amplifier is

$$V_o = -\frac{R_f}{R_1} V_1 = -KV_1 \qquad \text{Assume } K = \frac{R_f}{R_1}$$

k is the overall loop gain of the amplifier. When R_f and R_1 are selected as precision resistors, circuit output voltage k times of input voltage. If $R_f = R_1$, k = 1 and the circuit acts as an inverting amplifier. The negative sign indicates the phase inversion of output signal. If a sine wave signal is applied at V_1, then we get a amplified sine wave with a gain of k and 180° *phase shift* from input signal. Therefore, this circuit can be used as *sign changer* when the gain is one. If the ratio $\left|\frac{V_o}{V_1}\right|$ is greater than one, the circuit is called *scale changer*.

(c) Refer Section 4.10.

(d) The output voltage point A is

$$V_A = \left(1 + \frac{R_f}{R_1}\right) V_i$$

The output voltage point B is

$$V_B = \left(1 + \frac{R_f}{R_2}\right) V_A = \left(1 + \frac{R_f}{R_2}\right)\left(1 + \frac{R_f}{R_1}\right) V_i$$

The output voltage point C is

$$V_o = \left(1 + \frac{R_f}{R_3}\right) V_B = \left(1 + \frac{R_f}{R_3}\right)\left(1 + \frac{R_f}{R_2}\right)\left(1 + \frac{R_f}{R_1}\right) V_i$$

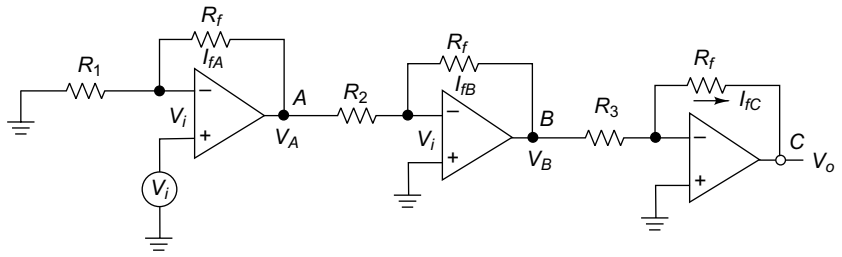


Fig. 4.42

After substituting the values of resistances R_f = 470 kΩ, R_1 = 4.3 kΩ, R_2 = 33 kΩ and R_3 = 33 kΩ for an input of 80 μV, we get

$$V_o = \left(1 + \frac{R_f}{R_3}\right)\left(1 + \frac{R_f}{R_2}\right)\left(1 + \frac{R_f}{R_1}\right)$$

$$V_i = \left(1 + \frac{470}{33}\right)\left(1 + \frac{470}{33}\right)\left(1 + \frac{470}{4.3}\right) \times 80 \times 10^{-6} \text{ V}$$

$$= 2.031 \text{ V}$$

5 APPLICATIONS OF OPERATIONAL AMPLIFIERS

5.1 INTRODUCTION

The basic operation of an operational amplifier, its dc and ac characteristics, limitations and different configuration have been explained in Chapter 4. Generally, an operational amplifier is a linear device and its output is directly proportional to the input. As per transfer characteristics, the practical operational amplifier operates as a linear device over a certain range of input signal and behaves as a nonlinear device over other regions. Hence, applications of operational amplifiers can be divided as linear applications and nonlinear applications.

Linear Applications In linear applications of operational amplifiers, the output signal is related with the input signal linearly. Some of the linear applications of operational amplifiers are as follows:

- Adder or summing
- Subtractor or difference
- Voltage to current converter
- Current to voltage converter
- Instrumentation amplifiers
- Analog computation
- Power amplifier

Nonlinear Applications In nonlinear applications, the relationship between input and output signals of operational amplifiers is nonlinear. Some of the nonlinear applications of operational amplifiers are as follows:

- Comparator
- Logarithmic and antilogarithmic amplifiers
- Multiplier
- Divider
- Integrator
- Differentiator
- Rectifier
- Pear detector
- Clipper
- Clamper
- Sample and hold circuits

In this chapter, adder or summing, subtractor or difference, voltage to current converter, current to voltage converter, instrumentation amplifiers, analog computation,

integrator, differentiator, comparator, logarithmic and antilogarithmic amplifiers, multiplier, and divider are discussed elaborately with examples.

5.2 INVERTING AMPLIFIER

Figure 5.1 shows the circuit diagram of an inverting amplifier using operational amplifier. In this circuit,

- Input voltage V_1 is applied to the inverting terminal through a series resistance R_1
- Output voltage V_o is fed back to the inverting terminal through the feedback resistance R_f
- The non-inverting terminal of operational amplifier is grounded

For circuit analysis, assume $A_v = \infty$, $R_i = \infty$ and $R_o = 0$. The input differential voltage V_i is approximately zero and operational amplifier does not draw any current. Therefore, current flows through R_1 is same as current flows throug R_f. As $V_i = 0$, the inverting terminal A is virtually grounded.

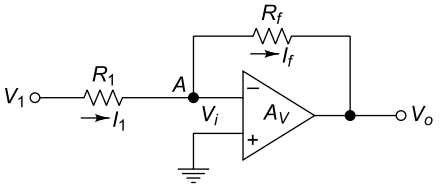


Fig. 5.1 *Inverting amplifier*

The current flows through R_1 is

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1} \text{ as } V_A = 0$$

The current flows through R_f is

$$I_f = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f} = -\frac{V_o}{R_f} \quad \text{as} \quad V_A = 0$$

Since $I_1 = I_f$, we can write

$$\frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

or,
$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

or,
$$V_o = -\frac{R_f}{R_1} V_1 = -A_{vf} V_1 \quad \text{Assume } A_{vf} = \frac{R_f}{R_1}$$

A_{vf} is the overall loop gain of the amplifier and its negative value indicates the phase inversion of the output signal. Hence, the circuit acts as an inverting amplifier. If a sine wave signal is applied at V_1 then we get an amplified sine wave with a gain of A_{vf} and 180° phase shift from input signal.

This circuit can be used as *sign changer* when the gain is one ($A_{vf} = 1$). If the ratio $\left|\frac{V_o}{V_1}\right|$ is greater than unity (one), the circuit is called a *scale changer*.

5.1 Design an operational amplifier circuit with a gain of –20. Assume input resistance is equal to 5 kΩ.

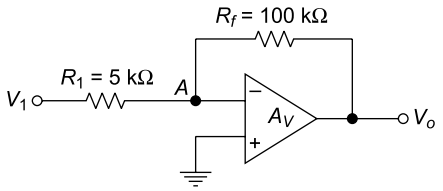


Fig. 5.2 *Circuit of Ex. 5.1*

Solution As gain of an operational amplifier is negative, an inverting amplifier has to be designed.

The gain of an inverting amplifier is

$$-\frac{R_f}{R_1} = -20$$

Since $R_1 = 5$ kΩ, $R_f = 20 \times 5$ kΩ = 100 kΩ. Figure 5.2 shows the operational amplifier with a gain –20.

5.2 An inverting amplifier is shown in Fig. 5.3. Determine (a) I_1 (b) V_o (c) I_L (d) I_o Assume input voltage V_1 is equal to 1 V.

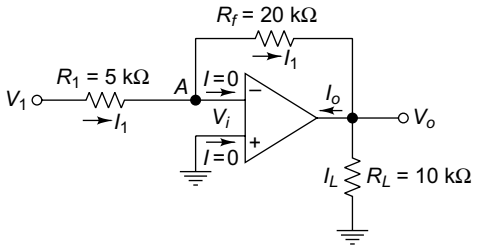


Fig. 5.3 *Circuit of Ex. 5.2*

Solution The current I_1 is

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1} = \frac{1}{5 \times 10^3} \text{ A} = 0.2 \text{ mA}$$

The output voltage is equal to

$$V_o = -\frac{R_f}{R_1} V_1 = -\frac{20}{5} \times 1 \text{ V} = -4 \text{ V}$$

The load current I_L is

$$I_L = \frac{V_O}{R_L} = \frac{4}{10 \times 10^3} = 0.4 \text{ mA}$$

The current I_o is equal to

$$I_o = I_1 + I_L = (0.2 + 0.4) \text{ mA} = 0.6 \text{ mA}$$

5.3 NON-INVERTING AMPLIFIER

The circuit diagram of the non-inverting amplifier using operational amplifier is illustrated in Fig. 5.4. In this circuit,

- Input voltage V_1 is applied to the non-inverting terminal of the amplifier

- The feedback resistance R_f is connected between the output voltage terminal and inverting input terminal and resistance R_1 is connected between inverting terminal and ground

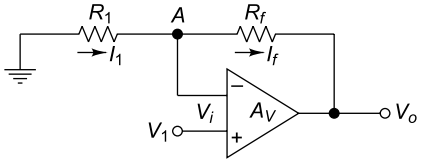


Fig. 5.4 *Non-inverting amplifier*

Assume $V_i = 0$

The potential at A is $V_A = V_1$

The current flows through R_1 is

$$I_1 = \frac{0 - V_A}{R_1} = -\frac{V_A}{R_1} = -\frac{V_1}{R_1}$$

The current flows through R_f is

$$I_f = \frac{V_A - V_o}{R_f} = \frac{V_1 - V_o}{R_f}$$

As $I_1 = I_f$, we can write

$$-\frac{V_1}{R_1} = \frac{V_1 - V_o}{R_f}$$

or, $$\frac{V_o}{R_f} = \frac{V_1}{R_f} + \frac{V_1}{R_1} = \left(\frac{1}{R_f} + \frac{1}{R_1}\right) V_1$$

or, $$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$$

or, $$\frac{V_o}{V_1} = \left(1 + \frac{R_f}{R_1}\right)$$

It is clear from the above expression that the output signal has the same sign as the input signal and there is no phase shift between input voltage and output voltage. Therefore, output is not inverted. The required amplifier gain can be achieved by selecting a proper value of R_f and R_1.

5.3 Design a non-inverting operational amplifier circuit with a gain of 10. Assume input resistance is equal to 10 kΩ.

Solution As gain of operational amplifier is positive, a non-inverting amplifier has to be designed.

The gain of non-inverting amplifier is

$$1 + \frac{R_f}{R_1} = 10$$

As $R_1 = 10\ \text{k}\Omega$, $R_f = 9R_1 = 9 \times 10\ \text{k}\Omega = 90\ \text{k}\Omega$. Figure 5.5 shows the operational amplifier with a gain 10.

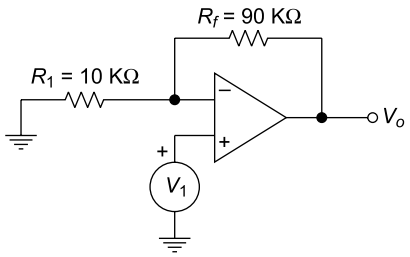


Fig. 5.5 *Circuit of Ex. 5.3*

5.4 Figure 5.6 shows the non-inverting amplifier, where R_f = 10 kΩ, R_f = 100 kΩ and V_1 = 1 V.

Determine (a) V_o, (b) gain, (c) I_1, (d) load current I_L, and (d) output current I_o.

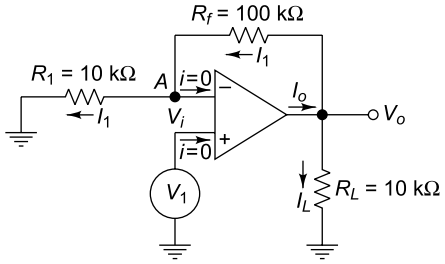


Fig. 5.6 ***Circuit of Ex. 5.4***

Solution Since V_1= 1 V, the potential at A will be V_A = 1 V (as V_i = 0)

The output voltage is equal to

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1 = \left(1 + \frac{100}{10}\right) \times 1 \text{ V} = 11 \text{ V}$$

The gain is $\frac{V_o}{V_1} = \frac{11}{1} = 11$

The current I_1 is

$$I_1 = \frac{V_A}{R_1} = \frac{1}{10 \times 10^3} V = 0.1 \text{ mA}$$

The load current I_L is

$$I_L = \frac{V_o}{R_L} = \frac{11}{10 \times 10^3} = 1.1 \text{ mA}$$

The current I_o is equal to

$$I_o = I_1 + I_L = (0.1 + 1.1) \text{ mA} = 1.2 \text{ mA}$$

5.4 VOLTAGE FOLLOWER

The voltage follower is a circuit in which the output voltage follows the input voltage. Figure 5.7 shows a typical voltage follower circuit. As output voltage follows the input voltage, V_o will be equal to V_{in}.

The potential at node A is V_{in}. As V_i = 0, V_A= V_B = V_{in}. It is clear from Fig. 5.7 that the output terminal is directly connected with node B. The potential at node B is V_B = V_o.

Therefore, we can write, V_o = V_{in}.

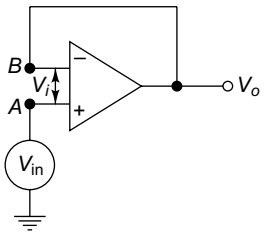


Fig. 5.7 ***Voltage follower***

As output voltage is equal to input voltage, the voltage gain of the voltage follower circuit is unity.

This circuit is also known as buffer circuit with high input impedance and zero output impedance.

5.5 ADDER OR SUMMING AMPLIFIER

Operational amplifiers can be used as adder circuits whose output is the sum of two or more input signals. Such a circuit is called a summing amplifier. There are two types of summing amplifiers such as inverting summing amplifier and non-inverting summing amplifier. In this section, both inverting and non-inverting summing amplifiers are explained.

5.5.1 Inverting Summing Amplifier

Figure 5.8 shows an inverting summing amplifier with two inputs V_1 and V_2, two input resistors R_1 and R_2, and a feedback resistor R_f. Assume operational amplifier is an ideal one. Therefore, $A_v = \infty$, $R_i = \infty$ and $V_i = 0$.

Hence, the non-inverting input terminal has ground potential as a virtual ground ($V_A = 0$)

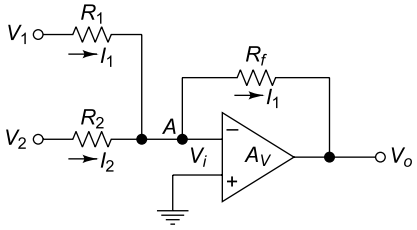


Fig. 5.8 *Inverting summing amplifier*

The current flows through R_1 is

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1}$$

The current flows through R_2 is

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2 - 0}{R_2} = \frac{V_2}{R_2}$$

The current flows through R_f is

$$I_f = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f} = -\frac{V_o}{R_f}$$

Applying KCL law at node A, we can write

$$I_1 + I_2 = I_f$$

or, $$\frac{V_1}{R_1} + \frac{V_2}{R_2} = -\frac{V_o}{R_f}$$

or, $$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right)$$

Therefore, the output voltage is an inverted weighted sum of two inputs. If $R_1 = R_2 = R_f = R$, the output voltage can be expressed as

$$V_o = -\left(V_1 + V_2\right)$$

Hence, the circuit acts as an inverting adder circuit.

When $R_1 = R_2 = 2R_f$, output voltage will be $V_o = -\left(\frac{V_1 + V_2}{2}\right)$

Thus the output voltage is the average of the two input voltages V_1 and V_2.

5.5.2 Non-inverting Summing Amplifier

A non-inverting summing amplifier with two inputs V_1 and V_2, two input resistors R_1 and R_2, and a feedback resistor R_f is shown in Fig. 5.9. Assume, the voltage at inverting (–) input terminal is V_A and the voltage at non-inverting (+) input terminal is also V_A.

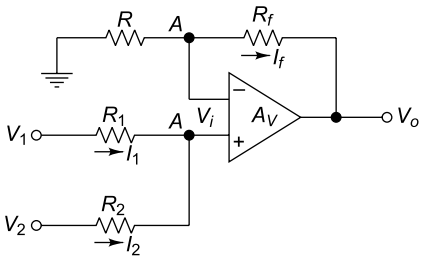


Fig. 5.9 ***Non-inverting summing amplifier***

Apply KCL law at node *A*, we can write

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} = 0$$

or,
$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{V_A}{R_1} + \frac{V_A}{R_2} = \left(\frac{1}{R_1} + \frac{1}{R_2}\right) V_A$$

or,
$$V_A = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}}$$

The non-inverting operational amplifier with resistors R_f and R has output voltage

$$V_o = \left(1 + \frac{R_f}{R}\right) V_A$$

Then, the output voltage can be expressed as

$$V_o = \left(1 + \frac{R_f}{R}\right) \times \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}}$$

The above expression is a non-inverted weighted sum of inputs.

If $R_1 = R_2 = R = R_f$, the output voltage is equal to $V_o = V_1 + V_2$

5.5 Figure 5.10 shows an adder circuit with $V_1 = 1$ V, $V_2 = 2$ V and $V_3 = -2$ V. Determine the output voltage V_o. Assume $R_1 = 2$ kΩ, $R_2 = 1$ kΩ, $R_3 = 2$ kΩ and $R_f = 4.7$ kΩ

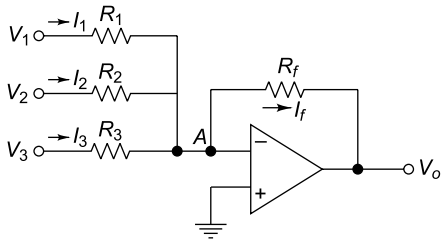


Fig. 5.10 *Circuit of Ex. 5.5*

Solution The output voltage of inverting amplifier is

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

$$= -\left(\frac{4.7}{2}\times 1 + \frac{4.7}{1}\times 2 + \frac{4.7}{2}(-2)\right)\text{V}$$

$$= -7.05\text{ V}$$

5.6 Figure 5.11 shows an operational amplifier circuit with R_1 = 1 kΩ, R_2 = 2 kΩ, and R_f = 10 kΩ. Derive the output voltage V_o expression in terms of V_1 and V_2.

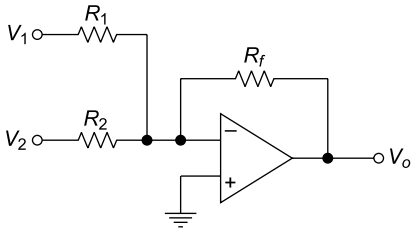


Fig. 5.11 *Circuit of Ex. 5.6*

Solution The output voltage of amplifier can be expressed as

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right)$$

$$= -\left(\frac{10\times 10^3}{1\times 10^3}\times V_1 + \frac{10\times 10^3}{2\times 10^3}\times V_2\right)\text{V} = -(10V_1 + 5V_2)$$

5.7 Implement the equation $V_o = -2V_1 - 7V_2$ using an operational amplifier circuit. Assume minimum value of resistance is 5 kΩ.

Solution The output voltage of amplifier circuit with two input voltages V_1 and V_2 as shown in Fig. 5.12 can be expressed as

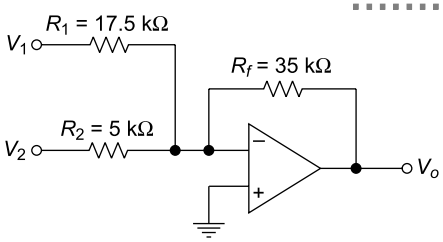


Fig. 5.12 *Circuit of Ex. 5.7*

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right) = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$$

The given output voltage is $V_o = -2V_1 - 7V_2$

Therefore, $\frac{R_f}{R_1} = 2$ and $\frac{R_f}{R_2} = 7$

Assume the value of resistance R_2 is 5 kΩ
Then feedback resistance is equal to $R_f = 7R_2 = 7 \times 5\ \text{k}\Omega = 35\ \text{k}\Omega$

The resistance of R_1 will be $R_1 = \frac{R_f}{2} = \frac{35}{2}\ \text{k}\Omega = 17.5\ \text{k}\Omega$

5.8 Figure 5.13 shows an amplifier circuit. Determine the output voltage V_o and currents I_L and I_o.

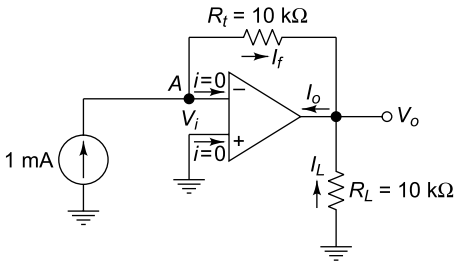


Fig. 5.13 ***Circuit of Ex. 5.8***

Solution In an ideal operational amplifier, input impedance is infinite and the input current, i is equal to zero. Hence the source current 1 mA flows through $R_f = 10\ \text{k}\Omega$.

The output voltage of amplifier circuit is

$$V_o = -I_f R_f = -1 \times 10^{-3} \times 10 \times 10^3 = -10\ \text{V}$$

The load current is

$$I_L = \frac{V_o}{R_L} = \frac{10}{10 \times 10^3} = 1\ \text{mA}$$

The current I_o is equal to

$$I_o = I_f + I_L = (1 + 1) = 2\ \text{mA}$$

5.9 An operational amplifier circuit is shown in Fig. 5.14. Determine the output voltage V_o and current flows through R_1, R_2, R_3 and R_f. Assume $V_1 = 2$ V, $V_2 = -2$ and $V_3 = 3$ V

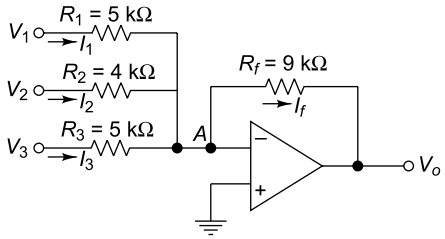


Fig. 5.14 ***Circuit of Ex. 5.9***

Solution The current flows through R_1 is

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1} = \frac{2}{5 \times 10^3} \text{ A} = 0.4 \text{ mA}$$

The current flows through R_2 is

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2 - 0}{R_2} = \frac{V_2}{R_2} = -\frac{2}{4 \times 10^3} \text{ A} = -0.5 \text{ mA}$$

The current flows through R_3 is

$$I_3 = \frac{V_3 - V_A}{R_3} = \frac{V_3 - 0}{R_3} = \frac{V_3}{R_3} = \frac{3}{5 \times 10^3} \text{ A} = 0.6 \text{ mA}$$

The current flows through R_f is

$$I_1 + I_2 + I_3 = I_f = (0.4 - 0.5 + 0.6) \text{ mA} = 0.5 \text{ mA}$$

The output voltage is equal to

$$V_o = -I_f R_f = -0.5 \times 10^{-3} \times 9 \times 10^3 \text{ V} = -4.5 \text{ V}$$

5.6 SUBTRACTOR OR DIFFERENCE AMPLIFIER

A difference amplifier is a circuit that amplifies the difference between two signals. It is also called a differential amplifier or a subtractor. Figure 5.15 shows a typical difference amplifier. In this circuit voltage V_1 is applied to operational amplifier-A (OP-AMP-A) with a gain = 1. Output of OP-AMP-A is V_{o1} and V_2 voltages are applied to OP-AMP-B with a gain = 1. Then output voltage of OP-AMP-B will be the difference between V_1 and V_2.

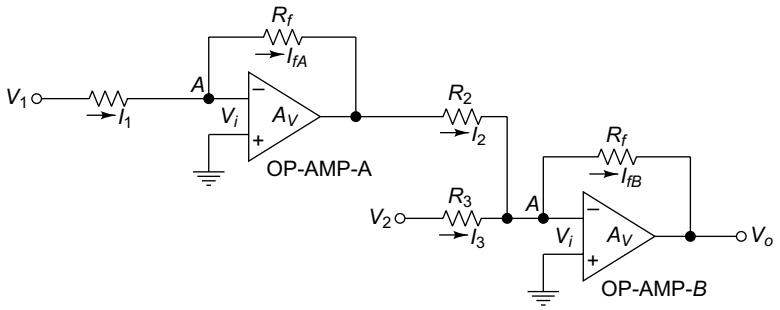


Fig. 5.15 ***Difference amplifier using two OPAMPs***

The output voltage of OP-AMP-A is

$$V_{o1} = -\frac{R_f}{R_1} V_1$$

If $R_f = R_1$, $V_{o1} = -V_1$

The output voltage of OP-AMP-B is V_o

$$V = -\frac{R_f}{R_2} V_{o1} - \frac{R_f}{R_3} V_2$$

If $R_f = R_2 = R_3$, $V_o = -V_{o1} - V_2$

As $V_{o1} = -V_1$, we can write $V_o = -(-V_1) - V_2 = V_1 - V_2$

5.7 DIFFERENCE AMPLIFIER WITH ONE OP-AMP

A typical differential amplifier with one operational amplifier is shown in Fig. 5.16. Assume the differential voltage between inverting (–) and non-inverting (+) terminals of operational amplifier is zero. Potential at *A* and potential at *B* are same potential. So that $V_A = V_B$.

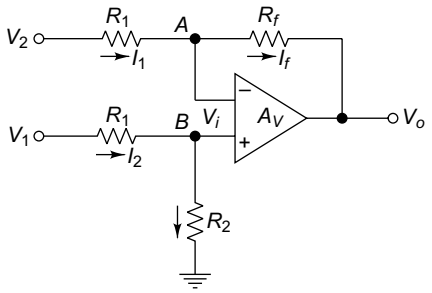


Fig. 5.16 *Difference amplifier using one OP-AMP*

The nodal equation at node *B* is

$$\frac{V_1 - V_B}{R_1} = \frac{V_B - 0}{R_2}$$

or, $$\frac{V_1}{R_1} = \frac{V_B}{R_1} + \frac{V_B}{R_2} = V_B\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = V_B\frac{R_1 + R_2}{R_1 R_2}$$

or, $$V_B = V_1\frac{R_2}{R_1 + R_2}$$

or, $$V_A = V_1\frac{R_2}{R_1 + R_2} \text{ as } V_A = V_B$$

Applying KCL at node *A* we can write

$$I_1 = I_f$$

or, $$\frac{V_2 - V_A}{R_1} = \frac{V_A - V_o}{R_f}$$

or, $$\frac{R_f}{R_1}V_2 - \frac{R_f}{R_1}V_A - V_A = -V_o$$

or, $$V_o = \left(1 + \frac{R_f}{R_1}\right)V_A - \frac{R_f}{R_1}V_2$$

$$= \left(1 + \frac{R_f}{R_1}\right)\frac{R_2}{R_1 + R_2}V_1 - \frac{R_f}{R_1}V_2$$

If $R_f = R_2$, the output voltage $V_o = \frac{R_2}{R_1}V_1 - \frac{R_2}{R_1}V_2 = \frac{R_2}{R_1}(V_1 - V_2)$

This circuit is very useful to detect very small difference between two signals, as the gain $\frac{R_2}{R_1}$ can be considered a large value. For example, when $R_2 = 100\ \text{k}\Omega$ and $R_1 = 1\ \text{k}\Omega$ and gain is 100, the difference potential $(V_1 - V_2)$ will be amplified by 100 times.

5.8 ADDER–SUBTRACTOR

Operational amplifiers can also be used to perform addition and subtraction simultaneously. Figure 5.17 shows the adder cum subtractor circuit. To determine the output voltage, usually Superposition theorem is used. Therefore, to find the output voltage V_o, the input voltages V_1, V_2, V_3 and V_4 are applied separately. When one voltage is applied, other voltages are zero. For example, when V_1 is present in the circuit, the input voltages V_2, V_3 and V_4 are at ground potential. Then output voltage is V_{o1}. Figure 5.18 shows the circuit diagram for this case and its equivalent is depicted in Fig. 5.19.

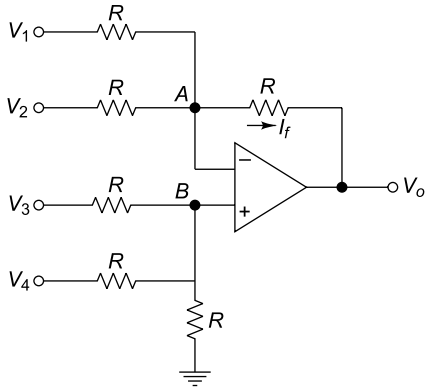


Fig. 5.17 *Adder-subtractor circuit*

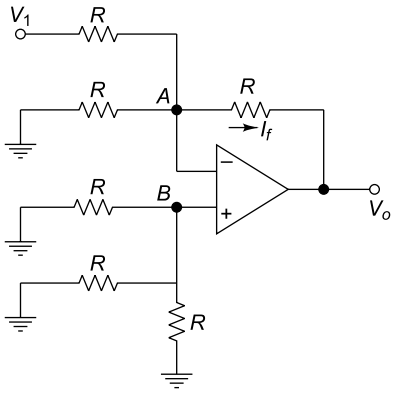


Fig. 5.18 *Adder-subtractor circuit with* $V_2 = V_3 = V_4 = 0$

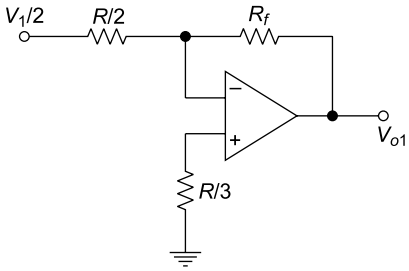


Fig. 5.19 *Equivalent circuit of Fig. 5.18*

The output voltage $V_{o1} = -\dfrac{R}{\frac{R}{2}}\dfrac{V_1}{2} = -V_1$ as $R_f = R$

Similarly, the output voltage for input voltage V_2 is $V_{o2} = -V_2$

Figure 5.20 shows the circuit diagram when V_3 is present and other voltages are zero. This circuit behaves as a non-inverting amplifier.

The voltage at node B is $V_B = \dfrac{\frac{R}{2}}{R+\frac{R}{2}} V_3 = \dfrac{V_3}{3}$

As the voltage difference between A and B is zero, $V_A = V_B$. Hence $V_A = V_B = \dfrac{V_3}{3}$

The output voltage due to input voltage V_3 is

$$V_{o3} = \left(1+\frac{R}{\frac{R}{2}}\right) V_A = 3V_A = 3\frac{V_3}{3} = V_3$$

In the same way, the output voltage due to input voltage V_4 is $V_{o4} = V_4$

After that applying the Superposition theorem, we can find the output voltage V_o due to all four input voltages as given below:

$$\begin{aligned} V_o &= V_{o1} + V_{o2} + V_{o3} + V_{o4} \\ &= -V_1 - V_2 + V_3 + V_4 \\ &= (V_3 + V_4) - (V_1 + V_2) \end{aligned}$$

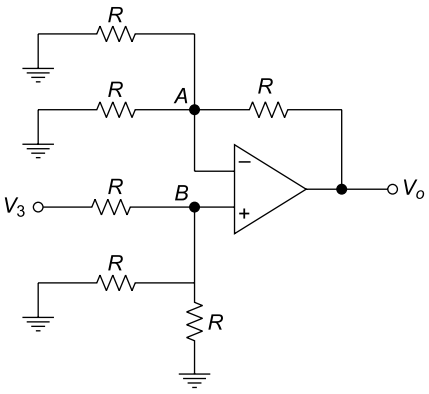


Fig. 5.20 ***Adder-subtractor circuit with $V_1 = V_2 = V_4 = 0$***

5.10 Determine the output voltage V_o for the operational amplifier circuit as shown in Fig. 5.21. Assume $V_1 = 2$ V, and $V_2 = -1$ V

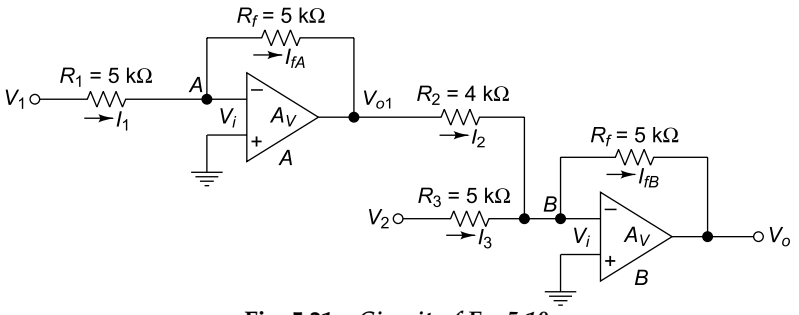


Fig. 5.21 ***Circuit of Ex. 5.10***

Solution The output voltage of operational amplifier $-A$ is V_{o1}

$$V_{o1} = -\frac{R_f}{R_1}V_1 = -\frac{5}{5}\times 2\ V = -2\ \text{V}$$

The output voltage of operational amplifier $-B$ is V_o

$$V_o = -\frac{R_f}{R_2}V_{o1} - \frac{R_f}{R_3}V_2 = -\frac{5}{4}\times(-2) - \frac{5}{5}\times(-1)\ \text{V} = 3.5\ \text{V}$$

5.11 Derive the expression of output voltage V_o for the operational amplifier circuit as shown in Fig. 5.22. Assume $R_1 = 10\ \text{k}\Omega$, $R_2 = 5\ \text{k}\Omega$, $R_3 = 10\ \text{k}\Omega$ and $R_f = 10\ \text{k}\Omega$.

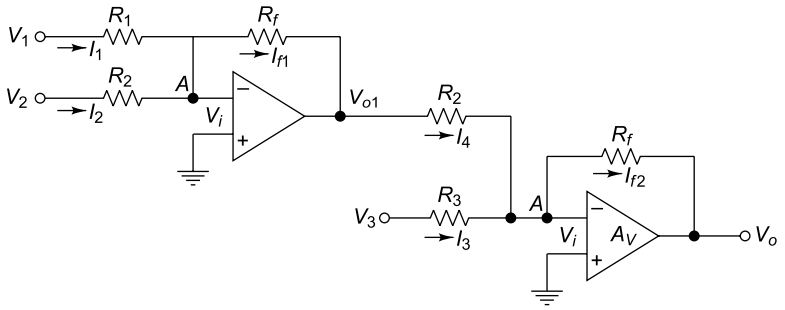


Fig. 5.22 ***Circuit of Ex. 5.11***

Solution The output voltage of first operational amplifier is V_{o1}

$$V_{o1} = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$$

$$= -\frac{10}{10}V_1 - \frac{10}{5}V_2 = -V_1 - 2V_2$$

The output voltage of second operational amplifier is V_o

$$V_o = -\frac{R_f}{R_2}V_{o1} - \frac{R_f}{R_3}V_3$$

$$= -\frac{10}{5}V_{o1} - \frac{10}{10}V_3$$

$$= -2V_{o1} - V_3 = -2(-V_1 - 2V_2) - V_3$$

$$= 2V_1 + 4V_2 - V_3$$

5.12 Figure 5.23 shows an operational amplifier circuit. Determine the current I_f and the output voltage V_o when $V_1 = 4$ V and $V_2 = 5$ V.

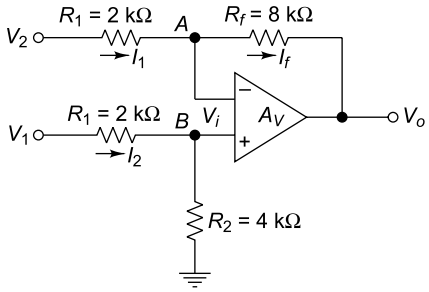


Fig. 5.23 ***Circuit of Ex. 5.12***

Solution The voltage at point B is

$$V_B = \frac{R_2}{R_1 + R_2} V_1 = \frac{4}{4+2} \times 4 \text{ V} = 2.66 \text{ V}$$

In an ideal operational amplifier, the inverting terminal voltage V_A is equal to the non-inverting terminal voltage V_B. Hence $V_A = V_B = 2.66$ V.

The current I_1 is

$$I_1 = \frac{V_2 - V_A}{R_1} = \frac{5 - 2.66}{2 \times 10^3} \text{ A} = 1.17 \text{ mA}$$

As the current input to inverting terminal is zero, $I_f = I_1$

Therefore, $I_f = 1.17$ mA

The output voltage of operational amplifier is V_o

As $I_f = \frac{V_A - V_o}{R_f}$, the voltage is $V_o = I_f R_f + V_A$

$= (1.17 \times 10^{-3} \times 8 \times 10^3 + 2.66)$ V = 12.02 V

5.13 Determine the common mode rejection ratio (CMRR) of the differential amplifier as shown in Fig. 5.24.

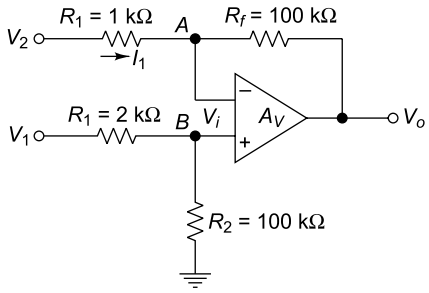


Fig. 5.24 ***Circuit of Ex. 5.13***

Solution The voltage at point B is

$$V_B = \frac{R_2}{R_1 + R_2} V_1 = \frac{100}{100+2} V_1 = \frac{100}{102} V_1$$

In an ideal operational amplifier, the inverting terminal voltage V_A is equal to the non-inverting terminal voltage V_B. Hence $V_A = V_B = \frac{100}{102} V_1$.

The current through resistance R_f is

$$I_f = \frac{V_A - V_o}{R_f} = \frac{V_2 - V_A}{R_1}$$

Therefore $V_A - V_o = \frac{R_f}{R_1} (V_2 - V_A) = \frac{100}{1} (V_2 - V_A) = 100\ V_2 - 100\ V_A$

Then output voltage is equal to

$$V_o = V_A + 100\ V_A - 100\ V_2 = 101\ V_A - 100\ V_2$$

After substituting V_A, we get

$$V_o = 101 \times \frac{100}{102} V_1 - 100\ V_2 = 99.019\ V_1 - 100\ V_2$$

Assume $V_1 = V_C + \frac{V_d}{2}$ and $V_2 = V_C - \frac{V_d}{2}$

The output voltage in terms of V_C and V_d is

$$V_o = 99.019\ V_1 - 100\ V_2$$

$$= 99.019\left(V_C + \frac{V_d}{2}\right) - 100\left(V_C - \frac{V_d}{2}\right)$$

$$= (99.019 - 100)\ V_C + (45.5095 + 50)\ V_d = -0.981\ V_C + 95.5095\ V_d$$

This output voltage can also be expressed as

$$V_o = A_C V_C + A_d V_d$$

Therefore, $A_C = 0.981$ and $A_d = 95.5095$

The common mode rejection ratio is

$$\text{CMRR} = \frac{A_d}{A_C} = \frac{95.5095}{0.981} = 97.35$$

5.14 Figure 5.25 shows an operational amplifier circuit. Determine the output voltage V_o.

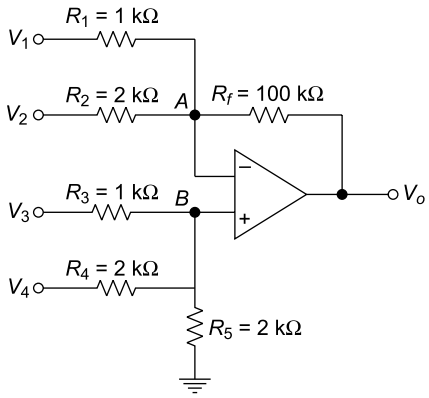


Fig. 5.25 *Circuit of Ex. 5.14*

Solution If the input voltages $V_3 = V_4 = 0$, the output voltage of operational amplifier circuit is

$$V_{o12} = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$$

$$= -\frac{100}{1}V_1 - \frac{100}{2}V_2 = -100\,V_1 - 50\,V_2$$

When input voltages $V_1 = V_2 = 0$, the equivalent circuit is shown in Fig. 5.26 while V_3 is present in the circuit and $V_4 = 0$.

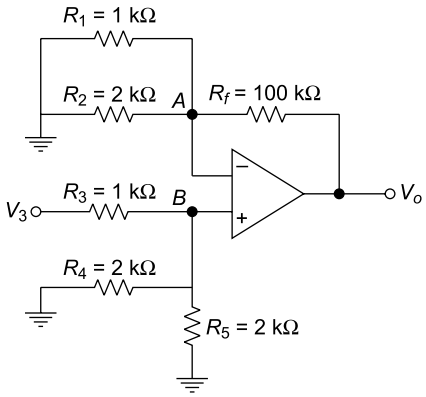


Fig. 5.26 ***Equivalent circuit of Ex. 5.14***

The potential at point B is

$$V_B = \frac{R_5 \parallel R_4}{R_5 \parallel R_4 + R_3}V_3 = \frac{2 \parallel 2}{2 \parallel 2 + 1}V_3 = \frac{V_3}{2} \qquad \text{as} \quad R_5 \parallel R_4 = 2 \parallel 2 = 1\ \text{k}\Omega$$

Then output voltage is

$$V_{o3} = \left(1 + \frac{R_f}{R_1 \parallel R_2}\right)V_A = \left(1 + \frac{100}{1 \parallel 2}\right)V_B \qquad \text{as} \quad V_A = V_B$$

Since $R_1 \parallel R_2 = 1 \parallel 2\ \text{k}\Omega = 0.67\ \text{k}\Omega$ and $V_B = \dfrac{V_3}{2}$, the output voltage is equal to

$$V_{o3} = \left(1 + \frac{100}{0.67}\right)\frac{V_3}{2} = 75.126\ \text{V}_3$$

Similarly, when input voltages $V_1 = V_2 = 0$, the equivalent circuit is shown in Fig. 5.27 while V_4 is present in the circuit and $V_3 = 0$.

The potential at point B is

$$V_B = \frac{R_5 \parallel R_3}{R_5 \parallel R_3 + R_4}V_4$$

As $R_5 \parallel R_3 = 2 \parallel 1 = 0.67\ \text{k}\Omega$

=

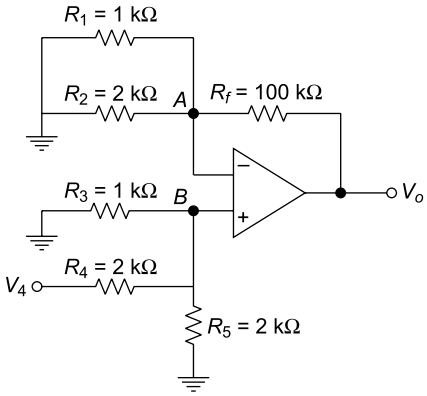


Fig. 5.27 ***Equivalent circuit of Ex. 5.14***

$$\frac{2\|1}{2\|1+2}V_4 = \frac{0.67}{0.67+2}V_4 = 0.250\,V_4$$

Then output voltage is

$$V_{o4} = \left(1+\frac{R_f}{R_1 \| R_2}\right)V_A = \left(1+\frac{100}{1\|2}\right)V_B \qquad \text{as } V_A = V_B$$

Since $R_1 \| R_2 = 1\| 2\ \text{k}\Omega = 0.67\ \text{k}\Omega$ and $V_B = 0.250\ V_4$, the output voltage is equal to

$$V_{o3} = \left(1+\frac{100}{0.67}\right)\times 0.250\ V_4 = 37.563\ V_4$$

Then output voltage V_o is equal to

$$\begin{aligned} V_o &= V_{o12} + V_{o3} + V_{o4} \\ &= -100\,V_1 - 50\,V_2 + 75.126\,V_3 + 37.563\,V_4 \end{aligned}$$

5.9 VOLTAGE-TO-CURRENT CONVERTER

Voltage-to-current converters are commonly used for analog systems, meters and relays, etc. Figure 5.28 shows the circuit diagrams of voltage to current converter.

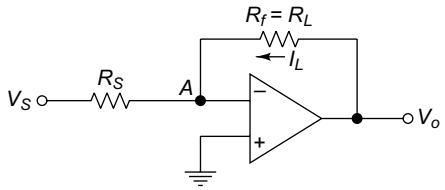


Fig. 5.28 *Voltage-to-current converter*

The current flows through resistance R_f is equal to

$$\frac{V_S - V_A}{R_S} = \frac{V_A - V_o}{R_L} = -I_L$$

Since $V_A = 0$, the above equation can be written as $\dfrac{V_S - 0}{R_S} = \dfrac{0 - V_o}{R_L} - I_L$

or, $$\frac{V_S}{R_S} = \frac{V_o}{R_L} = -I_L$$

or, $$I_L = -\frac{V_S}{R_S}$$

It is clear from the above expression that the output current is independent of the load resistance R_L and the circuit acts as a constant current source as V_S is constant. When one end of load is grounded and the load current is controlled by input voltage, a different circuit will be used for voltage to current converter. Figure 5.29 shows the voltage to current converter when the load is not floating type.

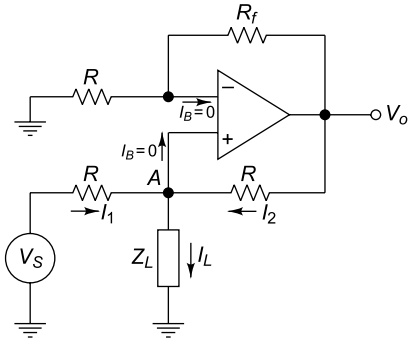


Fig. 5.29 *Voltage-to-current converter when load is not floating type*

Applying KCL at node *A*, we get $I_1 + I_2 = I_L$

where, current $I_1 = \dfrac{V_S - V_A}{R}$, current $I_2 = \dfrac{V_o - V_A}{R}$ and current $I_L = \dfrac{V_A}{Z_L}$

After substituting the value of I_1, I_2 and I_L, we obtain

$$\frac{V_S - V_A}{R} + \frac{V_o - V_A}{R} = I_L$$

or, $$\frac{V_S + V_o - 2V_A}{R} = I_L$$

or, $$V_A = \frac{V_S + V_o - I_L R}{2}$$

Since the operational amplifier operates in non-inverting mode, the gain of the circuit is $\left(1 + \dfrac{R_f}{R}\right)$.

If $R_f = R$, the gain of the circuit will be 2 and the output voltage can be expressed as

$$V_o = \left(1 + \frac{R_f}{R}\right) V_A = 2\ V_A$$

or, $$V_o = 2V_A = 2\left(\frac{V_S + V_o - I_L R}{2}\right)$$

or, $$V_o = V_S + V_o - I_L R$$

Therefore, $V_S = I_L R$ and load current will be

$$I_L = \frac{V_S}{R}$$

This equation states that the load current depends on the input voltage V_S and resistor *R* only.

5.10 CURRENT-TO-VOLTAGE CONVERTER

The output signal of photo cells, photodiodes and photovoltaic cells is current and its magnitude is directly proportional to intensity of light or incident radiant energy. The current output from these devices can be converted to voltage by using a voltage-to-current converter. Then the voltage will be measured to indicate the intensity of light or radiant energy incident on the photo devices.

The current-to-voltage (*I* to *V*) converter is shown in Fig. 5.30. As the inverting terminal is virtually ground, current flows through R_S is zero and I_S current flows through the feedback resistance R_f.

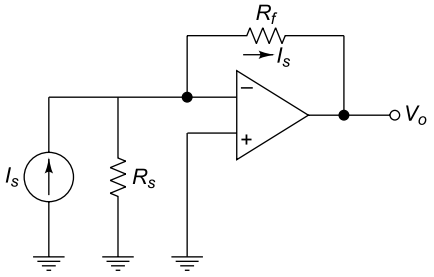


Fig. 5.30 ***Current-to-voltage converter***

Hence, the output voltage can be expressed as $V_o = -I_S R_f$. The *I* to *V* converters are commonly used in digital-to-analog converter (DAC) as DAC output is a current signal which is proportional to the digital input.

5.11 INTEGRATOR

5.11.1 Inverting Integrator

When the feedback resistance R_f is interchanged with a capacitor in an ideal inverting mode operational amplifier, the circuit works as an integrator. Figure 5.31 shows an integrator circuit where input voltage is V_{in}.

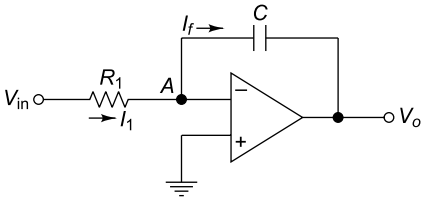


Fig. 5.31 *Integrator*

The current flows through R_1 is

$$I_1 = \frac{V_{\text{in}} - V_A}{R_1}$$

As non-inverting terminal is at ground potential, node *A* will also be at ground potential or virtual ground. Then $V_A = 0$.

So that $I_1 = \dfrac{V_{\text{in}}}{R_1}$

The current flows through capacitor is

$$I_f = C\frac{d\left(V_A - V_o\right)}{dt} = -C\frac{dV_o}{dt}$$

Applying KCL at node *A*, we get

$$I_1 = I_f$$

or, $$\frac{V_{\text{in}}}{R_1} = -C\frac{dV_o}{dt}$$

or, $$\frac{dV_o}{dt} = -\frac{1}{R_1 C}V_{\text{in}}$$

After integrating both sides, we get

$$\int dV_o = -\frac{1}{R_1 C}\int V_{\text{in}}\, dt$$

So, $$V_o(t) = -\frac{1}{R_1 C}\int_0^t V_{\text{in}}\, dt + V_0(0)$$

where, $V_o(0)$ is the initial output voltage. Therefore, this circuit provides an output signal which is the integral of the input voltage.

5.11.2 Non-inverting Integrator

Figure 5.32 shows the circuit diagram of a non-inverting integrator. In this circuit, the negative input terminal is connected to ground through R. The input voltage V_{in} is applied through resistor R. The voltage at non-inverting terminal is same as inverting terminal voltage which is equal to V_A.

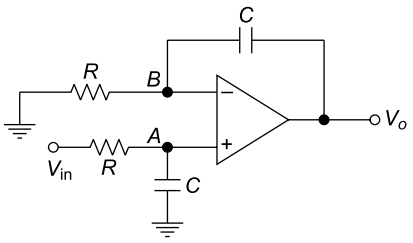


Fig. 5.32 *Non-inverting integrator*

Applying KCL at node A, we can write

$$\frac{V_{in} - V_A}{R} = \frac{V_A - 0}{\frac{1}{sC}}$$

or, $V_{in} - V_A = sCRV_A$

or, $V_{in} = (1 + sCR)\, V_A$

Applying KCL at node B, we get

$$\frac{V_o - V_B}{\frac{1}{sC}} = \frac{V_B - 0}{R}$$

or, $$V_o - V_B = \frac{1}{sC}\frac{V_B}{R} = \frac{V_B}{sCR}$$

or, $$V_o = V_B + \frac{V_B}{sCR} = \left(1 + \frac{1}{sCR}\right)V_B = \frac{sCR+1}{sCR}V_B$$

As $V_A = V_B$, we can write

$$V_o = \frac{sCR+1}{sCR}V_A$$

or, $$V_o = \frac{sCR+1}{sCR}\frac{V_{in}}{sCR+1} = \frac{V_{in}}{sCR} \quad \text{as } V_A = \frac{V_{in}}{1+sCR}$$

Since $\frac{1}{s} = \int$, we can write $V_o = \frac{1}{CR}\int V_{in}\, dt$

5.11.3 Practical Integrator

There are two sources of error at output voltage in an ideal integrator as given below:

- A very small dc offset voltage is present at the operational amplifier input.
- Input bias current flows through the feedback capacitor.

The above two effects will be integrated with respect to time and generate a continuously rising output voltage till the operational amplifier will saturate. Therefore,

this ideal integrator circuit can be used as integrator over a time range and before starting operation, the circuit must be recycled. Recycling can limit the output error voltage within an acceptable range. The bias current can be minimised by increasing C_f and simultaneously reducing the value of R_1. The limitations of an ideal integrator can be minimised if the feedback capacitor C_f is shunted by resistance R_f as depicted in Fig. 5.33.

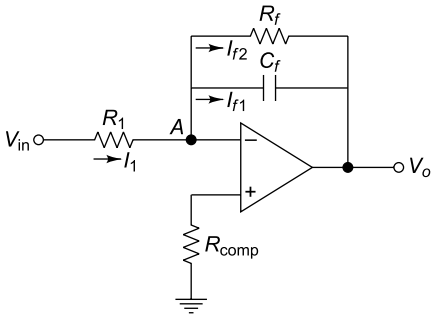


Fig. 5.33 *Practical integrator*

The parallel combination of R_f and C_f works like a practical capacitor, the circuit is also known as lossy integrator. The R_f resistor limits the low-frequency gain operational amplifier to $\frac{R_f}{R_1}$. The resistance R_{comp} is used to reduce the error due to bias current.

The equivalent impedance is equal to

$$Z_{eq} = R_f \| C_f$$

$$= \frac{R_f \frac{1}{sC_f}}{R_f + \frac{1}{sC_f}} = \frac{\frac{R_f}{sC_f}}{\frac{sC_f R_f + 1}{sC_f}}$$

$$= \frac{R_f}{1 + sC_f R_f}$$

Applying KCL at node A, we get

$$\frac{V_{in} - V_A}{R_1} = \frac{V_A - V_o}{Z_{eq}}$$

or, $$\frac{V_{in} - 0}{R_1} = \frac{0 - V_o}{Z_{eq}} \quad \text{as node } A \text{ is virtual ground , } V_A = 0$$

or, $$\frac{V_{in}}{R_1} = \frac{-V_o}{Z_{ep}}$$

The output voltage can be expressed as

$$V_o = -Z_{eq} \frac{V_{in}}{R_1}$$

After substituting the value of Z_{eq} in the above equation, we get

$$V_o = -\frac{R_f}{1 + sC_f R_f} \frac{V_{in}}{R_1} \quad \text{as} \quad Z_{eq} = \frac{R_f}{1 + sC_f R_f}$$

$$= -\frac{R_f}{R_1}\frac{1}{1+sC_fR_f}V_{\text{in}}$$

$$= -\frac{R_f}{R_1+sC_fR_fR_1}V_{\text{in}}$$

$$= -\frac{1}{\frac{R_1}{R_f}+sC_fR_1}V_{\text{in}}$$

If R_f is very large, $\frac{R_1}{R_f}$ can be neglected and the lossy integrator behaves as an ideal integrator. Then output voltage is equal to

$$V_o = -\frac{1}{sC_fR_f}V_{\text{in}}$$

As $\frac{1}{s} = \int dt$, we can write $V_o = -\frac{1}{R_1C_f}\int V_{\text{in}}\,dt$

After substituting $s = j\omega$, the magnitude of the gain of lossy integrator can be computed as

$$|A| = \left|\frac{V_o}{V_{\text{in}}}\right| = \frac{\frac{R_f}{R_1}}{\sqrt{1+\omega^2C_f{}^2R_f{}^2}}$$

Practical integrators are commonly used in

- Analog computation
- Ramp waveform generator
- ADC (analog to digital converter)
- Different wave-shaping circuits

5.11.4 Summing Integrator

The summing integrator amplifier can be used to integrate more than one input signal. A typical two inputs summing integral circuits is given in Fig. 5.34, where V_1 and V_2 are inputs.

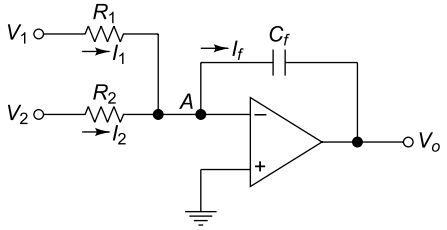


Fig. 5.34 *Summing integrator*

Assume inverting terminal of operation amplifier is at virtual ground. So that, $V_A = 0$.

Applying KCL at node *A,* we get

$$I_1 + I_2 = I_f$$

After substituting the value of currents, we obtain

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} = \frac{V_A - V_o}{\frac{1}{sC_f}}$$

or, $$\frac{V_1}{R_1} + \frac{V_2}{R_2} = -sC_f V_o$$

or, $$V_o = -\frac{1}{sC_f R_1} V_1 - \frac{1}{sC_f R_2} V_2$$

As $\frac{1}{s} = \int dt$, we can write

$$V_o = -\frac{1}{R_1 C_f} \int V_1 dt - \frac{1}{R_2 C_f} \int V_2 dt$$

$$= -\frac{1}{C_f} \int \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} \right) dt$$

It is clear from the above expression that the output voltage is the sum of the integration of two input signals. In the same way, more than two voltages will also be integrated.

5.15 Derive the output voltage of the integrating operational amplifier circuit as shown in Fig. 5.35. Assume operational amplifier is an ideal one.

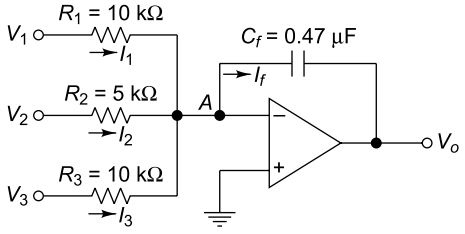


Fig. 5.35 ***Circuit of Ex. 5.15***

Solution The current flowing through resistance R_1 is

$$I_1 = \frac{V_1}{R_1} = \frac{V_1}{10} \text{ mA}$$

The current flowing through resistance R_2 is

$$I_2 = \frac{V_2}{R_2} = \frac{V_2}{5} \text{ mA}$$

The current flowing through resistance R_3 is

$$I_3 = \frac{V_3}{R_3} = \frac{V_3}{10} \text{ mA}$$

Then current flowing through capacitor C_f is

$$\begin{aligned} I_f &= I_1 + I_2 + I_3 \\ &= \frac{V_1}{10} + \frac{V_2}{5} + \frac{V_3}{10} \text{ mA} \end{aligned}$$

The output voltage will be

$$\begin{aligned} V_o &= -\frac{1}{R_1 C_f}\int V_1 dt - \frac{1}{R_2 C_f}\int V_2 dt - \frac{1}{R_3 C_f}\int V_3 dt \\ &= -\frac{1}{C_f}\int\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)dt \\ &= -\frac{1}{0.47\times 10^{-6}}\int\left(\frac{V_1}{10} + \frac{V_2}{5} + \frac{V_3}{10}\right)\times 10^{-3} dt \\ &= -\int\left(2.1276\, V_1 + 4.2552\, V_2 + 2.1276\, V_3\right)dt \end{aligned}$$

5.16 Prove that the operational amplifier circuit as shown in Fig. 5.36 is an integrator. Assume operational amplifier is an ideal one.

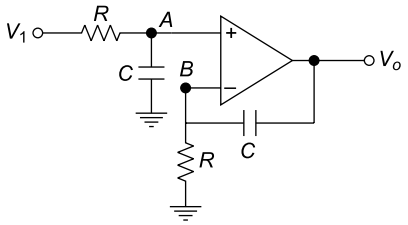


Fig. 5.36 ***Circuit of Ex. 5.16***

Solution The voltage at node *A* is

$$V_A = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_1 = \frac{1}{1 + sCR} V_1$$

As operational amplifier is an ideal one, the voltage at node *B* is equal to node *A* voltage.

Hence, $$V_B = V_A = \frac{1}{1 + sCR} V_1$$

The output voltage can be expressed as

$$V_o = \left(1 + \frac{\frac{1}{sC}}{R}\right) V_A = \frac{1 + sCR}{sCR} V_A$$

After substituting the value of V_A, we get

$$V_o = \frac{1 + sCR}{sCR} V_A = \frac{1 + sCR}{sCR} \frac{1}{1 + sCR} V_1 = \frac{1}{sCR} V_1$$

As $\frac{1}{s} = \int dt$, we can write

$$V_o = \frac{1}{RC} \int V_1 dt$$

Hence, it is proved that the operational amplifier circuit as shown in Fig. 5.36 is an integrator.

5.17 Prove that the output voltage of Fig. 5.37 is $V_o = \frac{2}{CR} \int V_1 \, dt$

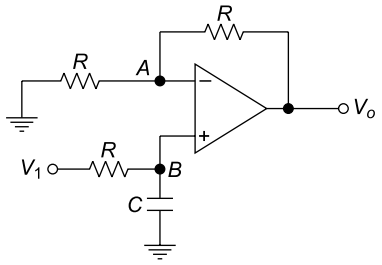


Fig. 5.37 *Circuit of Ex. 5.17*

Solution The potential at node *B* is

$$V_B = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_1 = \frac{1}{1 + sCR} V_1$$

Since the operational amplifier is an ideal one, the voltage at node *A* is equal to node *B* voltage.

Therefore, $V_B = V_A = \frac{1}{1 + sCR} V_1$

The output voltage can be expressed as

$$V_o = \left(1 + \frac{R}{R}\right) V_A = 2V_A$$

After substituting the value of V_A, we get

$$V_o = \frac{2}{1 + sCR} V_1 = \frac{1}{sCR} V_1 \qquad \text{assuming } sCR >> 1$$

As $\frac{1}{s} = \int dt$, we can write

$$V_o = \frac{2}{CR} \int V_1 dt$$

5.18 In an integrator circuit as shown in Fig. 5.38, the value of *RC* is 1 second. Find out the output voltage at $t = 1$ second, $t = 2$ seconds and $t = 3$ seconds when input voltage is 2 V.

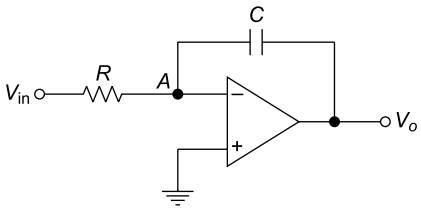


Fig. 5.38 *Circuit of Ex. 5.18*

Solution Given $RC = 1$ second and $V_{in} = 2$ V

The output voltage of integrator is

$$V_o = -\frac{1}{RC} \int V_{in}\, dt = -\frac{1}{1} \int 2dt \text{ V} = -\int 2dt \text{ V}$$

The output voltage at $t = 1$ second

$$V_o = -\int_0^1 2dt = -2 \text{ V}$$

The output voltage at $t = 2$ second

$$V_o = -\int_0^2 2dt = -4 \text{ V}$$

The output voltage at $t = 3$ second

$$V_o = -\int_0^3 2dt = -6 \text{ V}$$

5.19 Figure 5.39 shows an integrator circuit. Find out the output voltage when input voltage is $2 \sin 1000\pi t$ and show the output voltage waveform.

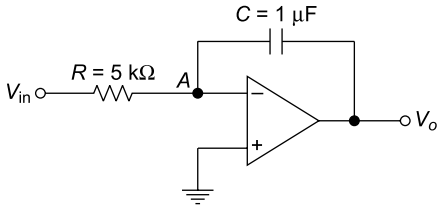


Fig. 5.39 *Circuit of Ex. 5.19*

Solution The input voltage is $V_{in} = 2 \sin 1000\, \pi t$

The output voltage is

$$V_o = -\frac{1}{RC}\int V_{\text{in}}\, dt$$

$$= -\frac{1}{5\times10^3\times1\times10^{-6}}\int (2\sin 1000\,\pi t)\, dt$$

$$= -400\int \sin 1000\,\pi t\, dt$$

$$= -400\times\frac{1}{1000\,\pi}\times(-\cos 1000\,\pi t) = 0.1273\cos 10000\,\pi t \text{ V}$$

The waveform of input voltage and output voltage are shown in Fig. 5.40(a) and (b)

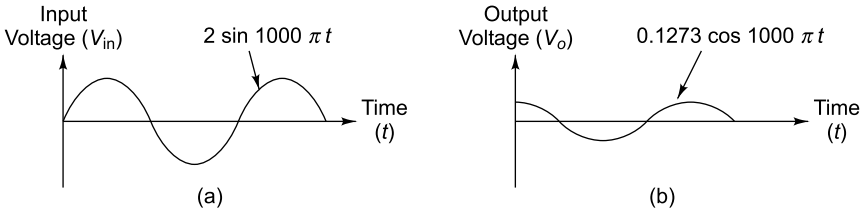


Fig. 5.40 ***Waveforms of input and output voltages***

5.20 When a step voltage input is applied to an integrator circuit from 0 to 0.5 ms as shown in Fig. 5.41, find out the output voltage at $t = 0.5$ milisecond.

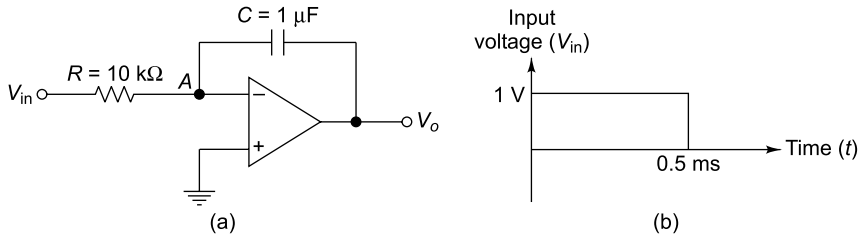


Fig. 5.41 ***Circuit of Ex. 5.20***

Solution The output voltage is

$$V_o = -\frac{1}{RC}\int V_{\text{in}}\, dt$$

$$= -\frac{1}{10\times10^3\times1\times10^{-6}}\int_0^{0.5\,\text{ms}} 1\, dt \text{ V}$$

$$= -100\left[t\right]_0^{0.5\,\text{ms}} \text{ V} = -100\times0.5\times10^{-3} \text{ V} = -50 \text{ mV}$$

5.21 If a square wave is applied as input voltage to an integrator circuit as shown in Fig. 5.42, find out the output voltage. Assume $RC = 0.1$second.

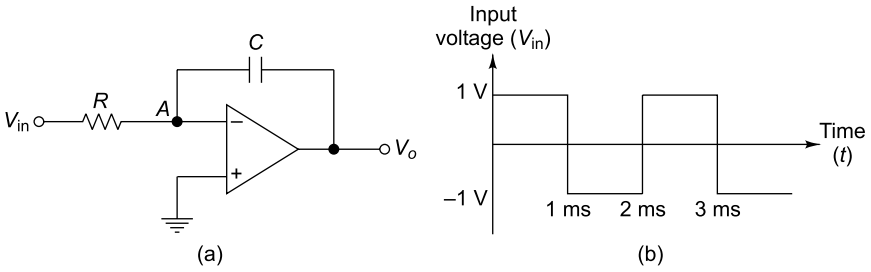


Fig. 5.42 ***(a) Circuit (b) Input voltage of Ex. 5.21***

Solution During $t = 0$ to $t = 1$ ms, the input voltage, V_{in} is 1 V.

At $t = 1$ ms, the output voltage is

$$V_o = -\frac{1}{RC}\int V_{in}\, dt$$

$$= -\frac{1}{0.1}\int_0^{1\text{ms}} 1dt \text{ V}$$

$$= -10\left[t\right]_0^{1\text{ ms}} \text{V} = -10 \times 1 \times 10^{-3} \text{ V} = -10 \text{ mV}$$

During $t = 1$ ms to $t = 2$ ms, the input voltage, V_{in} is –1 V.

At $t = 2$ ms, the output voltage is

$$V_o = -\frac{1}{RC}\int V_{in}\, dt$$

$$= -\frac{1}{0.1}\int_{1\text{ ms}}^{2\text{ ms}} (-1)\, dt + V_o(t = 1\text{ ms}) \text{ V}$$

$$= 10\left[t\right]_{1\text{ ms}}^{2\text{ ms}} + V_o(t = 1\text{ ms}) \text{ V} = 10 \times 1 \times 10^{-3} \text{ V} - 10 \text{ mV} = 0 \text{ V}$$

The output voltage waveform will be a triangular in nature as shown in Fig. 5.43.

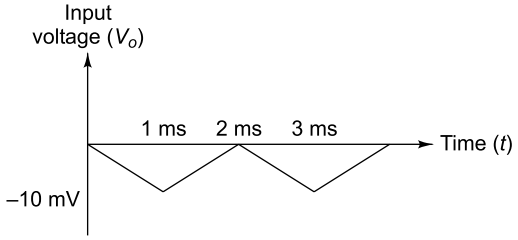


Fig. 5.43 ***Output voltage waveform of Ex. 5.21***

5.12 DIFFERENTIATOR

When the positions of resistor R and capacitor C in the integrator are interchanged, the integrator works as a differentiator. The circuit diagram of a differentiator is shown in Fig. 5.44. The potential at A is V_A and it is zero as the inverting terminal of operational amplifier is virtually ground.

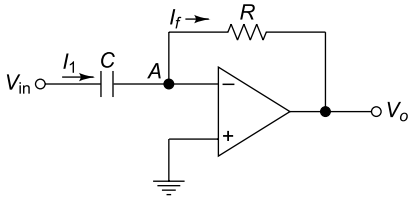


Fig. 5.44 *Differentiator*

Applying KCL at node A, we get

$$I_1 = I_f$$

or, $$C\frac{d(V_{in} - V_A)}{dt} = \frac{V_A - V_o}{R}$$

or, $$C\frac{dV_{in}}{dt} = -\frac{V_o}{R}$$

or, $$V_o = -CR\frac{dV_{in}}{dt}$$

Hence the output voltage is proportional to the derivative of the input voltage V_{in}. When $V_{in} = \sin \omega t$ is applied at the input terminal of the differentiator, the output is $V_o = -CR\omega \cos \omega t$. It means that output voltage proportionately increase linearly with signal frequency. Due to high-frequency signal, a frequency noise component greatly enhances signal distortions. Therefore, differential is usually avoided in high-frequency operations. At low frequency, the output voltage amplitude increases linearly with frequency which leads to use the differentiator as frequency to voltage converter.

5.12.1 Practical Differentiator

The limitations of a differentiator circuit are stability and noise problems at high frequency. These limitations can be eliminated by using practical differentiation. Figure 5.45 shows the circuit diagram of a practical differentiator. In this circuit, the resistance R_1 in series with a capacitor and capacitor C_f is connected in parallel with resistance R_f. The R_{comp} is used for bias compensation.

As R_1 and C_1 are connected in series, the equivalent impedance is equal to

$$Z_1 = R_1 + \frac{1}{sC_{in}} = \frac{sC_{in}R_1 + 1}{sC_{in}}$$

Since R_f and C_f are connected in parallel, the equivalent impedance is

$$Z_2 = \frac{R_f \dfrac{1}{sC_f}}{R_f + \dfrac{1}{sC_f}} = \frac{R_f}{1 + sR_fC_f}$$

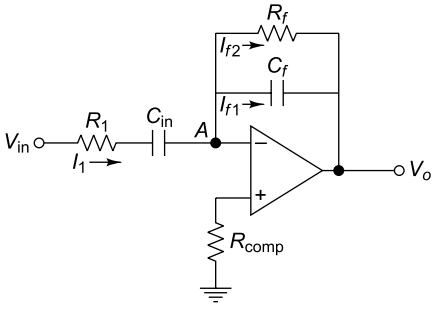


Fig. 5.45 *Practical differentiator*

As point A is virtual ground, $V_A = 0$

Applying KCL at node A, we can write

$$\frac{V_{\text{in}} - V_A}{Z_1} = \frac{V_A - V_o}{Z_2}$$

or, $$\frac{V_{\text{in}}}{Z_1} = \frac{-V_o}{Z_2}$$

or, $$\frac{V_{\text{in}}}{\frac{sC_{\text{in}}R_1 + 1}{sC_{\text{in}}}} = -\frac{V_o}{\frac{R_f}{1 + sR_fC_f}}$$

or, $$V_o = -\frac{R_f}{1 + sR_fC_f}\frac{sC_{\text{in}}}{sC_{\text{in}}R_1 + 1}V_{\text{in}}$$

or, $$V_o = -\frac{sR_fC_{\text{in}}}{(1 + sR_fC_f)(1 + sC_{\text{in}}R_1)}V_{\text{in}}$$

If $R_fC_f = R_1C_{\text{in}}$, the output voltage can be expressed as

$$V_o = -\frac{sR_fC_{\text{in}}}{(1 + sC_{\text{in}}R_1)^2}V_{\text{in}}$$

As the time constant R_fC_{in} is greater than R_fC_f or R_1C_{in}, the above equation becomes

$$V_o = -sR_fC_1V_{\text{in}}$$

Since $s = \frac{d}{dt}$, the output voltage can be expressed as $V_o = -R_fC_1\frac{d(V_{\text{in}})}{dt}$.

Hence, the output voltage is the R_fC_1 times the differentiation of the input voltage. Practical differentiators are used in

- Rate of change detector in FM demodulations
- Different wave-shaping circuits

5.12.2 Summing Differentiator

The summing differentiator circuit is shown in Fig. 5.46.

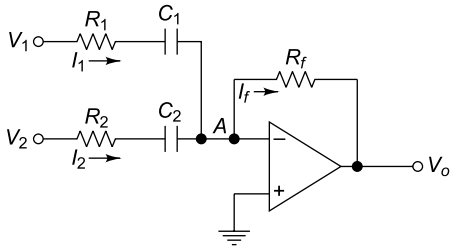


Fig. 5.46 *Summing differentiator*

Apply KCL at node *A*, we can write

$$I_1 + I_2 = I_f$$

After substituting the values of currents I_1, I_2 and I_f, we get

$$\frac{V_1 - V_A}{Z_1} + \frac{V_2 - V_A}{Z_2} = \frac{V_A - V_o}{R_f}$$

Assume inverting terminal is virtually ground, so that $V_A = 0$

Then $$\frac{V_1}{Z_1} + \frac{V_2}{Z_2} = -\frac{V_o}{R_f} \tag{5.1}$$

The equivalent impedance Z_1 is

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{sC_1R_1 + 1}{sC_1}$$

The equivalent impedance Z_2 is

$$Z_2 = R_2 + \frac{1}{sC_2} = \frac{sC_2R_2 + 1}{sC_2}$$

After substituting the values of currents Z_1, and Z_2 in Eq. 5.1, we obtain

$$\frac{V_1}{\frac{sC_1R_1 + 1}{sC_1}} + \frac{V_2}{\frac{sC_2R_2 + 1}{sC_2}} = -\frac{V_o}{R_f}$$

or, $$\frac{sC_1}{1 + sC_1R_1}V_1 + \frac{sC_2}{1 + sC_2R_2}V_2 = -\frac{V_o}{R_f}$$

or, $$V_o = -\frac{sC_1R_f}{1 + sC_1R_1}V_1 - \frac{sC_2R_f}{1 + sC_2R_2}V_2$$

If $C_1R_f >> C_1R_1$ and $C_2R_f >> C_2R_2$, we can get

$$V_o = -sC_1R_fV_1 - sC_2R_fV_2$$

As $s = \frac{d}{dt}$, the output voltage can be expressed as

$$V_o = -C_1R_f\frac{dV_1}{dt} - C_2R_f\frac{dV_2}{dt}$$

The above equation states that the output is the sum of the differentiation of input voltage V_1 and V_2.

5.22 Figure 5.47 shows a differentiation circuit. Draw the output voltage waveform when input voltage is $V_{in} = 2 \sin 100\,\pi t$. Assume $CR = 0.01$ second.

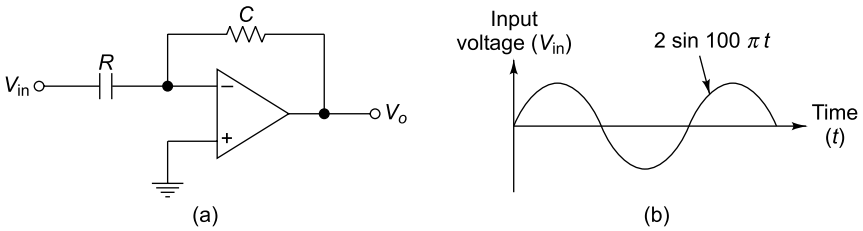


Fig. 5.47 *Circuit of Ex. 5.22*

Solution The output voltage of differentiation circuit is

$$V_o = -CR\frac{dV_{in}}{dt}$$

$$= -0.01\frac{d}{dt}(2\sin 100\pi t)$$

$$= -0.01 \times 2 \times 100\pi \cos 100\pi t$$

$$= -6.28\cos 100\pi t$$

The output voltage waveform is shown in Fig. 5.48.

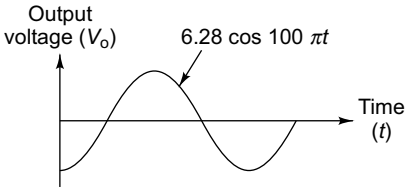


Fig. 5.48 *Output voltage waveform of Ex. 5.22*

5.23 Figure 5.49(a) shows a differentiation circuit. When a square wave input voltage as shown in Fig. 5.49(b) is applied to the differentiation circuit, what will be the output voltage waveform?

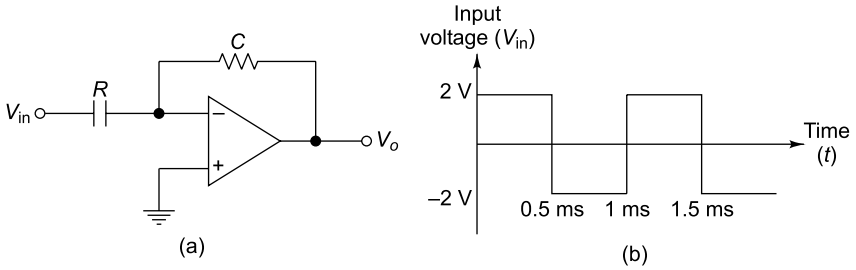


Fig. 5.49 *(a) Circuit (b) Input voltage of Ex. 5.23*

Solution The square wave input voltage has 2 V peak voltage and 1 kHz frequency. When the square wave input voltage is applied to the differentiation circuit, positive and negative spikes or impulse signal will be generated at output. The magnitude of the spikes will be about $\pm V_{saturation}$ that is approximately ±13 V or ±15 V.

When the input voltage changes from –2 V to +2 V, impulse signal will be negative. While the input voltage changes from +2 V to –2 V, impulse signal will be positive. During the time periods for which input voltage is constant at either +2 V or –2 V, there will be no output voltage as the differentiated of input voltage is zero. Figure 5.50 shows the output voltage waveform with respect to input voltage.

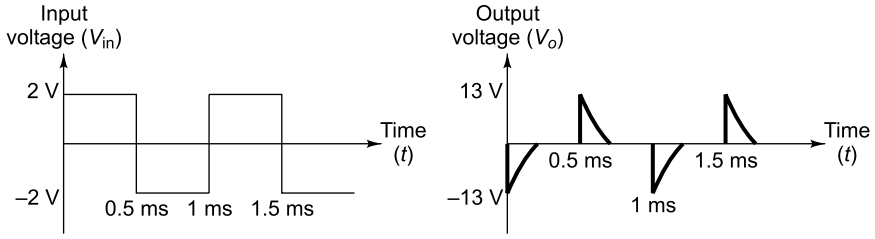


Fig. 5.50 *Output voltage waveform of Ex. 5.23*

5.13 LOGARITHMIC AMPLIFIER

The log and antilog amplifiers are nonlinear circuits where the output voltage is proportional to the exponent or logarithm of the input voltage. Usually, to perform multiplication and division in electronic circuits, addition and subtraction of logs are used. The other applications of log amplifiers are powers, roots, compression, decompression, true RMS detection and process control . There are two basic circuits of logarithmic amplifiers such as

- Diode connected transistor
- Transdiode

But most commonly, log amplifiers are diode-connected transistor log amplifiers In this section, the basic operation of a log amplifier is discussed.

In a logarithmic amplifier, the output voltage is directly proportional to the logarithm of the input voltage

$$\text{so that } V \propto \log V_i$$

where V_i is input voltate V_o is output voltage.

When the linear operational amplifier is combined with a nonlinear device such as diode or transistor, a logarithmic amplifier circuit can be achieved.

Figure 5.51 shows a logarithmic amplifier. In this circuit, collector (C) and emitter (E) terminal are connected between inverting terminal and output. Base of transistor (BJT) is grounded. The inverting terminal, A is virtually ground and $V_A = 0$

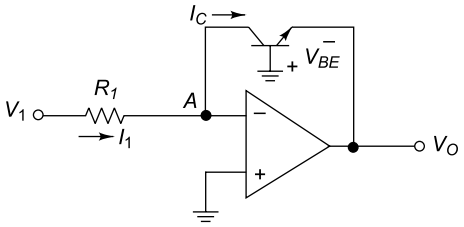


Fig. 5.51 *Logarithmic amplifier*

The transistor emitter current is

$$I_E = I_S \left(e^{\frac{qV_{BE}}{KT}} - 1 \right)$$

where I_s is emitter saturation current = 10^{-13} A

K is Boltzmann's constant = 8.62×10^{-5} eV/°K or 1.38×10^{-23} J/°K

T is absolute temperature in °K

q is the charge of electron = 1.6×10^{-19} C

As base of the transistor is grounded, $I_E = I_C$

Therefore, transistor collector current is equal to

$$I_C = I_S\left(e^{\frac{qV_{BE}}{KT}} - 1\right)$$

or, $$\frac{I_C}{I_S} = e^{\frac{qV_{BE}}{KT}} - 1$$

or, $$\frac{I_C}{I_S} + 1 = e^{\frac{qV_{BE}}{KT}}$$

As $I_C >> I_S$, we can write the above expression as $\frac{I_C}{I_S} = e^{\frac{qV_{BE}}{KT}}$

Taking log on both the sides, we find

$$\log\frac{I_C}{I_S} = \frac{qV_{BE}}{KT}$$

or, $$V_{BE} = \frac{KT}{q}\log\frac{I_C}{I_S}$$

The current flows through resistance R_1 is $I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1}$ (as $V_A = 0$)

Applying KCL at node A, we get

$$I_1 = I_C = \frac{V_1}{R_1}$$

or, $$V_{BE} = \frac{KT}{q}\log\frac{V_1}{I_S R_1}$$

Since the emitter of BJT is connected to the output of operational amplifier, the output voltage is equal to

$$V_o = -V_{BE} = -\frac{KT}{q}\log\left(\frac{V_1}{I_S R_1}\right)$$

Assume reference voltage $V_{\text{ref}} = I_S R_1$. Then we can obtain the output voltage as

$$V_o = -\frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}}$$

From the above expression, it is clear that the output voltage is proportional to the logarithm of the input voltage.

Disadvantages of Logarithm Amplifier The disadvantages of this amplifier are the following:

(i) The output voltage depends on temperature (T) and reverse saturation current (I_S).

(ii) The emitter saturation current varies from one transistor to other transistor and its magnitude also depends on temperature (T).

(iii) Therefore, temperature affects amplifier performance and accuracy and these effects can be reduced by temperature compensating circuits.

In this section, temperature-compensated logarithmic amplifier has been discussed.

Figure 5.52 shows a logarithmic amplifier with saturation current and temperature compensation. The input voltage V_1 is applied to one log-amplifier and a reference voltage V_{ref} is applied to another log amplifier. The two transistors T_1 and T_2 are integrated close together in the same silicon wafer. Hence, there is a close match of saturation currents and temperature tracking ensure very good result.

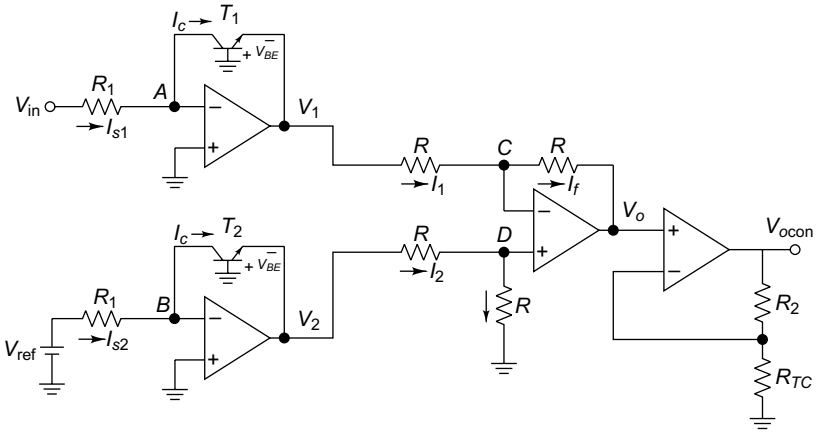


Fig. 5.52 ***Log amplifier with saturation and temperature compensation***

Assume the saturation current of transistor T_1 is equal to the saturation current of transistor T_2. Therefore, $I_{S1} = I_{S2} = I_S$

The output voltage V_1 can be expressed as

$$V_1 = -\frac{KT}{q}\log\left(\frac{V_{\text{in}}}{I_S R_1}\right)$$

In the same way, the output voltage V_2 will be

$$V_2 = -\frac{KT}{q}\log\left(\frac{V_{\text{ref}}}{I_S R_1}\right)$$

Then output voltage $V_o = V_2 - V_1$

After substituting the values of V_1 and V_2 in the above equation, we get

$$V_o = \frac{KT}{q}\left[\log\left(\frac{V_{\text{in}}}{I_S R_1}\right) - \log\left(\frac{V_{\text{ref}}}{I_S R_1}\right)\right]$$

or,
$$V_o = \frac{KT}{q}\log\left(\frac{V_{\text{in}}}{V_{\text{ref}}}\right)$$

Hence, the reference voltage level is now set with a single external voltage source. Consequently, output voltage does not depend on device emitter saturation current I_S. The voltage V_o is still dependent upon temperature and it is directly proportional to temperature (T). The temperature effect can be compensated by the last stage operational amplifier which provides a non-inverting gain $\left(1+\frac{R_2}{R_{TC}}\right)$.

Then actual output voltage can be expressed as

$$V_{o\ \text{comp}} = \left(1+\frac{R_2}{R_{TC}}\right)\frac{KT}{q}\log\left(\frac{V_{\text{in}}}{V_{\text{ref}}}\right)$$

where, R_{TC} = temperature sensitive resistance. It has a positive temperature coefficient so that slope of the above equation will be constant with the temperature changes.

As four operational amplifiers are used for temperature-compensated logarithmic amplifier, this circuit becomes expensive if FET operational amplifiers are used for precision. To reduce the circuit cost, two operational amplifiers can be used for log amplifier with same output voltage as depicted in Fig. 5.53.

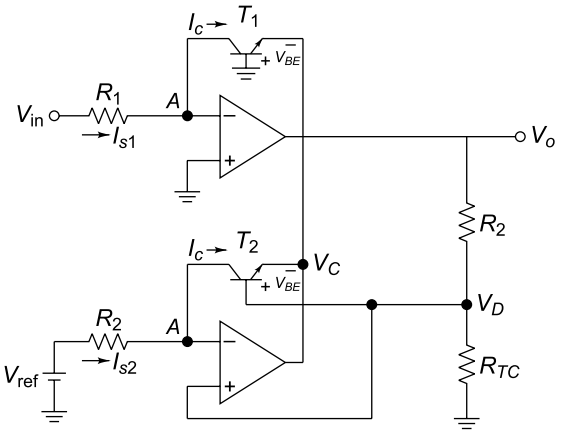


Fig. 5.53 *Log amplifier using two operational amplifiers*

5.14 ANTILOG AMPLIFIER

The antilog of a logarithmic number is a decimal number so that antilog amplifier performs the reverse operation of logarithmic amplifier. Figure 5.54 shows a typical antilog amplifier circuit using a diode. In this circuit, the diode is connected between input signal and inverting terminal of an operational amplifier. The feedback resistance R_f is connected between inverting and output terminals

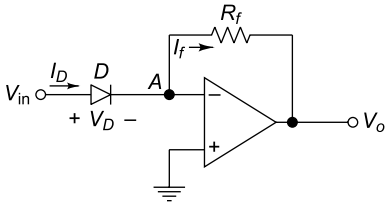


Fig. 5.54 *Antilog amplifier*

of an operational amplifier. As the non-inverting terminal is grounded, node A is at virtual ground and the potential at A is $V_A = 0$.

The current flows through diode is

$$I_D = I_O e^{\frac{V_D}{\tau V_T}}$$

where, I_D is diode current
I_O is reverse saturation current
V_D is diode voltage $\tau = 1$ for Ge diode
$\tau = 2$ for Si diode
V_T is voltage equivalent of temperature = K_T
K is the Boltzmann's constant
T is temperature in °K

Applying KCL at A, we get

$$I_f = I_D$$

The output voltage is

$$V_o = -I_f R_f = -I_o e^{\frac{V_{\text{in}}}{\tau V_T}} R_f$$

Taking log on both sides, we obtain

$$\log V_o = -I_o R_f \log e^{\left(\frac{V_{\text{in}}}{\tau V_T}\right)}$$

or,
$$\log V_o = -I_o R_f \frac{V_{\text{in}}}{\tau V_T}$$

Taking inverse log on both side, we get

$$\log^{-1}(\log V_o) = -I_o R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right)$$

or,
$$V_o = -I_o R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right)$$

It is clear from the above expression that the output V_o is the antilog of input voltage and consequently the amplifier acts as an antilog amplifier.

5.15 ANTILOG AMPLIFIER USING TRANSISTOR

A typical antilog amplifier using transistor is shown in Fig. 5.55.

The collector current can be expressed as

$$I_C = I_o e^{\frac{V_{BE}}{\tau V_T}}$$

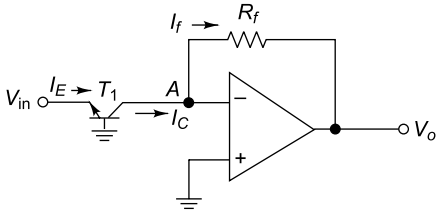


Fig. 5.55 *Antilog amplifier using transistor*

The non-inverting terminal is at ground potential. The node *A* is at virtual ground. Therefore, $V_A = 0$. The base of a transistor is at ground potential and the collector of transistor is at virtual ground. As a result, the voltage across base and emitter of transistor is V_{BE} which is equal to input voltage V_{in} so that $V_{BE} = V_{\text{in}}$

Then collector current is equal to

$$I_C = I_o e^{\frac{V_{\text{in}}}{\tau V_T}}$$

The output voltage can be expressed as

$$V_o = -I_f R_f = -I_o e^{\frac{V_{\text{in}}}{\tau V_T}} R_f \quad (\text{as } I_o = I_f)$$

or,
$$V_o = -I_o R_f e^{\frac{V_{\text{in}}}{\tau V_T}}$$

Taking log on both sides, we get

$$\log V_o = -I_o R_f \log e^{\frac{V_{\text{in}}}{\tau V_T}}$$

or,
$$\log V_o = -I_o R_f \frac{V_{\text{in}}}{\tau V_T}$$

Taking inverse log on both side, we obtain

$$\log^{-1}(\log V_o) = -I_o R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right)$$

So the output voltage will be equal to

$$V_o = -I_o R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right)$$

It is very clear from the above expression that the output voltage V_o is a inverse logarithm of the input voltage V_{in}. In the output voltage equation, I_o and V_T are present. The current I_o and voltage V_T are the functions of temperature. Due to temperature changes, these parameters change and there are serious errors at the output voltage. Therefore, a temperature compensation antilog amplifier must be used in place of simple antilog amplifier.

5.16 ANALOG MULTIPLIER

An analog voltage multiplier is a circuit where the output voltage is directly proportional to the product of the two input voltages. Figure 5.56 shows the circuit diagram of an analog voltage multiplier which consists of log amplifiers, adder circuits and an antilog amplifier.

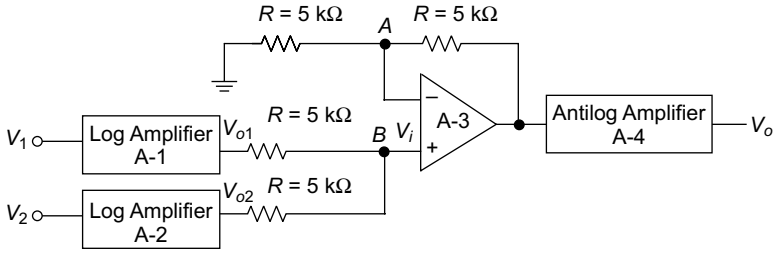


Fig. 5.56 ***Multiplier circuit***

The output log amplifier A_1 is

$$V_{o1} = -\frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}}$$

The output log amplifier A_2 is

$$V_{o2} = -\frac{KT}{q}\log\frac{V_2}{V_{\text{ref}}}$$

The output voltage of adder circuit is

$$V_{o3} = -V_{o1} - V_{o2}$$

After substituting the values of V_{o1} and V_{o2}, we get

$$V_{o3} = -\left(-\frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}}\right)-\left(-\frac{KT}{q}\log\frac{V_2}{V_{\text{ref}}}\right)$$

$$= \frac{KT}{q}\log\frac{V_1}{V_{\text{ref}}}+\frac{KT}{q}\log\frac{V_2}{V_{\text{ref}}}$$

$$= \frac{KT}{q}\log\left(\frac{V_1}{V_{\text{ref}}}\frac{V_2}{V_{\text{ref}}}\right) \text{ (as } \log(AB) = \log A + \log B)$$

The output voltage of antilog amplifier is

$$V_o = -I_o R_f \log^{-1}\left(\frac{V_{o3}}{\tau V_T}\right)$$

After substituting V_{o3} in the above equation, we obtain

$$V_o = -I_o R_f \log^{-1}\left(\frac{1}{\tau V_T}\times\frac{KT}{q}\log\frac{V_1\times V_2}{{V_{\text{ref}}}^2}\right)$$

Assuming $\frac{1}{\tau V_T}\times\frac{KT}{q}$ is about to 1, we get

$$V_o = -I_o R_f \log^{-1}\left(\log\frac{V_1\times V_2}{V_{\text{ref}}^2}\right)$$

Applying $\log^{-1}$ (log) = 1, we find

$$V_o = -I_o R_f \frac{V_1 V_2}{V_{\text{ref}}^2} = KV_1V_2 \text{ where } K = \frac{I_o R_f}{V_{\text{ref}}{}^2}$$

Therefore the output voltage is the product of two input voltages V_1 and V_2.
Analog multipliers are commonly used in

(i) Amplitude modulation, frequency modulation and phase frequency modulation, suppressed carrier frequency modulation
(ii) Phase detection circuit
(iii) Power measurement, velocity and acceleration measurement
(iv) Voltage-controlled attenuators and voltage-controlled amplifiers
(v) Gain of amplifier measurement
(vi) Voltage divider circuit, true RMS calculation
(vii) Frequency converters, and frequency doubling circuits
(viii) Square and square root calculations

5.17 ANALOG DIVIDER

An analog voltage divider is a circuit where the output voltage is directly proportional to the division of the two input voltages. Figure 5.57 shows the circuit diagram of an analog voltage divider which consists of log amplifiers, subtractor circuit and an antilog amplifier.

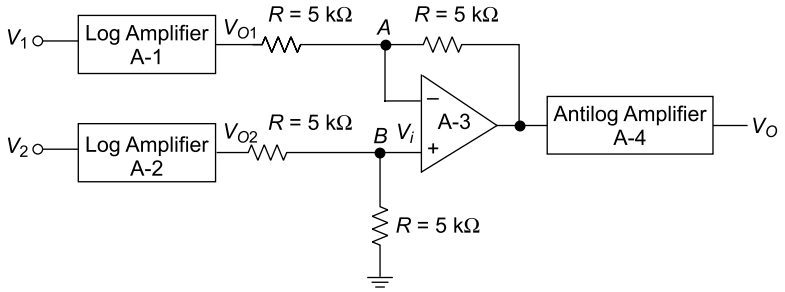


Fig. 5.57 ***Divider circuit***

The output log amplifier A_1 is

$$V_{o1} = -\frac{KT}{q} \log \frac{V_1}{V_{\text{ref}}}$$

The output log amplifier A_2 is

$$V_{o2} = -\frac{KT}{q} \log \frac{V_2}{V_{\text{ref}}}$$

The output voltage of subtractor circuit is

$$V_{o3} = K_1(V_{o2} - V_{o1}) \text{ where } K_1 \text{ is constant}$$

After substituting the value of V_{o1} and V_{o2} in the above equation, we get

$$V_{o3} = K_1 \frac{KT}{q}\left(\log \frac{V_2}{V_{\text{ref}}} - \log \frac{V_1}{V_{\text{ref}}}\right)$$

Applying as $\log\left(\frac{A}{B}\right) = \log A - \log B$, we get

$$V_{o3} = K_2\left(\log \frac{V_2}{V_{\text{ref}}} \times \frac{V_{\text{ref}}}{V_1}\right) = K_2\left(\log \frac{V_2}{V_1}\right) \text{ where } K_2 = K_1 \frac{KT}{q}$$

Hence we can state that output voltage V_{o3} is directly proportional to $\left(\log \frac{V_2}{V_1}\right)$ and we can write

$$V_{o3} \propto \log\left(\frac{V_2}{V_1}\right)$$

The output of antilog amplifier is

$$V_o \propto \log^{-1}(V_{o3})$$

After substituting the value of V_{o3} in the above equation, we get

$$V_o \propto \log^{-1}\left(\log\left(\frac{V_2}{V_1}\right)\right)$$

Applying $\log^{-1}(\log) = 1$, we can express the output voltage as

$$V_o \propto \left(\frac{V_2}{V_1}\right)$$

Hence the output voltage is proportional to the division of the two analog input voltages V_1 and V_2.

5.24 Figure 5.58 shows a log amplifier using OP-AMP and diode. The characteristics of the diode is expressed as $I = I_S\left(e^{\frac{qV_D}{KT}} - 1\right)$.

(a) Determine the output voltage in terms of input voltage V_{in}.

(b) Calculate the output voltage when $\frac{KT}{q}$ = 20 mV, R = 10 kΩ and I_S = 1 μA

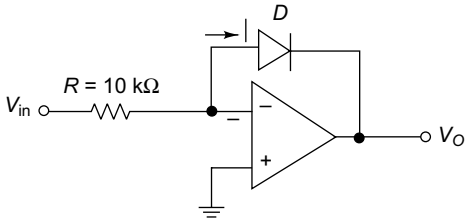


Fig. 5.58 *Circuit of Ex. 5.24*

Solution (a) The current flowing through diode is $I = I_S\left(e^{\frac{qV_D}{KT}} - 1\right)$

Therefore $\frac{I}{I_S} + 1 = e^{\frac{qV_D}{KT}}$

Taking log of both the sides, we get

$$\log\left(\frac{I}{I_S} + 1\right) = \log\left(e^{\frac{qV_D}{KT}}\right)$$

or, $$\frac{qV_D}{KT} = \log\left(\frac{I}{I_S}\right)$$

or, $$V_D = \frac{KT}{q}\log\left(\frac{I}{I_S}\right)$$

As current $I = \frac{V_{\text{in}}}{R}$, the output voltage V_o is equal to V_D and it can be expressed as

$$V_o = V_D = \frac{KT}{q}\log\left(\frac{V_{\text{in}}}{RI_S}\right)$$

(b) Given $\frac{KT}{q}$ = 20 mV, R = 10 kΩ and I_S = 1 μA

The output voltage is

$$V_o = \frac{KT}{q}\log\left(\frac{V_{in}}{RI_S}\right)$$

$$= 20\times10^{-3}\log\left(\frac{0.4}{10\times10^3\times1\times10^{-6}}\right) = 73.77 \text{ mV}$$

5.25 Determine the output voltage V_o of a log amplifier using OP-AMP and transistor as shown in Fig. 5.59. Assume V_{in} = 100 mV, R = 10 kΩ, T = 300°K and $I_S = 10^{-13}$A

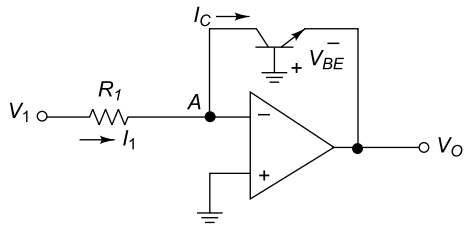


Fig. 5.59 *Circuit of Ex. 5.25*

Solution The output voltage V_o of a log amplifier is

$$V_o = -V_{BE} = -\frac{KT}{q}\log\left(\frac{V_1}{I_S R_1}\right)$$

$$= -\frac{1.38\times10^{-23}\times300}{1.6\times10^{-19}}\log\left(\frac{100\times10^{-3}}{10^{-13}\times10\times10^{3}}\right)\text{ V}$$

$$= -476.635\text{ mV}$$

5.26 Determine the output voltage V_o of an antilog amplifier using OP-AMP and transistor as shown in Fig. 5.60. Assume $V_{\text{in}} = 500$ mV, $R_f = 10$ kΩ, $\tau = 1$, $V_T = 25$ mV and $I_o = 10^{-13}$A.

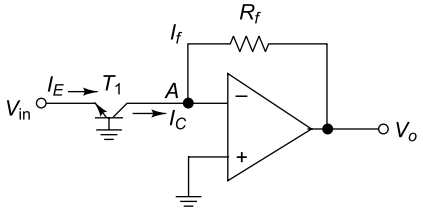


Fig. 5.60 ***Circuit of Ex. 5.26***

Solution The output voltage V_o of a log amplifier is

$$V_o = -I_O R_f \log^{-1}\left(\frac{V_{in}}{\tau V_T}\right)\text{ V}$$

$$= -10^{-13}\times10\times10^{3}\times\log^{-1}\left(\frac{500\times10^{-3}}{1\times25\times10^{-3}}\right)\text{ V}$$

$$= -0.485\text{ V}$$

5.18 COMPARATOR

A comparator is an electronic circuit which is able to compare an input voltage signal (V_{in}) with a known reference voltage (V_{ref}). It is basically an open-loop operational amplifier. The input voltage is applied to one of the input terminals of an OP-AMP and the reference voltage is applied at the other terminal of OP-AMP. The ideal characteristic of a comparator is shown in Fig. 5.61. When the input voltage $V_{\text{in}} > V_{\text{ref}}$, the output voltage is $+V_{\text{saturation}}$ ($+V_{\text{sat}}$). If the input voltage $V_{\text{in}} < V_{\text{ref}}$, the output voltage is $-V_{\text{saturation}}$ ($-V_{\text{sat}}$). Generally, three are two types of comparators such as

- Non-inverting comparators
- Inverting comparators

In this section, both inverting as well as non-inverting comparators are discussed elaborately.

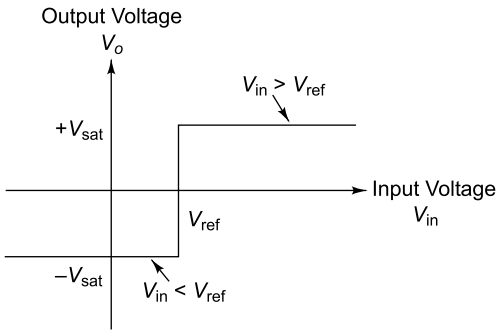


Fig. 5.61 *Transfer characteristic of an ideal comparator when V_{ref} is positive voltage*

5.18.1 Non-inverting Comparator

Figure 5.62 shows a non-inverting comparator. A fixed reference voltage V_{ref} is applied to inverting (–) terminal of OP-AMP through resistance R_2. The time-varying input voltage V_{in} is also applied to non-inverting terminal through resistance R_1. When input voltage V_{in} is less than reference voltage V_{ref}, output voltage will be $-V_{sat}$ ($-V_{CC}$). If the input voltage V_{in} is greater than reference voltage V_{ref}, output voltage will be $+V_{sat}$ ($+V_{CC}$).

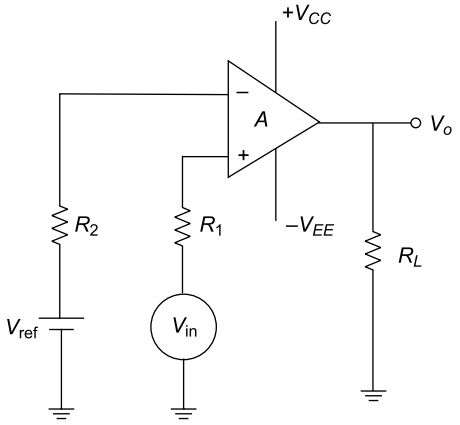


Fig. 5.62 *Non-inverting comparator*

A sinusoidal input voltage $V_m \sin \omega t$ is applied to the positive (+) input terminal and the output voltage will be either $-V_{sat}$ ($-V_{CC}$) or $+V_{sat}$ ($+V_{CC}$) as shown in Fig. 5.63 when voltage is V_{ref} is positive. While the reference voltage is negative, the output voltage waveform is shown in Fig. 5.64.

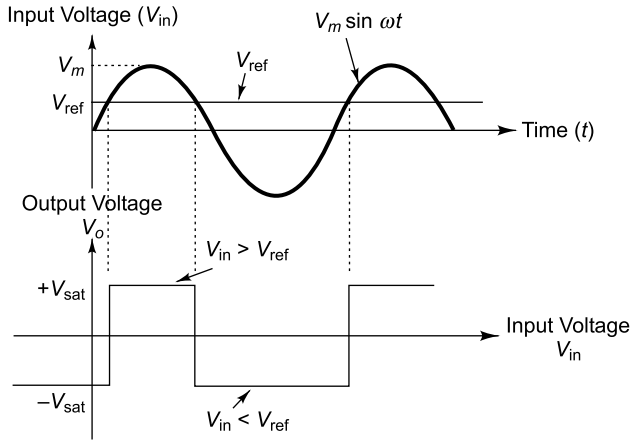


Fig. 5.63 ***Input and output voltage waveforms when V_{ref} is positive***

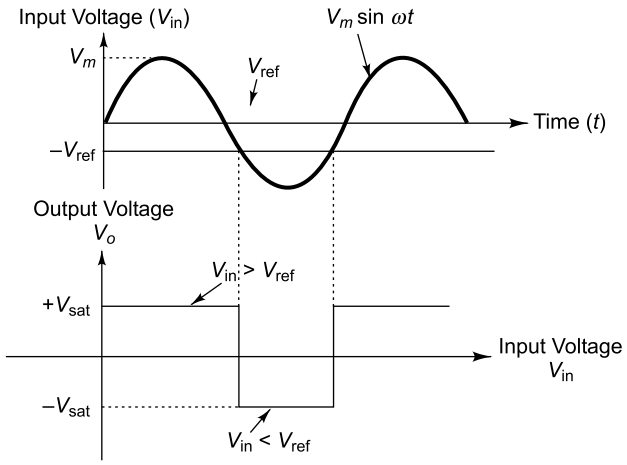


Fig. 5.64 ***Input and output voltage waveforms when V_{ref} is negative***

In a practical comparator circuit, V_{ref} can be obtained from a 10 kΩ variable resistance (potentiometer) which acts as a potential divider. In a 10 kΩ potentiometer, $+V_{CC}$ and $-V_{CC}$ are connected with the two end terminals and the wiper is connected with the inverting (–) input terminal of OP-AMP as shown in Fig. 5.65. Hence the reference voltage can be varied from $+V_{CC}$ to $-V_{CC.}$ When V_{ref} is positive , the output voltage waveform is shown in Fig. 5.63. If V_{ref} is negative, the output voltage waveform is depicted in Fig. 5.64.

In this circuit diodes D_1 and D_2 protects the operational amplifier from excessive input voltage V_{in}. Due to diodes, difference input voltage of operational amplifier is clamped to either + 0.7 V or – 0.7 V. Therefore, these diodes are called as clamp diodes. The resistance R_1 is connected in series with input voltage V_{in} and it is used to limit the current through diodes D_1 and D_2. To reduce the offset problem, a resistance R_2 is connected in series with reference voltage V_{ref}.

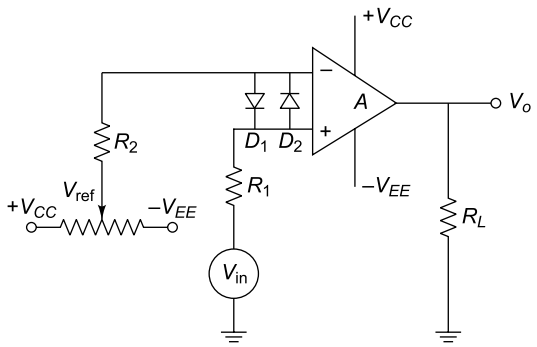


Fig. 5.65 ***Practical non-inverting comparator***

5.18.2 Inverting Comparator

Figure 5.66 shows an inverting comparator. The input voltage V_{in} is applied to inverting (–) terminal through resistance R_1. The fixed reference voltage V_{ref} is applied to non-inverting (+) terminal of OP-AMP through resistance R_2. In a practical inverting comparator, the V_{ref} can as be obtained from a 10 kΩ variable potentiometer which acts as a potential divider. In 10 kΩ potentiometer, $+V_{CC}$ and $-V_{CC}$ are connected with the two end terminals and the wiper is connected with the non-inverting (+) input terminal of OP-AMP. Consequently, by varying the wiper position, the reference voltage can be varied from $+V_{CC}$ to $-V_{CC.}$

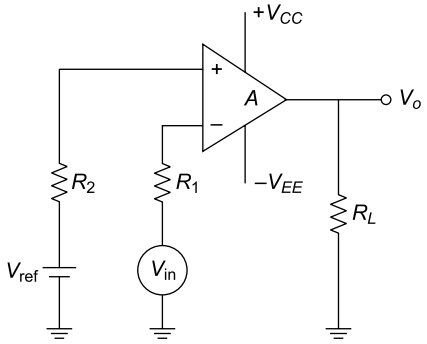


Fig. 5.66 ***Non-inverting comparator***

In inverting comparator, when input voltage V_{in} is less than reference voltage V_{ref}, output voltage will be $+V_{sat}$ $(+V_{CC})$. If the input voltage V_{in} is greater than reference voltage V_{ref}, output voltage will be $-V_{sat}$ $(-V_{CC})$. When a sinusoidal input voltage V_m is applied to the negative (–) input terminal of OP-AMP and the output voltage will be either $+V_{sat}$ $(+V_{CC})$ or $-V_{sat}$ $(-V_{CC})$ as shown in Fig. 5.67 and Fig. 5.68.

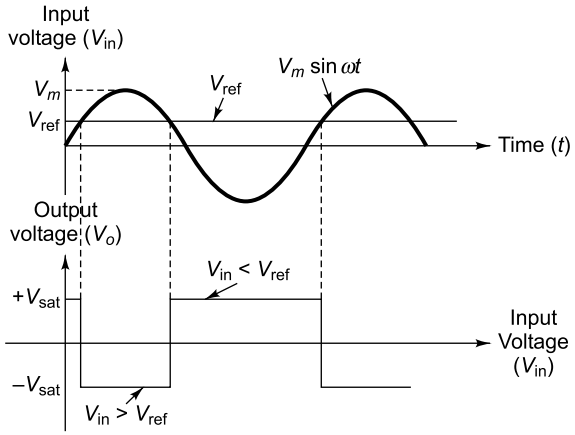


Fig. 5.67 *Input and output voltage waveforms when V_{ref} is positive*

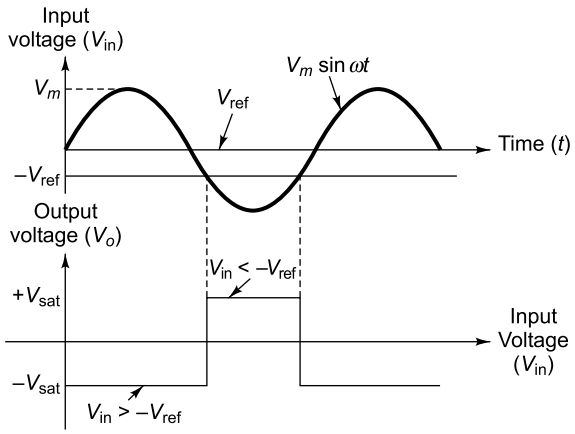


Fig. 5.68 *Input and output voltage waveforms when V_{ref} is negative*

Figure 5.69 shows a practical non-inverting comparator. When two back-to-back zener diodes are connected at the output of OP-AMP, the output voltage will be independent of supply voltage. The R is connected in series with zener diodes to limit the current flows through zener diodes. The limiting output voltage will be $(V_{Z1}+V_D)$ and $-(V_{Z2}+V_D)$ where V_D is the forward voltage drop of diode and V_{Z2} is the voltage across zener diode.

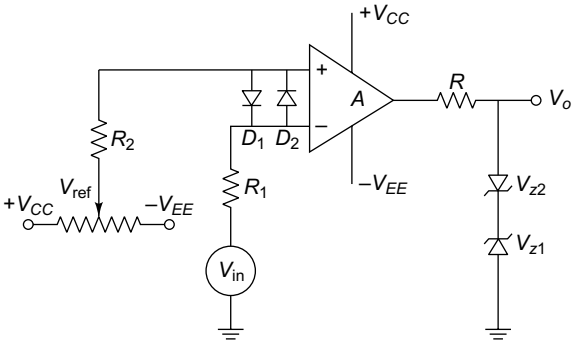


Fig. 5.69 *Practical non-inverting comparator*

5.18.3 Applications of Comparators

Comparators are commonly used in

(i) Zero crossing detector circuit
(ii) Window detector circuit
(iii) Multivibrators
(iv) Time marker generators
(v) Phase meters
(vi) Schmitt trigger

In this section, the operation of Zero Crossing Detector (ZCD) circuit is explained.

Zero Crossing Detector The inverting or non-inverting comparator can be used as a zero crossing detector circuit, when the reference voltage V_{ref} is zero. Figure 5.70 shows an inverting zero crossing detector circuit where $V_{ref} = 0$. In the positive half cycle of supply voltage, $V_{in} > V_{ref}$ and the output voltage is $-V_{sat.}$ During the negative half cycle of supply voltage, $V_{in} < V_{ref}$ and the output voltage is $+V_{sat.}$ The output voltage wave form is shown in Fig. 5.71. This circuit is called a *sine wave to square wave converter.*

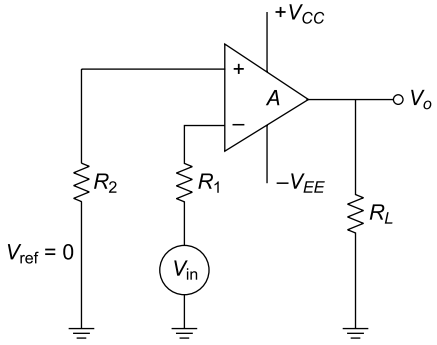


Fig. 5.70 ***Zero crossing detector circuit***

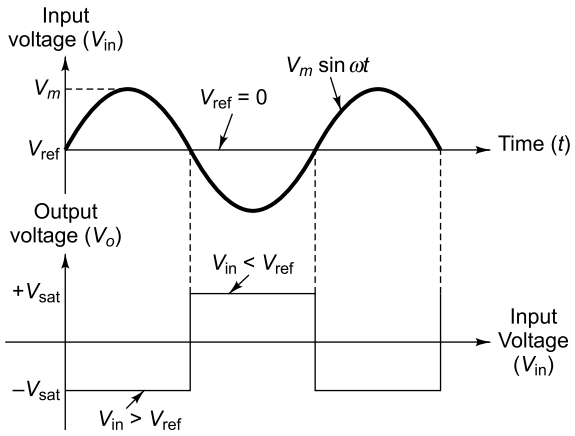


Fig. 5.71 ***Input and output voltage waveforms of zero crossing detector circuit***

5.19 SCHMITT TRIGGER

In an analog comparator circuit, the applied input voltage is compared with a known reference voltage. When a noise voltage signal exists in the input voltage, the comparator output signal will be square wave with some unwanted signals. The comparator output

state changes either from $+V_{sat}$ to $-V_{sat}$ or from $-V_{sat}$ to $+V_{sat}$ when there is some millivolt change in the input voltage which is above the reference voltage or less than reference voltage. As noise signal is generated at random value, the output consists of a series of pulses of different width as shown in Fig. 5.72. This phenomena is called *chattering*. This problem can be removed by a Schmitt trigger circuit. The positive feedback of a Schmitt trigger circuit can also speed up the response time of the system.

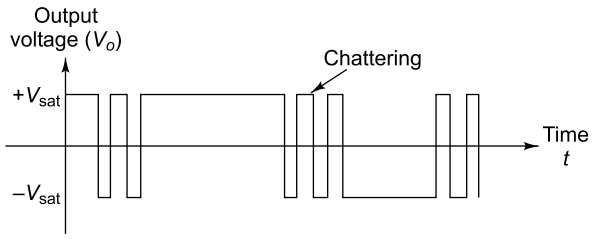


Fig. 5.72 ***Comparator output with chattering due to noise signal in input voltage***

Figure 5.73 shows a Schmitt trigger circuit. The input voltage is applied to the inverting (–) input terminal and feedback voltage is applied to the non-inverting (+) input terminal.

Assume the output voltage is $V_o = +V_{sat}$. Then the feedback voltage at non-inverting (+) input terminal will be

$$V_f = \frac{R_2}{R_1 + R_2} V_{sat} = V_{UT}$$

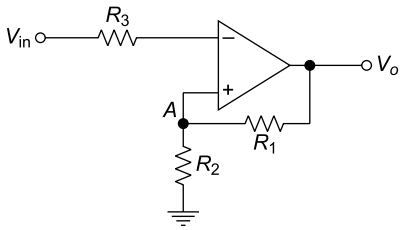


Fig. 5.73 ***Schmitt trigger circuit***

This voltage is also called the *upper threshold voltage*, V_{UT}. When the input voltage V_{in} is less than V_{UT} ($V_{in} < V_{UT}$), the output voltage V_o will be constant at $+V_{sat}$. If the input voltage V_{in} is just greater than V_{UT} ($V_{in} > V_{UT}$), the output voltage V_o of operational amplifier switches from $+V_{sat}$ to $-V_{sat}$ and this circuit behaves as regenerative comparator. When $V_{in} > V_{UT}$, the output voltage V_o will be constant at $-V_{sat}$ as shown in Fig. 5.74.

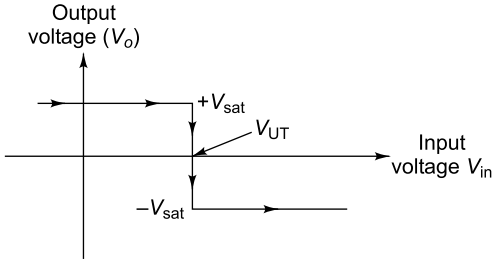


Fig. 5.74 ***Characteristics of Schmitt trigger for V_{in} increasing***

Then the feedback voltage is

$$-\frac{R_2}{R_1 + R_2} V_{sat} = V_{LT}$$

This voltage is known as *lower threshold voltage*, V_{LT}. The output voltage V_o will be $-V_{sat}$ when $V_{in} > V_{LT}$. While the input voltage V_{in} is just less than V_{LT} ($V_{in} < V_{LT}$), the output voltage V_o of operational amplifier switches from $-V_{sat}$ to $+V_{sat}$ as shown in Fig. 5.75. Then output voltage V_o will be constant at $+V_{sat}$ till $V_{in}<V_{LT.}$ The complete characteristics of Schmitt trigger is depicted in Fig. 5.75.

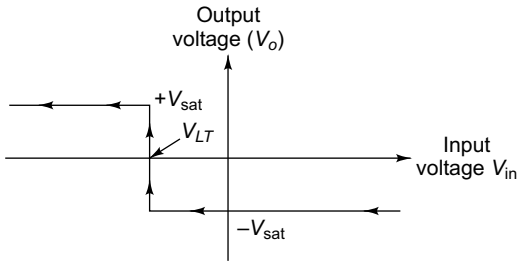


Fig. 5.75 ***Characteristics of Schmitt trigger for V_{in} decreasing***

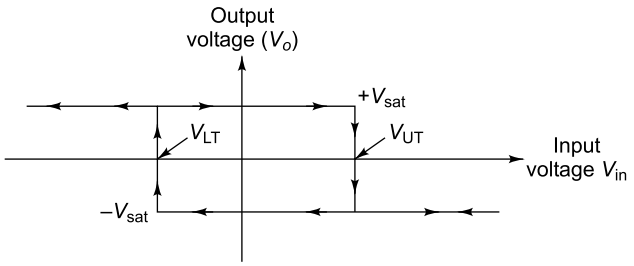


Fig. 5.76 ***Complete characteristics of Schmitt trigger***

In this circuit, the upper threshold voltage, V_{UT} must be greater than the lower threshold voltage, V_{LT}. The difference between V_{UT} and V_{LT} voltages is called hysteresis width V_H and it can be expressed as

$$V_H = V_{UT} - V_{LT} = 2\frac{R_2}{R_1 + R_2}V_{sat}$$

will be constant at $+V_{sat}$. If the input voltage V_{in} is just greater than V_{UT} ($V_{in} > V_{UT}$), the output voltage V_o of operational amplifier switches from $+V_{sat}$ to $-V_{sat}$ and this circuit behaves as regenerative comparator. When $V_{in} > V_{UT}$, the output voltage V_o will be constant at $-V_{sat}$.

Figure 5.77 shows a practical Schmitt trigger circuit. When two back-to-back zener diodes are connected at the output of OP-AMP, the output voltage will be independent of supply voltage ($+V_{sat}$ or $-V_{sat}$). The R is connected in series with zener diodes to limit the current flows through zener diodes. The limiting output voltage will be $(V_{Z1} + V_D)$ and $-(V_{Z2} + V_D)$ where V_D is the forward voltage drop of diode and V_Z is the voltage across zener diode.

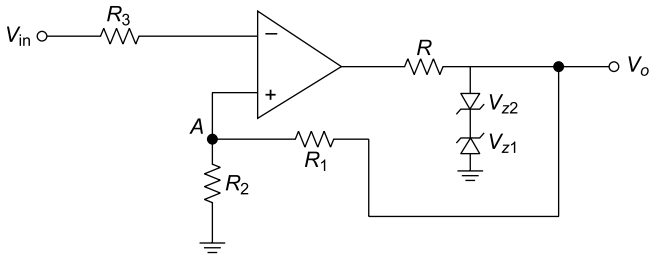


Fig. 5.77 ***Practical schmitt trigger circuit***

5.27 In a Schmitt trigger circuit as shown in Fig. 5.73, $R_1 = 10\ \text{k}\Omega$, $R_2 = 5\ \text{k}\Omega$, $V_{\text{in}} = 10 \sin \omega t$ and saturation voltage ±15 V.

(a) Determine the threshold voltage V_{UT} and V_{LT}. Calculate hysteresis width V_H

(b) Find the output voltage waveform.

Solution (a) The upper threshold voltage, V_{UT} is

$$V_{UT} = \frac{R_2}{R_1 + R_2} V_{\text{sat}} = \frac{5}{10+5} \times 15\ \text{V} = 5\ \text{V}$$

The lower threshold voltage, V_{LT} is

$$V_{UT} = -\frac{R_2}{R_1 + R_2} V_{\text{sat}} = -\frac{5}{10+5} \times 15\ \text{V} = -5\ \text{V}$$

The hysteresis width V_H is

$$V_H = V_{UT} - V_{LT} = 5 - (-5)\ \text{V} = 10\ \text{V}$$

(b) The output voltage waveform is shown in Fig. 5.78.

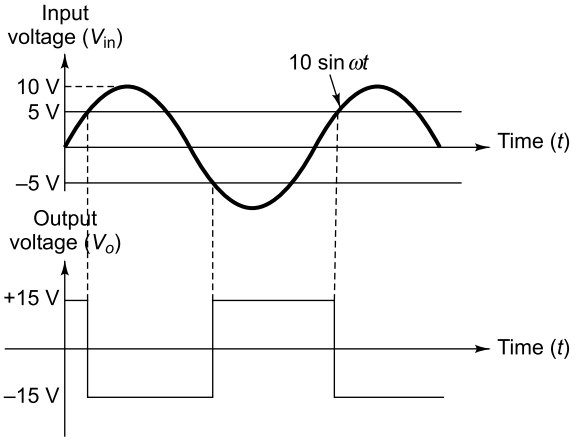


Fig. 5.78 ***Input and output voltage waveforms of schmitt trigger circuit***

5.28 Figure 5.79 shows a Schmitt trigger circuit where $R_1 = 50\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $V_{\text{ref}} = +5$ V, saturation voltage ±14 V, and $V_{\text{in}} = 12 \sin \omega t$.

(a) Find the threshold voltages V_{UT} and V_{LT} and determine hysteresis width V_H

(b) Show the output voltage waveform.

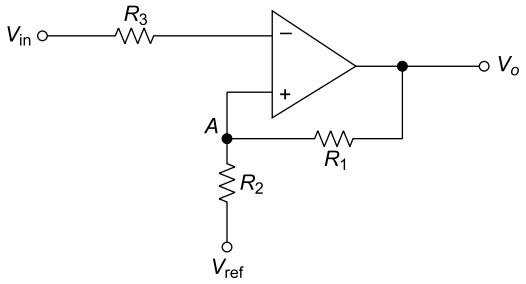


Fig. 5.79 ***Schmitt trigger circuit***

Solution (a) The upper threshold voltage, V_{UT} is

$$V_{UT} = V_{ref} + \frac{R_2}{R_1 + R_2}(V_{sat} - V_{ref}) = 5 + \frac{10}{50 + 10} \times (14 - 5)\ \text{V} = 6.5\ \text{V}$$

The lower threshold voltage, V_{LT} is

$$V_{LT} = V_{ref} - \frac{R_2}{R_1 + R_2}(V_{sat} + V_{ref}) = 5 - \frac{10}{50 + 10} \times (14 + 5)\ \text{V} = 1.83\ \text{V}$$

The hysteresis width V_H is

$$V_H = V_{UT} - V_{LT} = 6.5 - 1.83\ \text{V} = 4.67\ \text{V}$$

(b) The output voltage waveform is shown in Fig. 5.80.

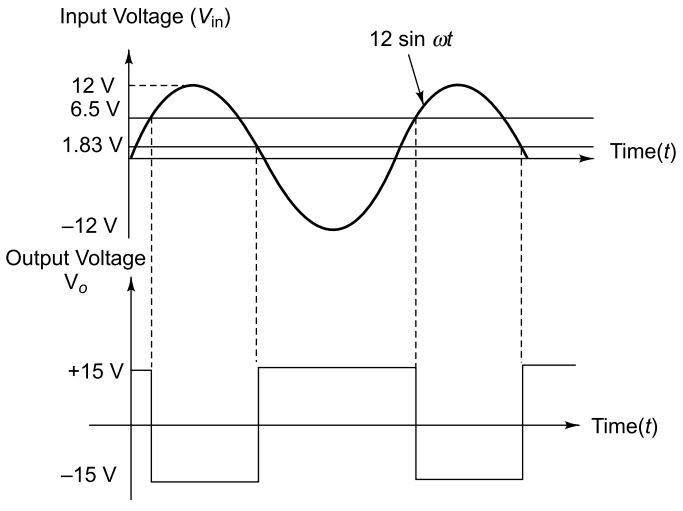


Fig. 5.80 ***Input and output voltage waveforms of Schmitt trigger circuit***

5.20 REALIZATION OF FUNCTIONS USING OP-AMP

In conjunction with an operational amplifier's use in the integrator circuit as depicted in Fig. 5.31, the op-amp can be also used in the realization of other first-order transfer functions, which are useful in filter design. The examples of first-order functions are low-pass filters, high-pass filters and all-pass filters. Though the low-pass and high-pass functions can be realized using RC circuits only, the application of the op-amp in the circuit provides it with gain and isolation from the circuit that follows it. The realization of low-pass, high-pass and all-pass circuits are explained in this section.

5.20.1 Low-pass Circuits

Figure 5.81 shows a first-order low-pass circuit and its transfer voltage ratio is equal to

$$F(s) = \frac{V_o}{V_i} = -\frac{\dfrac{1}{CR_1}}{s + \dfrac{1}{CR_2}}$$

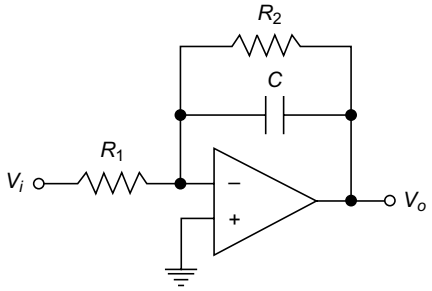


Fig. 5.81 *First-order low-pass circuit*

The circuit can be realized by the transfer function

$$F(s) = \frac{a}{s+b} \text{ where, } a = -\frac{1}{CR_1} \text{ and } b = \frac{1}{CR_2}$$

The dc gain is equal to $\dfrac{a}{b} = -\dfrac{R_2}{R_1}$

The alternative circuit of Fig. 5.81 without phase inversion is depicted in Fig. 5.82.

The transfer function of Fig. 5.82 is

$$F(s) = \frac{V_o}{V_i} = -\frac{\dfrac{K}{CR}}{s + \dfrac{1}{CR}} \text{ where, } K = 1 + \frac{R_2}{R_1}$$

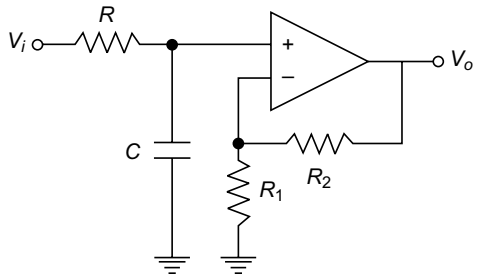


Fig. 5.82 ***First-order low-pass circuit***

The circuit can be realized by the transfer function

$$F(s) = \frac{a}{s+b} \text{ where, } a = \frac{K}{CR} \text{ and } b = \frac{1}{CR}$$

The dc gain is equal to $\frac{a}{b} = K$.

5.20.2 High-pass Circuits

Figure 5.83 shows a first-order high-pass circuit and its transfer voltage ratio is equal to

$$F(s) = \frac{V_o}{V_i} = -\frac{R_2}{R_1}\frac{s}{s+\frac{1}{CR_1}}$$

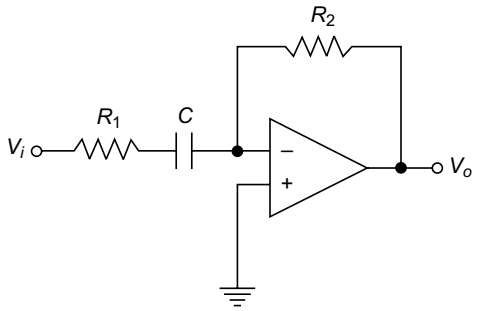


Fig. 5.83 ***First-order high-pass circuit***

The circuit can be realized by the transfer function

$$F(s) = \frac{as}{s+b} \text{ where, } a = -\frac{R_2}{R_1} \text{ and } b = \frac{1}{CR_1}$$

The alternative circuit of Fig. 5.83 without phase inversion is depicted in Fig. 5.84. The transfer function of Fig. 5.84 is

$$F(s) = \frac{V_o}{V_i} = -\frac{Ks}{s + \frac{1}{CR}} \text{ where, } K = 1 + \frac{R_b}{R_a}$$

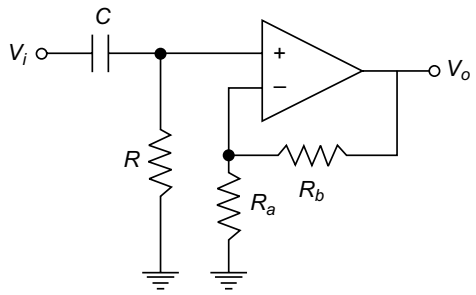


Fig. 5.84 *First-order low-pass circuit*

The circuit can be realized by the transfer function

$$F(s) = \frac{as}{s + b} \text{ where, } a = K = 1 + \frac{R_b}{R_a} \text{ and } b = \frac{1}{CR}$$

5.20.3 High-pass Circuits

Figure 5.85 shows a first-order high-pass circuit and its transfer voltage ratio is equal to

$$F(s) = \frac{V_o}{V_i} = -\frac{s - \frac{1}{CR}}{s + \frac{1}{CR}} = \frac{s - a}{s + a} \text{ where, } a = \frac{1}{CR}$$

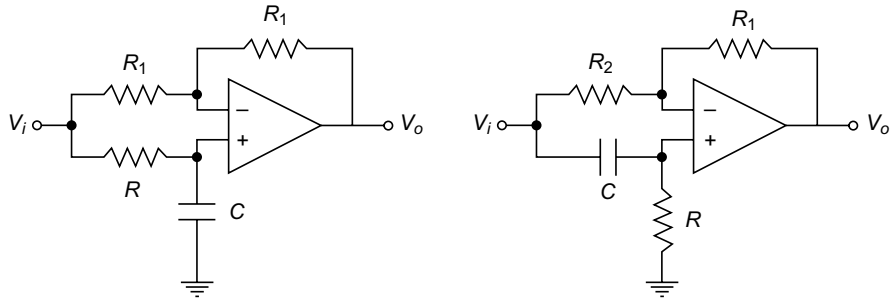


Fig. 5.85 *First-order high-pass circuit*

EXERCISES

Short- and Long-Answer-Type Questions

1. What do you mean by linear circuit? Give a list of linear applications of operational amplifiers.
2. What do you mean by nonlinear circuit? What is the difference between a linear circuit and nonlinear circuit? Write some nonlinear applications of operational amplifiers.
3. Draw the circuit diagram of an inverting amplifier. Derive the output voltage of inverting amplifier in terms of input voltage and resistances.
4. Define non-inverting amplifier. Write the difference between inverting amplifier and non-inverting amplifier.
5. Explain the voltage follower circuit. Justify the statement "voltage gain of the voltage follower circuit is unity".
6. Explain the following amplifier circuits:
   (a) Inverting summing amplifier
   (b) Non-inverting summing amplifier
   (c) Difference amplifier
   (d) Adder cum subtractor circuit
7. Draw the circuit diagram of a voltage-to-current converter and explain its operation.
8. Draw the circuit diagram of a current-to-voltage converter and explain its operation. What are the applications of current-to-voltage converters?
9. Define integrator. What are the types of integrators? Write some applications of integrators.
10. Discuss the following integrators:
    (a) Inverting integrator (b) Non-inverting integrator
    (c) Practical integrator (d) Summing integrator amplifier
11. Define differentiator. Write some applications of a differentiator.
12. Explain the following differentiators
    (a) Practical differentiator
    (b) Summing differentiator
13. Draw the circuit diagram of a logarithmic amplifier. Prove that the output voltage of logarithmic amplifier is $V_o = -\frac{KT}{q} \log \frac{V_1}{V_{\text{ref}}}$.
14. State the disadvantages of logarithmic amplifier. Explain how the temperature compensated logarithmetic amplifier can reduce the disadvantages of logarithmic amplifier .
15. Discuss antilog amplifier circuit using OP-AMP and transistor. Prove that the output voltage of antilog amplifier is $V_o = -I_o R_f \log^{-1}\left(\frac{V_{\text{in}}}{\tau V_T}\right)$
16. Define analog multiplier. Draw a circuit to generate the output voltage $V_o = -I_o R_f \frac{V_1 V_2}{V_{\text{ref}}^2}$, where input voltages are V_1 and V_2.

17. Give a list for applications of multipliers. Discuss the analog divider circuit. Prove that the output voltage of analog divider is $V_o \propto \left(\frac{V_2}{V_1}\right)$ where input voltages are V_1 and V_2.
18. Explain non-inverting comparators and inverting comparators. Write some disadvantages of comparator circuits.
19. What is the effect of noise in comparator circuits? Give a list for applications of comparator circuits.
20. Draw a practical Schmitt trigger circuit and explain its operation with waveforms. What is the difference between comparator and Schmitt trigger?
21. Figure 5.86 shows the non-inverting amplifier, where $R_1 = 10\ \text{k}\Omega, R_L = R_f = 100\ \text{k}\Omega$ and $V_1 = 5$ V. Calculate (a) V_o, (b) gain (c) I_1, (d) load current $I_{L,}$ and (e) output current I_o.

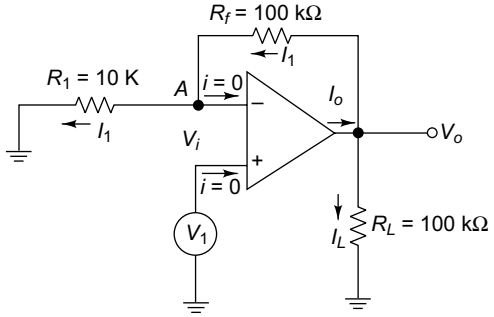


Fig. 5.86

22. Figure 5.87 shows an adder circuit with $V_1 = 2$ V, $V_2 = -5$ V and $V_3 = 4$ V. Determine the output voltage V_o. Assume $R_1 = 20\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega, R_3 = 20\ \text{k}\Omega$ and $R_f = 10\ \text{k}\Omega$.

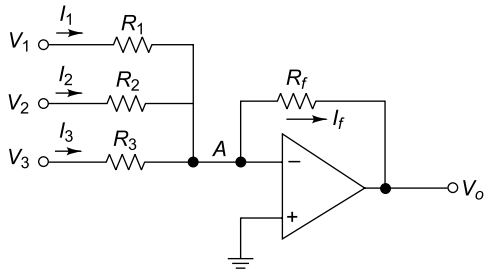


Fig. 5.87

23. Implement the equation $V_o = -(6V_1 + 2V_2)$ using an operational amplifier circuit. Assume minimum value of resistance is 4.7 kΩ.
24. An operational amplifier circuit is shown in Fig. 5.88. Determine the output voltage V_o and current flows through R_1, R_2, R_3 and R_f. Assume $V_1 = 3$ V, $V_2 = -5$ and $V_3 = 2$ V

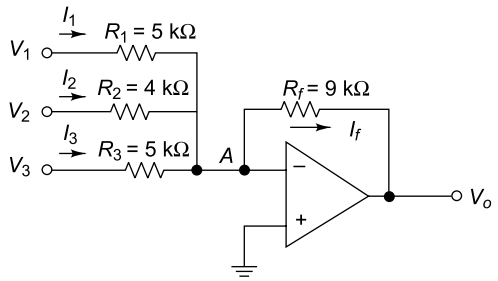


Fig. 5.88

25. Calculate the output voltage and common mode rejection ratio (CMRR) of the differential amplifier as shown in Fig. 5.89 Assume $V_1 = 3$ V and $V_2 = 2$.

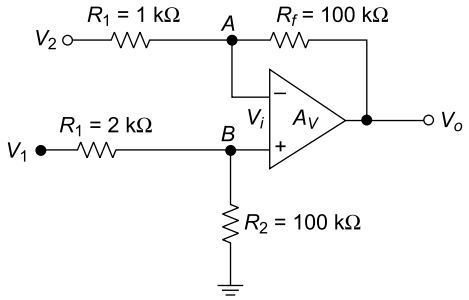


Fig. 5.89

26. Figure 5.90 shows an operational amplifier circuit. Determine the output voltage V_o.
Assume $V_1 = 3$ V, $V_2 = -5$, $V_3 = 2$ V and $V_3 = -2$ V

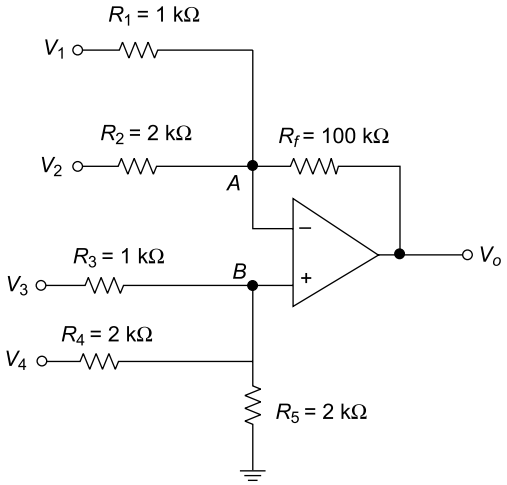


Fig. 5.90

27. In an integrator circuit, the value of RC is 1.5 second. Find out the output voltage at $t = 2$ seconds, $t = 4$ seconds and $t = 6$ seconds when input voltage is 5V.
28. Figure 5.91 shows an integrator circuit. Find out the output voltage when input voltage is 5 sin 100 πt and show the output voltage waveform.

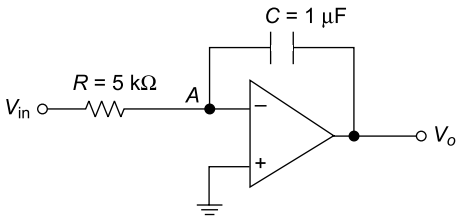


Fig. 5.91

29. When a square wave as shown in Fig. 5.92 is applied as input voltage to an integrator circuit, find out the output voltage. Assume $RC = 1$ second.

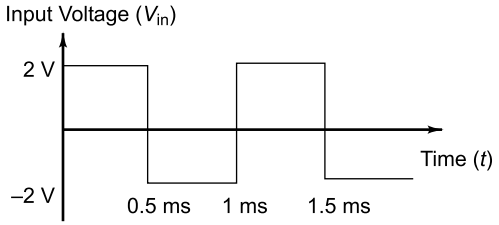


Fig. 5.92

30. Draw the output voltage waveform when input voltage of differentiation circuit is $V_{in} = 4$ sin 100 πt. Assume $CR = 0.01$ second.
31. When a square wave input voltage as shown in Fig. 5.93 is applied to the differentiation circuit, what will be the output voltage waveform?. Assume missing parameters.

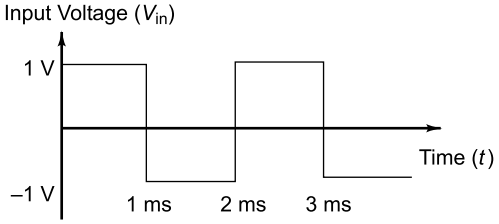


Fig. 5.93

32. Determine the output voltage V_o of a log amplifier using OP-AMP and transistor as shown in Fig. 5.94. Assume V_{in} = 500 mV, R = 10 kΩ, T = 290° K and $I_S = 10^{-13}$ A

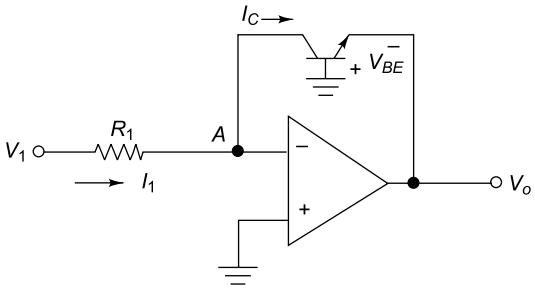


Fig. 5.94

33. Compute the output voltage V_o of an antilog amplifier using OP-AMP and transistor as shown in Fig. 5.95. Assume $V_{\text{in}} = 200$ mV, $R_f = 10$ K, $\tau = 1$, $V_T = 20$ mV and $I_o = 10^{-13}$A

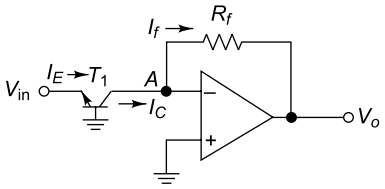


Fig. 5.95

34. Figure 5.96 shows a comparator circuit where $V_{Z1} = V_{Z2} = 10$ V, $V_D = 0.6$ V, $V_{\text{ref}} = +3$ V, saturation voltage ± 14 V, and $V_{\text{in}} = 2 \sin \omega t$.
Draw the output voltage waveform.

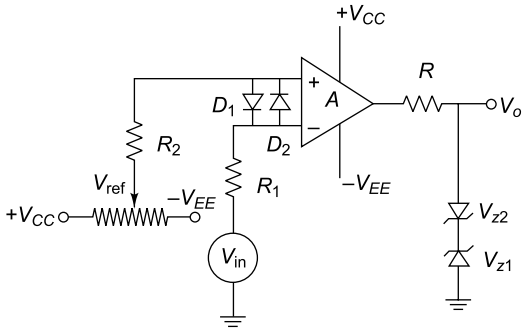


Fig. 5.96

35. A Schmitt trigger circuit is shown in Fig. 5.97 where $R_1 = 12$ kΩ, $R_2 = 6$ kΩ, $V_{\text{ref}} = +4$ V, saturation voltage ± 15 V, and $V_{\text{in}} = 10 \sin \omega t$.
    (a) Find the threshold voltages V_{UT} and V_{LT} and determine hysteresis width V_H.
    (b) Show the output voltage waveform.

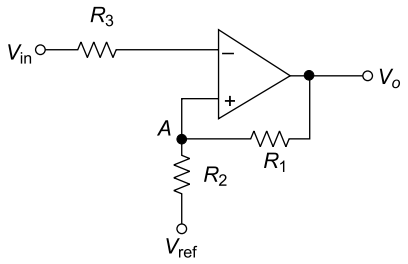


Fig. 5.97

36. In a Schmitt trigger circuit as shown in Fig. 5.98, R_1 = 10 kΩ, R_2 = 5 kΩ, V_{in} 5 sin ωt, and saturation voltage ±15 V. Assume V_{Z1} = V_{Z2} = 10 V, V_D=0.6 V
    (a) Determine the threshold voltage V_{UT} and V_{LT}. Calculate hysteresis width V_H.
    (b) Find the output voltage waveform.

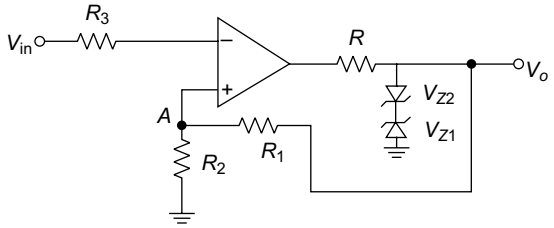


Fig. 5.98

MULTIPLE CHOICE QUESTIONS

1. The linear application of an operational amplifier is
    (a) adder circuit (b) log amplifier
    (c) antilog amplifier (d) Schmitt trigger
    Answer: (a) adder circuit
2. The non-linear application of operational amplifier is
    (a) adder circuit (b) comparator
    (c) subtractor circuit (d) voltage to current converter
    Answer: (b) comparator
3. The output voltage of an inverting amplifier is

    (a) $V_o = -\frac{R_1}{R_f} V_1$ (b) $V_o = \frac{R_f}{R_1} V_1$

    (c) $V_o = -\frac{R_f}{R_1} V_1$ (d) $V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$

    Answer: (c) $V_o = -\frac{R_f}{R_1} V_1$

4. The output voltage of a non-inverting amplifier is

   (a) $V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$ (b) $V_o = \frac{R_f}{R_1} V_1$

   (c) $V_o = \left(1 - \frac{R_f}{R_1}\right) V_1$ (d) $V_o = \left(1 + \frac{R_1}{R_f}\right) V_1$

   Answer: (a) $V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$

5. The output voltage of an OP-AMP circuit as shown in Fig. 5.99 is

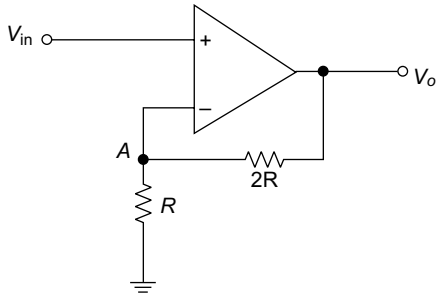


Fig. 5.99

   (a) $V_o = 3V_{\text{in}}$ (b) $V_o = 2V_{\text{in}}$ (c) $V_o = -3V_{\text{in}}$ (d) $V_o = -V_{\text{in}}$

   Answer: (a) $V_o = 3V_{\text{in}}$

6. When $R_1 = R_2 = R_f = R$, the output voltage of OP-AMP circuit as shown in Fig. 5.100 is

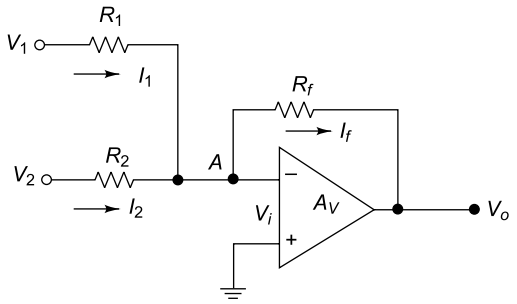


Fig. 5.100

   (a) $V_o = -(V_1 + V_2)$
   (b) $V_o = (V_1 + V_2)$
   (c) $V_o = -(V_1 - V_2)$
   (d) $V_o = (V_1 - V_2)$

   Answer: (a) $V_o = -(V_1 + V_2)$

7. Figure 5.101 shows an OP-AMP circuit. The output voltage of OP-AMP is

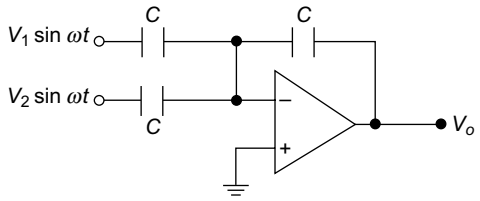


Fig. 5.101

(a) $V_o = (V_1 - V_2) \sin \omega t$ (b) $V_o = -(V_1 - V_2) \sin \omega t$

(c) $V_o = -(V_1 + V_2) \sin \omega t$ (d) $V_o = (V_1 + V_2) \sin \omega t$

Answer: (c) $V_o = -(V_1 + V_2) \sin \omega t$

8. The output voltage of differentiator circuit using OP-AMP is

(a) $V_o(t) = -\dfrac{1}{R_1 C} \int_0^t V_{\text{in}}\, dt + V_0(0)$

(b) $V_o = -CR \dfrac{dV_{\text{in}}}{dt}$

(c) $V_o = CR \dfrac{dV_{\text{in}}}{dt}$

(d) $V_o(t) = \dfrac{1}{R_1 C} \int_0^t V_{\text{in}}\, dt + V_0(0)$

Answer: (b) $V_o = -CR \dfrac{dV_{\text{in}}}{dt}$

9. The Schmitt trigger circuit has a
   (a) positive feedback
   (b) negative feedback
   (c) negative and positive feedback
   (d) none of these

   Answer: (a) positive feedback

10. The feedback element in a differentiator is
    (a) a capacitor (b) an inductor (c) a diode (d) a resistance

    Answer: (d) a resistance

11. The feedback element in a integrator is
    (a) a capacitor (b) an inductor
    (c) a diode (d) a resistance

    Answer: (a) a capacitor

12. The inverting amplifiers can be used as
    (a) voltage followers (b) sample and hold circuits
    (c) buffers (d) summing amplifiers

    Answer: (d) summing amplifiers

13. When one of the input terminals of a comparator is connected with ground, it becomes inverting amplifiers can be used as
    (a) zero crossing detectors (b) sample and hold circuits
    (c) buffers (d) summing amplifiers
    Answer: (a) zero crossing detectors
14. The log and antilog amplifiers can be used for
    (a) signal compression (b) multiplier
    (c) divider (d) summing amplifiers
    Answer: (a) signal compression, (b) multiplier, (c) divider
15. The output voltage of an integrator circuit is

    (a) $V_o^{(t)} = -\frac{1}{RC}\int_o^t V_{in}\, dt + V_o^{(o)}$ (b) $V_o^{(t)} = -CR\frac{dV_{in}}{dt}$

    (c) $V_o^{(t)} = CR\frac{dV_{in}}{dt}$ (d) $V_o^{(t)} = \frac{1}{RC}\int_o^t V_{in}\, dt$

    Answer: (a) $V_o^{(t)} = -\frac{1}{RC}\int_o^t V_{in}\, dt + V_o^{(o)}$

UNIVERSITY QUESTIONS WITH ANSWERS

Multiple-Choice-Type Questions

1. OPAMP comparator circuit uses
   (a) positive feedback (b) negative feedback
   (c) regenerative feedback (d) no feedback [WBUT-009]
   Solution (d) no feedback

Short- and Long-Answer-Type Questions

1. Find the output voltage V_o of the three input summing amplifier circuit of the following Fig. 5.102. [WBUT-2003]

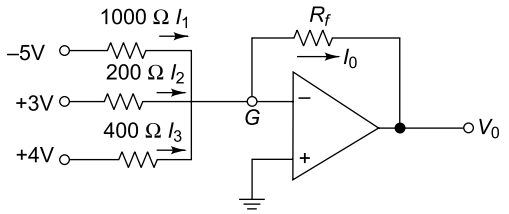


Fig. 5.102

Solution

Figure 5.102 shows the 3-input summing amplifier. The input resistances are $R_1 = 1000\ \Omega, R_2 = 200\ \Omega$ and $R_3 = 400\ \Omega$. The corresponding input voltages are $V_1 = -5$ V, $V_2 = +3$ V and $V_3 = +4$ V. The feedback resistance is R_f and output voltage is V_o.

Applying the KCL at G, we get

$$I_1 + I_2 + I_3 = I_0$$

or $$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_o}{R_f}$$

The output voltage $V_o = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) \times R_f$

$$= -\left(\frac{-5}{1000} + \frac{3}{200} + \frac{4}{400}\right) \times R_f = 0.02\ R_f$$

2. Describe the use of an OP-AMP as an integrator. [WBUT-2004]
Solution Refer Section 5.11.1.
3. Draw the circuit diagram to use an OPAMP as a voltage follower? [WBUT-2005]

Solution

Figure 5.103 shows the voltage follower circuit using OP-AMP. When R_1 and R_f are removed form an non-inverting amplifier, the circuit works as a voltage follower. The input voltage is applied at the non-inverting input of an OP-AMP and the inverting input is connected to the output terminal of OP-AMP. Due to direct connection between the inverting input and output terminals, a 100% voltage series feedback is applied.

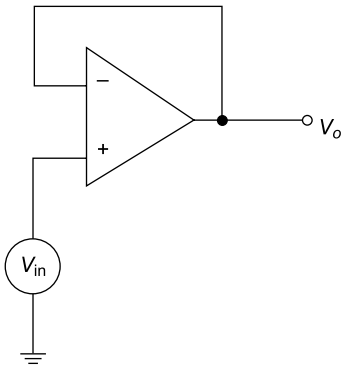


Fig. 5.103 ***Voltage follower***

The output voltage gain of a voltage follower is

$$A_V = 1 + \frac{R_f}{R_1} = 1 \quad \text{as} \quad R_f = 0$$

The common mode rejection ratio(CMRR) of a voltage follower is

$$\text{CMRR} = \frac{A_{CL}}{A_{CM}}$$

As the closed-loop gain $A_{CL} = 1$, the common mode rejection ratio is expressed as

$$\text{CMRR} = \frac{1}{A_{CM}}$$

The voltage follower has very high input impedance and very low output impedance. The application of a voltage follower is buffer amplifier.

4. A balanced differential amplifier using a single OP-AMP has a voltage gain of 10. The resistances connected to the input are R_1 each. Determine the value of other resistances. Derive the formula you may use. [WBUT-2006]

Solution

Figure 5.104 shows a balanced differential amplifier using a single operational amplifier. Assume the differential voltage between inverting (–) and non-inverting (+) terminals of operational amplifier is zero. Potential at *A* and potential at *B* are same potential, so that $V_A = V_B$.

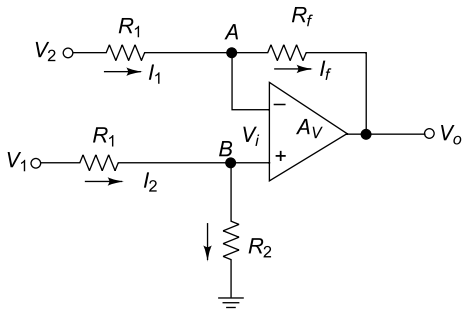


Fig. 5.104

The nodal equation at node *B* is

$$\frac{V_1 - V_B}{R_1} = \frac{V_B - 0}{R_2}$$

or, $$\frac{V_1}{R_1} = \frac{V_B}{R_1} + \frac{V_B}{R_2} = V_B\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = V_B \frac{R_1 + R_2}{R_1 R_2}$$

or, $$V_B = V_1 \frac{R_2}{R_1 + R_2}$$

or, $$V_A = V_1 \frac{R_2}{R_1 + R_2} \quad \text{as} \quad V_A = V_B$$

Applying KCL at node *A* we can write

$$I_1 = I_f$$

or, $$\frac{V_2 - V_A}{R_1} = \frac{V_A - V_o}{R_f}$$

or, $$\frac{R_f}{R_1} V_2 - \frac{R_f}{R_1} V_A - V_A = -V_o$$

or, $$V_o = \left(1 + \frac{R_f}{R_1}\right) V_A - \frac{R_f}{R_1} V_2$$

$$= \left(1 + \frac{R_f}{R_1}\right) \frac{R_2}{R_1 + R_2} V_1 - \frac{R_f}{R_1} V_2$$

If $R_f = R_2$, the output voltage $V_o = \frac{R_2}{R_1} V_1 - \frac{R_2}{R_1} V_2 = \frac{R_2}{R_1}(V_1 - V_2)$

The gain of differential amplifier is $\frac{R_2}{R_1}$ which is equal to 10.

Then $R_2 = 10.R_1$ and the $R_f = R_2 = 10.R_1$

5. (a) Draw the circuit diagram of an integrator using OP-AMP. Determine the expression for the output voltage in terms of input voltage.
   (b) If the input voltage is a square wave with magnitudes +2 V and –2 V with equal time interval, sketch the output waveform. [WBUT-2006]

Solution

(a) Refer Section 5.11.1.

(b) Figure 5.105 shows the integrator circuit with the square wave input voltage whose magnitudes varies in between +2 V and –2 V with equal time interval.

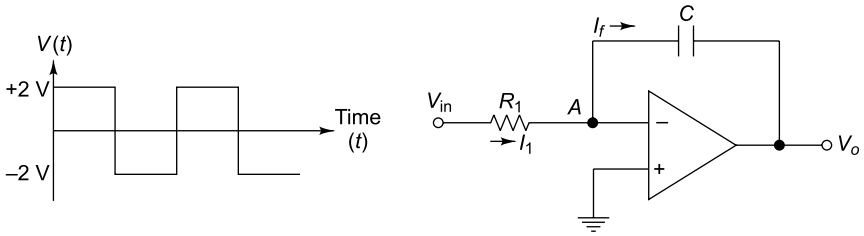


Fig. 5.105

The output voltage can be expressed as $V_o(t) = -\frac{1}{R_1 C} \int_0^t V_{in}\, dt + V_o(0)$

Assume $A_o(0) \neq 0$ and it has some initial value.

The output voltage waveform will be a triangular waveform as shown in the figure.

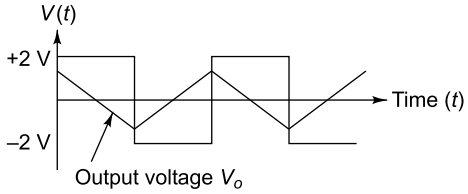


Fig. 5.106

6. Draw the circuit of a summing amplifier using inverting operational amplifier configuration. Establish the equation for the output voltage for this circuit. [WBUT-2007]

   Solution Refer Section 5.5.1.

7. Sketch the circuit of summer using OP-AMP to get
   $V_o = -V_1 + 2V_2 - 3V_3$ [WBUT-2008], [WBUT 2009]

   Solution

   Figure 5.107 shows the summer circuit using OP-AMP.

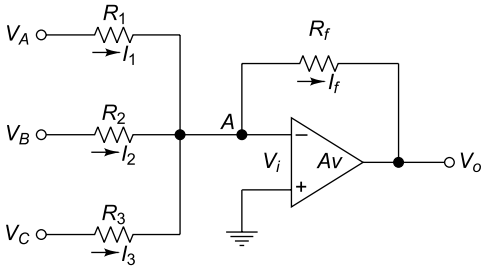


Fig. 5.107

The output voltage of summer circuit is

$$V_o = -\left(\frac{R_f}{R_1}V_A + \frac{R_f}{R_2}V_B + \frac{R_f}{R_3}V_C\right)$$

$$= -\frac{R_f}{R_1}V_A - \frac{R_f}{R_2}V_B - \frac{R_f}{R_3}V_C$$

$$= -V_1 + 2V_2 - 3V_3$$

To get $V_o = -V_1 + 2V_2 - 3V_3$,

$$\frac{R_f}{R_1} = 1, V_A = V_1, \frac{R_f}{R_2} = 2, V_B = -V_2, \frac{R_f}{R_3} = 3, \quad \text{and} \quad V_C = V_3$$

8. With the help of proper diagrams, explain the operation of an OP-AMP used as (i) adder, and (ii) integrator. [WBUT-2008]

   Solution

   (i) Refer Section 5.5.1. (ii) Refer Section 5.11.

9. Draw the circuit diagram and derive the expression for voltage gain of a non-inverting amplifier using OP-AMP. [WBUT-2008]

   Solution Refer Section 5.3.

10. Explain the working of an integrator circuit using ideal OP-AMP. [WBUT-2010]

    Solution Refer Section 5.11.

6 NUMBER SYSTEM, BOOLEAN ALGEBRA AND LOGIC CIRCUITS

6.1 INTRODUCTION

In digital systems, signals are represented in the binary form. As a binary quantity can be represented by two operating states called '0' and '1', it may be transmitted in the form of electronic OFF and ON pulses respectively. ON means binary '1' and OFF means binary '0'. When these pulses are received by any digital system, they are processed. The typical representation of voltage is shown in Fig. 6.1. Binary '1' means any voltage between 2 V to 5 V and binary '0' states any voltage between 0 V to 0.8 V. It will be noted that voltage between 0.8 V to 2 V is not used and this may create error in a digital circuit.

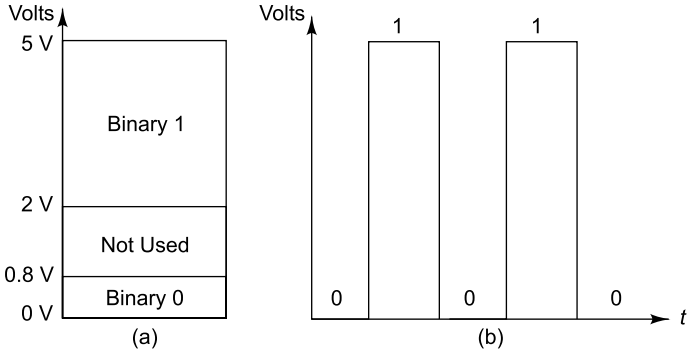


Fig. 6.1 *(a) Voltage representation of binary '1' and binary '0' (b) A digital signal*

In a digital system, all communication within the system is carried out in a digital manner. Usually, the digital communication means that all signals within the system can have only two possible states of OFF and ON or '0' and '1'. Digital electronics is a branch of electronics, and these electronic systems are composed of elements that exhibit this digital behaviour. As a digital system can only exhibit one of two possible states, they are usually easier to understand than analog systems, which can have an infinite number of states. The field of digital

electronics is very exciting, and fast changing. Advances in digital electronics make it possible to construct very complex systems in a simple manner. Digital electronics are a key element of many products, namely, personal computers, sophisticated sewing machines, microwave ovens, compact disc players, video cassette players, etc. The brains of all of these products and many parts of these products are composed of digital electronics. Presently, it is very difficult to survive in this world without digital electronics.

6.2 NUMBER SYSTEMS

In general, numbers are represented using '10' symbols or figures. These '10' symbols or figures are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9. The significance of each figure depends on its position inside the string of figures used to represent the number. These are numbers represented in "base 10". In digital system, there are many number systems but most commonly used number systems are the decimal, binary, octal, and hexadecimal systems. The decimal system is the most familiar number system that we commonly use in everyday life.

6.2.1 Decimal Number System

The decimal number system is composed of '10' symbols. These '10' symbols are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9. By using these symbols, we can write any quantity. The decimal system is also called the base '10' system as it has '10' digits. The representation of a decimal number is shown in Table 6.1.

Table 6.1 *Representation of a decimal number*

10^2	10^1	10^0		10^{-1}	10^{-2}	10^{-3}
=100	=10	=1	.	=0.1	=0.01	=0.001
Most			Decimal			**L**east
Significant			point			**S**ignificant
Digit						**D**igit (LSD)

The examples of decimal numbers can be 456 and 95.26. The decimal number $(456)_{10}$ can be written as

$(456)_{10} = 4 \times 10^2 + 5 \times 10^1 + 6 \times 10^\circ$ and the number $(95.26)_{10}$ can be represented as

$(95.26)_{10} = 9 \times 10^1 + 5 \times 10^\circ + 2 \times 10^{-1} + 6 \times 10^{-2}$

Any positive integer can be represented by symbols or digits in a positional number system. The number N can be represented in the equation form

$$N = d_n\, d_{n-1}\, d_{n-2} \ldots\ldots\ldots d_3\, d_2\, d_1\, d_0 \,.\, d_{-1}\, d_{-2}\, d_{-3} \ldots d_{n-1}\, d_n \qquad (6.1)$$

↑

Decimal Point

The d_i represents the digits, which have ten values ranging from 0 to 9. The value of 'n' may be any real integer to express the number N. The digit on the extreme right is called the Least Significant Digit (LSD) because it has the lowest positional value of 1 for integers. The next digit to the left of this least significant digit has the positional value of 10; the next, positional value is 100;

and so on. The digit on the extreme left is called the Most Significant Digit (MSD) as it has the highest positional value. The use of positional numbers can be extended to fractions by adding a decimal point and letting digits to the right of the decimal represent $\frac{1}{10}$ ths, $\frac{1}{100}$ ths, and so on, depending on position. The number N can be determined from Eq. (6.2).

$$N = d_n \times 10^n + d_{n-1} \times 10^{n-1} + \cdots + d_1 \times 10^1 + d_0 \times 10^\circ + d_{-1} \times 10^{-1} + d_{-2} \times 10^{-2} \cdots \quad (6.2)$$

6.2.2 General Positional Numbers

In general, we use 'base 10' in decimal system to represent a number, but a number system can have any base. The base of a number system is also called the *radix*. The rules concerning the decimal number representation in base 10 can be extended to 2 (binary), 8 (octal), and 16 (hexadecimal) based number system. The generalized representation of a positional number to any base b is given by Eq. (6.3) and (6.4).

$$N = d_n\, d_{n-1}\, d_{n-2} \cdots d_3\, d_2\, d_1\, d_0 \,.\, d_{-1}\, d_{-2}\, d_{-3} \cdots d_{-n-1}\, d_{-n} \cdots \quad (6.3)$$

↑

Radix Point

Equation (6.3) means

$$N = d_n \times b^n + \bullet\bullet + d_o \times b^\circ + d_{-1} \times b^{-1} + d_{-2} \times b^{-2} \cdots + d_{-n} \times b^{-n} \cdots \quad (6.4)$$

where,

d_i represents the digits,

b is the base or radix, and the "." represents the radix point.

The notation of generalized positional number system is N_b. Here, the subscript denotes the base.

6.2.3 Binary Number System

The simplest information is either TRUE or FALSE. This can be represented by two voltage levels: 5 volts for TRUE and 0 volts for FALSE or Switch is ON and switch is OFF as shown in Fig. 6.2.

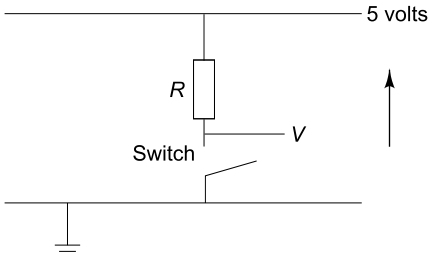


Fig. 6.2 ***Representation of binary by Switch ON and OFF***

A voltage signal, which has only two possibilities, is represented by a BIT. BIT stands for Binary Digit. Binary means: only 2 possible values. The advantages of using binary representation are simplicity to implement in electronic hardware (switch) and good tolerance to noise. FALSE means '0' and TRUE means '1'. Electronic storage devices are used in two distinct different states: '0' and '1'. So, these electronic storage devices use a number system based on only two digits. In the binary number system, the digits are zero (0) and one (1) and the radix/base is two (2). The example of a binary number is

$$N = 1011_2 = (1011)_2$$

where, the subscript '2' denotes the base of binary number system.

By using the formula of the general position number system, the number N can be presented in terms of base 10 or decimal numbers.

$$N = 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$$
$$= 8 + 2 + 1 = (11)_{10}$$

It is very convenient to determine the equivalent decimal number if we represent the positional value of each of the digits existing in binary system. After that we add the positional values corresponding to nonzero digits '1'. The positional value of each digit is given below:

8 4 2 1

In the binary system, there are only two symbols or possible digit values, '0' and '1'. This base-2 system can be used to represent any quantity that can be represented in decimal. Table 6.2 shows the representation of a binary number.

Table 6.2 *Representation of binary number*

2^3	2^2	2^1	2^0		2^{-1}	2^{-2}	2^{-3}
=8	=4	=2	=1	.	=1/2	=1/4	=1/8
Most				Binary			**L**east
Significant				Point			**S**ignificant
Bit (MSB)							**B**it (LSB)

The three-bit binary number with different possibilities is represented by its decimal equivalent as shown in Table 6.3.

Table 6.3 *Three-bit binary numbers and it's decimal equivalent.*

$2^2 = 4$	$2^1 = 2$	$2^0 = 1$	*Decimal Equivalent*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

6.2.4 Binary-to-Decimal Conversion

Any binary number can be converted to its decimal equivalent simply by summing together the weights of the various positions in the binary number, which contain 1. The decimal equivalent of binary number $(101010)_2$ is $(42)_{10}$ as shown below:

$(10\ 1\ 0\ 1\ 0)_2$ (binary)

$1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 32 + 8 + 2 = 42_{10}$ (decimal)

It should be noticed that this method is to find the weights (i.e., powers of 2) for each bit position that contains a 1, and then to add them up.

6.2.5 Decimal-to-Binary Conversion

For decimal-to-binary conversion, there are two methods, namely, reverse of binary to decimal and repetitive division. In this section, repetitive division method is represented.

The repetitive division method is that the decimal number is repeatedly divided by 2. To convert a decimal number into its binary equivalent, divide the decimal number by 2 progressively and the reminders are noted. During presentation of binary equivalent value, the reminders are arranged in reverse order form. The flowchart for converting decimal number into binary by repeated division is shown in Fig. 6.3 and the binary equivalent values for 0-15 are given in Table 6.4. For example, to convert 21_{10} to binary is given below:

Repetitive Division

```
21/2    = 10+ remainder   1     1 (Least Significant Bit)
10/2    =  5  +  remainder  0     0
5/2     =  2  +  remainder  1     1
2/2     =  1  +  remainder  0     0
1/2     =  0  +  remainder  1     1 (Most Significant Bit)
Result  21₁₀ =                    1 0 1 0 1₂
```

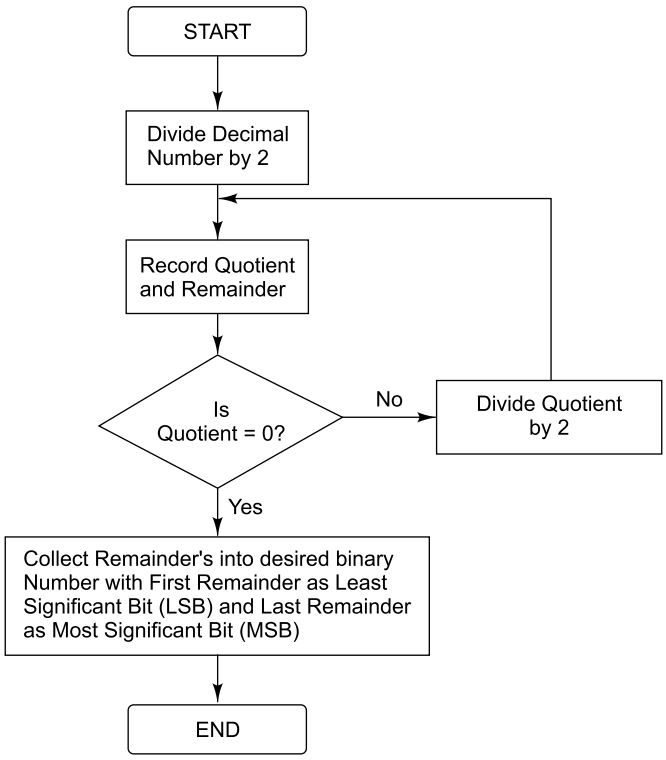


Fig. 6.3 *Flowchart for converting decimal number into binary by repeated division*

Table 6.4 *The binary equivalent values for 0–15*

Decimal			*Binary*				*Decimal*			*Binary*			
10^2	10^1	10^0	2^3	2^2	2^1	2^0	10^2	10^1	10^0	2^3	2^2	2^1	2^0
0	0	0	0	0	0	0	0	0	8	1	0	0	0
0	0	1	0	0	0	1	0	0	9	1	0	0	1
0	0	2	0	0	1	0	0	1	0	1	0	1	0
0	0	3	0	0	1	1	0	1	1	1	0	1	1
0	0	4	0	1	0	0	0	1	2	1	1	0	0
0	0	5	0	1	0	1	0	1	3	1	1	0	1
0	0	6	0	1	1	0	0	1	4	1	1	1	0
0	0	7	0	1	1	1	0	1	5	1	1	1	1

6.2.6 Conversion of Fractional Decimal Number into Binary

To convert a fractional decimal number to a binary number, we multiply the fractional part of the number repeatedly by base 2. The integer part obtained after multiplication is noting down separately and the fractional part is again considered for further multiplication. This process will continue till a zero fractional part has been obtained. In this conversion method, the first integer is the Most Significant Bit (MSB) and the last integer is the Least Significant Bit (LSB) of the fractional decimal number. The flowchart of conversion of fractional decimal number into binary is depicted in Fig. 6.4.

For example, the conversion of $(0.75)_{10}$ into binary is explained below:

To convert 0.75 decimal to binary, the computation uses repeated multiplication by 2. The integer part and fractional part of the product are separated after each multiplication.

Fraction Number	*Product*	*Fractional part*	*Integer Part*
.75	$.75 \times 2 = 1.5$	.5	1 MSB
.5	$.5 \times 2 = 1.0$	.0	1 LSB

The binary equivalent of $(.75)_{10}$ is $(.11)_2$. Similarly, the binary equivalent of .625 is given below:

Fraction Number	*Product*	*Fractional part*	*Integer Part*
.625	$.625 \times 2 = 1.25$	.25	1 MSB
.25	$.25 \times 2 = .5$	.5	0
.5	$.5 \times 2 = 1$	0	1 LSB

The binary equivalent of $(.625)_{10}$ is $(.101)_2$.

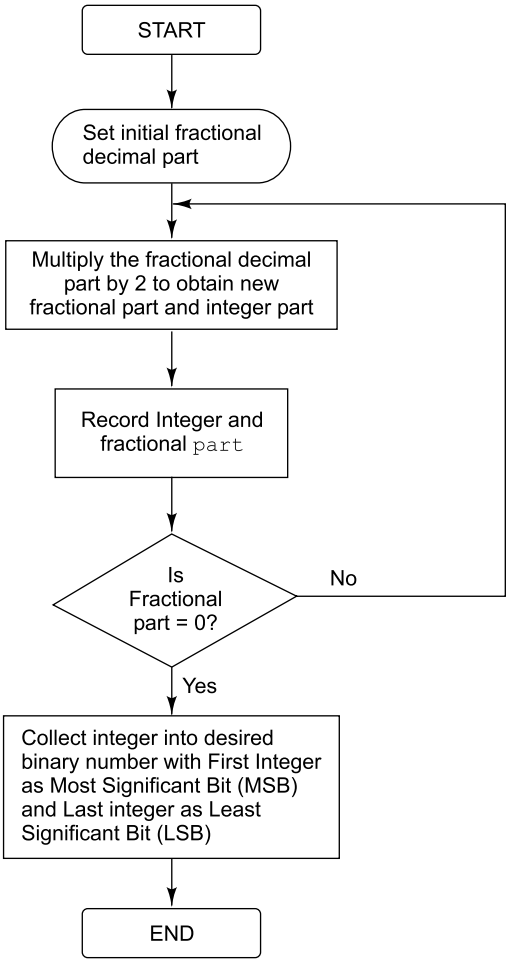


Fig. 6.4 *Flowchart for conversion of fractional decimal number into binary*

6.1 Convert the following decimal numbers to binary numbers:
(a) 15 (b) 215

Solution

(a) Conversion of $(11)_{10}$ to binary

```
15/ 2  = 7+ remainder of 1     1 (Least Significant Bit)
7/ 2   = 3 + remainder of 1    1
3 / 2  = 1 + remainder of 1    1
1 / 2  = 0 + remainder of 1    1(Most Significant Bit)
```

Result 15_{10} = **1** 1 1 **1**$_2$

(b) Conversion of $(215)_{10}$ to binary

```
215/ 2 = 107+ remainder of 1   1(Least Significant Bit)
107/ 2 = 53 + remainder of 1   1
53 / 2 = 26 + remainder of 1   1
26 / 2 = 13 + remainder of 0   0
```

```
13/2    = 6 + remainder of 1    1
6/2     = 3 + remainder of 0    0
3/2     = 1 + remainder of 1    1
1/2     = 0 + remainder of 1    1(Most Significant Bit)
Result 215₁₀ =                  1 1 0 1 0 1 1 1₂
```

6.2 Convert the following binary numbers to decimal numbers:
(a) 11011 (b) 10.11

Solution

(a) $(11011)_2 = 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$
$= 1 \times 16 + 1 \times 8 + 0 \times 4 + 1 \times 2 + 1 \times 1$
$= 16 + 8 + 0 + 2 + 1 = (27)_{10}$

(b) $(10.11)_2 = 1 \times 2^1 + 0 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2}$
$= 1 \times 2 + 0 \times 1 + 1 \times 0.5 + 1 \times 0.25$
$= 2 + 0.5 + 0.25 = (2.75)_{10}$

6.3 Convert the following decimal numbers to binary numbers:
(a) 0.85 (b) 12.25

Solution

(a) *Conversion of $(0.85)_{10}$ to binary*

Fraction Number	*Product*	*Fractional part*	*Integer Part*
0.85	.85 = 1.7	.7	1 MSB
.7	.7 × 2 = 1.4	.4	1
.4	.4 × 2 = 0.8	.8	0
.8	.8 × 2 = 1.6	.6	1
.6	.6 × 2 = 1.2	.2	1
.2	.2 × 2 = .4	.4	0 LSB

$(0.85)_{10}$ is equal to $(0.110110)_2$

(b) *Conversion of $(12.25)_{10}$ to binary*

```
12/ 2 = 6 + remainder 0    0(Least Significant Bit)
6 / 2 = 3 + remainder 0    0
3 / 2 = 1 + remainder 1    1
1 / 2 = 0 + remainder 1    1 (Most Significant Bit)
Result (12)₁₀ =            1 1 0 0₂
```

Fraction Number	*Product*	*Fractional part*	*Integer Part*
.25	.25 × 2 = .5	.5	0 MSB
.5	.5 × 2 = 1	0	1 LSB

$(12.25)_{10}$ is equal to $(1100.01)_2$

6.2.7 Octal Number

The octal number system has a base of eight, meaning that it has eight possible digits: 0, 1, 2, 3, 4, 5, 6, and 7. The octal number system is shown in Table 6.5.

Table 6.5 *Octal number system*

8^2	8^1	8^0		8^{-1}	8^{-2}	8^{-3}
= 64	=8	=1	.	=1/8	=1/64	=1/512
Most **S**ignificant **D**igit (MSD)			Octal Point			**L**east **S**ignificant **D**igit (LSD)

6.2.8 Decimal-to-Octal Conversion

Generally, decimal-to-octal conversion is done by using reverse octal to decimal and repetitive division method. Repetitive division method is explained in this section.

Repetitive Division This method uses repeated division by 8. In this method, in order to convert a decimal number to its octal equivalent, the decimal number is divided by 8 progressively and reminders are noted down. To obtain the octal equivalent value, the reminders are arranged in reverse order.

The example is converting 165_{10} to octal:

```
165/8    = 20+ remainder   5   5 (Least Significant Digit)
20/8     = 2 + remainder   4   4
2/8      = 0 + remainder   2   2 (Most Significant Digit)
Result   165₁₀ =               245₈
```

All of the remainders from the division are arranged in reverse order, from MSD to LSD to get the correct octal sequence. Therefore, the octal equivalent of decimal number $(165)_{10}$ is $(245)_8$

6.2.9 Binary-to-Octal/Octal-to-Binary Conversion

The binary equivalent of octal digits 0 to 7 are presented in Table 6.6.

Table 6.6 *Binary equivalent of octal digit*

Octal Digit	0	1	2	3	4	5	6	7
Binary Equivalent	000	001	010	011	100	101	110	111

It is clear from Table 6.6 that each octal digit is represented by three bits of binary digits. The example of binary-to-octal conversion is

$$(111\ 100\ 011)_2 = (111)\ (100)\ (011)_2 = (7\ 4\ 3\ )_{8.}$$

Similarly, the octal number $(453)_8$ can represented by the binary number $(100)\ (101)\ (011)_2 = (100101011)_2$

6.4 Convert the following decimal numbers to octal numbers:
(a) 294 (b) 20.6875

Solution

(a) *Conversion of $(234)_{10}$ to octal*

```
294/ 8  = 36+ remainder of  6  6 (Least Significant Bit)
36/8    = 4 + remainder of  4  4
4 / 8   = 0 + remainder of  4  4 (Most Significant Bit)
Result  294₁₀ =                4 4 6₈
```

(b) *Conversion of* $(20.6875)_{10}$ *to octal*

```
20/ 8   = 2 + remainder of 4   4 (Least Significant Bit)
4/8     = 0 + remainder of 4   4(Most Significant Bit)
Result 20₁₀ =                  44₈
```

Conversion of $(0.6875)_{10}$ *to octal*

Fraction Number	*Product*	*Fractional part*	*Integer Part*
0.6875	.6875 × 8 = 5.5	.5	5 MSB
.5	.5 × 8 = 4	.0	4 LSB

$(20.6875)_{10}$ is equal to $(44.54)_8$

6.5 Convert the following octal numbers to decimal numbers:
(a) 217 (b) 56.65

Solution

(a) $(217)_8 = 2 \times 8^2 + 1 \times 8^1 + 7 \times 8^0$
$= 2 \times 64 + 1 \times 8 + 7 \times 1$
$= 128 + 8 + 7 = 143$

(b) $(56.65)_8 = 5 \times 8^1 + 6 \times 8^0 + 6 \times 8^{-1} + 5 \times 8^{-2}$
$= 5 \times 8 + 6 \times 1 + 6 \times 0.125 + 5 \times 0.0156$
$= 40 + 6 + 0.125 + 0.0781 = 46.2031$

6.6 Convert the following octal numbers to binary numbers:
(a) 567.234 (b) 12347

Solution

(a) Conversion of $(567.234)_8$ to binary
$(567.234)_8 = 101\ 110\ 111\ .\ 010\ 011\ 100$

(b) Conversion of $(12347)_8$ to binary
$(12347)_8 = 001\ 010\ 011\ 100\ 111$

6.2.10 Hexadecimal Number

In the hexadecimal system, the base is 16. So, this system has 16 possible digit symbols. It uses the digits 0 through 9 and the letters A, B, C, D, E, and F as the 16 digit symbols. The letters A to F are used for the values of 10–15. This hexadecimal system is also used extensively in computing. The hexadecimal equivalent of decimal numbers 0 to 15 is presented in Table 6.7. Table 6.8 shows the hexadecimal number system.

Table 6.7 *Represent the decimal number into hexadecimal*

Decimal Base 10	*Hexadecimal Base 16*
0	0
1	1
2	2
3	3
4	4

(contd)

(contd)

5	5
6	6
7	7
8	8
9	9
10	A
11	B
12	C
13	D
14	E
15	F

Table 6.8 *Hexadecimal number system*

16^2 =256 **M**ost **S**ignificant **D**igit (MSD)	16^1 =16	16^0 =1	. Hexadecimal Point	16^{-1} =1/16	16^{-2} =1/256	16^{-3} =1/4096 **L**east **S**ignificant **D**igit (LSD)

6.2.11 Decimal to Hexadecimal Conversion

Decimal-to-hexadecimal conversion can be done by reverse hexadecimal to decimal and repetitive division methods. In this section, the repetitive division method is explained below.

Repetitive Division Method To convert decimal to hexadecimal, the decimal number is divided by 16 progressively and the reminders are noted down. To get the hexadecimal equivalent value, the reminders are arranged in reverse order. The example of converting 318_{10} to hexadecimal is given below:

```
318/16  = 19   + remainder 14   E (Least Significant Digit)
19/ 16  = 1    + remainder3     3
1 / 16  = 0    + remainder1     1 (Most Significant Digit)
Result  (318)10 =               (13E)16
```

All of the remainders from the division are arranged in reverse order, from MSD to LSD to form the correct hexadecimal sequence. Therefore, the hexadecimal equivalent of decimal number $(318)_{10}$ is $(13E)_{16}$.

6.2.12 Binary to Hexadecimal and Hexadecimal to Binary Conversion

Binary equivalents of hexadecimal digits (0 to F) are shown in Table 6.9. It is depicted in this table that each group of 4 binary digits (bits) is 1 hexadecimal digit. The example of binary to hexadecimal conversion is given below:

$$(1011\ 0011)_2 = (1011)\ (0011) = (B\ 3)_{16}.$$

The hexadecimal number $(46A)_{16}$ can be represented by the binary number $(0100)\ (0110)\ (1010)_2 = (0100\ 0110\ 1010)_2$.

Table 6.9 *Binary equivalent of hexadecimal digit*

Binary Equivalent	*Hexadecimal Digit*
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

6.7 Convert the following decimal numbers to hexadecimal numbers:
(a) 870 (b) 2536

Solution

(a) *Conversion of $(870)_{10}$ to hexadecimal*

```
870/16  = 54+ remainder of 6   6(Least Significant Bit)
54/ 16  = 3 + remainder of 6   6
3/16    = 0 + remainder of 3   3(Most Significant Bit)
```

Result 870_{10} = 366_{16}

(b) *Conversion of $(2536)_{10}$ to hexadecimal*

```
2536/16 = 158 + remainder of 8  8 (Least Significant Bit)
158/16  = 9   + remainder of 14 E
9/16    = 0   + remainder of 9  9(Most Significant Bit)
```

Result 2536_{10} = $9E8_{16}$

6.8 Convert the following hexadecimal numbers to decimal numbers:
(a) 3FC (b) DF8.28

Solution

(a) $(3FC)_{16} = 3 \times 16^2 + F \times 16^1 + C \times 16^0$
$= 3 \times 256 + 15 \times 16 + 12 \times 1$
$= 768 + 240 + 12 = 1020$

(b) $(DF8.28)_{16} = D \times 16^2 + F \times 16^1 + 8 \times 16^0 + 2 \times 16^{-1} + 8 \times 16^{-2}$
$= 13 \times 256 + 15 \times 16 + 8 \times 1 + 2 \times 0.0625 + 8 \times 0.0039$
$= 3328 + 240 + 8 + 0.125 + 0.0312 = 3576.1562$

6.9 Convert the decimal number 546 into octal and hexadecimal numbers.
Decimal number $(546)_{10}$ into octal

```
546/8   = 68+ remainder of 2   2 (Least Significant Digit)
68/8    = 8 + remainder of 4   4
8/8     = 1 + remainder of 0   0
```

```
1/8      = 0 + remainder of 1   1(Most Significant Digit)
Result   546(10) =              1 0 4 2(8)
```

Decimal number $(546)_{10}$ into hexadecimal

```
546/16   = 34+ remainder 2      2 (Least Significant Digit)
34/16    = 2 + remainder 2      2
2/16     = 0 + remainder 2      2 (Most Significant Digit)
Result   (546)10 =              (222)16
```

6.10 Convert the following binary numbers to hexadecimal numbers:
(a) 101111001011 (b) 101111001101.00110010

Solution

(a) *Conversion of $(101111001011)_2$ to hexadecimal*

$$(101111001011)_2 = (1011)\ (1100)\ (1011) = (BCB)_{16}$$

(b) *Conversion of $(101111001101.00110010)_2$ to hexadecimal*

$$(1011\ 1100\ 1101.00110010)_2 = (1011)\ (1100)\ (1101)\ .\ (0011)\ (0010)$$
$$= (BCD.32)_{16}$$

6.3 BINARY ARITHMETIC

In any numerical system, the most common arithmetical operations are addition, subtraction, multiplication, division, roots, powers, and logarithms, etc. If we perform one plus one operation, we get two by using the simple arithmetic operation of addition. But computers perform arithmetic operations on binary numbers only. In binary arithmetic, the output of one plus one is 0. So this binary operation of addition can be confusing to a person accustomed to working with decimal arithmetic operation only. In this section, the four basic operations of binary arithmetic are discussed.

6.3.1 Binary Addition

It is a very simple task to add two binary numbers and it is very similar to the addition of decimal numbers. In decimal numbers, we start by adding the bits one column at a time, from right to left. Unlike decimal addition, there is little to memorize for the binary addition of bits. The rules of binary addition are given in Table 6.10.

Table 6.10 *Rules of binary addition*

0 + 0 = 0
1 + 0 = 1
0 + 1 = 1
1 + 1 = 0 and a carry 1 (i.e. 10 in binary)
1 + 1 + 1 = 1 and carry 1 (i.e. 11 in binary)

If the sum in one column is a two-bit number, the least significant bit is written as part of the total sum and the most significant bit is carried to the next left column as carry. The following examples of binary addition are given below:

Addition of two binary number $(1\ 1\ 0\ 1)_2$ and $(0\ 0\ 1\ 0)_2$ is

$$\begin{array}{r} 1\ 1\ 0\ 1 \\ +\ 0\ 0\ 1\ 0 \\ \hline 1\ 1\ 1\ 1 \end{array}$$

Similarly, addition of $(1\ 0\ 0\ 1)_2$ and $(1\ 0\ 1\ 1)_2$ is

$$\begin{array}{r} 1\ \ 1 \quad \leftarrow \text{Carry bits} \\ 1\ 0\ 0\ 1 \\ +\ 1\ 0\ 1\ 1 \\ \hline 1\ 0\ 1\ 0\ 0 \end{array}$$

In the first problem of addition, there is no bit to be carried, since the sum of bits in each column was 1. In the second problem, carry is generated and it will be added with the next higher bit.

6.3.2 Binary Subtraction

To subtract one binary number from another, we use the standard techniques, which are adopted for decimal numbers. The subtraction of each bit pair, from right to left, borrowing as needed from bits to the left. The rules of binary subtraction are shown in Table 6.11.

Table 6.11 *Rules of binary subtraction*

0 – 0 = 0
1 – 0 = 1
1 – 1 = 0
0 – 1 = 1 with a borrow of 1

By using rules of binary subtraction, we will be able to subtract two binary numbers. The subtraction of 111 from 1101 is 110 as given below:

$$\begin{array}{r} 1\ \ 1 \leftarrow \text{Borrow bits} \\ 1\ 1\ 0\ 1 \\ -\ 1\ 1\ 1 \\ \hline 1\ 1\ 0 \end{array}$$

6.3.3 Binary Multiplication

Binary multiplication is the same as in real-number algebra, i.e., anything multiplied by 0 is 0, and anything multiplied by 1 remains unchanged. The rules of binary multiplication are given in Table 6.12.

Table 6.12 *Rules of binary multiplication*

$0 \times 0 = 0$
$1 \times 0 = 0$
$0 \times 1 = 0$
$1 \times 1 = 1$

The example of binary multiplication between two binary numbers $(1010)_2$ and $(11)_2$ is given below:

$$\begin{array}{r} 1\ 0\ 1\ 0 \\ \times\ 1\ 1 \\ \hline 1\ 0\ 1\ 0 \\ 1\ 0\ 1\ 0\times \\ \hline 1\ 1\ 1\ 1\ 0 \end{array}$$

The result of the multiplication of $(1010)_2$ and $(11)_2$ is $(1\ 1\ 1\ 1\ 0)_2$.

6.3.4 Binary Division

Division can be performed by repetitive subtraction. The rules of binary division are given in Table 6.13.

Table 6.13 *Rules of binary division*

0/0 = Undefined
1/0 = Undefined
0/1 = 0
1/1 = 1

The example for binary division of $(1011011)_2$ by $(111)_2$ is given below:

$$\begin{array}{r} 111)\ 1011011\ (1101 \\ 0111 \\ \hline 1000 \\ 0111 \\ \hline 000111 \\ 111 \\ \hline 000 \end{array}$$

The result of the binary division of $(1011011)_2$ by $(111)_2$ is $(1\ 1\ 0\ 1)_2$.

6.11 Add the following binary numbers:

(a) $\begin{array}{r} 10100 \\ 11011 \\ \hline \end{array}$ (b) $\begin{array}{r} 101 \\ 011 \\ \hline \end{array}$

Solution

(a) $\begin{array}{r} 1\ 0\ 1\ 0\ 0 \\ 1\ 1\ 0\ 1\ 1 \\ \hline 1\ 0\ 1\ 1\ 1\ 1 \end{array}$

↑

Carry

1 1 ← Carry

(b) $\begin{array}{r} 1\ 0\ 1 \\ 0\ 1\ 1 \\ \hline 10\ 0\ 0 \end{array}$

6.12 Subtract the following binary numbers:

(a) $\begin{array}{r} 11100 \\ -\ 1010 \\ \hline \end{array}$ (b) $\begin{array}{r} 1111 \\ -\ 1011 \\ \hline \end{array}$

Solution

$$\begin{array}{rr} & 1 \leftarrow \text{Borrow} \\ \text{(a)} & 1\ 1\ 1\ 0\ 0 \\ & -\ 1\ 0\ 1\ 0 \\ \hline & 1\ 0\ 0\ 1\ 0 \end{array}$$

$$\begin{array}{rr} \text{(b)} & 1\ 1\ 1\ 1 \\ & -\ 1\ 0\ 1\ 1 \\ \hline & 0\ 1\ 0\ 0 \end{array}$$

6.13 Multiply the following binary numbers:

(a) $\begin{array}{r} 1010 \\ \times\ 101 \\ \hline \end{array}$ (b) $\begin{array}{r} 1111 \\ \times\ 10 \\ \hline \end{array}$

Solution

(a)
$$\begin{array}{r} 1\ 0\ 1\ 0 \\ \times\ 1\ 0\ 1 \\ \hline 1\ 0\ 1\ 0 \\ 0\ 0\ 0\ 0\times \\ 1\ 0\ 1\ 0\times\times \\ \hline 1\ 1\ 0\ 0\ 1\ 0 \end{array}$$

The result of the multiplication of $(1010)_2$ and $(101)_2$ is $(1\ 1\ 0\ 0\ 1\ 0)_2$.

(b)
$$\begin{array}{r} 1\ 1\ 1\ 1 \\ \times\ 1\ 0 \\ \hline 0\ 0\ 0\ 0 \\ 1\ 1\ 1\ 1\times \\ \hline 1\ 1\ 1\ 1\ 0 \end{array}$$

The result of the multiplication of $(1111)_2$ and $(10)_2$ is $(1\ 1\ 1\ 1\ 0)_2$.

6.14 Divide the following binary numbers:

(a) 110)100001 (b) 111)1011011

Solution

(a)
$$\begin{array}{rl} 1\ 1\ 0) & 1\ 0\ 0\ 0\ 0\ 1\ \ (1\ 0\ 1.1 \\ & \underline{0\ 1\ 1\ 0\ \ \ } \\ & 0\ 0\ 1\ 0\ 0\ 1 \\ & \quad\ \underline{1\ 1\ 0\ \ } \\ & \quad\ \ 1\ 1\ 0 \\ & \quad\ \underline{1\ 1\ 0\ \ } \end{array}$$

The result of the binary division of $(100001)_2$ by $(110)_2$ is $(101\ .\ 1)_2$

(b)
$$\begin{array}{rl} 1\ 1\ 1) & 1\ 1\ 0\ 0\ 0\ 1\ \ (111 \\ & \ \ \underline{1\ 1\ 1\ \ } \\ & 0\ 1\ 0\ 1\ 0 \\ & \quad\ \underline{1\ 1\ 1\ \ } \\ & \quad\ \ 1\ 1\ 1 \\ & \quad\ \underline{1\ 1\ 1\ \ } \end{array}$$

The result of the binary division of $(1\ 1\ 0\ 0\ 0\ 1)_2$ by $(111)_2$ is $(111)_2$.

6.4 BINARY CODED DECIMAL (BCD) NUMBER SYSTEM

We are already familiar with the binary, decimal, octal and hexadecimal number systems. If we represent single-digit values for hex, the numbers 0–F, then these numbers can represent the values 0–15 in decimal, and occupy a nibble. Often, we wish to use a binary equivalent of the decimal system. This system is called Binary Coded Decimal or BCD, which also occupies a nibble. In BCD, the binary patterns 1010 through 1111 do not represent valid BCD numbers, and cannot be used. Table 6.14 shows the BCD equivalent of decimal number from 0 to 9. This Code is called as 8421 BCD code. This code replaces each decimal figure with a group of 4 bits in binary form. The conversion from decimal to BCD is performed according to Table 6.14.

Table 6.14 *BCD Code*

Decimal Number	*Binary Coded Decimal Number*			
	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Conversion from Decimal to BCD is very simple as shown in Table 6.14. Each digit of the decimal number can be represented by a byte. Then we can convert 0 through 9 to 0000 0000 through 0000 1001. The BCD equivalent value for the decimal number 5,219 is shown below. Since there are four digits in 5219 decimal number, there are four bytes in BCD number representation of 5219.

Thousands	*Hundreds*	*Tens*	*Units*
5	2	1	9
0 0 0 0 0 1 0 1	0 0 0 0 0 0 1 0	0 0 0 0 0 0 0 1	0 0 0 0 1 0 0 1

In computers, a minimum of 1 byte is required for storing a number. Therefore, we can say that the upper nibble of each BCD number is wasting storage space. BCD is still a weighted position number system in which we can perform mathematics, but we must use special techniques in order to obtain a correct answer.

6.15 Find the BCD of the following decimal number:
(a) 99 (b) 2487

Solution

(a) The BCD equivalent of $(99)_{10}$ is 1001 1001.
(b) The BCD equivalent of $(2487)_{10}$ is 0010 0100 1000 0111.

6.16 Determine the decimal equivalent of the following BCD numbers:
(a) 0111 0001 0101 0001 (b) 1001 0101 011 0110

Solution

(a) The BCD number is 0111 0001 0101 0001.

The BCD number is divided into 4-bit groups and then converted into its decimal equivalent.

Therefore, 0111 0001 0101 0001 = (0111) (0001) (0101) (0001) = 7151

(b) The BCD number is 1001 0101 011 0110.

The BCD number is divided into 4-bit groups and then converted into its decimal equivalent.

Therefore, 1001 0101 011 0110 = (1001) (0101) (0011) (0110) = 9536

6.5 BOOLEAN ALGEBRA

Boolean algebra was introduced by the mathematician George Boole in 1854. It is a two-state algebra used to solve logic problems and perform the logical and arithmetic calculations for digital equipments. This operates with logic variables, namely, '0' and '1'. The logic variables can also be represented by logical TRUE (T) and logical FALSE (F). Any statement can be represented by a logic variable. One example is "The sun rises in the east, (TRUE)". In this way, any statement can be modeled as a logic variable.

Boolean logic variables 0 or 1 are not used to represent actual numbers but are used to represent the state of voltage variables called logic levels. Commonly used representation of logic levels are shown in Table 6.15.

Table 6.15 *Representation of logic level*

Logic 0	*Logic 1*
False	True
Open Switch	Close Switch
Low	High
No	Yes
Off	On

Boolean Algebra consists of several rules of relationship between mathematical quantities, namely, true or false; '1' or '0'. This is a two-state algebra to solve logic problems. Presently, Boolean algebra is the backbone of a computer and it is also used to analyze and design digital circuits.

Boolean algebra uses alphabetical letters to denote variables in the same way as normal algebra. Boolean variables are always capital letters, never lowercase, as these variables are allowed to possess only one of two possible values, either '1' or '0'. The inversions, AND and OR operation of Boolean algebra, are explained as follows.

6.5.1 Inversion Operation

Each variable has a complement, meaning the opposite of its value. If we consider variable A has a value of '0', then the complement of A has a value of '1'. Boolean

notation uses a bar above this variable character to denote complementation as given below:

If $A = 0$ then $\overline{A} = 1$

or If $A = 1$ then $\overline{A} = 0$

The complement of A is denoted as A-not or A-bar. The prime symbol is also used to represent complementation. For an example, the complement of A will be A'. For inversion operation, NOT gate is used as depicted in Fig. 6.5.

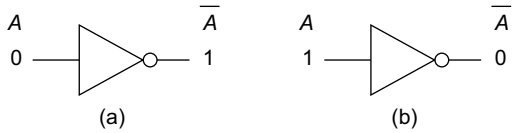


Fig. 6.5 *(a) and (b) Inversion operation*

6.5.2 OR Operation

In mathematics, the sum of any number and zero is the same as the original number. This algebraic identity can be written as $X + 0 = X$, where X is any number. Similar to ordinary algebra, Boolean algebra, has its individual identities based on the bivalent states of Boolean variables. In Boolean algebra, the sum of anything (1 or 0) and zero (0) is the same as anything (1 or 0). This logical function is known as OR operation. The equation for OR operation is

$$O = A \text{ OR } B$$

In Boolean algebra the '+' sign stands for the OR operation and the equation for OR operation is $O = A + B$. Figure 6.6 shows the relationship between inputs and output for OR operation.

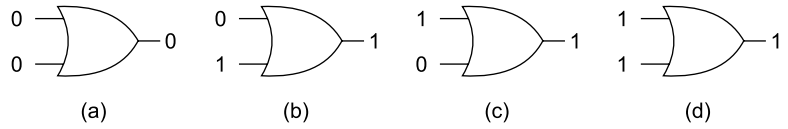


Fig. 6.6 *OR operation*

6.5.3 AND Operation

Multiplication is also valid in Boolean algebra and it is the same as in real-number algebra. Anything multiplied by 0 is 0, and anything multiplied by 1, is 1. This is nothing but the truth table for an AND gate. In other words, Boolean multiplication corresponds to the logical function of an AND gate. The equation for AND operation is

$$O = A.\ B$$

In Boolean algebra the multiplication sign, 'stands for AND operation. The above equation can be written simply $O = AB$. Figure 6.7 shows the AND operation.

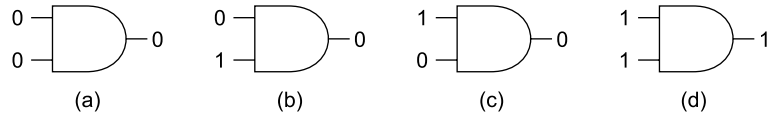


Fig. 6.7 *AND operation*

6.6 BOOLEAN LAWS

Boolean laws have been derived by using Boolean postulates. These laws are used to design and analyze logic circuits mathematically. Table 6.16 shows the Boolean laws. In this section, all these laws are explained.

Table 6.16 *The Boolean laws*

Laws of Union	
Law 1	$A + 0 = A$
Law 2	$A + 1 = 1$
Laws of Intersection	
Law 3	$A \,.0 = 0$
Law 4	$A.1 = \mathrm{A}$
Laws of Tautology	
Law 5	$A + A = A$
Law 6	$AA = A$
Laws of Complements	
Law 7	$A + \overline{A} = 1$
Law 8	$A.\overline{A} = 0$
Laws of Double Complements	
Law 9	$\overline{\overline{A}} = \mathbf{A}$
Laws of Commutation	
Law 10	$A + B = B + A$
Law 11	$AB = BA$
Laws of Association	
Law 12	$A + (B + C) = (A + B) + C$
Law 13	$A(BC) = (AB)C$
Laws of Distribution	
Law 14	$A(B + C) = AB + AC$
Law 15	$(A + B)(C + D) = AC + AD + BC + BD$
Laws of Absorption	
Law 16	$A\,(A + B) = A$
Law 17	$A + AB = A$
Law 18	$A(\overline{A} + B) = AB$
Law 19	$AB + \overline{B} = A + \overline{B}$
Law 20	$A\overline{B} + B = A + B$
De Morgan's Theorem	
Law 21	$\overline{A+B} = \overline{A}\,.\,\overline{B}$
Law 22	$\overline{A.B} = \overline{A} + \overline{B}$

6.6.1 Laws of Union

This is the first Boolean identity. It means that the sum of anything (1 or 0) and zero (0) is the same as that quantity (1 or 0). There is no difference between Boolean identity, laws of union and real-number algebra. Law 1 and Law 2 of Laws of union are shown in Fig. 6.8(a) and (b) respectively and their operations are explained as follows:

Law 1: $A + 0 = A$

Law 1 means that the output is always A and depends on the value of A. When $A = 1$, the output will be 1. If $A = 0$, output will be 0.

Law 2: $A + 1 = 1$

It means that output is independent of A and it will be always the same when $A = 1$ or $A = 0$. This identity is different from any seen in normal algebra. Here, we can see that the sum of anything and '1' is '1'.

Fig. 6.8 *Laws of union*

6.6.2 Laws of Intersection

There are two intersection identities: $A.0$, and $A.1$. These two laws are stated below with the help of Fig. 6.9(a) and (b):

Law 3 $A.0 = 0$

This law states that if one of two inputs in the AND gate is logic zero (0) and other input is connected with signal A, the output will be logic zero (0).

Law 4 $A.1 = A$

It is depicted in Fig. 6.9(b) that if one of two inputs in the AND gate is logic 1 and the other input is connected with signal A, the output will be A.

Fig. 6.9 *Laws of intersection*

6.6.3 Laws of Tautology

Law 5 $A + A = A$

The output of adding A and A together is A as shown in Fig. 6.10(a). When both inputs of an OR gate are connected to each other and output will be A same as input.

Law 6 $A.A = A$

In normal algebra, the product of a variable and itself is the square of that variable. But in Boolean algebra, $A.A$ is equal to A as depicted in Fig. 6.10(b). The equation, $A.A = A$ means that the product of a Boolean quantity and itself is the original quantity like $0 \times 0 = 0$ and $1 \times 1 = 1$. If both inputs of an AND gate are connected to each other and output will be A same as input.

Fig. 6.10 *Laws of tautology*

6.6.4 Laws of Complements

Law 7 $A + \overline{A} = 1$

In laws of complement of Boolean algebra, the output of OR operation of any variable and its complement is always '1'. So, the sum of any Boolean quantity and its complement must be '1' as shown in Fig. 6.11(a).

Law 8 $A.\overline{A} = 0$

In Boolean mathematics, the AND operation output between a variable A and its complement, $\overline{A}$ is 0. Therefore, the output must be '0' for AND operation between any variable and its complement. As the product of any Boolean quantity and '0' is '0', the product of a variable and its complement must be '0' as shown in Fig. 6.11(b).

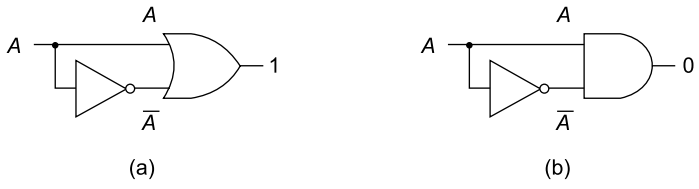


Fig. 6.11 *Laws of complements*

6.6.5 Laws of Double Complements

Law 9 $\overline{\overline{A}} = A$

There is also one identity with complementation that is known as double complement. Double complement means that a variable inverted twice. It simply states that it is actually the complement of the complement of a variable. After complementing a variable twice, we get the original Boolean value as shown in Fig. 6.12.

If $A = 0$, $\overline{A} = 1$ and $\overline{\overline{A}} = 0 = A$

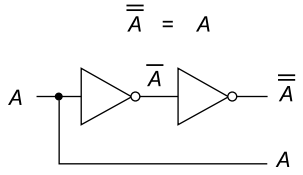


Fig. 6.12 *Laws of double complements*

6.6.6 Laws of Commutation

Law 10 $A + B = B + A$

Law 11 $AB = BA$

The commutative law is also applicable for Boolean algebra, and it applies equally to addition and multiplication. From this commutative property, we can say that we can reverse the order of variables in addition or multiplication as shown in Fig. 6.13(a) and (b) respectively.

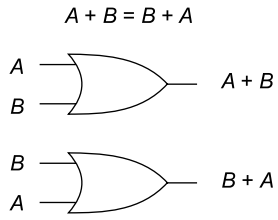


Fig. 6.13(a)

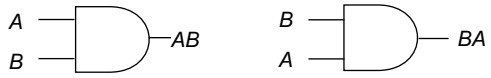


Fig. 6.13(b) *Laws of commutation*

6.6.7 Laws of Association

Law 12 $A + (B + C) = (A + B) + C$

Law 13 $A(BC) = (AB)C$

Laws of association of Boolean algebra are same as for conventional algebra. So associative property can be applied in addition and multiplication of variables as depicted in Law 12 and Law 13. Using this property, we can add or multiply between associate groups with parentheses as depicted in Fig. 6.14. In this case, the truth table will not be changed.

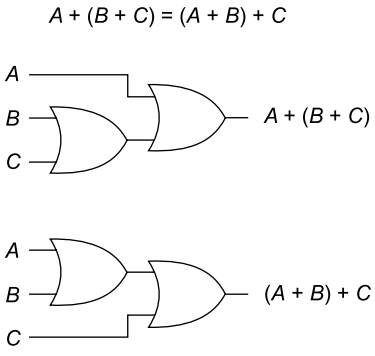


Fig. 6.14 *Law of association*

6.6.8 Laws of Distribution

Law 14 $A(B + C) = AB + AC$

Law 15 $(A + B)(A + C) = A + BC$

The laws of distribution are used to expand any Boolean expression. Laws 14 and 15 show the product of a sum and in reverse how all terms can be factored out of Boolean sums-of-products as depicted in Fig. 6.15.

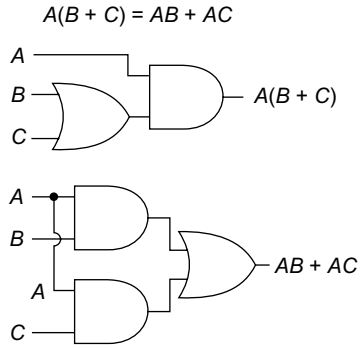


Fig. 6.15 ***Laws of distribution***

6.6.9 Laws of Absorption

Law 16	$A\,(A + B) = A$
Law 17	$A + AB = A$
Law 18	$A(\overline{A} + B) = AB$
Law 19	$AB + \overline{B} = A + \overline{B}$
Law 20	$A + \overline{A}\,B = A + B$

There are five laws of absorption in Boolean algebra as given above. These laws are used in the simplification of logic circuits. When logic circuits are represented by the most simplified Boolean form, the logic circuit is able to perform the same function with fewer logic gates. As a result, the reliability of the logic circuit will be increased and cost of manufacture will be decreased.

6.17 Prove $A(A + B) = A$

Solution

$A(A + B)$	$=$	$AA + AB$	Applying distributive property
	$=$	$A + AB$	Applying identity $AA = A$
	$=$	$A.1 + AB$	Factoring out A
	$=$	$A(1 + B)$	Apply identity $1 + B = 1$
	$=$	$A.1$	Apply identity $A.1 = A$
	$=$	A	

6.18 Prove $(A + B)\,(B + C) = B + AC$

Solution

$(A + B)\,(B + C)$	$=$	$AB + AC + BB + BC$	Applying distributive property
	$=$	$AB + AC + B + BC$	Applying identity $BB = B$
	$=$	$B + AB + AC + BC$	Apply $B + AB = B$
	$=$	$B + AC + BC$	
	$=$	$B + BC + AC$	Apply $B + AB = B$
	$=$	$B + AC$	

6.7 DE MORGAN'S THEOREM

De Morgan developed two important rules for group complementation in Boolean algebra. These two rules are the following:

De Morgan's First Theorem

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

De Morgan's Second Theorem

$$\overline{A.B} = \overline{A} + \overline{B}$$

De Morgan's First Theorem: Break → $\overline{A+B}$ → $\overline{A}\ \overline{B}$

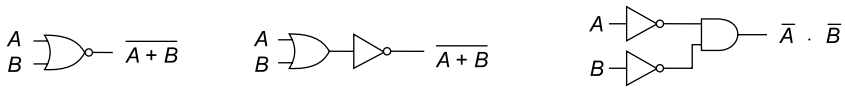
De Morgan's Second Theorem: Break → $\overline{AB}$ → $\overline{A} + \overline{B}$

6.7.1 De Morgan's First Theorem

According to De Morgan's first theorem, when a long bar is broken, the operation directly under the break changes from addition to multiplication as given below.

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

Both sides of the Boolean expression can be represented by logic circuits.



(a) (b) (c)

Fig. 6.16 ***De Morgan's first theorem***

Figure 6.16(a) is a 2-input NOR gate and Fig. 6.16(b) is the substitute of NOR gate using OR and inverter. Here the output is equal to

$$O = \overline{A+B}$$

Table 6.17 *Truth table*

Inputs		*Output*
A	*B*	$O = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Figure 6.16(c) has inverted inputs before they reach the AND gate. Therefore, the Boolean equation of output is

$$O = \overline{A} \cdot \overline{B}$$

Table 6.18 *Truth table*

Inputs		*Output*
A	*B*	$O = \overline{A} \cdot \overline{B}$
0	0	1
0	1	0
1	0	0
1	1	0

After comparing Tables 6.17 and Table 6.18, we can say that they are identical. This means the two circuits are logically equivalent; given the same inputs, the outputs are same. In other words, the circuits shown are interchangeable. Therefore, De Morgan's first theorem is proved from truth tables.

6.7.2 De Morgan's Second Theorem

According to De Morgan's second theorem, when a long bar is broken, the operation directly under the break changes from multiplication to addition as given below:

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

Both sides of the above Boolean equation can be implemented by logic circuits as shown in figures below.

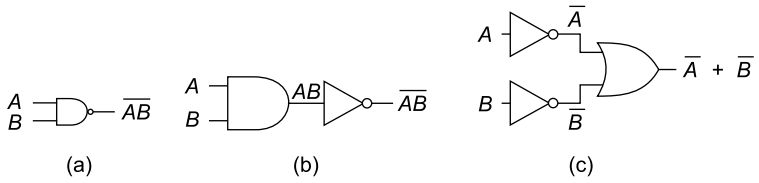


Fig. 6.17 ***De Morgan's second theorem***

Figure 6.17(a) is a 2-input NAND gate. Therefore, the Boolean equation of output is

$$O = \overline{A \cdot B}$$

Table 6.19 *Truth table*

Inputs		*Output*
A	*B*	$O = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Figure 6.17(c) has inverted inputs before they reach the OR gate. Therefore, the Boolean equation of output is

$$O = \overline{A} + \overline{B}$$

Table 6.20 *Truth table*

Inputs		*Output*
A	B	$O = \overline{A} + \overline{B}$
0	0	1
0	1	1
1	0	1
1	1	0

We can say that Table 6.19 and Table 6.20 are identical. This means the two circuits are logically equivalent; given the same inputs, the outputs are same. In other words, the circuits shown are interchangeable. In this way, the De Morgan's second theorem is proved.

6.19 Prove $A + B + C + D + \overline{A.BCD} = 1$

Solution

$A + B + C + D + \overline{ABCD} = A + B + C + D + \overline{A} + \overline{B} + \overline{C} + \overline{D}$ Breaking long bar in $ABCD$

$= A + \overline{A} + B + \overline{B} + C + \overline{C} + D + \overline{D}$ Apply identity $A + \overline{A} = 1$

$= 1 + 1 + 1 + 1$

$= 1$

6.8 LOGIC GATES

Logic gates are electronic circuits with a number of inputs and one output. The output voltage depends on the input voltages. Logic gate circuits are most commonly represented in a schematic by symbols in place of constituent transistors and resistors. The digital systems can be made by using three basic logic gates. These are AND gate, OR gate and NOT gate. The AND gate is an electronic circuit whose output is high when all its inputs are high. The OR gate is also an electronic circuit which gives a high output if one or more of its inputs are high. The NOT gate generates an inverted version of the input logic at its output. The most commonly used other logic gates are NAND, NOR, XOR, INV, and BUF. The term INV stands for 'inverter' and BUF stands for 'buffer'. In this section, functions of all logic gates have been explained elaborately.

6.8.1 AND Gate

The expression $O = A.B$ means output *'O'* equals A **AND** B. The '.' sign stands for the AND operation and actually it is same as ordinary multiplication of 1s and 0s. The AND operation produces a result of '1', when all input variables are '1'. But the output is '0' when one or more inputs are '0'. Figure 6.18 shows the two inputs AND gate and truth table is given in Table 6.21.

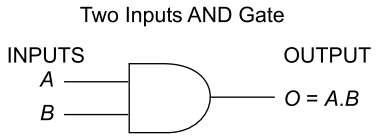


Fig. 6.18 *Two-input AND gate*

Table 6.21 *Truth table of two-input AND gate*

Inputs		*Output*
A	*B*	*O* = *A* . *B*
0	0	0
0	1	0
1	0	0
1	1	1

6.8.2 OR Gate

The expression $O = A + B$ is defined as output *'O'* equals *A* **OR** *B*. The + sign stands for the OR operation and it is not for arithmetic addition. When any of the inputs of OR gate is '1' the output of the OR gate will be '1'. But the output of OR gate is '0' only when all the input variables are '0'. The symbol of two inputs OR gate is shown in Fig. 6.19 and the truth table is also given in Table 6.22.

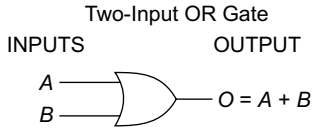


Fig. 6.19 *Two-input OR gate*

Table 6.22 *Truth table of two-input OR gate*

Inputs		*Output*
A	*B*	*O* = *A* + *B*
0	0	0
0	1	1
1	0	1
1	1	1

6.8.3 NOT Gate

The NOT gate or inverter circuit is represented by the symbol as shown in Fig. 6.20(a). An alternative symbol for an inverter is shown in Fig. 6.20(b). The NOT Gate has one input signal and one output signal. When the input signal *A* is subjected to the NOT operation, the output *O* can be expressed as

$$O = \overline{A} \text{ or } O = A'$$

Here, '–' or (′) represents the NOT operation. This expression means output *'O'* equals NOT *A* or *O* equals the inverse of *A* or *O* equals the complement of *A*. The truth table of the NOT gate is shown in Table 6.23. The NOT gate operations can be referred as inversion or complementation.

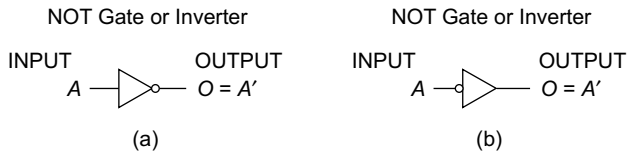


Fig. 6.20 ***NOT gate***

Table 6.23 *Truth table of NOT gate*

Inputs	*Output*
A	$O = \overline{A} = A'$
0	1
1	0

The NOT operation is also referred to as inversion or complementation, and these terms are used interchangeably.

6.8.4 NOR Gate

NOR gate is extensively used in digital electronic circuit. This gate is the combination of the basic gates AND, OR and NOT. NOR is the same as the inverted OR gate and its symbol is shown in Fig. 6.21. This gate has a small circle on the output. This small circle represents the inversion operation and the output expression of the two inputs NOR gate is

$$O = \overline{A + B} = (A + B)'.$$

The truth table of the NOR gate is shown in Table 6.24.

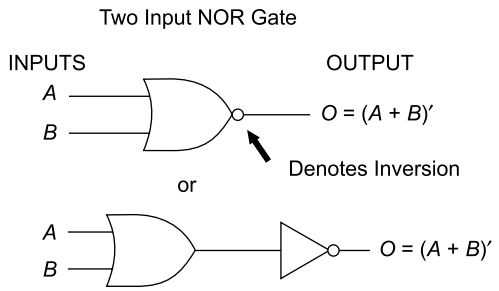


Fig. 6.21 ***Two-input NOR gate***

Table 6.24 *Truth table of two-input NOR gate*

Inputs		*Output*
A	*B*	$O = \overline{A+B} = (A + B)'$
0	0	1
0	1	0
1	0	0
1	1	0

6.8.5 NAND Gate

The inverted operation of AND gate is the NAND gate and its symbol is depicted in Fig. 6.22. There is a small circle on the output. This small circle represents the inversion operation. The output of the two inputs NAND gate can be expressed as

$$O = \overline{AB} = (AB)'.$$

The truth table of two inputs AND gate is given in Table 6.25.

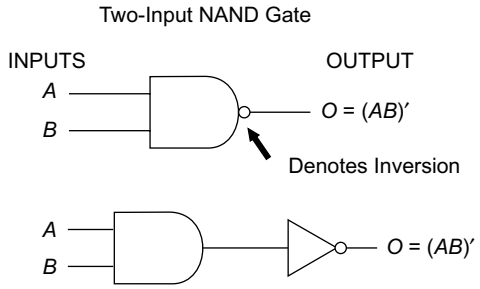


Fig. 6.22 *Two-input NAND gate*

Table 6.25 *Truth table of two-input NAND gate*

Inputs		*Output*
A	*B*	$O = \overline{AB} = (AB)'$
0	0	1
0	1	1
1	0	1
1	1	0

6.8.6 Exclusive-OR gate

The operation of the Exclusive-OR gate is quite different from the OR gate. When the inputs of Exclusive-OR gate are at different logic levels either '0' and '1' or '1' and '0', its output is 'high'. On the other hand, output of Exclusive-OR gate is 'low' logic level if the inputs are at the same logic

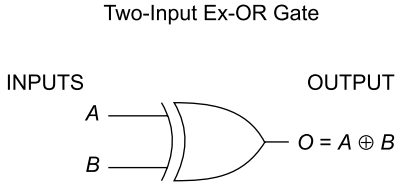


Fig. 6.23 *Ex-OR gate*

levels. The Exclusive-OR gate can be written as XOR or Ex-OR gate. Figure 6.23 shows the two-input Ex-OR gate and truth table is given in Table 6.26. The output of the two inputs XOR gate can be expressed as

$$O = A \oplus B$$

Table 6.26 *Truth table of XOR gate*

Inputs		*Output*
A	*B*	$O = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

6.8.7 Exclusive-NOR gate

The last gate for analysis is the Exclusive-NOR gate and it is known as the XNOR gate. It is equivalent to an Exclusive-OR gate with an inverted output. The truth table for this gate is absolutely opposite of the Exclusive-OR gate as given in Table 6.27. The output of the two inputs XNOR gate can be represented by

$$O = \overline{A + B}$$

Table 6.27 *Truth table of XOR gate*

Inputs		*Output*
A	*B*	$O = \overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

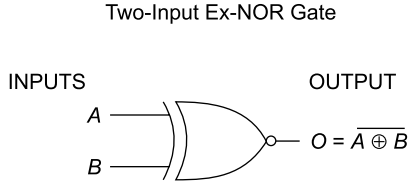


Fig. 6.24 ***Ex-NOR gate***

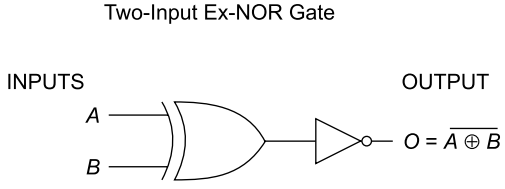


Fig. 6.25 ***Equivalent circuit of Ex-NOR gate***

Figure 6.24 shows the two-input Ex-NOR gate and its equivalent is depicted in Fig. 6.25. From the truth table, it is very clear that the purpose of an Exclusive-NOR gate is to output a 'high' when both inputs are at the same logic levels.

6.9 UNIVERSAL GATE

NAND and NOR gates have a unique property that they are universal. It means that universal gates are able to mimic the operation of any other gate. For example, the interconnected NAND gates can generate the OR function. Similarly, any gate can be replaced by the NAND and NOR gates. The construction of NOT, AND, and OR gate using NAND and NOR gates are explained below.

6.9.1 The NOT Gate Using NAND and NOR

It is depicted in Fig. 6.26 that there are two ways to construct a NOT gate or an inverter using NAND and NOR gates. The first method is that both input terminals of NAND and NOR gates will be interconnected and it will be same as inverter input terminal. In Fig. 6.26(a) and Fig. 6.26(c), both terminals are interconnected and used as an inverter input terminal. In the other method, one terminal is used as input and the unused terminal is connected with $+V_{CC}$ for NAND gate and ground for NOR gate as shown in Fig. 6.26(b) and Fig. 6.26(d) respectively.

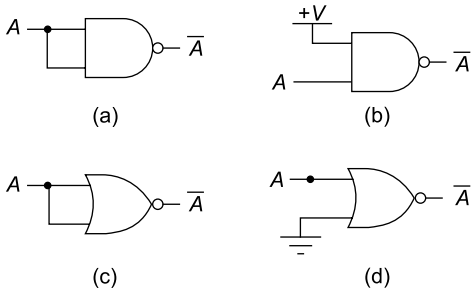


Fig. 6.26 *(a) NOT gate using NAND (b) NOT gate using NAND, (c) NOT gate using NOR (d) NOT gate using NOR*

6.9.2 The AND Gate Using NAND Gate

To construct an AND gate from NAND gates, an inverter or a NOT gate is required to invert the output of a NAND gate. This inversion cancels out the first inverted operation of NAND gate and the final result will be AND function as depicted in Fig. 6.27(a). The same function can also be implemented using NOR gates. Initially, all of the inputs are inverted using NOR gates as inverter and then fed to another NOR

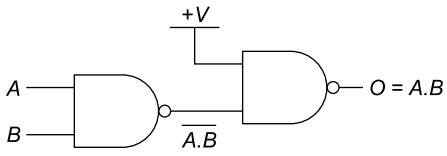


Fig. 6.27(a) *AND gate using NAND gate*

gate. So, three NOR gates are required to build up a AND gate as shown in Fig. 6.27(b).

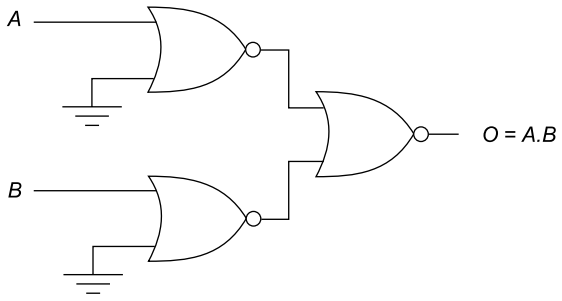


Fig. 6.27(b) *AND gate using NOR gate*

6.9.3 The OR Gate Using NAND and NOR

Figure 6.28 shows the construction of OR gate using NAND gates. Initially, all inputs are inverted by using NAND gates and then results are fed to another NAND gate for getting OR function. In this way, an OR gate can developed using three NAND gates. On the hand, an OR gate can be created by inverting the output of a NOR gate as shown in Fig. 6.29.

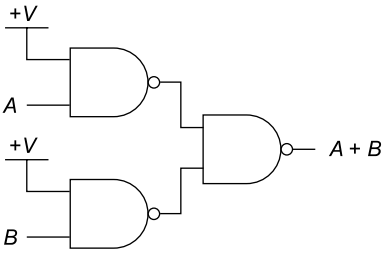


Fig. 6.28 *OR gate using NAND gate*

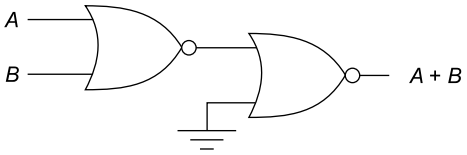


Fig. 6.29 *OR gate using NOR gate*

6.20 Write the truth table of the logic circuit as shown in Fig. 6.30.

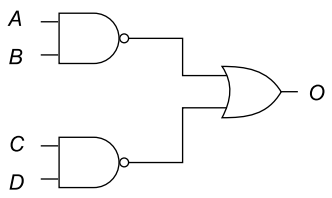


Fig. 6.30 *Logic circuit of Ex. 6.20*

Solution

Truth table of the above logic circuit is given below:

Table 6.28 *Truth table for Fig. 6.30*

A	B	C	D	$\overline{AB}$	$\overline{CD}$	$O = \overline{AB} + \overline{CD}$
0	0	0	0	1	1	1
0	0	0	1	1	1	1
0	0	1	0	1	1	1
0	0	1	1	1	0	1
0	1	0	0	1	1	1
0	1	0	1	1	1	1
0	1	1	0	1	1	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	0	0	0

6.21 Draw the circuit diagram of the logic expression:

$$O = \overline{A + BC} + ACD$$

Solution

The logic circuit diagram of Boolean expression is shown in Fig. 6.31. It is clear from this figure that two AND gates, one NOR gate and one OR gate are required to implement the logical equation $O = \overline{A + BC} + ACD$.

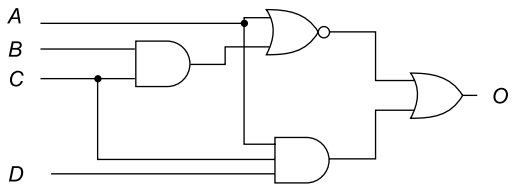


Fig. 6.31 ***Circuit diagram of Ex. 6.21***

6.22 Write the truth table of the logic circuit as shown in Fig. 6.32.

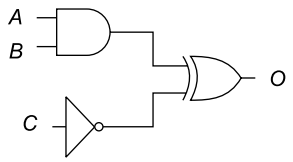


Fig. 6.32 ***Logic circuit of Ex. 6.22***

Solution

Truth table of the above logic circuit is given below:

Table 6.29 *Truth table for Fig. 6.32*

A	B	C	AB	$\overline{C}$	$AB \oplus \overline{C}$
0	0	0	0	1	1
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	0	0	0
1	1	0	1	1	0
1	1	1	1	0	1

6.23 Draw the output of the two input Ex-NOR gate with the given inputs A and B.

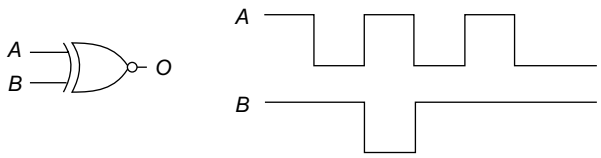


Fig. 6.33 ***Logic circuit of Ex. 6.23***

Solution

The A waveform can be read as 101010 and B waveform can be represented as 110111. The digital output of OR gate will be 100010. The waveform of output is given below:

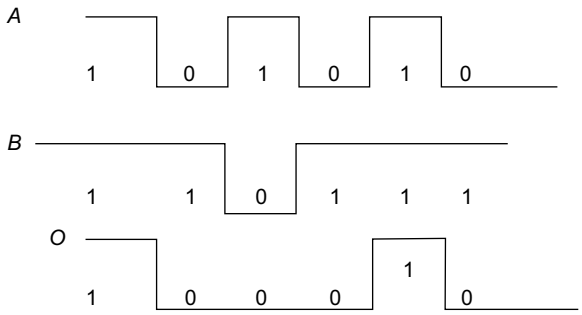


Fig. 6.34 ***Output waveform of Ex. 6.23***

6.24 Simplify the logic expression $O = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D}$.

Solution

$O = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D}$ Factoring out $\overline{A}\overline{C}$

$= \overline{A}\overline{C}(\overline{B}\overline{D} + \overline{B}D + B\overline{D})$ Factoring out $\overline{B}$ from first and second terms of $(\overline{B}\overline{D} + \overline{B}D + B\overline{D})$

$= \overline{A}\overline{C}(\overline{B}(\overline{D} + D) + B\overline{D})$ Applying $\overline{D} + D = 1$

$= \overline{A}\overline{C}(\overline{B} + B\overline{D})$

6.25 Simplify the following logic expressions using De Morgan's theorem.

(a) $O = \overline{(A + B + C)(\overline{A} + \overline{B} + C)}$

(b) $O = \overline{A + BCD}$

Solution

(a) $O = \overline{(A + B + C)(\overline{A} + \overline{B} + C)}$

$= \overline{A + B + C} + \overline{\overline{A} + \overline{B} + C}$

$= \overline{A}\overline{B}\overline{C} + AB\overline{C}$

(b) $O = \overline{A + BCD}$

$= \overline{A}\overline{BCD}$

$= \overline{A}(\overline{B} + \overline{C} + \overline{D})$

6.10 DIGITAL LOGIC CIRCUITS

Logic gates are discussed in Section 6.8. At present, these gates are available in integrated form and the digital integrated circuits (ICs) are most commonly used in complex digital logic circuits design. The logic gates can be designed in different methods. Therefore, there are different types of logic families, but unipolar and bipolar logic families are the main logic families. Transistors, diodes and resistors are the main elements of bipolar logic families. but MOSFETs are used in unipolar logic families. In this section, bipolar logic families are discussed briefly.

6.10.1 Classification of Digital Logic Circuits

The digital logic circuits have broadly two categories, namely, bipolar logic and unipolar logic. The *bipolar logic families* are classified as saturated and unsaturated types. In saturated type of bipolar logic family, transistors are operated in between cut-off and saturation. Resistor Transistor Logic (RTL), Direct Coupled Transistor Logic (DCTL), Integrated Injection Logic (IIL or I^2L), Diode Transistor Logic (DTL), Transistor Transistor Logic (TTL), and High Threshold Logic (HTL) are commonly used bipolar logic families. In *unsaturated bipolar logic family*, the transistors are operated in between cut-off and non-saturation. Schotty TTL and Emitter coupled logic (ECL) are example of unsaturated bi-polar logic family. There are two types of unipolar logic family namely *P*-channel MOS (PMOS) and *n*-channel MOS (NMOS) and complementary MOS (CMOS). The classification of digital logic circuits is shown in Fig. 6.35.

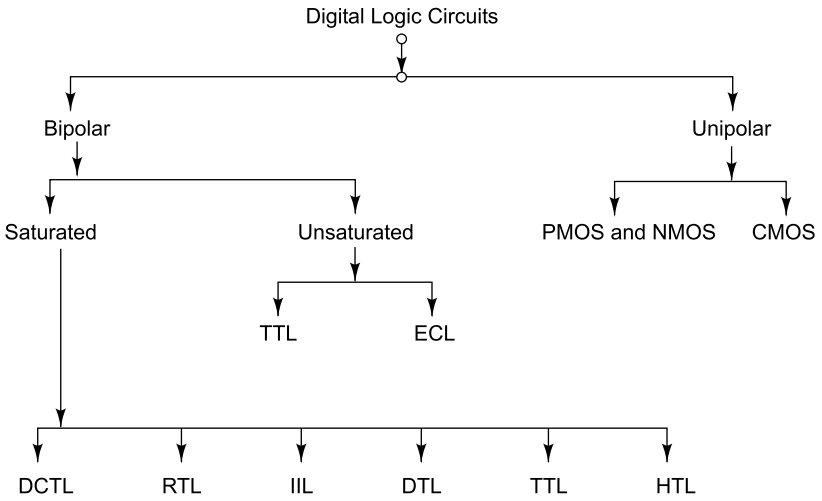


Fig. 6.35 ***Classification of digital logic circuits***

6.10.2 Characteristics of Digital Logic Circuit

Before discussion on various types of logic families, the performance parameters of a logic family are explained for better understanding. The most important performance parameters are given below:

- Speed of operation
- Power dissipation
- Voltage parameters
- Current parameters
- Noise immunity
- Fan-in
- Fan-out
- Cost
- Availability

The designer should select a particular logic family for any application based on the actual requirement. To design an efficient logic circuit, the designer should study the performance parameters from IC manuals in detail.

Speed of Operation The operating speed of a logic family is determined from the propagation delay. If a square wave is applied to the input of an inverter, the output of the inverter will be a square wave as shown in Fig. 6.36. It is very clear from Fig.6.36 that the propagation delay is measured from the time difference between 50% logic transition of input from its initial value and 50% logic transition of output. There are two types of propagation delay times, namely, t_{PHL} and t_{PLH}.

The propagation delay t_{PHL} is the delay time when output changes from HIGH to LOW due to change in input. Similarly, t_{PLH} is the propagation delay for output changes from LOW to HIGH. Generally, t_{PHL} and t_{PLH} are very close to each other. Actually, we consider the average value of t_{PHL} and $t_{PLH.}$ The propagation delay varies

in between 1 to 20 nanoseconds. For proper operation of a logic gate, the time period of input signal must be more than the propagation delay time. If input frequency is very high, and the cycle time is less than propagation delay, the switch starts malfunctioning.

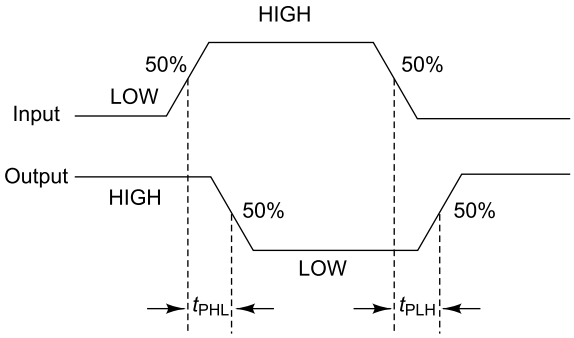


Fig. 6.36 *Input and output waveform of an inverter*

Power Dissipation Power dissipation is the amount of power drawn from the supply during static and dynamic condition. In static condition, the power dissipated in a logic gate is called *static power consumption*, and similarly the *dynamic power consumption* takes place in dynamic condition or switching transitions. The static power consumption is the power dissipated in logic gates when the device is either ON or OFF. During the transition from OFF to ON or ON to OFF, the power consumed in a gate is called dynamic power consumption. The voltage and current waveforms of logic gates are depicted in Fig. 6.37.

The power dissipation is directly proportional to switching frequency and inversely proportional with cycle time. CMOS ICs have very low power consumption at low frequency. If frequency increases, power dissipation increases. The average power dissipation is determined by the simplest expression $V_{CC}I_C$, where I_C is the average value of current. Generally, the power dissipation varies in the range of milliwatts (mW).

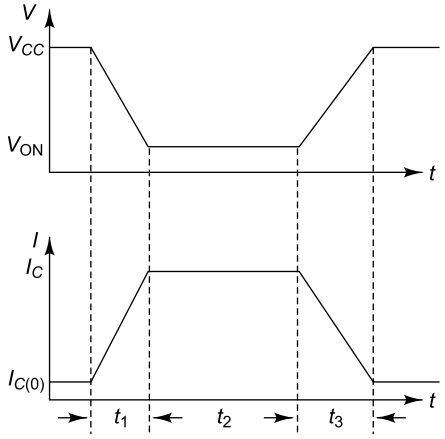


Fig. 6.37 *Voltage and current wave form of a logic gate*

Voltage Parameters

- *High-level Input Voltage (V_{IH})* V_{IH} is the minimum input voltage guaranteed to be recognised as logic 1 or HIGH. V_{IH} is 2 V for TTL and 3.5 V for CMOS. If input voltage is less than V_{IH}, it will not be accepted as logic 1 or HIGH.
- *Low-level Input Voltage (V_{IL})* V_{IL} is the maximum input voltage guaranteed to be recognised as logic 0 or LOW. V_{IL} is 0.8 V for TTL and 1.5 V for CMOS. When input voltage is greater than V_{IL}, it will not be accepted as logic 0 or LOW.
- *High-level Output Voltage (V_{OH})* V_{OH} is the minimum output voltage for HIGH state or logic 1 under defined load conditions. V_{OH} is 2.4 V for TTL and 4.9 V for CMOS.
- *Low-level Output Voltage (V_{OL})* V_{OL} is the maximum output voltage for LOW state or logic 0. V_{OL} is 0.4V for TTL and 0.1 V for CMOS.

Current Parameters

- *High-level Input Current (I_{IH})* I_{IH} is the current that flows into an input when a high level or logic '1' voltage is applied to that input.
- *Low-level Input Current (I_{IL})* I_{IL} is the current that flows into an input when a low level or logic '0' voltage is applied to that input.
- *High-level Output Current (I_{OH})* I_{OH} is the maximum current that flows from an output and the output can source in HIGH state or logic '1' while still maintaining the output voltage above $V_{OH.}$
- *Low-level Output Current (I_{OL})* I_{OL} is the maximum current that the output can sink in LOW state or logic '0' while still maintaining the output voltage below $V_{OL.}$

Noise Immunity Noise is always present in electronics circuits due to stray electric and magnetic fields. This signal is unwanted and spurious. Sometimes, the noise signal distorts the output voltage of the gate. Noise immunity of a logic gate means the circuit's ability to tolerate noise. In order to correctly recognise logic '0' and logic '1' states, noise immunity is measured quantitatively which is known as Noise Margin (NM). There are two types of noise margin such as low noise margin and high noise margin.

- *Low Noise Margin (LNM), V_{NL}* V_{NL} is the largest noise amplitude that is guaranteed for no change of the output voltage level when the input voltage of the logic gate is in the LOW interval. The low noise margin is measured by the expression as given below:

$$V_{NL} = V_{IL} - V_{OL}$$

- *High Noise Margin (HNM), V_{NH}* V_{NH} is the largest noise amplitude that is guaranteed for no change of the output voltage level when the input voltage of the logic gate is in the HIGH interval. It is measured by

$$V_{NH} = V_{OH} - V_{IH}$$

Fan-In Fan-in is the maximum number of inputs for a logic gate in a particular logic family. This number is limited due to delay time. For example, a two-input AND gate has fan-in of two, a three-input OR gate has a fan-in of three and a NOT gate or an inverter has a fan-in of one. Generally, delay of operation of any gate increases with increasing fan-in quadratically. Gate delay is the delay offered by a gate for the signal applied at input terminals, before it reaches the gate output. Gate delay is also known as propagation delay.

Fan-Out Fan out is defined as the number of similar logic gates driven by a single logic gate. While a logic gate has high fan out, it is advantageous to design integrated chips, as less number of driving circuits are required. The fan-out depends on the amount of source or sink current of a gate while the gate drives other gates. When a logic gate output has more than its rated fan-out, the logic gate has the following effects:

- The operating temperature of the device will be increased. Hence, reliability of the device will be reduced and eventually the device may fail.
- Propagation delay will be increased and it may be above the specified value.
- The output rise and fall times may be increased beyond specification.
- In the low state, the output voltage V_{OL} may increase above maximum value of V_{OL}.
- In the high state, the output voltage V_{OH} may decrease below the minimum value of V_{OH}.

The factors that limit the fan-out of a gate are the output current capacity as specified by the parameters I_{OH} and I_{OL}, and the input current requirements of the driven gates as specified by their parameters I_{IH} and I_{IL}. Certainly, the sum of the currents I_{IH} for all the gates driven by a gate must be less than the current I_{OH} of the driving gate. In the same way, the sum of the I_{IL} current parameters must be less than I_{OL} for these gates. When all of the gates have the same current parameter values then the fan-out due to current considerations can be expressed by a constant integer which is the maximum number of gate inputs that can be connected to a single gate output. The fan-out can be defined as the largest integer less than or equal to minimum of (I_{OH}/I_{IH}, I_{OL}/I_{IL}), where I_{OH}/I_{IH} is the number of gates that can be driven by a single gate when output signal is high, and I_{OL}/I_{IL} is the maximum number if the output signal is low. Figure 6.38 shows a TTL AND gate drives '*N*' numbers of similar AND gates for high level output and low level output. Here, *N* is the fan out of the gate and it can be determined from current driving capability of output and the current requirement of input. If maximum current driving capability I_{OH} and maximum current requirement of each input I_{IH} are known, the fan out of the gate will be

$$N = \frac{I_{OH}}{I_{IH}}$$

For example, consider I_{OH} is equal to 50 μA and I_{IH} is 25 μA. The fan out is

$$N = \frac{I_{OH}}{I_{IH}} = \frac{500}{25} = 20$$

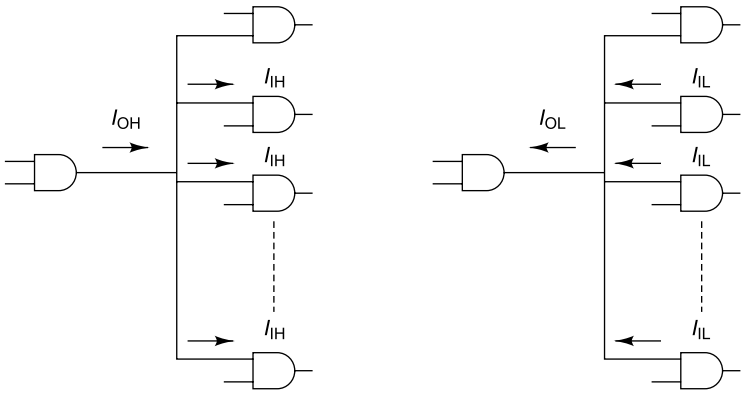


Fig. 6.38 ***(a) Fan-out computation for high-level output***
(b) Fan-out computation for low-level output

Cost The cost of a digital IC depends on the quantity manufactured. The designer always tries to design low-cost ICs though the quantity of ICs used is large.

Availability To choose a logic family for particular applications, availability is an important parameter. Availability can be considered in two different ways as given below:

Popularity of the Logic Family The popularity of a particular logic family depends upon the users and digital circuit designers. If application of a logic family is more, a large number of ICs of that logic family will be manufactured. Therefore, the cost per IC will be very small and easily available in the market.

Breadth of the Logic Family The breadth of the logic family means the number of different logic functions, ICs available. The complex functions would have to be constructed using basic ICs. For example, the TTL logic family has very good popularity and high breadth over other logic families.

Wired Logic Capability Due to wired-logic capability, the outputs may be connected jointly to achieve extra logic without additional hardware. Various flexibilities are available in different IC logic families and these must be considered while selecting a logic family.

Availability of Complement Outputs If the complement of outputs is available in ICs, the additional inverter is not required to invert the output.

6.26 Calculate the fan-out of a AND gate which drives AND gates.

Assume I_{OH} = 0.8mA, I_{OL} = 20 mA, I_{IH} = 0.02 mA, and I_{IL} = 0.6 mA.

Solution

Fan out at high-level output , $N = \dfrac{I_{OH}}{I_{IH}} = \dfrac{0.8}{0.02} = 40$

Fan out at low-level output, $N = \dfrac{I_{OL}}{I_{IL}} = \dfrac{20}{0.6} = 33.33 = 33$ (approx.)

The fan-out of the gate is minimum of $\left(\dfrac{I_{OH}}{I_{IH}}, \dfrac{I_{OL}}{I_{IL}}\right)$ = minimum of (40, 33) = 33

6.10.3 Direct-Coupled Transistor Logic (DCTL)

Figure 6.39 shows the Direct Coupled Transistor Logic (DCTL) for a three-input NOR gate. The input voltage is applied to the base of transistors and the output is taken from the collector of transistor. When logic 1 or $+V_{CC}$ is input to A, B, and C, transistors saturate and the output voltage drops to its saturation voltage or 0 V. The operations of DCTL is highly affected due to change in slight differences in characteristics of transistors. If the base emitter resistance of one transistor is slightly less than other transistors then the transistor draws most of the current and proper operation of DCTL circuit will be disturbed. This phenomenon is called *current hogging*. This current hogging can be reduced if resistances are connected in series with the base of the transistor and then the base current is less dependent on base emitter characteristics. Then the circuit is called Resistor Transistor Logic (RTL).

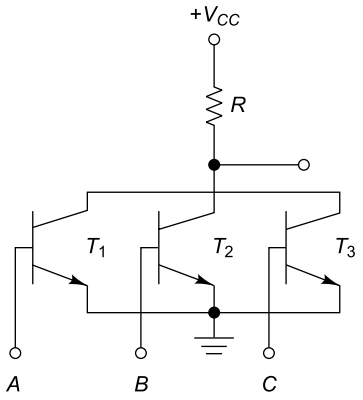


Fig. 6.39 ***Direct-coupled Transistor Logic (DCTL)***

6.10.4 Resistor Transistor Logic (RTL)

A Resistor Transistor Logic (RTL) circuit of a three-input NOR gate is shown in Fig. 6.40. In this circuit, resistance is connected in series with the base of each transistor to reduce the hogging current effect. Actually, the input capacitance has been charged and discharged through this additional resistance and time constant will be increased. Therefore, the switching speed becomes slower. The fan-out of RTL is four or five and time delay is approximately 50 ns.

If inputs A, B and C are LOW, transistors T_1, T_2 and T_3 are cut-off and the

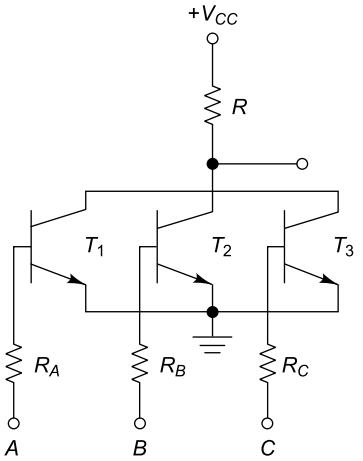


Fig. 6.40 ***Resistor Transistor Logic (RTL)***

output is HIGH or $+V_{CC}$. When any one of the inputs A, B and C is HIGH, the corresponding transistor operates in saturation and the output will be LOW or 0.2 V approximately. Thus NOR logic is satisfied.

6.10.5 Diode Transistor Logic (DTL)

The Diode Transistor Logic (DTL) circuit is most commonly used in the logic family. Figure 6.41 shows a DTL logic circuit. This circuit is actually a NAND gate. To perform logical operation inputs are given at the terminals A, B, and C of the diodes D_1, D_2 and D_3 respectively. Then the signal is coupled with a diode D and an inverter, which consists of a transistor and a load resistance.

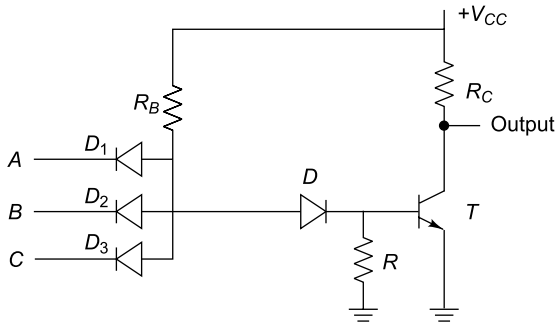


Fig. 6.41 ***Diode Transistor Logic (DTL)***

When all inputs are logical 1 or $+V_{CC}$, diodes D_1, D_2, D_3 are reversed biased and no current passes through diodes. The diode D is forward biased and current will flow through Resistance R, Diode D and base of the transistor T. Then transistor T operates at saturation. The output voltage of the transistor is logic 0. As the signal passes through the forward bias diodes to transistors, the switching speed of DTL is faster than RTL. Fan out is also increased due to high input impedance. The switching delay is approximately 25 ns and fan-out is 8. Therefore, DTL integrated circuits are economical.

6.10.6 Transistor–Transistor Logic (TTL)

In Transistor Transistor logic (TTL), logic gates are built only around transistors. TTL was developed in 1965. All TTL families are available in Small Scale Integration (SSI) packages and in more complex forms as MSI and LSI packages. The differences in the TTL series are not in the digital functions that they perform but rather in the values of resistances and different type transistors which are used to develop basic gates. There are many versions or families of TTL such as Standard TTL, High Speed TTL, Low Power TTL and Schhottky TTL. TTL gates in all the versions come in three different types of output configuration such as

- Totem pole output configuration
- Open collector output configuration
- Tristate or three states output configuration

TTL circuit is most popular in bipolar logic family as it is the fastest saturating logic family. Figure 6.42 shows the basic TTL circuit for a two-input NAND gate. A single multi-emitter transistor replaces input diodes and the series diode of DTL. Each emitter-base diode serves as one input, and the base-collector diode functions as the series diode. The multi-emitter transistor, is economically fabricated in monolithic form. In a multi-emitter transistor, a single isolated collector region is

diffused, a single base region is diffused and formed in the collector region, and the several emitter regions are diffused as separate areas into the base region.

An output stage using an active pull-up transistor is added to the basic logic circuit to give current-gain drive for switching in both directions. This output configuration results in faster switching speed and higher fan-out capability. The TTL circuit is adaptable to virtually all forms of IC logic and produces the highest performance-to-cost ratio of all logic types. TTL circuits for all gates have been discussed later in detail.

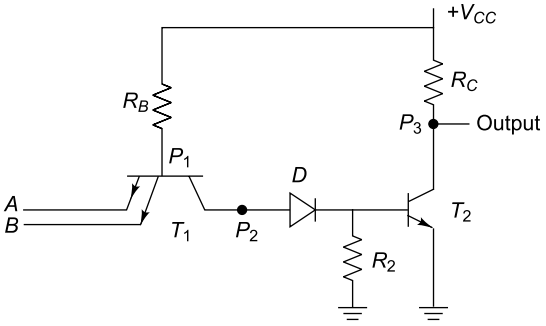


Fig. 6.42 ***Transistor-Transistor Logic (TTL)***

The different series of TTL circuits are presently available. All these circuits are based on the same basic circuit, but some of their properties have been optimized based on special applications. These devices in the standard TTL series are designated with a number prefixed by a 74. For example, 7400 stands for a NAND gate, and 7404 stands for an inverter, etc. If the resistor values in the TTL circuit are increased, its average power dissipation can be reduced. On the other hand, propagation delay will be increased. This low power TTL series are designated as 74LXX (74L00, 74L04, etc.) and the typical power dissipation range is 1 mW to 10 mW for any standard gate. Typical propagation delays are 33 ns for 74L circuits as compared to 9 ns for 74 series circuits. The high speed TTL series are designated as 74HXX (74H00, 74H04, etc.). The typical power dissipation of a 74H00 NAND gate is 22.5 mW, but its propagation delay is about 6 ns.

6.10.7 Emitter-Coupled Logic (ECL)

The emitter-coupled logic circuit is shown in Fig. 6.43. The emitters of transistors T_1 and T_3 are coupled with the emitter of a reference transistor T_2. The common-emitter resistor of transistors T_1, T_2, and T_3 is very high so that it behaves as a constant-current source. Figure 6.43 depicts a constant current source in place of the common-emitter resistor of transistors T_1, T_2, and T_3. A reference voltage V_R is connected to the base of transistor T_2.

When the inputs A and B are logical '0' or ground potential, T_1 and T_3 are in cut-off. Current will not flow through R_C, and the output Y_1 will be logical high, $+V_{CC}$.

If one of the inputs or both inputs are logical '1' and greater than the reference voltage V_R, transistor T_1 or T_3 or both transistors conduct. As current flows through the corresponding transistors, R_C, the collector potential, becomes low. Then output Y_1 is logical '0'.

When current through the transistors T_1 or T_3 increases, current through the reference transistor T_2 decreases. The threshold voltage of T_1 or T_3 is equal to the reference voltage V_R. As emitter coupling is present in the circuit, it does not allow transistors

to operate in saturation. Therefore, the switching speed of ECL is very fast and it is approximately few nanoseconds. Power dissipation of ECL is comparatively high and its value is about 50 mW. As output impedance of ECL circuit is very low, fan-out of this logic family is very high, approximately 25.

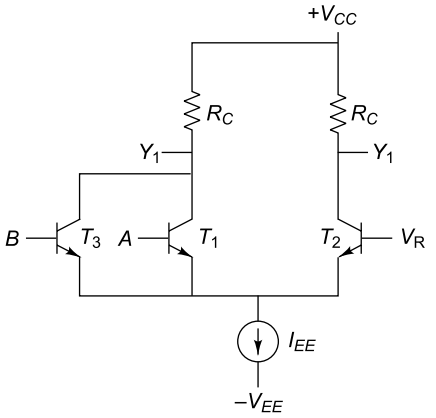


Fig. 6.43 ***Emitter-coupled Logic (ECL)***

The standard digital circuits of DCTL, RTL, DTL, TTL and ECL are explained above. The designer chooses a particular logic family for a specific application after reading all performance parameters of each logic family from their data sheet. Table 6.30 shows the comparison between RTL, DTL, TTL and ECL logic families based on power dissipation, propagation delay and fan-out.

Table 6.30 *Comparison of logic family*

Logic family	*Power dissipation*	*Propagation delay*	*Fan out*
RTL	24 mW	50 ns	5
DTL	10 mW	30 ns	8
TTL	10 mW	10 ns	10
ECL	40 mW	2 ns	High

6.10.8 Schottky TTL

The Schottky TTL is an unsaturated logic family and this TTL series is actually known in the name of Schottky diode inverter. In a Schottky TTL circuit, transistors are prevented from saturation by using Schottky transistors. These transistors are obtained when a Schottky diode is connected between the base and the collector of a normal transistor as shown in Fig. 6.44(a). Figure 6.44(b) shows the symbol of Schottky transistors. Schottky diodes have different characteristic from normal *p-n* junction diodes and these diodes have very low saturation voltage of the order of 0.4 V. In case of normal *p-n* junction diodes, the saturation voltage is about 0.6 V. In TTL logic family transistors operate in saturation. When a silicon transistor operates in saturation, the base to emitter voltage (V_{BE}) is about 0.7 V and the collector to emitter voltage (V_{CE}) is about 0.1 V. If a Schottky diode is connected with a normal transistor, the collector to emitter voltage (V_{CE}) voltage will be more than 0.4 V but less than the base to emitter voltage (V_{BE}). Consequently, the Schottky diode holds the collector to a voltage, which prevents the transistor to operate in fully saturation.

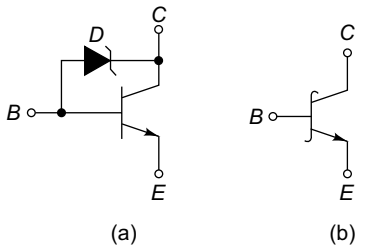


Fig. 6.44 ***Schottky transistor***

So, the diffusion capacitance and propagation delay are reduced. Therefore, Schottky transistors can operate at very high switching speeds and perform consistently up to about 100 MHz. A Schottky TTL NAND is shown in Fig. 6.45. Transistors T_2 to T_6 are Schottky transistors and diodes D_1 to D_5 are Schottky diodes in Fig. 6.45. All resistances R_1 to R_6 are high value compared to TTL logic family. Four different types Schottky TTL, namely, Schottky TTL, low power Schottky TTL, advanced Schottky TTL and advanced low-power Schottky TTL are available.

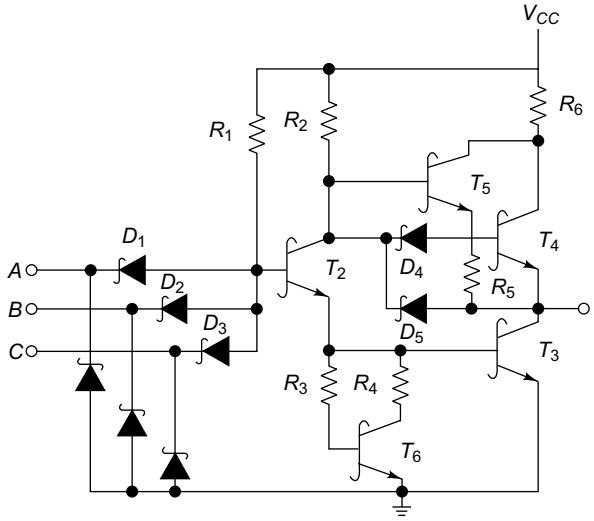


Fig. 6.45 ***Schottky TTL NAND gate***

6.27 Determine the fan out of the DTL circuit as shown in Fig. 6.46.

Assume $V_{CC} = 5$ V, $R = 10$ kΩ, $R_1 = R_2 = \ldots R_N = 20$ kΩ, $V_{CE(sat)} = 0.25$ V, $V_D = 0.7$ V and $I_C = 1.8$ mA.

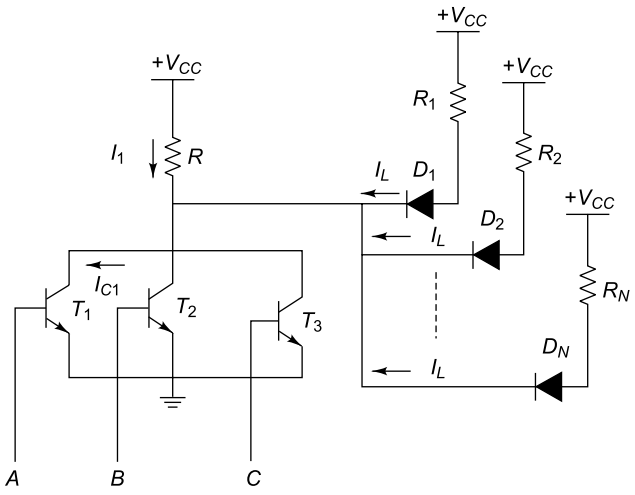


Fig. 6.46 ***Circuit of Ex. 6.27***

Solution

Consider input at terminal A is logic level 1 and other terminals are in logic level 0.
Therefore transistor T_1 operates in saturation.
The current flow through diodes $D_1, D_2 \ldots D_N$ is I_L and it is calculated by

$$I_L = \frac{V_{CC} - V_D - V_{CE(\text{sat})}}{R_1}$$

$$= \frac{5 - .7 - .25}{20} \text{ mA}$$

$$= 0.2025 \text{ mA}$$

The current flow through the resistance R is I_1.

$$I_1 = \frac{V_{CC} - V_{CE(\text{sat})}}{R_1} = \frac{5 - .25}{20} \text{ mA} = 0.475 \text{ mA}$$

The collector current of transistor T_1 is

$$I_{C1} = N I_L + I_1 \qquad \text{where, } N \text{ is the fan-out}$$

So, the fan out $N = \dfrac{I_C - I_1}{I_L} = \dfrac{1.8 - 0.475}{0.2025} = 6.54 = 6$ (approx)

6.28 Determine the voltages at P_1 and P_2 of TTL circuit as shown in Fig. 6.47.
Assume $V_A = 1.1$ V, $V_B = 4.5$ V, $V_D = 0.7$ V, $V_{BE} = 0.7$ V, $V_{CC} = 5$ V, $R_1 = 4.7$ kΩ, $R_2 = 4.7$ kΩ, $R_3 = 2.2$ kΩ

Solution

The input voltages at A, B are $V_A = 1.1$ V, and $V_B = 4.5$ V respectively. As V_A is 1.1 V, emitter base junction of T_1 to input terminal A is in conduction state.
Consequently, the $V_{P1} = V_A + V_{BE} = 1.1 \text{ V} + 0.7 \text{ V} = 1.8 \text{ V}$
The transistor T_2 will be saturate when $V_{P1} = 0.7 + 0.7 + 0.7 = 2.1$ V.
As V_{P1} is 1.8 V, T_2 will be OFF but transistor T_1 conducts to input terminal A.
Therefore $I_{B2} = 0$ and the output voltage is equal to 5 V.
Therefore, $V_{P2} = 5$ V.

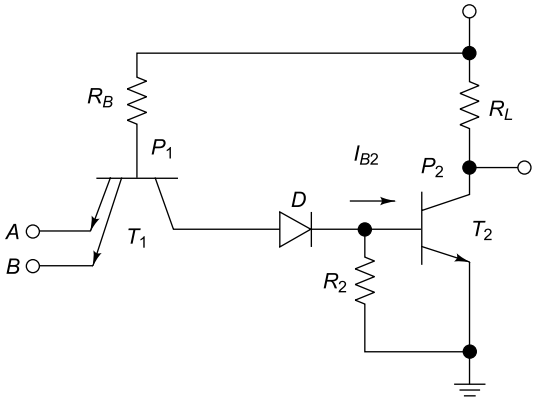


Fig. 6.47 ***Transistor–transistor Logic (TTL) of Ex. 6.28***

6.29 Determine fan-out of transistor T_0 as shown in Fig. 6.48. Consider V_{CC} = 5 V, R = 20 kΩ, I_B = 0.1 mA for saturation.

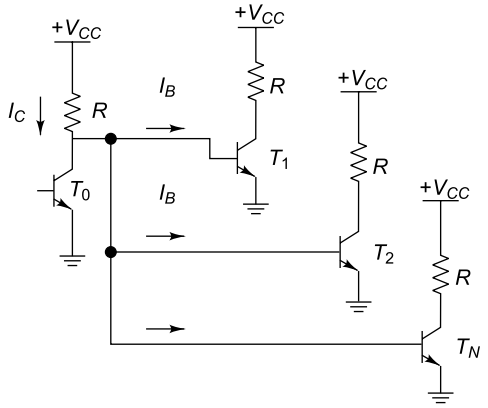


Fig. 6.48 ***Circuit of Ex. 6.29***

Solution

Assume V_{CC} = 5 V, R = 20 kΩ, I_B = 0.1 mA for saturation.

The collector current $I_C = \dfrac{V_{CC} - V_{CE}}{R} = \dfrac{(5 - 0.2)}{20}$ mA = 0.24 mA

The fan-out of transistor T_0 is $N = \dfrac{I_C}{I_B} = \dfrac{0.24}{0.1}$ =2.4

So, N = 2 as fan-out is always an integer.

6.30 Determine I_{B1}, I_{B2}, I_{C1} and I_{C2} for the transistor T_1 and T_2 as depicted in Fig. 6.49. Consider $R_1 = R_2$ = 1.5 kΩ, R = 4.7 kΩ, V_{CC} = 5 V, h_{fe} = 50, and V_{CE} = 0.2 V.

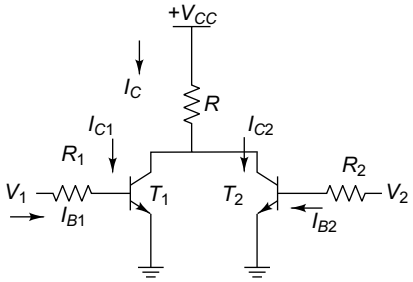


Fig. 6.49 ***Circuit of Ex. 6.30***

Solution

Given $R_1 = R_2$ = 1.5 kΩ, R = 4.7 kΩ, V_{CC} = 5 V, h_{fe} = 50, and V_{CE} = 0.2 V.

The current I_{C1} and I_{C2} are

$$I_{C1} = I_{C2} = \frac{V_{CC} - V_{CE}}{R} = \frac{5 - 0.2}{4.7} \text{ mA} = 1.021 \text{ mA}$$

The current I_{B1} and I_{B2} are

$$I_{B1} = I_{B2} = \frac{V_{CC} - V_{CE}}{R_1} = \frac{5 - 0.8}{1.5} \text{ mA} = 2.8 \text{ mA}$$

6.31 Determine the current through diode D_1 as shown in Fig. 6.50. Consider $R_B = R_C = 1.5$ kΩ, $R = 4.7$ kΩ, $V_1 = 0.2$V and $V_{D1} = 0.7$ V.

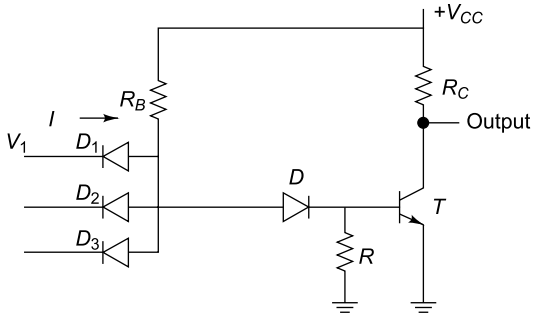


Fig. 6.50 ***Circuit of Ex. 6.31***

Solution

Given $R_B = R_C = 1.5$ kΩ, $R = 4.7$ kΩ $V_1 = 0.2$ V and $V_{D1} = 0.7$ V.

The current flow through diode D_1 is

$$I = \frac{V_{CC} - (V_1 + V_D)}{R_B} = \frac{5 - (0.2 + 0.7)}{1.5} \text{ mA} = 2.74\text{mA}$$

6.32 Determine the current through R_B, R, R_C and base of the transistor as shown in Fig. 6.51.

Assume $V_{CC} = 5$ V, V_{BE} (sat) = 0.7 V, V_{CE}(sat) = 0.2 V, $R_B = R_C = 2.5$ kΩ, $R = 4.7$ kΩ, $V_1 = 3$ V and $V_B = -2$ V.

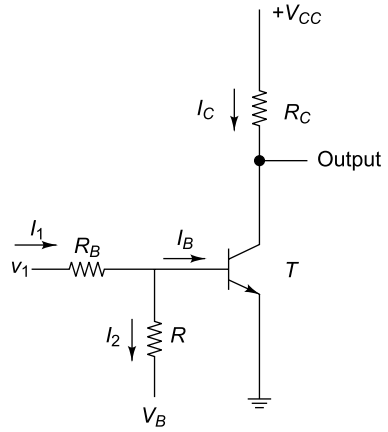


Fig. 6.51 ***Circuit of Ex. 6.32***

Solution

The current through R_B is $I_1 = \dfrac{V_1 - V_{BE}}{R_B} = \dfrac{3 - 0.7}{2.5}$ mA = 0.92 mA

The current through R is $I_2 = \dfrac{V_{BE} + V_B}{R} = \dfrac{0.7 + 2}{4.7}$ mA = 0.574 mA

The base current of transistor T is $I_B = I_1 - I_2 = (0.92–0.574)$ mA = 0.346 mA

The current through R_C is $I_C = \dfrac{V_{CC} - V_{CE}}{R_C} = \dfrac{5 - 0.2}{2.5}$ mA = 1.92 mA

EXERCISES

1. Convert the following binary numbers to decimal numbers.
   (a) 1110011 (b) 101010101
2. Convert the following decimal numbers to binary numbers.
   (a) 29 (b) 365 (c) 129.625
3. Convert the following binary numbers to octal, and hexadecimal numbers.
   (a) 101111010 (b) 1101101
4. Convert the following octal numbers to binary numbers.
   (a) 25 (b) 267
5. Convert the following hexadecimal numbers to binary numbers.
   (a) FF (b) BCD (c) 245
6. Convert the following decimal numbers to octal and hexadecimal numbers.
   (a) 46 (b) 274 (c) 645
7. Add the following binary numbers.
   (a) 10110 (b) 1111
   10100 1010
8. Convert the following decimal numbers to BCD.
   (a) 456 (b) 999 (c) 267
9. Convert the following BCD numbers into decimal numbers.
   (a) 0011 0101 1001 (b) 1000 0101 0110 1001
10. Write the truth table of the logic circuit as given below:

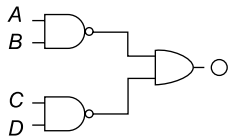


Fig. 6.52

11. Derive the logic expression of the logic circuit as given below and also write the truth table.

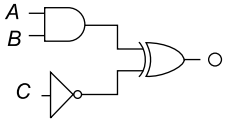


Fig. 6.53

12. Draw the output of the two input AND gate with the given inputs A and B.

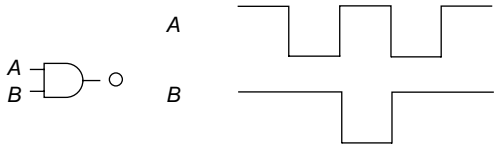


Fig. 6.54

13. Prove the following identities of Boolean algebra:
    (a) $A + A = A$ (b) $A.\ \overline{A} = 0$
14. Prove the commutative law
    (a) $A + B = B + A$ (b) $AB = BA$
15. Prove the distributive law
    (a) $A + (BC) = (A + B)(A + C)$ (b) $A(B + C) = (AB) + (AC)$
16. Simplify the following logic expressions using De *Morgan's theorem*.
    (a) $O = \overline{(AB + \overline{CD})}$ (b) $O = \overline{(A + B + CD)}$
17. What are the types of digital logic circuits? Explain briefly any one logic circuit.
18. Draw the circuit diagram of DCTL to perform logical AND and explain briefly the operation of circuit.
19. Determine the rise time of a RTL circuit as depicted in Fig. 6.55. Assume $R_1 = 450$ ohms, $R = 640$ ohms, $C = 5$ pF, $N = 10$

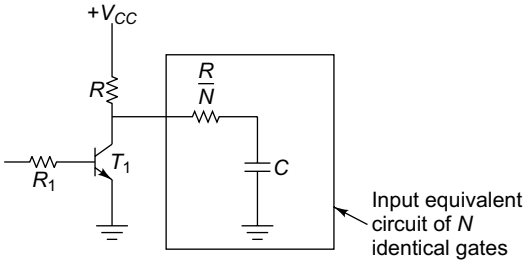


Fig. 6.55

20. Write the truth table of the DTL circuit as depicted in Fig. 6.56.

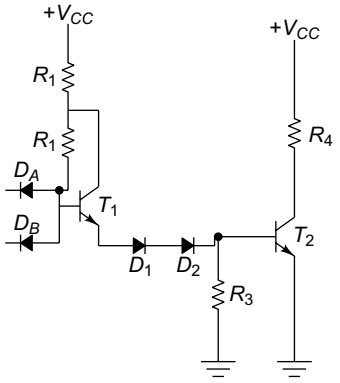


Fig. 6.56

21. Determine the voltage V_1 in a NAND gate for the following conditions
    (i) T_2 begins to come out of cutoff
    (ii) T_2 operates at the edge of saturation
    Consider $R_1 = 3\ k\Omega$, $R_2 = 10\ k\Omega$, $R_3 = 5\ k\Omega$, $R_4 = 10\ k\Omega$, $V_Z = 6.8$ V, $V_{CC} = 12$ V. Assume all necessary parameters.

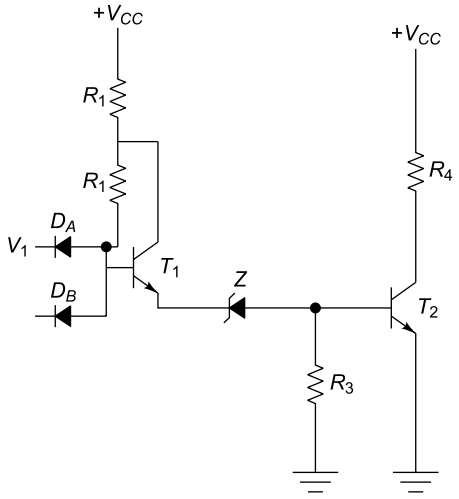


Fig. 6.57 *NAND Gate*

22. Define propagation delay, noise margin and fan-out. of digital logic circuits.

MULTIPLE CHOICE QUESTIONS

1. The binary equivalent of the decimal number 15 is
   (a) 1001 (b) 1111 (c) 1010 (d) 1101
2. The decimal equivalent of 111.101 is
   (a) 7.29 (b) 7.625 (c) 73 (d) 5.625
3. The decimal equivalent of the hexadecimal number FB is
   (a) 229 (b) 151 (c) 251 (d) 351
4. $(1111.01)_2$ is
   (a) $(15.25)_{10}$ (b) $(12.25)_{10}$ (c) $(23)_{10}$ (d) $(12)_{10}$
5. In the BCD form, the decimal number 621 is written as
   (a) 1100 0010 0001 (b) 1000111
   (c) 1100 0010 (d) 0010 0001
6. Indicate which of the following binary additions is correct.
   (a) 10101 + 1111= 111101 (b) 1010 + 1101 = 10111
   (c) 1010 + 1110 = 11001 (d) 1010 + 1001 = 1111
7. The decimal number 576 is equal to which of the following hexadecimal numbers?
   (a) 229 (b) 279 (c) 240 (d) 245

8. The binary number 111011 is equivalent to
   (a) 59 (b) 56 (c) 69 (d) 79
9. Convert $(234)_8$ into base 2
   (a) 011100111 (b) 11100111 (c) 11101011 (d) 10011100
10. Which of the following range is used as low-level (logic 0) input voltage in TTL circuit?
    (a) 0.4 V – 1.2 V (b) 0 V– 0.8 V (c) 0.8 V–2.4 V (d) 1 V–2.4 V
11. Which of the following range is used as high-level (logic 1) input voltage in TTL circuit?
    (a) 2 V – 5 V (b) 0.8 V– 5 V (c) 0.8 V–2.4 V (d) 1 V–5 V
12. Which of the following logic family is the fastest of all?
    (a) TTL (b) RTL (c) DCTL (d) ECL
13. Which of the following logic families is most widely used?
    (a) TTL (b) DTL (c) ECL (d) None of these
14. What is the fan-out of TTL devices?
    (a) 2 (b) 4 (c) 6 (d) 10
15. What are the three basic parameters for selecting a digital logic family?
    (a) Speed, cost, power consumption (b) Speed, size, power consumption
    (c) Speed, size, propagation delay
16. In a positive logic circuit
    (a) Logic 0 and 1 represented by 0 V (ground) and positive voltage($+V_{CC}$) respectively
    (b) Logic 0 and 1 represented by negative and positive voltages respectively
    (c) Logic 0 voltage level is higher than logic 1 voltage level
    (d) Logic 0 voltage level is lower than logic 1 voltage level
17. A NAND gate is called a universal logic element because
    (a) all digital computers use NAND gates
    (b) all the minimization techniques are applicable for optimum NAND gate realization
    (c) everybody use this gates
    (d) any logic function can be realized by NAND gates alone
18. If an input signal A=10101 is applied to a NOT gate, its output signal is
    (a) 01010 (b) 01001 (c) 00011 (d) 1000
19. A 3-input logic gate has its three inputs: $A = 1$, $B = 0$ and $C = 1$. If its output $O = 1$, the gate is
    (a) NOR (b) NAND (c) AND (d) OR
20. The following equation corresponds to De Morgan's theorem in Boolean algebra:
    (a) $(A + B)(A + B) = A + AB + B$
    (b) $(A + B)(A + B) = AA + AB + BB + BA$
    (c) $\overline{AB} = \overline{A} + \overline{B}$
    (d) None of these
21. A 2-input logic gate has its inputs $A = 0$, and $B = 1$. If its output $O = 1$, the gate would be
    (a) NOT (b) OR (c) AND (d) NOR

22. Boolean algebra is based on the premise that
    (a) differential equations can be solved by analog circuits
    (b) there are two states
    (c) data can be stored and retrieved
    (d) none of these
23. What are the values of the inputs for a NAND gate if output is 1?
    (a) $A = 0, B = 0$
    (b) $A = 1, B = 0$
    (c) $A = 0, B = 1$
    (d) $A = 1, B = 1$
24. Which function is implemented by the circuit as shown in Fig. 6.58?

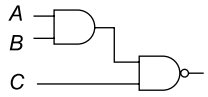


Fig. 6.58

    (a) $O = \overline{ABC}$ (b) $O = \overline{A+B+C}$
    (c) $O = \overline{AB+C}$ (d) None of these
25. Boolean algebra is different from ordinary algebra in which way?
    (a) Boolean algebra can represent more than 1 discrete level between 0 and 1.
    (b) Boolean algebra have only 2 discrete levels: 0 and 1.
    (c) Boolean algebra can describe up to levels of logic levels.
    (d) They are actually the same.

ANSWERS TO MCQ

1 (b)	2 (b)	3 (c)	4 (a)	5 (a)	6 (b)	7 (c)
8 (a)	9 (d)	10 (b)	11 (a)	12 (d)	13 (a)	14 (d)
15 (a)	16 (a)	17 (d)	18 (a)	19 (b)	20 (c)	21 (b)
22 (b)	23 (a)	24 (a)	25 (b)			

SOLVED WBUT QUESTION PAPER (2012)

GROUP – A

(Multiple Choice-Type Questions)

1. Choose the correct alternatives for any five of the following: $5 \times 1 = 5$

(i) An ideal Op-Amp is an ideal
- (a) voltage controlled current source
- (b) voltage controlled voltage source
- (c) current controlled current source
- (d) current controlled voltage source

Ans: (b) voltage controlled voltage source

(ii) The AND function can be realized by using only n number of NOR gates. What is n equal to
- (a) 2 (b) 3 (c) 4 (d) 5

Ans: (b) 3

(iii) The Boolean expression $ABC + \bar{A}\bar{B}C + AB\bar{C} + \bar{A}\bar{B}\bar{C}$ is of
- (a) OR gate (b) AND gate
- (c) Ex-NOR gate (d) Ex-OR gate

Ans: (c) Ex-NOR gate

(iv) Which of the following statements is/are correct in regard to excess 3 code?
- (a) It is a BCD code
- (b) It is an unweighted code
- (c) It is a self complementing code
- (d) All of these

Ans: (d) All of these

(v) In Barkhausen criterion, phase of $A\beta$ is

(a) 0° (b) multiple of 180°

(c) 0° or multiple of 180° (d) 0° or multiple of 360°

Ans: (d) 0° or multiple of 360°

(vi) In inverting amplifier circuit if input and feedback resistances are 1 kΩ and 3 kΩ respectively, *i/p* voltage is 3 Volt and power supply voltage is ± 6 V, then the output voltage of OP-Amp is

(a) – 6 Volt (b) + 6 Volt

(c) – 9 Volt (d) + 9 Volt

Ans: (a) – 6 Volt

GROUP – B

Answer any two of the following $2 \times 5 = 10$

2. Mention the advantages and disadvantages of negative feedback amplifier.

Solution: Refer to Solution of Question No. 18 (a) of University Questions with answers of Chapter 2.

3. Discuss the operation of OP-AMP as an integrator

Solution: Refer to Section 5.11.

4. (a) Implement the function $F = (\overline{AB + CD})$ using NAND gates

Solution:

$$F = (\overline{AB + CD})$$

$$= \overline{AB} \cdot \overline{CD}$$

$$= \overline{\overline{AB}} \cdot \overline{\overline{CD}}$$

The implementation of the function $F = (\overline{AB + CD})$ using NAND gates is shown in Fig. 1.

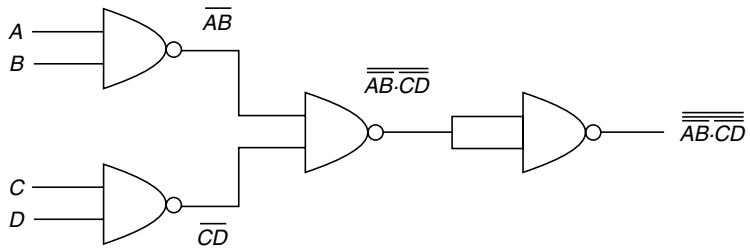


Fig. 1

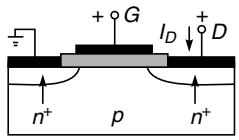
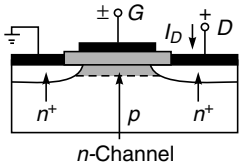
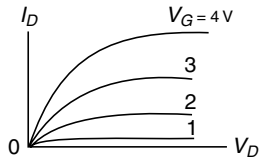
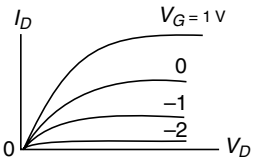
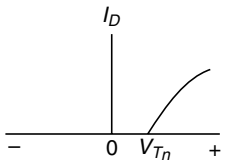
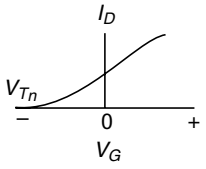
(b) $(11011)_2 = (?)_{10}$

Solution:

$$(11011)_2 = 2^4 \times 1 + 2^3 \times 1 + 2^2 \times 0 + 2^1 \times 1 + 2^0 \times 1$$
$$= 16 + 8 + 2 + 1 = (27)_{10}$$

(c) Write down the basic difference between enhancement type and depletion type MOSFETs.

Solution: The difference between enhancement type and depletion type MOSFETs are given below:

Enhancement type MOSFETs	**Depletion type MOSFETs**
n-channel and *p*-channel enhancement type MOSTFETs are normally OFF	*n*-channel and *p*-channel depletion type MOSTFETs are normally ON
The cross-section view of *n*-channel enhancement type MOSFET is 	The cross-section view of *n*-channel depletion type MOSFET is 
The *Drain or output characteristics* of *n*-channel enhancement type MOSFET is 	The *Drain or output characteristics* of *n*-channel depletion type MOSFET is 
The *transfer characteristics* of *n*-channel enhancement type MOSFET is 	The *transfer characteristics* of *n*-channel depletion type MOSFET is 

5. (a) What is virtual ground of an Op-Amp?

Solution: Refer to Section 4.11

(b) Draw and explain the voltage comparator circuit using Op-Amp.

Solution: Refer to Section 5.18.

GROUP – C

Answer any two of the following $2 \times 10 = 20$

6. (a) What is the effect of negative feedback on output impedance and phase distortion?

Solution:

For the effect of negative feedback on output impedance, refer to Section 2.6.2.

For the effect of negative feedback on phase distortion, refer to Section 2.7.5.

(b) An amplifier has a voltage gain of – 100. The feedback ratio is – 0.04. Find

(i) the voltage gain with feedback

(ii) The amount of feedback in dB

(iii) The output voltage of the feedback amplifier for an input voltage of 40 mV

(iv) The feedback factor

(v) The feedback voltage

Solution: $A = -100, \beta = -0.04$

(i) the voltage gain with feedback is

$$A_f = \frac{A}{1+\beta A} = \frac{-100}{1+(-0.04)(-100)} = -20$$

(ii) The amount of feedback in dB is

$$20 \log_{10}\left(\frac{A_f}{A}\right) = 20 \log_{10}\left(\frac{-20}{-100}\right)$$

$$= 20 \log_{10}\left(\frac{1}{5}\right) = -20 \log_{10} 5 \text{ dB} = -13.979 \text{ dB}$$

(iii) The output voltage of the feedback amplifier for an input voltage of 40 mV is equal to

$$V_o = A_f V_i = -20 \times 40 \text{ mV} = -800 \text{ mV}$$

(iv) The feedback factor is

$$\frac{1}{1+\beta A} = \frac{1}{1+(-0.04)(-100)} = 0.2$$

(v) The feedback voltage is equal to

$$V_f = \beta V_o = (-0.04) \times (-800)\ \text{mV} = 32\ \text{mV}$$

7. (a) Explain the basic operation of depletion type *n*-channel MOSFET with a suitable diagram.

Solution: Refer to Section 1.15.

(b) What are the basic differences between BJT and FET?

Solution: Refer to Section 1.8.

(c) As V_{GS} is changed from 0 V to 0.2 V keeping V_{DS} constant, I_D of the FET drops from 10.25 mA to 9.65 mA. What is the transconductance of the FET? If the ac drain resistance is 32 kΩ, find also the amplification factor of the FET.

Solution: Transconductance is

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{(10.25 - 9.65) \times 10^{-3}}{0.2} = 3 \times 10^{-3}\ \text{mho}$$

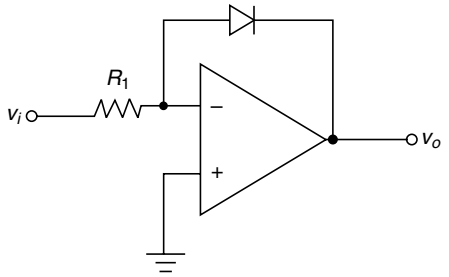
The ac drain resistance r_d is 32 kΩ
Amplification factor of FET is

$$\mu = g_m r_d = 3 \times 10^{-3} \times 32 \times 10^3 = 96$$

(d) What do you mean by pinch off voltage for *n* channel JFET?

Solution: Refer to Section 1.4.

8. (a) If the feedback resistance R_f is replaced by a diode for a negative feedback amplifier using Op-Amp, then derive the expression of o/p voltage v_o for it. Also mention the type of application for this modification.



Solution: The current flows through diode is $I = I_S\left(e^{\frac{qV_D}{KT}} - 1\right)$

where V_D is diode voltage
K_T is the Boltzmann's constant
T is temperature in $°K$
I_S is reverse saturation current

Therefore, $\frac{I}{I_S} + 1 = e^{\frac{qV_D}{KT}}$

Taking log both the sides, we get

$$\log\left(\frac{I}{I_S} + 1\right) = \log\left(e^{\frac{qV_D}{KT}}\right)$$

or, $$\frac{qV_D}{KT} = \log\left(\frac{I}{I_S}\right)$$

or, $$V_D = \left(\frac{KT}{q}\right)\log\left(\frac{I}{I_S}\right)$$

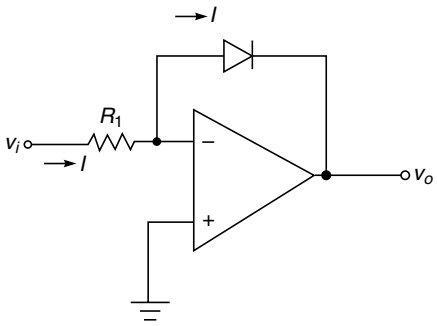


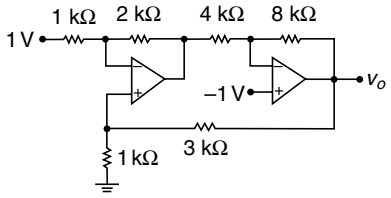
Fig. 1

As current $I = \frac{V_i}{R_1}$, the output voltage V_O is equal V_D and it can be expressed as

$$V_O = V_D = \frac{KT}{q}\log\left(\frac{V_i}{R_1 I_S}\right)$$

This circuit is used in *analog multiplier* and *analog divider.*

(b) For the given circuit find the output voltage v_o

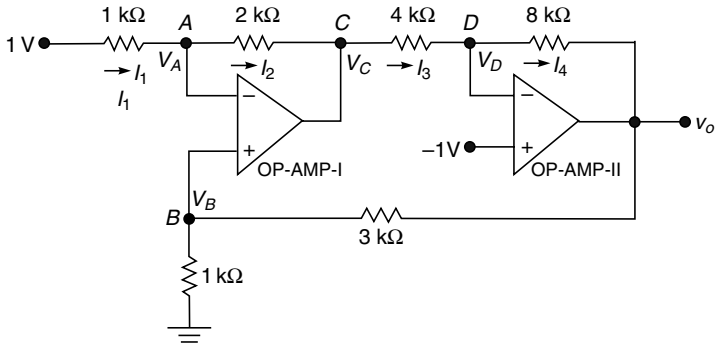


Solution: The potential at point B is equal to

$$V_B = \frac{1\,\text{k}\Omega}{1\,\text{k}\Omega + 3\,\text{k}\Omega} V_o = \frac{V_o}{4}$$

The potential at point A is equal to the potential at point B.

Therefore $V_A = V_B = \frac{V_o}{4}$



In OP-AMP-I, the current I_1 is equal to current I_2

Then $$I_1 = \frac{1 - V_A}{1\,\text{k}\Omega} = I_2 = \frac{V_A - V_C}{2\,\text{k}\Omega}$$

or, $$\frac{1 - \frac{V_o}{4}}{1\,\text{k}\Omega} = \frac{\frac{V_o}{4} - V_C}{2\,\text{k}\Omega}$$

or, $$2 - \frac{V_o}{2} = \frac{V_o}{4} - V_C$$

or, $$V_C = \frac{V_o}{4} + \frac{V_o}{2} - 2 = \frac{3}{4} V_o - 2$$

The potential at point D is $V_D = -1$ V.
In OP-AMP-II, the current I_3 is equal to current I_4

Then $$I_3 = \frac{V_C - V_D}{4\,\text{k}\Omega} = I_4 = \frac{V_D - V_o}{8\,\text{k}\Omega}$$

or, $$\frac{V_C - V_D}{4\,\text{k}\Omega} = \frac{V_D - V_o}{8\,\text{k}\Omega}$$

or, $$\frac{\frac{3}{4} V_o - (-1)}{4\,\text{k}\Omega} = \frac{(-1) - V_o}{8\,\text{k}\Omega}$$

or, $$\frac{3}{2} V_o + 2 = -1 - V_o$$

or, $$\frac{5}{2} V_o = -3$$

Therefore, $$V_o = -1.2 \text{ V}$$

9. Write short notes on any two of the following:

(a) Topologies of feedback amplifier

Solution: Refer to Section 2.5.

(b) Summing amplifier

Solution: Refer to Section 5.5.

(c) CMOS

Solution: Refer to Section 1.20.

(d) Design of Exclusive-OR gate

Solution: The operation of Exclusive-OR gate is quite different from OR gate. When the inputs of Exclusive-OR gate are at different logic levels either '0' and '1' or '1' and '0', its output is "high". On the other hand, output of Exclusive-OR gate is "low" logic level if the inputs are at the same logic levels. The Exclusive-OR gate can be written as XOR or Ex-OR gate. Figure 1 shows the two inputs Ex-OR gate and truth table is given in Table 1.

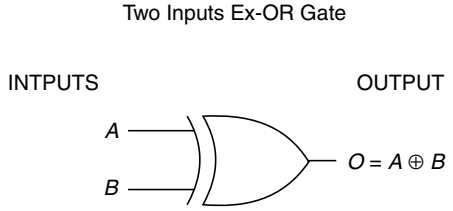


Fig. 1 ***Ex-OR gate***

Table 1 *Truth table of XOR gate*

Inputs		*Output*
A	*B*	$O = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

The output of Ex-OR gate can be expressed as $O = \bar{A}B + A\bar{B}$. The Exclusive-OR gate can be designed by using Universal gates such as NAND gates.

$$
\begin{aligned}
O &= \bar{A}B + A\bar{B} \\
&= \bar{A}B + \bar{B}B + A\bar{B} + \bar{A}A \\
&= B(\bar{A} + \bar{B}) + A(\bar{B} + \bar{A}) \\
&= B \cdot \overline{AB} + A \cdot \overline{AB} \\
&= \overline{AB} \cdot B + \overline{AB} \cdot A \\
&= \overline{\overline{\overline{AB} \cdot B} \cdot \overline{\overline{AB} \cdot A}} \\
O &= \overline{\overline{\overline{AB} \cdot B} \cdot \overline{\overline{AB} \cdot A}}
\end{aligned}
$$

The implementation of X-OR gate using NAND gates is illustrated in Fig. 2.

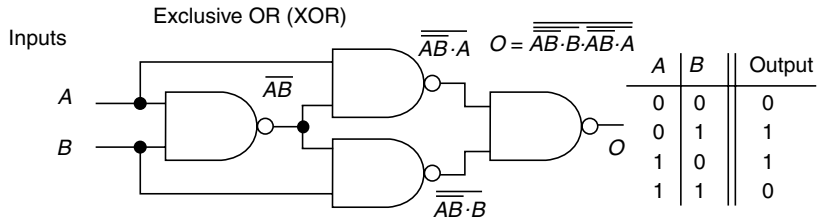


Fig. 2

SOLVED WBUT QUESTION PAPER (2013)

ES-201

GROUP – A

(Multiple-Choice-Type Questions)

1. Choose the correct alternatives for any five of the following: $5 \times 1 = 5$

(i) The threshold voltage of an enhancement PMOS is

(a) negative (b) positive

(c) zero with respect to source (d) zero with respect to drain

Ans: (a) negative

(ii) For a source follower circuit, the voltage gain is

(a) zero (b) slightly lesser than unity

(c) slightly greater than unity (d) none of these

Ans: (c) slightly greater than unity

(iii) The expression of closed-loop gain (A_f) for a positive feedback amplifier is

(a) $\frac{A}{1+A\beta}$ (b) $\frac{A}{1-A\beta}$ (c) $\frac{1}{1+A\beta}$ (d) $\frac{1}{1-A\beta}$

Ans: (b) $\frac{A}{1-A\beta}$

(iv) CMMR of an Op-Amp is the ratio

(a) $\frac{\text{Differential Gain}}{\text{Common Mode Gain}}$ (b) $\frac{\text{Common Mode Gain}}{\text{Differential Gain}}$

(c) $\frac{\text{Slew Rate}}{\text{Common Mode Gain}}$ (d) $\frac{\text{Slew Rate}}{\text{Differential Gain}}$

Ans: (a) $\frac{\text{Differential Gain}}{\text{Common Mode Gain}}$

(v) Conversion of $(444.456)_{10}$ into its octal equivalent is

(a) 673.5136 (b) 674.35136

(c) 674.735 (d) none of these

Ans: (b) 674.35136

(vi) NOR and NAND are called universal logic gates because

(a) they are independent of input voltages starts

(b) any logic function can be realized by these gates

(c) they provide minimization technique

(d) none of these

Ans: (b) any logic function can be realized by these gates

GROUP – B

(Short-Answer-Type Questions)

Answer any two of the following $2 \times 5 = 10$

2. Draw schematically the structure of an *n*-channel JFET and define the terms 'source', 'drain', 'gate' and 'channel'.

Solution: Refer Section 1.13.

(a) Explain the importance of the term 'field effect'.

Solution: In the field-effect transistor (FET), an electric field (voltage) is used to control the shape of the channels of the transistor and, hence, the conductivity of a channel of one type of charge carrier in a semiconductor material is controlled. FETs are unipolar transistors as they involve single-carrier-type operation. FETs can be majority-charge-carrier devices, in which the current is carried predominantly by majority carriers, or minority-charge-carrier devices, in which the current is mainly due to a flow of minority carriers. The device consists of an active channel through which charge carriers, electrons or holes flow from the source to the drain. Source- and drain-terminal conductors are connected to the semiconductor through ohmic contacts. The conductivity of the channel is a function of the potential (voltage) applied across the gate and source terminals. Therefore, field effect by changing voltage can be used to control the conductivity of the channels of the transistor.

3. With the help of a block diagram, explain the working principle of a feedback amplifier.

Solution: Refer Section 2.4.

(a) Derive an expression for the voltage gain with feedback.

Solution: Refer Section 2.5.1.

4. What is an operational amplifier (Op-Amp)?

Solution: Refer Section 4.3.

(a) Mention the properties of an ideal Op-Amp.

Solution: Refer Section 4.2.

(b) What type of feedback is used in an Op-Amp adder?

Solution: In a non-inverting Op-Amp adder, negative feedback is used.

5. (a) Perform the following number conversions:

(i) $(10110.1101)_2 = (?)_{10}$

Solution: $1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4}$

$= 16 + 4 + 2 + 0.5 + 0.25 + 0.0625 = 22.8125$

(ii) $(143.3125)_{10} = (?)_2$

Solution: $1 \times 2^7 + 0 \times 2^6 + 0 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 0 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4}$

$= (10001111.0101)_2$

(b) Realize the following Boolean expression using minimum number of NOR gates.

$$Y = (A + \bar{B})(\bar{A} + B)$$

Solution: $Y = (A + \bar{B})(\bar{A} + B)$

$= A\bar{A} + AB + \bar{B}\bar{A} + \bar{B}B$

$= AB + \bar{B}\bar{A}$

or, $\bar{Y} = \overline{(A+\bar{B})(\bar{A}+B)} = \overline{(A+\bar{B})(\bar{A}+B)}$

$\bar{\bar{Y}} = Y = \overline{(\overline{A+\bar{B}}) + (\overline{\bar{A}+B})}$

The implementation of the Boolean expression $Y = (A + \bar{B})(\bar{A} + B)$ using NOR gates is depicted in Fig. 1.

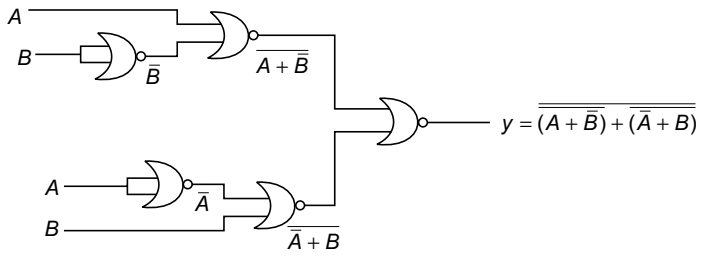


Fig. 1

GROUP – C

(Long-Answer-Type Questions)

Answer any two of the following $2 \times 10 = 20$

6. (a) What are the advantages of FET over BJT?

Solution: Refer Section 1.8 (Table 1.2).

(b) What do you mean by pinch-off voltage?

Solution: Refer Section 1.8 (Page II.1.8 and II.1.9).

(c) As V_{GS} is changed from –1 V to –1.5 V keeping V_{DS} constant, I_D of FET drops from 7 mA to 5 mA. What is the transconductance of the FET? If the ac drain resistance is 200 kΩ, find also the amplification factor of the FET.

Solution: Transconductance is $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}}$ when V_{DS} is constant

$$= \frac{(5-7)\times 10^{-3}}{-1.5-(-1)} = 4 \times 10^{-3} \text{ mho}$$

The ac drain resistance r_d is 200 kΩ
The amplification factor of the FET is

$$\mu = g_m r_d = 4 \times 10^{-3} \times 200 \times 10^3 = 800$$

7. (a) Draw and explain the operation of an Op-Amp integrator circuit.

Solution: Refer Section 5.115.

(b) An inverting amplifier has $R_F = 500$ kΩ, $R_I = 5$ kΩ. Determine the voltage gain, output voltage and input current if the input voltage is 0.1 V.

Solution: In an inverting amplifier, the voltage gain is equal to

$$A_f = -\frac{R_f}{R_I} = -\frac{500\ \text{k}\Omega}{5\ \text{k}\Omega} = -100$$

The output voltage is

$$V_o = -\frac{R_f}{R_I} V_{\text{in}} = -\frac{500\ \text{k}\Omega}{5\ \text{k}\Omega} \times 0.1 = -100 \times 0.1 = -10\ \text{V}$$

The input current $I = \dfrac{V_{\text{in}}}{R_I} = \dfrac{0.1}{5\ \text{k}\Omega} = 0.02\ \text{mA}$

8. (a) Draw the circuit diagram of an emitter follower and explain the nature of feedback in this circuit. What is the feedback topology of the emitter follower?

Solution: Refer Section 2.9.2.

(b) The open-loop gain of an amplifier changes by 20% due to the changes in the parameters of the active amplifier device. If a change of gain by 2% is allowable, what type of feedback has to be applied? If the amplifier gain with feedback is 10, find the minimum value of the feedback ratio and the open-loop gain.

Solution: In a feedback amplifier,

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1+\beta A|}\left|\frac{dA}{A}\right|$$

where, A_f = closed-loop gain, A = open-loop gain and β = feedback ratio.

Here, $\frac{dA_f}{A_f} = 2\% = \frac{2}{100}$ and $\frac{dA}{A} = 20\% = \frac{20}{100}$

$\therefore \quad \frac{2}{100} = \frac{20}{100}\frac{1}{1+\beta A}$

Therefore, $\beta A = 9$

As $\beta A > 1$, the negative feedback has to be applied.

The overall loop gain of a feedback amplifier is

$$A_f = \frac{A}{1+\beta A}$$

If $A_f = 10$, $A_f = \frac{A}{1+\beta A}$ or, $10 = \frac{A}{1+9}$

Therefore, open-loop gain is $A = 100$

The feedback ratio is $\beta = \frac{9}{A} = \frac{9}{100} = 0.09$

11. Write short notes on any two of the following $2 \times 5 = 10$

(a) Enhancement-type MOSFET

Solution: Refer Sections 1.13 and 1.13.2.

(b) Barkhausen criteria

Solution: Refer Section 3.4.1.

(c) CMMR

Solution: Refer Section 4.10.6.

(d) De Morgan's theorem

Solution: Refer Section 6.7.

SOLVED WBUT QUESTION PAPER (2014)

ES-201

.....

GROUP – A

(Multiple-Choice-Type Questions)

1. Choose the correct alternatives for any five of the following: $5 \times 1 = 5$

(i) The decimal equivalent of binary 11.1 is

(a) 3.5 (b) 3.1 (c) 5.1 (d) 2.2

Ans: (a) 3.5

(ii) Open-loop voltage gain of an Op-Amp is

(a) small (b) large (c) can be anything

Ans: (b) large

(iii) Which of the following devices has the highest input impedance?

(a) MOSFET (b) BJT (c) JFET

Ans: (a) MOSFET

(iv) CMMR of an Op-Amp is

(a) much larger than unity

(b) much smaller than unity

(c) unity

(d) none of these

Ans: (a) much larger than unity

(v) Which of the following feedback topologies offers high input impedance?

(a) Voltage series (b) Voltage shunt

(c) Current series (d) Current shunt

Ans: Voltage series

(vi) Oscillators use the following feedback:

(a) Negative (b) Positive

(c) Both negative and positive (d) None

Ans: (b) Positive

GROUP – B

(Short-Answer-Type Questions)

Answer any two of the following: $2 \times 5 = 10$

2. Draw and explain the working principle of the CMOS inverter circuit.

Solution:

CMOS Inverter

Two complementary MOSFETs. namely, *p*-channel MOSFET (PMOS) and *n*-channel MOSFET (NMOS) are connected in such a way that the circuit behaves as inverter. Figure 1 shows the complementary CMOS inverter. The drains are joined together. V_{dd} is connected with source of PMOS and source of NMOS is also connected with ground. Figure 1(a) shows the operation of CMOS inverter when input is connected with low voltage (logic 0). When input voltage is low, the NMOS will be cut-off and PMOS will be operating in saturation mode. Then output will be V_{dd}. Similarly, when input voltage is high, PMOS will be in cut-off and NMOS operate in saturation. Therefore, the output voltage will be almost zero volt. In this way, this circuit behaves as inverter. Table 1 shows the truth table of CMOS inverter.

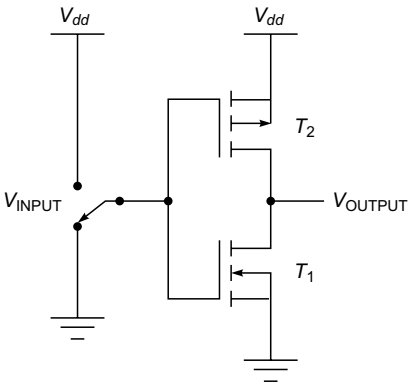


Fig. 1(a) *Complementary CMOS inverter circuit with input ground*

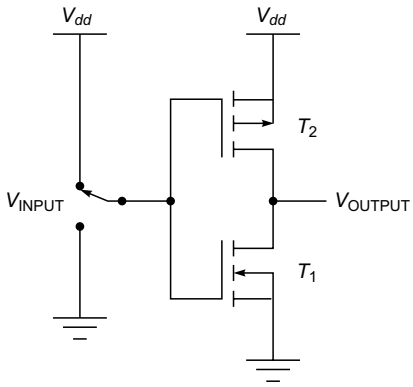


Fig. 1(b) *Complementary CMOS inverter circuit when input connected to* V_{dd}

Table 1 *The truth table of CMOS inverter*

Input	***Transistor***		***Output***
A	T_1	T_2	*O*
Low	Cut-off	Saturation	High
High	Saturation	Cut-off	Low

The transistor T_2 is a *P*-channel MOSFET. When the channel is more positive than the gate, the channel is enhanced and current is allowed between source and drain. Therefore, the upper transistor T_2 is turned on. The transistor T_1, having zero voltage between gate and source, is in its cut-off mode. Thus, the actions of these two transistors are such that the output terminal of the gate circuit has a solid connection to V_{dd} and a very high resistance connection to ground. This makes the output high or logic 1 for the low or logic 0 state of the input.

3. What is positive feedback?

Solution: Refer Section 2.2.2.

(a) Name the different feedback topologies.

Solution: Refer Section 2.5.

4. Identify the circuit and find out the output voltage V_o of the circuit.
If $V_{in} = 5 \sin 2000\pi t$ mV, $R = 100$ kΩ and $C = 1$ μF

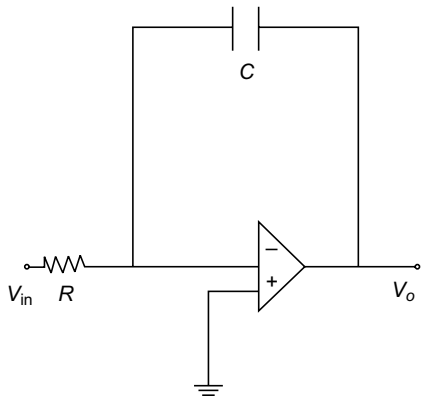


Fig. 2

Solution: Figure 2 shows an integrator circuit.
The output voltage of the integrator is

$$V_o(t) = \frac{1}{RC}\int_0^t V_{in}\,dt$$

$$= -\frac{1}{100 \times 10^3 \times 1 \times 10^{-6}} \int_0^t 5 \sin 2000\,\pi t \cdot dt$$

$$= -50 \int_0^t \sin 2000\,\pi t \cdot dt = -50 \times \frac{1}{2000\,\pi} \times (-\cos 2000\,\pi t)$$

$$= 0.00795 \cos 2000\,\pi t$$

5. (a) Perform the following number conversions:

(i) $(ABC)_{16} = (?)_2$

Solution: $(1010\ \ 1011\ \ 1100)_2$

(ii) $(165)_8 = (?)_2$

Solution: $(001\ \ 110\ \ 101)_2$

(b) Realize the following Boolean expression using minimum number of NAND gates:

$$Y = (A + \bar{B})(\bar{A} + \bar{B})$$

Solution: $Y = (A + \bar{B})(\bar{A} + \bar{B})$

$$= A\bar{A} + A\bar{B} + \bar{B}\bar{A} + \bar{B}\bar{B}$$

$$= A\bar{B} + \bar{B}\bar{A} + \bar{B}$$

or, $\bar{Y} = \overline{(A + \bar{B})(\bar{A} + \bar{B})}$

$$= \overline{(A + \bar{B}) + (\bar{A} + \bar{B})}$$

$$= \bar{A}B + AB$$

or, $Y = \bar{\bar{Y}} = \overline{\bar{A}B + AB}$

The implementation of the Boolean expression $Y = (A + \bar{B})(\bar{A} + \bar{B})$ using NAND gates is depicted in Fig. 3.

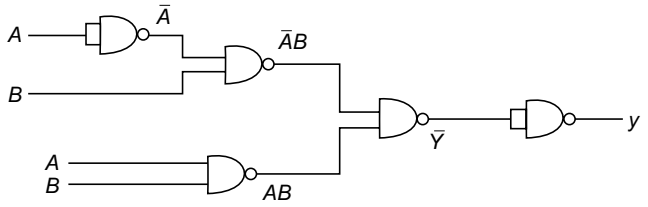


Fig. 3

GROUP – C

(Long-Answer-Type Questions)

Answer any two of the following $2 \times 10 = 20$

6. (a) In a JFET for an applied voltage, $V_{GS} = 0$ V and $V_{DS} = 2.5$ V. The drain current appears to be 13.5 mA. What is the value of I_{DSS} here? If V_{DS} is increased to 3 V and the pinch-off voltage is stated as –2 V. What is the value of I_D?

Solution: Given $I_D = 13.5$ mA, $V_{GS} = 0$ V and $V_{DS} = 2.5$ V.

The drain current $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

Therefore, $13.5 \times 10^{-3} = I_{DSS}\left(1 - \frac{0}{V_P}\right)^2$

The value of I_{DSS} is 13.5 mA.

We know that $V_{DS} = V_{GS} - V_P$

So, $V_{GS} = V_{DS} + V_P = 3 - 2 = 1$ V

The drain current $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 13.5\left(1 - \frac{1}{-2}\right)^2 = 30.375$ mA

(b) What is known as gain-bandwidth product of an amplifier?

Solution: Refer Section 2.7.3.

7. State the Barkhausen criteria.

Solution: Refer Section 3.4.1.

8. (a) What is an integrator and a differentiator? Describe them with suitable block diagrams.

Solution: Refer Sections 5.11 and 5.12.

(b) The midrange open-loop gain of a certain Op-Amp is 120 dB. Negative feedback reduces this gain by 50 dB. What is the closed-loop gain?

Solution: The closed-loop gain is equal to $A_{cl} = 120$ dB – 50 dB = 70 dB

9. (a) Define the truth table of the XOR gate.

Solution: Refer Section 6.8.6.

10. (a) Implement the XOR operation using the minimum number of two-input NAND gates.

Solution: Refer Answer of 9(d) from QP of 2012.

(b) In an adder, 3 input resistances are 2 kΩ, 4 kΩ and 8 kΩ, and the feedback resistance is 10 kΩ. What is the output voltage of the Op-Amp?

Solution: The output voltage of the adder circuit using the Op-Amp is equal to

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_1}V_2 + \frac{R_f}{R_3}V_3\right)$$

where, $R_1 = 2\ \text{k}\Omega$, $R_2 = 4\ \text{k}\Omega$ and $R_3 = 8\ \text{k}\Omega$ and the feedback resistance $R_f = 10\ \text{k}\Omega$.

Input voltages are V_1, V_2 and V_3 and the output voltage is V_o.

$$V_o = -\left(\frac{10}{2}V_1 + \frac{10}{4}V_2 + \frac{10}{8}V_3\right)$$

or, $$V_o = -(5V_1 + 2.5V_2 + 1.25V_3)$$

11. Write short notes on any two of the following: $2 \times 5 = 10$

(a) MOSFET

Solution: Refer Section 1.13.

(b) Feedback amplifier

Solution: Refer Section 2.4.

(c) Universal gates

Solution: Refer Section 6.9.

(d) Operational amplifier

Solution: Refer Sections 4.2 and 4.3.

SOLVED WBUT QUESTION PAPER (2015)

ES-201

Part-I (Electrical)

GROUP – A

(Multiple-Choice-Type Questions)

1. Answer any five questions: $5 \times 1 = 5$

(i) The output voltage of a dc generator is:

(a) AC square wave (b) AC sinusoidal wave

(c) Pulsating dc (d) Pure dc

Ans: (c) Pulsating dc

(ii) In a transformer, the flux phasor:

(a) Leads the induced emf by 90°

(b) Lags the induced emf by 90°

(c) Leads the induced emf by slightly less than 90°

(d) Lags the induced emf by slightly less than 90°

Ans: (a) Leads the induced emf by 90°

(iii) When a 50 Hz transformer is operated at 400 Hz, its KVA rating is:

(a) Increased by 8 times

(b) Reduced by 8 times

(c) Unaffected

(d) Determined by load on secondary

Ans: (d) Determined by load on secondary

(iv) Two wattmeters are connected to measure the input to a balanced three phase circuit. The readings of the instruments are W_1 and W_2 respec-

tively. The currents lag by an angle θ behind the corresponding phase voltages:

(a) If $\theta = 0°$, $W_1 > W_2$

(b) If $\theta < 60°$ both W_1 and W_2 are positive

(c) If $\theta = 30°$, $W_2 > 0$

(d) If $\theta > 60°$, W_1 is positive

Ans: (b) If $\theta < 60°$ both W_1 and W_2 are positive

(v) Power developed by dc motor is maximum when the ratio of back emf and applied voltage is:

(a) Double (b) Zero (c) Unity (d) Half

Ans: (d) Half

(vi) The critical resistance of a dc generator refers to the resistance of:

(a) Load (b) Brushes

(c) Field (d) Armature

Ans: (c) Field

GROUP – B

(Short-Answer-Type Questions)

Answer any two questions: $2 \times 5 = 10$

2. Draw the exact equivalent circuit of a transformer and describe briefly the various parameters involved in it.

   Solution: Refer Article 3.9 (**Part I**).

3. Find an expression of electric field intensity and electric potential of an isolated point charge.

   Solution: Refer Article 1.7 (**Part I**).

4. Show that the power in a three phase circuit can be measured using 2 wattmeters.

   Solution: Refer Article 4.6 and Fig. 4.13 (**Part I**).

5. What is slip? Deduce a relationship between rotor current frequency and supply frequency in terms of slip of an induction motor.

   Solution: Refer Article 5.7 and 5.8 (**Part I**).

GROUP – C

(Long-Answer-Type Questions)

Answer any two questions $2 \times 10 = 20$

6. (a) Why is the open circuit test on a transformer conducted at a rated voltage? Explain. 3

Solution: (a) To get rated core loss (core loss is proportional to the square of the applied voltage) which remains constant for operation of the transformer under any load and for calculation of efficiency. Refer Article 3.16.1 (**Part I**).

(b) A 20 kVA, 2000/20 V single phase transformer has a primary resistance of 2.1 Ω and a secondary resistance of 0.02 Ω. If the total iron loss equals 200 W, find the efficiency on (i) full load and a power factor of 0.5 lagging (ii) half load and a power factor of 0.8 leading. 7

Solution: Refer problem 3.22 on Page I.3.26 (**Part I**).

7. (a) What is meant by back emf ? Explain the principle of torque production in a dc motor. 5

Solution: Refer Article 2.12 and 2.13 (**Part I**).

(b) A dc motor takes an armature current of 100 A at 230 V. The armature resistance is 0.05 Ω. The total number of lap connected armature conductors are 500 and the number of poles is 4. The flux per pole is 0.03 Wb. Find the speed and torque. 5

Solution: Refer problem number 2.37 in page I.2.38 (**Part I**).

8. (a) "A rotating field is created in a three phase induction motor when a balanced three phase ac supply is applied at the stator". Explain. 5

Solution: Article 5.6 (**Part I**).

(b) A three phase 4 kW, 400 V, 50 Hz induction motor is working at full load with an efficiency of 90% at a power factor of 0.8 lagging. Calculate (i) the input power (ii) the line current. 5

Solution: Refer problem 5.18 in Page I.5.29 (**Part I**).

9. (a) In a three phase 4 wire power distribution system, phase B is open while current through R and Y are $100\angle -30°$ and $60\angle -60°$. Find the current through the neutral connection. 4

Solution: Refer problem no. 4.22 in page I.4.21 (**Part I**).

(b) Three equal charges each of magnitude 3.5×10^{-6} C are placed at three corners of a right angled triangle of sides 3 cm, 4 cm and 5 cm. Find the force on the charge at the right angle corner. 6

Solution: Refer problem 1.1 in page I.1.14 (**Part I**).

Part-II (Electronics)

GROUP – A

(Multiple-Choice-Type Questions)

1. Answer any five questions: $5 \times 1 = 5$

(i) FET is less noisy than BJT because of:
(a) High input resistance (b) Low output resistance
(c) Voltage controlled current (d) Unipolar current
Ans: (a) High input resistance

(ii) MOSFET is a:
(a) Current controlled device
(b) Voltage controlled device
(c) Temperature controlled device
(d) None of these
Ans: (b) Voltage controlled device

(iii) Current shunt feedback is used in:
(a) Voltage amplifier (b) Current amplifier
(c) Transconductance amplifier (d) Transresistance amplifier
Ans: (b) Current amplifier

(iv) An OP-AMP has:
(a) Negligible input resistance (b) Infinitely large voltage gain
(c) Very large output impedance (d) All of these
Ans: (b) Infinitely large voltage gain

(v) The simplest form of Boolean expression is:
(a) A (b) B (c) AB (d) $A + B$
Ans: (d) $A + B$

(vi) What range of decimal values can be represented by an eight bit positive unsigned binary number:
(a) 0 to 63 (b) 0 to 127
(c) 0 to 255 (d) 0 to 511
Ans: (c) 0 to 255

GROUP – B

(Short-Answer-Type Questions)

Answer any two questions $2 \times 5 = 10$

2. (a) What is the relation among JFET parameters? 2.5
Solution: The JFET has the following parameters:
Transconductance (g_m)

Drain resistance (r_d)
Amplification factor (μ)
The relation among JFET parameter is:

$$\mu = g_m r_d$$

For derivation of the above equation, refer to Section 1.6 (**Part II**).

(b) What are the advantages of FET over BJT? 2.5

Solution: Refer to Section 1.8 (**Part II**).

3. Deriving proper expression explain the effect of positive feedback on gain, input impedance, output impedance, stability and bandwidth. 5

Solution: When the feedback voltage or current (energy) is the phase with the input signal and thus aids it, it is called positive feedback. Since both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop. Using the feedback voltage V_f to be in phase with the input signal V_{in}.

- *The effect of positive feedback on gain*: The positive feedback increases the gain of the amplifier.
- *The effect of positive feedback on input impedance*: The positive feedback increases the input impedance.
- *The effect of positive feedback on output impedance*: The positive feedback decreases the output impedance.
- *The effect of positive feedback on bandwidth*: The positive feedback decreases the bandwidth.
- *The effect of positive feedback on stability*: Distortion and instability will be increased due to positive feedback.

4. Draw the block diagram of an OP-AMP and write down the characteristics of an ideal OP-AMP. 5

Solution: Refer Sections 4.2 and 4.7 (Fig. 4.7) (**Part II**).

5. (a) Perform the following number conversion: 2.5

(i) $(11011.1010)_2 = (?)_{10}$

Solution:
$$(11011.1010)_2 = 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3}$$
$$= 16 + 8 + 0 + 2 + 1 + 0.5 + 0 + 0.125$$
$$= (27.625)_{10}$$

(ii) $(756.603)_8 = (?)_{16}$

Solution:
$$(756.603)_8 = (111\ 101\ 110.110\ 000\ 011)_2$$
$$= (1\ 1110\ \ 1110.1100\ \ 0001\ \ 1000)_2$$
$$= (1\ \text{EE.C18})_2$$

(b) Realize the Boolean expression using minimum number of NOR gates. 2.5

$$Y = AB' + A'B$$

Solution: $Y = A\bar{B} + \bar{A}B$

Then $\bar{Y} = \overline{A\bar{B} + \bar{A}B}$

$= \overline{A\bar{B}}.\overline{\bar{A}B} = (\bar{A} + B).(A + \bar{B})$

Therfore, $Y = \bar{\bar{Y}} = \overline{(\bar{A} + B).(A + \bar{B})} = \overline{(\bar{A} + B)} + \overline{(A + \bar{B})}$

The implementation of Boolean expression $Y = A\bar{B} + \bar{A}B$ using NOR gates is depicted in Fig. 1

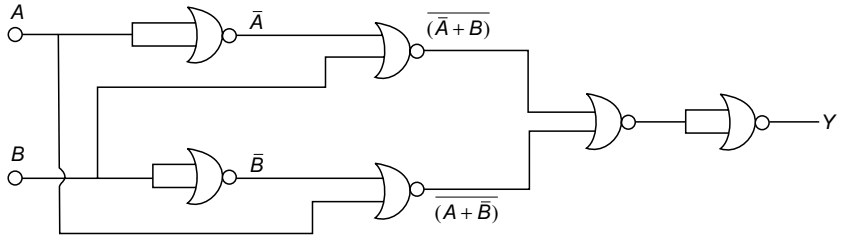


Fig. 1

GROUP – C

(Long-Answer-Type Questions)

Answer any two questions $2 \times 10 = 20$

6. (a) An *N*-channel JFET amplifier with a voltage divider biasing circuit as shown in Fig. 3 has the following parameters: $V_P = -4$ V, $I_{DSS} = 4$ mA. Calculate the value of drain current at the operating point. Verify whether the FET will operate in the pinch-off region. 7

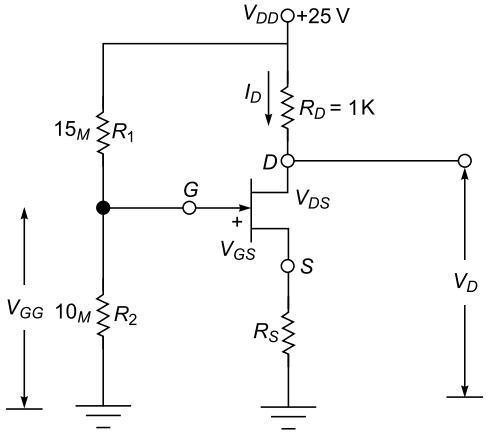


Fig. 2

Solution: Given:

$$R_1 = 15\ \text{M}\Omega$$
$$R_2 = 10\ \text{M}\Omega$$
$$R_D = 1\ \text{k}\Omega$$
$$V_{DD} = 25\ \text{V}$$
$$V_P = -4\ \text{V}$$
$$I_{DSS} = 4\ \text{mA}$$

The voltage $V_{GG} = \dfrac{R_2}{R_1 + R_2} V_{DD} = \dfrac{10}{15+10} \times 25\ \text{V} = 10\ \text{V}$

We know that $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$

$V_{GS} = V_{GG} - I_d R_S$ assume $R_s = 4\ \text{k}\Omega$
At Q-point,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or $$I_D = 4\left(1 - \frac{V_{GG} - I_D R_s}{-4}\right)^2$$

or $$I_D = 4\left(\frac{-4 - 10 + I_D \times 4}{-4}\right)^2$$

or $$4I_D = (4I_D - 14)^2 = 16I_D^2 - 112I_D + 196$$

or $$16I_D^2 - 112I_D + 196 = 0$$

Therefore, $I_D = 3.5$ mA

Since drain current $I_D = 3.5$ mA which is less than $I_{DSS} = 4$ mA, the FET will not operate in the pinch-off region.

(b) Explain the basic operation of depletion type *n* channel MOSFET with a suitable diagram. 3

Solution: Refer Section 1.15 (**Part II**).

7. (a) Obtain the closed loop gain, CMRR in dB and maximum operating frequency for the non-inverting amplifier shown in Fig. 3 whose common-mode gain is 0.003 and slew rate is 0.2 V/μs. 5

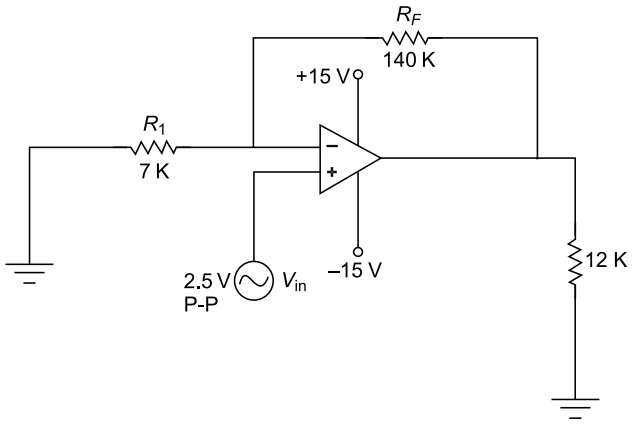


Fig. 3

Solution: Common-mode gain $A_C = 0.003$

Slew rate $SR = 0.2$ V/μs,

$$\Delta V_o = 2.5 \text{ V}$$

(i) The closed loop gain is equal to:

$$1 + \frac{R_f}{R_1} = 1 + \frac{140 \text{ k}\Omega}{7 \text{ k}\Omega} = 21$$

(ii) CMRR is equal to $\rho = \left|\frac{A_d}{A_C}\right| = \frac{21}{0.003} = 7000$

CMRR in dB is equal to:

$$20 \log \left|\frac{A_d}{A_C}\right| \text{dB} = 20 \log \left|\frac{21}{0.003}\right| = 20 \log (7000) = 70.901 \text{ dB}$$

(iii) Slew rate:

$$SR = \frac{\Delta V_o}{\Delta t} \text{ V/μs}$$

Therefore,

$$\Delta t = \frac{\Delta V_o}{SR} \text{μs} = \frac{2.5}{0.2} \text{μs} = 12.5 \text{ μs}$$

The maximum operating frequency:

$$f = \frac{1}{\Delta t} = \frac{1}{12.5 \times 10^{-6}} \text{Hz} = 80 \text{ kHz}$$

(b) What do you mean by negative feedback? 2

Solution: Refer Section 2.2.1 (**Part II**).

(c) Why is it used in designing an amplifier? 3

Solution: Refer Section 2.1 (**Part II**).

8. (a) Why NAND gate is called a universal gate? Explain with examples. 5

Solution: Refer Section 6.9 (**Part II**).

(b) A current series feedback amplifier has the following circuit parameters: $R_L = 1\ \text{k}\Omega$, $R_E = 100\ \Omega$, $R_2 = 20\ \text{k}\Omega$, $R_1 = 30\ \text{k}\Omega$, $h_{fe} = 100$. Calculate A, R_{if}, A_f and loop gain in dB. 5

Solution: Given: $R_L = 1\ \text{k}\Omega$, $R_E = 100\ \Omega$, $R_2 = 20\ \text{k}\Omega$, $R_1 = 30\ \text{k}\Omega$, $h_{fe} = 100$

$$V_{th} = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{20}{20 + 30} V_{CC} = 0.4 V_{CC}$$

$$R_{th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} V_{CC} = \frac{30 \times 20}{20 + 30} = 12\ \text{k}\Omega$$

Assume $V_{CC} = 10$ V

$$V_{th} = 0.4 \times 10 = 4\ \text{V}$$

$$I_E = (1 + h_{fe}) I_B = (1 + 100) I_B = 101 I_B$$

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E = 12000 I_B + 0.7 + 101 * 100 I_B$$

$$= 0.7 + 22100 I_B = 0.4 V_{CC}$$

$$22100 I_B = 0.4 V_{CC} - 0.7 = 0.4 \times 10 - 0.7 = 3.3\ \text{V}$$

The base current:

$$I_B = \frac{3.3}{22100} A = 0.149\ \text{mA}$$

$$I_E = 101 I_B = 101 \times 0.149\ \text{mA} = 15.049\ \text{mA}$$

AC emitter resistance:

$$r_e' = \frac{25\ \text{mV}}{15.049\ \text{mA}} = 1.66\ \Omega$$

Voltage gain without feedback $A = \frac{R_L}{r_e'} = \frac{1000}{1.66} = 602.4$

$$\beta = \frac{R_E}{R_C} = \frac{100}{1000} = \frac{1}{10}$$

$$R_{if} = R_{th} + (1 + h_{fe}) R_E = 12 \times 10^3 + (1 + 100) \times 100 = 22.1\ \text{k}\Omega$$

The voltage gain with feedback is:

$$A_f = \frac{A}{1 + \beta A} = \frac{1}{\beta} = \frac{R_C}{R_E} = \frac{R_L}{R_E} = \frac{1000}{100} = 10$$

Loop gain in dB is equal to:

$$20 \log A_f = 20 \log 10 = 20\ \text{dB}$$

9. Write short notes on any two of the following: 2×5

   (a) Slew rate
   Solution: Refer Section 4.10.8 (**Part II**).

   (b) Barkhausen criterion
   Solution: Refer Section 3.4.1 (**Part II**).

   (c) Pinch-off condition of JFET
   Solution: Refer Section 1.4 (**Part II**).

   (d) Op-amp as an integrator
   Solution: Refer Section 5.11 (**Part II**)

Output Intents

No output intents